

HP 12205A Control Store Card

Installation and Reference Manual

PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

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GENERAL INFORMATION

S	ECTION

1-1. INTRODUCTION

This manual provides general information, installation procedures, and programming information for the HP 12205A Control Store Card for the HP 1000 A900 Computers.

1-2. DESCRIPTION

The control store (CS) card provides the computer system with the internal computer hardware to develop, store, and execute user-designed microprograms. The CS card has a writable control store (WCS) bank that provides storage for up to 4096 (4k) microprogram instructions, and a PROM control store (PCS) bank for 2k microinstructions. Microprograms can be loaded into the WCS via the computer I/O system and executed by the computer processor during the microprogram development phase. Completed microprograms can then be permanently stored in PROMs and executed whenever addressed by macrocode instructions in the processor.

The CS card installs in the highest I/O-priority slot (slot 1) of the computer card cage. Card cage backplane connections provide the I/O system interface for WCS and required power, while the CS frontplane provides address, data, and control interface to the A900 sequencer card. Operation of the WCS is under program control, with both programmed I/O and direct memory access (DMA) capability.

The HP 92049A Microprogramming Package provides complete software support (in the HP RTE-A system environment) for the HP 12205A Card.

1-3. UNPACKING

If ordered separately from the computer system, inspect the CS kit shipping carton contents upon arrival for possible damage during shipment. If any kit items are damaged, contact the shipping agent immediately for claims adjustment procedures, and the nearest Hewlett-Packard Sales and Service Office for replacement of the damaged items.

1-4. CARD IDENTIFICATION

The CS card part number is located on the component side of the card. Refer to this part number in all correspondence concerning the CS card.

1-5. ADDITIONAL INFORMATION

For additional information on programming and use of the CS card, refer to the following:

- HP 1000 A900 Computer Reference Manual, part no. 02139-90001.
- HP 92049A Microprogramming Package Reference Manual, part no. 92049-90001.

1-6. EQUIPMENT SUPPLIED

The equipment supplied with the control store kit is as follows:

- Control Store Card, part no. 12205-60001.
- Control Store Frontplane, part no. 12205-60002.
- HP 12205A Control Store Card Installation and Reference Manual, part no. 12205-90001.

1-7. SPECIFICATIONS

Table 1-1 provides the specifications for the CS card.

Table 1-1. HP 12205A Control Store Card Specifications

ELECTRICAL CHARACTERISTICS

Required Power: 22.72 Watts Max.

(19.22W without PROMs)

Required Current: 3.7

3.7 Amps Max. at +5V for WCS only; add 0.7

Amps for PROMs.

0.06 Amps Max. at +12V

OPERATING TEMPERATURE

0° to +55°C (32° to 131°F)

CONTROL STORE CAPACITY

WCS:

4k words

PCS:

2k words

DMA TRANSFER RATE

Word Mode:

166k words per second

INSTALLATION

SECTION

This section provides information on setting the select code of the control store (CS) card, installing PROMs (if necessary), and installing the CS card.

2-1. SELECT CODE ASSIGNMENT

Before installing the CS card, ensure that I/O select-code switches U1S3-S8 have been set to the proper select code for the card. (See Figure 2-1.) An open switch represents a logic 1 and a closed switch a logic 0, with U1S3 as the most-significant bit. Switches U1S1 and U1S2 are not used.

2-2. PROM INSTALLATION AND BANK ADDRESS SELECT

CAUTION

STATIC SENSITIVE DEVICES. Use anti-static handling procedures when installing or removing a PROM chip.

PROM chips can be burned out if installed backwards in the PROM sockets. Ensure that all PROMs are aligned correctly before applying power to the CS card.

When installing programmed PROMs in PROM bank sockets on the CS card, ensure that the alignment notch at one end of each PROM chip pack matches up with the alignment notch on the chip socket.

If the user has installed PROMs on the CS card, it is necessary to select a bank address for the PROMs. The PROM bank address is set by switches U0201S1-S8 on the CS card, and the address must be appropriate for the microprogram addresses in the PROMs. Table 2-1 lists the address-select switch settings for each 2k module within the 32k address space of control store.

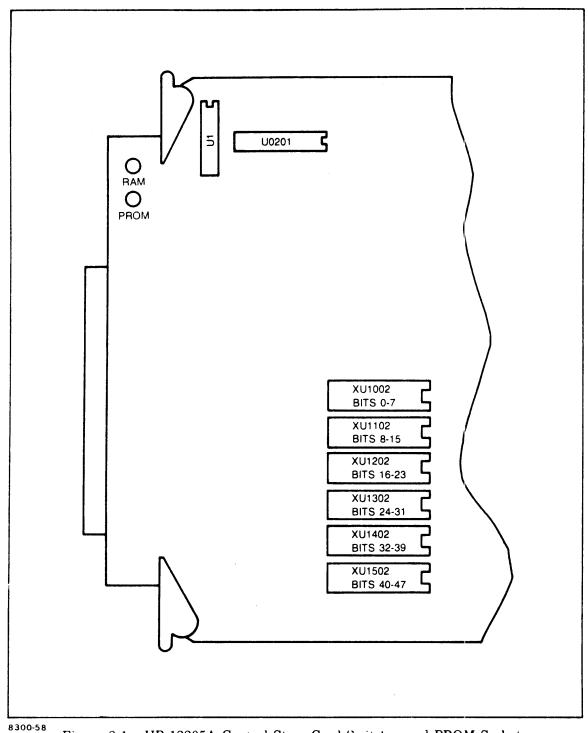


Figure 2-1. HP 12205A Control Store Card Switches and PROM Sockets

Table 2-1. PCS Address Select for 2k PROMs

MODULE	CONTROL STORE ADDRESSES				U0201 SWITCH*		
MODULE NUMBER	DECIMAL	OCTAL	HEX	\$4	201 S S5	S6	S8
0	0 - 2047	000000 - 003777	0-7FF	0	0	0	0
1	2048 - 4095	004000 - 007777	800-FFF	0	0	0	1
2	4096 - 6143	010000 - 013777	1000-17FF	0	0	1	0
3	6144 - 8191	014000 - 017777	1800-1FFF	0	0	1	1
4	8192 - 10239	020000 - 023777	2000-27FF	0	1	0	0
5	10240 - 12287	024000 - 027777	2800-2FFF	0	1	0	1
6	12288 - 14335	030000 - 033777	3000-37FF	0	1	1	0
7	14366 - 16383	034000 - 037777	3800-3FFF	0	1	1	1
8	16384 - 18431	040000 - 043777	4000-47FF	1	0	0	0
. 9	18432 - 20479	044000 - 047777	4800-4FFF	1	0	0	1
10	20480 - 22527	050000 - 053777	5000-57FF	1	0	1	0
11	22528 - 24575	054000 - 057777	5800-5FFF	1	0	1	1
12	24576 - 26623	060000 - 063777	6000-67FF	1	1	0	0
13	26624 - 28671	064000 - 067777	6800-6FFF	1	1	0	1
14	28672 - 30719	070000 - 073777	7000-77FF	1	1	1	0
15	Reserved for use by Hewlett-Packard.						

 *1 = open (up); 0 = closed (down)

Notes: Switches U0201S1-S2 must be open; and switches U0201S3 and S7 must be closed. Switch U0201S9 must be closed to enable the PCS, and open to disable the PCS. Switch U0201S10 may be set to either position (don't care).

2-3. INSTALLATION

CAUTION

Static sensitive devices. Use antistatic procedures when handling the control store card.

To install the CS card, proceed as follows:

- a. Set the computer Power switch to OFF and open the card cage.
- b. Insert the CS card (with component side to the right or facing up) into slot 1 of the card cage.

NOTE

There can be no empty card slots between the CS card, processor cards, memory cards, and any I/O cards. This is required in order to maintain the computer backplane I/O interrupt chain. Also, if the CS card is removed from slot 1 then an I/O card must be installed there to enable computer operation.

c. Connect the CS frontplane between the frontplane connectors on the the CS card and the A900 sequencer card.

NOTE

The CS frontplane, part no. 12205-60002, is not interchangeable with the memory frontplane. Be sure to use the CS frontplane when installing the CS card.

2-4. OPERATIONAL CHECKOUT

Load and run the HP 12205A diagnostic to ensure proper WCS operation. (Refer to the HP 1000 A-Series Computer Interface Diagnostic Reference Manual, part no. 24612-90004, for instructions.)

WCS PROGRAMMING CONSIDERATIONS

SECTION

This section provides general programming considerations for WCS operation of the control store (CS) card, including frontplane interface, backplane interface, direct memory access (DMA) operation, programmed I/O interface, and programming examples.

3-1. LOGICAL MODULES

The 32k control store space is logically divided into eight 4k WCS modules, and the base address of one of these modules must be programmatically assigned to the 4k WCS bank before a microprogram is loaded into the WCS bank. The assigned base address must be appropriate for the addresses in the microprogram. The module numbers and corresponding base addresses are as follows:

MODULE NUMBER	BASE ADDRESS (OCTAL)
0	00000
1	10000
2	20000
3	30000
4	40000
5	50000
6	60000
7	70000

Refer to Table 2-1 for decimal and hex equivalents.

3-2. FRONTPLANE INTERFACE

The CS frontplane provides address, data, and control signal connections between the CS card and the A900 sequencer card. Access to the frontplane for WCS operation is under program control, and is enabled only when the CS card is in the On state.

With the proper select code stored in the Global Register, frontplane access for WCS is enabled and disabled by the following backplane I/O instructions (refer to paragraph 3-3):

OTA 32B	bits 14 and 13 of A set to 1 Enables WCS access to frontplane
OTA 32B	bits 14 and 13 of A cleared to 0 Disables WCS access to frontplane

When the CS card is in the On state, WCS is enabled, and the microinstruction being addressed is located in WCS, then the WCS disables the PCS and the main control store on the Sequencer card. The LED labeled RAM on the CS card is lit when the WCS bank is enabled; the LED labeled PROM is lit when the PCS bank is enabled. (See Figure 2-1.)

3-3. BACKPLANE INTERFACE

Backplane interface for WCS operation is provided through standard I/O Master logic, and is under program control. (Refer to the HP 1000 L-Series Computer I/O Interfacing Guide, part no. 02103-90005, for complete information on the I/O Master.) Backplane access to the CS card I/O Master logic and card contents requires that the CS card be in the Off state and (with the exception of the CLC 0 instruction) that the Global Register be loaded with the card select code and be enabled.

The following is a summary of I/O instructions executed on the CS card via the computer backplane.

OTA/B 30B	Writes data to the WCS RAMs
LIA/B 30B	Reads data from WCS RAMs
OTA/B 31B	Sets WCS module number (0-7) in the three least significant bits
OTA/B 31B	Writes WCS data RAM address for programmed I/O transfer
LIA/B 31B	Reads status of both CS card and WCS bank and address
OTA/B 32B	Enables CS card and WCS (to frontplane access)

3-4. DIRECT MEMORY ACCESS (DMA) OPERATION

Direct memory access (DMA) operations transfer data to and from the WCS bank of the CS card via the standard I/O system, and operate with the following restrictions on DMA Control Word 1. (Refer to the HP 1000 A900 Computer Reference Manual, part no. 02139-90001, for information on DMA control words).

- Bit 14 DVCMD; must be set.
- Bit 13 BYTE; must be clear.
- Bit 8 AUTO; must be clear for input transfer, set for output.

3-5. PROGRAMMED I/O INTERFACE

User interface to the WCS on the CS card is provided by the backplane I/O system and software. Backplane access to WCS is enabled only when the CS card is in the Off state, the Global Register contains the card select code, and the Global Register is enabled.

The following provides a list of I/O applications with corresponding I/O instructions and required bit status:

Turns CS card On

```
LDA 20000B sets bit 13 of A to 1
OTA 31B sets bit 13
OTA 32B turns on CS card
```

Turns CS card Off

LDA 0	clears bit 13 of A to 0
OTA 31B	clears bit 13
OTA 32B	turns off CS card

Enables WCS and sets WCS base address

LDA MODUL puts the WCS module number (0-7) into A

IOR 60000B sets bits 14 and 13 of A to 1

OTA 31B sets bits 14 and 13
OTA 32B enables WCS

Disables WCS

LDA 0 sets bits 14 and 13 of A to 0

OTA 31B clears bits 14 and 13

OTA 32B disables WCS

Reads status of CS card

LIA 31B sign bit of A is 1 = CS card On; 0 = CS Off

bit 14 of A is 1 = WCS enabled; 0 = WCS disabled

Address WCS bank

OTA/B 31B A/B bits 11-0 must contain WCS bank address

Write data to WCS RAMs

OTA/B 30B A/B contains 1/3 of microword (16 bits).

Bits 32 through 47 are written first, then bits 16 through 31, and then

bits 0 through 15.

Read data from WCS RAMs

LIA/B 30B 1/3 of microword returned in A/B (16 bits).

Bits 32 through 47 are read first, then bits 16 through 31, and then bits

0 through 15.

3-6. WCS PROGRAMMING EXAMPLES

In the programming examples in the following paragraphs, operand definitions are as follows:

200 SELCD — Select Code of CS card.

2 ° 2 COUNT — Complement of number of words to be transferred.

203 AAAAA — Address bits.

XXXXX — Can be any value, user defined.

20) ccccc — COUNT value.

204: 6 RDATx - Data.

३००: २ WDATx — Data.

MODUL — WCS module number (0-7).

3-7. CONTROL STORE OPERATION (CS CARD TURNED OFF)

Enable WCS and Set WCS Base Address

Disable WCS

LDA SELCD Load and enbale Global Register

OTA 2,C

.
.
.
.
.
.
LDA OB Disable WCS

OTA 31B

Read Status of WCS

LDA SELCD
Load and enable Global Register

OTA 2,C

.
.
.
LIA 31B
Sign bit of A is 1 = CS card On; 0 =

Sign bit of A is 1 = CS card On; 0 = CS Off. Bit 14 of A is 1 = WCS enabled; 0 = WCS disabled

Address and Load WCS RAMs

OTA 32B

	060200	LDA SELCD	Load and enable Global Register
′	103602	OTA 2,C	A the manches of missessed to be transformed
			Load the number of microwords to be transferred,
3	070202	STA COUNT	and initialize loop counter
		•	
		•	
	, , ,	•	
	060203	LDA 00AAAAB	RAM address in A
ŝ	103621	OTA 31B	Output address
6	Jy ⊌ ≧ ⊇ ~LOOP	LDA RDATO	RAM data bits 0-15
7	102630	OTA 30B	Output data
110	103230	STC 30B	Go to bits 16-31
ı	060205	LDA RDAT1	RAM data bits 16-31
2	10263.0	OTA 30B	Output data
ĵ		STC 30B	Go to bits 32-47
المشا	7 3 10 7 1 3	LDA RDAT2	RAM data bits 32-47
5	103630	OTA 30B	Output data
6	1 3 5 7 2 3	STC 30B	Increment address to next microword
7	034202	ISZ COUNT	
	630 100	JMP LOOP	
	157732	CLC 30,C	Clear Flag 30

Address and Read WCS RAMs

130 065200	LDA SELCD	Load and enable Global Register
1 103602	OTA 2,C	
12 060201	LDA CCCCC	Load the number of microwords to be transferred,
3 070202	STA COUNT	and initialize loop counter
	•	
	•	
134 660203	•	
- 9 102631	LDA 00AAAAB	RAM address in A
9 10 = 6 91	OTA 31B	Output address
6 102530LOOP	LIA 30B	Read RAM data
7 270300	STA WDATO	Store data bits 0-15 in memory
140 102730	STC 30B	Go to bits 16-31
1 102530	LIA 30B	Read RAM data
2 0703 01	STA WDAT1	Store data bits 16-31 in memory
3, 102730	STC 30B	Go to bits 32-47
4 1025 30	LIA 30B	Read RAM data
5 070302	STA WDAT2	Store data bits 32-47 in memory
6 102730	STC 30B	Increment address to next microword
7 034202	ISZ COUNT	
150 024136	JMP LOOP	
1 107730	CLC 30B,C	Clear Flag 30

3-8. DMA OPERATION (CS CARD TURNED OFF)

Address and Load WCS RAMs

LDA SELCD OTA 2,C	Load and enable Global Register
LDA BUFDW OTA 20B STC 20B,C SFS 21B JMP +-1 CLC 30B,C	Set up DMA self-configuration
DEF ++1 DCT 0414XX DCT 00AAAA DEF MEMAD DCT CCCCC	Control Word 1 Address in RAM Memory address of data Three times the number of microwords to be transferred

WCS Programming Considerations

Address and Read WCS RAMs

	LDA SELCD OTA 2,C	Load and enable Global Register
	•	
	LDA BUFDR	Set up DMA self-configuration
	OTA 20B	Set up DMA sen-configuration
	STC 20B	
	SFS 21B	
	JMP +-1	
	CLC 30B	
	•	
	•	
BUEDR	DEF +-1	
20. DK	DCT 0412XX	Control Word 1
	DCT 00AAAA	Data RAM address
	DEF MEMAD	Address to store data
	ост ссссс	Three times the number of microwords to be transferred

NOTE

Bit 6 of Control Word 1 is user definable for WCS operations (can be any value).

As shown in the preceding examples, a subroutine can be written to perform DMA self-configuration for all WCS access operations, with parameters passed in order to determine read/write, data RAM, and other variables.

READER COMMENT SHEET

HP 12205A CONTROL STORE CARD Installation and Reference Manual

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