ABSOLUTE BINARY PROGRAM 12560-16001
DATE CODE 1540

12560A DIGITAL PLOTTER INTERFACE DIAGNOSTIC

reference manual

For HP 2100 Series Computers

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SECTION I
INTRODUCTION

1-1. GENERAL

This diagnostic provides go/no-go indications to evaluate performance of the HP 12560A Digital Plotter Interface Kit. The test is run based on the assumption that the computer and plotter are in proper operating condition. The basic I/O portion of the card and the command channel circuits are tested. A troubleshooting section of the diagnostic enables the operator to select individual commands for testing.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. An HP 2100 Series Computer with a minimum 4K memory.

b. An HP 12560A Digital Plotter Interface Kit.

c. An HP 2792A (Calcomp 563) or HP 2791A (Calcomp 565) Digital Plotter.

d. A teleprinter (console device) for message reporting.

e. A loading device for loading the diagnostic program.

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator (part numbers below) is used for equipment configuration and as a console device driver.

Binary object tape	Part No. 24296-60001
Manual	Part No. 02100-90157

b. HP 12560A Calcomp Plotter Interface Diagnostic binary object tape, Part No. 12560-16001.

The diagnostic serial number (DSN) is contained in memory location 126 (octal) of the program. The DSN for this diagnostic is 107000 (octal).

All addresses, halt codes, and select codes mentioned in this manual are in octal unless specifically stated otherwise.

SECTION II
PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program contains a control and initialization section, seven tests, and Pseudo Operator Design. The initialization and control section prepares the diagnostic by accepting the select code and option required by the tests.

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device for operator information then executes the tests according to the options selected on the Switch Register by the operator. The control section mainly checks Switch Register bits 15, 13 and 12.

The program also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 10 is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed.

The operator has the capability to select his own test or sequence of tests with the help of bit 9 in the Switch Register. Paragraph 3-2 outlines the test selection.

2-3. MESSAGE REPORTING

There are two types of messages; error and information. Error messages are used to inform the operator when the interface fails to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operation related to the function of the unit. In this case, an associated halt will occur to allow the operator time to perform the function. The operator must then press RUN. If a console device is used, the printed message will be preceded by the letter E (error) or the letter H (information) and a number (in octal). The number is also related to

the halt code when a console device is not available. Examples of error and information messages are as follows:

Example - Error with Halt
Message: E030 FLAG DID NOT SET
Halt code: 102030

Example - Information with halt
Message: H024 PRESS PRESET (EXT & INT), RUN
Halt code: 102024

Example - Information only
Message: H025 BI-O COMPLETE
Halt code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by setting Switch Register bit 10. Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-O). When Switch Register bit 12 is set, the tests that are selected will be repeated. All operator intervention will be suppressed.

2-4. DIAGNOSTIC LIMITATIONS

The interface capability for receiving, passing, and denying priority (priority string logic) is not completely checked by this diagnostic. If the interface does not receive priority (i.e., PRH from the next lower select code) an error E014 NO INT will occur. To check this, remove an interface of a lower select code and run the Basic I/O test. The above mentioned error should occur. Checking the interface ability to pass or deny priority is beyond the scope of this diagnostic.

This diagnostic verifies only the interface kit not the plotter. However the routines furnished in the diagnostic may be used as a troubleshooting aid for the plotter.

SECTION III
OPERATING PROCEDURE

3-1. RUNNING THE DIAGNOSTIC

A flowchart to aid in running the diagnostic is provided in figure 3-1. Ensure that the pen writes before starting the diagnostic. If a paper tape dump is desired refer to the Diagnostic Configurator manual, part no. 02100-90157.

At the completion of each pass of the diagnostic, the pass count is output to the console for operator information. If Switch Register bit 12 was not selected, the computer will halt with 102077 in Memory Data Register (T-register). At this point, the A-register contains the pass count. To run another pass, the operator need only to press RUN. Bit 12, if set, is used to loop on the diagnostic; bit 13 is used to loop on a given test specified in table 3-3; and bit 15, if set, will halt the computer at the completion of a test.

If a trap cell halt occurs (106077), the user must determine the cause of the interrupt or transfer of control to the location in the M-register. The program may need to be reloaded to continue.

When a halt occurs and/or a message is printed on the console device, the operator must refer to table 4-2 for the meaning of the halt.

NOTE

For Pseudo Operator Design instruction refer to paragraph 4-6.

3-2. TEST SELECTION BY OPERATOR

The control portion of the program allows the operator the option to select a test or sequence of tests to be run. The operator sets Switch Register bit 9 to indicate that he wants to make a selection and presses RUN. The computer will come to a halt 102075 to indicate it is ready for the selection. If the program is running, the test in progress will be completed and then the program will halt. Now the operator loads the A-register with the tests desired. Bit 0 of the A-register represents Test 00, bit 1 represents Test 01, and so on up to bit 4 which represents Test 04. The operator must then clear Switch Register bit 9 and press RUN. The operator-selected test(s) will then be run. If the operator clears all bits in the A-register, then all tests defined in table 3-3 will be executed (except Test 04, Pseudo Opdesign).

3-3. RESTARTING

The program may be restarted by setting the P-register to 2000, loading S-register with desired diagnostic option per table 3-2 and pressing PRESET (EXT, INT), RUN.

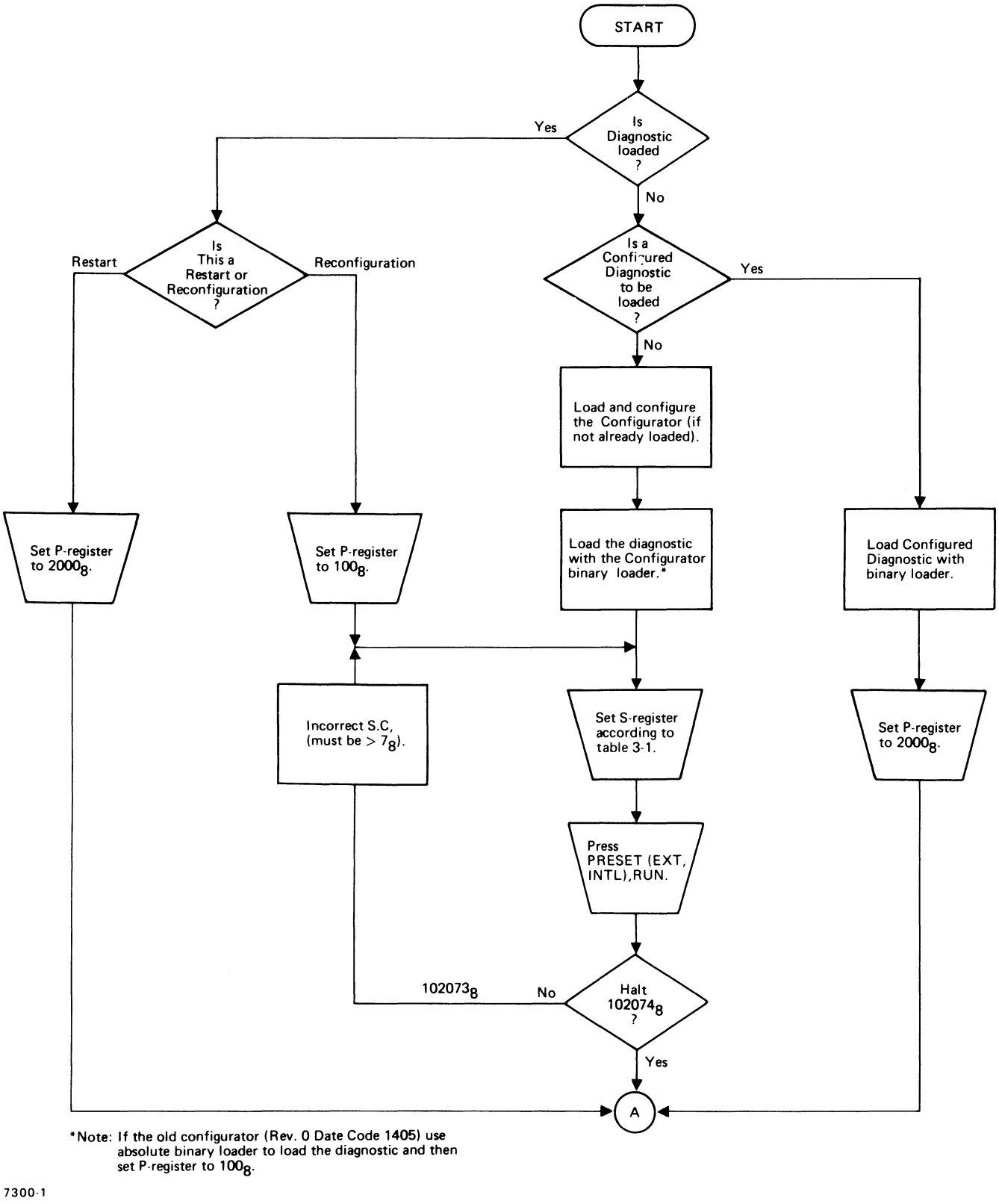

Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

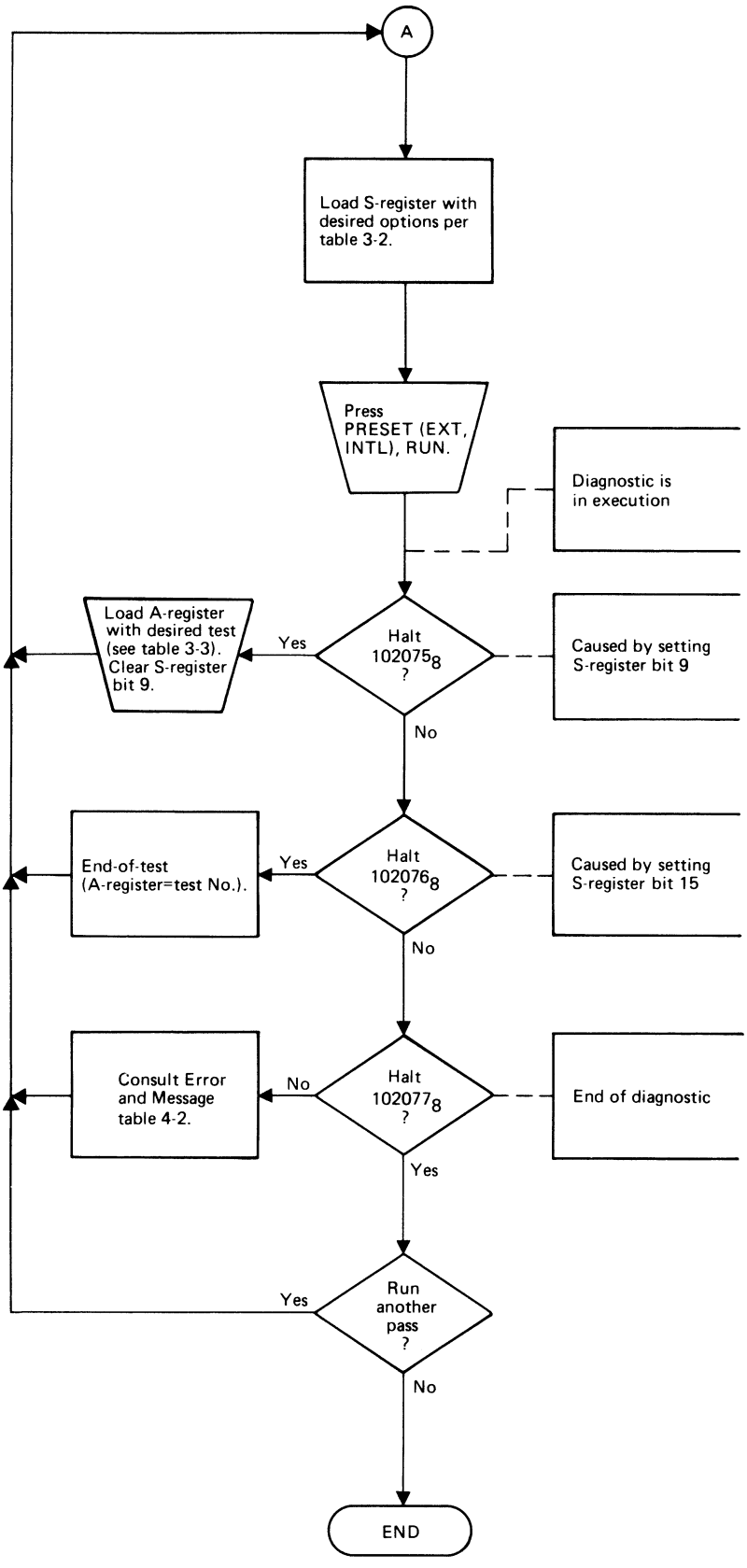

Figure 3-1. Operating Procedure Flowchart (2 of 2).

Table 3-1. Hardware Select Code and Options

BITS	MEANING
5-0	Select Code of Plotter Interface
14	Set if the plotter being tested has a metric stepper motor.
15	Set if the plotter being tested is an HP 2792A (the large plotter).

Table 3-2. Switch Register Options

BIT	MEANING IF SET
0	Reserved }
1	Reserved
2	Reserved
3	Reserved } Pseudo Operator Design, refer to paragraph 4-6.
4	Reserved
5	Reserved
6	Reserved }
7	
8	Suppress tests requiring operator intervention (Basic I/O).
9	Abort current diagnostic execution and halt (102075); user may specify a new group of tests in the A-register (see table **3-3**) clear bit 9 of the Switch Register and then press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teletype is not present. Also, those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

Table 3-3. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	Test 00 BI-O Test
1	Test 01 One Shot Test
2	Test 02 Octagon Test (decreasing)
3	Test 03 Octagon Test (over draw)
4	Test 04 Pseudo Opdesign
5-15	Reserved
B-Register	Reserved

SECTION IV
DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Refer to table 4-2 for additional details on the content of each test.

4-2. BASIC I/O TEST 0 E000-E026

Subtest 1 - Checks the ability to clear, set, and test the interrupt system. The following instruction combinations are tested:

```
CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - SFC 0
STF 0 - SFS 0
```

Errors in the above sequences produce error messages E000-E003 as shown in table 4-2.

Subtest 2 - Checks the ability to clear, set, and test the interface flag. The following instruction combinations are tested:

```
CLF CH - SFC CH
CLF CH - SFS CH
STF CH - SFC CH
STF CH - SFS CH
```

Errors in the above sequences produce error messages E005-E010 as shown in table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the Flag and Control set on the interface and the interrupt system off. The sequence of instructions is shown below:

```
STF 0
STF CH
STC CH
CLF 0
```

The CLF 0 instruction should inhibit an interrupt from occurring. Error message E004 occurs if CLF 0 fails.

Subtest 4 - Checks that the Flag of the interface under test is not set when all other select code Flags are set. Error message E011 occurs if a Flag is set incorrectly.

Subtest 5 - Checks the ability of the interface to interrupt. With the Flag and Control set and the interrupt system on, there should be an interrupt on channel CH; if not, error message E014 occurs. Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority-affecting instructions are executed. The following instructions are used to check the hold off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and E015 will occur if the hold-off fails. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if an interrupt does occur. Checks that no instruction was missed during the interrupt (E026 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the CH Control and Flag set, there is no interrupt following a CLC CH instruction. The following sequence of instructions is used:

```
STC CH
STF CH
STF 0
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message E016 will occur

Subtest 7 - Checks that the CLC 0 instruction inhibits interrupts when the CH Control and Flag are set. The following sequence of instructions is used.

```
CLF CH
STC CH
STF CH
STF 0
CLC 0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

Subtest 8 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) switches on the operator panel performs the following actions:

1. Sets interface Flag (EXTERNAL).
2. Clears Control (EXTERNAL).
3. Turns off the interrupt system (INTERNAL).
4. Clears the I/O data lines (EXTERNAL).
5. Clears the data register in the interface (INTERNAL).

4-3. ONE-SHOT TEST 01

This routine checks the two one shots on the interface board. The 2.9 (4.5) Millisecond One Shot is used for direction and pen-up commands to allow the plotter time to respond before the computer outputs another command. The 60 Millisecond One Shot is used when a pen-down command is given. The pen-down time is longer because the pen is not under magnetic force when lowered. The time test tolerances are 2.5 to 3.5 (4.0 to 5.0) ms for the 2.9 (4.5) Millisecond One Shot and 50 to 70 ms for the 60 Millisecond One Shot. The numbers in parenthesis represent the one shot time if jumper W1 on the interface is in the "A" position.

4-4. OCTAGON PATTERN TEST 02

This routine draws nine concentric decreasing octagons. The octagons change between solid, blank, and dashed (in that order). This is mainly used to verify each command and pen control (see figure 4-1). The pen-down to pen-up ratio for the dashed octagons is 1:1.

4-5. OCTAGON PATTERN TEST 03

This routine draws nine octagons decreasing in size and with the same origin. This is used to check the stepper motor and control to ensure that there is no drifting (see figure 4-1.)

4-6. PSEUDO OPERATOR DESIGN TEST 04

This routine is for troubleshooting the interface and/or plotter. It must be optionally selected (refer to operator selection paragraph 3-2).

When the section is entered the program will output the message "H035 MAKE SWR SELECTION FOR OPDESIGN" and then halt 102035. At this point the operator should make a command selection from table 4-1 and press RUN. The program will output the command and halt again 102035 (if SWR Bit 6 is clear). If the operator has selected bit 6, the program will continue to output the chosen commands until bit is cleared.

To exit opdesign, clear Switch Register bits 6-0.

Table 4-1. Pseudo Opdesign Selection

BIT	MEANING	
0	Drum down +X AXIS (vertical up)	If both bits are set, drum down command overrides.
1	Drum up −X AXIS (vertical down)	
2	Carriage left +Y AXIS (horizontal left)	If both bits are set, carriage left command overrides.
3	Carriage right −Y AXIS (horizontal right)	
4	Pen-up	If both bits are set, pen-down command overrides.
5	Pen-down	
6	Loop on selection	

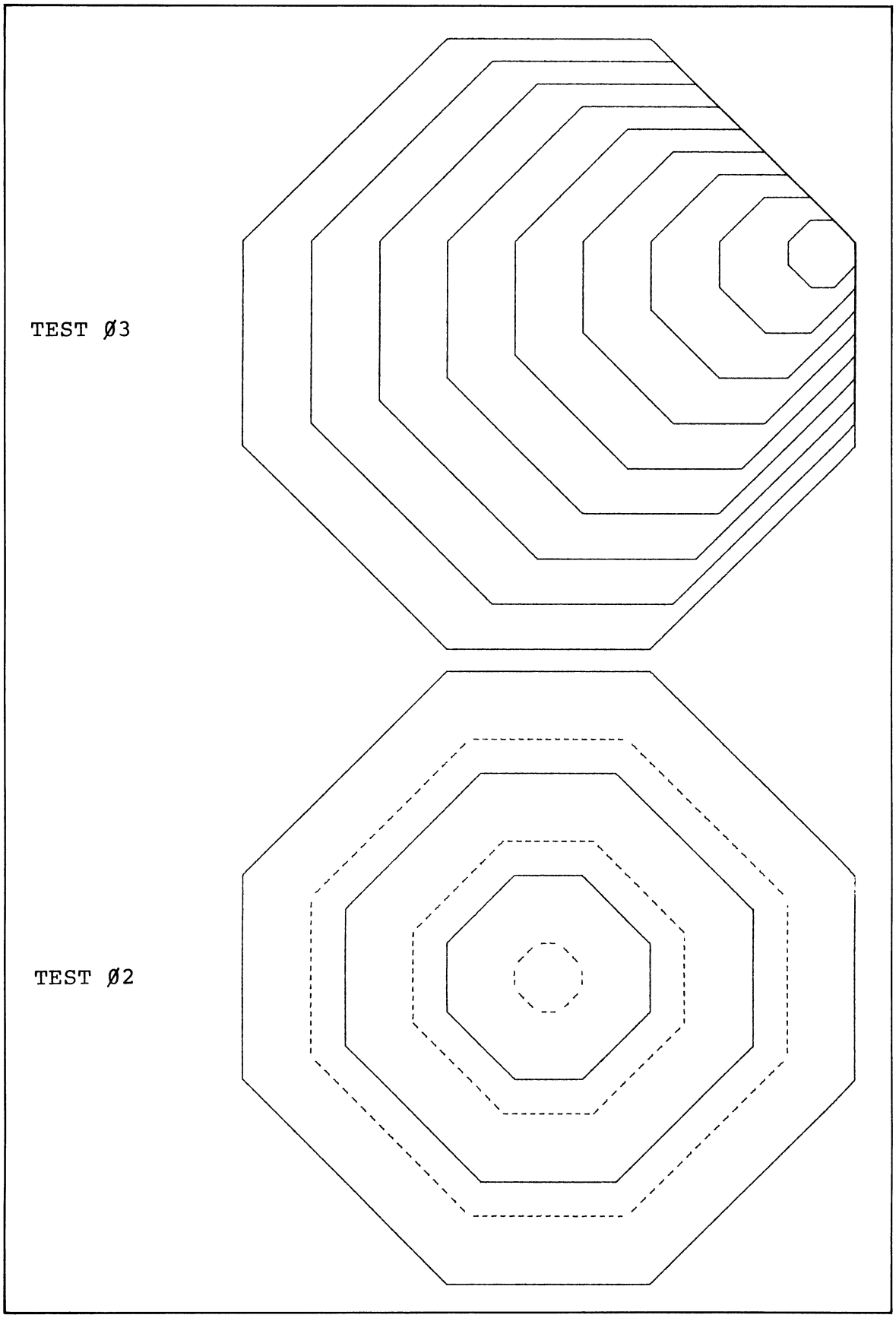

Figure 4-1. Octagon Test Patterns

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	SECTION	MESSAGE	COMMENTS
None	Test Control	CAL COMP PLOTTER DIAGNOSTIC	Introductory message.
None	Test Control	TEST XX	Information message before error message. (XX = test number). Message occurs only once within a test but is suppressed for any subsequent messages within the same test.
102000	Test 0	E000 CLF 0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102001	Test 0	E001 CLF 0-SFS 0 ERROR	CLF/SFS 0 combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102002	Test 0	E002 STF 0-SFC 0 ERROR	STF/SFC 0 combination failed. STF did not set Flag or SFC caused skip with Flag set.
102003	Test 0	E003 STF 0-SFS 0 ERROR	STS/SFS 0 combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102004	Test 0	E004 CLF 0 DID NOT INHIBIT INT	With card Flag and Control set, CLF 0 did not turn off interrupt system.
102005	Test 0	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear Flag or SFC caused no skip with Flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear Flag or SFS caused skip with Flag clear.
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set Flag or SFC caused skip with Flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STS/SFS CH combination failed. STF did not set Flag or SFS caused no skip with Flag set.
102011	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. A-register contains XX (octal) where XX = select code that caused that card Flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupted a second time after initial interrupt was processed.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102014	Test 0	E014 NO INT	No interrupt occurred with card Flag and Control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC CH ERROR	CLH CH did not clear card Control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear Control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card Flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear Control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT), RUN	Press PRESET (EXTERNAL, INTERNAL) and RUN.
102025	Test 0	H025 BI-O COMP	Basic I/O Test complete.
102026	Test 0	E026 INT EXECUTION ERROR	Installations being executed prior to and just after interrupt did not execute correctly.
102030	Tests 1-4	E030 FLAG DID NOT SET	Interface failed to respond to an STC SC,C command within 100 ms. A-register = output command.
102031	Test 1	E031 2.9 (4.5) MS ONE-SHOT TOO SHORT	Refer to paragraph **4-3**.
102032	Test 1	E032 2.9 (4.5) MS ONE-SHOT TOO LONG	Refer to paragraph **4-3**.
102033	Test 1	E033 60 MS ONE-SHOT TOO SHORT	Refer to paragraph **4-3**.
102034	Test 1	E034 60 MS ONE-SHOT TOO LONG	Refer to paragraph **4-3**.
102035	Test 4	H035 MAKE SWR SELECTION FOR OPDESIGN	Refer to paragraph 4-6.

Table 4-2. Error Information Messages and Halt Codes (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102073	Configuration	None	I/O select code entered at configuration is invalid. Must be greater than 7 (octal). Re-enter a valid select code and press RUN.
102074	Configuration	None	Select code input okay, make Switch register selection (see table 3-2), and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter in A-register the desired group of tests to be executed, clear bit 9 in Switch Register and press RUN. (See tables 3-1 and 3-2.)
102076	Test Control	None	End-of-test halt resulting from Switch Register bit 15 being set (A-register has the test number). To continue, press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. Register options may be changed (A-register has the pass count). To continue press RUN.
106077	Test Control	None	Halt stored in location 2-77 (octal) to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.