PAPER TAPE NO. 12989-16001

HP12989A
CARD READER PUNCH SUBSYSTEM
DIAGNOSTIC

for

hp-2894A CARD READER PUNCH/
12930A-003 UNIVERSAL INTERFACE KIT

reference manual

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I. INTRODUCTION

The purpose of this diagnostic is to test the proper operation of the HP 2894A Card Reader Punch (Decision Data) interacting with either an HP 2100A/S or an HP 21MX computer via an HP 12930A-003 Universal Interface Kit. The program is designed to test primarily the Card Reader Punch although it confirms some basic functions of the interface. It is assumed that the on-line performance test has been performed in accordance with the instructions provided in Section VI of the HP 12989A Card Reader Punch Subsystem Operating and Reference Manual, part no. 12989-90002. At this point, more extensive diagnostic testing can be performed using the Card Reader Punch Subsystem Diagnostic binary tape, part no. 12989-16001 and the information provided in this manual or the performance of the interface can be diagnosed using the Diagnostic Test Hood, part no. 12930-90003; Universal Interface Diagnostic binary tape, part no. 24289-60001; and the information provided in the HP 12930A Universal Interface Test manual, part no. 12930-90004.

II. REQUIRED HARDWARE

A) HP 2100A/S or HP 21MX Computer with at least 8K of memory
B) Device for loading diagnostic (e.g., paper tape reader)
C) Teleprinter for error reporting (optional, but strongly recommended)
D) HP 2894A Card Reader Punch (device being tested)
E) HP 12930A-003 Universal Interface Kit

III. SOFTWARE

The diagnostic is an absolute program written in HP Assembly Language which will run on either an HP 2100A/S or HP 21MX computer. The Diagnostic Configurator (HP Product No. 24296A) is used for system configuration and for providing the necessary I/O communication programs and general utility routines.

IV. FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

The HP 12930A-003 Universal Interface Kit provides a means of bidirectional control and data transfer between an HP 2100A/S or HP 21MX computer and the HP 2894A Card Reader Punch. Two channels are required for the interface, the data channel (with higher priority and lower select code) and the command channel (with lower priority and the higher select code). The individual control, data, and status bits associated with each channel are shown in Table III.

The diagnostic program provides twelve (12) standard tests (Test 0 through Test 11) and a special test procedure called the Operator Design (Test 12). A standard diagnostic run includes execution of all standard tests. In addition, each test or any subset of tests may be selected individually through the test selection phase of the program (see Section VID). The Operator Design, which is not a standard test, may be entered by selecting Test 12. Other options, such as looping on individual test, suppressing messages, etc., may also be made through the switch register. If the Operator Design is entered, the switch register bits 0 through 4 are used to specify a required order. Tables I and IV explain function of individual switch register bits in more detail. Normally, all the tests require operator intervention. Some tests require a visual check of printed data to confirm the proper operation of the print station. Operator intervention may be minimized by using the switch register options except for the requirements to load input hoppers and to unload stackers (see Section IX and Table I).

V. LIMITATIONS

This diagnostic is designed to test the Card Reader Punch by the following two methods of data transfer:

- "Wait-for-flag" method
- Interrupt method

The DMA method is not used. If the DMA circuitry of the interface is to be tested, HP 12930A Universal Interface Test (HP Product No. 24289A) should be used.

VI. PROGRAM ORGNAIZATION

The description of the program organization is divided into four parts:

- Configuration
- Test Control and Execution
- Message Reporting
- Test Selection

A. CONFIGURATION

The configuration section performs the following functions:

1) Turns off the interrupt system (CLC 0,C) and clears the system.
2) Loads the data channel (higher priority) I/O select code from the switch register and checks that the code is greater than 7_8. If it is less than or equal to 7_8 a halt (102073) will occur. The operator must enter a valid select code greater than 7_8. If it is a valid select code, a halt (102074) will occur.
3) Configures Data Channel and Command Channel I/O instructions used by the diagnostic.

The configuration section may be executed by starting the program at location 100_8. The configuration section may be bypassed by starting the program at 2000_8. At the completion of the configuration section halt 102074 will occur to allow the operator time to enter program option bits via the switch register. If the program is started at location 2000_8 the program is at the same point as if the program had been continued from the 102074 halt or from halt 102075 generated by setting switch 9.

B. TEST CONTROL AND EXECUTION

The control sequence for the diagnostic allows the selection and execution of up to 32 tests (the first thirteen are used in this diagnostic, Test 0 through Test 11 are standard tests, Test 12 is Operator Design).

Tests are written in subroutine form. The subroutines are placed in a contiguous manner in memory. To execute the individual diagnostic test subroutines, the control program uses a table of pointers to determine the test location.

Since the diagnostic is switch register controlled, program option bits are monitored by the control program to determine operator changes in diagnostic execution. Switch register bits 9, 12, 13 and 15 are checked by the control program. Bit 8 and 12 is checked during basic I/O testing by the control program and also by tests 2 through 11.

The test control and execution section performs the following functions:

1) Turns off the interrupt system (CLC 0,C) and clears the system.
2) Outputs an introductory message preceded by a carriage return/line feed. No halt will occur after the message is output.
3) Checks switch register bit 9 to initiate changes in the sequence of tests to be performed with bit 0 of the A register corresponding to test 0, bit 12 to test 12.

   a) If bit 9 is not set, a default set of all the twelve standard tests is executed. The octal constant which defines the default set of tests is stored in location 143_8 as shown below:

      143_8 OCT 007777

   b) If bit 9 is set a halt (102075) will occur to allow the operator time to change the tests to be executed. If no tests are selected at this point the program will use the default set of tests defined by location 143_8.

      Bit 9 must be reset after entering changes to the A register; otherwise halt 102075 will occur to request new information on program selection. The A register will contain the previously selected tests from the original halt.

4) Puts halts in locations $2\text{-}77_8$. The halts are of the form 106077. Before the execution of each test the trap cells will be restored to halt 106077.
5) Checks A register test selection to determine if a test is to be run. If yes, it runs tests; if no, it checks next bit and continues to search for a test selected.

6) After running a selected test, switch register bits 15, 9 and 13 are checked in that order for operator changes to program running.

   a) Bit 15 initiates a halt at the end of individual tests. The halt will be of the form 102076. The A register will contain the test number in octal.

   b) Bit 9 initiates a return to user test selection. A halt (102075) will occur with the A register containing the last selected set of tests.

   c) Bit 13 initiates a loop on the current test being executed.

7) At the completion of all selected tests the following occurs:

   a) Switch register bit 12 is checked to determine if a loop on all tests is being requested.

   b) Prints the message "PASS XXXXXX" (if teleprinter present) and halts (102077) if bit 12 is not set. The A register will contain pass count in octal at halt 102077. After the 102077 halt, the user may change the tests to be executed by setting bit 9.

   c) Prints the message "PASS XXXXXX" (if teleprinter present) and continues program execution if bit 12 is set. The pass count is an octal number and is reset whenever program is restarted from location 2000_8. Also those tests requiring extensive operator intervention will be suppressed if bit 8 or 12 is set.

Note: The test control and execution section begins at location 2000_8 in memory. The configuration section is bypassed by starting the program at this location. Switch register options are shown in Table I.

C. MESSAGE REPORTING

There are two types of messages, error and information. Error messages are used to inform the operator of a failure of the Card Reader Punch to respond to a given command or sequence of commands. Information messages are used to inform the operator of the progress of the diagnostic

or instruct the operator to perform some operation related to the device function. In this case, an associated halt will occur to allow the operator time to perform the operation; the operator must then press RUN.

If a console device is used, the printed message will be preceded by an "E" (error) or "H" (information) and a number (in octal). The number is also related to the halt code when a console device is not available. It should be noted that some information messages are not preceeded by "H" (e.g., the introductory message). Refer to Table IIb for specific details of error and information messages.

Some error messages are indicated by an asterisk (*) (the asterisk is a part of the message and is also printed on the teleprinter). After an error message with the asterisk is given and the corresponding halt occurs, the operator may optionally obtain current status of the Card Reader Punch. If the switch register bit 7 is set and RUN is pressed, the status is reported by the message H123 followed by a halt (10623). The diagnostic then may be continued by pressing RUN again. During standard tests, the message H123 will not be normally given if the switch register bit 7 is not set.

Error messages can be suppressed by setting the switch register bit 11. Switch register bit 14 is used to suppress error halts and a halt after the message H123. Information messages can be suppressed by setting the switch register bit 10.

Since the same error message may be given during execution of several different tests, the error messages are preceded by the message "TEST XX" (XX = test number in octal). This message occurs only for the first error within a test but is suppressed for any subsequent error messages within the same test.

Numerous information messages instruct the operator to press STOP, START, and RUN. Note that the STOP and START buttons are located on the front panel of the Card Reader Punch while the RUN button is located on the front panel of the computer.

Some information messages contain the request "CLEAR DEVICE". The operator clears the device by switching a two-position OFF-LINE/ON-LINE toggle switch from OFF-LINE to ON-LINE position (transition from OFF-LINE to ON-LINE is necessary).

D. TEST SELECTION

The control portion of the program provides for the operator to select a particular test or a sequence of tests to be run. The operator selects switch register bit 9 to indicate he is ready to make a new test sequence selection. If the program is running, current test will be completed and then the halt 102075 will occur. Now the operator sets the A register bits corresponding to the desired tests. The A register bit 0 represents Test 0 (Basic I/O for data channel), bit 1 represents Test 1 (Basic I/O for command channel), and so on up to bit 11 which represents Test 11. The Operator Design, which is considered to be Test 12, is entered by setting bit 12. The operator must then clear switch register bit 9 and press RUN. The selected tests will then be run. If the operator clears all bits or makes no selection, the standard sequence of tests (Test 0 through 11) will be run. Refer to Table VI for a list of test numbers and their corresponding A register settings.

VII. DESCRIPTION OF TESTS

The diagnostic provides twelve (12) standard tests (Test 0 through 11) and a special test procedure called the Operator Design (Test 12). Each standard test consists of two or more subtests. Tests 0 and 1 are commonly referred to as basic I/O tests. The remaining tests verify the proper operation of the Card Reader Punch. The Operator Design is described in Section VIII. The action of each standard test is outlined below:

TEST 0 - Basic I/O test for data channel

Note: CH = data channel select code

SUBTEST 1 Checks the ability to clear, set and test the interrupt system. The following instruction combinations are tested:

CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - SFC 0
STF 0 - SFS 0

Errors in the above sequences produce error messages E000-E003 as shown in Table IIb.

SUBTEST 2 Checks the ability to clear, set and test the card select code. The following instruction combinations are tested:

```
CLF CH - SFC CH
CLF CH - SFS CH
STF CH - SFC CH
STF CH - SFS CH
```

Errors in the above sequence produce error messages E005-E010 as shown in Table IIb.

SUBTEST 3 Checks that the test select code does not cause an interrupt with the flag and control set on the card and the interrupt system off. The sequence of instructions is shown below:

```
STF 0
STF CH
STC CH
CLF 0
```

The CLF 0 instruction should inhibit an interrupt from occurring. Error message E004 occurs if CLF 0 fails.

SUBTEST 4 Checks that the flag of the card under test is not set when all other select code flags are set. Error message E011 occurs if a flag is set incorrectly.

SUBTEST 5 Checks the ability of the card to interrupt. With the flag and control set and the interrupt system on, there should be an interrupt on the CH channel. If not error message E014 occurs. Checks that the interrupt occured where expected. The interrupt should not occur before a string of priority affecting instructions are executed. The following instructions are used to check the hold off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages E012 and E015 will occur if this is not true. The instructions being executed prior to and just after the interrupt are checked to see that they execute properly. If they do not, error message E026 will occur. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message E013 will occur if this is not true.

SUBTEST 6 Checks that with the interrupt system on and the CH control and flag set, there is no interrupt following a CLC CH instruction. The following sequence of instructions are used.

```
STC CH
STF CH
STF 0
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message E016 will occur.

Checks that the CLC 0 instruction inhibits interrupts when the CH control and flag are set. The following sequence of instructions are used.

```
CLF CH
STC CH
STF CH
STF 0
CLC 0
```

If the CLC 0 fails to inhibit an interrupt, error message E017 will occur.

SUBTEST 7 Checks that the PRESET (EXTERNAL and INTERNAL if applicable) buttons on the front panel performs the following actions:

1. Sets all flags (EXTERNAL)
2. Clears all control (EXTERNAL)
3. Turns off the interrupt system (INTERNAL)
4. Clears the I/O data lines (EXTERNAL)

Error messages E020-E023 will occur if an error occurs in the above tests.

TEST 1 - Basic I/O test for command channel

Note: CH = command channel select code

The operation of this test is the same as Test 0 except that the Subtests 1 through 7 are performed on command channel.

TEST 2 - Checks the individual data channel and command channel status bits under static conditions (no FEED REQUEST is given). If the test fails in any of the following subtests, i.e., one or more status bits are not set as expected, error message E030 and E031 (or both) will result.

SUBTEST 1 Operator is instructed to clear device (transition from OFF-LINE to ON-LINE is necessary), clear stackers and hoppers, and to press STOP, START, and RUN.

This is requested by the message H032.

Individual status bits are tested to verify proper setting of the status lines. The READY and HOPPER light indicators should be on.

SUBTEST 2 Instructs the operator by the message H033 to press STOP and RUN.

The READY and READY FOR COMMAND status lines should go false.

The READY light should be turned off.

SUBTEST 3 Instructs the operator by the message H034 to press START and RUN.

The READY and READY FOR COMMAND status lines should return from false to true. The READY light should be turned on.

SUBTEST 4 Instructs the operator to load hopper #1 with one blank card, press STOP twice, and press RUN (message H035).

The PRIMARY HOPPER EMPTY status line should go false.

SUBTEST 5 Instructs the operator to load hopper #2 with one blank card, press STOP twice, and press RUN (message H036).

The SECONDARY HOPPER EMPTY status line should go false. The HOPPER light should be turned off.

SUBTEST 6 The message H037 (without halt) informs the operator that the stacker control mode check follows. The operator is then instructed by the message H041 to extend the stacker #1 arm to limit (to simulate stacker #1 being full) and to press RUN.

The STACKER FULL status line should go true and the READY and READY FOR COMMAND status lines should go false. The READY light should be turned off and the STACKER light should be turned on.

SUBTEST 7 Instructs the operator to press STOP, START, and RUN (message H043). The READY light should be turned off.

The operator is then instructed by the message H042 to extend the stacker #2 arm to limit (to simulate stacker #2 being full) and to press RUN.

The STACKER FULL status line should go true and the READY and READY FOR COMMAND status lines should go false. The READY light should be turned off and the STACKER light should be turned on.

SUBTEST 8 Instructs the operator to press STOP, START, and RUN (message H043). The READY light should be turned on and the STACKER light should be turned off.

The message H040 (without halt) informs the operator that the stacker overflow mode check follows. The operator is then instructed by the message H041 to extend the stacker #1 arm to limit and to press RUN.

The STACKER FULL status line should stay false and the READY and READY FOR COMMAND status lines should stay true. The READY light should stay on and the STACKER light should stay off.

SUBTEST 9 The operator is instructed by the message H042 to extend the stacker #2 arm to limit and to press RUN.

The STACKER FULL status line should go true and the READY and READY FOR COMMAND status lines should go false. The READY light should be turned off and the STACKER light should be turned on.

The operator is then instructed to press STOP, START, and RUN (message H043). The STACKER FULL status line should go false and the READY and READY FOR COMMAND status lines should go true. The READY light should be turned on and the STACKER light should be turned off.

Since in each of the following tests (Tests 3 through 11 and Operator Design) the FEED REQUEST command is used, a pick failure may occur. If a pick failure is detected, error message E111 will be given, followed by the message H112 instructing the operator to correct hopper conditions, clear device, and to press STOP, START, and RUN. If more than 2 consecutive pick failures occur, error message E101 will result and either current subtest or entire test will be aborted. In the case that entire test is aborted, E101 is followed by E054. After pressing RUN, the diagnostic proceeds to the next test.

Whenever a device malfunction is detected during the test execution, an appropriate error message is given depending on the nature of the malfunction. Refer to Table IIb for specific details of error messages.

TEST 3 — Checks the individual data channel and command channel status bits in combination with FEED REQUEST, picking cards from both hoppers, and stacking cards in both stackers. If the test fails in any of the following subtests, i.e., one or more status bits are not set as expected, error message E030 or E031 (or both) will result.

A visual verification is required whether the cards are fed from the expected hopper or stacked in the expected stacker.

If the operator does not load each hopper with at least 10 cards before the test is started (see Subtest 1), the "hopper empty" condition will be detected during the test and error message E030 or E031 (or both) will result.

SUBTEST 1 Instructs the operator by the message H052 to load both hoppers with blank cards and to press STOP twice, START, and RUN. At least 10 cards must be loaded in each hopper. However, since the subsequent tests also use blank cards from hopper #2, it is convenient to load hopper #2 with approximately 120 blank cards at this point.

The message H040 (without halt) then informs the operator that the stacker overflow mode check follows and five cards should be subsequently fed from hopper #1 and stacked in stacker #1. During this operation, all relevant status bits are checked. After the operation is completed, the wait station should be empty. The operator is then instructed by the message H041 to extend the stacker #1 arm to limit and to press RUN.

Five cards should be then fed from hopper #2 and stacked in stacker #2. After the operation is completed, the wait station should be empty.

SUBTEST 2 Instructs the operator by the message H053 to clear device and stackers (transition from OFF-LINE to ON-LINE is necessary), and to press STOP, START, and RUN. The message H037 (without halt) then informs the operator that the stacker control mode check follows and five cards should be fed from hopper #1 and stacked in stacker #1.

SUBTEST 3 Five cards should be fed from hopper #2 and stacked in stacker #2. After the operation is completed, the wait station should be empty. The operator is then instructed by the message H055 to clear stackers and to press STOP, START, and RUN.

As shown in Table I, Subtest 7 in Tests 0 and 1 and Tests 2 and 3 are suppressed if the switch register bit 8 or 12 is set.

The following tests (4 through 11) are designed to thoroughly test all the functions of the Card Reader Punch including data transfers between computer memory and the output, print, and input buffers. Tests 4, 6, 8, and 10 use the "wait-for-flag" method for data transfers while the Tests 5, 7, 9, 11 and Operator Design (Test 12) use the interrupt method. In all the remaining tests, the stacker control mode of operation is used.

Each test is subdivided into two subtests. In Subtest 1, twelve (12) blank cards are subsequently fed from hopper #2, punched or printed (or both), and stacked in stacker #2.. After the Subtest 1 is completed, stacker #2 contains twelve (12) cards which are called Test Cards for the test under consideration. Test card patterns for each test are shown in Tables Va through Vh. The operator counts cards from the beginning of stack; top is the beginning, starting number is one (1). Wait station should always be empty after the Subtest 1 completion.

Whenever a non-blank card is detected in the wait station during Subtest 1, error message E107 will result. After pressing RUN, the operator is instructed by the message H114 to clear device, remove non-blank card (which is fed during clearing from the wait station into stacker #2), and to press STOP, START, and RUN. If more than two consecutive non-blanks are detected, error message E054 is given and the test is aborted. The operator should check the cards in hopper #2 and remove all non-blanks. If the last blank card was picked from hopper #2 and the Subtest 1 has not yet been completed, the operator is instructed by the message H056 to load blank cards and to press STOP twice, START, and RUN.

In Subtest 2, the operator is first instructed by the message H062 to load hopper #1 with test cards for current test, and to press STOP twice, START, and RUN. Note that during standard run, the test cards are generated during Subtest 1 and stacked in stacker #2. The operator therefore takes twelve test cards from stacker #2 and loads them in hopper #1. After pressing RUN, the test cards are subsequently fed from hopper #1 and their contents are read and compared with expected result.

The cards are then stacked in stacker #1. If the data read does not agree with expected result, error message E110 will occur. The operator should then verify the card and column in error. The verification is made by comparing the card with corresponding test card pattern shown in Tables Va through Vh. If the card is punched correctly, the read was in error.

If hopper #1 becomes empty and Subtest 2 has not yet been completed, the operator is instructed by the message H063 to load test cards and to press STOP twice, START, and RUN. The test cards must be loaded in correct order, otherwise error message E110 will result.

TEST 4 — Checks basic punch and read functions.

SUBTEST 1 — Twelve (12) test cards are punched (without printing) using the data pattern shown in Table Va. Before each card is punched, corresponding data is loaded into the output buffer.

A visual check should be made that none of the cards were printed during the punch process.

SUBTEST 2 — Test cards are read into the input buffer and the correctness of punched data is verified by the program.

TEST 5 — Checks basic punch, print, and read functions.

SUBTEST 1 — Twelve (12) test cards are punched and printed using the data pattern shown in Table Vb. The same data is punched and printed. Output buffer is used to hold data to be punched and printed.

The operator should visually check the printed data (using Table Vb).

SUBTEST 2 — Test cards are read into the input buffer and the correctness of punched data is verified by the program.

TEST 6 — Checks punching, printing and reading printable Hollerith data.

SUBTEST 1 — Twelve (12) test cards are punched and printed using the data pattern shown in Table Vc. The same Hollerith data is punched and printed. Output buffer is used to hold data to be punched and printed.

The operator should visually check the printed data (using Table Vc).

SUBTEST 2 — Test cards are read into the input buffer and the correctness of punched data is verified by the program.

TEST 7 — Checks printing Hollerith data and reading blanks.

SUBTEST 1 — Twelve (12) test cards are printed (without punching) using the data pattern shown in Table Vd. Output buffer is used to hold Hollerith data to be printed.

The operator should visually check the printed data (using Table Vd).

SUBTEST 2 — Test cards are read into the input buffer and verification by program is made that none of the cards were punched in Subtest 1.

TEST 8 — Checks punching and reading laced cards and printing separate Hollerith data.

SUBTEST 1 — Twelve (12) test cards are punched and printed using separate data for punching and printing as shown in Table Ve. Output buffer is used to hold punch data while print buffer is used to hold separate Hollerith data to be printed.

The operator should visually check the printed data (using Table Ve).

SUBTEST 2 — Test cards are read into the input buffer and the correctness of punched data is verified by the program. The punched data can also be easily verified visually since on each card all the twelve positions in each column are punched.

TEST 9 — Checks punching and reading all but one row with an attempt to print same (non-printable) data.

SUBTEST 1 — Twelve (12) test cards are punched using the data pattern shown in Table Vf. At the same time, an attempt is made to print the same data. Output buffer is used to hold data to be punched.

A visual check should be made that none of the cards were printed during the punch process (none of the 12-bit combinations in any column corresponds to a printable Hollerith character).

SUBTEST 2 Test cards are read into the input buffer and the correctness of punched data is verified by the program.

TEST 10 Checks punching and reading worst case data with an attempt to print separate non-printable data.

SUBTEST 1 Twelve (12) test cards are punched using the data pattern shown in Table Vg. Output buffer is used to hold data to be punched. At the same time, an attempt is made to print separate non-printable data stored in the print buffer. Data for Test 9 (see Table Vf) is used as non-printable data.

A visual check should be made that none of the cards were printed during the punch process.

SUBTEST 2 Test cards are read into the input buffer and the correctness of punched data is verified by the program.

TEST 11 Punch station test (punch and read, and attempt to print same non-printable data).

SUBTEST 1 Twelve (12) test cards are punched using the data pattern shown in Table Vh. At the same time, an attempt is made to print the same data. Output buffer is used to hold data to be punched.

A visual check should be made that none of the cards were printed during the punch process.

SUBTEST 2 Test cards are read into the input buffer and the correctness of punched data is verified by the program.

VIII. OPERATOR DESIGN

The Operator Design is a special test procedure which allows the operator to read, punch, or print cards using his own data patterns, and to obtain the device status.

To enter the Operator Design, the operator must select Test 12 (see Section VID). The Operator Design is not a standard test and, therefore, is not entered when the standard set of tests is used.

The message H115 is printed when the Operator Design is entered. This is followed by the message "H116 @" indicating the program is ready to accept an order from the operator. A set of available orders is defined in Table IV. Each order is assigned a unique octal number. After the message "H116 @" is given, a halt (106016) will occur. The operator then sets the octal number corresponding to the desired order into the switch register bits 0 through 3 as shown in Table IV and presses RUN. After RUN is pressed, the program confirms acceptance of the order by printing ":XX" (XX = octal number corresponding to the order). No confirmation of the order is given if the teleprinter is not present. The required order is then executed, followed by the message "H116 @" indicating that a new order may be entered. When the order "11_8" (Exit from Operator Design) is given, the message ":11" is followed by the message "PASS XXXXXX" and halt 102077.

Two buffers in computer memory are reserved in connection with orders defined in Table IV. The buffers are called buffer X and buffer Y. Each buffer has 80 12-bit positions corresponding to 80 data columns on a card. Whenever the Operator Design is entered, all the buffer X bits are preset to 1, the buffer Y is preset to hold Hollerith data (the data pattern used is the same as for Test 6, Card 1; see Table Vc). The contents of each buffer are not affected until replaced by new data (using orders "0_8" and "1_8").

In some cases, it may be useful to execute the same order several times without necessary pressing RUN each time the order is to be executed (e.g., punching a deck of cards containing the same data). To accomplish this, switch register bit 4 is used in conjunction with bits 0 through 3. If bit 4 is set and RUN is pressed, the execution of the order specified by bits 0 through 3 is repeated until bit 4 is reset. After RUN is pressed, the message ":XX" (XX = octal

number corresponding to the order) is printed only once and not for each repeated execution of the same order. Switch register bit 4 should be reset before pressing RUN if the order is to be executed only once. It should be noted that there is no practical use of bit 4 in conjunction with orders "2_8", "3_8", and "11_8".

If the octal number set into bits 0 through 3 does not correspond to any order defined in Table IV, the message H121 is given followed by "H116 @". If the device fails to perform a required function during the execution of an order one or more error messages related to the failure may be given, followed by the message E112 and halt (106022). After the RUN is pressed, "H116 @" message is given ; operator may then enter a new order.

IX. OPERATING INSTRUCTIONS

1. Install interface card and priority jumper card (if needed) to enable priority chain. Turn on the Card Reader Punch. Load the configurator and set it up according to the M.O.D. for the configurator.
2. Load the Diagnostic binary object tape using the Binary Loader.
3. If desired, dump the combined diagnostic/Diagnostic Configurator using the dump routine provided by the Configurator. See Configurator M.O.D. for the correct operating procedure. (This step may also be used after 7.)
4. Load address 100_8 into the P register.
5. Load the switch register with the data channel select code (bits 0-5).
6. Press PRESET (INTERNAL AND EXTERNAL if applicable); then press RUN.
7. Halt 102074 should occur to indicate that the select code entered is valid (i.e.> 7_8). If halt 102073 occurs the select code was invalid. Reenter a valid select code and repeat step 6.
8. Enter program execution option bits to the switch register (if desired). If the switch register is cleared a standard test run is performed. If it is desired to change the tests to be run at this point, switch register bit 9 is set and RUN pressed. Halt 102075 will occur. The A register may be set to the desired tests followed by clearing switch register bit 9. It is recommended that the standard run be performed initially before changing the tests selected.
9. Press RUN.
10. An introductory message "HP 2894 CARD READER PUNCH DIAGNOSTIC" will be typed (if teleprinter was configured in step 1). The diagnostic is now being executed. If the tests requiring manual intervention from the operator are not suppressed (switch register bits 8 or 12) then the following message will occur:

"H024 PRESS PRESET (EXT/INT),RUN"

followed by the message

"H025 BI-O COMP FOR DATA CH"

The message H024 then occurs again in connection with basic I/O test for command channel, followed by the message:

"H025 BI-O COMP FOR CMND CH"

11. At the completion of the diagnostic the following message will occur;

"PASS XXXXXX"

followed by halt 102077 (A register will be equal to pass count).

At this point, the operator may repeat the diagnostic by pressing RUN. If the operator wishes to change the tests being executed, he may set bit 9 of the switch register and press RUN. Halt 102075 will occur. He may then change the A register to correspond to the tests desired* and then press RUN.

*NOTE: (A REG bit 0 = Test 0, bit 1 = Test 1,..., bit 11 = Test 11_{10}, 13_8)

If the A register is zeroed, all tests will be run.

The above procedures have assumed no errors have occured during the diagnostic run. If an error does occur a message will be typed followed by a halt. The program may be continued by pressing RUN.

During the first diagnostic run, the operator should visually verify punched and printed data (using test card patterns in Tables Va through Vh) after the Subtest 1 in Tests 4 through 11 is completed. The reason is that a possible punch error in Subtest 1 might be compensated by a read error in Subtest 2. Thus, neither the punch error nor the read error would ever be detected.

As shown in Table I, the switch register bit 8 is used to minimize operator intervention. The operator intervention is also minimized when a loop on diagnostic is required, i.e., if switch 12 is set. The following subtests, tests, and messages will be suppressed if bit 8 or 12 is set:

- Subtest 7 in Tests 0 and 1,
- Test 2 and 3,
- Message H062.

Refer to Section VII for description of subtests or tests being suppressed.

After the Tests 4 through 11 are completed during a standard diagnostic run, stacker #1 should contain 8 x 12 test cards, i.e., 96 cards. Test cards for Test 4 are at the top of the deck followed by test cards for Test 5 and so on up to test cards for Test 11, which are at the bottom of the deck. Test cards for Tests 4 through 11 in the order described above constitute the Test Deck.

Subtest 2 in Tests 4 through 11 may be suppressed using switch register bit 5 (i.e., if set, only punch and print operations are performed). Subtest 1 in Tests 4 through 11 may be suppressed using switch register bit 6 (i.e., if set, only read operation is performed). It should be noted, however, that either the entire test deck or at least 12 test cards for a particular test must have been previously generated in some of the earlier diagnostic runs, if the switch register bit 6 option is to be used.

The message H062 is suppressed if any of the switch register bits 6, 8, 12, or 13 is set. This allows the operator to load hopper #1 with several test decks, to load hopper #2 with blank cards, and to run the diagnostic without halting and loading hopper #1 after each completion of Subtest 1 in Test 4 through 11. This is particularly useful whenever a loop on the diagnostic or its portion is required. Note that if a loop on a single test is required hopper #1 must be loaded with several identical sets of 12 test cards for the test under consideration.

In general, switch register option bits should be used with caution. For example, if the message H062 with associated halt is suppressed, hopper #1 must either be empty or contain the test deck or test cards in a correct order. If it is empty, the operator is instructed by the message H063 to load test cards; however, if a card with incorrect data is picked from hopper #1, error message E110 occurs.

TABLE I

SWITCH REGISTER OPTIONS

BIT	MEANING IF SET
0 1 2 3 4	Used only within Operator Design to specify a required order. A set of available orders is defined in Table IV.
5	Suppress Subtest 2 (read operation) in Tests 4 through 11.
6	Suppress Subtest 1 (punch and print operations) in Tests 4 through 11; message H062 with associated halt will also be suppressed.
7	Report status by message H123 after each error message indicated by the asterisk (*) (see Table IIb).
8	Minimize operator intervention; Subtest 7 in Tests 0 and 1, Tests 2 and 3, and message H062 will be suppressed.
9	Abort diagnostic execution and halt (102075) at the end of current test; user may then specify a new group of tests in the A register, reset bit 9, and press RUN.
10	Suppress non error messages.
11	Suppress error messages.

BIT	MEANING IF SET
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teleprinter is not present. Also the operator intervention is minimized (same effect as if bit 8 was set).
13	Repeat last test executed (loop on test); message H062 with associated halt will also be suppressed.
14	Suppress error halts and halt after message H123.
15	Halt (102076) at the end of each test; A register will contain the test number.

TABLE IIa

HALT CODE SUMMARY

Halt	Meaning
102000-102067	Error or information messages $00\text{-}67_8$
106000-106024	Error or information messages $100\text{-}124_8$
102073	Select code input error
102074	Select code input complete
102075	User selection request
102076	End of Test (A register = Test number)
102077	End of diagnostic run
106077	Trap cell halts in location $2\text{-}77_8$

TABLE IIb

ERROR/INFORMATION MESSAGES AND HALTS

Halt Code	Program Section	Message	Comments
102073	Configuration	None	I/O select code entered at configuration invalid. Must be greater than 7_8. Reenter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration valid. Enter program option bits to switch register and press RUN.
102075	Test Control	None	Test selection request resulting from switch bit 9 being set. Enter to A/B registers the desired group of tests to be executed and press RUN.
102076	Test Control	None	End of test halt resulting from switch register bit 15 being set (A register = test number). To continue press RUN.
102077	Test Control	PASS XXXXXX	Diagnostic run complete. (A REG = XXXXXX). Switch register options may be changed or test selection changed by setting bit 9 of switch register. To continue press RUN.
106077	Test Control	None	Halt stored in location $2\text{-}77_8$ to trap interrupts which may occur unexpectedly because of hardware malfunctions. M register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.

Halt Code	Section	Message	Comments
None	Test Control	HP 2894 CARD READER PUNCH DIAGNOSTIC	Introductory message.
None	Test Control	TEST XX	Information message before error message (XX = test number in octal). Message occurs for the first error within a test but is suppressed for any subsequent messages within the same test.

Halt Code	Section	Message	Comments
102000	Test 0-1	E000 CLF 0-SFC 0 ERROR	CLF/SFC 0 combination failed. CLF did not clear flags or SFC caused no skip with flags clear.
102001	Test 0-1	E001 CLF 0-SFS 0 ERROR	CLF/SFS 0 combination failed CLF did not clear flags or SFS caused skip with flags clear.
102002	Test 0-1	E002 STF 0-SFC 0 ERROR	STF/SFC 0 combination failed. STF did not set flags or SFC caused skip with flags set.
102003	Test 0-1	E003 STF 0-SFS 0 ERROR	STF/SFS 0 combination failed STF did not set flags or SFS caused no skip with flags set.
102004	Test 0-1	E004 CLF 0 DID NOT INHIBIT INT	With card flag and control set, CLF 0 did not turn off interrupt system.
102005	Test 0-1	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102006	Test 0-1	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102007	Test 0-1	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set flag or SFC caused skip with flag set.
102010	Test 0-1	E010 STF CH-SFS CH ERROR	STF/SFS CH combination failed. STF did not set flag or SFS caused no skip with flag set.
102011	Test 0-1	E011 STF XX SET CARD FLAG	Select code screen test failed. XX = select code that caused that card flag to set.

A REG = XX

Halt Code	Section	Message	Comments
102012	Test 0-1	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0-1	E013 SECOND INT OCCURRED	Card interrupt a second time after initial interrupt was processed.
102014	Test 0-1	E014 NO INT	No interrupt occurred with card flag and control set and the interrupt system on
102015	Test 0-1	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0-1	E016 CLC CH ERROR	CLC CH did not clear card control with the interrupt system on.
102017	Test 0-1	E017 CLC 0 ERROR	CLC 0 did not clear control with the interrupt system on.
102020	Test 0-1	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card flag.
102021	Test 0-1	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0-1	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear control.
102023	Test 0-1	E023 PRESET (EXT) DID NOT CLEAR I/O LINES	PRESET (EXT) did not clear I/O data lines
102024	Test 0-1	H024 PRESS PRESET (EXT+ INT), RUN	Press PRESET (External, Internal), RUN.
None	Test 0-1	H025 BI-0 COMP FOR DATA CH (OR CMND CH)	Basic I/O Tests completed for data or command channel.
102026	Test 0-1	E026 INT EXECUTION ERROR	Instructions being executed prior to and just after interrupt did not execute correctly.

Halt Code	Section	Message	Comments
102030	Test 2-3	E030 CMND STATUS ERR EXP: Y YYY YYY YYY YYY YYY ACT: X XXX XXX XXX XXX XXX	Y's represent expected state of the command channel or data channel status word; X's represent the actual state. After halt, A register contains Y-bits and B-register contains X-bits.
102031	Test 2-3	E031 DATA STATUS ERR EXP: Y YYY YYY YYY YYY YYY ACT: X XXX XXX XXX XXX XXX	
102032	Test 2	H032 CLEAR DEVICE, STACKERS, HOPPERS; PRESS STOP, START, RUN	To clear device, transition from OFF-LINE to ON-LINE is necessary.
102033	Test 2	H033 PRESS STOP, RUN	
102034	Test 2	H034 PRESS START, RUN	
102035	Test 2	H035 LOAD HOP-1 WITH 1 BLANK CARD; PRESS STOP 2X, START, RUN	
102036	Test 2	H036 LOAD HOP-2 WITH 1 BLANK CARD; PRESS STOP 2X, START, RUN	
None	Test 2-3	H037 STACKER CONTROL MODE CHECK FOLLOWS	
None	Test 2-3	H040 STACKER OVERFLOW MODE CHECK FOLLOWS	
102041	Test 2-3	H041 EXTEND STACK - 1 ARM TO LIMIT; PRESS RUN	

Halt Code	Section	Message	Comments
102042	Test 2-3	H042 EXTEND STACK-2 ARM TO LIMIT; PRESS RUN	
102043	Test 2	H043 PRESS STOP, START, RUN	
102044	Test 4-12	H044 STACKER FULL, UNLOAD; PRESS STOP, START, RUN	
102045	Test 4-12	E045 STATUS SHOWS STACKER FULL AFTER UNLOAD (*)	See Note 1
102046	Test 4-12	H046 NOT READY FOR CMND; CLEAR DEVICE, PRESS STOP, START, RUN	To clear device, transition from OFF-LINE to ON-LINE is necessary.
102047	Test 4-11	E047 NOT READY FOR CMND AFTER CLEAR (*)	See Note 1
102050	Test 4-11	H050 CARD IN WAIT STATION; CLEAR DEVICE, PRESS STOP, START, RUN	To clear device, transition from OFF-LINE to ON-LINE is necessary. Card will be fed from wait station and stacked in stacker #2.
102051	Test 4-11	E051 STATUS SHOWS CARD IN WAIT STATION AFTER CLEAR (*)	See Note 1
102052	Test 3	H052 LOAD HOP-1&2 WITH BLANK CARDS; PRESS STOP 2X, START, RUN	At least 10 cards must be loaded in each hopper. However, it is convenient to load hopper #2 with more blank cards.
102053	Test 3	H053 CLEAR DEVICE, STACKERS; PRESS STOP, START, RUN	To clear device, transition from OFF-LINE to ON-LINE is necessary.

Halt Code	Section	Message	Comments
102054	Test 2-11	E054 TEST ABORTED (*)	After pressing RUN, diagnostic proceeds to the next test. See also Note 1.
102055	Test 3	H055 CLEAR STACKERS; PRESS STOP, START, RUN	
102056	Test 4-11	H056 HOP-2 EMPTY, LOAD WITH BLANK CARDS; PRESS STOP 2X, START, RUN	
102057	Test 4-11	E057 STATUS SHOWS HOP-2 EMPTY AFTER LOAD (*)	See Note 1.
102060	Test 4-11	E060 NO CARD ARRIVED IN WAIT STATION (*)	See Note 1.
102061	Test 4-12	E061 NO RETURN TO READY FOR CMND (*)	See Note 1.
102062	Test 4-11	H062 LOAD HOP-1 WITH TEST CARDS; PRESS STOP 2X, START, RUN	Tables Va through Vh show test card patterns for each test.
102063	Test 4-11	H063 HOP-1 EMPTY, LOAD WITH TEST CARDS; PRESS STOP 2X, START, RUN	Test cards must be loaded in correct order. Tables Va through Vh show test card patterns for each test.
102064	Test 4-11	E064 STATUS SHOWS HOP-1 EMPTY AFTER LOAD (*)	See Note 1.
102065	Test 4-12	E065 NOT READY FOR CMND BEFORE FEED REQ (*)	See Note 1.

Halt Code	Section	Message	Comments
102066	Test 4,6,8 and 10	E066 LOAD OUT BUFF ERR; DATA FLAG NOT SET (COL: XX, CRD: YY) (*)	XX represents column no. and YY represents test card no. The operator counts cards from the beginning of stack; top is the beginning, starting no. is one. Tables Va through Vh show test card patterns for each test. After halt, A register contains octal equivalent of XX and B register contains octal equivalent of YY. See also Note 1.
102067	Test 4,6,8 and 10	E067 LOAD PRINT BUFF ERR; DATA FLAG NOT SET (COL: XX, CRD=YY) (*)	
106000	Test 4-12	E100 IN BUFF FULL (CMND FLAG) NOT SET (*)	
106001	Test 4-12	E101 UNLOAD IN BUFF ERR; DATA FLAG NOT SET (COL: XX, CRD: YY) (*)	
106002	Test 5,7,9,	E102 LOAD OUT BUFF ERR; NO INT ON DATA CH (COL: XX, CRD: YY) (*)	
106003	Test 5,7,9,	E103 LOAD PRINT BUFF ERR; NO INT ON DATA CH (COL: XX, CRD: YY) (*)	
106004	Test 5,7,9,	E104 UNLOAD IN BUFF ERR; NO INT ON DATA CH (COL: XX, CRD: YY) (*)	
106005	Test 4,7,9, 11 and 12	E105 IN BUFF FULL NOT SET; NO INT ON CMND CH (*)	
106006	Test 5,7,9	E106 UNEXP INT ON CMND CH (*)	Unexpected interrupt on command channel occurred.
106007	Test 4-11	E107 NON-BLANK CARD IN WAIT STATION (*)	

Halt Code	Section	Message	Comments
106010	Test 4-11	E110 DATA COMPARE ERR (COL: XX, CRD: YY) (*) EXP: VVV VVV VVV VVV ACT: ZZZ ZZZ ZZZ ZZZ	XX represents column no. and YY represents test card no. V's represent expected data and Z's represent actual data read. After halt, A register contains V-bits and B-register contains Z-bits. See also Note 1.
106011	Test 4-12	E111 PICK FAILURE (*)	After pressing RUN, message H112 will occur. See also Note 1.
106012	Test 4-12	H112 CORRECT HOP COND, CLEAR DEV; PRESS STOP, START, RUN	Operator should correct condition of a hopper where the pick failure occured. To clear device, transition from OFF-LINE to ON-LINE is necessary.
106013	Test 4-12	E113 INPUT CHECK (*)	Input Check status bit is true. See also Note 1.
106014	Test 4-11	H114 CLEAR DEV, REMOVE NON-BL CRD; PRESS STOP, START, RUN	To clear device, transition from OFF-LINE to ON-LINE, is necessary. Card will be stacked in stacker #2.
None	Test 12	H115 OPERATOR DESIGN FOLLOWS	
106016	Test 12	H116 @	The program is ready to accept an order from the operator (within Operator Design). See Table IV for definitions of available orders.

Halt Code	Section	Message	Comments
None	Test 12	H117 BUFFER X: 8x { PQRS PQRS...PQRS PQRS PQRS...PQRS ⋮ ⋮ ⋮ PQRS PQRS PQRS } 10x	PQRS represents one column of data which was read from a card into buffers X or Y. P,Q,R, and S are octal equivalents of data punched in positions 12-11-0, 1-2-3, 4-5-6, and 7-8-9, respectively. In the message, starting from the left, first row of PQRS's correspond to columns 1 through 10, second row corresponds to columns 11 through 20, and so on up to eights row which corresponds to columns 71 through 80.
None	Test 12	H120 BUFFER Y: 8x { PQRS PQRS...PQRS PQRS PQRS...PQRS ⋮ ⋮ ⋮ PQRS PQRS PQRS } 10x	
None	Test 12	H121 ORDER NOT RECOGNIZED	
106022	Test 12	E122 ERR IN ORDER EXECUTION	
106023	Test 4-12	H123 STATUS CMND: Y YYY YYY YYY YYY YYY DATA: X XXX XXX XXX XXX XXX	Y's represent the command channel status bits; X's represent the data channel status bits. After halt, A register contains Y-bits and B register contains X-bits.
106024	Test 4-12	E124 READ CHECK (*)	Read Check status bit is true. See also Note 1.
None	Test 12	:0	Confirmation of an order entered by the operator (within Operator Design). See Table IV for definitions of available orders.
None	Test 12	:1	
None	Test 12	:2	
None	Test 12	:3	
None	Test 12	:4	
None	Test 12	:5	
None	Test 12	:6	
None	Test 12	:7	
None	Test 12	:10	
None	Test 12	:11	

NOTE 1: After an error message with the asterisk (*) is given and the corresponding halt occurs, the operator may optionally obtain current status of the Card Reader Punch. If the switch register bit 7 is set and RUN is pressed, the status is reported by the message H123. See Section VIC for more details.

NOTE 2: Operator Design is considered to be Test 12.

Table III

Data Channel and Command Channel Bit Assignment

DATA INPUT REGISTER - DATA CHANNEL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPUT BUFFER FULL (also C.C. FLAG)	DEVICE FLAG LINE DATA CHAN.	N.U.	READ CHECK	INPUT(1) CHECK / DATA ROW 12	OUTPUT(1) CHECK / DATA ROW 11	HOPPER #1 EMPTY (1) / DATA ROW 0	STACKER(1) FULL / DATA ROW 1	DATA ROW 2	DATA ROW 3	DATA ROW 4	DATA ROW 5	DATA ROW 6	DATA ROW 7	DATA ROW 8	DATA ROW 9

(1) IF INPUT BUFFER FULL = FALSE, THESE COLUMNS ARE STATUS

DATA OUTPUT REGISTER - DATA CHANNEL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLEAR BUFFER FULL	N.U.	N.U.	N.U.	INHIBIT(4) INPUT FEED / DATA ROW 12	DATA ROW 11	DATA ROW 0	DATA ROW 1	DATA ROW 2	DATA ROW 3	DATA ROW 4	DATA ROW 5	DATA ROW 6	DATA ROW 7	DATA ROW 8	DATA ROW 9

(4) = INHIBIT INPUT FEED WHEN FEED REQUEST ISSUED

STATUS INPUT REGISTER - COMMAND CHANNEL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTROL REGISTER BIT 15 (2)	CONTROL REGISTER BIT 14 (2)	CONTROL REGISTER BIT 13 (2)	CONTROL REGISTER BIT 12 (2)	CONTROL REGISTER BIT 11 (2)	CONTROL REGISTER BIT 10 (2)	N.U.	N.U.	N.U.	READY	READY FOR COMMAND	CARD IN WAIT STATION	N.U.	N.U.	SECONDARY HOPPER EMPTY (#2)	COMMAND CHANNEL FLAG F.F.

(2) A READOUT OF THE EXISTING CONDITION OF THE CONTROL REGISTER(TIED INTERNALLY ON THE INTERFACE CARD)

CONTROL OUTPUT REGISTER - COMMAND CHANNEL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HOPPER #2 SELECT	PUNCH	PRINT	STACKER CONTROL MODE (3)	SELECT STACKER (STACKER #2 = 1)	SEPARATE PRINT DATA	N.U.	N.U.	N.U.	N.U.	N.U.	N.U.	N.U.	N.U.	N.U.	N.U.

(3) ONLY HAS CONTROL ON FIRST FEED REQUEST AFTER 'ON LINE', ELSE OVERFLOW MODE.

N.U. = NOT USED - DON'T CARE

DATA CHANNEL

DEVICE FLAG	DEVICE COMMAND
OUTPUT BUFF AVAILABLE PRINT BUFF AVAILABLE INPUT DATA AVAILABLE	LOAD OUTPUT BUFFER NEW DATA REQUEST

COMMAND CHANNEL

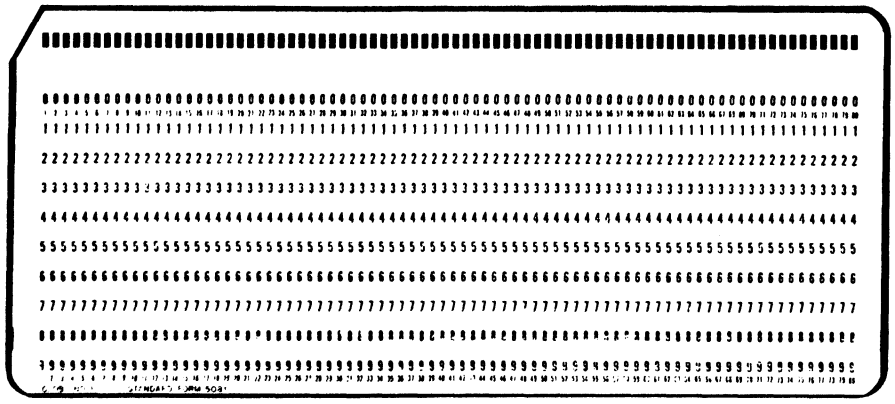
DEVICE FLAG	DEVICE COMMAND
INPUT BUFFER FULL (also DATA BIT 15)	FEED REQUEST

TABLE IV

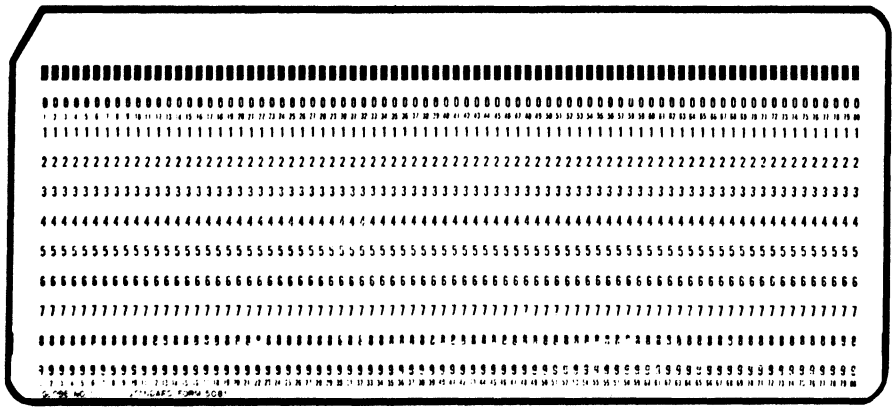
OPERATOR DESIGN ORDERS

Octal digits set into switch register bits		
Bit 3	Bits 0 through 2	Order
0	0	Feed one card from hopper #1, read its contents into Buffer X, and stack the card in stacker #1.
0	1	Feed one card from hopper #1, read its contents into Buffer Y, and stack the card in Stacker #1.
0	2	Display contents of Buffer X by the message H117.
0	3	Display contents of Buffer Y by the message H120.
0	4	Punch data from Buffer X.
0	5	Print data from Buffer X.
0	6	Punch and print data from Buffer X.
0	7	Punch data from Buffer X and print data from Buffer Y.
1	0	Report current status of the device by the message H123.
1	1	Exit from Operator Design.

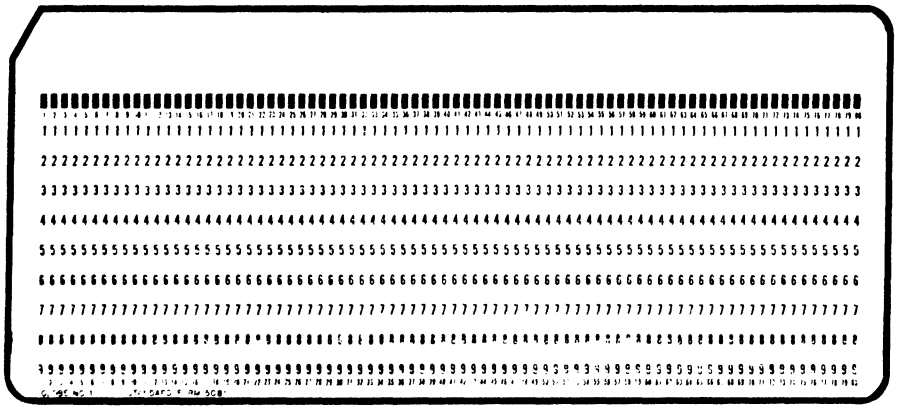
If an order is to be executed only once, the switch register bit 4 should be reset. If set, the order is repeated until bit 4 is reset.



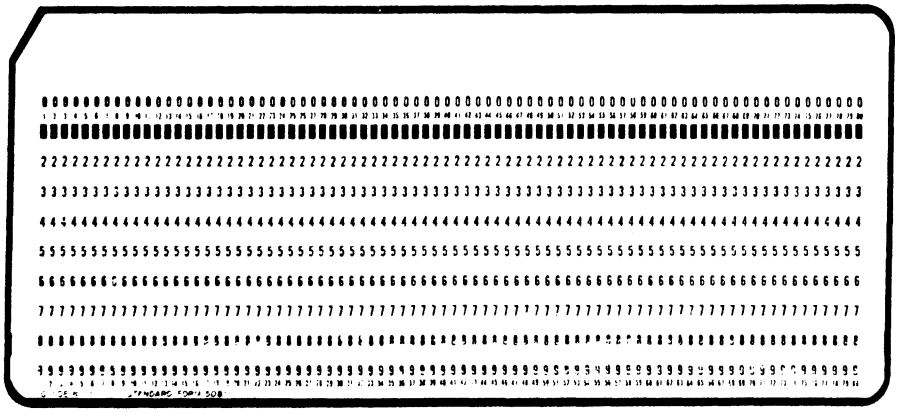
Card 1



Card 2



Card 3

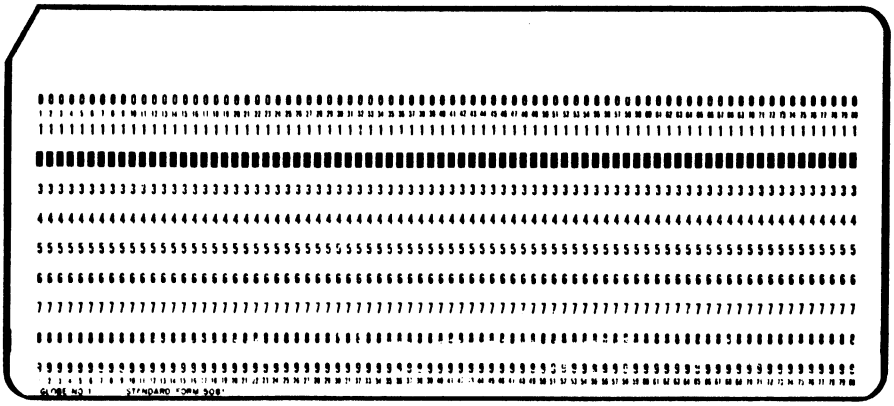


Card 4

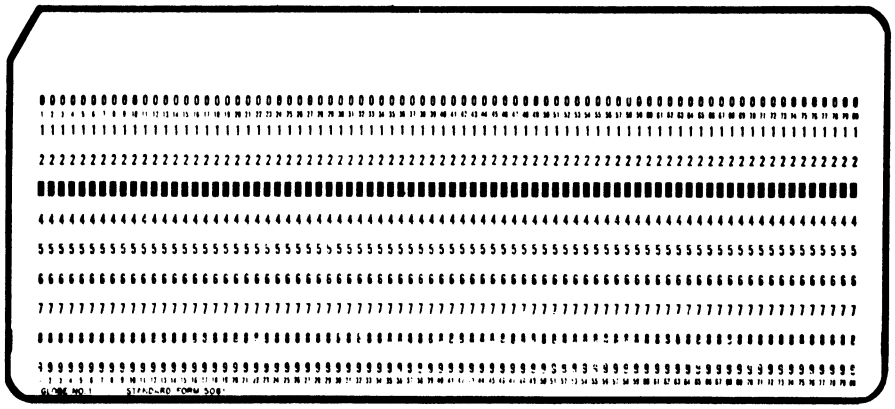
TABLE Va

Test Cards for Test 4

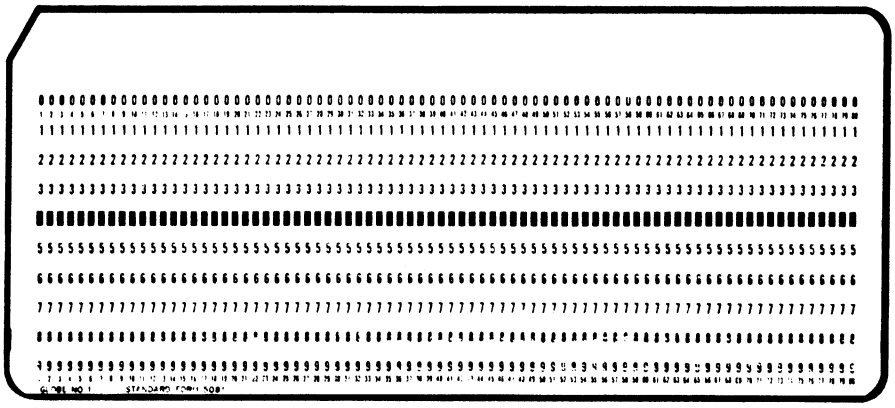
TABLE Va
(continued)



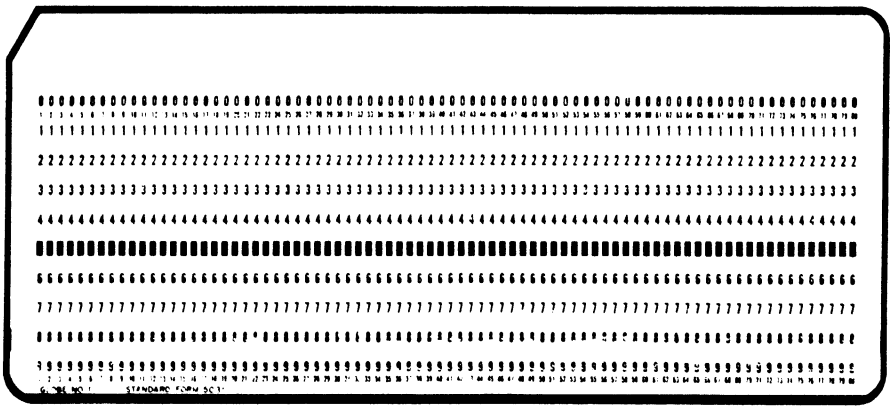
Card 5



Card 6

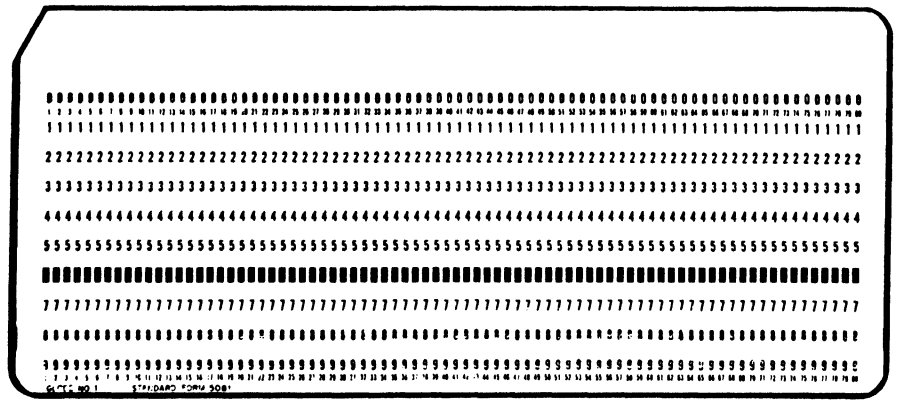


Card 7

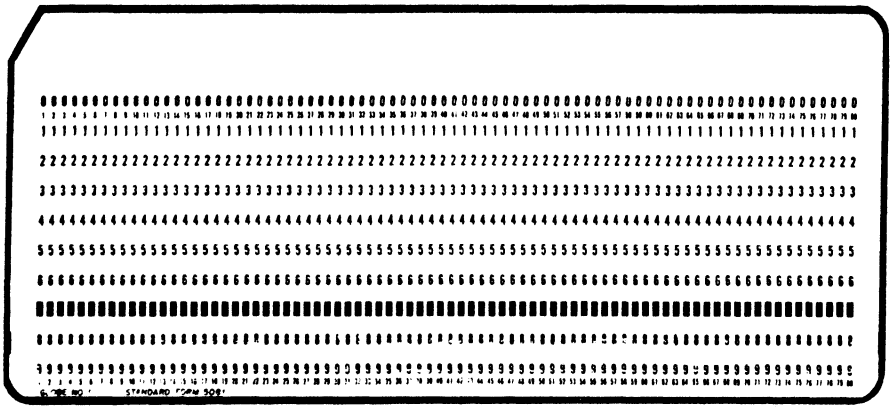


Card 8

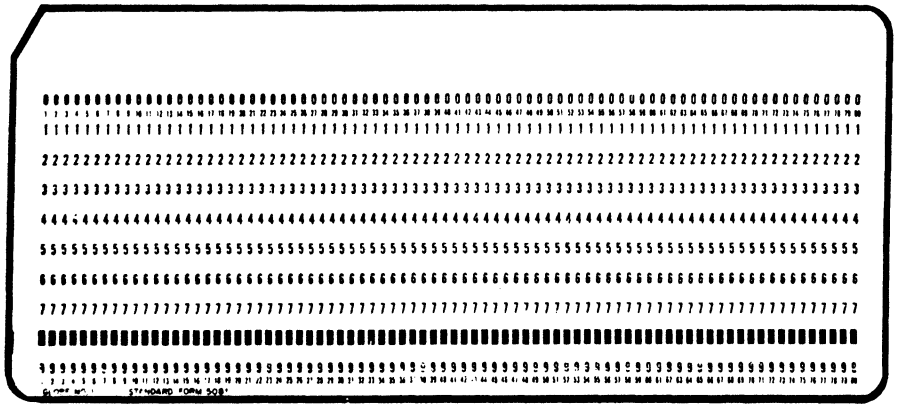
TABLE Va
(continued)



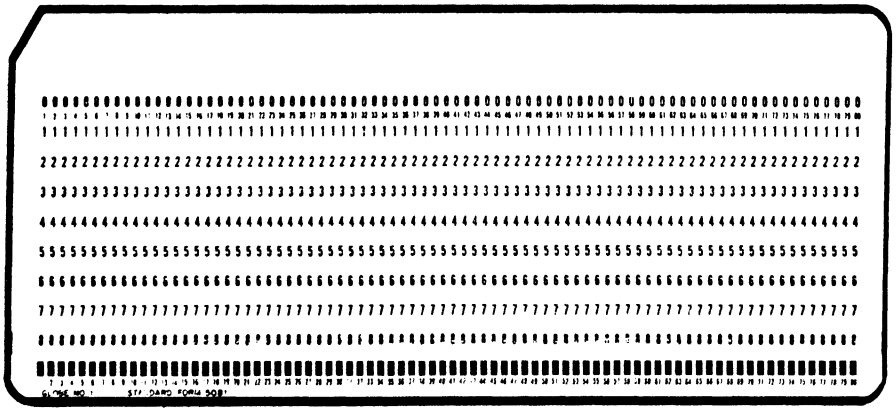
Card 9



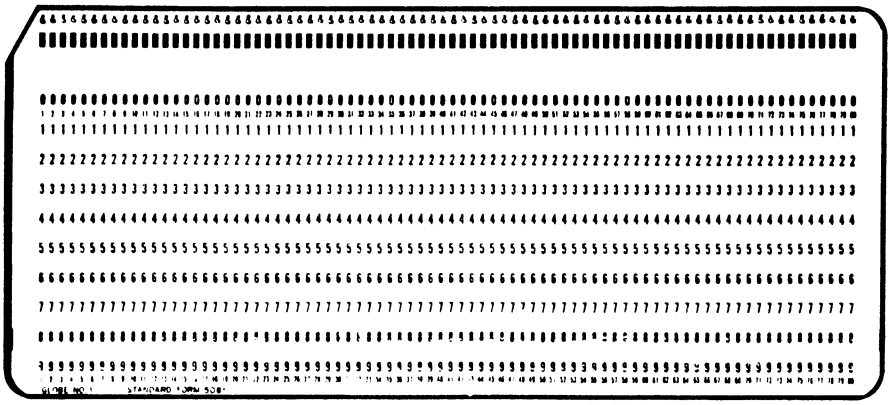
Card 10



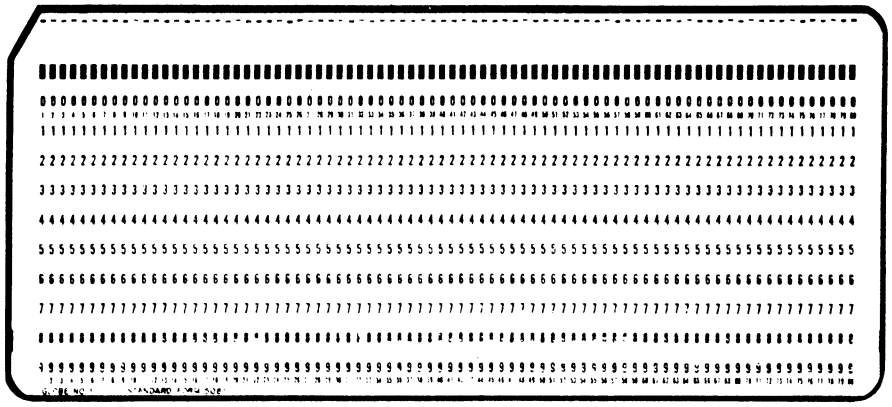
Card 11



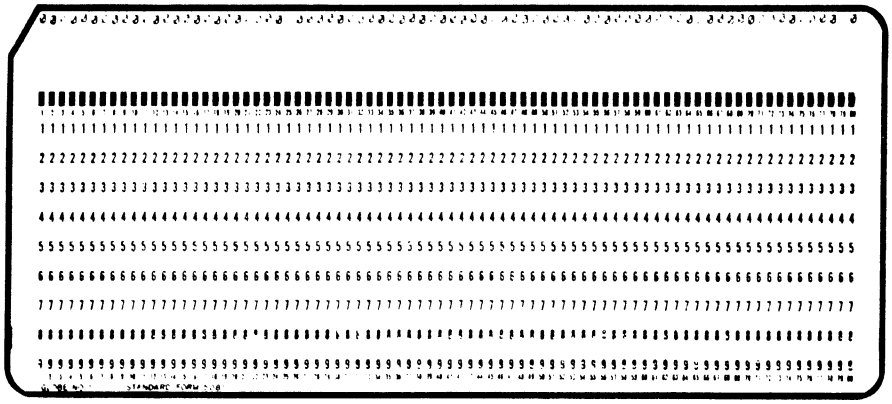
Card 12



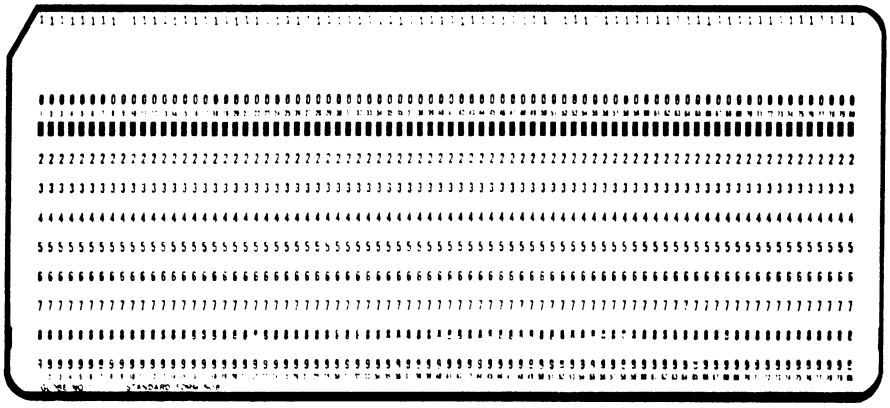
Card 1



Card 2



Card 3

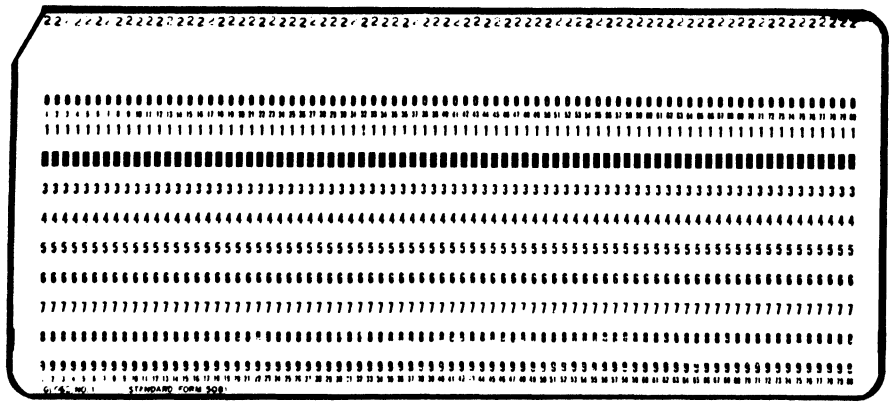


Card 4

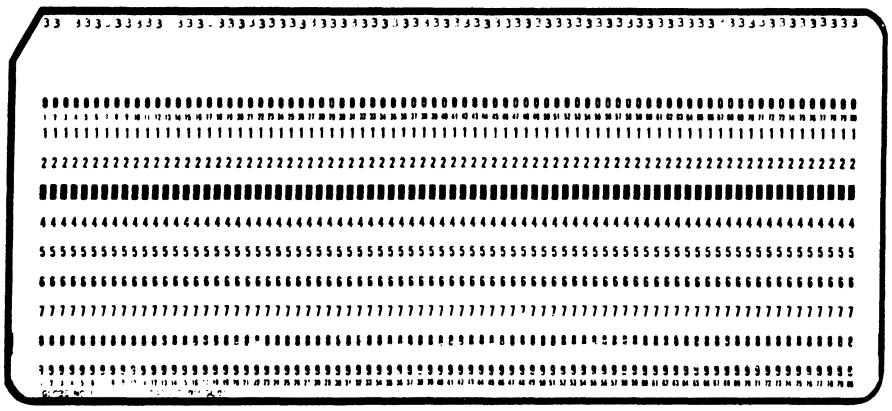
TABLE Vb

Test Cards for Test 5

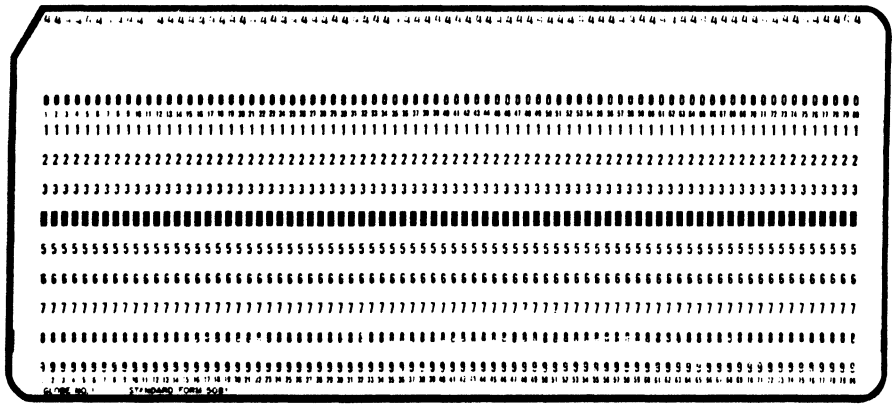
TABLE Vb
(continued)



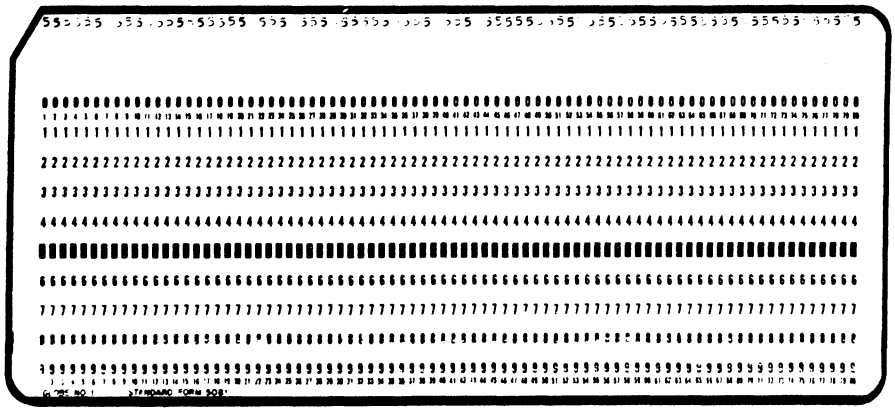
Card 5



Card 6

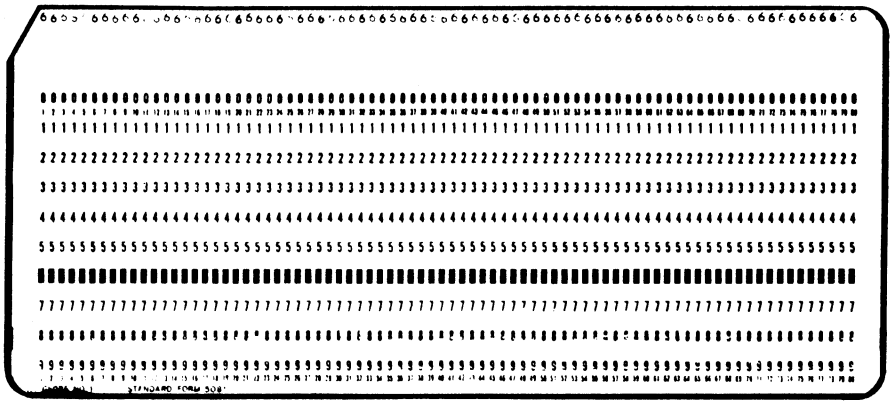


Card 7

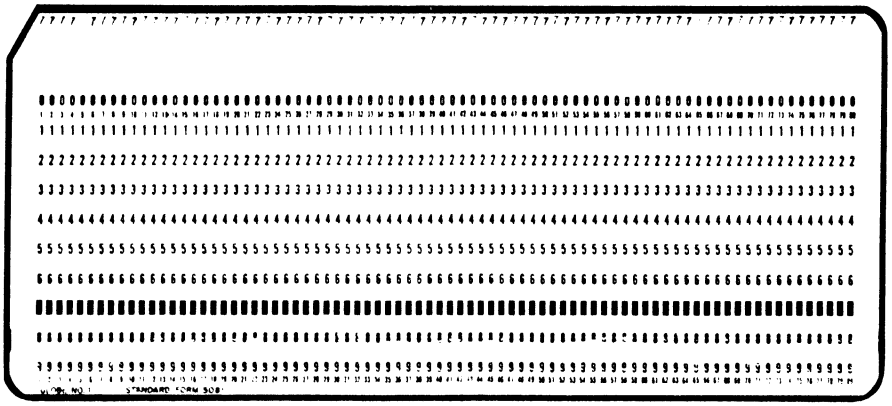


Card 8

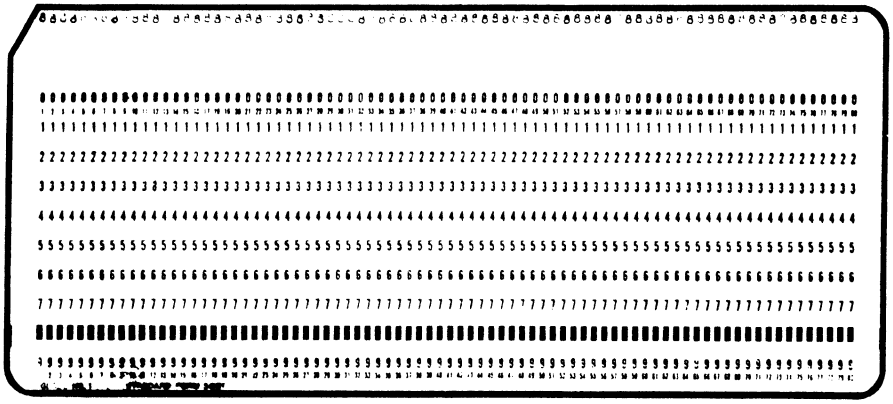
TABLE Vb
(continued)



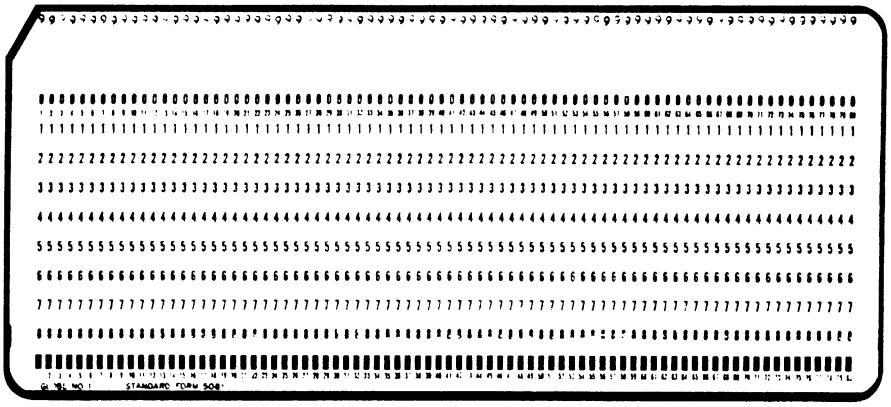
Card 9



Card 10



Card 11



Card 12

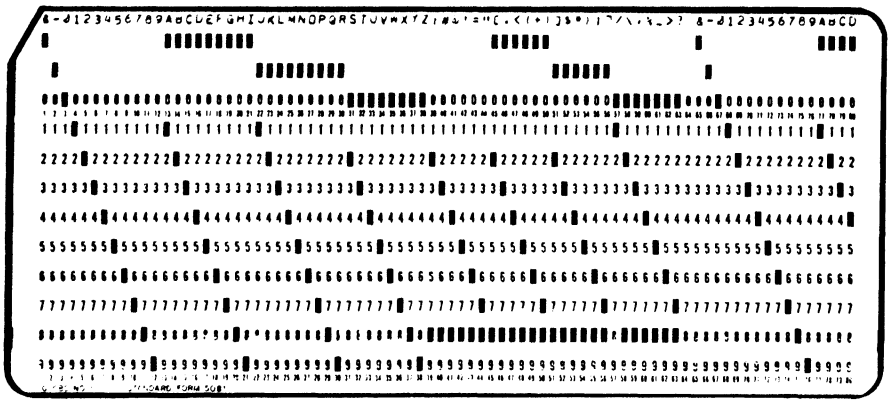
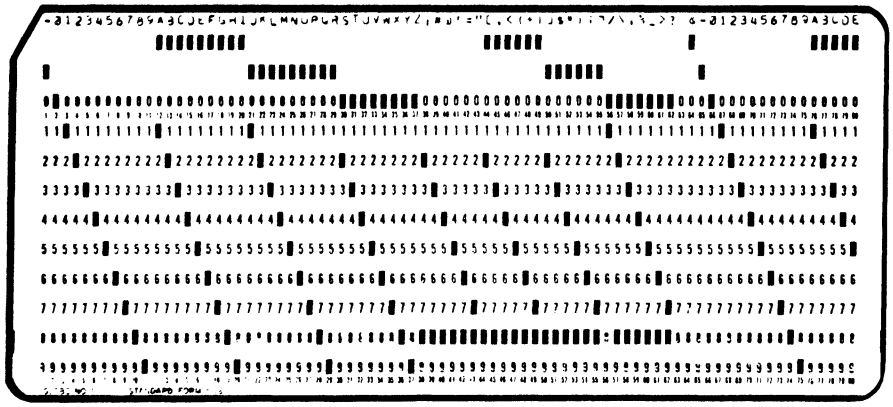


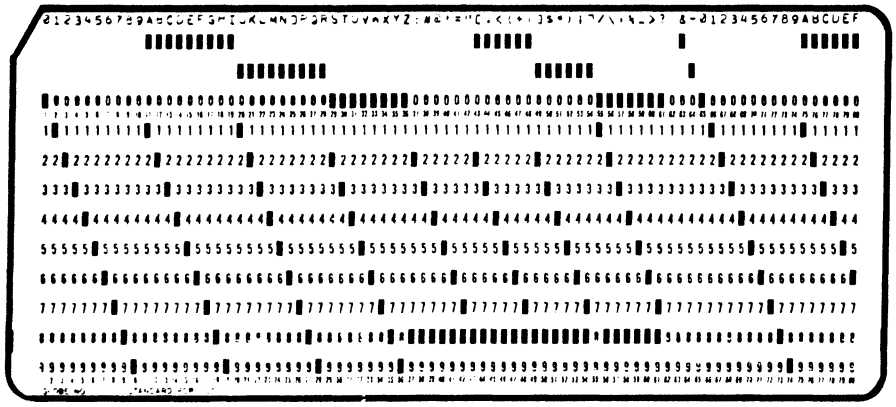
TABLE Vc

Test Cards for Test 6

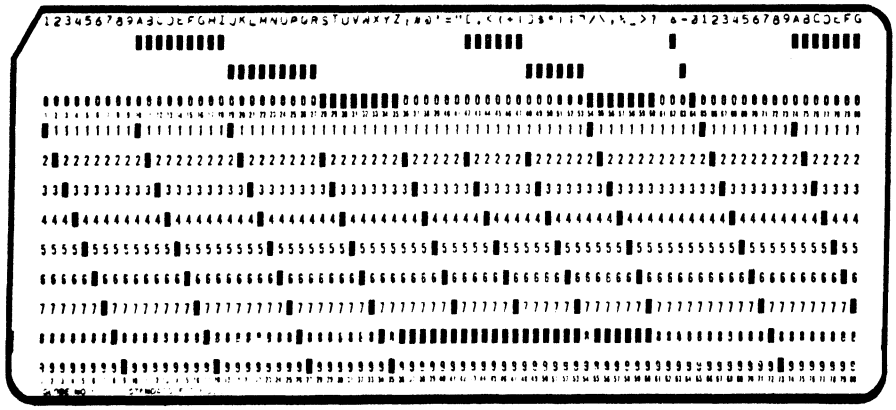
Card 1, 5, and 9



Card 2, 6, and 10



Card 3, 7, and 11



Card 4, 8, and 12

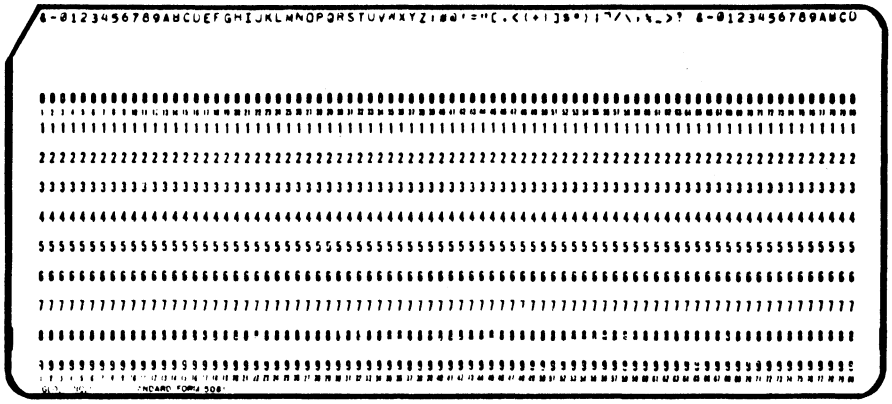
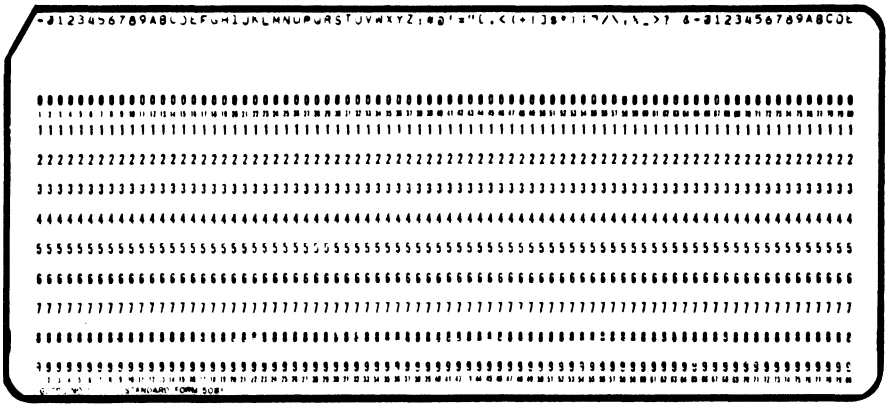


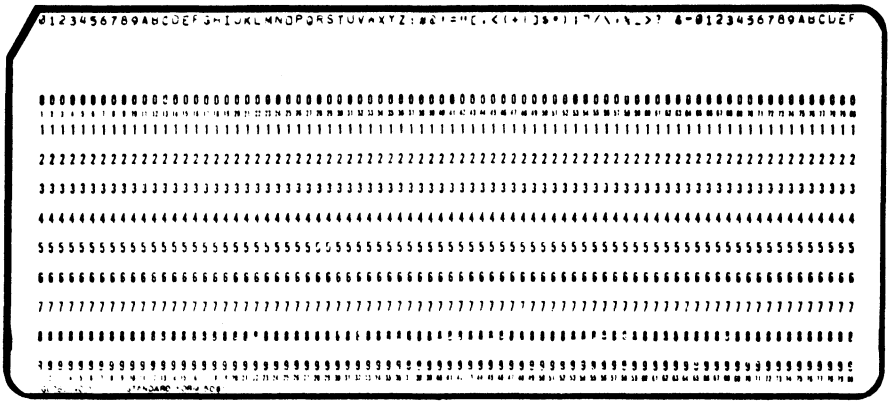
TABLE Vd

Test Cards for Test 7

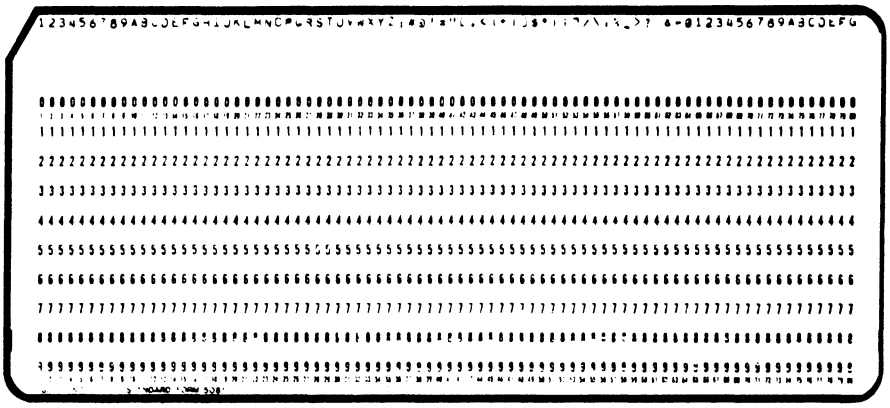
Card 1, 5, and 9



Card 2, 6, and 10



Card 3, 7, and 11



Card 4, 8, and 12

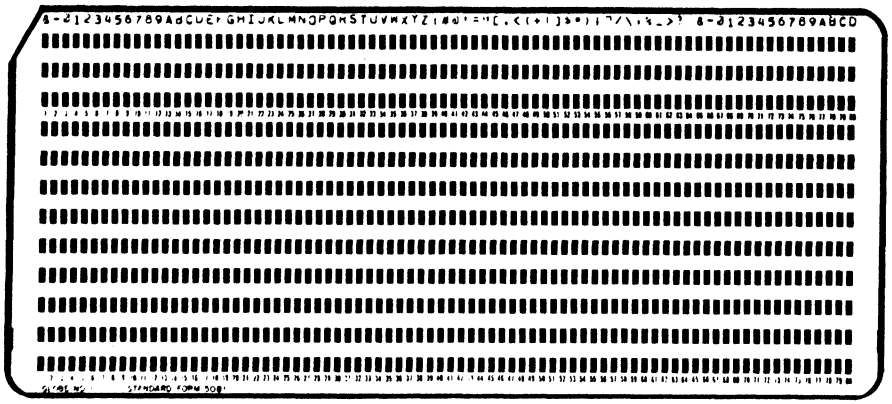
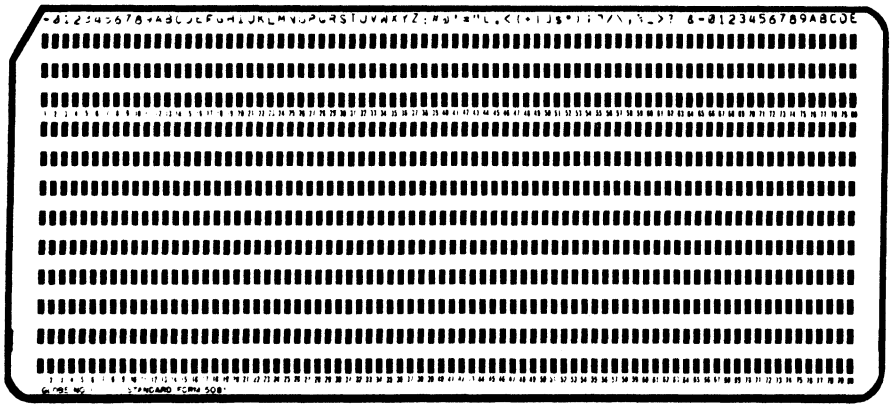


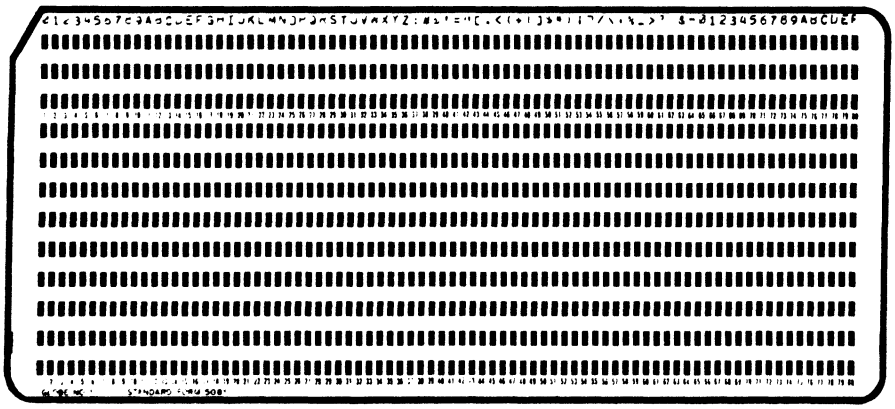
TABLE Ve

Test Cards for Test 8

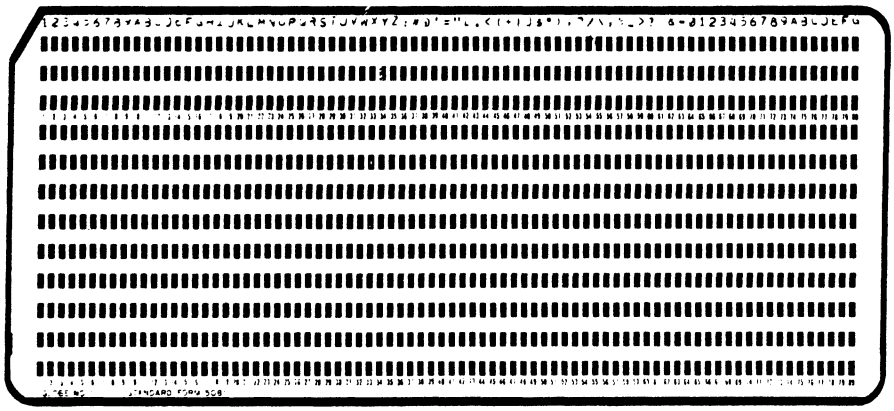
Card 1, 5, and 9



Card 2, 6, and 10



Card 3, 7, and 11



Card 4, 8, and 12

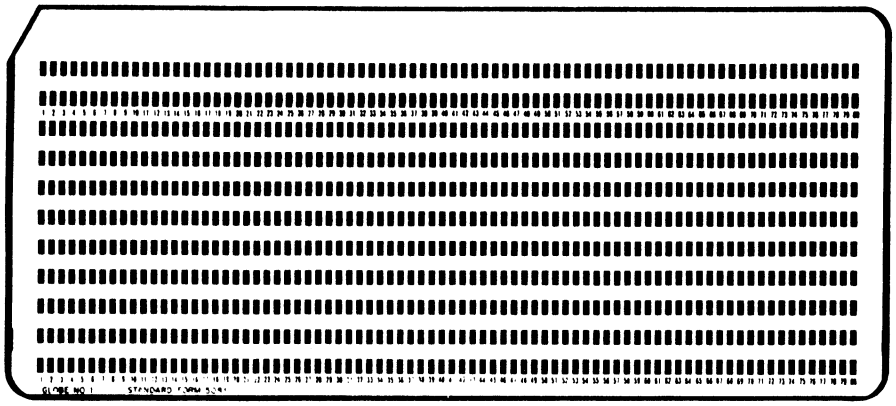
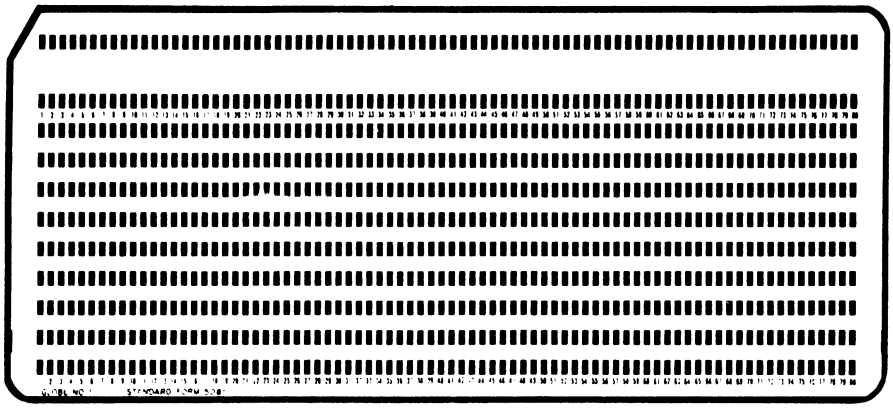
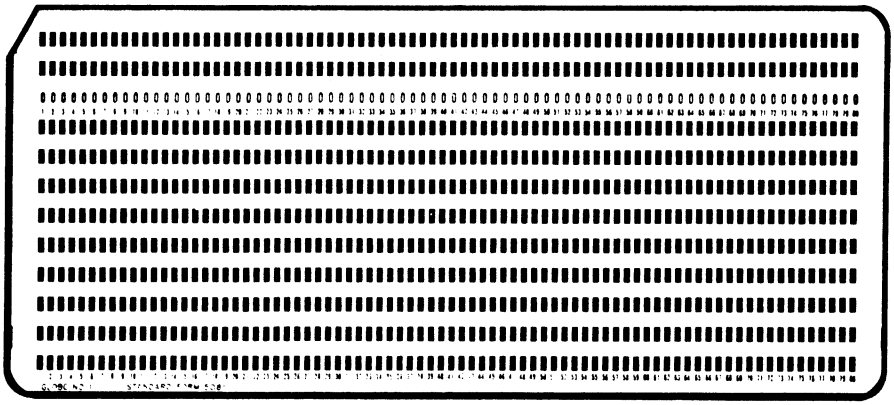


TABLE Vf
Test Cards for Test 9

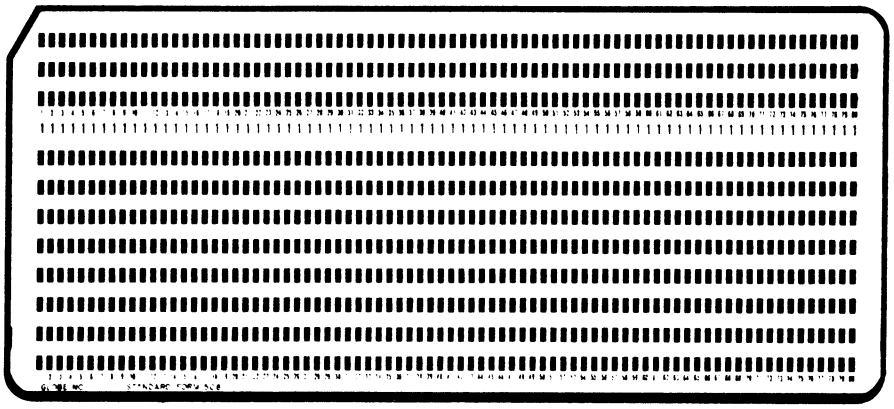
Card 1



Card 2



Card 3



Card 4

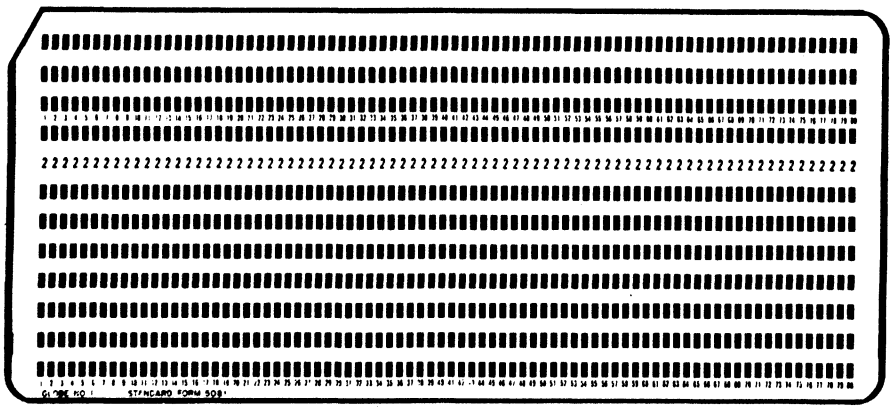
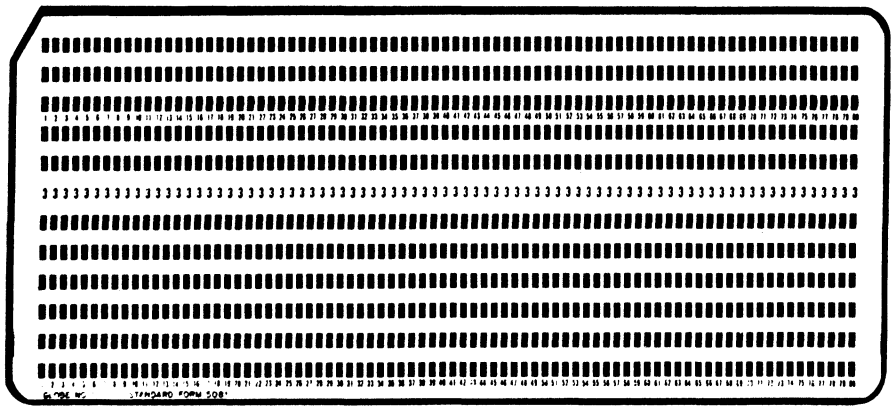
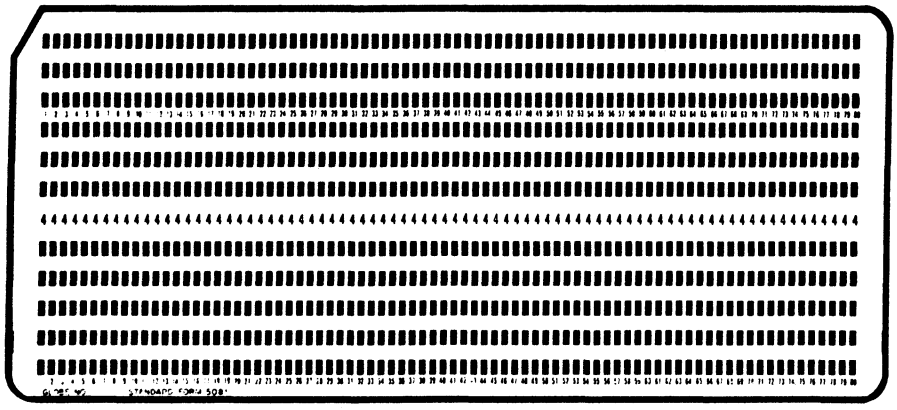


TABLE Vf
(continued)

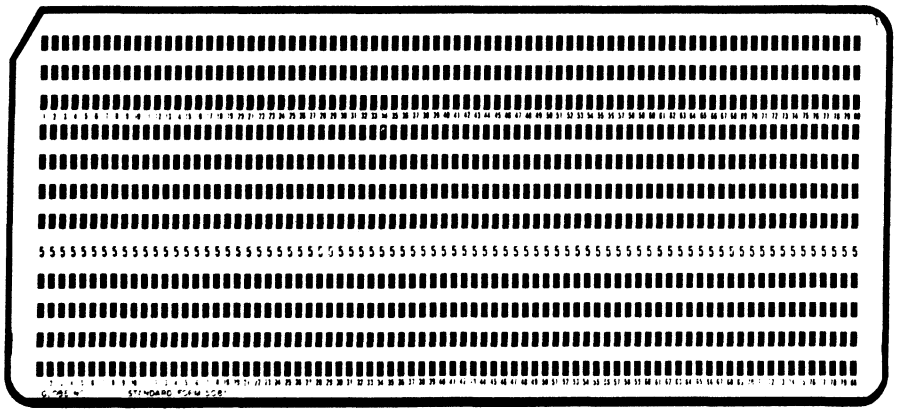
Card 5



Card 6

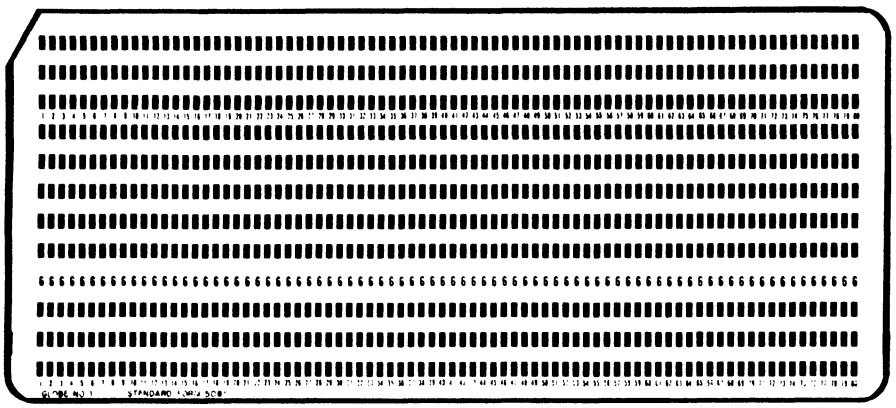


Card 7

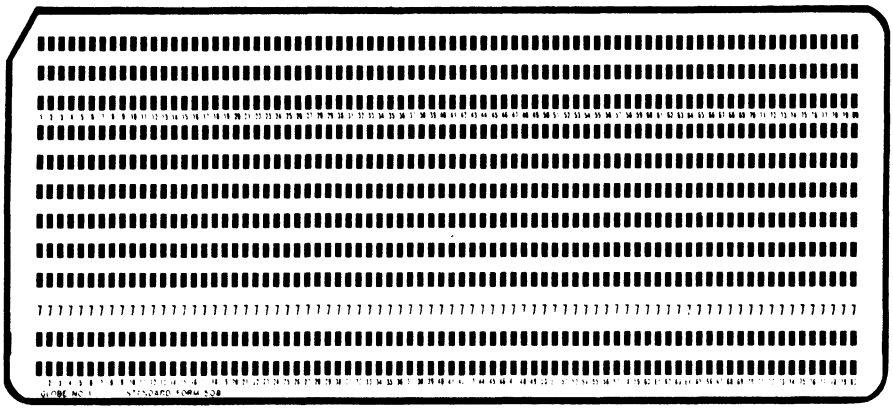


Card 8

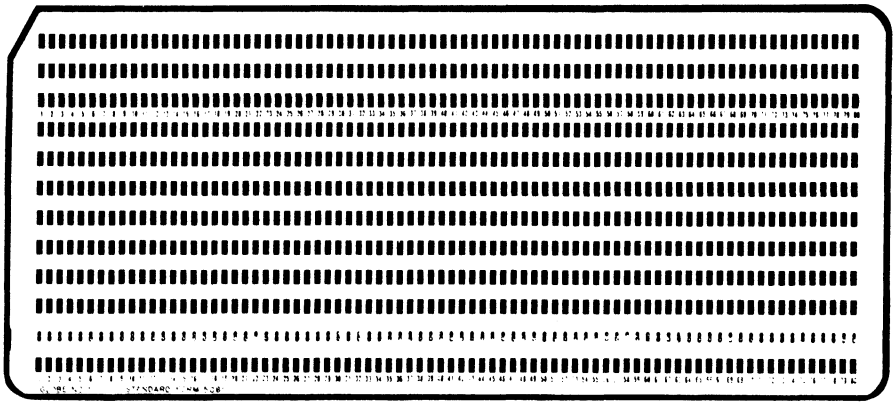
TABLE Vf
(continued)



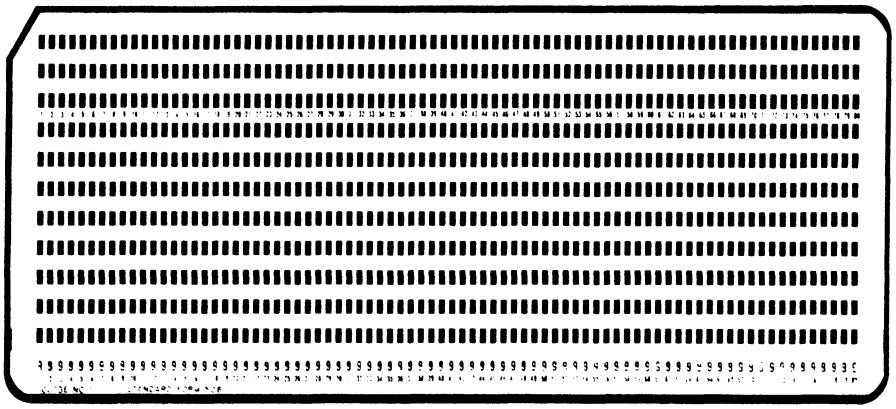
Card 9



Card 10

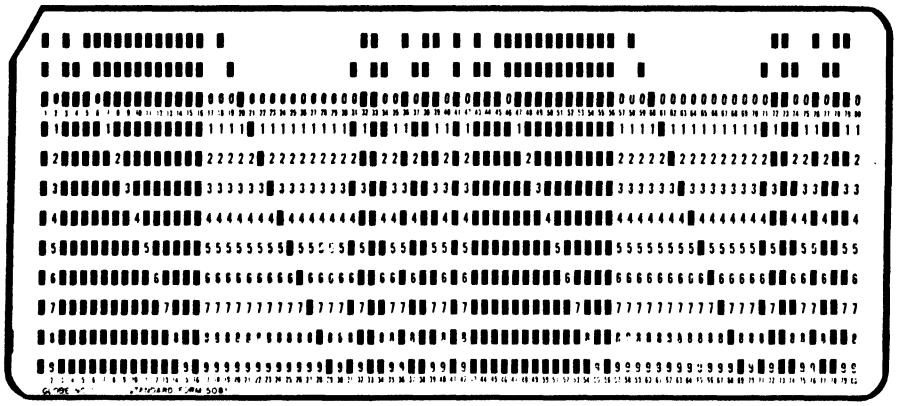


Card 11



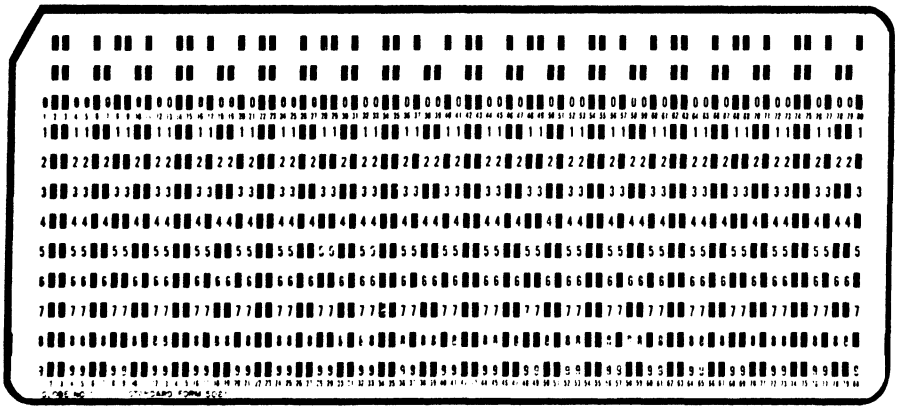
Card 12

TABLE Vg
Test Cards for Test 10



Card 1 through 12

TABLE Vh
Test Cards for Test 11



Card 1 through 12

TABLE VI

LIST OF TESTS

Test Number		Corresponding	
Decimal	Octal	A register bit	Test Title
0	0	0	Basic I/O test for data channel.
1	1	1	Basic I/O test for command channel.
2	2	2	Static status test.
3	3	3	Card motion test.
4	4	4	Basic punch and read (one row).
5	5	5	Basic punch, print, and read (one row).
6	6	6	Punch, print, and read Hollerith.
7	7	7	Print Hollerith and read blanks.
8	10	8	Punch and read laced cards, print separate Hollerith.
9	11	9	Punch and read all but one rows, attempt to print same (non-printable) data.
10	12	10	Punch and read worst case data, attempt to print separate (non-printable) data.
11	13	11	Punch station test (punch and read, attempt to print same non-printable data).
12	14	12	Operator Design.

NOTE: Test cards and data patterns used in each test are shown in Tables Va through Vh.