

HP 2100 AND HP 1000 M/E-SERIES FLOATING POINT DIAGNOSTIC

reference manual

For HP 2100 and HP 1000 M/E-Series Computers

ABSOLUTE BINARY PROGRAM NO. 24320-16001 DATE CODE 1551

LIST OF EFFECTIVE PAGES

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INTRODUCTION



1-1. GENERAL

The Floating Point Diagnostic will test the ability of the floating point firmware in the HP 2100 and HP 1000 M/E-Series computers to execute the FIX, FLT, FAD, FSB, FMP and FDV macroinstructions.

All diagnostic messages and halts will be explained in Tables 4-1 and 4-2.

All numbers in this document will be in octal unless otherwise stated.

1-2. REQUIRED HARDWARE

The following hardware is required to test the 2100 or 21MX Floating Point module:

- a. HP 2100 (with a 12901A Floating Point option installed) or a HP 1000 M/E-Series computer with a minimum 4k memory
- b. An absolute binary loading device (used to load the diagnostic only)
- c. A console device (optional for message reporting)

1-3. REQUIRED SOFTWARE

The following software is required to test the FP instructions:

- a. Diagnostic Configurator
 Absolute Binary Program No. 24296-60001
 Reference Manual Part No. 02100-90157
- Floating Point Diagnostic
 Absolute Binary Program No. 24320-16001
 Diagnostic Manual Part No. 24320-90001

The diagnostic serial number (DSN) is contained in memory location 126 of the program. The DSN for this program is 101207 (prior revisions are not compatible with this reference manual).

PROGRAM ORGANIZATION

SECTION

2-1. ORGANIZATION

The diagnostic program consists of six tests plus the control and initialization sections. The control and initialization sections accept the options selected by the operator. The tests are called into execution by the control section as sequential or selectable subroutines. The following instructions are placed under test by this diagnostic:

Floating Point to Integer (FIX)	TST00
Integer to Floating Point (FLT)	TST01
Floating Point Add (FAD)	TST02
Floating Point Subtract (FSB)	TST03
Floating Point Multiply (FMP)	TST04
Floating Point Divide (FDV)	TST05

2-2. TEST CONTROL AND EXECUTION

The diagnostic outputs a title message to the console for operator information and then executes the test sections by default or according to the options selected in the switch register by the operator. The diagnostic also keeps count of the number of passes that have been completed and will output it at the completion of each pass.

2-3. SELECTION OF TESTS BY OPERATOR

The operator is allowed to select any test section or sequence of test sections with the help of S-Reg bit 9. For actual operation refer to Paragraph 3-4.

2-4. MESSAGE REPORTING

Error messages are used to inform the operator of a failure in the execution of the diagnostic. See Table 4-2. These messages, output only if a console is used, will precede a specified coded error halt.

2-5. DIAGNOSTIC LIMITATIONS

The diagnostic cannot verify errors incurred in the FP ROM module which cause the computer to:

- Alter any memory contents
- Not return from the FP ROM Module
- Not return to the proper P-register setting

OPERATING PROCEDURES

SECTION

3-1. RUNNING THE DIAGNOSTIC

A flowchart of the operating procedure is provided in Figure 3-1.

The program will execute the diagnostic according to the options selected in the S-register. At the completion of each pass of the diagnostic, the pass count is printed on the console device to inform the operator. The computer halts with 102077 displayed in the T-register and the pass count in the A-register. At this point, the operator need only press RUN to execute another pass of the diagnostic.

If S-register bit 12 was selected, the number of passes is printed, and the diagnostic control program will restart the execution of the selected test(s).

3-2. RESTARTING THE DIAGNOSTIC

The program may be restarted by setting the P-register to 100 or 2000, selecting S-register options found in Table 3-2 and pressing RUN.

If a trap cell halt (106077) occurs, the user must determine the cause of the interrupt or transfer control to the location of the M-register which holds the SC of the interrupting trap cell. The program may need to be reloaded to continue.

3-3. TEST SELECTION BY OPERATOR

The control portion of this diagnostic program allows the operator the option of selecting one test or sequence of tests to be run. By setting S-register BIT 9, the operator indicates the desire to make a test selection. When RUN is pressed, the control program will halt (102075) or if the program is running when S-register Bit 9 is selected, the test in progress will be completed before the program halt (102075).

At this time, the operator selects the desired test(s) by setting the A-register bit(s) which equal the desired test number(s). A-register BIT 0 represents Test 00, BIT 1 represents Test 01, etc. For a definition of tests, see Table 3-1.

The operator now must clear S-register BIT 9 and press RUN. The selected test(s) will then be run. To run all tests after special selection, the operator need only set the A-register to zero.

Operating Procedures

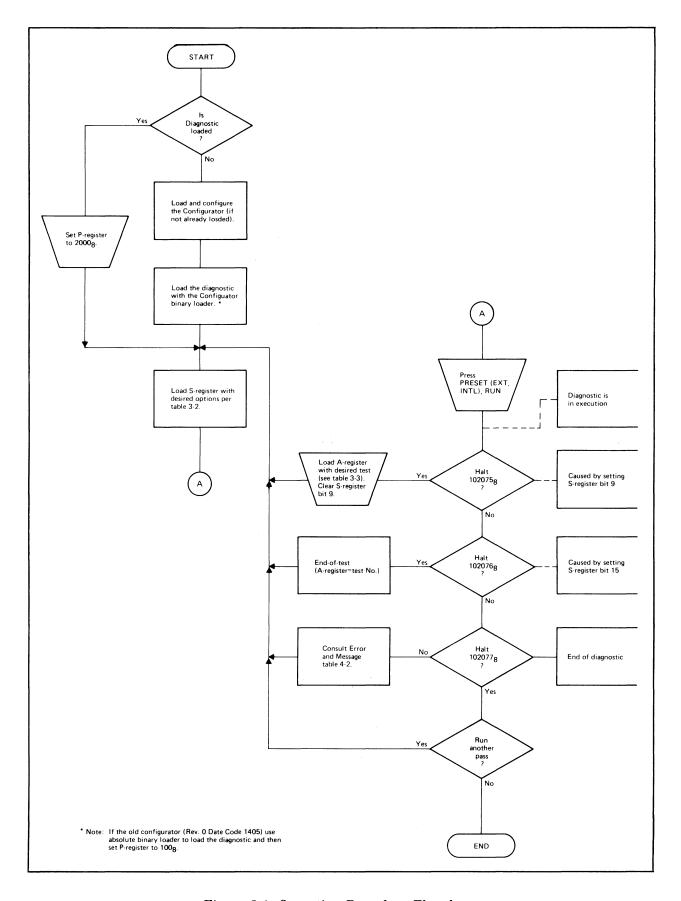


Figure 3-1. Operating Procedure Flowchart

24320 Operating Procedures

Table 3-1. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	TST00-FLOATING POINT TO INTEGER
1	TST01-INTEGER TO FLOATING POINT
2	TST02-FLOATING POINT ADD
3	TST03-FLOATING POINT SUBTRACT
4	TST04-FLOATING POINT MULTIPLY
5	TST05-FLOATING POINT DIVIDE
6-15	NOT SIGNIFICANT
Note: All B-register bits are not	significant.

Table 3-2. Switch Register Options

ВІТ	MEANING IF SET	
15	Halt (102076) at the end of each test; the A-Register will contain the octal equivalent of the test just completed.	
14	Suppress Error Halts	
13	Repeat last test-executed (loop on test)	
12	Repeat all selected tests after diagnostic run is complete without halting. The end of pass message "PASS XXXXXX" will be output before looping.	
11	Suppress error messages.	
10	Supress non-error messages.	
9	Abort the current diagnostic execution and halt (102075); user may at this time specify a new set of tests in the A/B register, clear bit 9 of the Switch Register and press run (see Paragraph 3-4).	
8-0	Not significant	

TEST DESCRIPTIONS

SECTION

IV

4-1. GENERAL

Every test section executes a software and then the equivalent firmware floating point instruction on a set of data. The results of the two executions are compared for equality. Each data pattern of 32 bits is rotated 32 different times to generate random data patterns from the original data pattern. The set of data patterns selected in this diagnostic insures any branch of any algorithm used in the M-Series, E-Series or 2100 Firmware is tested. Also, proper indirect operand addressing is verified in TST02-05.

4-2. DESCRIPTION OF TST00

TST00 verifies proper execution of the floating point to integer (FIX) instruction. This includes returning a zero in the A-register when the floating point number is less than one and returning 77777 if the number is greater than 2¹⁶.

4-3. DESCRIPTION OF TST01

TST01 verifies proper execution of the integer to floating point (FLT) instruction. All values from 0 to 177777 are tested.

4-4. DESCRIPTION OF TST02

TST02 verifies proper execution of the floating point add (FAD) instruction. This includes verifying overflow if the result is outside the range $(1-2^{-23})^*-2^{127}$ through $(1-2^{-23})^*2^{127}$ and verifying underflow if the result is within the range $(1+2^{-22})^*-2^{-129}$ through $(1+2^{-22})^*2^{-129}$.

4-5. DESCRIPTION OF TST03

TST03 verifies proper execution of the floating point subtract (FSB) instruction. Overflow and underflow are checked as in the FAD instruction (see Paragraph 4-4).

4-6. DESCRIPTION OF TST04

TST04 verifies proper execution of the floating point multiply (FMP) instruction. Overflow and underflow are checked as in the FAD instruction (see Paragraph 4-4).

Test Descriptions 24320

Table 4-1. Halt Code Summary

or (E) messages 00-06
er Selection request d of Test (A=octal test number) d of Diagnostic Run (A=PASS COUNT) fer to Configurator Manual p cell halts in locations 2-77
End Ref

Table 4-2. Error Information Messages and Halt Codes

HALT CODE	TEST	MESSAGE	COMMENTS
102000	00	E000 FIX	FIX FAILURE*
102001	01	E001 FLT	FLT FAILURE*
102002	02	E002 FSB	FAD FAILURE*
102003	03	E003 FSB	FSB FAILURE*
102004	04	E004 FMP	FMP FAILURE*
102005	05	E005 FDV	FDV FAILURE*
102006	02-05	NONE	Secondary error halt where:
			A=Test Pattern in Operand (upper 16 Bits)
			B=Test Pattern in Operand (lower 16 Bits)
			(Press RUN for additional information)
102007	00-05	NONE	SEQUENTIAL ERROR HALT where:
			A=Actual result in A
			B=Actual result in B
			O-REG=Actual overflow result
			(Press RUN for additional information)
102010	00-05	NONE	SEQUENTIAL ERROR HALT where:
			A=Expected A-Register
			B=Expected B-Register
			O-REG=Expected Overflow Register
103002	02	E102 FAD	INDIRECT OPERAND
			FAD FAILURE*
103003	03	E103 FSB	INDIRECT OPERAND
			FSB FAILURE*
103004	04	E104 FMP	INDIRECT OPERAND
			FMP FAILURE*
103005	05	E105 FDV	INDIRECT OPERAND
			FDV FAILURE*
NONE		2100-21MX	INTRODUCTORY MESSAGE
		FLOATING POINT	
	Į.	DIAGNOSTIC	
NONE		PASS XXXXXX	INDICATES NUMBER OF DIAGNOSTIC
			PASSES COMPLETED
NONE	00-05	TEST XX	INFORMATION MESSAGE PRIOR TO
			ERROR MESSAGES

 $^{^*}A=Test$ Pattern in A

B=Test Pattern in B

Press RUN for additional information

24320 Test Descriptions

4-7. DESCRIPTION OF TST05

TST05 verifies proper execution of the floating point divide (FDV) instruction. Overflow and underflow are checked as in the FAD instruction (see Paragraph 4-4).

If a console device has been chosen during configuration and an error has been detected, only primary error halts (102000-102005 or 103002-103005) will be reached after the following message has been output:

TEST PATTERN IN A AND B $A = XXXXXX \qquad B = XXXXXX$ TEST PATTERN IN OPERAND* $XXXXXX \qquad XXXXXX*$ ACTUAL RESULT $A = XXXXXX \qquad B = XXXXXX \qquad OVF = X$ EXPECTED RESULT $A = XXXXXX \qquad B = XXXXXX \qquad OVF = X$

^{*}NOTE: Not included in test 00 or 01.

