HEWLETT
PACKARD

ABSOLUTE BINARY PROGRAM NO. 24322-16002
DATE CODE 1705

Direct Memory Access (DMA) Dual Channel Port Controller (DCPC) Diagnostic

Reference Manual

For HP 2100A/S and HP 1000 M/E/F-Series Computers

NOTICE

The absolute binary code for this diagnostic is contained on one or more media (e.g., paper tape, cartridge tape, disc, and magnetic tape). The binaries also exist on single as well as multiple files. For the current date code(s) associated with these media, refer to Appendix A in the *Diagnostic Configurator Manual,* part no. 02100-90157, dated August 1976 or later.

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Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what software manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

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INTRODUCTION

SECTION I

1-1. GENERAL

This diagnostic program confirms proper operation of the Direct Memory Access (DMA) in the HP 2100A/S Computer or the Dual Channel Port Controller (DCPC) in the HP 1000 M/E/F-Series Computer. This confirmation is achieved by testing the ability of DMA[1] to transfer data approaching the maximum rate possible and verifying the ability of the Word Count Registers (WCR) and Memory Address Registers (MAR) to count sequentially up to 32K.

1-2. REQUIRED HARDWARE

The following hardware is required.

a. HP 2100 or HP 1000 M/E/F-Series Computer with a minimum 4K memory.

b. DMA or DCPC option installed. On an HP 2100, the DMA card A9 requires a special test connector, part no. 1251-0335. Any 2x24 pin connector with no interconnected pins can be used.

c. A loading device for loading the diagnostic program and Configurator.

d. A console device for message reporting (recommended but not required).

e. HP 12554A 16-Bit Duplex Register, 12597A 8-Bit Duplex Register, 12566B/C Microcircuit Interface (12566A not suitable), or 12930A Universal Interface.

The following test connectors are used with the interface cards.

INTERFACE CARD	TEST CONNECTOR	USED FOR TEST
12554A	1251-0332	00-14
12597A	1251-0332	00-14
12566B/C	1251-0332	00-14
12930-60001	12930-60006	00-14
12930-60001 (two cards)	Special cable (see appendix A)	15 (see appendix A)

CAUTION

When the 12566B/C interface card is used, pins 22,Z have to be connected to pins 23,AA on the 1251-0332 test connector. A test connector with this modification can still be used for 12554A and 12597A cards.

1-3. JUMPER AND SWITCH SETTINGS

Jumper and switch configuration requirements for interface cards are given in table 1-1.

---

[1] DMA refers to either DMA or DCPC.

Table 1-1. Jumper and Switch Settings (TST00-TST14)

HP 12554A 16-BIT DUPLEX REGISTER
(Either Configuration 1 or Configuration 2 can be used)

CONFIGURATION 1		CONFIGURATION 2	
JUMPERS	POSITION	JUMPERS	POSITION
W4-W6	B	W4-W5	A
W7	A	W6-W7	B
W8-W12	IN	W8-W12	IN
W13	A (if applicable)	W13	A (if applicable)
W14	A (if applicable)	W14	A (if applicable)

HP 12597A 8-BIT DUPLEX REGISTER
(Either Configuration 1 or Configuration 2 can be used)

CONFIGURATION 1		CONFIGURATION 2	
JUMPERS	POSITION	JUMPERS	POSITION
W1-W2	A	W1-W2	B
W3-W4*	IN	W8*	IN

*W3 and W8 *must not* be installed at the same time.

HP 12930A UNIVERSAL INTERFACE (12930-60001)
(These switch settings are only applicable for TST00-TST14)

SWITCH	POSITION	SWITCH	POSITION
U85S1	1	U102S1	2
S2	5	S2	7
S3	10(0)	S3	10(0)
U87S1	1	U106S1	1
S2	4	S2	5
S3	8	S3	9
U97S1	2		
S2	5		
S3	10(0)		

Note: These programmable switches are set using a screwdriver to position the contact mechanism. See figure A-3 for switch locations and switch positions.

Switch settings are for 12930A with diagnostic test connector (12930-60006) when running the standard test run (tests 0-14). When running test 15, switch U85S1 is configured differently. See table A-1.

Table 1-1. Jumper and Switch Settings (TST00-TST14) (Continued)

HP 12566B/C MICROCIRCUIT INTERFACE

	12566B	12566C
W1	C	C
W2	B	B
W3	B	B
W4	B	B
W5	IN	OUT
W6	IN	OUT
W7	IN	OUT
W8	IN	OUT
W9	A	A
W10	NA	B
W11	NA	IN
W12	NA	OUT
W13	NA	OUT

1-4. SOFTWARE REQUIREMENTS

The following software is required:

a. HP 1000 M/E/F-Series Computer Systems Diagnostic Configurator used for equipment configuration and as a console device driver. The product includes the following:

   Binary object tape, part no. 24296-60001
   Reference manual, part no. 02100-90157

b. DMA/DCPC Diagnostic

   Binary object tape, part no. 24322-16002
   Reference manual, part no. 24322-90002

The diagnostic serial number (DSN), which is contained in memory location 126 (octal), is 101220 (octal). The approximate execution time to run TST00-TST14 successfully is 1 minute.

PROGRAM ORGANIZATION

SECTION

II

2-1. ORGANIZATION

This diagnostic program consists of 16 tests plus Control and Initialization sections. The Control and Initialization sections accept the select code and options required by the tests, which are called into execution by the Control section as sequential or selectable subroutines. The following circuits are placed under test by this diagnostic:

TST00 — DMA Flag Test
TST01 — DMA Interrupt Test
TST02 — DMA Control Reset Test
TST03 — Preset Test
TST04 — Priority Test
TST05 — Basic Word Count Register Test
TST06 — Basic Word Count Rollover Test
TST07 — STC Decision Control Test
TST08 — CLC Decision Control Test
TST09 — DMA CLF Test
TST10 — Illegal Select Code Test
TST11 — Incremental Word Count Register Test
TST12 — Incremental Memory Address Register Test
TST13 — DMA Input Transfer Test
TST14 — STC, CLF and Override Test

A special test (TST15), which is described in appendix A, is not part of the standard test run and is entered only by selecting two select codes during configuration. Test 15 is run in the same manner as described in paragraph 2-2 with the exception that "test selection by operator" or "default" is omitted. (Refer to paragraphs 2-2 and 2-3).

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device (if present) for operator information and then executes the tests according to the options selected on the Switch Register. The Control section primarily checks Switch Register bits 15, 13 and 12.

The Control section keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if Switch Register bit 10 is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed. Refer to paragraph 2-3.

2-3. TEST SELECTION BY OPERATOR

The Control portion of the program allows the operator the option of selecting a test or sequence of tests to be executed. The operator sets Switch Register bit 9 to indicate that he wants to make a selection and presses RUN. The computer will come to a halt 102075 (octal) to indicate it is ready for the selection. If the program is running, the test in progress will be completed and then the program will halt. The operator then loads the A-register with the test(s) desired. A-register bit 0 represents test 00, bit 1 represents test 01, and so on up to A-register bit 14. The operator must then clear Switch Register bit 9 and press RUN. The operator-selected test(s) will then be run. If the A-register is cleared, all tests (0-14) will be executed. See table 3-3.

2-4. MESSAGE REPORTING

There are two types of messages: error and information. Error messages are used to inform the operator of a failure of DMA to respond to a given control or sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some operations related to the unit's function. In this case, an associated halt will occur to allow the operator time to perform the operation; the operator must then press RUN.

If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available.

Example—Error with halt
    Message: E000 CLF-SFS6
    Halt Code: 102000 (T-register or Memory Data Register)

Example—Information with halt
    Message H324 PRESS RESET AND RUN
    Halt Code: 107024

Example—Information only
    Message: DMA-DCPC DIAGNOSTIC
    Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by setting Switch Register bit 10. Tests that require operator intervention are suppressed by setting Switch Register bit 8. When Switch Register bit 12 is set, the selected tests will be repeated and all operator intervention will be suppressed.

2-5. DIAGNOSTIC LIMITATIONS

If the DMA diagnostic is run on a computer with 8K or less of memory, complete operation of the DMA Memory Address Register bits 13 and 14 cannot be verified.

OPERATING PROCEDURES

SECTION III

3-1. OPERATING PROCEDURE FLOWCHART

A flowchart of the operating procedure is provided in figure 3-1. Connect the appropriate test connector to the interface as specified in paragraph 1-2. Set the interface jumpers (or switches) as listed in table 1-1.

3-2. RUNNING THE DIAGNOSTIC

The program will execute the diagnostic according to options selected in the Switch Register. At the completion of each pass of the diagnostic, the pass count is printed on the console device for operator information. If Switch Register bit 12 was not set, the computer will halt with 102077 (octal) in the Memory Data Register. At ths point, the A-register contains the pass count. To run another pass, the operator need only press RUN.

3-3. RESTARTING

The program may be restarted by setting the P-register to 2000 (octal). Select Switch Register options shown in table 3-1 and press RUN.

If a trap cell halt occurs (106077 octal), the user must determine the cause of the interrupt or transfer of control to the location shown in the M-register. The program may need to be reloaded to continue.

3-4. FULL-SPEED TESTING (HP 2100 ONLY)

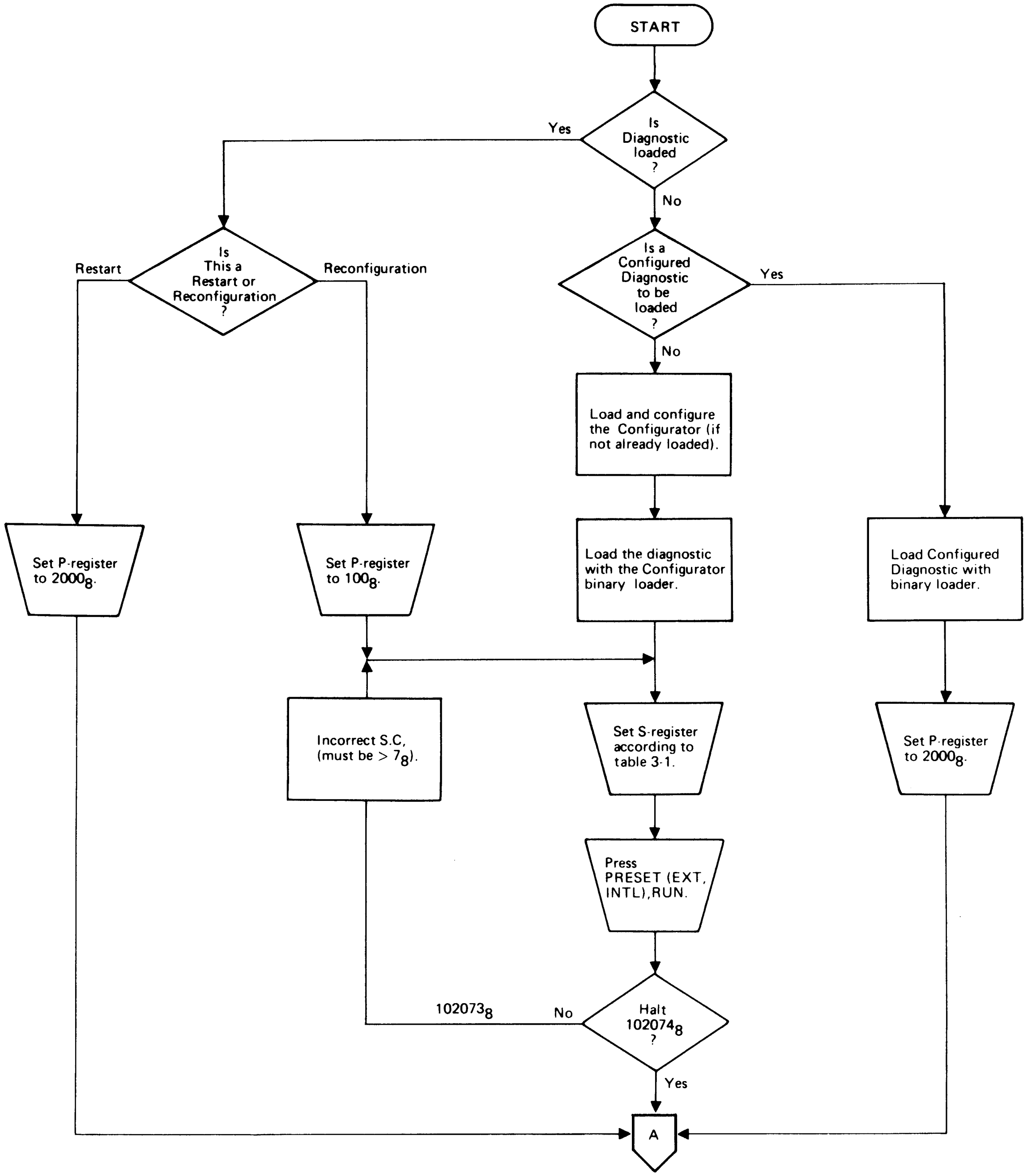
This mode of testing may be induced by shorting pins W and X to pin BB on the DMA test connector (part no. 1251-0335) attached to the 2100 DMA board in location A9. However, the operator must observe several restrictions:

a. May only be used with a 12566B/C as the test interface.

b. May only be used on a 2100A/S.

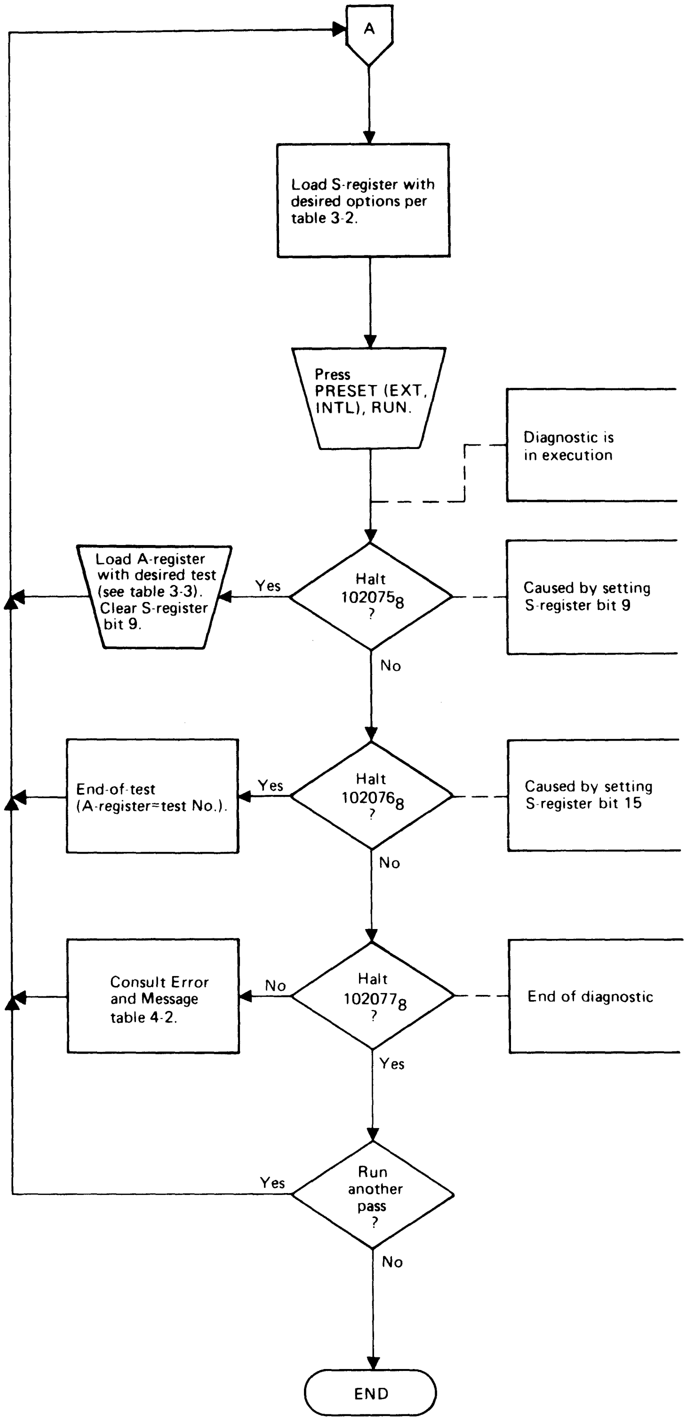
c. Tests 9 and 11 will fail; these tests should be omitted using test selection by the operator. (Refer to paragraph 2-3).

d. A normal pass without the shorted DMA should be made prior to a full-speed pass.


START
Is Diagnostic loaded ?
Yes
No
Is This a Restart or Reconfiguration ?
Restart
Reconfiguration
Is a Configured Diagnostic to be loaded ?
Yes
No
Load and configure the Configurator (if not already loaded).
Set P-register to 2000₈.
Set P-register to 100₈.
Load the diagnostic with the Configurator binary loader.
Load Configured Diagnostic with binary loader.
Incorrect S.C, (must be > 7₈).
Set S-register according to table 3-1.
Set P-register to 2000₈.
Press PRESET (EXT, INTL),RUN.
102073₈
No
Halt 102074₈ ?
Yes
A

7300-1

Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)


A
Load S-register with desired options per table 3-2.
Press PRESET (EXT, INTL), RUN.
Diagnostic is in execution
Load A-register with desired test (see table 3-3). Clear S-register bit 9.
Yes
Halt 102075₈ ?
Caused by setting S-register bit 9
No
End-of-test (A-register=test No.).
Yes
Halt 102076₈ ?
Caused by setting S-register bit 15
No
Consult Error and Message table 4-2.
No
Halt 102077₈ ?
End of diagnostic
Yes
Yes
Run another pass ?
No
END

7300-2

Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-1. Initial Switch Register Options

BITS	MEANING
TESTS 00 THROUGH TEST 14	
5–0	Select Code of 12554A, 12597A, 12566B/C or 12930A Interface card.
15–6	Reserved
SPECIAL TEST 15 (REFER TO APPENDIX A)	
5–0	Select Code of 12930A (first card).
9–6	Select Code of 12930A (second card).
15–10	Reserved

Table 3-2. Switch Register Test Options

BITS	MEANING IF SET
0	Abort current test when reporting error.*
7–1	Reserved.
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (102075). User may specify a new group of tests in the A-register (see table 3-3), clear bit 9, and then press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 10 is set or teleprinter is not present. Also, those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at the end of each test; the A-register will contain the test number in octal.

*Bit 0 is used to abort the current test when errors are being reported. This is useful in a test that prints a long list of errors. When errors are being printed and the operator sets bit 0, the next or current error will be printed. The program then clears Switch Register bit 0 and aborts the current test.

Table 3-3. Test Selection

A-REG BIT (IF SET)	TESTS SELECTED
0	TST00 — DMA Flag test
1	TST01 — DMA Interrupt test
2	TST02 — DMA Control Reset test
3	TST03 — Preset test
4	TST04 — Priority test
5	TST05 — Basic Word Count Register test
6	TST06 — Basic Word Count Rollover test
7	TST07 — STC Decision Control test
8	TST08 — CLC Decision Control test
9	TST09 — DMA CLF test
10	TST10 — Illegal Select Code test
11	TST11 — Incremental Word Count Register test
12	TST12 — Incremental Memory Address Register test
13	TST13 — DMA Input Transfer test
14	TST14 — STC, CLF and Override test
Note: Test 15 cannot be selected by A-register.	

DIAGNOSTIC PERFORMANCE

SECTION IV

4-1. PRETEST AND CONFIGURATION

A pretest is made on the I/O interface test card during configuration. If the test card fails, halt 102072 will occur and the I/O test card must be repaired or replaced before proceeding. A halt 102074 indicates that the test card and the I/O select code are valid.

4-2. TEST DESCRIPTIONS

4-3. DMA INTERRUPT TEST (TST00)

Tests the DMA Flag and SKF logic via the STF, CLF, SFS and SFC instructions.

4-4. DMA INTERRUPT TEST (TST01)

Tests the ability of DMA to interrupt, to be held off from interrupting, and to hold off or allow lower priority interrupts.

4-5. DMA CONTROL RESET TEST (TST02)

Tests the ability of CRS and CLC DMA to clear the DMA Control flip-flops.

4-6. PRESET TEST (TST03)

Ensures PON and PRSE generated from the display (operator) panel PRESET switch(es) sets the DMA Flag flip-flops.

4-7. PRIORITY TEST (TST04)

Tests the ability of the DMA to receive, propagate, or deny interrupt priority logic signals PRH and PRL.

4-8. BASIC WORD COUNT REGISTER TEST (TST05)

This test section outputs all patterns to the word count registers while verifying the ability to read back the proper pattern.

4-9. BASIC WORD COUNT ROLLOVER TEST (TST06)

Tests the ability of the word count registers to rollover from all one's to all zero's and to set the DMA Flag flip-flops.

4-10. STC DECISION TEST (TST07)

Tests the ability of DMA to generate or not generate a STC signal during DMA cycle.

4-11. CLC DECISION TEST (TST08)

Tests the ability of DMA to generate or not generate a CLC signal during the last DMA cycle.

4-12. DMA CLF TEST (TST09)

Tests the ability of DMA to generate a CLF signal during a DMA cycle.

4-13. ILLEGAL SELECT CODE TEST (TST10)

Ensures select codes 2,3,6 and 7 are not illegally decoded from any other select codes.

4-14. INCREMENTAL WORD COUNT REGISTER TEST (TST11)

Executes sequential two-word transfers, which exercise and test the ability of the word count registers to increment from an all zero's state to an all one's state. This approach simulates 65K word transfers.

4-15. INCREMENTAL MEMORY ADDRESS REGISTER TEST (TST12)

Executes sequential two-word DMA output transfers from every computer memory address starting at address 2. This sequence continues through 32K of memory transfers regardless of the physical memory installed in the computer. This test approach verifies the ability of the DMA memory address registers to increment from address 2 through address 77777_8.

4-16. DMA INPUT TRANSFER TEST (TST13)

Verifies proper operation of the DMA input transfer logic.

4-17. STC, CLF AND OVERRIDE TEST (TST14)

Verifies no STC or CLF occurs on the last DMA input transfer and that a DMA1 cycle holds off a DMA2 cycle.

4-18. ERROR INFORMATION MESSAGES/HALT CODES

Table 4-1 will summarize the halt codes and table 4-2 provides a complete description of the individual halts.

Table 4-1. Halt Code Summary

HALT	MEANING
TESTS 00 THRU 14	
102000-102067	Error (E) and information (H) messages 00-67.
103000-103006	Error (E) and information (H) messages 100-106.
107024	Error (E) Message 324.
CONTROL	
102072	Test interface didn't respond correctly.
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of test (A-register = test number).
102077	End of diagnostic run.
106077	Trap cell halts in location 2-77.
106070-106076	Refer to *Diagnostic Configurator Reference Manual.*
Note: See table 4-2 for a complete explanation of individual halts.	
TEST 15	
103007-103016	Error (E) Message 107-116.
Note: See table A-2 for a complete explanation of individual halts.	

Table 4-2. Error Information Messages and Halt Codes (TST00-TST14)

HALT CODE	SECTION	MESSAGES	COMMENTS
102000	00	E000 CLF-SFS 6	CLF 6 did not clear DMA1 Flag or SFS 6 caused a skip with DMA1 Flag clear.
102001	00	E001 CLF-SFC 6	SFC 6 didn't skip with DMA1 Flag clear.
102002	00	E002 STF-SFC 6	STF 6 didn't set DMA1 Flag or SFC 6 caused a skip with DMA1 Flag set.
102003	00	E003 STF-SFS 6	SFS 6 didn't skip with DMA1 Flag set.
102004	00	E004 CLF-SFS 7	CLF 7 didn't clear DMA2 Flag or SFS 7 caused a skip with DMA2 Flag clear.
102005	00	E005 CLF-SFC 7	SFC 7 didn't skip with DMA2 Flag clear.
102006	00	E006 STF-SFC 7	STF 7 didn't set DMA2 Flag or SFC 7 caused a skip with DMA2 Flag set.
102007	00	E007 STF-SFS 7	SFS 7 didn't skip with DMA2 Flag set.
102010	01	E010 ILLEGAL DMA1 INT	DMA1 interrupted with interrupt system off.
102011	01	E011 ILLEGAL DMA2 INT	DMA2 interrupted with interrupt system off.
102012	01	E012 NO DMA1 INT	DMA1 didn't interrupt after STC 6, STF 6, STF 0.
102013	01	E013 ILLEGAL DMA1 INT	IAK didn't disable DMA1 interrupts.
102014	01	E014 ILLEGAL DMA1 INT	DMA1 interrupted from wrong location: A=actual interrupt location B=expected interrupt location.
102015	01	E015 NO DMA2 INT	DMA2 didn't interrupt after STC 7, STF 7, STF 0.
102016	01	E016 ILLEGAL DMA2 INT	IAK didn't disable DMA2 interrupts.

Table 4-2. Error Information Messages and Halt Codes (TST00-TST14) (Continued)

HALT CODE	SECTION	MESSAGES	COMMENTS
102017	01	E017 ILLEGAL DMA2 INT	DMA2 interrupted from wrong location. A=actual interrupt location B=expected interrupt location.
102020	02	E020 DMA1 CRS	CLC 0 didn't clear DMA1 Control FF.
102021	02	E021 DMA2 CRS	CLC 0 didn't clear DMA2 Control FF.
102022	02	E022 CLC 6	CLC 6 didn't clear DMA1 Control FF.
102023	02	E023 CLC 7	CLC 7 didn't clear DMA2 Control FF.
102024	03	E024 DMA PRESET	PRESET didn't set DMA1 Flag FF.
102025	03	E025 DMA2 PRESET	PRESET didn't set DMA2 Flag FF.
102026	04	E026 PRIORITY	DMA1 priority didn't hold off DMA2 from interrupting.
102027	04	E027 PRIORITY	DMA2 priority didn't hold off I/O from interrupting.
102030	04	E030 PRIORITY	DMA1 priority didn't hold off I/O from interrupting.
102031	04	E031 PRIORITY	DMA1 cycle didn't inhibit an I/O interrupt.
102032	10	E032 SC DECODE	A-REG contains instruction which erroneously executed an LIA 2
102033	05	E033 WCR1 EXP=XXXXXX ACT=XXXXXX	Basic output-input operation to WCR1 failed: A=output data to WCR1 B=bad data returned from WCR1.
102034	05	E034 WCR2 EXP=XXXXXX ACT=XXXXXX	Basic output-input operation to WCR2 failed: A=output data to WCR2 B=bad data returned from WCR2.
102035	05	E035 DMA1 CRS	CLC 0 didn't clear WCR2 Control FF.
102036	05	E037 NO DMA1 INT	DMA1 didn't interrupt after a one-word transfer.

Table 4-2. Error Information Messages and Halt Codes (TST00-TST14) (Continued)

HALT CODE	SECTION	MESSAGES	COMMENTS
102037	06	E037 NO DMA1 INT	DMA1 didn't interrupt after a one-word transfer.
102040	06	E040 NO DMA2 INT	DMA2 didn't interrupt after a one-word transfer.
102041	06	E041 WCR1	After a DMA1 interrupt after a one-word transfer, WCR1 should be zero and wasn't: A=actual WCR1 contents.
102042	06	E042 WCR2	After a DMA2 interrupt after a one-word transfer, WCR2 should have been zero but wasn't: A=actual WCR2 contents.
102043	07	E043 DMA1 STC FF	DMA1 didn't generate a STC on last output transfer with control word bit 15 set.
102044	07	D044 DMA1 STC FF	DMA1 generated an STC on last output tranfer with control word bit 15 clear.
102045	07	E045 DMA2 STC FF	DMA2 didn't generate an STC on last output transfer with control word bit 15 set.
102046	07	E046 DMA2 STC FF	DMA2 generated an STC on last output transfer with control word bit 15 clear.
102047	08	E047 DMA1 CLC FF	DMA1 didn't generate a CLC on last output transfer with control word bit 13 set.
102050	08	E050 DMA1 CLC FF	DMA1 generated a CLC on last output transfer with control word bit 13 set.
102051	08	E051 DMA2 CLC FF	DMA2 didn't generate a CLC on last output transfer with control word bit 13 set.
102052	08	E052 DMA2 CLC FF	DMA2 generated a CLC on last output transfer with control word bit 13 clear.
102053	09	E053 DMA1 CLF	DMA1 didn't generate a CLF during an output transfer.

Table 4-2. Error Information Messages and Halt Codes (TST00-TST14) (Continued)

HALT CODE	SECTION	MESSAGES	COMMENTS
102054	09	E054 DMA2 CLF	DMA2 didn't generate a CLF during an output transfer
102055	09	E055 STF 6	STF 6 didn't terminate DMA1 transfers.
102056	09	E056 STF 7	STF 7 didn't terminate DMA2 transfers.
102057	10	E057 SC DECODE	A-Register contains instruction which erroneously executed a CLF 6.
102060	10	E060 SC DECODE	A-Register contains instruction which erroneously executed a CLF 7.
102061	11	E061 WCR1 EXP=XXXXXX ACT=XXXXXX	After disabling DMA1 after two output transfers, WCR1 was not as expected. A=expected WCR1 contents B=actual WCR1 contents.
102062	11	E062 WCR2 EXP=XXXXXX ACT=XXXXXX	After disabling DMA2 after two output transfer, WCR2 was not as expected: A=expected WCR2 contents B=actual WCR2 contents.
102063	12	E063 DMA1 OUT TRANSFER ADDR = XXXXXX EXPECTED DATA = XXXXXX ACTUAL DATA = XXXXXX	A DMA1 output transfer didn't transfer contents of proper address: A=transfer address B=actual data.
102064	12	E064 DMA2 OUT TRANSFER ADDR = XXXXXX EXPECTED DATA = XXXXXX ACTUAL DATA = XXXXXX	A DAM2 output transfer contents after proper address A=transfer address B=expected data.
102065	13	E065 DMA1 IN TRANSFER ADDR = XXXXXX EXPECTED DATA = XXXXXX ACTUAL DATA = XXXXXX	DMA1 input transfer failed to transfer data into proper address: A=transfer address B=actual data.

Table 4-2. Error Information Messages and Halt Codes (TST00-TST14) (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102066	13	E066 DMA2 IN TRANSFER ADDR = XXXXXX EXPECTED DATA = XXXXXX ACTUAL DATA = XXXXXX	DMA2 input transfer failed to transfer data into proper address: AA=transfer address B=expected data.
102067	10	E067 SC DECODE	A-Register contains instruction which erroneously executed an LIA 3.
102072	Configuration	None	Test interface didn't respond properly to a data output/input operation during configuration (check select code, test connector, jumpers, and interface card). Refer to paragraph 4-1.
102073	Configuration	None	I/O select code entered at configuration is invalid; must be greater than 7. Reenter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration is valid. Enter program option bits in Switch Register and press RUN.
102075	Test Control	None	Test selection request resulting from Switch Register bit 9 being set. Enter desired group of tests to be executed into A-register and press RUN. (See table 3-1.)
102076	Test	None	End-of-test halt resulting from Switch Register bit 15 being set (A-register equals test number).
102077	Test Control	PASS XXXXXX	Diagnostic run complete. Switch Register options may be changed (A-register has pass count). To continue, press RUN.

Table 4-2. Error Information Messages and Halt Codes (TST00-TST14) (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
103000	14	E100 DMA1 STC GENERATION	Illegal DMA1 STC occurred on last input transfer.
103001	14	E101 DMA2 STC GENERATION	Illegal DMA2 STC occurred on last input transfer.
103002	14	E102 DMA1 CLF	Illegal DMA1 CLF occurred on last input transfer.
103003	14	E103 DMA2 CLF	Illegal DMA2 CLF occurred on last input transfer.
103004	14	E104 DMA1 OVERRIDE	DMA1 didn't hold off a DMA2 cycle.
103005	6	E105 WCR2	DMA1 transfer illegally incremented or altered WCR2.
103006	6	E106 WCR1	DMA2 transfer illegally incremented or altered WCR1.
106077	Test Control	None	Halt stored in locations 2-77 to trap interrupts which may occur unexpectedly because of hardware malfunctions. M-register contains I/O slot number which interrupted. Diagnostic may be partially destroyed and have to be reloaded if it was caused by a CPU failure; the problem should be corrected before proceeding.
106070-107076	Configuration	None	Refer to HP 1000 M/E/F-Series Computer Systems Diag. Reference Manual.
107024	03	H324 PRESS PRESET AND RUN	Informs operator to press PRESET(s) and RUN.
103007-103113		See error table A-2.	

TEST 15—DUAL CHANNEL BLOCK TRANSFER TEST

APPENDIX

A

A-1. GENERAL

Test 15 is an appendix of the DMA/DCPC diagnostic. This test, which is not part of the standard DMA test run (TST00-TST14) will verify that DMA1 and DMA2 can run together stealing every machine cycle in a 2100A/S or 21MX M-Series computer. It is possible in some 21MX E-Series computers to get two DMA cycles followed by a CPU cycle. Therefore, the number of CPU cycles will be counted and compared with the number of words transferred under DMA. If the count of CPU cycles are greater than the words transferred, message E117 will be printed. This test will be useful for checking where DMA problems are in a system environment using DMA with Disc Drives, Magnetic Tape Units, etc.

Test 15 requires two 12930-60001 Universal Interface cards (must be furnished by user) with a special test cable built by the user. Figures A-1 and A-2 show how to fabricate the test cable. Each Universal Interface (UI) has a set of programmable switches which must be set according to table A-1.

A-2. OPERATION

Test 15 uses both DMA1 and DMA2 with two UI cards. One DMA channel is set up for an input operation and the other for an output operation. Since each UI card has only one data storage register, the sequence of first outputting then inputting must be made in that order. To accomplish this, the "Data Channel Device Command" output logic of one channel is connected to the input of the other UI card's "Data Channel Device Command" inputs logic circuitry, and vice versa. This holds each DMA channel in synchronization with each other allowing an output followed by an input until the block transfer has been completed.

The program sets up two buffers in the unused memory area, i.e., from FWAM to LWAM. Therefore, the buffer size depends upon the memory size of the computer used. The buffer size of the data to be transferred may then be calculated by the following:

$$B = \left\lfloor \frac{\text{LWAM} - \text{FWAM}}{2} \right\rfloor - 1$$

where

B = buffer size
LWAM = last word of available memory (contents of memory location 106_8),
FWAM = first word of available memory (contents of memory location 105_8), and
$\lfloor\ \rfloor$ = indicates the largest possible integer less than or equal to the specified part of the equation.

A memory map is provided. See figure A-4.

A software routine generates a pattern where the initial value of K (K = 135 octal) is added to the diagnostic pass count. This value is stored in the first location of buffer 2, then complemented, and stored into the second location of buffer 2. The original value that was stored in the first location of buffer 2 is then added to the value of K and stored in the third location of buffer 2 and so on. This operation is repeated until buffer 2 has been filled.

At this point, DMA1 and DMA2 are initialized and started. The DMA transfers the contents of buffer 2 into buffer 1. After DMA has completed, buffer 1 is compared with buffer 2. If any errors are detected, error message E107 and/or error halt 103007 will occur.

Error message—example

```
    E107 Dual CH DMA BLOCK TRANSFER FAILED
    EXP   = YYYYYY       ADDR = XXXXXX
    ACT   = ZZZZZZ       ADDR = XXXXXX
```

When an error message halt occurs, the B-register contains the actual value and A-register contains the expected value.

Many types of hardware failures (i.e., memory, I/O, bad UI cards, test cable, or DMA logic failures) could cause an error; it is up to the user to determine the error and correct any failures.

A two-word buffer is constructed between buffer 1 and buffer 2. This buffer is called BUFZ. It is initially set with a 125252_8 and 052525_8. This buffer is checked to see that DMA does not write past the specified word count. Note that if DMA writes past the word count more than two words, then buffer 2 will also be destroyed and data will not compare.

A-3. OPERATING INSTRUCTIONS

Test 15 is run and executed in the same manner as the standard tests with the exception that, to enter test 15, two select codes must be entered and Switch Register option bit 9 is omitted. Therefore, to run test 15:

a. Set P-register to 100_8.

b. Set S-register with select codes: SC1 in bits 0-5 and SC2 in bits 6-9.

c. Press PRESET (INT and EXT) and RUN.

d. If select codes are valid, then halt 102074 will occur. If either select code is invalid, an error halt 102073 will occur. If both select codes entered are equal, an error halt 102071 will occur. Enter correct select code and press RUN.

e. After halt 102074, then set S-register with Switch Register options from table 3-2 (with the exception of bit 9).

f. Press RUN.

g. Test 15 will run until an error is detected or the test has completed; at this time test 15 will return control to the Diagnostic Control portion of the diagnostic program and will then perform according to the S-register options specified.

h. If S-register bit 12 is set or RUN is pressed after halt 102077, another pass of test 15 will be executed. The pass count is printed at the end of each completed pass.

i. When another pass is started, the pass count is added to the value K (see paragraph A-2) and a new pattern is generated and stored in buffer 2.

j. Test 15 may be restarted by:
   (1) Starting at step a,
   (2) By pressing RUN, or
   (3) By setting P = 2000, setting S-register with desired options, and pressing RUN.

k. To end test 15 and run standard test(s), either clear S-register bit 12 and wait for halt 102077 or press HALT.
   (1) Set P-register to 100_8
   (2) Enter a single select code in the S-register.
   (3) Press RUN and follow the instruction outlined in Section III and figure 3-1.

NOTE

Standard run is entered by selecting one select code. Test 15 is entered by entering two select codes of the two UI cards. Refer to table 3-1.

A-4. TEST CABLE FABRICATION

An interconnecting cable kit, part no. 12930-60007, and a diagnostic test connector, part no. 12930-60006, is furnished with the Universal Interface. If the interconnecting cable kit has been used for another application, another cable kit plus an additional 100-pin connector (figure A-1) must be ordered. Fabricate the test cable as follows:

a. Insert approximately 10 inches (25 centimeters) of twisted-pair cable, part no. 8120-1895, into connector hood. (See figure A-1.)

b. Remove approximately 5 inches (13 centimeters) of outer jacket from cable end.

c. Separate twisted-pair wires into five groups of 10 pairs each.

d. Starting at connector end nearest pins 50A and 50B, connect the wires according to the wiring diagram shown in figure A-2 (record pin numbers versus wire color codes for future use):

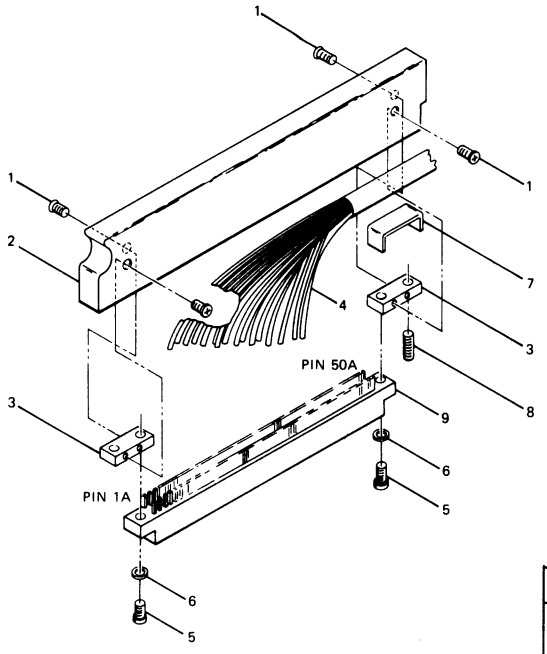
   (1) Solder the multicolored wires to their respective pins on A-side of connector; e.g., 49A, 41A, ... 1A. Insulate each pin with shrink tubing as shown in figure A-1.

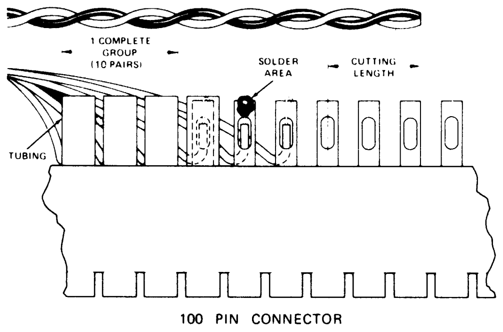
   (2) Solder the white wire of each twisted-pair to the respective pins on the B-side of connector; e.g., solder to pin 49B the white wire associated with multicolored wire soldered to pin 49A. Insulate each pin with shrink tubing.

e. Tape and bundle unused twisted-pair wires and save for spares.

f. For most applications, the cable length may be cut to approximately 13 feet (4 meters). This will allow one end of test cable to be plugged into the CPU mainframe and the other end of the test cable plugged into an I/O extender when mounted in a double rack-mount cabinet.

g. To connect the second connector to the opposite end of cable, follow steps a through e above.


1
1
1
2
4
7
3
8
PIN 50A
9
3
6
PIN 1A
5
6
5


1 COMPLETE GROUP (10 PAIRS)
SOLDER AREA
CUTTING LENGTH
TUBING
100 PIN CONNECTOR

ITEM	DESCRIPTION	PART NO.
1	Screw, flathead 4-40, 0.375	2200-0144
2	Hood	5020-7329
3	Mounting block connector	5020-7319
4	Cable, 50 twisted pair	8120-1895
5	Screw, external locking	2200-0111
6	Washer, flat	3050-0229
7	Cable clamp	5000-8038
8	Set screw; 4-40, 0.5	3030-0144
9	Connector, 100 pin	1251-2658

Figure A-1. Cable Fabrication Diagram and Parts List

24322

FROM P1 PIN	TO P2 PIN	FROM P1 PIN	TO P2 PIN	FUNCTION
1A	26A	26A	1A	IOB0
1B	26B	26B	1B	IOB0
2A	27A	27A	2A	IOB1
2B	27B	27B	2B	IOB1
3A	28A	28A	3A	IOB2
3B	28B	28B	3B	IOB2
4A	29A	29A	4A	IOB3
4B	29B	29B	4B	IOB3
5A	30A	30A	5A	IOB4
5B	30B	30B	5B	IOB4
6A	31A	31A	6A	IOB5
6B	31B	31B	6B	IOB5
7A	32A	32A	7A	IOB6
7B	32B	32B	7B	IOB6
8A	33A	33A	8A	IOB7
8B	33B	33B	8B	IOB7
9A	34A	34A	9A	IOB8
9B	34B	34B	9B	IOB8
10A	35A	35A	10A	IOB9
10B	35B	35B	10B	IOB9
11A	36A	36A	11A	IOB10
11B	36B	36B	11B	IOB10
12A	37A	37A	12A	IOB11
12B	37B	37B	12B	IOB11
13A	38A	38A	13A	IOB12
13B	38B	38B	13B	IOB12
14A	39A	39A	14A	IOB13
14B	39B	39B	14B	IOB13
15A	40A	40A	15A	IOB14
15B	40B	40B	15B	IOB14
16A	41A	41A	16A	IOB15
16B	41B	41B	16B	IOB15
24A	49A	49A	24A	DATA COMMAND/FLAG
24B	49B	49B	24B	DATA COMMAND/FLAG

Figure A-2. Test Cable Wiring Diagram

Table A-1. Universal Interface Programmable Switch Settings (TST15)

U85S1-2
S2-5
S3-10(0)

U87S1-1
S2-4
S3-8

U97S1-2
S2-5
S3-10(0)

U102S1-2
S2-7
S3-10(0)

U106S1-1
S2-5
S3-9

Note: The programmable switches are set using a screwdriver to position the contact mechanism. See figure A-3 for switch locations and switch positions.

The above switch settings are for test 15 with two UI cards and special test cable shown in figure A-2. When running standard test run (tests 0-14), use the switch settings given in table 1-1.

Table A-2. Error Information Messages and Halt Codes (TST15 Only)

HALT CODE	SECTION	MESSAGE	COMMENTS
103007	15	E107 DUAL CH DMA BLOCK TRANSFER FAILED EXP=XXXXXX ADDR=XXXXXX ACT=XXXXXX ADDR=XXXXXX	A failure was detected during the DMA transfer operation between the two UI cards and the two DMA channels. The expected and actual data and the addresses of the two buffers are printed. The A-register shows the expected data; the B-register shows the actual data.
103010	15	E110 DMA FLAG X SET BUT WCR = ORIGINAL WC VALUE	After a DMA transfer, the DMA Flag (6 or 7) was set and the WCR equaled the starting word count value. See note 1.
103011	15	E111 DMA FLAG X SET BUT WCR NOT ZERO.	After a DMA transfer, the DMA Flag (6 or 7) was set but the WCR was not zero. The value is somewhere between starting value and zero. The B-register contains the WCR actual value and the A-register contains the starting WC value. See note 2.

Table A-2. Error Information Messages and Halt Codes (TST15 Only) (Continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
103012	15	E112 DMA FLAG X NOT SET AND WCR = ORIGINAL WC VALUE	After a DMA transfer, the DMA Flag (6 or 7) was not set and the WCR equals the starting WC value. The A-register contains the starting WC value and B-register contains the actual WC value. See note 3.
103013	15	E113 DMA FLAG X NOT SET BUT WCR = ZERO	After a DMA transfer, the DMA Flag (6 or 7) was not set but the WCR equals zero. See note 4.
103014	15	E114 DMA FLAG X NOT SET AND WCR = XXXXXX	After a DMA transfer, the DMA Flag (6 or 7) was not set and the WCR was between the starting value and zero. The B-register contains the actual WCR value and the A-register contains the starting value. See note 5.
103015	15	E115 DMA WROTE 1 WORD PAST WC	DMA wrote past the word count value into buffer Z first location.
103016	15	E116 DMA WROTE 2 OR MORE WORDS PAST WC	DMA wrote past the word count value into buffer Z's first and second location. Note: Buffer 2 may have been written into and will produce error E107 if word count writes more than two words past WC value.
103017	15	E117 EXCESSIVE CPU	In a 2100/21MX-M the test allows only one CPU cycle during a DMA block transfer. In a 21MX-E, the test allows one CPU cycle for every two DMA cycles (or one CPU cycle for every word transferred from memory thru the two UI boards back into memory by DMA).

Notes

After a DMA transfer, the DMA flag should be set and the WCR should be zero.

Note 1. Possible failures for error E110 (103010):
- a. DMA Flag held in set state
- b. Bad SFS logic
- c. DMA not started:
  - (1) DMA/CPU logic failure
  - (2) Bad UI cards
  - (3) Bad test cable
  - (4) Priority denied

Note 2. Possible failures for error E111 (103011):
- a. DMA Flag held in set state
- b. Bad SFS logic
- c. Bad WCR status
- d. DMA not stealing every cycle

Note 3. Possible failures for error E112 (103012):
- a. DMA Flag held reset
- b. Bad SFS logic
- c. DMA not started:
  - (1) DMA/CPU logic failure
  - (2) Bad UI cards
  - (3) Bad test cable
  - (4) Priority denied

Note 4. Possible failures for error E113 (103013):
- a. DMA Flag held in reset state
- b. Bad SFS logic
- c. Bad WCR status
- d. DMA not started:
  - (1) Bad DMA/CPU logic
  - (2) Bad UI cards
  - (3) Bad test cable
  - (4) Priority denied

Note 5. Possible failures for error E114 (103014):
- a. DMA Flag held reset
- b. Bad SFS logic
- c. Bad WCR status
- d. DMA not stealing every cycle

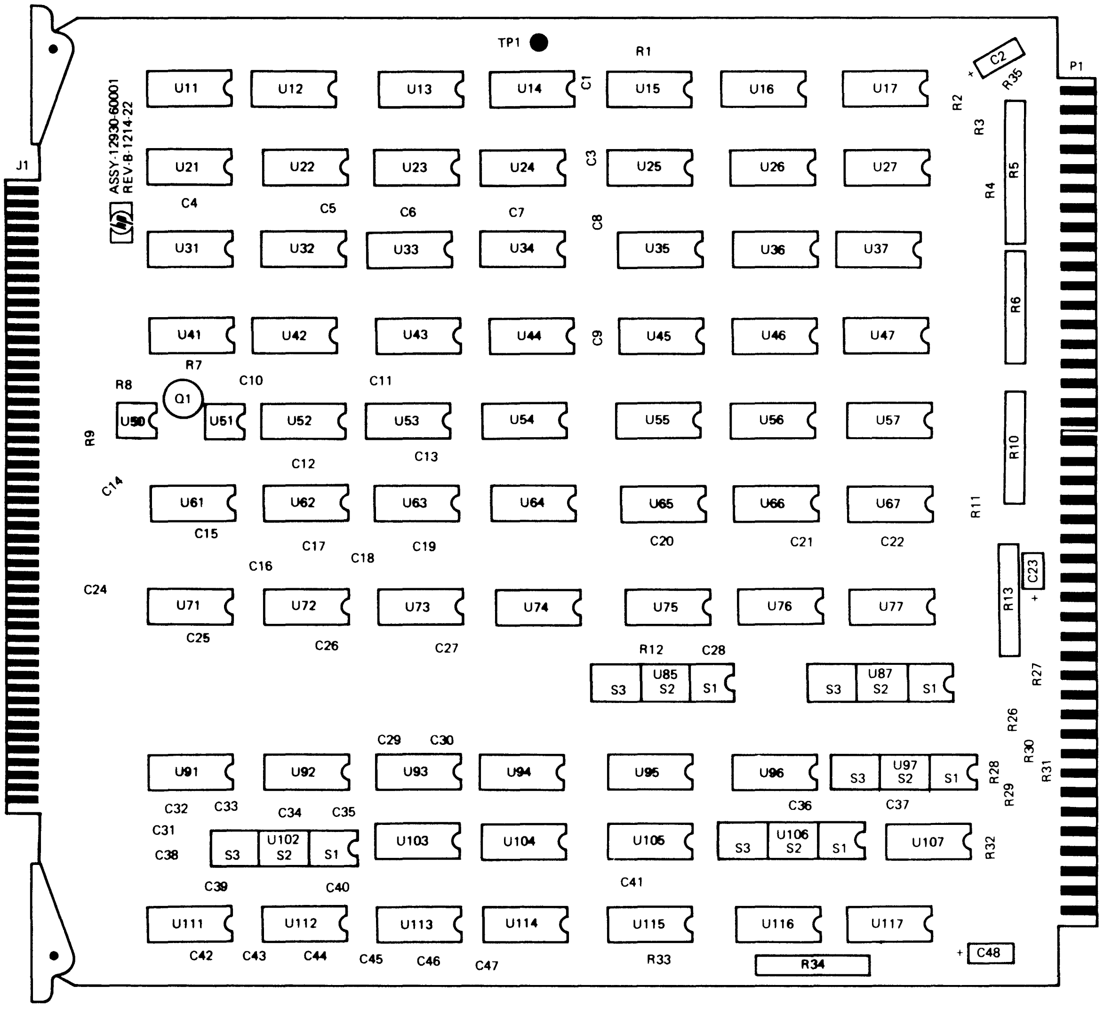
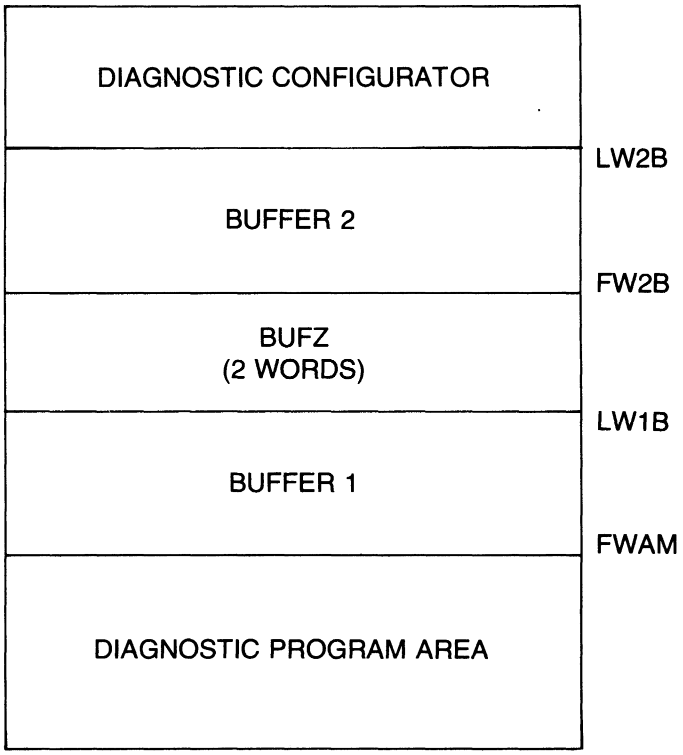

TP1
R1
C2
R35
P1
R2
R3
R4
R5
R6
R10
R11
R13
C23
R27
R26
R30
R31
R28
R29
R32
J1
ASSY-12930-60001
REV-B-1214-22
U11
U12
U13
U14
C1
U15
U16
U17
U21
U22
U23
U24
C3
U25
U26
U27
C4
C5
C6
C7
C8
U31
U32
U33
U34
U35
U36
U37
U41
U42
U43
U44
C9
U45
U46
U47
R7
R8
C10
C11
Q1
U50
U51
U52
U53
U54
U55
U56
U57
R9
C12
C13
C14
U61
U62
U63
U64
U65
U66
U67
C15
C17
C18
C19
C20
C21
C22
C16
C24
U71
U72
U73
U74
U75
U76
U77
C25
C26
C27
R12
C28
U85
S3
S2
S1
U87
S3
S2
S1
C29
C30
U91
U92
U93
U94
U95
U96
U97
S3
S2
S1
C32
C33
C34
C35
C36
C37
C31
C38
U102
S3
S2
S1
U103
U104
U105
U106
S3
S2
S1
U107
C39
C40
C41
U111
U112
U113
U114
U115
U116
U117
C42
C43
C44
C45
C46
C47
R33
R34
C48

Figure A-3. Universal Interface (12930-60001) Parts Location Diagram


DIAGNOSTIC CONFIGURATOR
LW2B
BUFFER 2
FW2B
BUFZ
(2 WORDS)
LW1B
BUFFER 1
FWAM
DIAGNOSTIC PROGRAM AREA

LW1B = FWAM + B
FW2B = LW1B + 2
LW2B = FW2B + B
LW2B < N6477 = LWAM

(N = 0 FOR 4K, N = 1 FOR 8K, N = 2 FOR 12K,
N = 3 FOR 16K, N = 5 FOR 24K, N = 7 FOR 32K)

Figure A-4. Memory Map

HEWLETT
PACKARD

MANUAL PART NO. 24322-90002
Printed in U.S.A. April 1982
E0482

HEWLETT-PACKARD COMPANY
Data Systems Division
11000 Wolfe Road
Cupertino, California 95014