

Z80 Preprocessor Interface Module

MODEL 64683A

TECHNICAL DATA 15 MAR 82

Description

Model 64683A Z80 Preprocessor Interface Module is a specialized plug-in probe module that is installed in Model 64650A General Purpose Preprocessor for convenient interface to Model 64620S Logic State/Software Analyzer. The module provides a simple hook-up to Z80 microprocessors via a low mechanical profile, 40-pin dual-in-line probe/chip carrier. Forty state analysis input channels are used to monitor processor bus activities, leaving 20 preprocessor input channels available for additional circuit probing. Interface software, ordered separately, provides inverse assembly of executed code and automatic formatting for analyzer measurements.

Features

Convenient, 40-pin low mechanical-profile carrier

Z80 instruction set disassembly

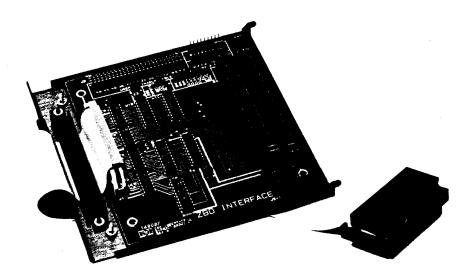
Programmable stimulus and halt lines for processor control

User-definable functions for input/output lines

Symbolic mapping of address and operand information

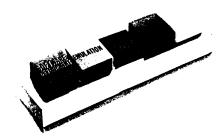
Z80 Instruction Set Disassembly

The interface software package (Model 64683ST on tape cartridge or Model 64683SF on flexible disc) translates the full Z80 instruction set for displays in mnemonic form. Trace displays may also incorporate user-defined symbols in the address field and instruction operand field for powerful symbolic tracing (figure 1). Additionally, the software sets the appropriate formats for each analyzer measurement. The software is automatically loaded from mass storage into the Model 64620S software analyzer whenever the interface is used.



Base: hex hex rel hex Map: ADDR MAP ADDR MAP OFTR 0 ED -004 MAIN+0047 OTIR 0 ED -002 MAIN+0048 B3 opcode fetch 4.00 usec B3 -001 10 DPORTI 1F i/o write 4.00 usec 1F -001 10 DPORTI 1F i/o write 4.00 usec 1F trigger MAIN+0049 CALL MEM_LOAD+0000 2.52 usec CD -001 MAIN+004A FB memory read 4.43 usec FB -002 MAIN+004B 00 memory write 4.00 usec 00 -003 STACK-0000 00 memory write 4.00 usec 00
-004 MAIN+0047 OTIR 0 ED -003 MAIN+0048 B3 opcode fetch 4.00 usec B3 -002 abs 008F 1F memory read 5.48 usec 1F -001 10-1007 1F 1/0 write 4.00 usec 1F trigger MAIN+0049 CALL MEM_LOAD+0000 2.52 usec CD -001 MAIN+0048 D0 memory read 4.49 usec FB -002 MAIN+004B 00 memory read 3.00 usec 00
-004 MAIN+0047 OTIR 0 ED -003 MAIN+0048 B3 opcode fetch 4.00 usec B3 -002 abs 008F 1F memory read 5.48 usec 1F -001 10_PORT1 1F 1/o write 4.00 usec 1F trigger MAIN+0049 CALL MBM_LOAD+0000 2.52 usec CD -001 MAIN+0048 D memory read 4.49 usec FB -002 MAIN+004B 00 memory read 3.00 usec 00
-002 abs 008F 1F memory read 5.48 usec 1F -001 10_PORT1 1F i/o write 4.00 usec 1F trigger MAIN+0049 CALL MBM_LOAD+0000 2.52 usec CD -001 MAIN+004A FB memory read 4.49 usec FB -002 MAIN+004B 00 memory read 3.00 usec 00
-001 IO_PORT1 1F i/o write 4.00 usec 1F trigger MAIN+0049 CALL MEM_LOAD+0000 2.52 usec CD -001 MAIN+004A FB memory read 4.43 usec FB -002 MAIN+004B 00 memory read 3.00 usec 00
-001 IO_PORT1 1F i/o write 4.00 usec 1F trigger MAIN+0049 CALL MEM_LOAD+0000 2.52 usec CD -001 MAIN+004A FB memory read 4.49 usec FB -002 MAIN+004B 00 memory read 3.00 usec 00
+001 MAIN+004A FB memory read 4.49 usec FB +002 MAIN+004B 00 memory read 3.00 usec 00
+001 MAIN+004A FB memory read 4.48 usec FB +002 MAIN+004B 00 memory read 3.00 usec 00
+003 STACK-0000 00 memory write 4.00 usec 00
+004 STACK-0001 4C memory write 3.00 usec 4C
+005 MEM_LOAD+0000 LD HL,[MEM_PTR+0000] 2.52 usec 2A
+006 MEM_LOAD+0001 80 memory read 4.48 usec 80
+007 MEM_LOAD+0002 FF memory read 3.00 usec FF
+008 MEM_PTR+0000 90 memory read 3.00 usec 90
+009 MEM_PTR+0001 01 memory read 3.00 usec 01
TATUS: Awaiting state command - userid TESTOR

Figure 1. Symbolic display of trace data provided by the Z80 processor inverse assembler.



Specifications

Processor compatibility: Zilog* Z80 and all microprocessors made by other manufacturers which comply with Zilog Z80 specifications and operate at clock speeds up to 6 MHz.

GENERAL

Maximum clock speed: 6 MHz
Signal line loading: one LS TTL load for all
monitored signal lines and approx 35 pF capacitance
Outputs: STIMULUS and HALT are LS TTL
open collector active-low outputs; max sinking
current, 6 mA.

Input: ACK, acknowledge for STIMULUS line active

low, TTL level.

Power consumption: 0.3 A at +5 Vdc max, supplied by Model 64620S Logic Software Analysis Subsystem.

ENVIRONMENTAL

Temperature: operating, 0° to +55° C (+32° to +131° F); nonoperating, -40° to +75° C (-40° to 167° F).

Altitude: operating, 4600 m (15 000 ft); nonoperating, 15 300 m (50 000 ft). **Humidity:** 90% noncondensing. Avoid sudden, extreme temperature changes which could cause

Ordering Information

condensation within the instrument.

Model 64683A Z80 Preprocessor Interface Module for installation in Model 64650A General Purpose Preprocessor Model 64683ST Z80 Software on tape cartridge Model 64683SF Z80 Software on floppy disc

NOTE: Model 64683A must be installed in Model 64650A General Purpose Preprocessor.

Model 64650A General Purpose Preprocessor

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