

HP64000 Logic Development System

Model 64155A Wide Address Memory Controller



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CW&A 2/81

SERVICE MANUAL

FOR

MODEL 64155A

WIDE ADDRESS MEMORY CONTROLLER

REPAIR NUMBERS

This manual applies directly to options with a repair number prefix of 2124A. For additional information about repair numbers, refer to options covered by this manual in Section I.

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COLORADO SPRINGS, COLORADO, U.S.A.

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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General Information

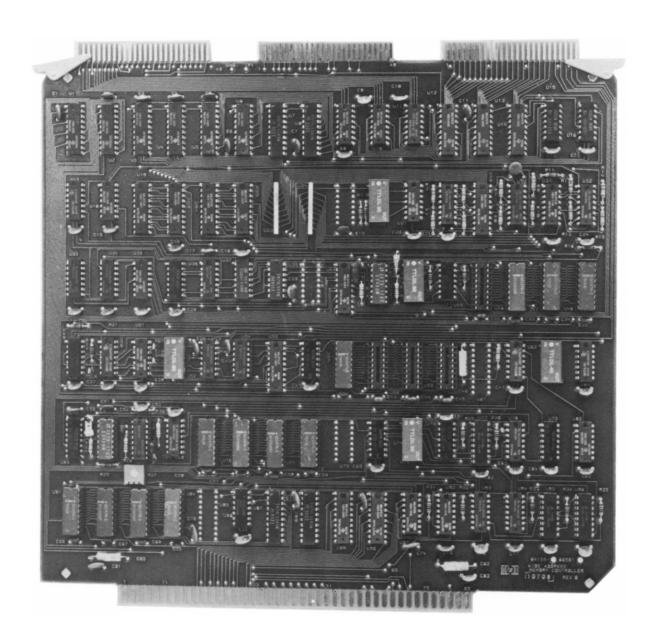


Figure 1-1. 64155A Wide Address Memory Controller Option

SECTION I

GENERAL INFORMATION

- 1-1. INTRODUCTION.
- 1-2. This manual contains installation, replaceable parts, performance verification and service information for the Model 64155A Wide Address Memory Controller Option used in the HP 64000 Logic Development System.
- 1-3. OPTIONS COVERED BY THIS MANUAL.
- 1-4. The Wide Address Memory Controller Option is assigned a repair number which can be found on the printed circuit board in the following form: 0000A0000. It is in two parts: the first four digits and the letter are the repair number prefix; the last four are the suffix. The prefix is the same for all identical units and will change only if the option is modified. The suffix, however, is assigned sequentially and is different for each unit manufactured. This manual applies to options with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.
- 1-5. An Option manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. An unlisted repair number prefix indicates that the option is different from those described in this manual. If this is the case, this manual should be accompanied by a Manual Changes supplement which explains how to adapt this manual for the newer option.
- 1-6. In addition to change information, the Manual Changes supplement contains information for correcting errors in this manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified by the manual print date and part number. Both may be found on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.
- 1-7. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.
- 1-8. DESCRIPTION.
- 1-9. The 64155A Wide Address Memory Controller Option consists of a single printed circuit board which plugs into the Motherboard of the 64100 Mainframe. The 64155A is shown in figure 1-1.
- 1-10. The Wide Address Memory Controller Option is the interface between Emulation Memory, the installed Emulator and the 64000 operating system. It will also signal the analysis equipment and halt emulation when a GUARDED memory access is attempted and, if optionally configured, when a write to ROM is attempted.

- 1-11. This option maps the users address into available Emulation Memory. In a 16 Bit emulation system, up to four Low Power Emulation Memory Boards (HP Model 64152B, 64153B or 64154B) can be installed.
- 1-12. The Emulation Memory Address is specified via the data outputs of Mapper RAMs which reside on the Memory Controller Option. The Mapper RAMs also specify what type of memory the given block of Emulation Memory is supposed to act like (RAM, ROM or GUARDED Memory), or whether a given address is to be regarded as user address space and not acted upon within the Emulation Memory system.

SECTION II

INSTALLATION AND REMOVAL

- 2-1. INTRODUCTION.
- 2-2. This section contains information for unpacking, initial inspection, installation and removal of the Model 64155A.
- 2-3. UNPACKING AND INSPECTION.
- 2-4. Unpack the option and keep the shipping carton and cushioning material until the contents have been checked for completeness and the option has been checked mechanically and electrically. The electrical performance verification is given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the option does not pass the performance verification, notify the nearest Hewlett-Packard Sales/Service Office. If the shipping carton is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office and keep the shipping materials for the carrier's inspection. The sales and service office will arrange for repair or replacement at HP option without waiting for the claim against the carrier to be settled.
- 2-5. INSTALLATION CONSIDERATIONS.
- 2-6. In a 16 Bit emulation system, up to four Low Power Emulation Memory Boards (HP Model 64152B, 64153B or 64154B) can be installed. Typically the Memory Boards are installed in Motherboard slots 2 thru 5 with slot 6 reserved for the Memory Controller. This recommended configuration is shown in figure 2-1. Notice that slot 9 is empty. This is to prevent accidental damage to Rear Panel Bus Cable which may occur if the board occupying slot 9 rubs against the cable as it is installed in or removed from the mainframe. If slot 9 is used, care should be taken when installing or removing the board to prevent damage to this cable.

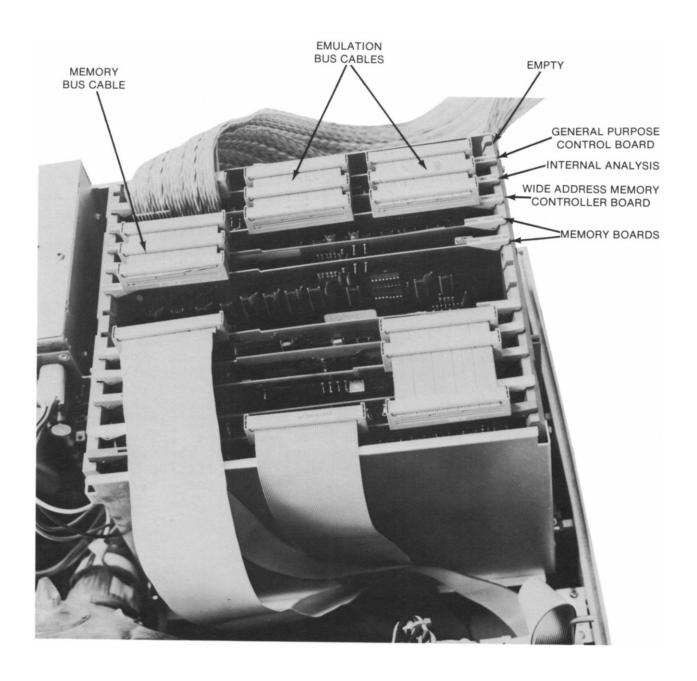


Figure 2-1. Recommended Motherboard Slot Configuration

- 2-7. SAFETY CONSIDERATIONS.
- 2-8. There are no high voltages on the 64155A Wide Address Memory Controller Board. There are, however, high voltages associated with the 64100 Mainframe and warnings are give where these voltages exist.
- 2-9. INSTALLATION PROCEDURE.
- 2-10. Use the following procedure to install Model 64155A.
 - a. Turn the mainframe power switch to the OFF position.

CAUTION

To avoid equipment damage in the following step make sure the component side of the Memory Controller is facing toward the front of the mainframe before the board is installed.

- b. Orient the component side of the Memory Controller toward the front of the mainframe, align the edge connector of the board with the Motherboard connector and then press down.
- c. Refer to figure 2-1 and connect the Memory and Emulation Bus Cables. These cables are keyed so that they can be installed in one direction only. Proper orientation can be verified by noting the orange dot on the left side of the cable connector when viewed from the front of the 64100 station.
- d. Refer to Section IV and run the performance verification.

2-11. REMOVAL PROCEDURE.

- a. Turn the mainframe power switch to the OFF position.
- b. Remove the Memory and Emulation Bus Cables.
- c. Pull up on the two extractor levers and remove the Memory Controller from the cardcage.

SECTION III

OPERATION

3-1. The functions of the 64155A Wide Address Memory Controller are transparent and require no interaction with the operator. Refer to the "16 Bit Emulator/Analysis Reference Manual" for an explanation of emulation and memory space partitioning.

SECTION IV

PERFORMANCE VERIFICATION

- 4-1. INTRODUCTION.
- 4-2. This section contains the performance verification procedures for isolating failures on the 64155A Wide Address Memory Controller and Memory Boards. The 64155A Wide Address Memory Controller is a blue stripe (exchange) item and not supported to component level repair.
- 4-3. Before attempting to isolate a suspected failure on the Wide Address Memory Controller Board, some preliminary steps should be performed to systematically isolate the problem. These are detailed in Section IV of the 64100 Mainframe Service Manual and summarized below:
 - a. Verify that the mainframe performance verification passes to insure that the problem is not in the mainframe.
 - b. Disconnect the target system to eliminate it as a possible source of the problem.
 - c. Reseat the Wide Address Memory Controller, Memory Boards and bus cables to insure good electrical connections.
- 4-4. PERFORMANCE VERIFICATION THEORY.
- 4-5. There are five individual performance verification tests that can be run. These include:

System -> Board Access Test

Memory Mapper Test

Memory Control Test

Memory Test

Emulation Access Test

4-6. The above tests can be run individually, or the tests can be cycled and repeated automatically. These tests and the procedures to run them are described in the following paragraphs.

4-7. To run the performance verification tests, it is first necessary to execute the option_test instruction. This instruction directs the 64100 to identify the option boards occupying its cardcage and then load the appropriate performance verification software. To do this, type in the following lower case instruction (figure 4-1):

option_test

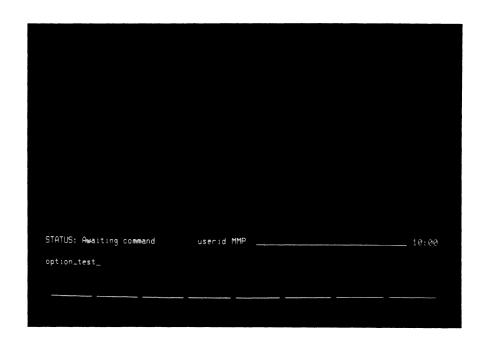


Figure 4-1. Selecting option_test

4-8. The CRT will now display a directory of the installed option boards with their corresponding slot locations. A typical example is shown in figure 4-2. Enter the slot number indicated for the Wide Address Memory Controller. For example, if the Wide Address Memory Controller is in slot 6, enter:

6 (RETURN)

| | HP 64000 Option Performance Verification | |
|---------------|---|-------|
| Card # | ID * Module | |
| | 1000H Prom Programmer 0201H Wide Address Memory Controller 0100H Analysis 00F1H General Purpose Controller - Z8002 Pod | |
| | | |
| | | |
| | | |
| | | |
| STATUS: 6_ | Awaiting test selection | 10: |
| | | |
| | <u>⟨SLOT ♦⟩</u> | print |

Figure 4-2. Slot Selection

4-9. The CRT will now show the overview display as shown in figure 4-3.



Figure 4-3. Overview Display

4-10. The Softkeys present in the overview display have the following functions:

end

Halts execution of the Wide Address Memory Controller Tests.

cycle

Continuously cycles through all of the tests noted in the overview display except for the Emulation Access Test which is skipped when cycling. Normally this would be the first key depressed to cycle through the tests and indicate any failures which can then be investigated more closely. However, a specific test can be specified without cycling at this level.

next_test

Moves the inverse video bar to the next test to be run.

select

Selects the test indicated by the inverse video bar for further investigation of failures. This key does not start the test but rather displays the failure information gathered from cycling at the overview level.

print

Provides a hard copy of the current display above the STATUS line provided a printer is connected to the 64100. This key will work only if there are no tests in progress. If the printer is busy, the STATUS line will indicate "Waiting for Printer."

- 4-11. It is advisable at this time to press the cycle Softkey, run through several test cycles, and note if there are any failures. The inverse video bar will move from test to test as they are performed. After several test cycles have been run, press the end Softkey to stop cycling. If any test fails, the individual test can be run for a closer examination of the failure. This is explained in the following paragraphs.
- 4-12. Individual Test Selection Descriptions.
- 4-13. An individual test may be selected by pressing the next test softkey until the inverse video bar indicates the test to be investigated. The following Softkeys are present in the individual test displays.

| : | SYSTEM -> BOARD ACCESS TEST SOFTKEYS |
|-------------------------------------|--|
| (end) (c | ycle (next_test) (start) (print) |
| N | 1EMORY MAPPER TEST SOFTKEYS |
| (end) (| cycle (next_test) (start) (print) |
| N | MEMORY CONTROL TEST SOFTKEYS |
| (end) (e | cycle (next_test) (start) (print) |
| N | MEMORY TEST SOFTKEYS |
| (end) (c | cycle (next_test) (start) (img test) (retn test) (print) |
| E | MULATION ACCESS TEST SOFTKEYS |
| (end) (| cycle) (next_test)(start) () (() (calib.) (print) |
| 4-14. The Softke following function | eys present in the individual displays have the ons: |
| (end | Returns to the overview level. |
| (cycle) | Cycles through all tests shown in the given test display. |
| (next_test) | Moves the inverse video bar to a specific test to be $\operatorname{run}_{\:\raisebox{1pt}{\text{\circle*{1.5}}}}$ |
| (start) | Causes the test indicated by the inverse video bar to be run continuously at a high repetition rate. The high repetition rate is useful as it will provide a stable display on an oscilloscope. Also, when cycling the Memory Mapper and Emulation Access Test, the results will alternate if they are different for the two modes. Running only one test will provide a stable cumulative result. |
| (print) | Provides a hard copy of the current display above the STATUS line provided a printer is connected. This key will work only if no tests are in progress. If the printer is busy, the STATUS line will show "Waiting for Printer." |
| (img test) | See Memory Test Description. |
| (retn test) | See Memory Test Description. |
| (calib. | See Emulation Access Test Description. |

4-15. System -> Board Access Test Description.

4-16. The System -> Board Access Test can be run without working memory. When run, Interrupt and Access Status tests are performed at a very basic level. Interrupt Status checks to see if HROM and HGRD (U65-7,9) can be set and cleared individually. The Access Status Test checks to see if the Access Status Bit will set and clear properly when the CPU is attempting to make a successful access. Figure 4-4 shows a System -> Board Access Test Display and table 4-1 explains how to interpret test failures.

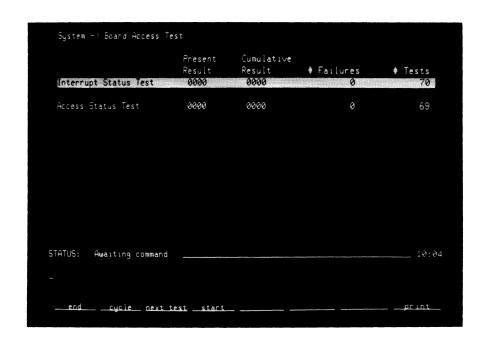


Figure 4-4. System -> Board Access Test Display

Table 4-1. System -> Board Access Test Results

| Test | Result | Interpretation |
|-------------|--------|--|
| Intr Status | 0001 | Can't set HROM |
| Intr Status | 0010 | Can't set HGRD |
| Intr Status | 0011 | Can't clear Status bits after setting them |
| Intr Status | 1100 | Can't clear the Interrupt Status Bits Initially |
| Acc Status | 0001 | Unable to set status bit to normally high |
| Acc Status | 0010 | Status bit did not go low to indicate lack of access |
| Acc Status | 0011 | Status bit did not go high to indicate successful access |

- 4-17. Memory Mapper Test Description.
- 4-18. The Memory Mapper Test performs five tests on the addresss and data buses in two configurations and requires at least one row of good memory at address 0000H to provide valid results for the 64155A. The first test checks the data bus in the word mode. If any opens or supply shorts are detected, it prevents execution of the other tests. Next, it indicates which lines are failing and sets a flag to note that the remainder of the tests were not performed. If there are supply shorts or opens, the data bus is next tested in the word mode for data lines shorted to each other. If this test fails, the remaining tests are aborted and a flag is set to note they were not performed. Any shorted lines are reported in both the word and byte results. If the data bus passes in the word mode, it is then tested in the byte mode to check for data lines shorted together and byte write strobes shorted together. In all cases, if the first three tests do not all pass, the STATUS line will display, for a short time, an error message noting that the software was unable to access memory location zero. If these three tests do pass, all remaining tests will be performed without aborts, regardless of their results.
- 4-19. The System Address Bus Test walks 1's and 0's across LAO LA10. This creates unique bit patterns which are read back to check the lines for being open or shorted together, or shorted to a power supply line.
- 4-20. The Mapper Image Test checks the Mapper RAM output for problems that would create images in memory. Since the amount of memory can be variable, this test checks to see how much memory is available and masks off failures which could not possibly exist due to the lack of memory present. This masking process is not impervious to failure. The fast access rates used by this board does not allow the charge stored on the data bus to bleed off and may allow erroneous results to appear in some instances. However, this is rare. Without a full complement of memory, there will rarely be any failures reported with walking 0's. The address lines checked by this test are All Al5. The System Address Register Test walks 1's and 0's across the upper address register to test for shorts and opens on the outputs of the register. If the Image Test indicates that All is failing, the register test will show "OFFF" on the results for both walking 1's and 0's. The Memory Mapper Test Display is shown in figure 4-5 and table 4-2 explains how to interpret test failures.

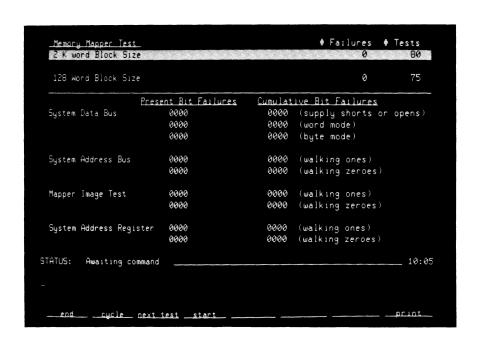


Figure 4-5. Memory Mapper Test Display

Table 4-2. Memory Mapper Test Results

| Test | Result | Interpretation |
|---------------------------------------|--------|---|
| Data Bus Test | xxxx | D15 - D0 in hex |
| Addr Bus Test 2k mode | _xxx | MA10 - MAO in hex (right justified) |
| Addr Bus Test 128 mode | xx | MA6 - MAO in hex (right justified) |
| Mppr Img Test 2k mode | _x x_ | MA15 - MA11 in hex (right justified in the x's) |
| Mppr Img Test 128 mode | _xxx | MA15 - MA7 in hex (right justified) |
| Addr Reg Test | _xxx | Address Register outputs MSB to LSB, left to right |
| All Tests Except Data Bus Tests | F000 | Test was not performed due to data bus failure |
| Data Bus Test Byte Mode | FF00 | If word mode showed no failures, this usually indicates that the memory write strobes are shorted together. |
| Addr Bus Test walking 1's | 1xxx | This means that address 0000H failed also |
| Addr Bus Test walking O's | 1xxx | This means that address OFFFH failed also |

- 4-21. Memory Control Test Description.
- 4-22. There are four tests associated with the Memory Control Test. The Block Size Select Option test checks the ability to select between a 2k word block size and a 128 word block size.
- 4-23. The Real-time Access Test checks to see, when real time is NOT selected and the emulator is halted, that the CPU can access Emulation Memory. Also, it checks to see, when real time is selected and the emulator is halted, that the CPU can NOT access Emulation Memory. In the latter, transitions are not occurring on HMAV when the emulator is not running. These transitions are necessary to initiate an access to memory in the real time mode. Effectively therefore, this test checks the ability to program CNTLA (U96-11) to a 1 or 0.
- 4-24. The Allow Writes to ROM Option Test checks to see that interrupts will not occur (even though enabled by the CPU) when HROM (U65-9) is set and writes to ROM are allowed. This indirectly checks to see if a Break will occur since both LIR1 (U86-8) and LBRK (U54-12) are controlled by the same signal. The successful completion of the Memory Controller Interrupt Option Test will validate this indirect test. If this indirect test fails, the results of the Allow Writes to ROM Test may not be valid. That is, if the output of U86-8 (LIR1) is bad, the Allow Writes to ROM Test will never fail.
- 4-25. The Memory Controller Interrupt Option Test checks to see that an interrupt is generated (when enabled) if either HROM or HGRD (U65-7,9) is set. It also checks to see that those interrupts are cleared. The Memory Control Test Display is shown in figure 4-6.



Figure 4-6. Memory Control Test Display

- 4-26. Memory Test Description.
- 4-27. The Memory Test checks the static RAM boards that the Memory Controller is connected to via the Memory Bus. Primarily, this test assumes a perfectly working Memory Controller Board and does not abort if there is a failure. However, if a known good Memory Board(s) is used, clues to problems on the Memory Controller Board can be obtained.
- 4-28. The Memory Test includes three types of tests. The first, and the only one activated by cycling, is the memory cell read/write test. This test writes and immediately reads back a random pattern in all cells in a selected row of memory. This is followed by reading back all of the block of memory to see if any cell was overwritten by an image. The data failure results are displayed in a cumulative form.
- 4-29. The next test is the Image Test and is activated by pressing the "img test" Softkey. This test was developed for use primarily in a production environment and checks for pins on the 6147 RAMs that do not make proper socket contact. However, it may be used for finding address line problems in blocks of memory above the first block, which is the only one tested in the Memory Mapper Test. The Memory Mapper Test does not test above the first block of addresses because only one row of RAM (corresponding to one memory block in this test) is required to be installed in the system. If a block of memory is chosen where no memory resides, the Image Test is rarely valid because of the data line charge problem discussed in paragraph 4-20.
- 4-30. The third test is the Retention Test and is activated by pressing the retn test Softkey. This test can only be aborted by a pressing the RESET key twice. This test takes about two minutes to run. When it is running, a countdown is displayed for both passes through memory. On the first pass, 0's are written to memory and read back approximately fifty seconds later. On the second pass, 1's are written to memory and read back approximately fifty seconds later. The test aborts upon finding a failure. Thus, depending on where the test stops, a 1 or 0 failure can be detected. The results of the Image and Retention Tests are displayed in the same area of the CRT, and they overwrite each other. If no failures are found, this will be noted on the STATUS line and the result area will be cleared. If there is a failure in any of the tests, the address it occurred at in a chosen block of memory is displayed in hex as well as the data bits that failed.
- 4-31. Neither the Image nor Retention Test will increment the test or fail counters because they are not a part of the normal test procedure. They are meant to be used for Image testing on a production checkout basis and as a last resort test for extremely rare occurrences of soft failures in static RAMs. The Memory Test Display is shown in figure 4-7.

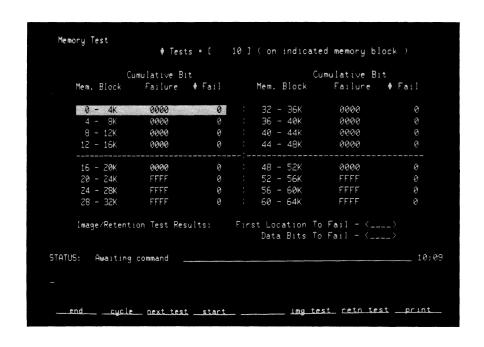


Figure 4-7. Memory Test Display

4-32. Emulation Access Test Description.

NOTE

Before running the Emulation Access Tests, disconnect the Emulation Bus Cables and leave only the Memory Bus Cable connected. In the Overview Display this test is skipped over when cycling. However, at this level, a continuous error message will be displayed if the start, cycle or calib Softkeys are pressed unless the Emulation Bus Cables are removed.

4-33. The Emulation Access Test performs six tests on the emulation access circuitry in two configurations and requires at least one row of good memory at address 0000H to provide valid results for the 64155A. The first test is on the data bus in the word mode. opens or supply shorts are found, the test aborts, preventing execution of any other tests. If the test aborts, the failures are displayed and a flag is set to note that the remainder of the tests were not performed. If there are no opens or supply shorts the data bus is next tested in the word mode for data lines shorted to each other. If this test does not pass, the lines that are shorted together are reported in both the word and byte mode results and a flag is set to note that the remaining tests were not performed. If the data bus passes in the word mode, it is then tested in the byte mode for data lines shorted together and byte write strobes shorted together. Unless all three tests pass, the STATUS line will display, for a short time, an error message indicating that the software was able to access location zero. If they do pass, the address tests will be performed regardless of their results.

4-34. The Emulation Address Bus Test first checks the unmapped bits by walking 1's and 0's across LEA1 - LEA11. This creates a set of unique bit patterns which are read back to check for address line problems. The mapped bits are then tested by walking 1's and 0's across LEA23-LEA12 to test for problems on the inputs of the Mapper RAMs.

NOTE

If there is a problem with MA11 (A16), it will cause erroneous results for the $\,$ Emulation Address Bus Test.

In the 128 word mode the 1's and 0's are walked across LEA1 - LEA7 and LEA19 - LEA8 respectively. If there are any failures in the mapped bits, the Timing and Status Tests are not run.

4-35. The Timing Test checks to see that writes to ROM and Guarded Memory cause the appropriate status bits to be set. It also checks to see that writes to User Memory do not cause a memory modification to occur or status bits to be set.

4-36. The calib Softkey is used to provide a stable scope display when setting the U66 one shot via the R27 potentiometer. This adjustment is critical (125 ns +-5 ns) and is explained in Section V. If the cables are attached, an error message will be displayed.

4-37. The Emulation Access Test Display is shown in figure 4-8. Table 4-3 explains how to interpret failures.

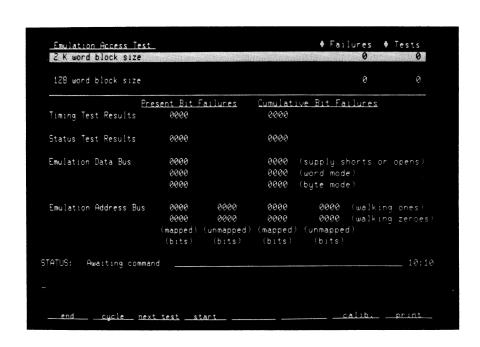


Figure 4-8. Emulation Access Test Display

Table 4-3. Emulation Access Test Results

| Test | Result | Interpretation |
|---------------------------------------|--------|---|
| Data Bus Test | xxxx | LED15 - LEDO in hex |
| Unmapped Bits 2k mode | _xxx | LEA7 - LEA1 in hex (right justified) |
| Unmapped Bits 128 mode | xx | LEA7 - LEA1 in hex (right justified) |
| Mapped Bits 2k mode | _xxx | LEA23 - LEA12 in hex (right justified) |
| Mapped Bits 128 mode | _xxx | LEA19 - LEA8 in hex (right justified) |
| All Tests Except Data Bus Tests | F000 | Test was not performed due to previous failure |
| Data Bus Test Byte Mode | FF00 | If word mode showed no failures, this usually indicates that the memory write strobes are shorted together |
| Unmapped Bits walking 1's | 1xxx | This means that address 000H failed also |
| Addr Bus Test walking O's | 1xxx | This means that address OFFFH failed also |
| Timing Test | 1100 | Means that the configuration using the leading edge of WDAV and a O ns setup time of address input to HMAV going low, didn't work. |
| Timing Test | 0001 | Means that the configuration using the leading edge of WDAV and a 64 ns setup time of address input to HMAV going low, didn't work. |

Table 4-3. Emulation Access Test Results (Cont'd)

| Test | Result | Interpretation |
|-------------|----------------------|---|
| Timing Test | 0010 | Means that the configuration using the trailing edge of WDAV and a 0 ns setup time of address input to HMAV going low, didn't work. |
| Status Test | 0001 | Write to ROM status bit did not set. |
| Status Test | 0010 | Write to GUARDED Memory status bit did not set. |
| Status Test | 0011 | Both status bits went high when only one should have. |
| Status Test | xFxx | Write to Emulation Memory was not prevented when a write to either USER, ROM or GUARDED Memory was performed. |
| Status Test | xExx | Read from Emulation Memory was not prevented when a read from USER Memory was performed. |
| Status Test | Fx01 Fx10 Fx11 | ROM Write to USER Memory GRD set the indicated BOTH status bits. |

Model 64155A Adjustments

SECTION V

ADJUSTMENTS

- 5-1. INTRODUCTION.
- 5-2. There is one adjustment on the 64155A Wide Address Memory Controller. This is the RDY STB adjustment which is used for the Emulation Access Test. RDY STB is adjusted at the factory and normally will not have to be changed. If it is changed, an oscilloscope should be used that is capable of measuring a pulse width of 125 ns (+ or -5 ns).
- 5-3. SAFETY CONSIDERATIONS.
- 5-4. There are no safety hazards associated with the 64155A Wide Address Memory Controller. There are, however, high voltages associated with the 64100 Mainframe. Appropriate warnings are given where a hazard may exist.
- 5-5. EQUIPMENT REQUIRED.
- 5-6. An oscilloscope capable of measuring a negative going pulse width of 125 ns (+-5 ns).
- 5-7. RDY STB ADJUSTMENT.
- 5-8. Use the following procedure to adjust RDY STB.
 - a. Turn the 64100 Mainframe power switch to the OFF position and remove all Bus Cables.
 - b. Place the 64155A Wide Address Memory Controller on an extender board.
 - c. Reconnect the Memory Bus Cable. Do NOT reconnect the Emulation Bus Cables.
 - d. Turn the 64100 Mainframe power switch to the ON position.
 - e. Refer back to the performance verification in Section IV and select the Emulation Access Test.
 - f. With the Emulation Access Test Display on the CRT, press the calib Softkey.
 - g. Refer to figure 5-1 and connect the oscilloscope probe to the RDY STB test point. A Convenient GND is located just below the RDY STB test point. This GND should be used for grounding the oscilloscope probe (the use of a spanner tip probe is recommended).

Adjustments Model 64155A

h. Adjust R27 (see figure 5-1) for a 125 ns negative going pulse width as shown in figure 5-2. This adjustment must be within + or -5 ns.

- i. Turn the 64100 Mainframe power switch to the OFF position and reinstall the 64155 Wide Address Memory Controller in the cardcage.
- j. Reconnect the Memory and Emulation Bus Cables.

Adjustments

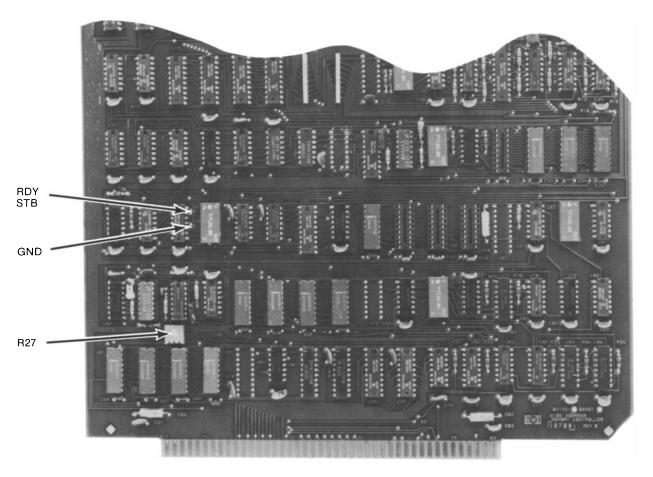


Figure 5-1. Emulation Access Timing Adjustment Test Points

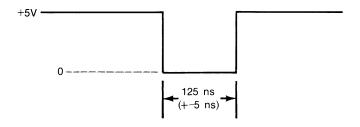


Figure 5-2. RDY STB Pulse Width

SECTION VI

REPLACEABLE PARTS

- 6-1. INTRODUCTION.
- 6-2. This section contains information concerning replaceable parts. Table 6-1 lists abbreviations used in the parts list and throughout this manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five digit numbers.
- 6-3. EXCHANGE ASSEMBLIES.
- 6-4. The Model 64155A is a part of the Hewlett-Packard Corporation's Blue Stripe Exchange program. New assemblies required for spare parts stock must be ordered by the new assembly part number listed in table 6-2. Factory repaired and tested assemblies are available on a trade in basis only by ordering the following rebuilt part number:

64155-69501

- 6-5. ABBREVIATIONS.
- 6-6. Table 6-1 lists abbreviations used in the parts list, on the schematics and throughout this manual. In some cases, two forms of the abbreviations are used: one all in capital letters and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, on the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.
- 6-7. REPLACEABLE PARTS.
- 6-8. Table 6-2 is the list of replaceable parts and is organized by components in alphanumerical order by reference designator.
- 6-9. The information for each part consists of the following:
 - a. The Hewlett-Packard part number and the check digit.
 - b. The total quantity (Qty) used on the PC board.
 - c. The description of the part.
 - d. A five digit code that indicates the manufacturer.
 - e. The manufacturer's part number.

- 6-10. The total quantity for each part is given at the first appearance of the part number on the list.
- 6-11. For ordering information, see Section VI of the 64100 $\,$ Mainframe Tab.

Table 6-1. Reference Designators and Abbreviations

| | | | HEFERENC | E DESIGNAT | OHS | | |
|-------|---|---------|-------------------------|------------|-----------------------------------|----------|--------------------------------------|
| A | = assembly | F | = fuse | MP | = mechanical part | U | = integrated circuit |
| В | = motor | FL | = filter | P | = pluq | v | = vacuum, tube, neon |
| BT | = battery | ic | = integrated circuit | Q. | = transistor | - | bulb, photocell, etc |
| C | = capacitor | J | = jack | R | = resistor | VR | = voltage regulator |
| CP | = coupler | K | = relay | RT | = thermistor | w | = cable |
| CR | = diode | L | = inductor | S | = switch | x | = socket |
| DL | | LS | | T | = transformer | Ŷ | = crystal |
| DS | = delay line | | = loud speaker | TB | = terminal board | ż | = tuned cavity networ |
| E E | = device signaling (lamp) | M MK | = meter | TP | | 2 | - tuned cavity networ |
| _ | = misc electronic part | WIK | = microphone | IP. | = test point | | |
| | | | ABBI | REVIATIONS | | | |
| A | = amperes | н | = henries | N/O | = normally open | RMO | = rack mount only |
| AFC | automatic frequency control | HDW | = hardware | NOM | = nominal | RMS | = root-mean square |
| AMPL | = amplifier | HEX | = hexagonal | NPO | = negative positive zero | RWV | = reverse working |
| | | HG | = mercury | | (zero temperature | | voltage |
| BFO | = beat frequency oscillator | HR | = hour(s) | | coefficient) | | |
| BE CU | = beryllium copper | HZ | = hertz | NPN | = negative-positive- | S-B | = slow-blow |
| вн | = binder head | | | | negative | SCR | = screw |
| BP | = bandpass | | | NRFR | = not recommended for | SE | = selenium |
| BRS | = brass | IF | = intermediate freq | | field replacement | SECT | = section(s) |
| BWO | = backward wave oscillator | IMPG | = impregnated | NSR | = not separately | SEMICON | = semiconductor |
| | | INCD | = incandescent | | replaceable | SI | = silicon |
| CCW | = counter-clockwise | INCL | = include(s) | | · | SIL | = silver |
| CER | = ceramic | INS | = insulation(ed) | OBD | = order by description | SL | = slide |
| СМО | = cabinet mount only | INT | = internal | ОН | = oval head | SPG | = spring |
| COEF | = coeficient | | | OX | = oxide | SPL | = special |
| СОМ | = common | K | = kilo=1000 | | | SST | = stainless steel |
| COMP | = composition | | | | | SR | = split ring |
| COMPL | = complete | LH | = left hand | Р | = peak | STL | = steel |
| CONN | = connector | LIN | = linear taper | PC | = printed circuit | | |
| CP | = cadmium plate | LK WASH | = lock washer | PF | = picofarads= 10-12 | TA | = tantalum |
| CRT | = cathode-ray tube | LOG | = logarithmic taper | | farads | TD | = time delay |
| CW | = clockwise | LPF | = low pass filter | PH BRZ | = phosphor bronze | TGL | = toggle |
| | | | To the passes that the | PHL | = phillips | THD | = thread |
| DEPC | = deposited carbon | м | = milli=10-3 | PIV | = peak inverse voltage | TI | = titanium |
| DR | = drive | MEG | = meg=106 | PNP | = positive-negative- | TOL | = tolerance |
| | | MET FLM | = metal film | | positive | TRIM | = trimmer |
| ELECT | = electrolytic | MET OX | = metallic oxide | P/O | = part of | TWT | = traveling wave tube |
| ENCAP | = encapsulated | MFR | = manufacturer | POLY | = polystyrene | | |
| EXT | = external | MHZ | = mega hertz | PORC | = porcelain | U | = micro=10-6 |
| | | MINAT | = miniature | POS | = position(s) | - | #:# := |
| F | = farads | MOM | = momentary | POT | = potentiometer | VAR | = variable |
| FH | = flat head | MOS | = metal oxide substrate | PP | = peak-to-peak | VDCW | = dc working volts |
| FIL H | = fillister head | MTG | = mounting | PT | = point | | J |
| FXD | = fixed | MY | = "mylar" | PWV | = peak working voltage | W/ | = with |
| G | = giga (109) | N | = nano (10–9) | RECT | = rectifier | W WIV | <pre>= watts = working inverse</pre> |
| GE | = germanium | N/C | = normally closed | RF | = radio frequency | **** | voltage |
| GL | = glass | NE | = neon | RH | = radio frequency = round head or | ww | = wirewound |
| GRD | = ground(ed) | NI PL | = nickel plate | **** | right hand | W/O | = without |
| 4110 | groundied | 141 F L | morei piate | | rigin nanu | **/ 5 | without |

Table 6-2. Replaceable Parts

| | | | lab | le 6-2. Replaceable Part | . S | |
|---------------------------------|---|------------------|-------------|--|---|---|
| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
| | 64155-66501 | 0 | 1 | WIDE ADDRESS MEMORY CONTROLLER BOARD | 28480 | 64155-66501 |
| C1 C2 C3 C4 C5 | 0160-3622 0160-3622 0160-3622 0160-3622 0160-3622 | 8 8 8 8 | 22 | CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER | 26654 26654 26654 26654 26654 | 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z |
| C6 | 0160-3622 | 8 | | CAPACITOR-FXD .1UF +80-20% 100VDC CER | 26654 | 2130Y5V100R104Z |
| C7 C8 C9 C10 C11 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 | 9 9 9 9 | 53 | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 |
| C12 C13 C14 C15 C16 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 | 9 9 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 |
| C17 C18 C19 C20 C21 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 | 9 9 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 |
| C22 C23 C24 C25 C26 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 | 9 9 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 |
| C27 C28 C29 C30 | 0160-2055 0160-2055 0160-2055 0140-0190 | 9 9 9 7 | 1 | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD 39PF +-5% 300VDC MICA | 28480 28480 28480 72136 | 0160-2055 0160-2055 0160-2055 DM15E390J0300WV1CR |
| 031 032 033 034 | 0180-0373 0160-3622 0160-3622 0160-3622 | 8 8 8 | 1 | CAPACITOR-FXD .68UF+-10% 35VDC TA CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER | 56289 26654 26654 26654 | 150D684X9035A2 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z |
| C35 C36 C37 C38 C39 | 0160-3622 0160-2055 0160-2055 0160-2055 0160-2055 | 8 9 9 9 | | CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 26654 28480 28480 28480 28480 | 2130Y5V100R104Z 0160-2055 0160-2055 0160-2055 0160-2055 |
| C40 C41 C42 C43 C44 | 0160-2055 0160-2055 0160-3622 0160-3622 0160-3622 | 9 9 8 8 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER | 28480 28480 26654 26654 26654 | 0160-2055 0160-2055 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z |
| C45 C46 C47 C48 C49 | 0160-3622 0180-0229 0160-2055 0160-2055 0160-2055 | 8 7 9 9 | 3 | CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD 33UF+-10% 100VDC TA CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 26654 56289 28480 28480 28480 | 2130Y5V100R104Z 150D336X9010B2 0160-2055 0160-2055 0160-2055 |
| C50 C51 C52 C53 C54 | 0160-2235 0160-2055 0160-4492 0160-2055 0140-0194 | 7 9 2 9 | 1 1 1 | CAPACITOR-FXD .75PF +25PF 500VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD 18PF +-5% 200VDC CER 0+-30 CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD 110PF +-5% 300VDC MICA | 28480 28480 51642 28480 72136 | 0160-2235 0160-2055 200-200-MP0-180J 0160-2055 DM15F111J0300WV1CR |
| C55 C56 C57 C58 C59 | 0160-2055 0160-3622 0160-3622 0160-3622 0160-3622 | 9 8 8 8 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER | 28480 26654 26654 26654 26654 | 0160-2055 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z |
| C60 C61 C62 C63 C64 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 | 9 9 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 0160-2055 0160-2055 |
| C65 C66 C67 C68 C69 | 0160-2055 0160-3622 0160-3622 0160-3622 0160-3622 | 9 8 8 8 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER CAPACITOR-FXD .1UF +80-20% 100VDC CER | 28480 26654 26654 26654 26654 | 0160-2055 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z 2130Y5V100R104Z |
| | | | | | | |

Table 6-2. Replaceable Parts (Cont'd)

| Potoronoo | HP Part | c | | -2. Replaceable Parts (C | Mfr | |
|---------------------------------|---|-----------------------|-------------|--|---|---|
| Reference Designation | Number | D | Qty | Description | Code | Mfr Part Number |
| C70 C71 | 0160-2055 0160-2055 | 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 | 0160-2055 0160-2055 |
| C72 C73 C74 | 0160-2055 0160-2055 0160-2055 | 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 |
| C75 C76 | 0160-2055 0160-2055 | 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 | 0160-2055 0160-2055 |
| C77 C78 C79 | 0160-2055 0160-2055 0160-2055 | 9 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 28480 28480 | 0160-2055 0160-2055 0160-2055 |
| C80 | 0180-0229 | 7 | | CAPACITOR-FXD 33UF+-10% 10VDC TA | 56289 | 150D336X9010B2 |
| C81 | 0160-2055 | 9 | | CAPACITOR-FXD .01UF +80-20% 100VDC CER | 28480 | 0160-2055 |
| C82 C83 | 0180-0229 0160-2055 | 7 | | CAPACITOR-FXD 33UF+-10% 10VDC TA CAPACITOR-FXD .01UF +80-20% 100VDC CFR | 56289 28480 | 150D336X9010B2 0160-2055 |
| R1 | 0757-0442 | 9 | 19 | RESISTOR 10K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1002-F |
| R2 R3 R4 R5 | 0757-0442 0698-3383 0698-3383 0698-3383 | 9 7 7 7 | 13 | RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 | 24546 24546 24546 24546 | C4-1/8-T0-1002-F NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F |
| R6 R7 R8 R9 | 0698-3383 0698-3383 0698-3383 0698-3383 | 7 7 7 7 | | RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 | 24546 24546 24546 24546 | NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F |
| R10 R11 | 0698-3383 0757-0442 | 7 9 | | RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 10K 1% .125W F TC=0+-100 | 24546 24546 | NC4-1/8-T2-56R0-F C4-1/8-T0-1002-F |
| R12 R13 R14 R15 | 0698-3383 0698-3383 0698-3383 0698-3383 | 7 7 7 7 | | RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 56 1% .125W F TC=0+-50 | 24546 24546 24546 24546 | NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F NC4-1/8-T2-56R0-F |
| R16 R17 R18 R19 R20 | 0757-0442 0757-0438 0757-0438 0757-0442 0757-0442 | 9 3 3 9 | 5 | RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 5.11K 1% .125W F TC=0+-100 RESISTOR 5.11K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 | 24546 24546 24546 24546 24546 | C4-1/8-T0-1002-F C4-1/8-T0-5111-F C4-1/8-T0-5111-F C4-1/8-T0-1002-F C4-1/8-T0-1002-F |
| R21 R22 R23 R24 R25 | 0757-0442 0757-0442 0698-3383 0757-0438 0757-0442 | 9 9 7 3 9 | | RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 56 1% .125W F TC=0+-50 RESISTOR 5.11K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 | 24546 24546 24546 24546 24546 | C4-1/8-T0-1002-F C4-1/8-T0-1002-F NC4-1/8-T2-56R0-F C4-1/8-T0-5111-F C4-1/8-T0-1002-F |
| R26 R27 R28 R29 R30 | 0757-0438 2100-3252 0757-0438 0757-0442 0757-0442 | 3 6 3 9 | 1 | RESISTOR 5.11K 1% .125W F TC=0+-100 RESISTOR-TRMR 5K 10% C TOP-ADJ 1-TRN RESISTOR 5.11K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 | 24546 28480 24546 24546 24546 | C4-1/8-T0-5111-F 2100-3252 C4-1/8-T0-5111-F C4-1/8-T0-1002-F C4-1/8-T0-1002-F |
| R31 R32 R33 R34 R35 | 0757-0442 0757-0442 0757-0442 0757-0442 0757-0442 | 9 9 9 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 24546 24546 24546 24546 24546 | C4-1/8-T0-1002-F C4-1/8-T0-1002-F C4-1/8-T0-1002-F C4-1/8-T0-1002-F C4-1/8-T0-1002-F |
| R36 R37 R38 | 0757-0442 0757-0442 0757-0442 | 9 9 9 | | RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 RESISTOR 10K 1% .125W F TC=0+-100 | 24546 24546 24546 | C4-1/8-T0-1002-F C4-1/8-T0-1002-F C4-1/8-T0-1002-F |
| U1 U2 U3 U4 U5 | 1820-1633 1820-1633 1820-2699 1820-2699 1820-2699 | 8 8 8 | 2 4 | IC BFR TTL S LINE DRVR OCTL IC BFR TTL S LINE DRVR OCTL IC-74F241 IC-74F241 IC-74F241 | 01295 01295 28480 28480 28480 | SN745240N SN745240N 1820-2699 1820-2699 1820-2699 |
| U6 U7 U8 U9 U1 0 | 1820-2699 1820-2075 1820-2075 1820-1428 1820-1428 | 8 4 4 9 | 4 2 | IC-74F241 IC MISC TTL LS IC MISC TTL LS IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 28480 01295 01295 01295 01295 | 1820-2699 SN74LS245N SN74LS245N SN74LS158N SN74LS158N |
| U11 U12 U13 U14 U15 | 1820-1439 1820-2024 1820-2024 1820-2024 1820-1158 | 2 3 3 2 | 1 8 | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE IC DRVR TTL LS LINE DRVR OCTL IC DRVR TTL LS LINE DRVR OCTL IC DRVR TTL LS LINE DRVR OCTL IC GATE TTL S AND-OR-INV DUAL 2-INP | 01295 01295 01295 01295 01295 | SN74LS258AN SN74LS244N SN74LS244N SN74LS244N SN74LS244N SN74S51N |
| U16 U17 U18 U19 U20 | 1820-1158 1820-2684 1820-2685 1820-1997 1820-2024 | 2 1 2 7 3 | 4 5 4 | IC GATE TTL S AND-OR-INV DUAL 2-INP IC-74F00 IC-74F02 IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN IC DRVR TTL LS LINE DRVR OCTL | 01295 28480 28480 01295 01295 | SN74S51N 1820-2684 1820-2685 SN74LS374N SN74LS244N |
| | | | | | | |

Table 6-2. Replaceable Parts (Cont'd)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|---|--|--------------------------------------|------------------|--|--|--|
| U21 U22 U23 U24 U25 | 1820-1997 1820-2024 1810-0280 1810-0280 | 7 3 8 8 | 2 | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN IC DRVR TTL LS LINE DRVR OCTL NETWORK-RES 10-SIP10.0K OHM X 9 NETWORK-RES 10-SIP10.0K OHM X 9 NOT ASSIGNED | 01295 01295 01121 01121 | SN74LS374N SN74LS244N 210A103 210A103 |
| U26 U27 U28 U29 U30 | 1810-0555 1820-2685 1820-2695 1820-1997 1820-2695 | 0 2 4 7 4 | 3 | DELAY LINE-50NS IC-74F02 IC-74F158 IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN IC-74F158 | 28480 28480 28480 01295 28480 | 1810-0555 1820-2685 1820-2695 5N74L5374N 1820-2695 |
| U31 U32 U33 U34 U35 | 1820-1195 1820-2695 1820-1275 1820-1275 1820-2685 | 7 4 4 4 2 | 3 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM IC-74F158 IC GATE TTL S NOR DUAL 5-INP IC GATE TTL S NOR DUAL 5-INP IC-74F02 | 01295 28480 01295 01295 28480 | SN74LS175N 1820-2695 SN74S260N SN74S260N 1820-2685 |
| U36 U37 U38 U39 U40 | 1820-2506 1820-2687 1820-1197 1820-1198 | 6 4 9 0 | 4 1 1 1 | IC INV TTL F HEX IC-74F10 IC GATE TTL LS NAND QUAD 2-INP IC GATE TTL LS NAND QUAD 2-INP NOT ASSIGNED | 07263 28480 01295 01295 | 74F04PC 1820-2687 SN74LS00N SN74LS03N |
| U41 U42 U43 U44 U45 U46 | 1820-2024 1820-1782 1810-0555 1820-2691 | 3 8 0 0 | 2 2 12 | IC DRVR TTL LS LINE DRVR OCTL IC MV TTL S MONOSTBL RETRIG/RESET DUAL DELAY LINE SONS IC-74F74 NOT LOADED IC NNOS 4096 (4K) RAM STAT 35-NS 3-S | 01295 34335 28480 28480 | SN74LS244N AM26S02PC 1810-0555 1820-2691 |
| U46 U47 U48 U49 U50 U51 | 1818-1586 1818-1586 1818-1586 1820-2691 1820-2684 1820-2685 | 5 5 0 1 2 | 12 | IC NMUS 4096 (4K) RAM STAT 35-NS 3-S IC NMUS 4096 (4K) RAM STAT 35-NS 3-S IC NMUS 4096 (4K) RAM STAT 35-NS 3-S IC-74F74 IC-74F00 IC-74F02 | 34649 34649 34649 28480 28480 28480 | D21 47H-1 D21 47H-1 D21 47H-1 1820-2691 1820-2684 1820-2685 |
| U52 U53 U54 U55 U56 | 1810-0556 1820-2686 1820-0684 1820-1997 1820-2506 | 1 3 7 7 6 | 1 3 1 | DELAY LINE-60NS IC-74F08 IC INV TTL S HEX 1-INP IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN IC INV TTL F HEX | 28480 28480 01295 01295 07263 | 1810-0556 1820-2686 SN74505N SN74L8374N 74F04PC |
| U57 U58 - U60 | 1818-1586 NOT LOADED | 5 | | IC NMOS 4096 (4K) RAM STAT 35-NS 3-S NOT ASSIGNED | 34649 | D2147H-1 |
| U61 U62 U63 U64 U65 U66 U67 U68 U69 | 1820-2684 1810-0554 1820-2684 1820-2693 1820-1782 1820-1423 1820-2690 1818-1586 | 1 9 1 2 8 4 9 5 | 1 1 1 1 | IC-74F00 DELAY LINE-40NS IC-74F00 IC-74F109 IC MV TTL S MONOSTBL RETRIG/RESET DUAL IC MV TTL LS MONOSTBL RETRIG DUAL IC MV TTL LS MONOSTBL RETRIG DUAL IC-74F32 IC NMOS 4096 (4K) RAM STAT 35-NS 3-S | 28480 28480 28480 28480 34335 01295 28480 34649 | 1820-2684 1810-0554 1820-2684 1820-2693 AM26S02PC SN74LS123N 1820-2690 D2147H-1 |
| U70 U71 U72 U73 U74 | 1818-1586 1818-1586 1818-1586 1820-2506 | 555 6 | | IC NMOS 4096 (4K) RAM STAT 35-NS 3-S IC NMOS 4096 (4K) RAM STAT 35-NS 3-S IC NMOS 4096 (4K) RAM STAT 35-NS 3-S NOT ASSIGNED IC INV TTL F HEX | 34649 34649 34649 07263 | D2147M-1 D2147H-1 D2147H-1 74F04PC |
| บ75 บ76 บ77 บ78 บ79 | 1810-0555 1820-1144 1820-0625 1820-2686 1820-2506 | 0 6 3 6 | 1 3 | DELAY LINE-50NS IC GATE TTL LS NOR QUAD 2-INP IC FF TTL S J-K NEG-EDGE-TRIG IC-74F08 IC INV TTL F HEX | 28480 01295 01295 28480 07263 | 1810-0555 SN74L802N SN74S11E 1820-2686 74F04PC |
| U80 U81 U82 U83 U84 | 1820-2685 1818-1586 1818-1586 1818-1586 1818-1586 | ឧភភភភភ | | IC-74F02 IC NMOS 4096 (4K) RAM STAT 35-NS 3-S IC NMOS 4096 (4K) RAM STAT 35-NS 3-S IC NMOS 4096 (4K) RAM STAT 35-NS 3-S IC NMOS 4096 (4K) RAM STAT 35-NS 3-S | 28480 34649 34649 34649 34649 | 1820-2685 D2147H-1 D2147H-1 D2147H-1 D2147H-1 |
| U85 U86 U87 U88 U89 | 1820-0682 1820-2075 1820-2075 1820-2024 | 5 4 4 3 | 1 | NOT ASSIGNED IC GATE TIL S NAND QUAD 2-INP IC MISC TIL LS IC MISC TIL LS IC DRVR TIL LS LINE DRVR OCTL | 01295 01295 01295 01295 01295 | SN74S03N SN74LS245N SN74LS245N SN74LS244N |
| บ90 บ91 บ92 บ93 บ94 | 1820-2024 1820-1216 1820-1216 1820-1275 1820-2686 | 3 3 4 3 | 2 | IC DRVR TTL LS LINE DRVR OCTL IC DCDR TTL LS 3-TO-8-LINE 3-INP IC DCDR TTL LS 3-TO-8-LINE 3-INP IC GATE TTL S NOR DUAL 5-INP IC-74F08 | 01295 01295 01295 01295 01295 28480 | SN74LS244N SN74LS138N SN74LS138N SN74S260N 1820-2686 |
| บ95 บ96 | 1820-0629 1820-0629 | 0 | | IC FF TTL S J-K NEG-EDGE-TRIG IC FF TTL S J-K NEG-EDGE-TRIG | 01295 01295 | SN74S112 SN74S112 |
| W1 W2 W3 | 65151-61602 64151-61603 64151-61604 64151-61605 | 9 | 1 1 1 1 | MEMORY BUS CABLE FOR J1 (2 CONN) MEMORY BUS CABLE FOR J1 (3 CONN) MEMORY BUS CABLE FOR J1 (4 CONN) MEMORY BUS CABLE FOR J1 (5 CONN) | 28480 28480 28480 28480 | 64151-61602 64151-61603 64151-61604 64151-61605 |
| U95 U96 W1 W2 | 1820-0629 1820-0629 65151-61602 64151-61603 64151-61604 | 0 0 8 9 | 1 1 | IC FF TTL S J-K NEG-EDGE-TRIG IC FF TTL S J-K NEG-EDGE-TRIG MEMORY BUS CABLE FOR J1 (2 CONN) MEMORY BUS CABLE FOR J1 (3 CONN) MEMORY BUS CABLE FOR J1 (4 CONN) | 01295 01295 28480 28480 28480 | SN74S112 SN74S112 64151-61602 64151-61603 64151-61604 |

Table 6-2. Replaceable Parts (Cont'd)

| Heference | D. | | т 1 | | -2. Replaceable Parts (C | · | · / |
|--|--------------------------|-------------------------------------|-------------|-----|--|-------------------------|-------------------------------------|
| XU46 | Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
| XU66 | XU46 XU47 XU48 | 1200-0539 1200-0539 1200-0539 | 7 7 | 12 | SOCKET-IC 18-CONT DIP DIP-SLDR SOCKET-IC 18-CONT DIP DIP-SLDR SOCKET-IC 18-CONT DIP DIP-SLDR | 28480 28480 28480 | 1200-0539 1200-0539 1200-0539 |
| XU72 | XU66 XU67 XU69 | 1200-0607 1200-0607 1200-0539 | 0 0 7 | | SOCKET-IC 16-CONT DIP DIP-SLDR SOCKET-IC 16-CONT DIP DIP-SLDR SOCKET-IC 18-CONT DIP DIP-SLDR | 28480 28480 28480 | 1200-0607 1200-0607 1200-0539 |
| | XU72 XU81 XU82 | 1200-0539 1200-0539 1200-0539 | | | SOCKET-IC 18-CONT DIP DIP-SLDR SOCKET-IC 18-CONT DIP DIP-SLDR SOCKET-IC 18-CONT DIP DIP-SLDR | 28480 28480 28480 | 1200-0539 1200-0539 1200-0539 |
| 64155-70901 5 1 SERVICE MANUAL 28480 64155-70901 | XU84 | | 1 | | | 1 | |
| | | | | | | | |

Table 6-3. Manufacturers' Codes

| Mfr No. | Manufacturer Name | Address | Zip Code |
|------------|------------------------------------|------------------|-------------|
| 01121 | ALLEN-BRADLEY CO | MILWAUKEE. WI | 53204 |
| 01295 | TEXAS INSTR INC SEMICOND CMPNT DIV | DALLAS TX | 75222 |
| 07263 | FAIRCHILD SEMICONDUCTOR DIV | MOUNTAIN VIEW CA | 94042 |
| 24546 | CORNING GLASS WORKS (BRADFORD) | BRADFORD PA | 16701 |
| 26654 | VARADYNE INC | SANTA MONICA CA | 90404 |
| 28480 | HEWLETT-PACKARD CO CORPORATE HQ | PALO ALTO CA | 94304 |
| 34335 | ADVANCED MICRO DEVICES INC | SUNNY VALLE CA | 94086 |
| 34649 | INTEL CORP | MOUNTAIN VIEW CA | 95051 |
| 51642 | CENTRE ENGINEERING INC | STATE COLLEGE PA | 16801 |
| 56289 | SPRAGUE ELECTRIC CO | NORTH ADAMS MA | 01247 |
| 72136 | ELECTRO MOTIVE CORP SUB IEC | WILLIMANTIC CT | 06226 |

See introduction to this section for ordering information

SECTION VII

MANUAL CHANGES

7-1. This section normally contains information for backdating this manual for models with a repair number prefix prior to the one shown on the title page. Because this edition includes the information for the first repair number prefix assigned, no backdating is required.

SECTION VIII

SERVICE

- 8-1. INTRODUCTION.
- 8-2. This section contains block diagrams, schematics and theory of operation for the 64155A Wide Address Memory Controller.
- 8-3. Emulation System Block Diagram Description.
- 8-4. Figure 8-1 is a basic block diagram of an emulation system and shows the placement of the 64155A Wide Address Memory Controller in the system.
- 8-5. The 64155A Wide Address Memory Controller is the interface between Emulation Memory, the installed Emulator, and the 64000 operating system. This option also maps the users address received via the Emulation Bus into available Emulation Memory. The mapping process is performed by Mapper RAMs which reside on the Memory Controller. In a 16 bit emulation system, up to four Low Power Emulation Memory Boards (HP Model 64152B, 64153B or 64154B) can be installed. A read/write operation to Emulation Memory is performed via the Memory Bus.
- 8-6. The Mapper RAMs also output signals which specify what type of memory the given block of Emulation Memory is supposed to act like (RAM, ROM or GUARDED Memory), or whether a given address is to be regarded as user address space and not acted upon. The Memory Controller will also signal the analysis equipment and halt emulation when a GUARDED memory access is attempted and, if optionally configured, when a write to ROM is attempted.

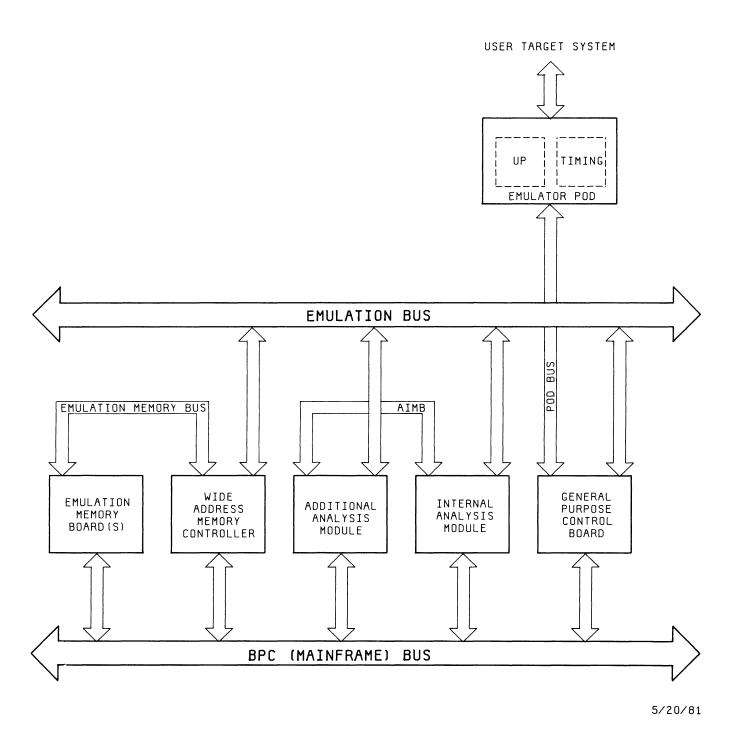


Figure 8-1. Emulation System Block Diagram

8-7. 64155A Wide Address Memory Controller Block Diagram.

8-8. A detailed block diagram of the 64155A Wide Address Memory Controller is shown six times in this section. Each time it is repeated, the shaded area will represent the circuitry for an associated schematic. A circuit description, which includes this block diagram level, is given after the mnemonic table.

8-9. Signal Mnemonics.

8-10. Table 8-1 lists the signal mnemonics used on the schematics and in the theory of operation in this section:

Table 8-1. Signal Mnemonics

| Mnemonic | Meaning | 0rigin |
|----------|--|--------------------------|
| 25 MHz | 25 MHz system clock. | CPU Bus, Schematic 1. |
| B25 MHz | Buffered 25 MHz. Buffered version of the 25 MHz system clock. | U79-12, Schematic 1. |
| CNTLA | Control "A". Control signal that determines whether or not the CPU waits for the emulator to finish a memory access before it begins its own access. | U55-19, Schematic 5. |
| CNTLB | Control "B". Control signal that determines whether or not emulation address must be set up for 64 ns before the falling edge of HMAV. | U55-16, Schematic 5. |
| CNTLC | Control "C". Control signal that determines which edge of LWDV is used to strobe write data into Emulation Memory. | U55-15, Schematic 5. |
| CNTLW | Control Write. Signal that clocks the control bits into the control register. | U91-13, Schematic 4. |
| CPUWSTB | CPU Write Strobe. Initiates a write for the CPU. | U62-11, Schematic 2. |
| DRVEM | Drive Emulator Bus. When low this signal enables the data bus buffers to drive the emulation bus for a read operation from Emulation Memory. | U50-11, Schematic 3. |
| | | |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|----------|--|--------------------------------|
| EMWSTB | Emulation Write Strobe. Write strobe for the write strobe generation circuitry. Generated by the emulation access circuitry. | U18-4, Schematic 2. |
| HBSTM | High Buffered Start Memory. Inverted, buffered version of LSTM. Gated via U62B to enable the U42B one shot to start a CPU memory access timeout. | U74-4, Schematic 4. |
| HCOMPL | High Complete Access. Status bit which is high if the CPU assess to Emulation Memory just performed was completed successfully. | U44-9, Schematic 1. |
| HDISCONB | High Disconnected Cable B. High if cable "B" is disconnected. This is the center Emulation Bus Cable. | Emulation Bus, Schematic 5. |
| HDISCONC | High Disconnected Cable "C". High if cable "C" is disconnected. This is the Emulation Bus cable located on the upper right side of the board, as viewed from the front of the mainframe. | Emulation Bus, Schematic 5. |
| HGRD | High Guarded. Status bit which is high if an access to guarded memory was made. | U65-7, Schematic 3. |
| HMAV | High Memory Available. When high, the emulator is not presently making an access to Emulation Memory. | Emulation Bus, Schematic 3. |
| HREAD | High Read. High when a read from Emulation Memory is being performed. This signal enables the Data Bus Drivers on the Memory Board. | U17-11, Schematic 2. |
| HREADY | High Ready. When this signal goes high an Emulator Memory access has been completed. | U68-11, Schematic 3. |
| HR OM | High ROM. Status bit which is high to note an access to ROM was made. | U65-9, Schematic 3. |
| HWDV | High Write Data Valid. The inverted version of LWDV which is gated to generate the Emulation Write Strobe (EMWSTB). | U56-12, Schematic 3. |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|------------|---|---------------------------|
| LA0-LA10 | Low Address 0-10. 64000 System address lines, active low. | CPU Bus, Schematic 4. |
| LA12, LA13 | Low Address 12, 13. 64000 System address lines, active low. | CPU Bus, Schematic 4. |
| LBA0-LBA10 | Low Buffered Address 0-10. Buffered system address lines. | U89, U90, Schematic 4. |
| LBBPOP | Low Buffered Buffered Power On Preset. LPOP which has been buffered twice for fan out reasons. | U94-8, Schematic 2. |
| LBBYTE | Low Buffered Byte. Buffered version of LBYTE. | U89-12, Schematic 2. |
| LBPOP | Low Buffered Power On Preset. LPOP which has been buffered once. | U94-6, Schematic 2. |
| LBRK | Low Break. Pulls emulation break line which sends the Emulator into the Monitor Mode. | U54-12, Schematic 3. |
| LBSEL | Low Buffered Select. Buffered version of LSEL. | U89-9, Schematic 4. |
| LBSTB | Low Buffered Strobe. Buffered version of LSTB. | U89-7, Schematic 4. |
| LBSTM | Low Buffered Start Memory. Buffered version of LSTM. | U89-5, Schematic 4. |
| LBUPB | Low Buffered Upper Byte. Buffered version of LUPB. | U37-6, Schematic 2. |
| LBWRT | Low Buffered Write. Buffered version of LWRT. | U94-3, Schematic 4. |
| LBYTE | Low Byte. When low, indicates that a memory cycle is to involve an eight bit byte, rather than the full sixteen bits of the word. | CPU Bus, Schematic 2. |
| LCLSTA | Low Clear Status. Clears the HROM and HGRD status bits. | U78-6, Schematic 5. |
| | | |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|--------------------|--|----------------------------|
| LD0-LD15 | Low Data 0 - 15. A 16 bit bi-directional bus used to transfer data to and from the CPU. When LSTB is low, data is present on the bus. | CPU Bus, Schematic 4. |
| LDISCON | Low Disconnected Cables. Signal which is low if both Emulation cables are disconnected. | U38-11, Schematic 5. |
| LEA1-LEA23 | Low Emulation Address 1 - 23. Emulation address bus signals. | U12 - U14, Schematic 5. |
| LEBUP | Low Emulation Byte Upper. Same as LUPB except it comes from the Emulator instead of the CPU. | U41-12, Schematic 3. |
| LEBYT | Low Emulation Byte. Same as LBYTE except comes from Emulator instead of the CPU. | U41-9, Schematic 3. |
| LEDO-LED15 | Low Emulation Data O - 15. Emulation Data Bus lines. | U3 - U6, Schematic 7. |
| LGRD | Low Guard. Signal which goes low if the current Emulation Memory Access is mapped as Guarded Memory. | U2-14, Schematic 7. |
| LIDEN | Low Identification Enable. When low, enables all PC Boards in slots O thru 9 (option slots) to generate card-type ID codes after interrogation by the slot select command. | CPU Bus, Schematic 5. |
| LIDENG | Low Identify Enable Gated. This signal is used with LIDEN to enable the board ID code. This signal is generated by U92 via LBSTB and LBSEL. | U92-7, Schematic 4. |
| LIR1 | Low Interrupt Request 1. Requests a system interrupt. | U86-8, Schematic 3. |
| LLA11 - LLA22 | Low Latched Address 11 - 22. Outputs of the upper address register. | U29, U31, Schematic 5. |
| LLA19I - LLA22I | Low Latched Address 19 - 22 Inverted. The inverted version of the upper four bits of the upper address register. | U31, Schematic 5. |
| | | |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|------------------|--|--|
| LMAP1 - LMAP3 | Low Address Map 1 - 3. Extends address selection capability to 64k locations on each option card. Active low. | CPU Bus, Schematics 1, 2 and 4. |
| LMAP1G | Low Map 1 Gated. A version of LMAP1 which is used to enable the U19 and U21 readback latches. | U92-9, Schematic 4. |
| LMAP2G | Low Map 2 Gated. A version of LMAP2 which is used to enable U91. | U92-10, Schematic 4. |
| LMAP3G | Low Map 3 Gated. A version of LMAP3 which is gated with LBWRT to initiate the Mapper RAM write signal (LMPRWE). | U92-12, Schematic 4. |
| LMAV | Low Memory Available. Inverted version of HMAV which clocks U96. | U56-10, Schematic 3. |
| LMBRKS | Low Memory Break Status. This signal, when low, means that the memory controller pulled LBRK low and not the Analysis unit. | U56-2, Schematic 3. |
| LMD0-LMD15 | Low Memory Data O - 15. Emulation Memory Data Bus. | Memory Bus/ U20, U22, Schematic 7. |
| LMPRWE | Low Mapper Write Enable. This is the write Strobe for the Mapper RAMs. | U62-3, Schematic 4. |
| LMSKINT | Low Mask Interrupts. When low this signal prevents the CPU from being interrupted when the memory controller pulls LBRK. | U55-9, Schematic 5. |
| LMSYN | Low Memory Sync. A signal from addressed devices. When low, forces the CPU to wait until the addressed devices can complete the read or write operation. | U54-4, Schematic 1. |
| LPOP | Low Power on Pulse. When low, initializes and prevents the CPU from running. When LPOP is released, the CPU begins operation at address 20 Hex. | CPU Bus, Schematic 2. |
| | | |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|----------|---|--------------------------|
| LPVEN | Low Performance Verification Enable. When this control bit is low the PV buffers and transceivers are enabled if the Emulation Bus cables have been removed. | U55-5, Schematic 5. |
| LPVENG | Low Performance Verification Enable Gated. This signal is generated by gating LPVEN and LDISCON. If PV is enabled and the Emulation Bus cables are disconnected, the PV buffers will be enabled. | U32-8, Schematic 5. |
| LPVRD | Low PV Read. This signal goes low when a PV read is being performed. | U91-10, Schematic 4. |
| LPVWRT | Low PV Write. This signal goes low when a PV write is being performed. | U91-11, Schematic 4. |
| LRDINT | Lcw Read Interrupt. This signal enables the interrupt status bits for a BPC read operation. | U91-12, Schematic 4. |
| LRDSTA | Low Read Status. This signal enables the HCOMPL and LDISCON status bits for a BPC read operation. | U91-14, Schematic 4. |
| LROM | Low ROM. This signal goes low when the current emulation access is from memory which is mapped as ROM. | U2-18, Schematic 7. |
| LROMEN | Low ROM Enable. When this control bit is low it allows a write to ROM to cause LBRK to be pulled. | U55-6, Schematic 5. |
| LSEL | Low Select. Slot select signal for the card cage. | CPU Bus, Schematic 4. |
| LSTB | Low Strobe. When low, and in the write mode, indicates the data bus has valid information on it. When low, and in the read mode, indicates the CPU is not driving the bus, and the device addressed can now drive it. | CPU Bus, Schematic 4. |
| | | |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|------------|---|---|
| LSTM | Low Start Memory. Used to initiate a memory cycle. When low, indicates the the information on the Address Bus is valid. | CPU Bus, Schematic 4. |
| LUPB | Low Upper Byte. When low, indicates the upper byte is being written or read and is used only when LBYTE is low. | CPU Bus, Schematic 4. |
| LUSER | Low User. When low this signal means that the current access being made by the emulator is from user memory. | U2-16, Schematic 7. |
| LUSERL | Low User Latched. Latched version of LUSER. | U49-5, Schematic 3. |
| LWADRUP | Low Write Address Upper. Write strobe for the upper address register. | U91-15, Schematic 4. |
| LWDV | Low Write Data Valid. A signal which is inverted and gated to generate the Emulator Write Strobe (EMWSTB). | U41-14, Schematic 3. |
| LWRL | Low Write Lower. Write strobe for the lower 8 bits of Emulation Memory. | U18-13, Schematic 3. |
| LWRT | Low Write. Read/Write status line for the CPU. | CPU Bus, Schematic 4. |
| LWRU | Low Write Upper. Write strobe for the upper 8 bits of Emulation Memory. | U18-1, Schematic 2. |
| MA0-MA19 | Memory Address O - 19. Emulation Memory Address Bus. | U9 - U11 on Schematic 5 and U1, U2 on Schematic 7. |
| MD00-MD07 | Mapper Data Out O - 7. | U81 - U84 and U69 - U72, Schematic 6. |
| MD08-MD015 | Mapper Data Out 8 - 15. | U57 - U60 and U45 - U48, Schematic 6. |
| MPX | Multiplex. When high this signal turns the address multiplexer to point toward the CPU instead of the Emulator. | U74-10, Schematic 2. |

Table 8-1. Signal Mnemonics (Cont'd)

| Mnemonic | Meaning | Origin |
|------------|---|--------------------------------|
| MPX | MPX Inverted. Inverted version of MPX used on the multiplexer which requires a low to turn toward the CPU. | U93-6, Schematic 2. |
| MRAO-MRA11 | Mapper RAM Address O - 11. Address inputs to the Mapper RAMs. | U28, U30, U32, Schematic 5. |
| RCVEM | Receive Emulation Bus. When high this signal enables the Emulation Data Bus Transceivers so that data can be input from the Emulator during an emulation write operation. | U18-10, Schematic 3. |
| S | Select. This control bit selects the block size. When low the block size is 128 words, when high the block size is 2k words. | U55-12, Schematic 3. |
| <u>s</u> | Select Inverted. Inverted version of select. | U56-6, Schematic 5. |
| SSMA | Sync Start Memory Access. | U64-11, Schematic 1. |
| STHGRD | Set HGRD. This signal goes low to set the HGRD status bit for Performance Verification. | U91-9, Schematic 4. |
| STHROM | Set HROM. This signal goes low to set the HROM status bit for Performance Verification. | U91-7, Schematic 4. |

- 8-11. THEORY OF OPERATION.
- 8-12. Mapper RAMs.
- 8-13. The Mapper RAMs map the users address into available Emulation Memory. That is, a given address input is received from the Emulation Bus and is loaded into the RAMs. The data outputs of the RAMs then serve as the address for Emulation Memory. Three of the RAMs (U46, U47 and U48) are not used for generating a memory address. These three RAMs identify what type of memory the given block of Emulation Memory is supposed to act like. It can act like RAM, ROM or GUARDED memory, or a given address can be regarded as user address space and not acted upon. The resistors in series on the Mapper RAM address lines reduce ringing which might occur because of the high input impedance of the RAMs.
- 8-14. Data Buses.
- 8-15. There are essentially three data buses on this board:

CPU Data Bus (LDO-LD15)
Emulation Data Bus (LEDO-LED15)
Memory Data Bus (LMDO-LMD15)

- 8-16. The CPU Data Bus is buffered immediately when it comes on board by the U87 and U88 transceivers. These transceivers are always enabled and normally point toward the Memory Controller. They point toward the CPU Bus when U37 pin 8 goes low. This only occurs when the board is selected (U36 pin 8 goes high), a read operation is being performed (LBWRT is high), and LSTB is active (U74 pin 6 is high).
- 8-17. After the incoming CPU Data Bus is buffered, it is routed to the Upper Address Register (U29 and U31), the Control Register (U55), the Memory Bus Write Buffers (U20 and U23), the Emulation Bus Transceivers (U7 and U8) and the Mapper RAM data inputs. Most read and write signals for the various registers and Mapper RAMs are generated by address decoders U92 and U93. The write strobe for the Mapper RAMs, however, is generated by U62 pin 3. This occurs each time U76 pin 10 goes positive. The duration of the write strobe is determined by the U75 delay line.
- 8-18. The Memory Bus Write Buffers are used to transfer write data from the CPU Bus to the Memory Bus during a CPU write to Emulation Memory. The CPU Readback Latches (U19 and U21) are used to latch data during a high speed memory read. This permits the CPU to read the latched data when it is ready thereby not tying it up for a microsecond or more at a time.
- 8-19. The Emulation Bus PV Transceivers connect between the Emulation Data Bus and the CPU Data Transceivers. They permit the CPU to look like an emulator during Emulation Bus Performance Verification cycles.

8-20. The Emulation Data Bus also connects to the PV Data Bus Transceivers. These permit the emulator to access Emulation Memory when necessary and are otherwise tri-stated.

- 8-21. The Emulation Memory Bus permits Emulation Memory to be accessed by both the CPU and read/write devices on the Emulation Bus.
- 8-22. Address Buses.
- 8-23. There are four address buses on this board:

The CPU Address Bus (LAO - LA10)
Mapper RAM Address Bus (MRAO - MRA11)
Memory Mapper Address Bus (MAO - MA19)
Emulation Address Bus (LEA1 - LEA23)

- 8-24. The CPU Address Bus is buffered immediately upon entering the board by U89 and U90. After it is buffered, it connects to the Emulation Address Bus PV Buffers (U12 U14) and the Memory/Mapper Address Bus Multiplexers (U9 U11, U28, U30, U32). Also, the outputs of the Upper Address Register (U29 and U31) are a part of the CPU Address Bus. These latched outputs (LLA11 LLA18) constitute the upper half of the CPU Address. The Emulation Address Bus PV Buffers, as previously noted, make the CPU look like an emulator during Emulation Bus PV cycles. The multiplexers select the proper address bus to drive the memory/mapper address lines. The inverted outputs of U31 duplicate the inversion caused by the discrete multiplexer on the Emulation Address Bus's upper 4 bits.
- 8-25. The Emulation Address Bus is connected to the Emulation Address PV Buffers and the Multiplexers. U15 and U16 form a discrete multiplexer which selects between LEA20 LEA23 and LEA8 LEA11 to go to the uppermost Mapper Address Bus Multiplexer. This in turn selects the block size the emulator will use.
- 8--26- The Memory Address Bus is normally formed by the outputs of U9 U11. However, when the 128 word block size is selected, the outputs of U11 are tri-stated and the outputs of U1 pins 3, 5, 7 and 9 are enabled instead. The Mapper Address Bus is then formed by the data outputs of the Mapper RAMs as well as U9 and U10. The Mapper RAM outputs are buffered by U1 and U2 to provide the necessary drive for the Memory Board Address Buffers.
- 8-27. The Mapper RAM Address Bus is formed by the outputs of the U28, U30 and U32 Multiplexers. This bus provides the address for the Mapper RAMs.

8-28. Performance Verification Circuitry.

8-29. In addition to the circuitry already mentioned, U41, U53 pin 8, U38 pin 11, and U32 pin 8 test the Emulation Bus. U38 pins 12 and 13 determine if the Emulation Bus Cables have been removed. If not, grounds on the Emulation Bus will pull down these inputs which are pulled high by R1 and R16 when the cables are removed. If the cables are not removed, a status bit will flag the CPU of this. The PV buffers cannot be enabled unless the Emulation Bus Cables are removed. When LPVEN is set in the Control Register (U55), accesses through address 5XXX Hex with LMAP2 low will be directed through the Emulation Bus. U51 pin 1, U67 and U54 pin 6 add wait states which slow down the CPU long enough to compensate for the delays added by all the buffers.

8-30. Read/Write Strobe Circuitry.

8-31. Three Sections of U17 form the read strobe generator. If the multiplexers are pointed toward the emulator (MPX low) and the emulator is reading (LEWRT high), or if the multiplexers are pointed toward the CPU (MPX high) and the CPU is reading (LBWRT high), HREAD will be high and a read is indicated. U33, U34, U35 and parts of U18, U36 and U37 form the write strobe generation circuitry. Depending upon the states of LEBYT and LEBUP, or LEBUP and LUPB, the outputs of U35 will allow generation of either LWRU or LWRL, or both. Depending upon the output of U37 pin 12, writes from the emulator may be prevented. The signals that initiate the write strobes are: CPUWSTB for the CPU, and EMWSTB for the Emulator.

8-32. CPU Emulation Memory Access Circuitry.

8-33. A CPU access is initiated when LMAP1 and LBSEL are LBSTM makes a high to low transition (HBSTM also goes high). At this time, two actions are initiated: LMSYN is pulled low and U42 pin makes a high to low transition which starts a circuit timeout action of about 1 ms (U42 - U44). Then, when LBSTB goes low, the CPU request is initiated (U77 pin 5 goes high). If CNTLA is high, the CPU request will be granted within 40 ns after LMAV goes low. If never goes low, the access will never be granted, in which case the timeout circuitry will timeout and release the CPU. It will also clear a status bit signifying that the access was never granted. The status bit will remain clear until read, at which time U42 pin 7 and U78 pin 11 will set it again. If the access is granted by LMAV going low or if CNTLA is low, it is allowed to continue by U78 pin 8 going high. Since accesses are granted asynchronously with respect to the synchronous state machine (U80, U95 and U96), the accesses must be synchronized. This is done by the CPU access synchronizer (U64). A discrete negative edge latch is used to reduce the time that the output might When U64 pin 11 goes low signifying a granted access. meta-stable. U80 pin 10 goes high and starts the state machine in

The state machine first turns the multiplexers toward the CPU (U96 pin 5 goes low which causes U93 pin 6 to go high. Two states later, U95 pin 5 goes high which causes the CPUWSTB (U62 pin 11) to go low. At the same time this occurs U96 pin 6 goes low causing U94 pin 11 to go low. This clears the access request (U77 pin 5), clears the CPU holdoff (U77 pin 9), and also clears the timeout oneshot. When the oneshot is cleared, U42 pin 9 makes a low to high transition and clocks a low into U44 pin 2, which does not change it from its stable state. If U42 pin 9 timed out without being cleared, a high would be clocked into U44 pin 2. This would cause U44 pin 5 to go high for 50 ns which would clock a low into the access status register (U44 pin 9). With U95 pin 5 high, MPX stays high and, when two U96 pin 5 goes low two states later, the CPUWSTB will go high. Then, the next state would clock a low into U95 pin 5 causing MPX to go low and stop the state machine. The state machine and all access circuitry is cleared at power on by LBPOP and LBBPOP. U93 pin 5 is used to turn the multiplexers around for loading the Mapper RAMs.

8-34. Emulation Memory Access Circuitry.

8-35. An Emulation Memory access is initiated any time HMAV goes low. The state of CNTLB (U53 pin 2) determines the delay from HMAV (from the Emulation Bus) TCLK (U51 pin 10) going high. If CNTLB is high, HMAV propagates through U53, U52 and U51. If CNTLB is low, HMAV propagates through U56 pin 11, U51 pin 12 and U51 pin 9. U52 provides a 60 ns delay for TCLK to permit the address to propagate through the Mapper RAMs and be valid at the outputs of the buffers. initiates several actions. First, it clocks the LUSER status bit into U49. If LUSER is low, reads are disabled by U50 pin 13 and writes are disabled by U62 pin 10. If LUSER is high, the access proceeds normally. TCLK also clocks the LGRD status bit into U65. If LBRK (U54 pin 12) and LMBRKS (U56 pin 2) are pulled low. When LBRK is asserted, it can only be released by performing an ID read. This causes LCLSTA to toggle which clears all of U65. TCLK also initiates the triggering of HREADY (U68 pin 11). The inputs to U66 pins 11 and 12 are gated to allow LEWRT (U50 pin 10) and HWDV (U53 pin 5) to transition either before or after TCLK and still provide the necessary time for a write cycle. When U66 pin 9 is triggered, the output goes low for 125 ns (+ or -5ns) and then goes high again. This causes a low to be clocked into U49 pin 9. HREADY, which went low when U50 pin 1 went high, is then allowed to go high again, signifying that the cycle is completed.

Model 64155A

which will return EMWSTB high.

8-36. For certain emulators, HWDV will not go high within 125 ns of TCLK. This would cause this circuitry to react as though a read was

performed before the write cycle was one half completed. To prevent this, when HWDV propagates through U53 pins 5 and 6, U66 pin 6 is triggered. This causes U51 pin 4 to go low which in turn presets U49 pin 9. If HREADY has already gone low and back high again, the preceeding circuit action will cause it to again go low. Therefore, when HWDV occurs later than than 125 ns after TCLK, the emulator must be able to tolerate HREADY going high for a period during the cycle. If HWDV goes high before the timeout is complete, HREADY will stay low and U66 pin 9 will be retriggered to start the cycle from that point in time. The gated HWDV is also used to clock LROM into U65 pin 10. If LROM is low and LROMEN is low, LBRK and LMBRK will be pulled low. They must be cleared as described above. LMAV going low again clears both one shots and the LUSERL flip flop. It also presets U49 pin 9 for the next cycle. HWDV also initiates the Emulation Memory Write Strobe. EMWSTB. If LUSERL is high and HWDV goes high, U62 pin 8 will go low. If CNTLC (U27 pin 2) is low, U27 pin 1 will go high and cause EMWSTB (U18 pin 4) to go low and stay low until HWDV goes high and propagates through the circuitry. Then, EMWSTB will go high again. If CNTLC (U53 pin 12) is high, the output of U62 pin 8 will cause U27 pin 4 to go high. This drives U53 pin 11 high causing EMTSTB to go low. At the same time the output of U62 pin 8 propagates through U79 pins 1 and 2

and the U26 50 ns delay line. After this occurs, U27 pin 4 will go low

Table 8-1. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term).

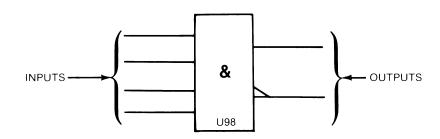
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol

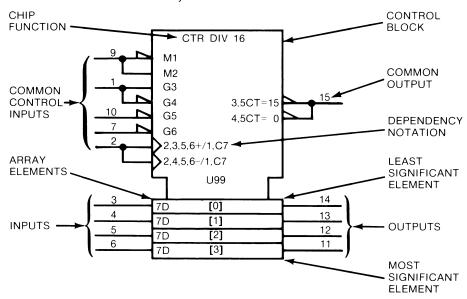
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements,)

ARRAY ELEMENTS - All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. The least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in []).

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer,

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

- a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.
- b. Interconnection (Z) indicates connections inside the symbol.
- Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are
- Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.
- Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).
- Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.
- Address (A) identifies the address inputs.

DEPENDENCY NOTATION SYMBOLS

- Address (selects inputs/outputs) (indicates binary range) Control (permits action)
- EN Enable (permits action)
- AND (permits action)
- Mode (selects action)

- Negate (compliments state)
- Reset Input Set Input
- OR (permits action)
- Interconnection

OTHER SYMBOLS

→ Shift Right (or up)

 Φ Logic symbol not defined due to complexity.

J J Input

| | AND | 0 | Negation | / | Solidus (allows an input or output to ha more than one function) |
|---|--------------|----------------|--|----------|--|
| | Bit Grouping | -X- | Nonlogic Input/Output | ∇ | Tri-State |
| > | Buffer | \triangle | Open Circuit (NPN) (external resistor) | ٧ | |
| | Compare | ፟ | Open Circuit (PNP) (external resistor) | , | Causes notation and symbols to effi inputs/outputs in an AND relationship, and occur in the order read from left to right. |
| > | Dynamic | ≥1 | OR | | |
| 1 | Exclusive OR | ♦ | Passive Pull Down (internal resistor) | () | Used for factoring terms using algebr techniques. |
| L | Hysteresis | 会 | Passive Pull Up (internal resistor) | [] | Information not defined. |
| | | | | | |

LABELS

CO Carry Output

Postponed

← Shift Left (or down)

? Interrogation

BCD

BIN BUF

CTR DEC

BG Borrow Generate

| ы | Borrow Input | CP | Carry Propagate | K | K Input |
|----|------------------|----|-----------------------------|---|------------|
| ВО | Borrow Output | CT | Content | Р | Operand |
| BP | Borrow Propagate | D | Data Input | Т | Transition |
| CG | Carry Generate | Ε | Extension (input or output) | + | Count Up |
| CI | Carry Input | F | Function | - | Count Down |

MATH FUNCTIONS

| \sum | Adder | > | Greater Than |
|--------|-----------------------|-------|---------------------------|
| ALU | Arithmetic Logic Unit | < | Less Than |
| COMP | Comparator | CPG | Look Ahead Carry Generato |
| DIV | Divide By | π | Multiplier |
| = | Equal To | P-Q | Subtractor |

CHIP FUNCTIONS

| Binary Coded Decimal | DIR | Directional | RAM | Random Access Memory |
|----------------------|------|---------------|------|----------------------|
| Binary | DMUX | Demultiplexer | RCVR | Line Receiver |
| Buffer | FF | Flip-Flop | ROM | Read Only Memory |
| Counter | MUX | Multiplexer | SEG | Segment |
| Decimal | OCT | Octal | SRG | Shift Register |
| | | | | |

DELAY and MULTIVIBRATORS

| Astable |
|-----------------------------|
| Delay |
| Nonretriggerable Monostable |
| Nonvolatile |
| |

Retriggerable Monostable

MEMCON 8-15

Service

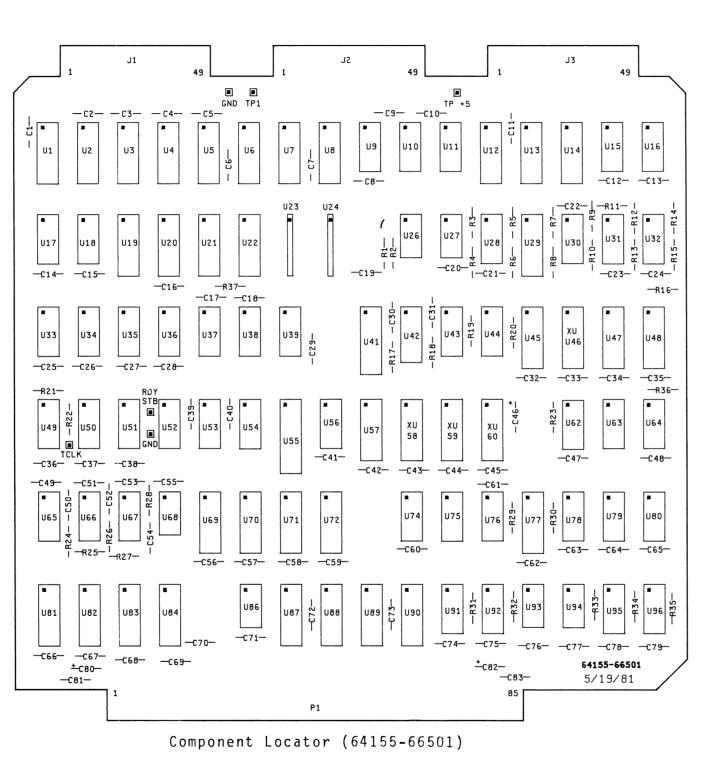


Figure 8-2. 64155A Wide Address Memory Controller

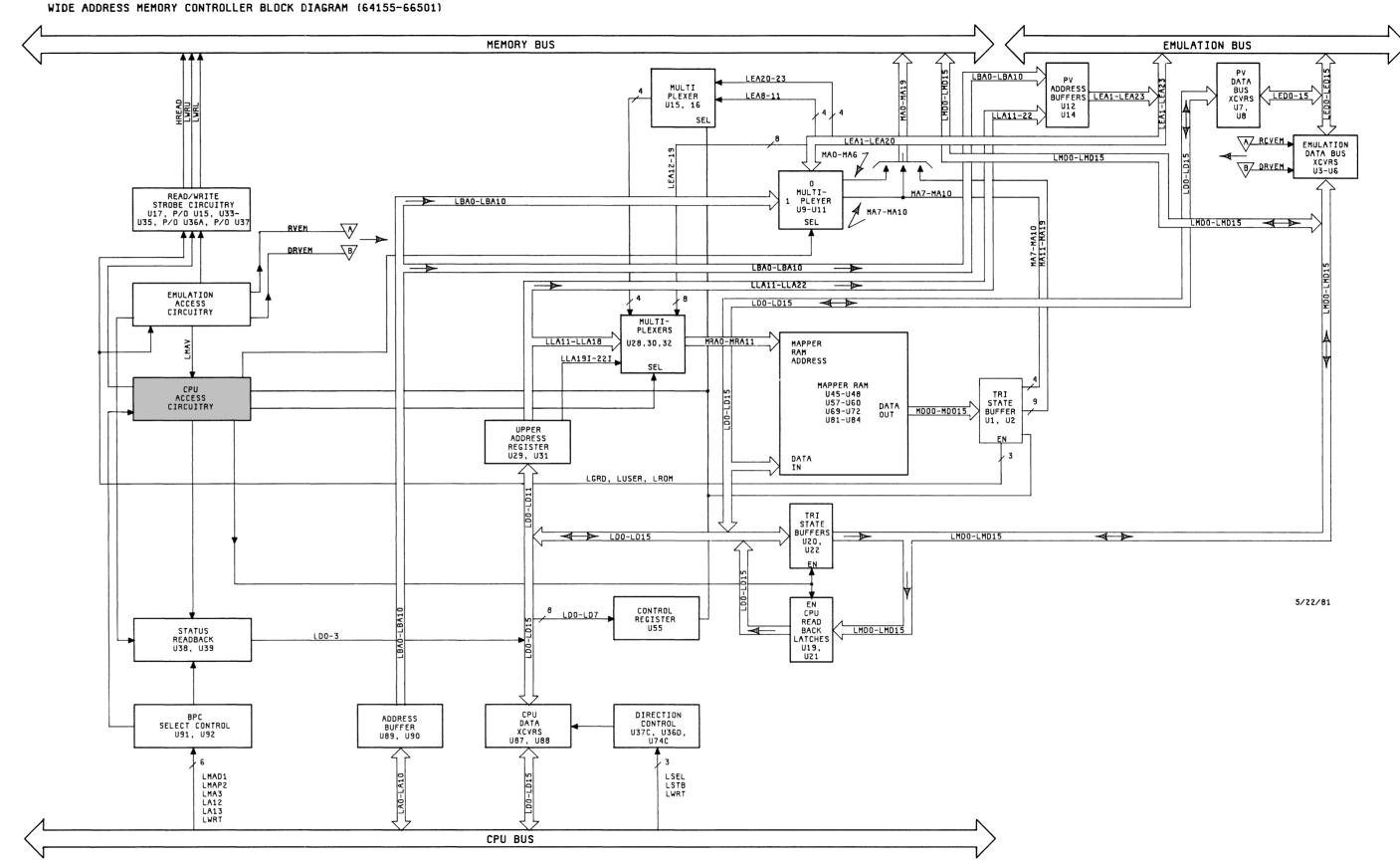


Figure 8-3. CPU Access Timing (Sheet 1 of 2)

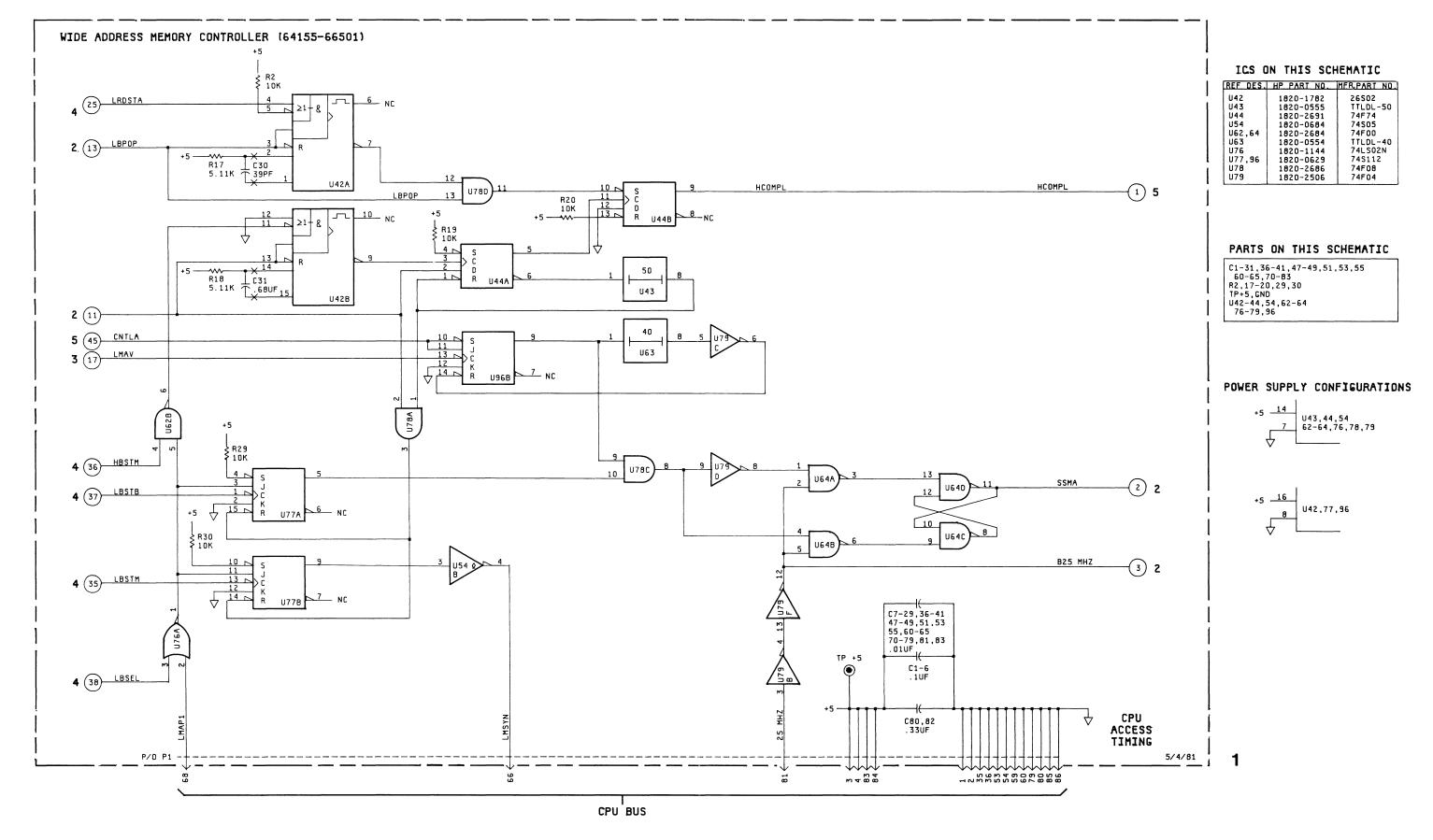


Figure 8-3.
CPU Access Timing (Sheet 2 of 2)
MEMCON 8-17

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

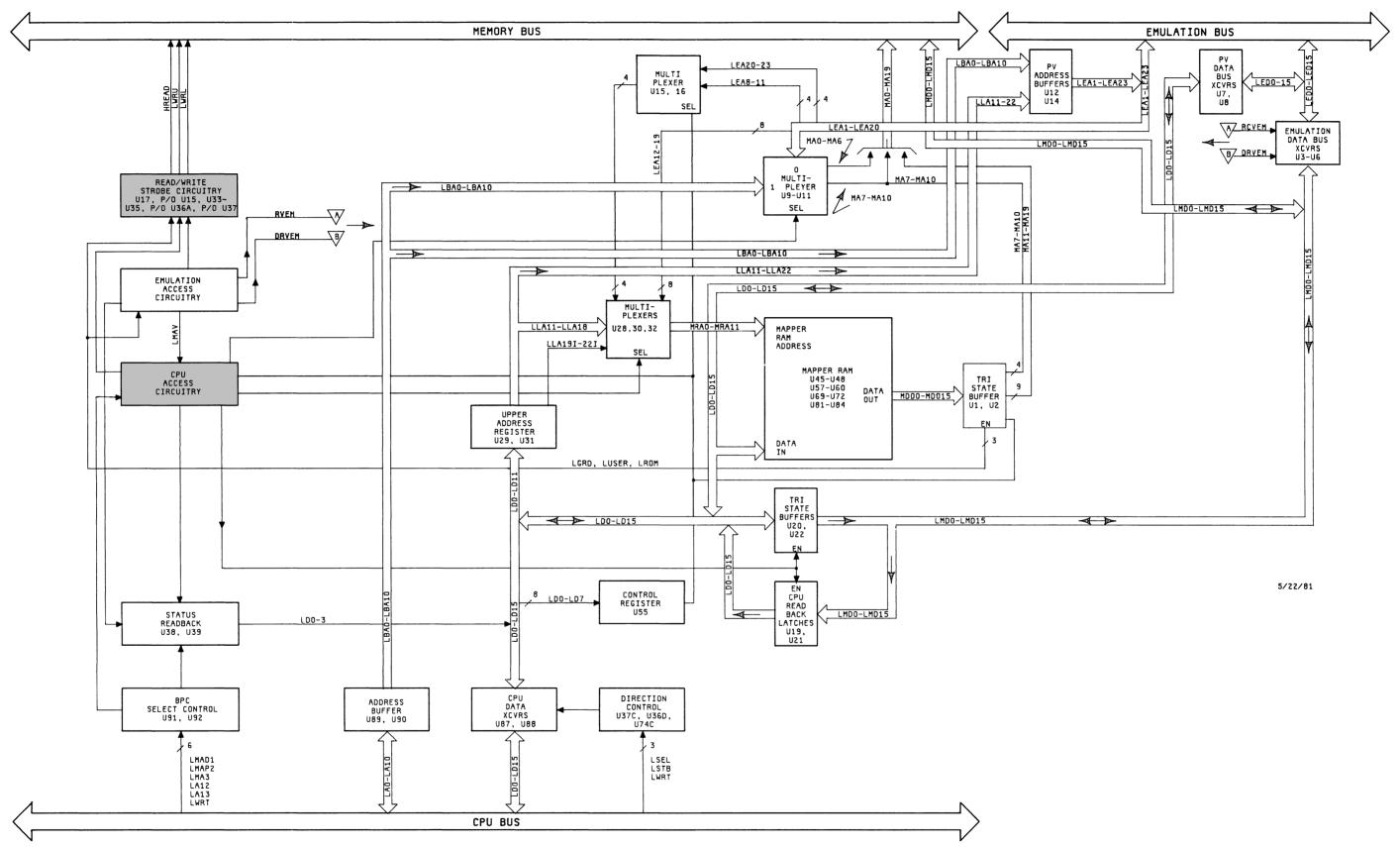


Figure 8-4. CPU Access Timing and Read/Write Strobe Generation (Sheet 1 of 2)

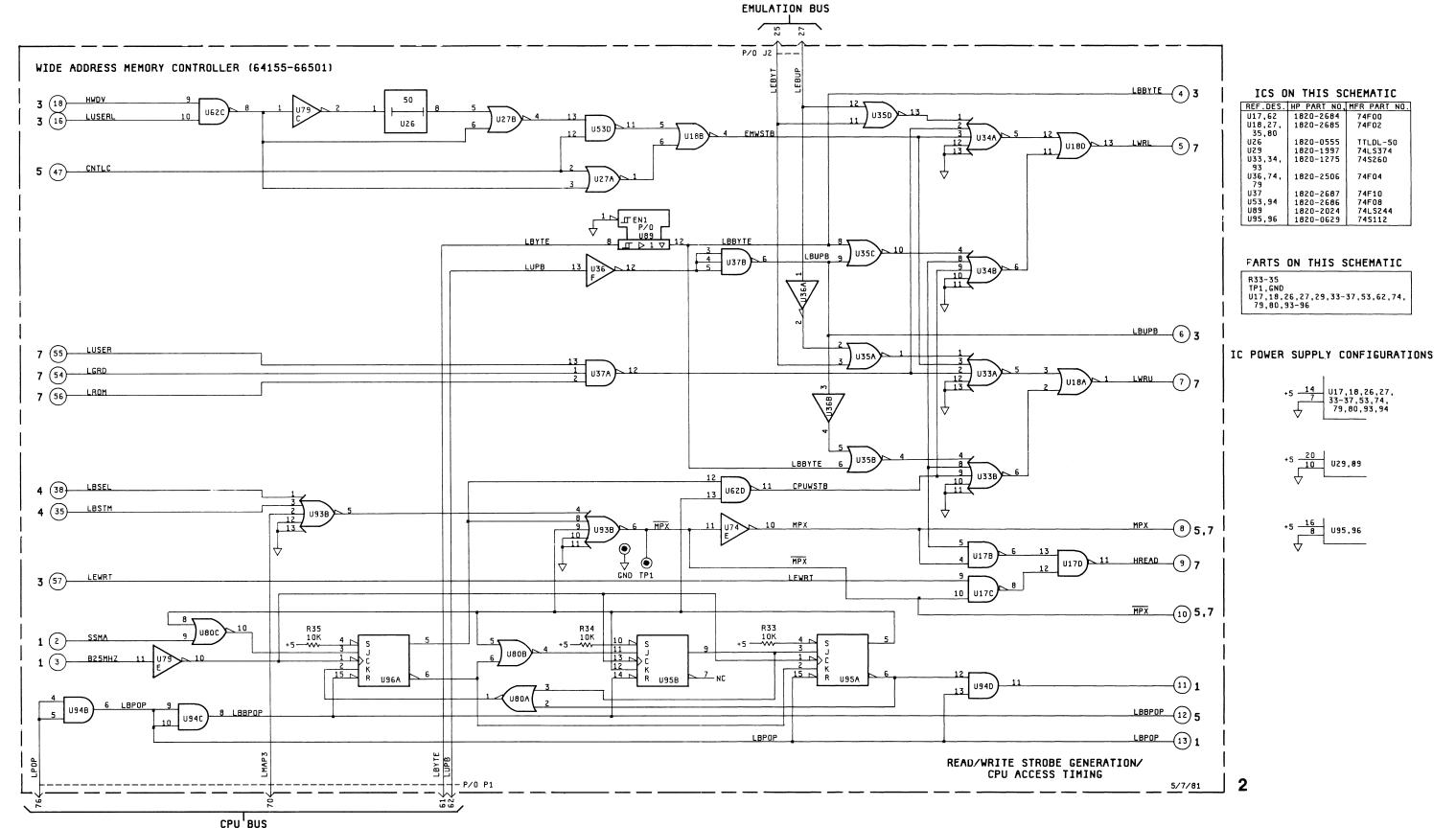


Figure 8-4.
CPU Access Timing and Read/Write Strobe Generation
(Sheet 2 of 2)
MEMCON 8-19

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501) MEMORY BUS EMULATION BUS PV DATA BUS XCVRS U7, U8 PV ADDRESS BUFFERS U12 U14 LBA0-LBA10 LEA20-23 MULTI PLEXER U15, 16 LEDO-15 LLA11-22 EMULATION DATA BUS XCVRS U3-U6 MAO-MA6 7 LMDO-LMD15 B DRVEM MULTI-1 PLEYER U9-U11 READ/WRITE STROBE CIRCUITRY U17, P/O U15, U33-U35, P/O U36A, P/O U37 ■ LBAO-LBA10 —₩_ SEL _____B LBA0-LBA10 LLA11-LLA22 EMULATION ACCESS CIRCUITRY LDO-LD15 MULTI-PLEXERS LLA11-LLA18 U28,30,32 MAPPER RAM ADDRESS LLA19I-22I MAPPER RAM U45-U48 U57-U60 U69-U72 U81-U84 CPU ACCESS CIRCUITRY MD00-MD015 TRI STATE BUFFER DATA OUT UPPER ADDRESS REGISTER U29, U31 DATA In LGRD, LUSER, LROM TRI STATE BUFFERS U20, U22 LMD0-LMD15 ■ LD0-LD15 EN CPU READ BACK LATCHES U19, U21 5/22/81 8 LDO-LD7 CONTROL REGISTER U55 LMDO-LMD15 STATUS READBACK U38, U39 DIRECTION CONTROL U37C, U36D, U74C CPU DATA XCVRS U87, U88 BPC SELECT CONTROL U91, U92 ADDRESS BUFFER U89, U90 LMAD1 LMAP2 LMA3 LA12 LA13 LWRT LSEL LSTB LWRT

CPU BUS

Figure 8-5. Emulation Access Timing (Sheet 1 of 2) 8--20~MEMCON

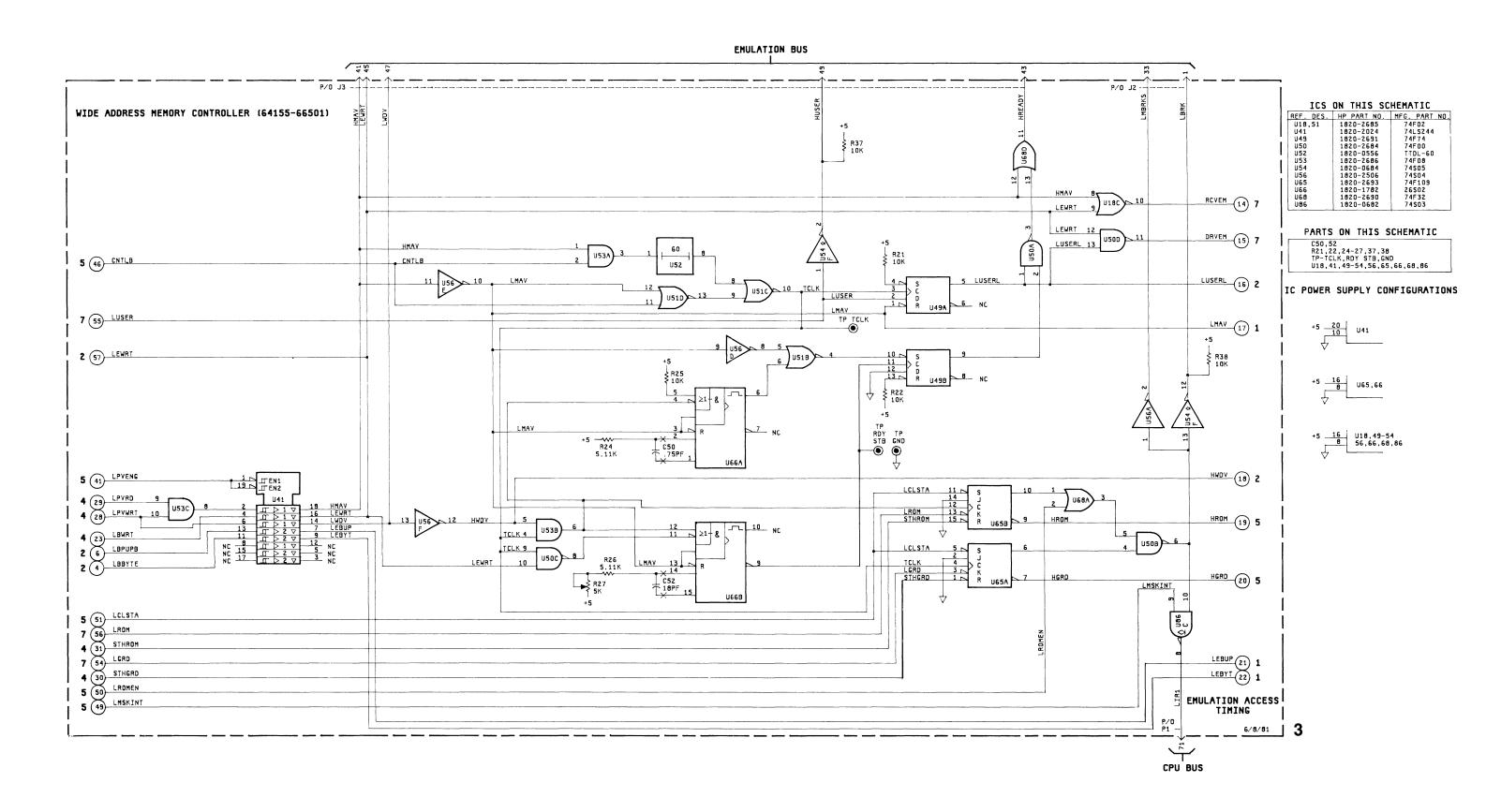


Figure 8-5.
Emulation Access Timing (Sheet 2 of 2)
MEMCON 8-21

Model 64155A

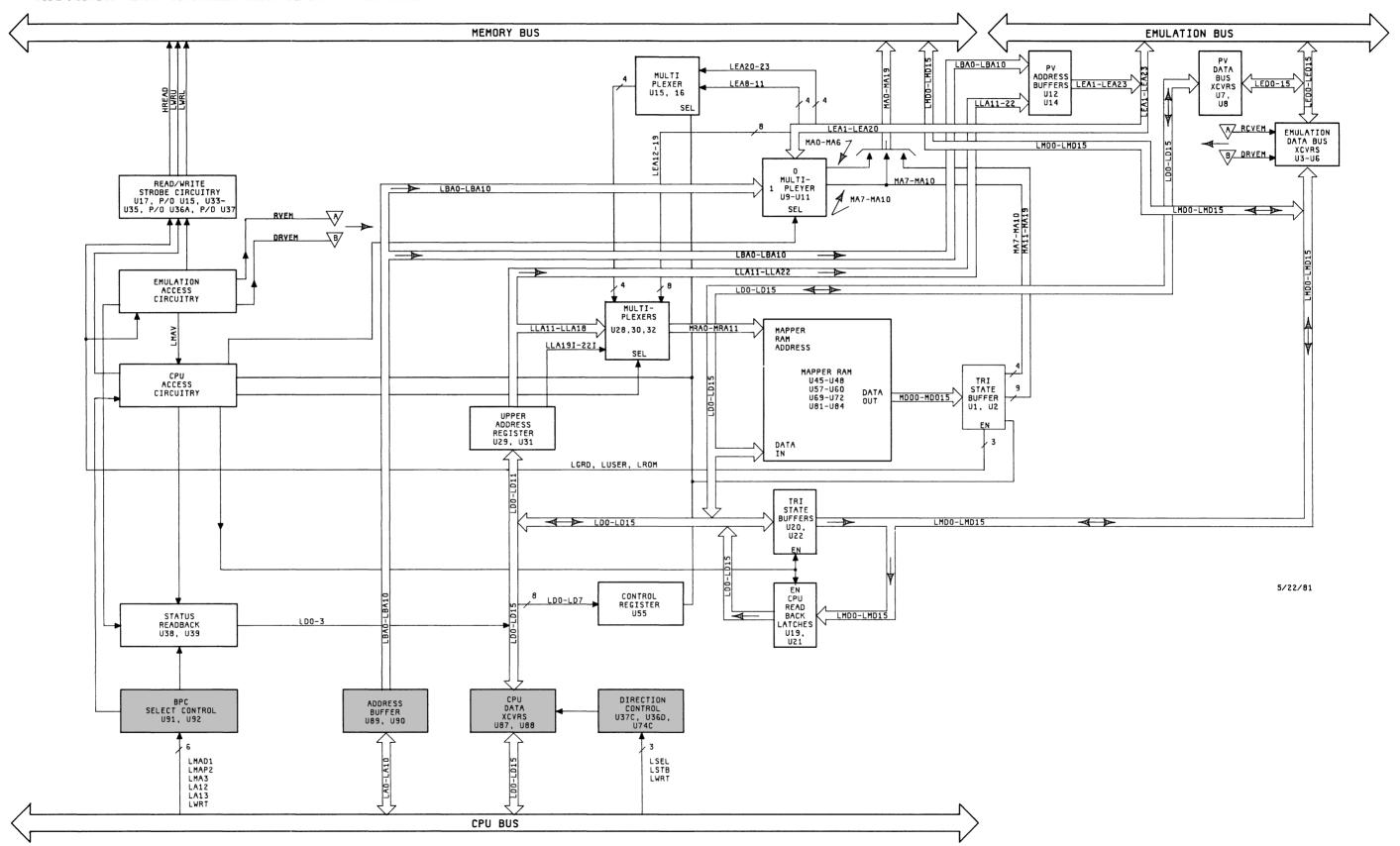


Figure 8-6. CPU Control Select and CPU Address and Data Buffers (Sheet 1 of 2)

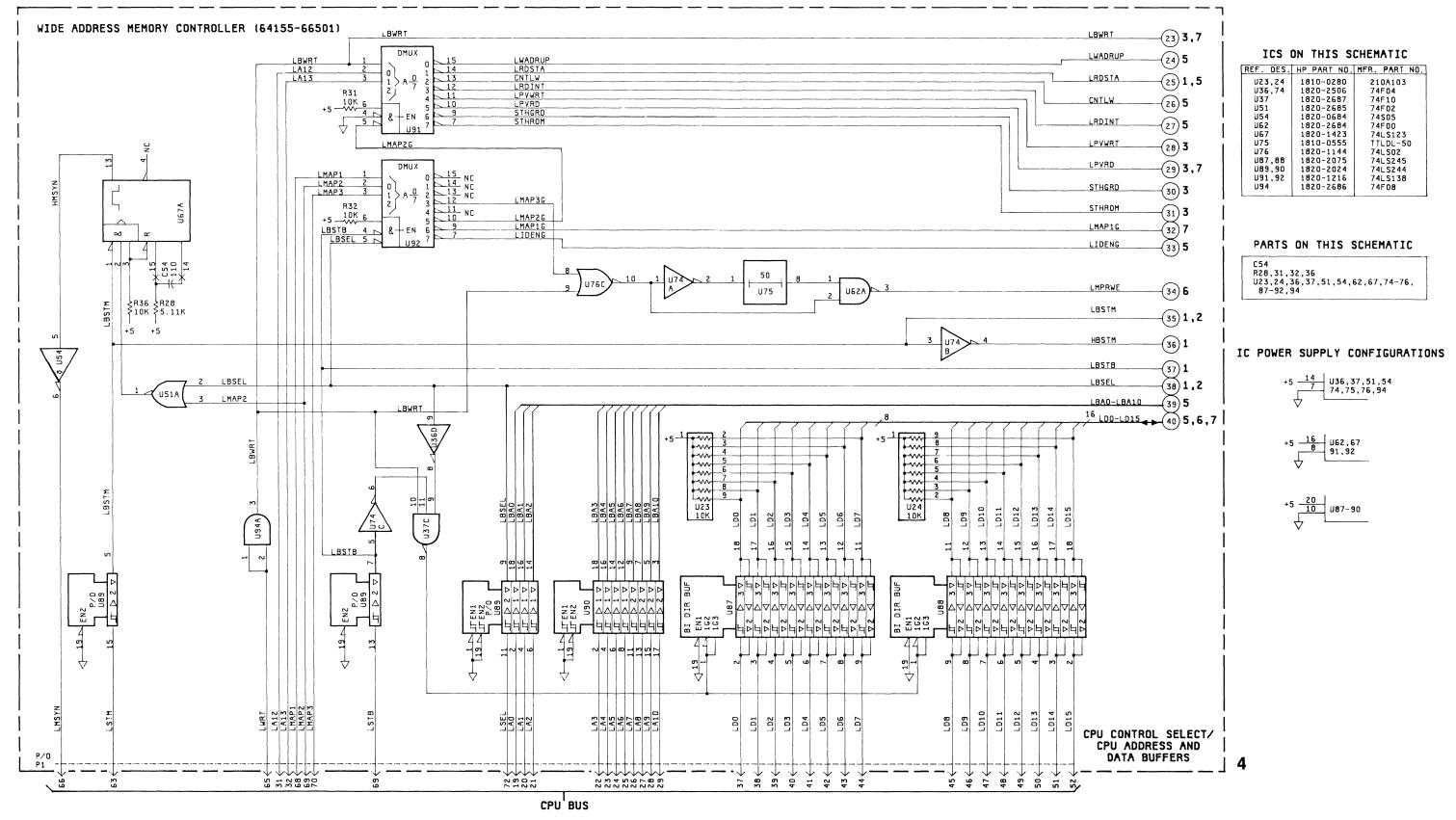


Figure 8-6.
CPU Control Select and CPU Address and Data Buffers
(Sheet 2 of 2)
MEMCON 8-23

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

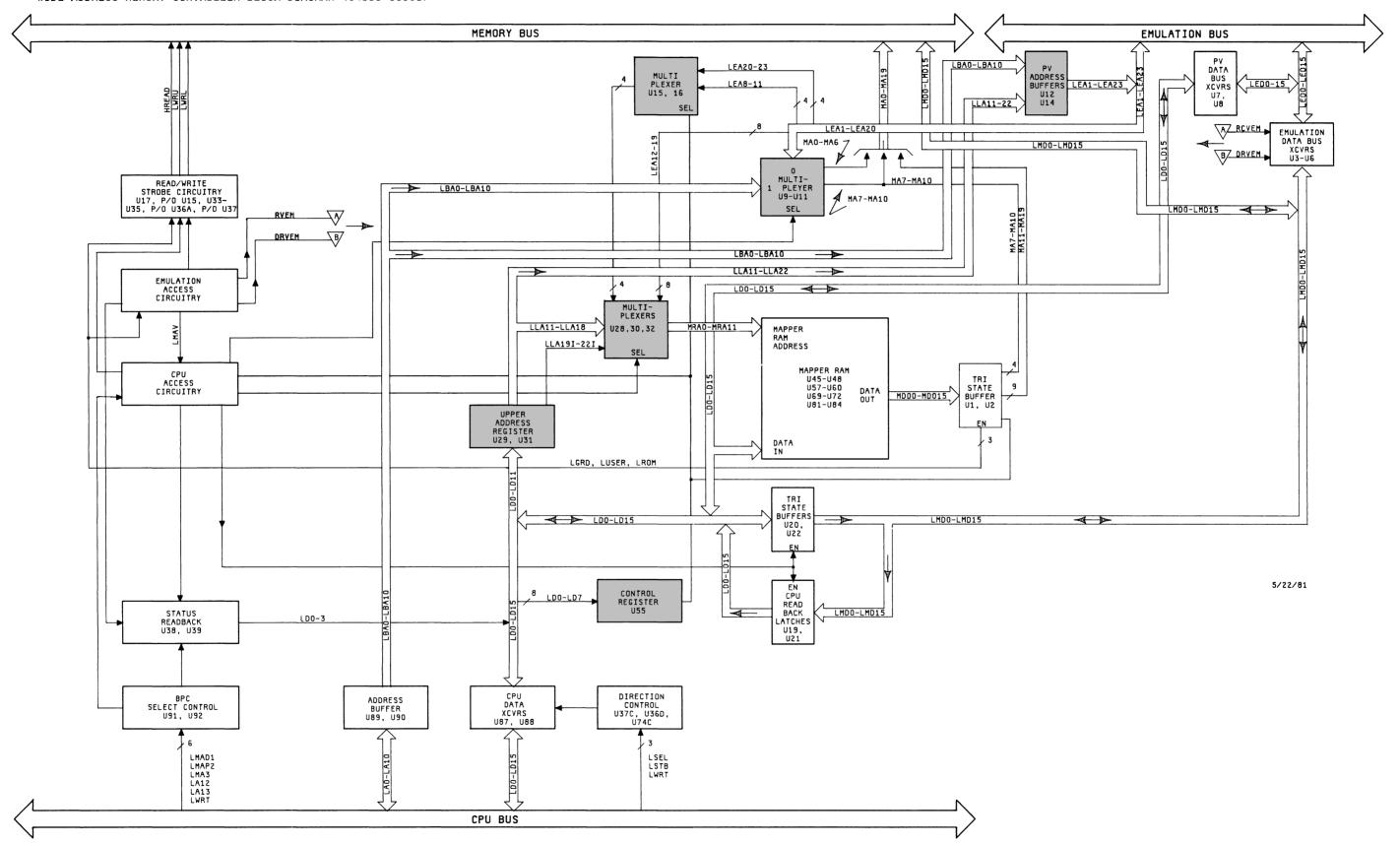


Figure 8-7. Mapper RAM Address Generator and Memory Address Specifier (Sheet 1 of 2)

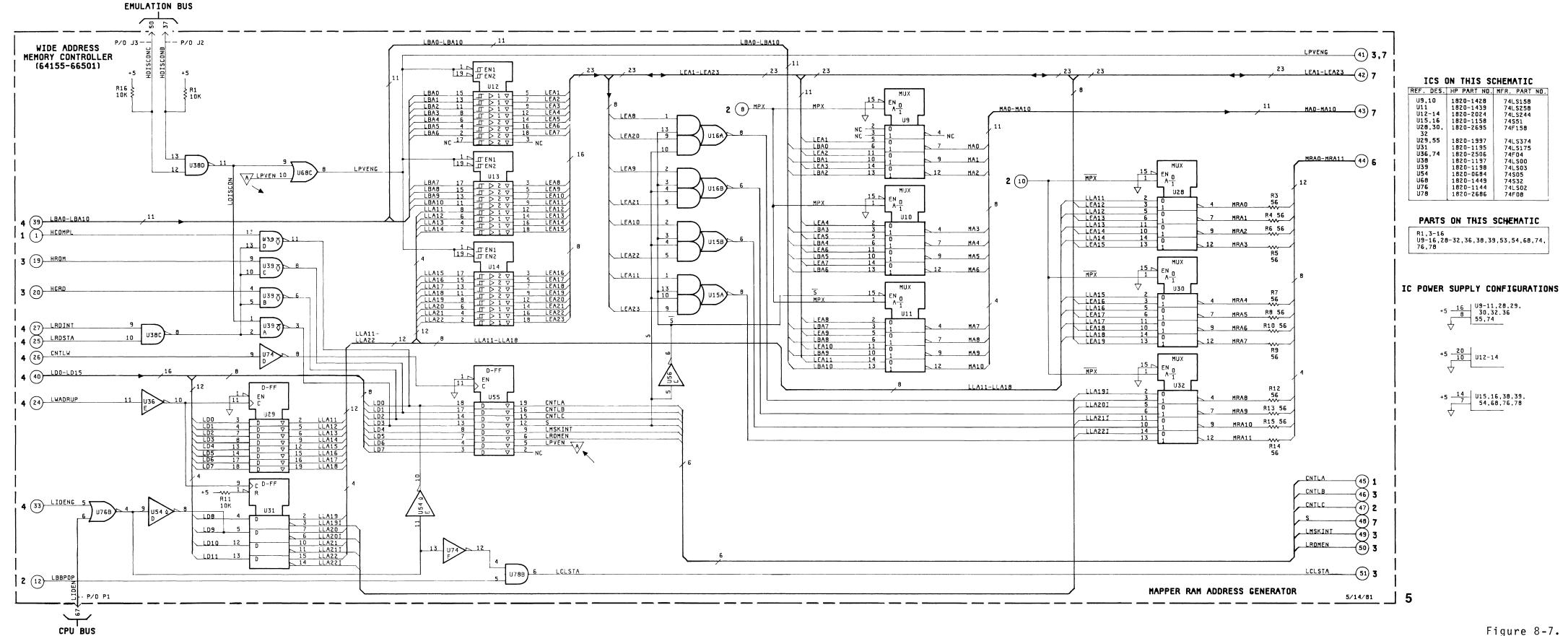


Figure 8-7.
Mapper RAM Address Generator and Memory Address Specifier
(Sheet 2 of 2)
MEMCON 8-25

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

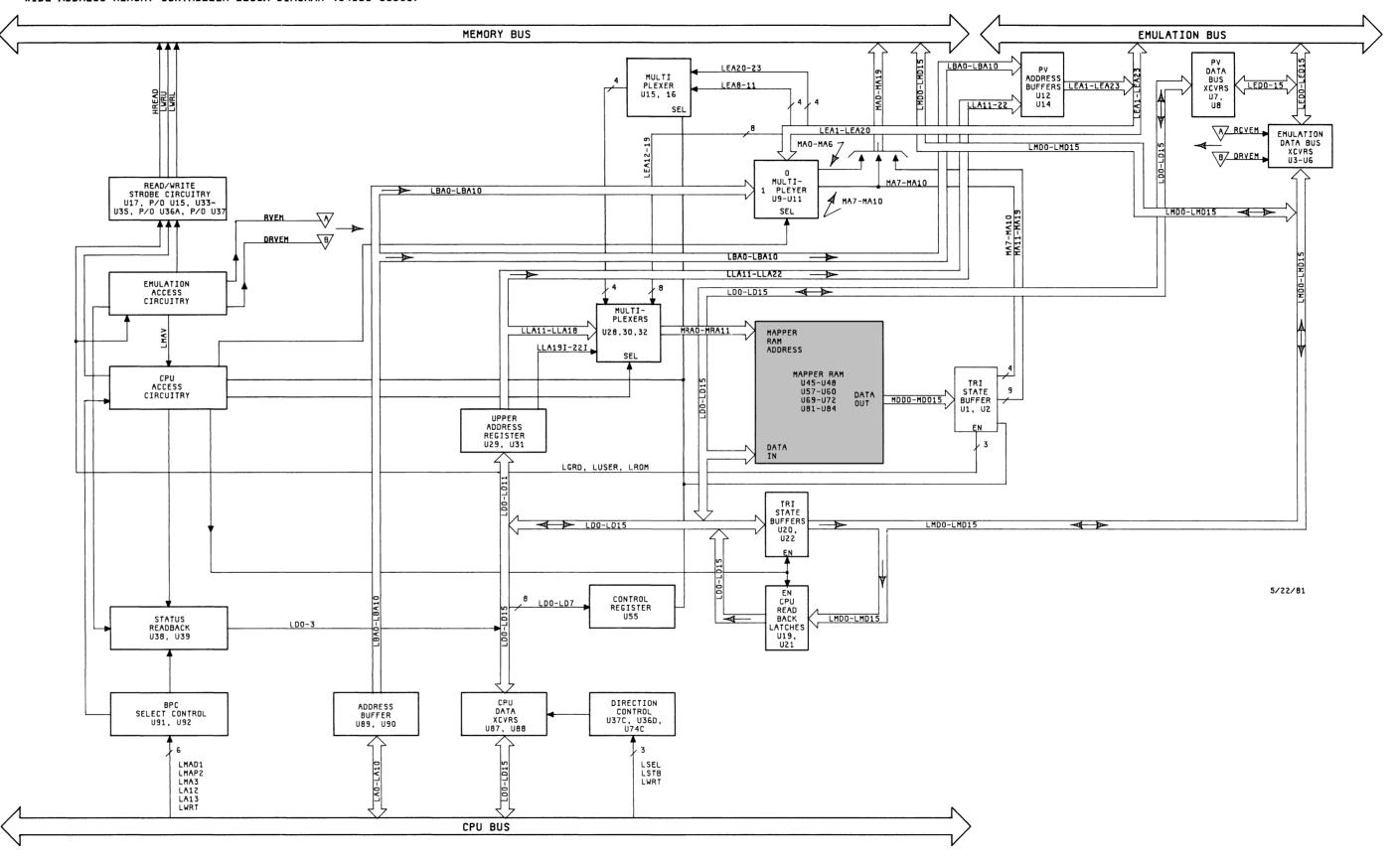


Figure 8-8. Mapper RAMs (Sheet 1 of 2)

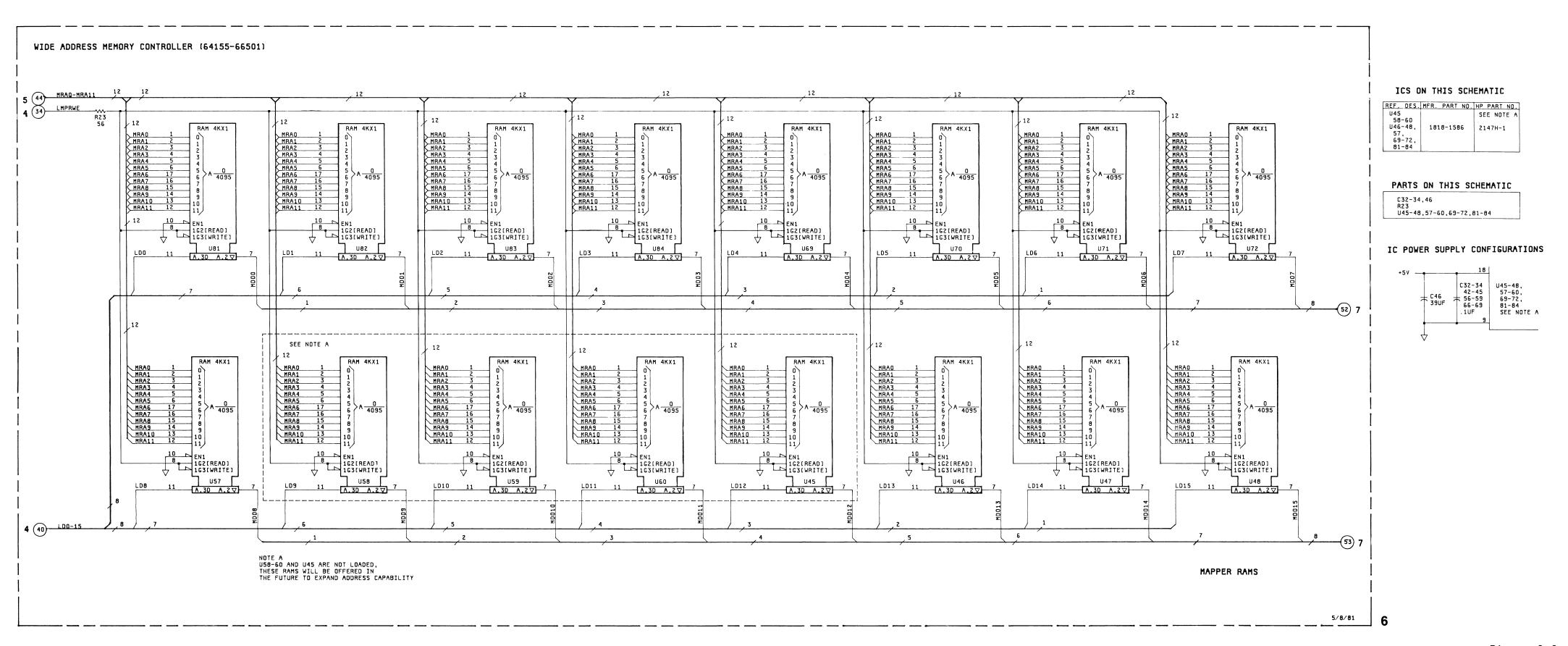


Figure 8-8.
Mapper RAMs (Sheet 2 of 2)
MEMCON 8-27

WIDE ADDRESS MEMORY CONTROLLER BLOCK DIAGRAM (64155-66501)

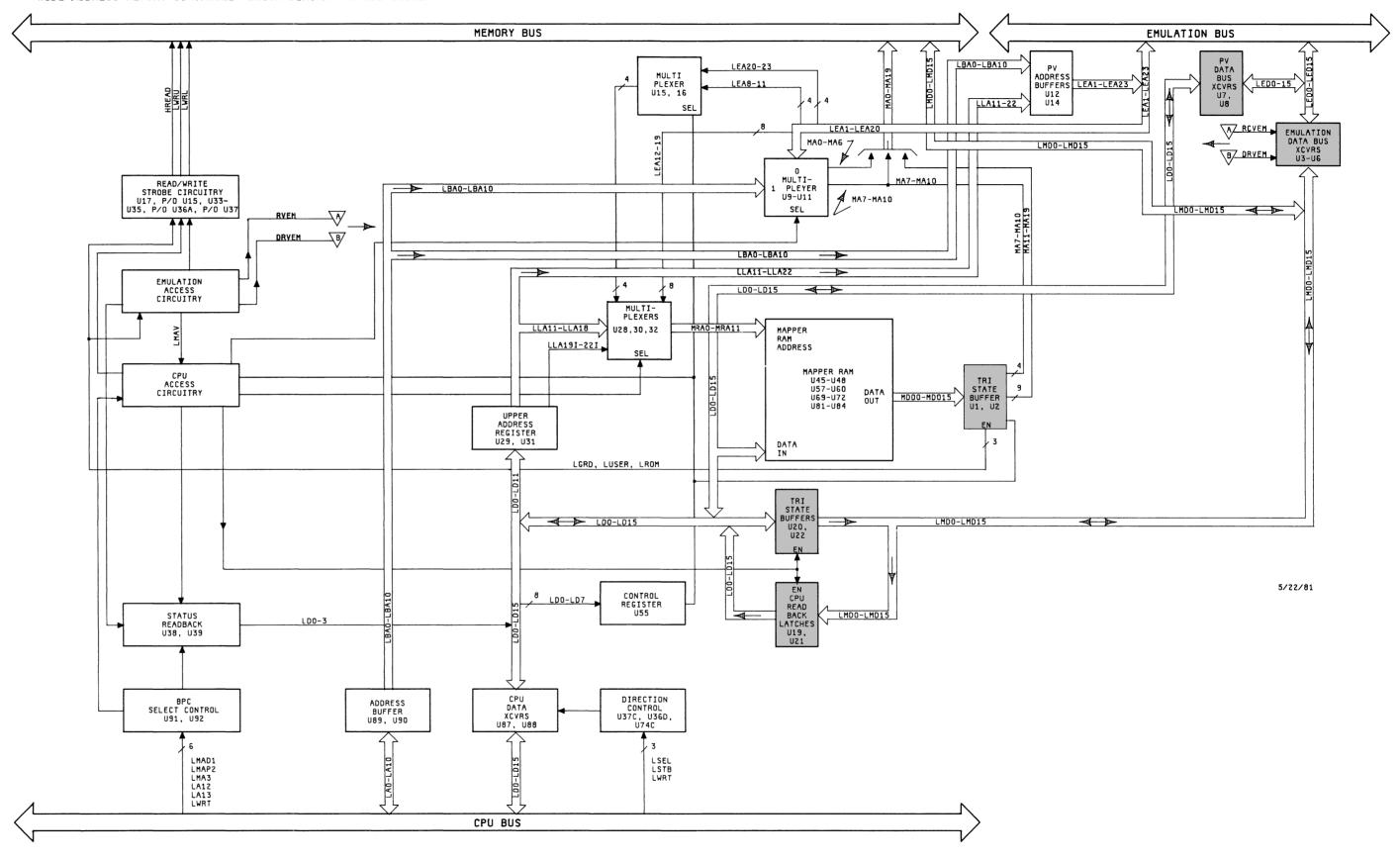


Figure 8-9. Address Mapper (Sheet 1 of 2)

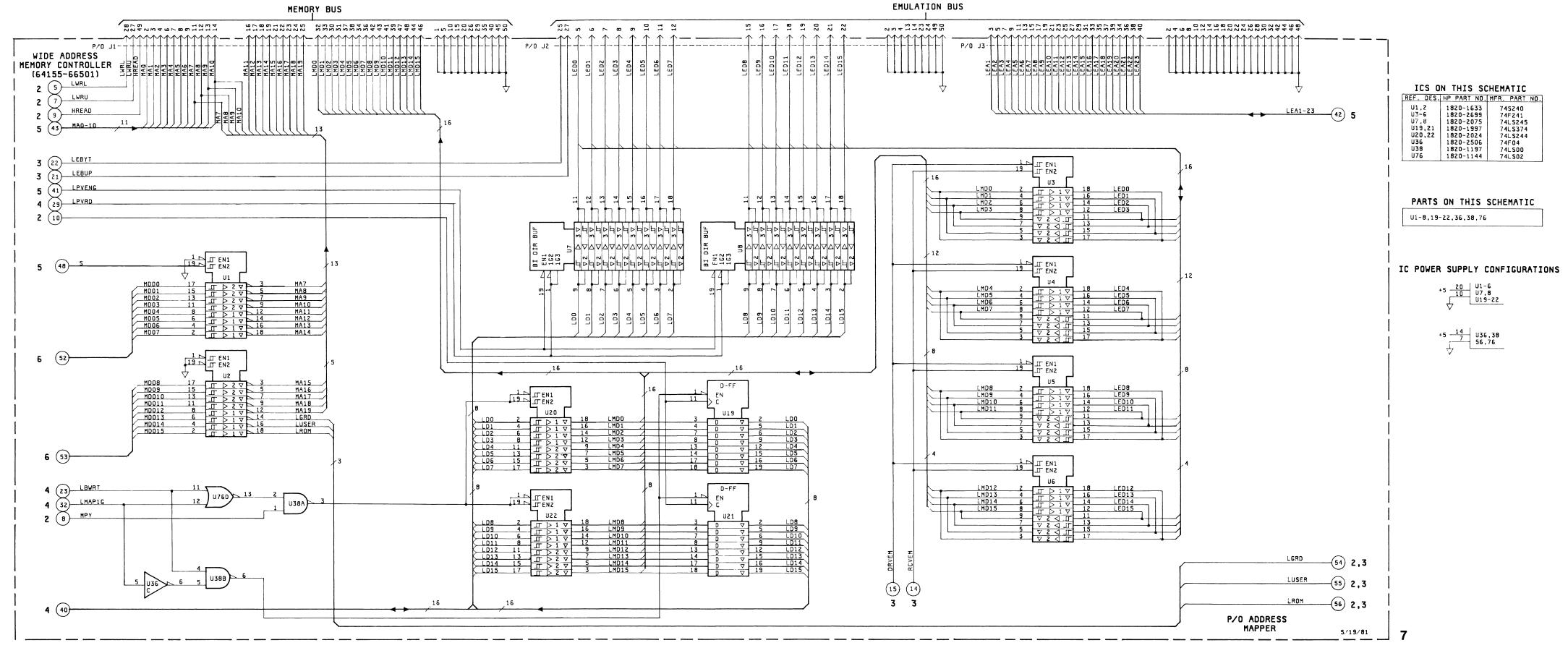


Figure 8-9.
Address Mapper (Sheet 2 of 2)
MEMCON 8-29





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