

# 64000 LOGIC DEVELOPMENT SYSTEM



## SITE SELECTION AND INSTALLATION

## **CERTIFICATION**

*Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.*

## **WARRANTY**

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

## **LIMITATION OF WARRANTY**

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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## **ASSISTANCE**

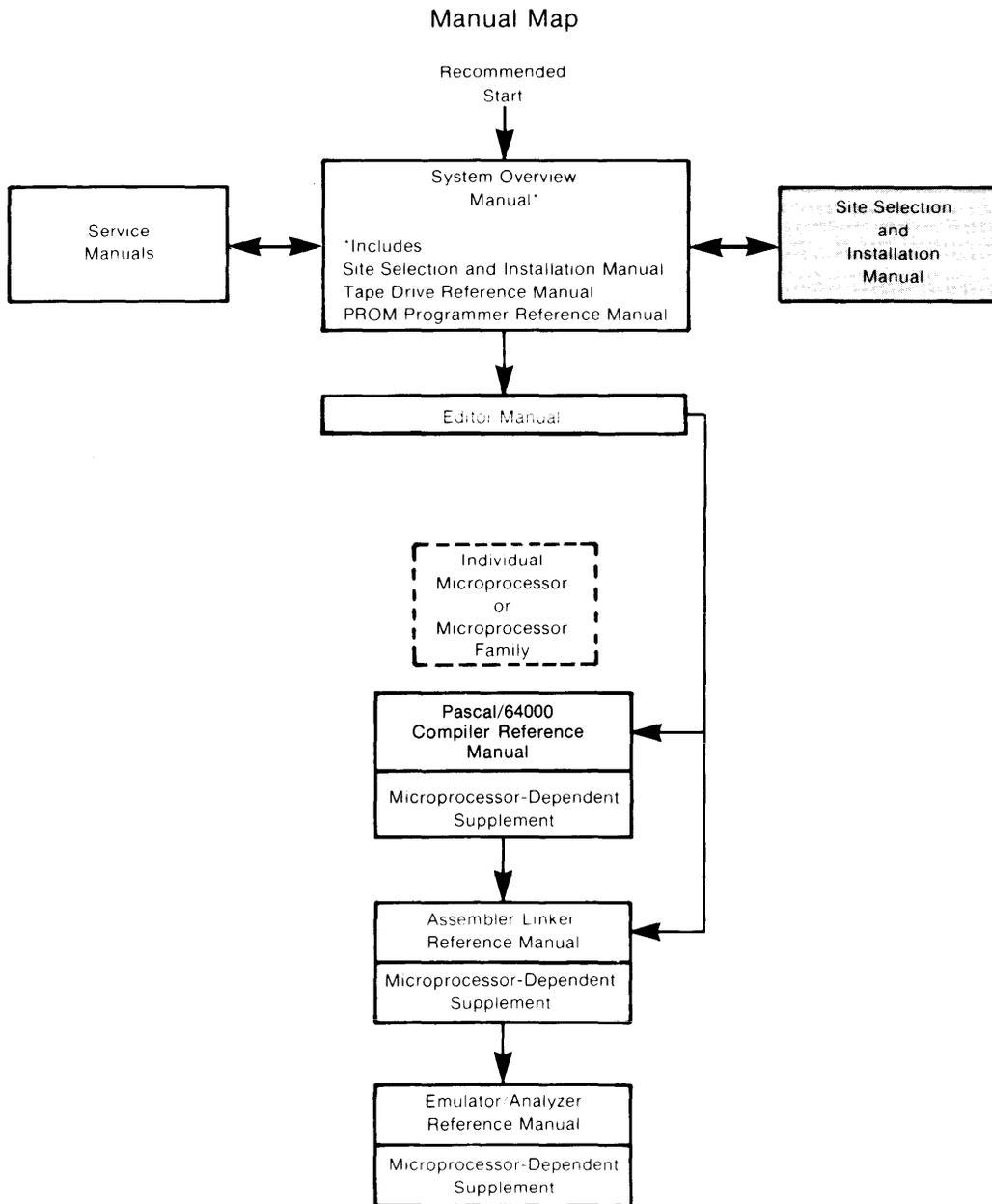
*Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.*

*For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.*

# Model 64000 Reference Manuals

The following block diagram shows the documentation scheme for the HP Model 64000 Logic Development System. The interconnecting arrows show the recommended progression through the manuals as a way of gaining familiarity with the system.

For a detailed map showing specific manuals and their part numbers, refer to the Manual Map in the System Overview Manual.



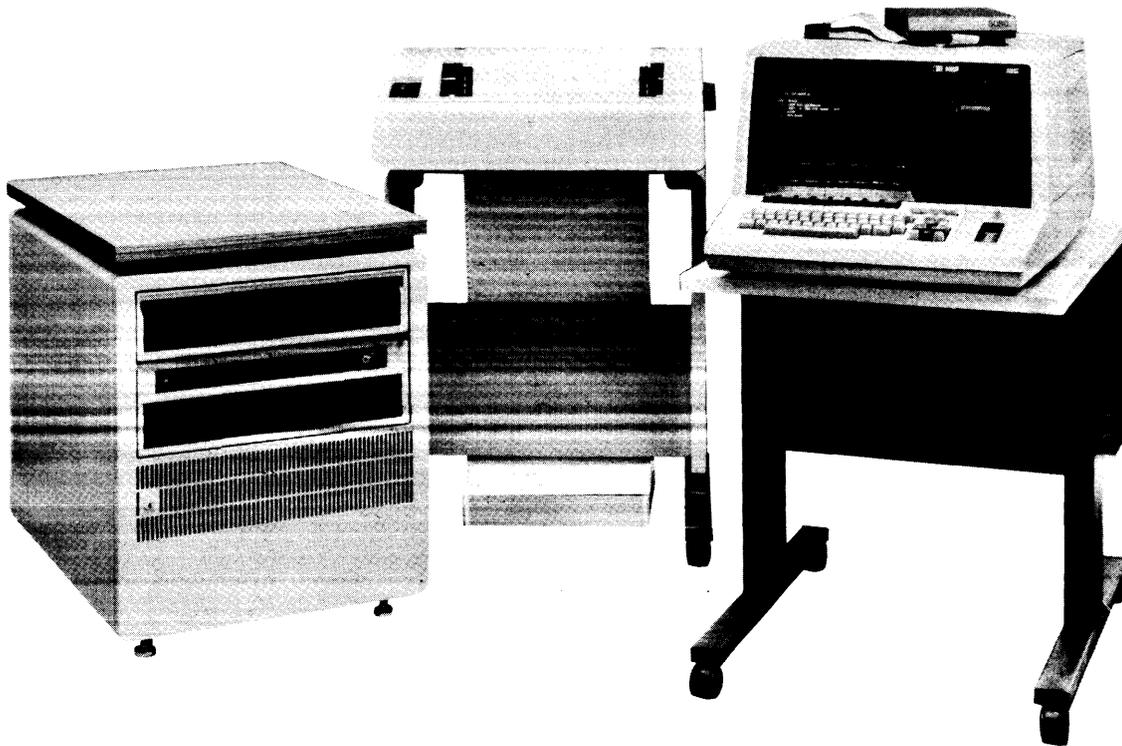
## **Printing History**

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## Site Selection and Installation



**HP Model 64000 Logic Development System**

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## **NOTE**

The contents of this manual have been taken directly from the System Overview Manual and reflect the chapter number, page numbers, and figure and table numbers used in that manual.

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# Chapter 2

## Site Selection and Installation

### Introduction

This chapter provides information for site selection, installation, and checkout of the Model 64000 Logic Development System.

### Quick System Connect and Checkout

After site selection criteria (as detailed in this chapter) are met, the following brief outline may be used to get the system up and running.

- a. Unpack system components.
- b. Do performance verification on development stations.  
Set development station boot-up switches to PERFORMANCE VERIFICATION.
- c. Verify U3 and U4 are set for master acontroller (see figure 2-24).
- d. Set address switches on system components as follows:

disc = 0, line printer = 1, development stations = 2-7

- e. Connect disc to development station (components in series).
- f. Initiate system tape (HP Model 64800).
- g. Run disc performance verification. Format disc. Load system software.
- h. Connect system line printer.
- i. Add additional development stations one at a time.

## Site Selection Responsibilities

### Customer

It is the customer's responsibility to provide adequate space, electrical power, and air conditioning to ensure that the selected site will be suitable for HP installed equipment. Hewlett-Packard retains the right to refuse to maintain supplied equipment if the area is deemed inadequate.

The customer is also responsible for unpacking, inventory, and placement of equipment on the selected site; all necessary information is provided in this chapter.

### NOTE

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The Model 64000 generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the Operating and Service Manuals, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for class A computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

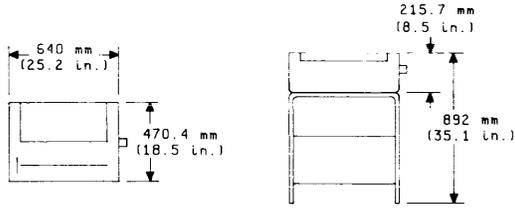
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### Customer Engineer

When HP installs the system, the CE (Customer Engineer) will contact the customer to schedule a date for system installation after the delivery date has been verified.

On the installation date, the CE will visually inspect all system components, install the system, and run diagnostic programs to verify system operation.

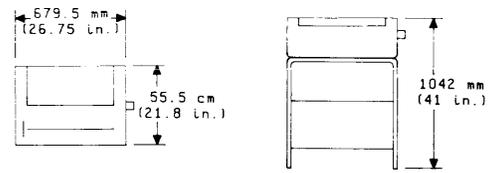
**1. HP Model 2631B Opt 046 Line Printer**



**Clearance Requirements**

- a. Front and Rear - Adequate for operator access.
- b. Side - 76 mm (3 in.)

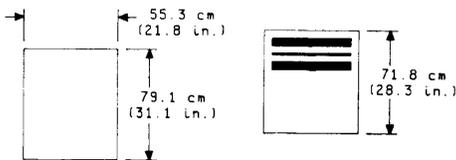
**2. HP Model 2608 Opt 046 Line Printer**



**Clearance Requirements**

- a. Front and Rear - Adequate for operator access.
- b. Left Side - 203 mm (8 in.) minimum.

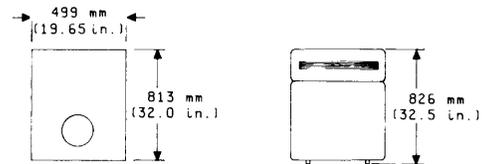
**3. HP Model 7906 Opt 102 Disc Drive**



**Clearance Requirements**

- a. Rear - 500 mm (20 in.) minimum from any object or barrier.

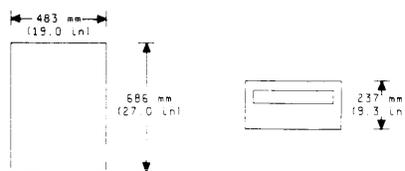
**4. HP Model 7920/7925 Opt 102 Disc Drive**



**Clearance Requirements**

- a. Rear - 500 mm (20 in.) minimum from any object or barrier.

**5. HP Model 7910H Disc Drive**



**Clearance Requirements**

- a. Rear - 500 mm (20 in.) minimum from any object or barrier.

**Figure 2-1. Space Requirements**

Clearance Requirements

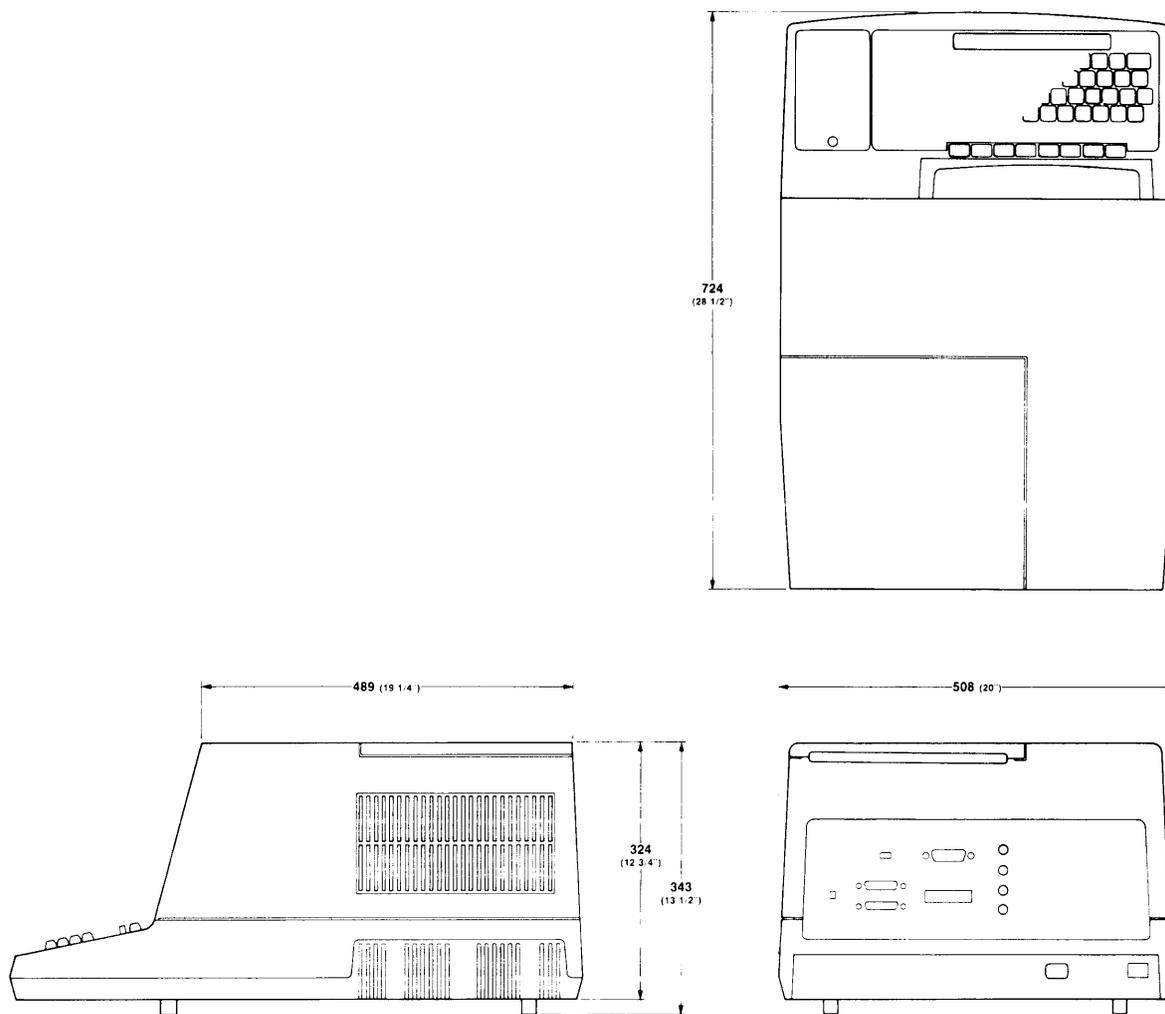
- a. Front and Rear - Adequate for operator access.
- b. Sides - 203 mm (8 in.) min.

**NOTE**

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Dimensions are in millimetres and (inches).

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**Figure 2-1. Space Requirements (Cont'd)**

**Table 2-1. Power and Environmental Requirements**

<b>Product</b>	<b>Maximum 120 V</b>	<b>Current 240 V</b>	<b>Maximum Heat Load</b>	<b>Weight</b>	<b>Power Cable</b>	<b>Bus Cable</b>
Model 64100A Mainframe _____ units	4.58 A	2.29 A	1661 BTU/hr 455 W	34.02 kg (75 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7906M Disc Drive (Opt 102) _____ units	8.15 A	4.08 A	2756 BTU/hr 755 W	154 kg (340 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7906S (Opt 102) Disc _____ units	5.45 A	2.73 A	1740 BTU/hr 510 W	138 kg (303 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7910H _____ units	2.27 A	1.22 A	920 BTU/hr 270 W	32 kg (70.6 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7920M (Opt 102) Disc Drive _____ units	8.45 A	4.23 A	2788 BTU/hr 817 W	159 kg (350 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7920S (Opt 102) Disc _____ units	5.8 A	2.9 A	1809 BTU/hr 530 W	143 kg (315 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7925M (Opt 102) Disc Drive _____ units	8.6 A	4.3 A	2901 BTU/hr 850 W	158 kg (350 lb)	2.2 m (7 ft)	2 m (6 ft)
Model 7925S (Opt 102) Disc _____ units	6.5 A	3.25 A	2014 BTU/hr 590 W	143 kg (315 lb)	2.2 m (7 ft)	2 m (6 ft)
2631B (Opt 046) Line Printer	2.2 A	1.1 A	901 BTU/hr 245 W	23 kg (51 lb)	2.2 m (7 ft)	2 m (6 ft)
Stand				24 kg (53 lb)		

**Table 2-1. Power and Environmental Requirements (Cont'd)**

Product	Maximum Current		Maximum Heat Load	Weight	Power Cable	Bus Cable
	120 V	240 V				
2608 (Opt 046) Line Printer	12.5 A	6.25 A	5120 BTU/hr 1500 W	97 kg (217 lb)	2.2 m (7 ft)	2 m (6 ft)
Total	_____ A	_____ A	_____ BTU/hr _____ W	_____ lb _____ kg		

**Environmental Operating Requirements**

Line Voltage	100/120/220/240V ~ +5%, -10% Single Phase
Line Frequency	47.5 - 66 Hz
Operating Temperature	10°C (50°F) to 40°C (104°F)
Operating Humidity	8% to 80% RH Noncondensing (max wet bulb temp - 26°C (78°F))

**Power Outlets**

US, Canada, Japan	NEMA 5-15 (15 A)
UK	BS 1363 (13 A)
Australia, New Zealand	AS C112 (7-5 A)
Europe (except UK and Switzerland)	CEE 7-V11 (10/16 A)
Switzerland	SEV 1011 (10 A)

**Power Requirements**

Table 2-2 lists power requirements for the various system components. Before connecting the system to the power source, verify that sufficient operating power is available.

**Table 2-2. Model 64000 Component Power Requirements**

<b>Development Stations</b>	
64100A	110/220 Vac +/-15%, 48-66 Hz, single phase; 455 W/4.58 A maximum at 120 Vac
<b>Line Printer</b>	
2631B (opt 046)	100/120/220/240 Vac, +/-10%, 48 to 62 Hz, single phase; 265 W/2.2 A maximum at 120 Vac
2608A (opt 046)	100/120/220/240 Vac, +5% -10%, 47.5 to 66 Hz, single phase; 1500 W/12.5 A maximum at 120 Vac
<b>Discs</b>	
7906M (opt 102)	100/120/220/240 Vac, +5% -10%, 47.5 to 66 Hz, single phase; 755 W/8.15 A maximum at 120 Vac
7910H	100/120/220/240 Vac, +5% -10%, 47.5 to 66 Hz, single phase; 272 W/2.27 A maximum at 120 Vac
7920 (opt 102)	100/120/220/240 Vac, +5% -10%, 47.5 to 66 Hz, single phase; 817 W/8.45 A maximum at 120 Vac
7925 (opt 102)	100/120/220/240 Vac, +5% -10%, 47.5 to 66 Hz, single phase; 635 W/5.15 A maximum at 120 Vac

## Configuring Power Options

Make sure each component in the system is configured for the correct voltage.

For Model 64100A:

- a. Set line selector to proper source voltage.
- b. Verify fuse rating for source. 110 V fuse should be 6 A.  
220 V fuse should be 3 A.

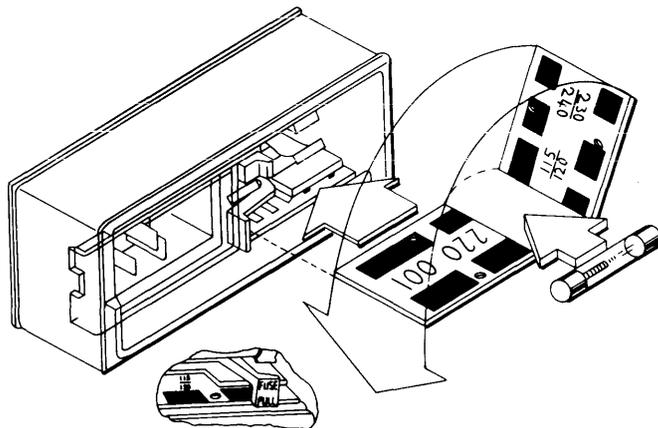
For Model 7910H:

- a. Set voltage select switch (on rear panel) for proper voltage.
- b. Verify that fuse rating is correct for selected voltage (indicated on rear panel).

For Model 2631B:

The receptacle for the power cord also contains a fuse and a printed circuit card (figure 2-2) that is used to select one of four line voltages. The proper voltage selection is normally done at the factory, but changes are easily accomplished by changing the position of the printed circuit card. If it becomes necessary to change the input supply voltage, do the following:

- a. Remove the power cable if it is installed.
- b. Slide the cover over the fuse into the area of the power cable connection.
- c. Move the fuse release lever and remove the fuse.
- d. Using a pointed tool, such as a scribe, remove the card by the small hole that is exposed near the outer edge.
- e. The card can be installed in four different ways as indicated by the voltages ranges; i.e., 100, 120, 220, and 240. Select the proper voltage and insert the card so the selected voltage can be read on the card when viewed from the rear of the unit.
- f. Reseat the fuse release lever and reinsert the 2.5A fuse.
- g. Slide the cover back over the fuse and card area; this exposes the cable connection.
- h. Connect power cable to the unit.



**Figure 2-2. Model 2631B Power Module**

### Determining System Power Requirements

For a minimum system, the requirements at 120V are determined as follows:

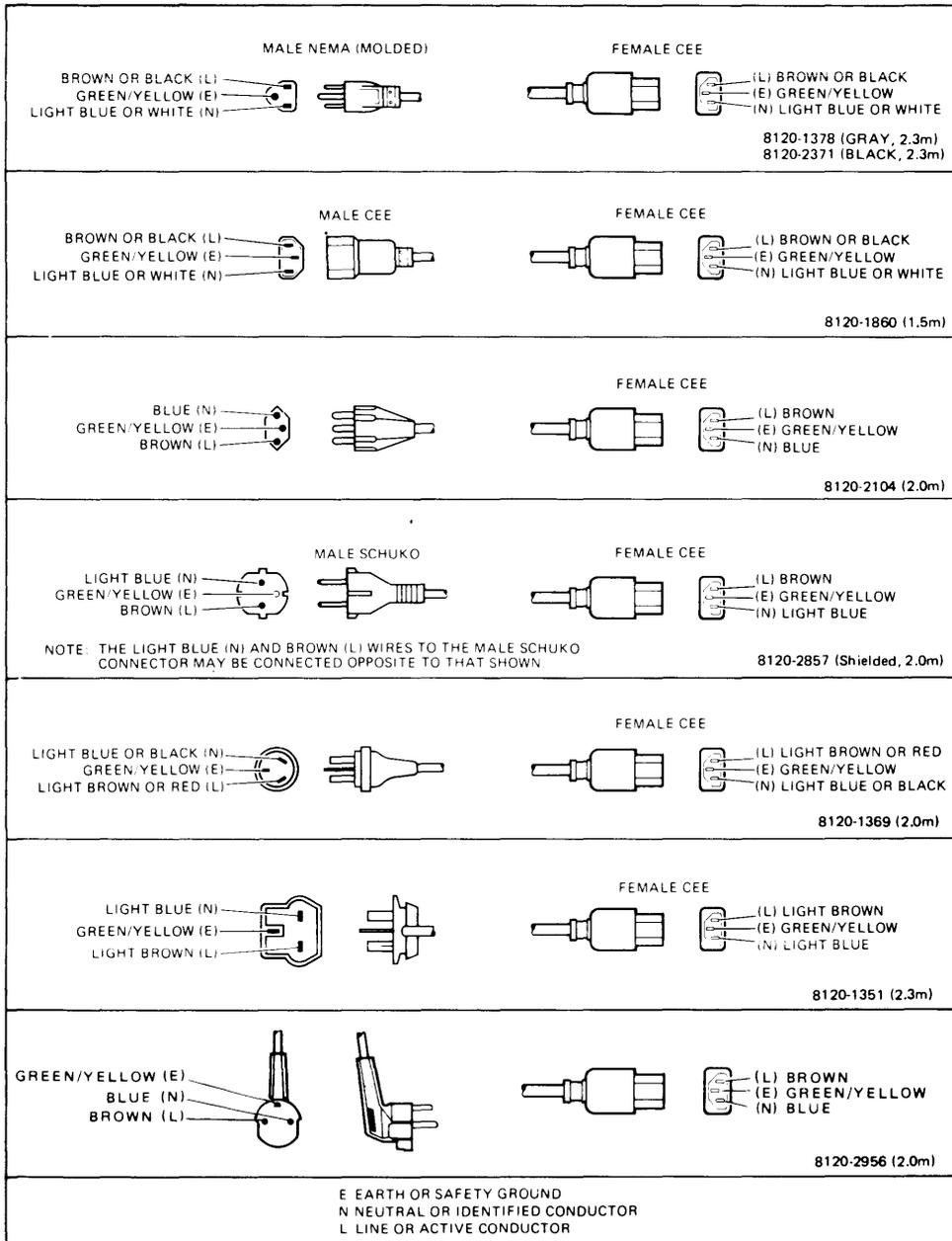
1 Model 64100A Development Station	4.58 Amp
1 Model 7910H Disc	2.27 Amp
1 Model 2631B Line Printer	2.30 Amp
	Total = 9.15 Amp

Expanded System Example:

6 Model 64100A Development Stations (6 x 4.58A)	27.48 Amp
1 Model 7920M Disc	8.45 Amp
1 Model 2608A Line Printer	12.50 Amp
	Total = 48.43 Amp

### Power Cords

Detachable power cords, with country-dependent plugs to match standard wall sockets, are supplied with each component. Figure 2-3 shows the available power plugs for various countries, ordering options, specification numbers, and HP part numbers. The green-wire ground connection on each power plug is also shown.



REF 7311-1D

Figure 2-3. Power Cord Sets

**WARNING**

Do not use extension power cords under any circumstances.

## Grounding

Model 64000 component are equipped with three-conductor power cords which, when connected to appropriate power receptacles, ground the system. The green-wire safety ground is connected to the metal frame of each component in the system to provide a return path for fault currents due to equipment malfunction or external faults such as lightning strikes. Do not operate the system from an ac power outlet which has no ground connection. Be sure there is a green-wire ground from the power outlet to the distribution panel where the circuit breaker is installed.

### NOTE

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To ensure good communications over the system bus, all power sources must be at the same ground potential.

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## Convenience Outlets

Power outlets for janitorial maintenance (vacuum cleaners, floor buffers, etc.) must be wired on a separate circuit breaker from the Model 64000. If these precautions are not taken, operation of janitorial equipment will induce noise transients on the system power lines, which can cause abnormal operation of the system.

## Isolation Transformers

Switching heavy electrical machinery loads or operating certain types of equipment near the system can cause problems, even though the source is on a different circuit breaker. In some cases, it is mandatory to provide a separate circuit and circuit breaker for the system directly from the main building power. In extreme cases of severe electrical noise, it may be necessary to install an isolation transformer.

## **Power Line Noise**

Power from a typical ac power line is inherently noisy, and fluctuations can be caused by:

- a. utility power company switching
- b. circuit breakers tripping
- c. air conditioning equipment
- d. electrical welders
- e. elevators
- f. copying machines
- g. start-up of large electric motors.

Even though you cannot control or prevent disruptions from the first two items, remember to avoid connecting Model 64000 components on the same circuit breaker with any of the other named equipment.

## **Telephone**

A telephone should be located near the system so that a customer or CE can discuss a servicing problem while working on the unit.

## Ordering and Shipping

### Carrier Selection

The Model 64000 is sold F.O.B. origin, so you can choose the type of carrier for hauling and delivery. There are three different methods for shipping Model 64000 components. They are: 1) electronic padded van, 2) Air Consolidation Program (ACP), and 3) common carrier (truck). Any of the methods are available within the continental U.S.A. and Canada. All international shipments use ACP. For all shipments, HP selects the carrier company for your specific choice of conveyance. Advantages and disadvantages of the three shipping methods are as follows:

	<b>Advantages</b>	<b>Disadvantages</b>
1. Electronic Padded Van	Carrier will place the system on site at the exact spot designated by the customer. No crate required. Least susceptible to shipping damage. Short shipping time.	Cost slightly higher than Air Consolidation Program
2. Air Consolidation Program (used for all International shipments)	Fastest shipping method	System is delivered to customer dock but not the actual installation site. Customer must uncrate the system.
3. Common Carrier	Lowest cost to customer	Longer shipping time than other methods. Most susceptible to shipping damage. System is delivered to customer dock but not the actual installation site.

## Arrival of Coordinated Shipments

All Model 64000 components will be delivered on a drop-ship basis. The normal time span for delivery of all system components is a maximum of two weeks.

If you do not receive a complete shipment of your purchase order within two weeks of the first delivery, you should notify the CE so that proper action can be taken for completing delivery.

## Receiving the Model 64000

### NOTE

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Hewlett-Packard personnel are not authorized to accept or sign for deliveries of Hewlett-Packard equipment for the customer. Accepting deliveries is the responsibility of the customer.

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You have the responsibility to place the system on site, unpack, and dispose of any packing material.

## Inspecting the Shipment

The main components (Model 64100A Development Stations, Model 7910H Disc, and Model 2631B Printer) of the Model 64000 Logic Development System arrive in separate cartons from different Hewlett-Packard divisions.

**NOTE**

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Disc Models 7906, 7920, and 7925 require unique installation procedures that must be performed by an HP Service Representative.

---

Before unpacking the system, it is extremely important that you verify the packing list for any discrepancies, and visually inspect the shipment for damage.

Verify the packing list as follows:

Only one packing list is attached to each shipment, in an envelope on the outside of one of the cartons. If there are missing items when checked against the packing list, you must notify the carrier immediately for determination of those items.

**Inspecting for Shipping Damage**

Before unpacking the system, you should visually inspect all shipping crates and boxes for damage.

If there is external damage to the Model 64000 component case as a result of mishandling during shipment (damaged crates, stains, etc.), the carrier is liable for repair and/or replacement of any parts. The customer should also immediately open all cabinets and make a visual inspection of all internal parts. If there is internal damage, the carrier is also liable for repair and/or replacement of those parts.

Internal damage (within a cabinet) may be discovered after the shipment has been unpacked. On the premise that there was no damage to the shipping container, HP is liable for repair and/or replacement of any parts. You must notify the local HP Customer Engineer so the part can be replaced immediately under warranty.



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The Model 64100A weighs 34.02 kg (75 lb), the Model 7910H weighs 32 kg (71 lb), and the Model 2631B (with stand) weighs 47 kg (104 lb). Two persons are required to lift these units from the shipping containers.

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## Unpacking the Model 64000 Components

When unpacking the units, retain all packing materials and hardware for future use. Remove the units from the shipping carton and the packing material.

After unpacking all units, verify that serial numbers listed on shipping documents and identification tags (located on the backs of the units) agree.

If for any reason, it becomes necessary to reship one of the units, repack it in the original packing material and shipping carton.

### NOTE

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The stand for the Model 2631B requires assembly instructions located in the documentation package for the line printer.

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## Support Documentation

Besides the system manuals (see Manual Map, page i), each component part of the Model 64000 is supported by a series of installation, operating, and service support manuals as listed in table 2-3.

**Table 2-3. Support Manuals**

<b>Model</b>	<b>Manual</b>
HP Model 64100A Development Station	HP 64100A Service Manual
HP Model 7906 Disc Drive	HP 7906 Disc Drive User's Manual HP 7906 Disc Drive Installation Manual
HP Model 7910 Disc Drive	HP 7910 Disc Drive Installation Manual HP 7910 Disc Drive Service Manual
HP Model 7920 Disc Drive	HP 7920 Disc Drive User's Manual Installation Manual
HP Model 7925 Disc Drive	HP 7925 Disc Drive User's Manual HP 7925 Disc Drive Installation Manual
HP Model 2631B Line Printer	HP 2631B Printer Operator's Manual Reference Manual for 2610 Family
HP Model 2608 Line Printer	HP 2608A Operator's Manual HP 2608A Service Manual
HP Model 13037C Controller (Not required with 7910H Disc Drive)	HP 13037C Installation and Service Manual
HP Model 12745A HP-IB Disc Controller to HP-IB Adapter Kit (Not required with 7910H Disc Drive)	HP 12745A Installation and Service Manual
HP Model 29425 Disc Cabinet (for 7906M only)	HP 29425 Disc Cabinet Installation and Service Manual

## Boot-Up

There are four methods of booting up the Model 64100A Development Station. The position of the boot-up switch (located on the rear panel) determines the function of the system control source. This switch function is the two left-most bits of the switch under the label SYSTEM CONTROL SOURCE.

Figure 2-4 shows the rear panel system control source. Refer to table 2-4 for boot-up switch positions.

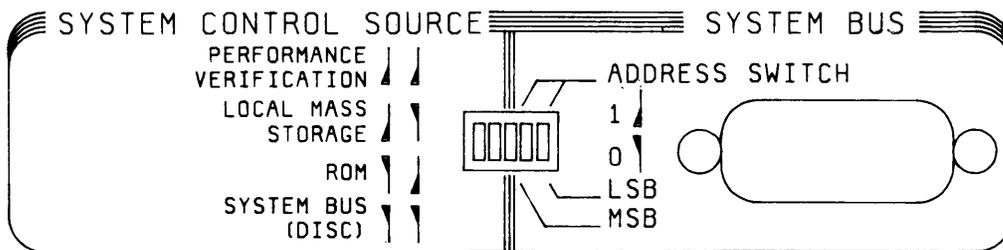


Figure 2-4. System Control Source

Table 2-4. System Control Source Switch Settings

Bit Position	Value	Function	Resulting Action
1 1	11	PERFORMANCE VERIFICATION	In this mode, an internal self check is run on the Model 64100A Development Station.
1 0	10	LOCAL MASS STORAGE	In this mode, the Model 64100A is set to load the operating system (software) from the minicartridge to the disc.
0 1	01	ROM	Reserved for future use.
0 0	00	SYSTEM BUS	After the operating system has been loaded on the disc, the Model 64100A must be set to this mode for normal operation.

## Software Updating Procedure

This procedure should be used to update system software after user-generated files have been stored on the disc. The following procedure eliminates disc reformatting and performance verification, which is assumed to be unnecessary.

---

**CAUTION**

---

---

To ensure that user-generated files are not accidentally destroyed (by reformatting the disc), they should be backed up on tape cartridge.

---

---

**CAUTION**

---

---

This caution note applies only to systems with Model 7906 Disc Drives: See figure 2-21. You must determine whether your disc is formatted as an "entire" logical unit (LU) or as two logical units. Figure 2-21 shows a display indicating LU=0 for an "entire" logical unit. For discs formatted as two logical units, the display will indicate LU=0, LU=1. (This display can be generated by cycling the power at any station off and back on.)

---

### Procedure:

---

**NOTE**

---

---

This procedure must be run on the master controller; all other stations must be powered off.

---

- a. Set System Control Source switches to LOCAL MASS STORAGE (10).
- b. Check contents of Software Update Kit (supplied by HP). If the kit does not contain an Operating System Tape, omit steps e thru g.

- c. Insert Operating System (or other) tape in front-panel tape drive slot of the master controller development station.
- d. With development system power on, hold SHIFT key down and press RESET key once. Tape light should come on and display should indicate BOOT IN PROGRESS; if not, cycle station power off and back on.

**NOTE**

---

Step e applies only to systems with a Model 7906 Disc Drive. It must be determined whether the 7906 is formatted for one or two LU's.

---

- e. On systems with a Model 7906 Disc Drive, display should be as shown in figure 2-19. If 7906 is formatted as LU=0, LU=1, press soft key labeled "upper"; otherwise, press "entire".
- f. The soft key label line will appear as follows:



- g. Press **tst & fmt**.
- h. For all systems, select soft-key answers to the following questions as they are displayed sequentially on the screen:

Question: TEST TIME IN MINUTES?  
 Answer: no test.




---

For the next question, do not press the "yes" soft key unless you wish to reformat the disc. To do so will destroy all files currently on the disc and will reformat the disc.

---

Question: DO YOU WANT TO FORMAT?  
 Answer: no

Question: DO YOU WANT TO LOAD THE SYSTEM SOFTWARE  
 CONTAINED ON THIS TAPE CARTRIDGE?  
 Answer: yes

**NOTE**

---

When tape load is complete, system "software load complete" message should be displayed on the screen.

---

- g. Insert other tape (if provided) in tape drive; tape should begin booting automatically and **BOOT IN PROGRESS** message should appear on screen. (Repeat this step for each additional tape.)
- h. When all tape loading is complete, remove tape cartridge and reset System Control Source Switches to 00, **SYSTEM BUS (DISC)**; normal operation is now automatically resumed.

**NOTE**

---

For format, test, soft fix, or hard fix options, refer to the System Overview Service Manual.

---

## Performance Verification

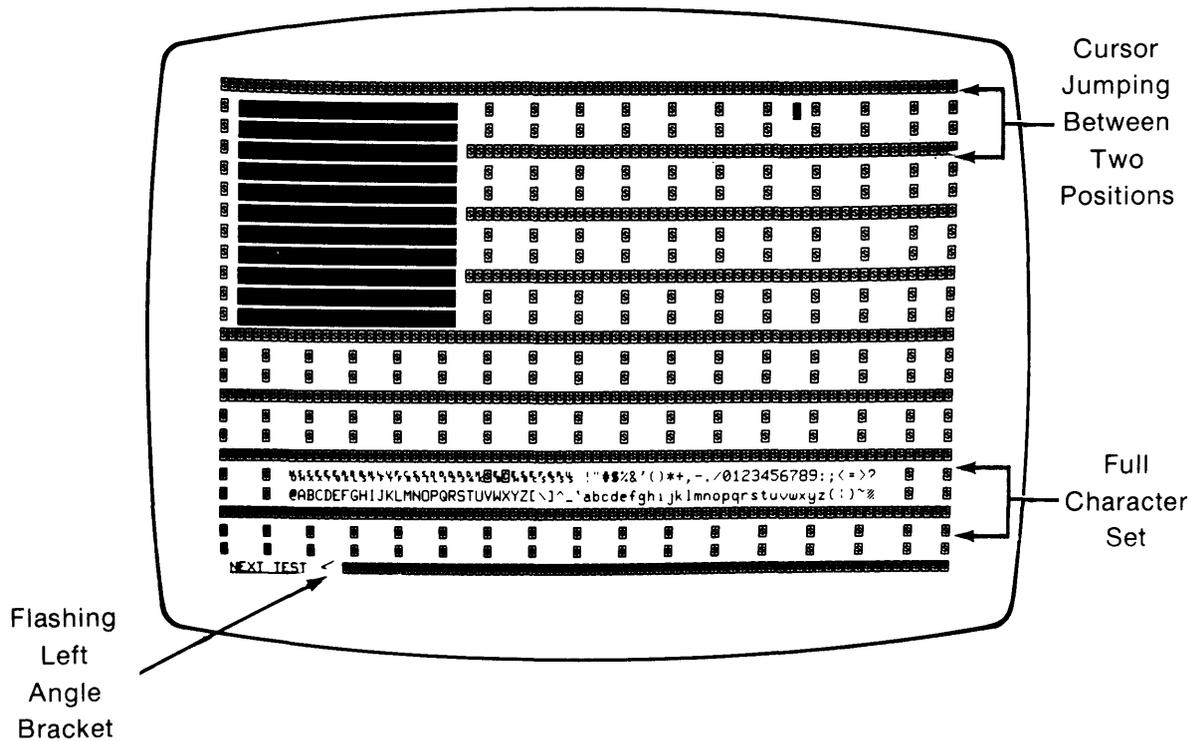
### Development Station

Set **SYSTEM CONTROL SOURCE** switches (located on rear panel) to **PERFORMANCE VERIFICATION (11)**. Turn the development station power ON. There will be a loud beep the instant that power is switched on. This will quickly be followed by another beep and, if the display is warmed up, a random series of characters in the upper-left corner of the display. The random characters will remain approximately 1/2 second after which a second beep will be heard and a display pattern as shown in figure 2-5 will be visible.

The first beep signals the successful completion of the Short ROM Test which ensures that enough of the ROM code is working to enable the use of the Long ROM Test's diagnostic capability. This is accomplished by doing a partial checksum of the ROM code. If the checksum is good, the Performance Verification proceeds to the Short RAM Test; otherwise, the Short ROM Test loops.

The second beep signals the successful completion of the Short RAM Test which reads ROM data and writes this information to RAM addresses. This includes some general memory locations and all display and basepage locations. The test then waits one second to verify the RAM's refresh and XOR's the ROM and RAM data. At the same time the ROM data is read again, complemented, and stored in RAM. After another one-second delay, the RAM data is XOR'd with complemented ROM data. If ROM and RAM data are identical, the XORs will result in all zeros and the test will pass. Any difference between ROM and RAM data gives a nonzero result which causes the test to repeat. Random data should be visible in the upper-left corner of the display during this test.

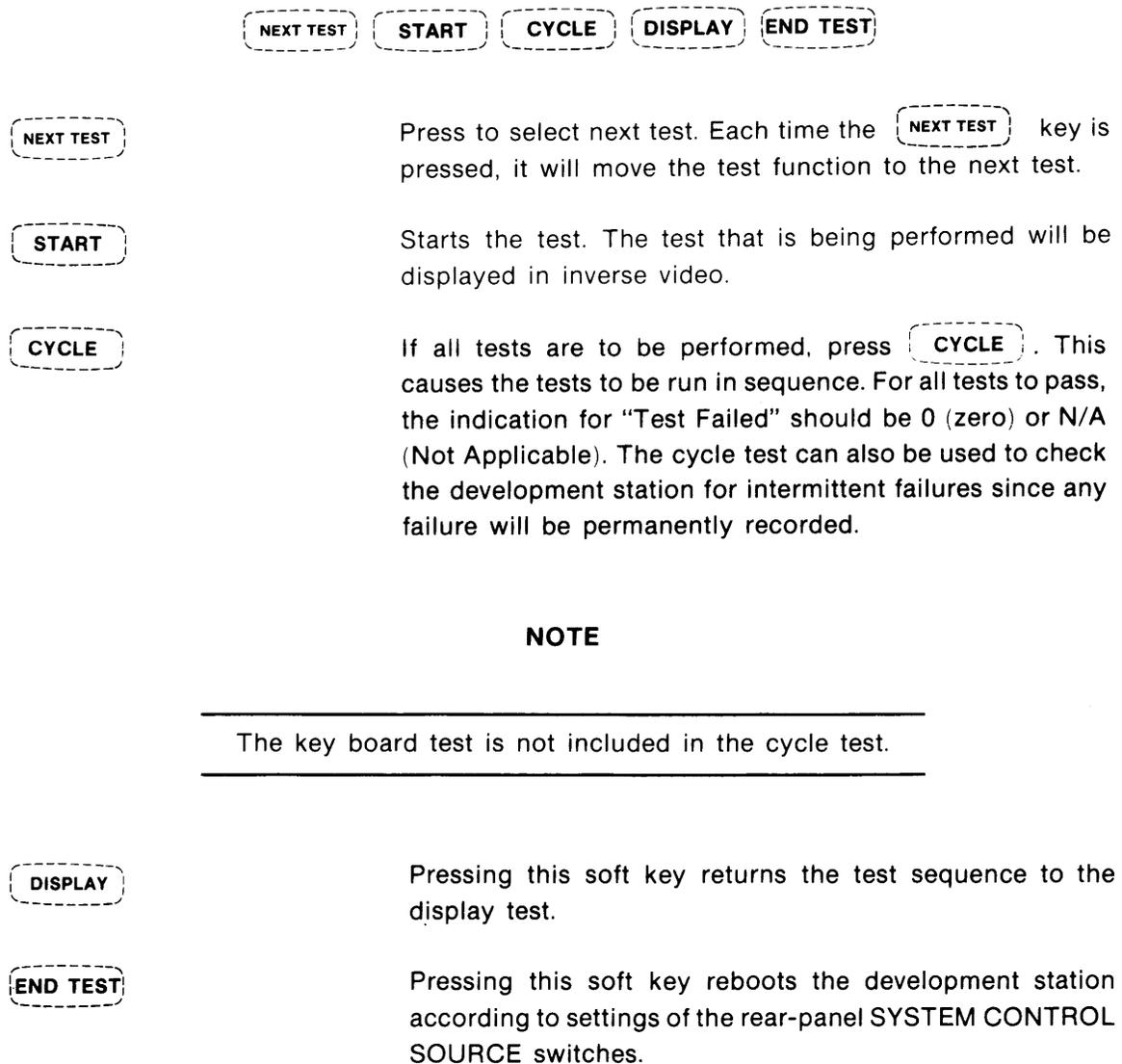
Figures 2-5 through 2-15 explain each step in the Performance Verification. This is valid whether tests are conducted in single-step fashion or on a cycle basis. If a test is displayed in inverse video, then that is the test in progress.



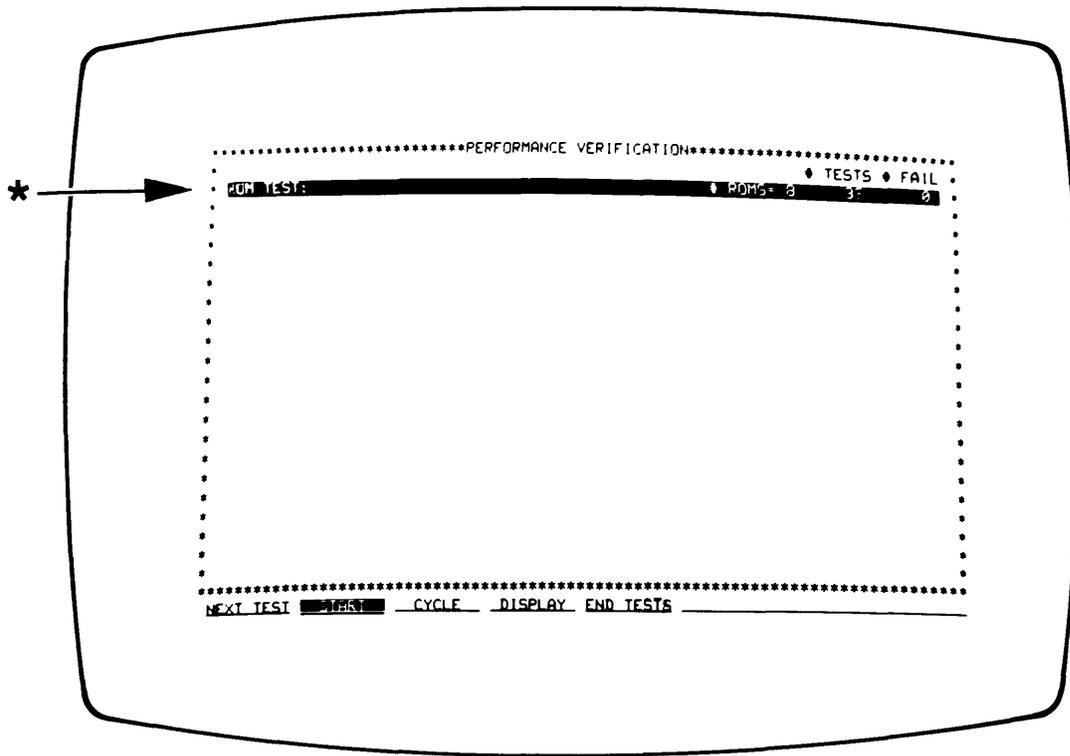
**Purpose:** Displays a standard pattern that contains all possible characters. The test is repetitive and does not indicate the number of passes or the number of failures. The presence of all characters (no blanks in character lines) indicates proper operation of the display circuits. The presence of the cursor jumping back and forth indicates the ability of the CPU to write to the display RAM. The blinking character indicates correct operation of the blinking function. If a character is missing, if the cursor is not jumping back and forth between indicated points, or if the blinking function is not working, refer to the service manual.

**Figure 2-5. Display Test**

After the display test is verified, press **NEXT TEST**. The soft keys are relabeled to those shown in figure 2-6.



**Figure 2-6. Performance Verification**



Purpose: Verifies ROM operation. This test compares the checksum of each ROM to its expected value. If all checksums are correct, the test will pass. In order to keep uninstalled ROMs from being displayed, the test routine ignores the test result if checksums of the upper and lower byte of a ROM pair are zero. Since a hardware problem could cause this same result, the number of ROMs detected with a nonzero checksum is displayed.

**Figure 2-7. ROM Test**

```

*****PERFORMANCE VERIFICATION*****
*
* ROM TEST:                               # ROMS= 8      # TESTS # FAIL *
*
* RAM TEST:  BIT ERROR MASK:  UPPER-BANK=0000, LOWER-BANK=0020      1      1 *
*
* I/O WRITE TEST:                          1      N/A *
*
*   READ TEST:                              1      N/A *
*
*   TIME INTERRUPT TEST:                    1      0 *
*
*   KYBD TEST:                              0      0 *
*
*   SYS BUS TEST:                           1      0 *
*
*   RS232 TEST:                              1      0 *
*
* TAPE SYSTEM TEST                          0      0 *
* WIND REW0 WRT0 REW1 WRT1 REW0 RED0 RED0 REW1 FIND RED1
*
*
*
*****
NEXT TEST  START  CYCLE  DISPLAY  END TESTS

```

**NOTE**

---

Duration of this test is approximately eight seconds.

---

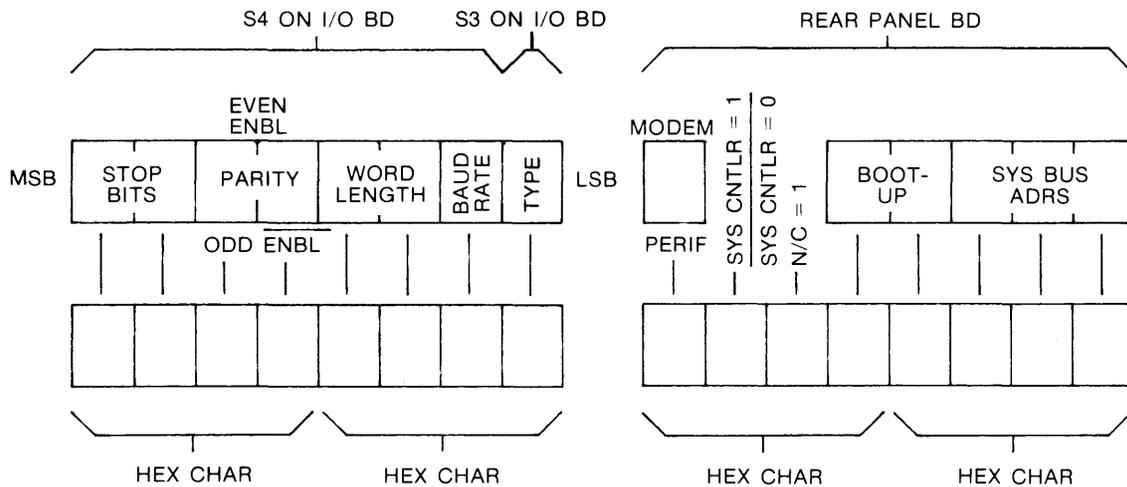
Purpose: Verifies RAM operation. The test is divided into two steps. The first step reads the contents of the primary ROM and then stores the data in RAM (that portion not checked during the short RAM test). The RAM is read and compared to ROM just as in the Short RAM Test. The second step rechecks RAM previously checked in the Short RAM Test. This time, however, part of the RAM contains display information which must be read before the test and restored after the test. The test itself consists of writing walking 1's and 0's patterns to each RAM address and reading them back again. The walking 1's and 0's are visible on the CRT as a blinking pattern with characters moving to the bottom of the CRT. If the test fails, refer to the service manual.

**Figure 2-8. RAM Test**

The I/O Test checks the following I/O functions:

I/O WRITE - operates the beeper and other write functions.

I/O READ - reads the status of S4 on the I/O Board and the rear-panel board switches.



I/O Interrupt - checks processing of the line frequency interrupt.

I/O Keyboard - operator input to verify functional operations of all keys.

I/O System Bus - verifies system bus circuitry.

I/O RS-232 - verifies serial communications circuitry.

Tape Test - verifies operation of tape drive unit.

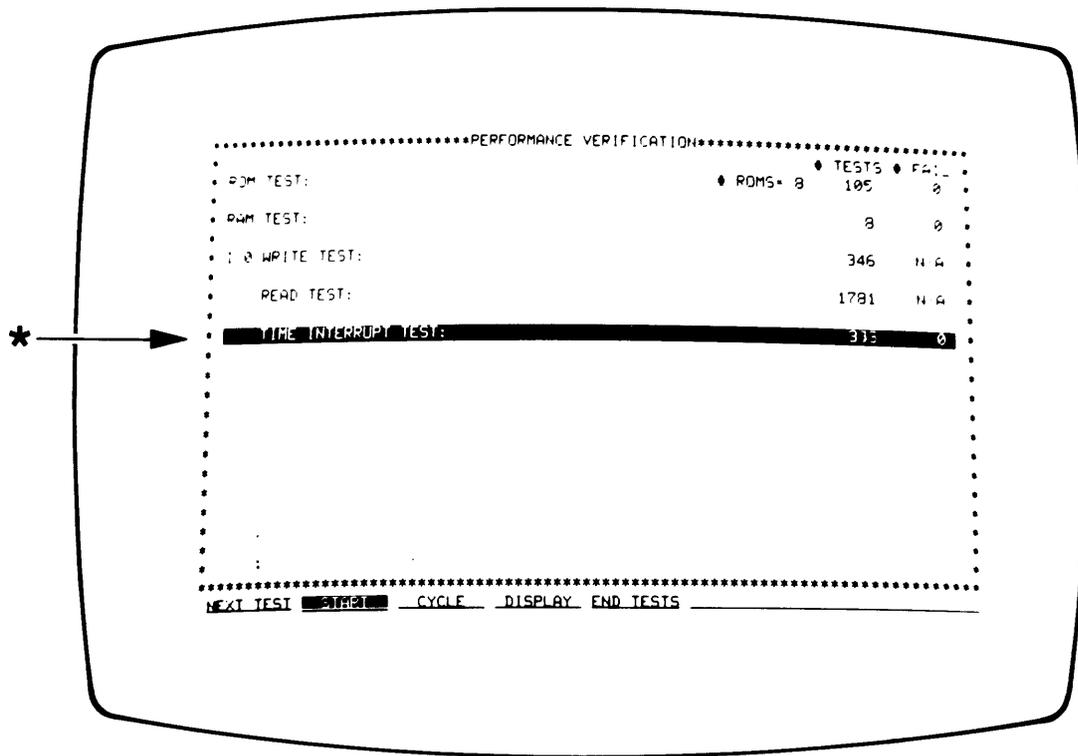
You must recognize the failures for the I/O WRITE and I/O READ Test. Each time the I/O WRITE Test is performed the beeper sounds. Each time the I/O READ Test is performed you must be able to verify that the hex characters shown correspond to the actual switch settings on the I/O Board. (See figure 2-35 and tables 2-11 through 2-13 for I/O board information.)

**Figure 2-9. I/O Tests**

```
*****PERFORMANCE VERIFICATION*****
*
* ROM TEST:                                # ROMS= 8    # TESTS # FAIL *
*
* RAM TEST:                                3          0      *
*
* I/O WRITE TEST:                          1          N/A   *
*
* READ TEST:  I/O BD S4 = FF, R. PANEL = 78 205      N/A   *
*
* TIME INTERRUPT TEST:                      2          0      *
*
* KYBD TEST:                                0          0      *
*
* SYS BUS TEST:                             2          0      *
*
* RS232 TEST:                               2          0      *
*
* TAPE SYSTEM TEST                          2          0      *
* WIND REW0 WRT0 REW1 WRT1 REW0 RED0 RED0 REW1 FIND RED1
*
*
*
*****
NEXT TEST        CYCLE        DISPLAY        END TESTS       
```

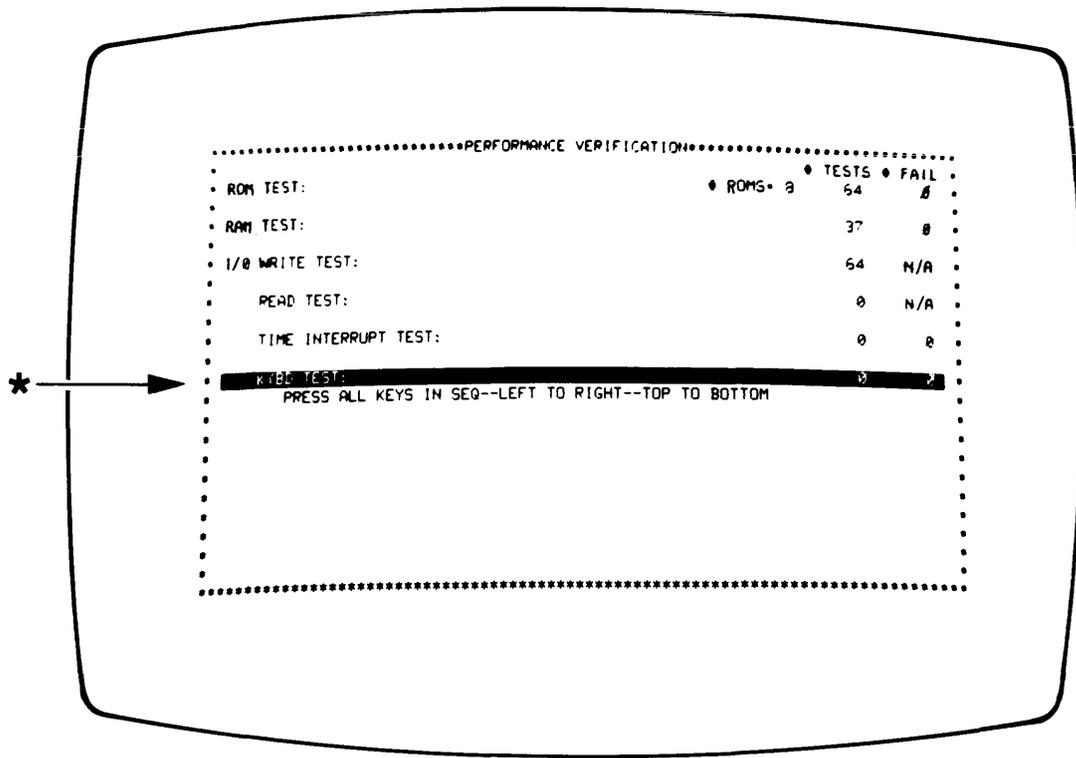
The I/O READ test displays the status (in hex) of I/O switch S4 and the rear-panel switches.

Figure 2-10. I/O Read Test



The power line sync signal is used to interrupt the CPU so that it can keep track of time. This test verifies that an internal signal causes this interrupt at a rate of 48 to 62 Hz and that the CPU can correctly read and respond to the interrupt.

Figure 2-11. I/O Time Interrupt Test



Purpose: This test verifies functional operation of all front-panel keys. Press **NEXT TEST** until KYBD TEST is in inverse video. Press the keys in sequence as shown in figure 2-12 (sheet 2 of 2). If a key is pressed out of sequence or if two keys are pressed at the same time, a "TEST FAILED" message will be displayed on the CRT. If the keys are pressed in sequence and all pass, a "TEST PASSED" message will be displayed on the CRT. If a true keyboard failure is encountered, refer to the service manual.

**Figure 2-12. I/O Keyboard Test  
(Sheet 1 of 2)**

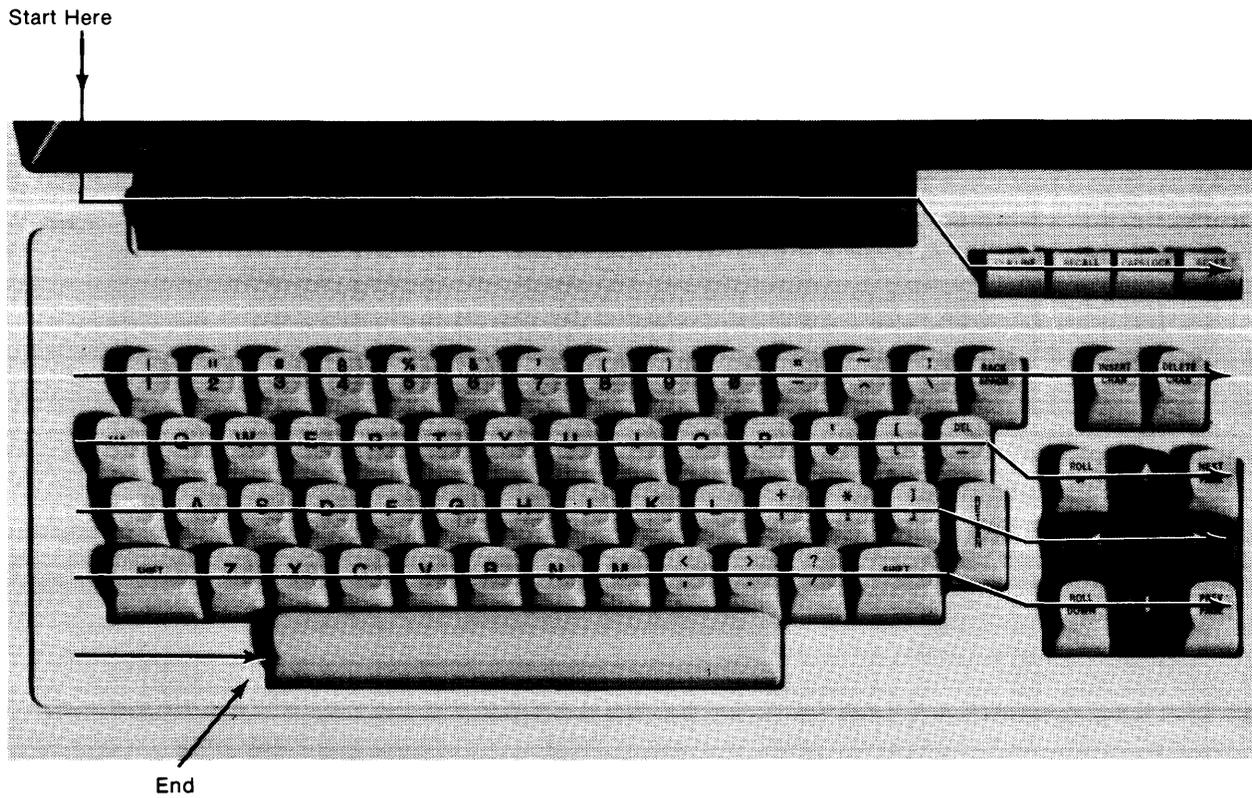
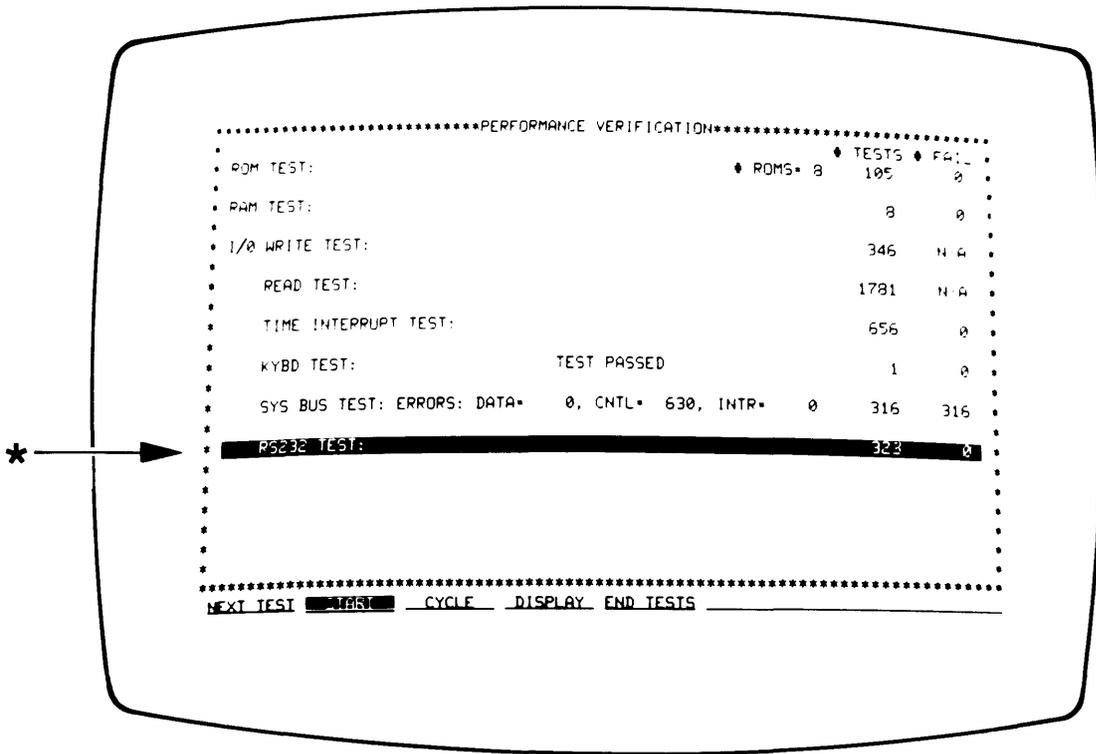


Figure 2-12. I/O Keyboard Test (Sheet 2 of 2)





**NOTE**

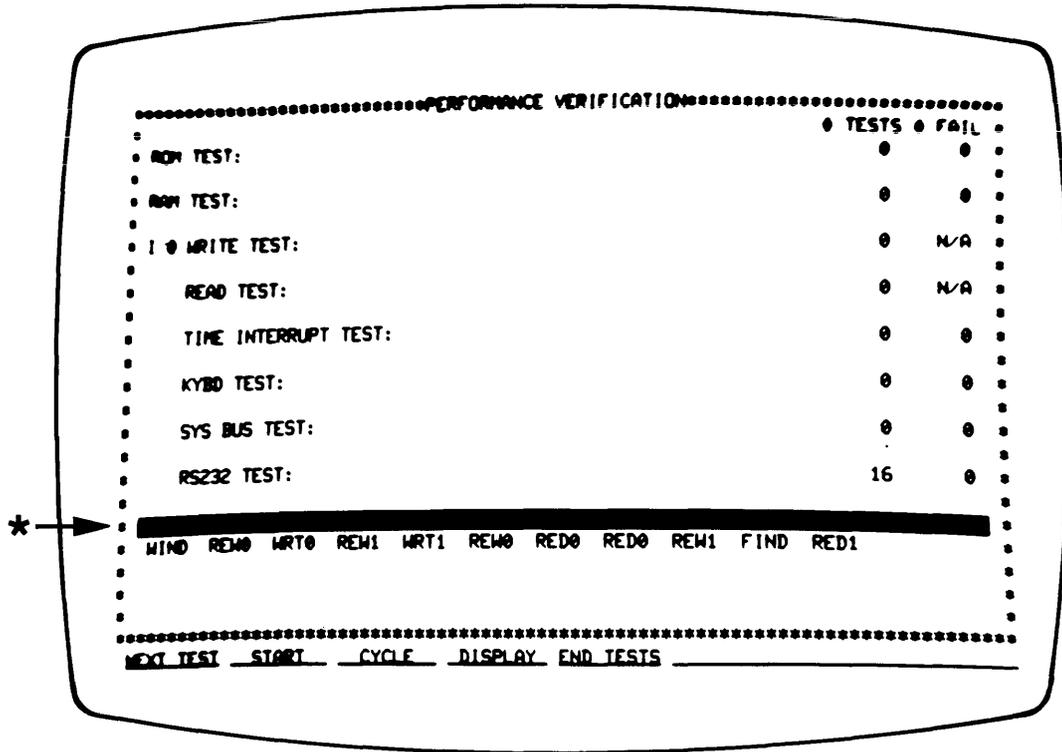
---

Bit 1 of S5 (see figure 2-35) must be set to the 0 (half-duplex) position or the RS-232 test will fail. These failures are identified as CNTL failures.

---

Purpose: Verifies operation of USART and associated I/O circuitry. If a failure occurs, refer to the service manual.

**Figure 2-14. I/O RS232 Test**



**NOTE**

---

Install new blank minicartridge at start of test.

---

Purpose: Verifies operation of all tape functions. Install a blank minicartridge (not write protected) in the tape drive unit. The test will automatically step through the sequence. If a tape error occurs, refer to Chapter 10.

**Figure 2-15. Tape System Test**

After the development station has passed the performance verification, determine if it is going to be the master controller or slave controller (see figure 2-24). Set one station to master controller. Set SYSTEM CONTROL SOURCE switches to LOCAL MASS STORAGE. Set SYSTEM BUS switches to "2". Connect the system bus cable between the disc and master controller development station. Turn the development station power off.

## Disc Performance Verification

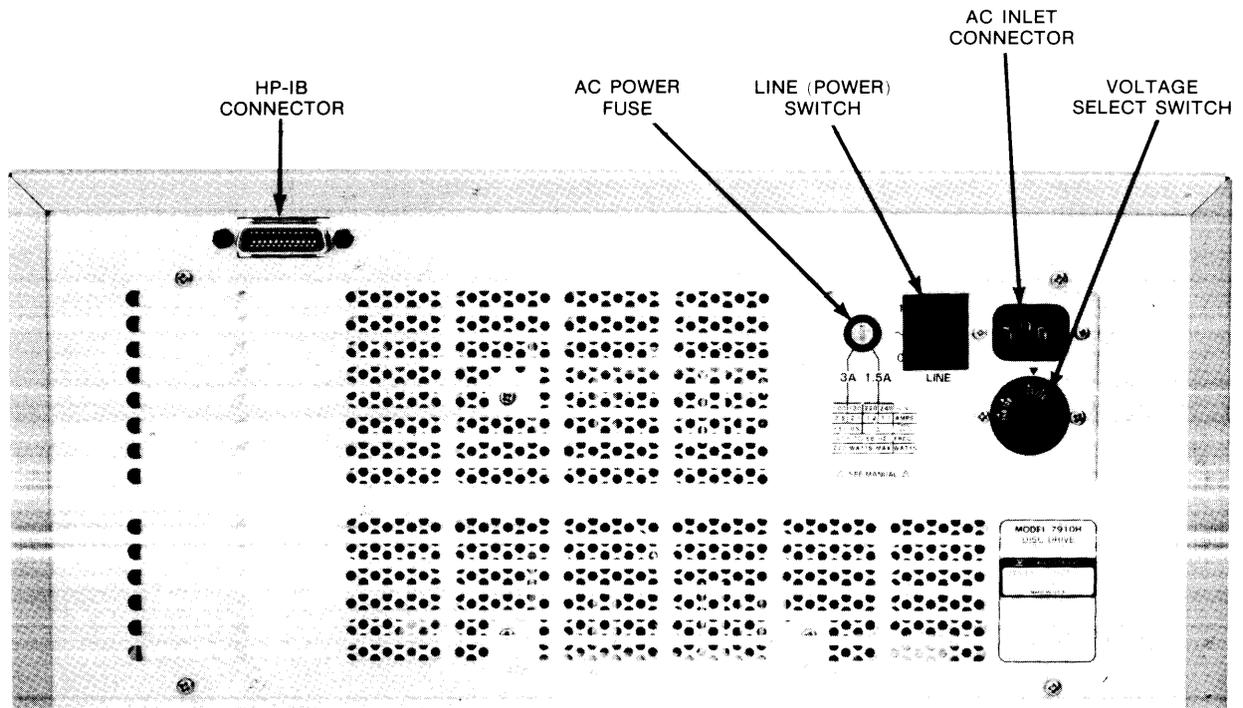
### NOTE

---

Disc performance verification and system load can only be accomplished from a development station set as master controller and with a tape drive unit.

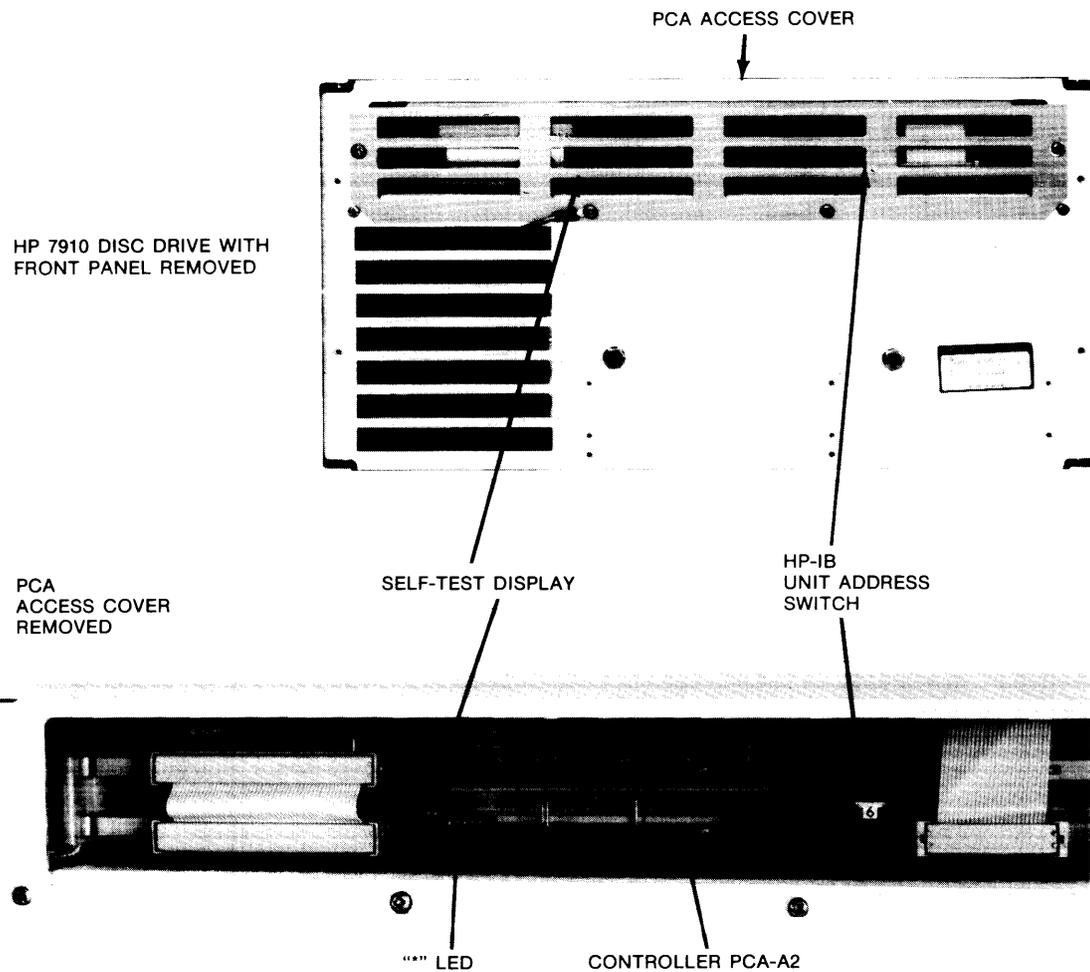
---

Verify that 7910H Voltage Select switch is set for the correct line voltage. Connect one end of the system bus cable to the HP-IB Connector on the rear panel (see figure 2-16). Pull and lift 7910H front panel (see figure 2-17). Remove PCA access cover (by removing four knurled screws). Set HP-IB Unit Address Switch to 0, then replace PCA access cover. Set rear-panel power (LINE) switch to on.



HP 7910H DISC DRIVE

Figure 2-16. 7910H Rear Panel Control Locations



**Figure 2-17. 7910H HP-IB Unit Address Switch Location**

Allow approximately 30 to 60 seconds for the disc to come up to operating speed and complete self test.

During self test, the 10 LED's located on the 7910H Controller Board (front panel) will be flashing. When self test is complete, all the LED's on the Controller Board should be off except for the self-test LED (\*) which should remain on until a disc access is performed. If LED's indicate otherwise, refer to the 7910H Service Manual.

Connect the system bus cable to the master controller development station. Leave boot-up switches in LOCAL MASS STORAGE position. Turn station power on.

The development station CRT will display the message:

BOOT IN PROGRESS

WAITING FOR CARTRIDGE

Install the HP 64800 system tape into the tape transport as shown in figure 2-18.

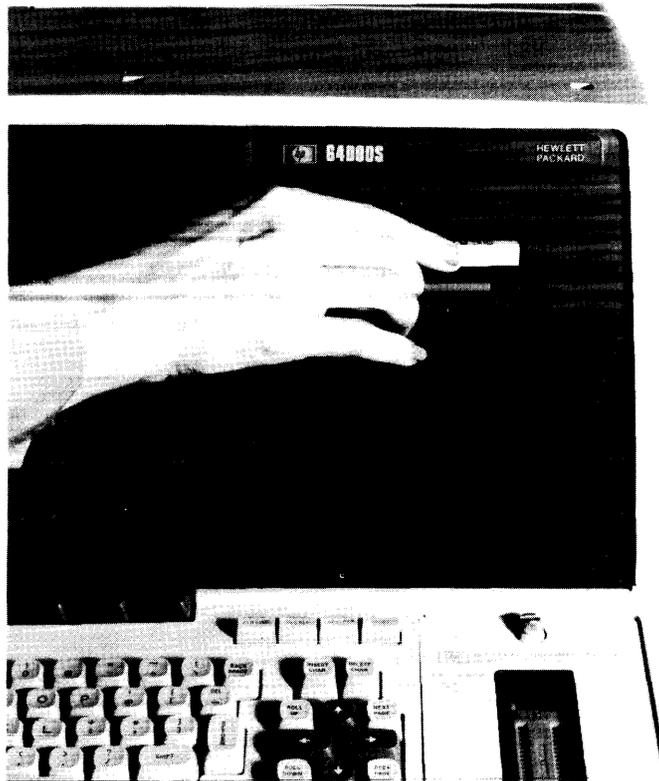
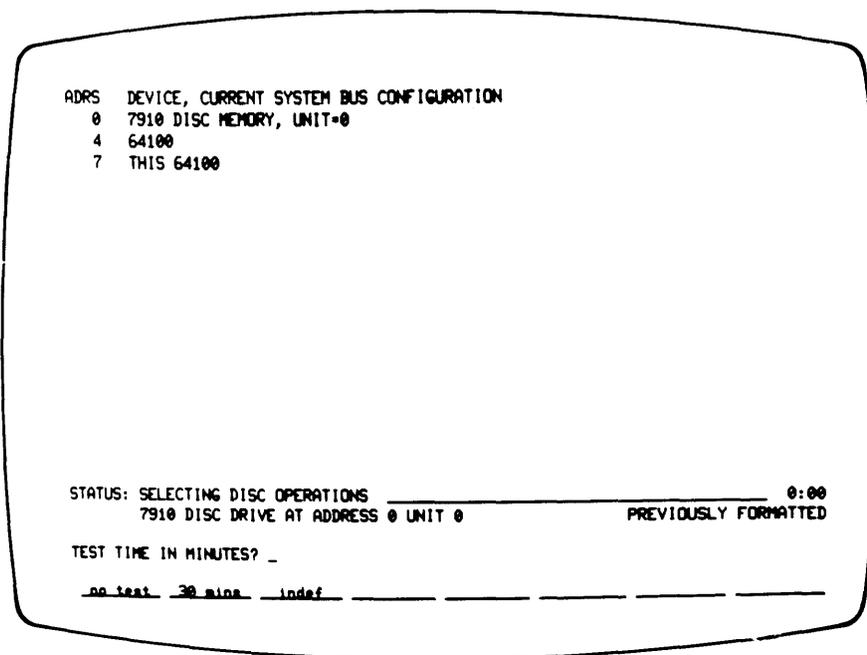


Figure 2-18. System Tape Installation

The tape transport light will come on and the transport can be heard moving.

After several moments the display will appear as shown in figure 2-19.



**Figure 2-19. Initial Disc Verification Display**

Note that the message on the bottom of the screen will say "NOT PREVIOUSLY FORMATTED." Discs that have been initialized for the Model 64000 will indicate "PREVIOUSLY FORMATTED."

The soft keys now indicate the total number of minutes for the test. The standard test time is 30 minutes. Press **30 min** and then **RETURN**

The following question will appear on the screen:

DO YOU WANT TO FORMAT?

**CAUTION**

---

If the disc has been previously formatted, a flashing inverse video WARNING will be displayed. This warning states that FORMATTING causes the permanent loss of all information stored in disc memory.

---

If you do not wish to format, press no, and proceed to Line Printer Performance Verification.

If you press yes, the system will now format all disc tracks indicating the number of defective tracks found. Next, the display changes (see figure 2-20) and shows the minutes of testing, megabytes verified, disc errors (if any), megabytes of I/O, transmit or receive errors, the number of timed seeks, and seek errors (if any). Upon completion of testing, the system writes a file directory and builds a free list of available pages for future file storage.

```

MINUTES OF TESTING---- 5
                    LIMIT= 10

MEGABYTES VERIFIED-- 26
                    DISC ERRORS= 0

MEGABYTES OF I/O----- 1
                    TRANSMIT ERRORS= 0
                    RECEIVE ERRORS= 0

TIMED SEEKS----- 166
                    SEEK ERRORS= 0

1 DEFECTIVE TRACKS

STATUS: TESTING _____ 0:17
        7910 DISC DRIVE AT ADDRESS 0 UNIT 0 PREVIOUSLY FORMATTED

end_test _abort_ new_limit _____

```

Figure 2-20. Disc Verification Display

Disc errors, transmit/receive errors, and seek errors should all indicate 0. If the number is not 0, contact the appropriate service personnel.

After the testing is complete, any tracks which tested as bad two or more times will be marked to a DEFECTIVE status. Regardless of whether any tracks are found defective, the following messages will appear in sequence on the status lines:

Writing Directory  
Building Free List

After the free list is built, the disc is completely initialized. System software files residing on the 64800 tape are now automatically loaded onto the disc memory.

After all files on the 64800 tape cartridge are loaded, the CRT display will say that system software load is complete. At this time, insert any additional software tapes to be stored on the disc.

When all software is loaded, set the development station SYSTEM CONTROL SOURCE switches to SYSTEM BUS. The CRT display should be as shown in figure 2-21.

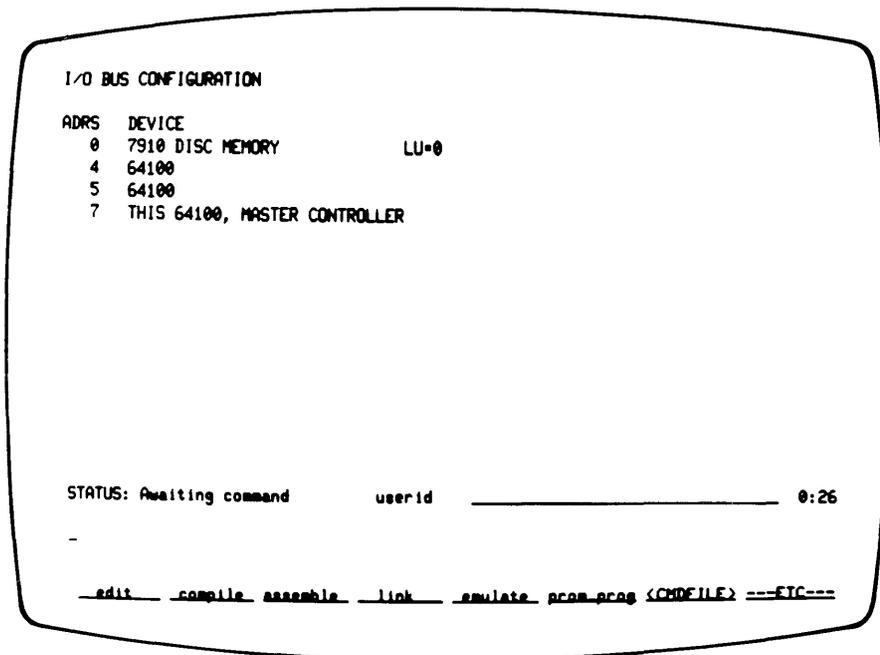


Figure 2-21. System Boot-Up Display

## Line Printer Performance Verification

The SELF TEST switch on the operator control panel initiates a Go/No Go routine which tests the printer to determine if it is in proper operating condition. This self test function may also be performed with a control code.

Push the SELF TEST switch to activate the self test function. When the switch is pressed:

- a. ROM, RAM, Interface, and Real-time Clock are tested. An audible tone sounds if all tests function properly.
- b. Servo movement is tested. If the carriage is not in the home position (column 0), it will return to this position then drive right to the right stop position then reverse and drive to the home position again. If all servo test conditions are correct, the tone will sound.
- c. The power-on sequence and reset are complete and the printer is set at default conditions.
- d. The primary character set is then printed. The order of the printing test is:

two lines of 6 LPI (Normal Mode)

two lines of 8 LPI (Normal Mode)

one line each of compressed, expanded and auto-underline mode.

### NOTE

---

LPI= lines per vertical inch.

---

Display Functions are set, and the complete primary character set is printed, followed by a carriage return and line feed. The printout will contain more than one line for the Expanded Mode and the Display Functions Mode.

### NOTE

---

The second line of the printout displays the alternate character set. If no alternate character set is present, the second line will be blank.

---

- e. When the self-test printout has been completed (see figure 2-22), the printer is reset.

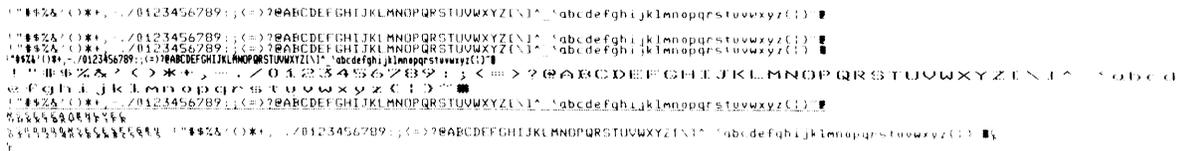
**NOTE**

---

If the self test routine fails, press  and try the test a second time. If the self test fails the second time, contact your HP Service Representative.

---

Set rear-panel address switches to address 1. Connect the line printer to the disc with a system bus cable. Press   on the development station.



**Figure 2-22. Line Printer Performance Verification**

## Additional Development Stations

Additional development stations can be added (in series) up to a total of six. With the first development station set as master controller, all other stations must be set as slave controllers.

To add development stations, proceed as follows:

- Set station to slave controller.
- Run development station performance verification.
- Set address switch to next appropriate address.
- Connect system bus cable to next component.

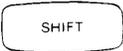
**NOTE**

---

The master controller station must be on one end of the entire bus system (refer to "System Bus" in this chapter).

---

e. Turn slave controller power on.

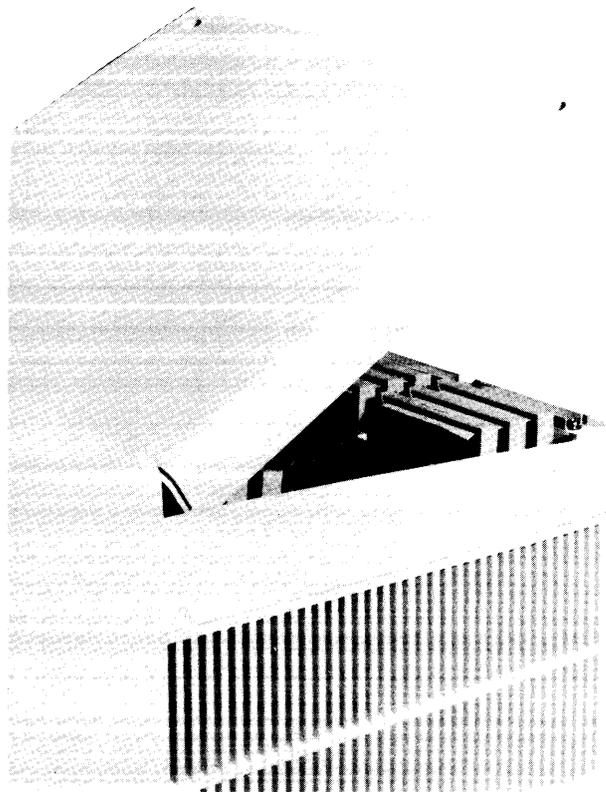
f. Press   on the master controller.

The display should show the I/O configuration with the new station recognized by address. If a "DEVICE NOT RECOGNIZED" message is given for the particular address, rerun the Performance Verification. If the problem still exists, contact the appropriate service personnel.

g. Once all development stations are on line, the entire system is operational.

h. Unique information concerning RS-232 and TTY communications is given at the end of this chapter.

i. General system operations are given in Chapters 3 through 11.



**Figure 2-23. Card Cage Access**

## Card Cage

On the right-hand back portion of the top of the development station is a cover (see figure 2-23). This cover is removed by loosening the two hold-down screws. Lift the back portion of the cover and remove.

## Master Controller

Just inside the rear panel is the rear-panel board (see figure 2-24). On the lower left-hand side are four sockets and two IC's. The positions of these IC's determine whether the development station will act as a master controller or slave controller. If the IC's are in the U3 and U4 positions, the development station will act as a master controller; if the IC's are in positions U11 and U12, the development station will act as a slave controller. The master controller has responsibility for initializing the bus at power up, bus error recovery, and resistive line termination. Otherwise, after power-up, all stations operate as peers in the cluster.

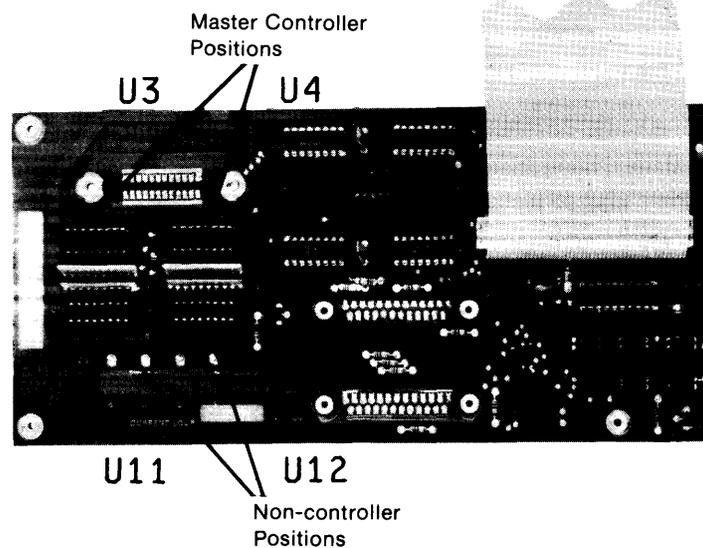


Figure 2-24. Rear Panel Board

In a single development station system, the development station must be designated the master controller by putting the IC's in the U3 and U4 controller positions.

**NOTE**

---

In a multistation development system, only the end development station can be designated as the master controller.

---

In any power-up sequence of a multistation system, the master controller must be turned on. Due to the electrical configuration of the rear panel, this development station must be left on any time system operation is desired.

**NOTE**

---

If it becomes necessary to perform maintenance on the master controller station, reconfigure another development station (U3 and U4) and move that development station to one end of the bus. Make sure the old master controller is removed from the bus. When the old development station is ready to be added back into the system, put the IC'S in the slave-controller position (U11 and U12) and add it to the system.

---

**Card Slots**

There are 13 card slots. The first three slots have cards installed at the factory. These cards must be in the system in the order given for the system to operate. The three required cards (plus the one option card) are:

- slot A - I/O pc card
- slot B - Display control pc card
- slot C - CPU pc card
- slot 0- Tape Controller Card (if used; required for at least one station.)

### Power Supply Loading

There is a limit to the number and types of option boards that may be installed in the card cage with the 300-watt power supply. The limit is determined by the amount of available current from the power supplies. Table 2-5 is an example of power supply loading using the values given in table 2-6.

Table 2-6 gives the current requirements.

**Table 2-5. Power Supply Available Currents**

Power Supply	+12 Vdc	+5 Vdc	(-5.2 Vdc) + (-3 Vdc)
<b>Available Current</b>	6.0 A	20.0 A	10 A
CARD CAGE			
Analysis Board		3.0	
6800 Emulation System		6.5	
PROM Programmer System		1.3	
Minicartridge Control (tape drive system)		0.3	
Memory			
Control		1.0	
16K addressed		3.6	
16K		1.9	
		17.6A	

When the listed options are placed in the Model 64100A it totals 17.6 amperes. This leaves 2.4A available for use by an option board. Do not add any option board that exceeds 2.4 amperes.

Each time the option cards are reconfigured, total loading of the cards must be recalculated to ensure that power supply limits are not exceeded.

**Table 2-6. Power Supply Loads**

<b>Supply Voltages</b>	+12 Vdc	+5 Vdc	(-5.2 Vdc) + (-3 Vdc)
<b>Available Current</b>	2.5A	18.25A	10.0A
<b>OPTION CARDS</b>	<b>CURRENT RATING</b>		
Analysis (see note 1)		3.0A	0.6A
8080 Emulation Sys 8085 Emulation Sys 6800 Emulation Sys Z80 Emulation Sys Prom Programmer Cartridge Control	0.1A    0.1A 0.3A	6.0A 6.4A 6.5A 5.3A 1.3A 0.3A	
Memory Control (see note 2)		1.0A	
Memory 4K (8KBytes) 8K (16KBytes) 16K (32KBytes)		(see note 3) 2.9 (1.2)A 3.1 (1.5)A 3.6 (1.9)A	
<p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. An emulation system consists of the emulation controller card and an emulation pod.</li> <li>2. The memory control card can control up to four (4) memory boards.</li> <li>3. One row on one memory board is addressed at all times. Number in ( ) applies when no rows are addressed. This condition will occur only when more than one memory board is installed.</li> </ol>			

**CAUTION**

---

When configuring the card cage, ensure that the current limits are not exceeded.

---

In table 2-6, the option cards have their current ratings listed in the appropriate supply column. The available current rating is the total current rating that is available for option cards from that supply or supplies.

The remaining card slots are defined in the Emulation/Memory configuration section of this chapter.

The cards interface to the system through the mother board on the bottom of the card cage. A cable from the rear panel board (on the rear panel) makes connection to the top center connector on the I/O board.

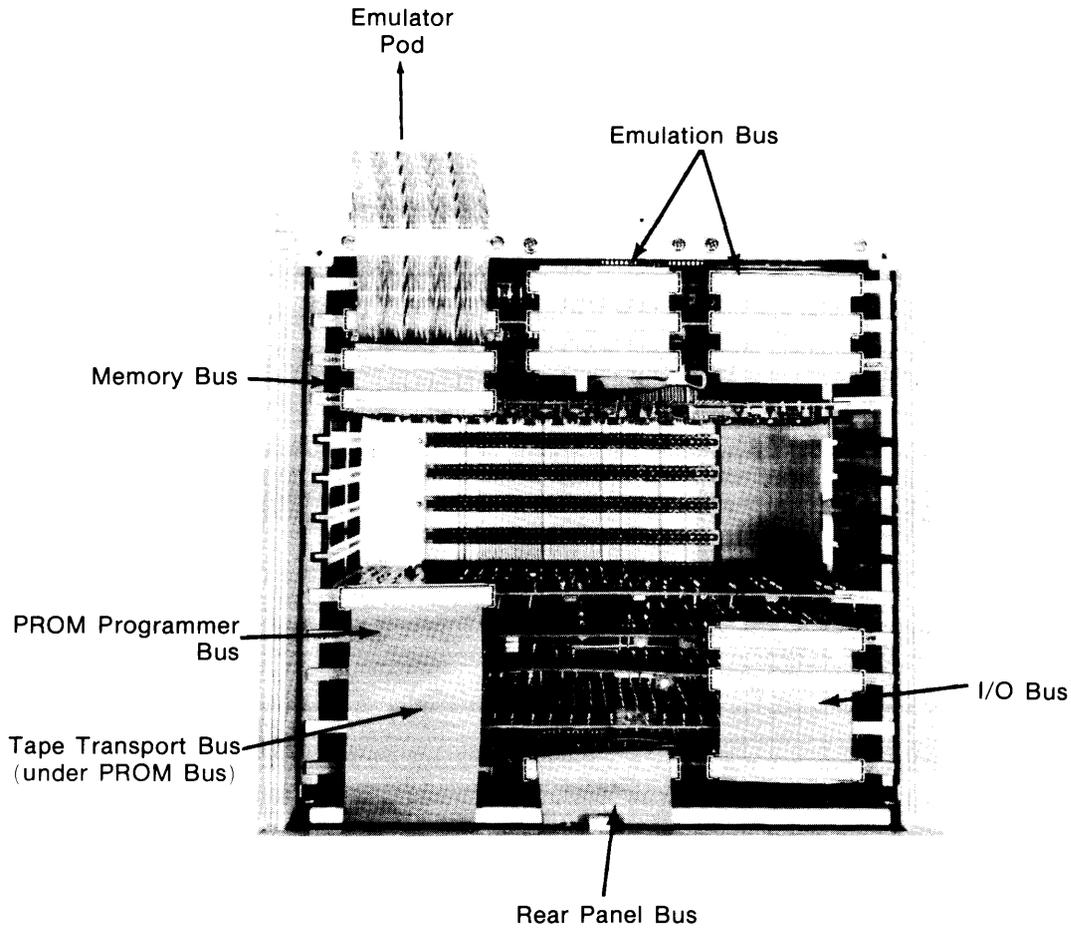
Emulation pod cables are routed to the outside of the development station through three slots located at the back of the top cover and the rear panel. Cable lengths for the option cards are determined at the factory and shipped at maximum length.

For convenience, a label is just above the card cage on the left-hand side. As cards are inserted into the card cage, mark the card name on the label. The label can be erased and the card name changed as the card cage is reconfigured.

## Bus Configuration

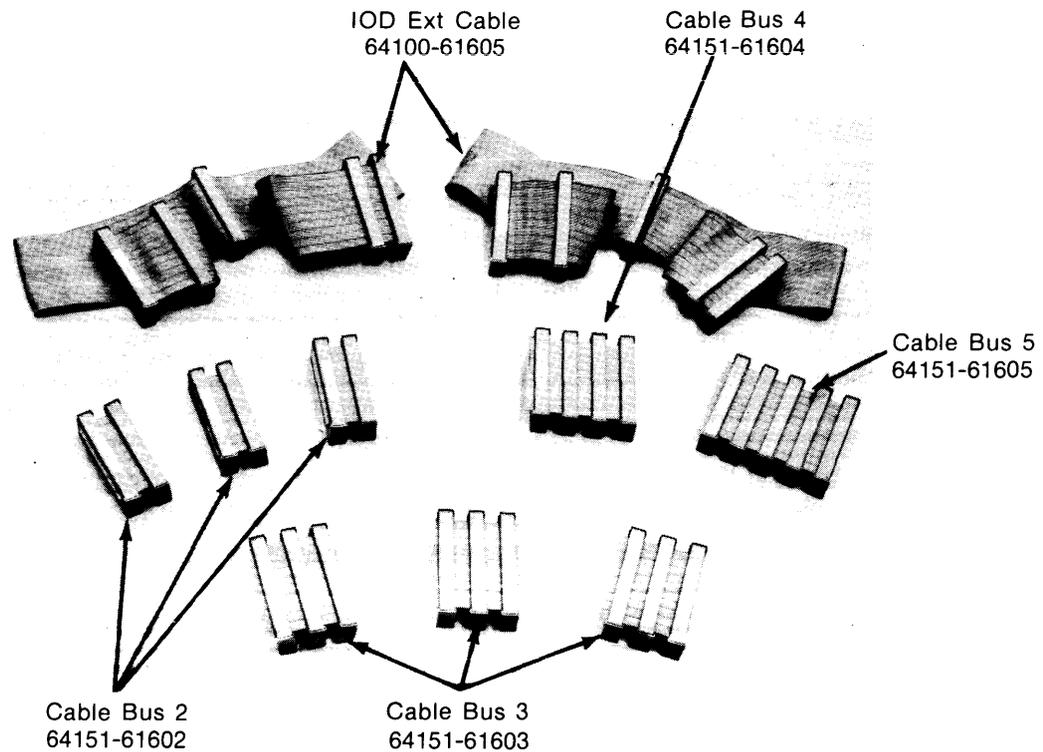
Figure 2-25 identifies six buses as follows:

- I/O (Input/Output) Bus
- Memory Bus
- Emulation Bus
- PROM Programmer Bus
- Tape Transport Bus
- Rear Panel Bus



**Figure 2-25. Bus Configuration**

The I/O bus requires connection between the I/O (slot A) card and CPU card (slot C). The connection is made with a ribbon cable on the top right-hand connector of each card. If the tape controller card is in the system the top right-hand connector must be connected to the I/O bus. This may require a different cable than is in the development station. Figure 2-26 shows the cables in the HP Model 52150A cable kit.



**Figure 2-26. Model 52150A Cable Kit**

The memory bus requires that the memory control board be connected to the applicable memory boards. This connection is made on the top left-hand connector. Appropriate 2- or 3-connector bus cables should be used to interconnect all memory boards.

**NOTE**

---

There must be one memory controller board for every four memory boards or less, regardless of the amount of memory.

---

The emulator bus requires a cable connection from the emulator board to the analysis (optional) card and the memory control card. The center and right-hand connectors of these cards are for the emulator bus.

The analysis bus requires interconnection between all analysis cards. This connection is made on the top left-hand connector.

Two additional cable connections are not identified as bus connections. They are the cables from the tape drive card and the PROM programmer control card.

The tape drive cable runs from the top left-hand connector (small pin connector) on the tape drive board to the tape drive unit on the right inside of the front panel.

The PROM cable (HP part no. 64501-61601) runs from the PROM programmer control card over the top of the card cage and down to the well of the PROM programmer module (lower right front of development station). There should be a single connector on the end connecting to the PROM programmer control card. There should be two connectors on the end in the well. Certain PROM programmer modules require the double connection. Refer to the PROM programmer chapter of this manual for proper installation of PROM programmer modules.

## **Card Installation**

To install one of the option cards, hold the edge of the card as shown in figure 2-27. The components should face the front of the development station. Slide the board down into the card cage. Align the connector on the bottom of the board with the socket on the mother board. Apply enough pressure to seat the board in the socket.

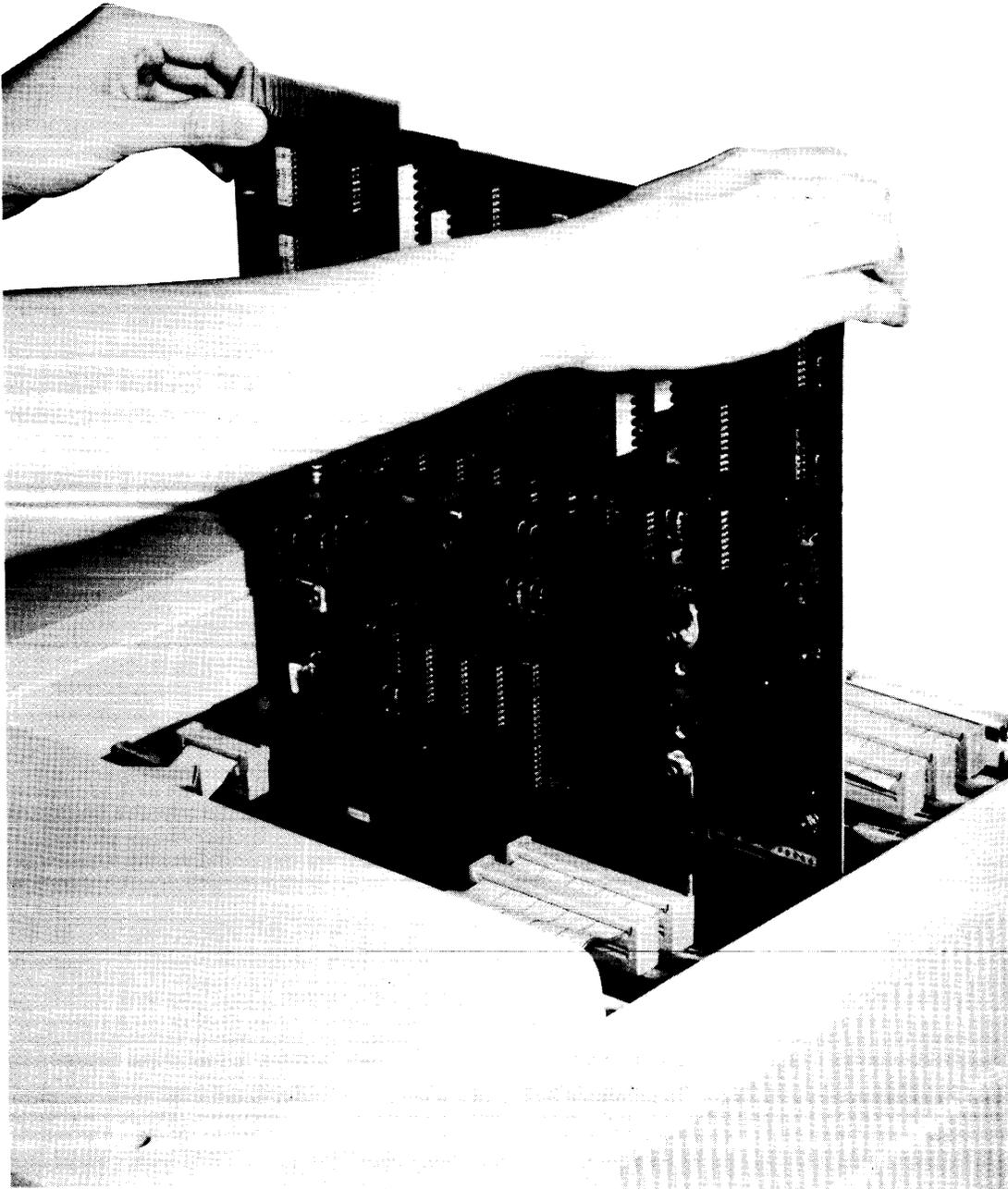


Figure 2-27. Card Installation

## Emulation/Memory Configuration

Figure 2-28 gives two card cage configurations:

1) Emulation/Analysis/Memory and 2) Emulation/Memory. The PROM Programmer Control card can be placed in any slot 0 through 9 depending on the configuration.

### 1. Emulation/Analysis/Memory

A _____	I/O Board
B _____	Display Control Board
C _____	CPU Board
0 _____	Tape Controller Board (If used in the system)
1 _____	
2 _____	PROM Programmer Control Board may be
3 _____	in any slot 1 through 4.
4 _____	
5 _____	Memory Board
6 _____	Memory Board
7 _____	Memory Control Board
8 _____	Internal Analysis Board
9 _____	Emulator Board

### 2. Emulation/Memory

A _____	I/O Board
B _____	Display Control Board
C _____	CPU Board _____ Tape Controller Board
0 _____	Tape Controller Board (If used in the system)
1 _____	
2 _____	PROM Programmer Control Board may be
3 _____	in any slot 1 through 5.
4 _____	
5 _____	
6 _____	Memory Board
7 _____	Memory Board
8 _____	Memory Control Board
9 _____	Emulator Board

**Figure 2-28. Recommended Card Cage Configuration**

## Address Settings

The address provides a unique identifier for each component in the system. This allows intercommunications between components to be done in an efficient manner.

The system disc must always have a system bus address setting of 0. The line printer must have an address of 1. Development station(s) must always have an address setting of from 2 through 7. Each development station must be a unique address. Table 2-7 gives the address settings for the development station.

Figure 2-29 shows the development station address switch. Only the three right-hand bits are applicable to the address setting. For the disc, rotate the thumb wheel until the address displays 0. Figure 2-31 shows the address switch for the HP Model 2631B Line Printer. Table 2-8 gives the switch settings of the line printer switches (always address 1).

### NOTE

---

For the 7906M, 7920M, and 7925M disc memories, a total of three address selections must be made as follows:

1. System Bus Address = 0 (Selected by right-hand thumbwheel switch on HP-IB Board, top slot inside the 13037 Disc Controller.)
  2. CPU = 0 (Selected by left-hand thumbwheel switch, on HP-IB Board, top slot inside the 13037 Disc Controller.)
  3. Disc Drive Unit Select = 0 (Selected by rotary switch on disc drive operator panel.)
- 

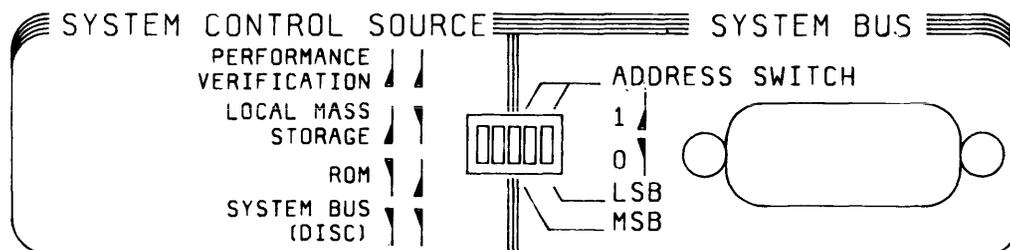
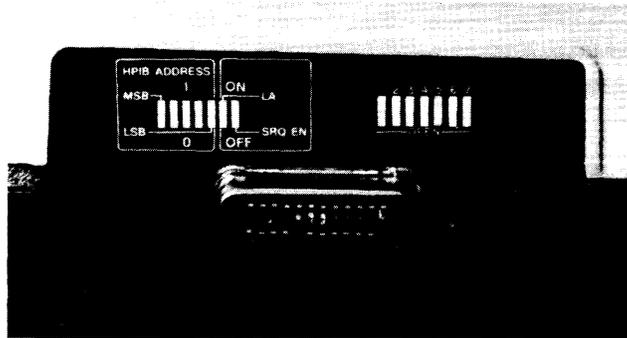


Figure 2-29. Model 64100A Address Switch



**Figure 2-30. Model 2631B Address Switch**

The development station address switch has a unique function (discussed under “Card Cage” in this chapter).

**Table 2-7. Model 64100A Address Switch Setting**

Address	MSB		LSB	
0	0	0	0	
1	0	0	1	
2	0	1	0	} Valid Development Station Addresses
3	0	1	1	
4	1	0	0	
5	1	0	1	
6	1	1	0	
7	1	1	1	

**Table 2-8. Model 2631 Line Printer Address Switch Settings**

Address	Address Switches				
	A1 (MSB)	A2	A3	A4	A5 (LSB)
0	0	0	0	0	0
1 (valid printer address)	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1

**NOTE**


---

Verify positions 6 and 7 as both in 0 position; otherwise, the bus locks up.

---

## System Bus

### General Interconnect Information

Model 64000 components must be connected in series, and the master controller development station must be connected to one end. It must not be connected in the center of the system. The system bus connector (figure 2-31) provides the necessary interface between the Model 64100 and other components in the system. Maximum distance for the interconnection is 20 metres (65 ft), except in systems with only one development station and one disc drive, in which case the maximum distance is 18 metres (59 ft). The bus cable part number is 8120-2718.

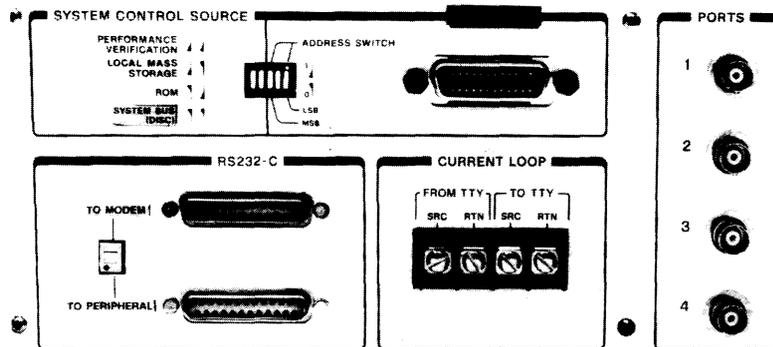


Figure 2-31. System Bus

#### NOTE

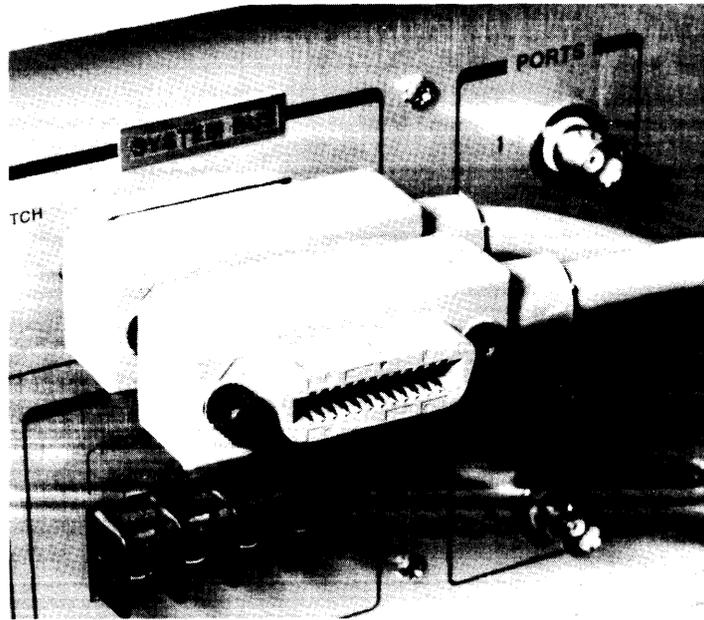
---

Although the cable(s) used to interconnect components of the 64000 System are HP-IB cables, do not interpret the system bus as an HP-IB bus. Only those items specified for the Model 64000 Logic Development System may be connected to this bus. No more than six development stations may be connected on the bus.

---

## Bus Connections

Figure 2-32 shows the standard bus connection between the development station, line printer and the disc. In order for the development station, line printer and the disc to communicate with each other, each must have a unique address. In this configuration there can be no more than two interface cables connected at one place.



**Figure 2-32. Standard Bus Connections**

**NOTE**

---

Star connections (3 cables connected at one point) are not allowed in the Model 64000. Only two connectors may be connected at one point.

---

## RS-232-C/Current Loop Communications

### EIA RS-232-C Interface Standard

Most voltage interfaces in North America conform to the EIA RS-232-C Interface Standard. This specifies a 25-pin connector as the standard interface in data communication networks, with lettered pin assignments for ground, data, control and timing circuits. The interface also specifies the mechanical and electrical requirements of an interface, within an operating range of 0 to 19,200 bps in-bit-serial operation. It provides a common meeting ground, allowing interaction between many types of equipment and manufacturers, providing great flexibility in the selection of equipment for data communication networks.

### Mechanical

The signal interface between the Data Communications Equipment (DCE), usually a modem, and the Data Terminal Equipment (DTE), usually a remote terminal or data processor, is located at the RS-232-C-specified connector located between equipment. Cables less than 50 feet (15 meters) are recommended for interconnection. Longer cables may be used provided the load capacitance is suitable. The Model 64100A pin assignment shown in table 2-9 must be used and unassigned pins may carry additional circuits determined by mutual agreement between the communicating parties. Figure 2-33 is the Model 64100A Development Station RS-232-C/Current Loop Schematic. Figure 2-34 is the RS-232/Current Loop Interface.

### Electrical

Except for protective and signal grounds, all circuits carry bipolar low-voltage signals suitable for electronic circuits. All voltages are measured at the connector with respect to signal ground (AB) and cannot exceed  $\pm 25$  V. The significance of the bipolar signals is summarized in table 2-10, with the region between  $\pm 3$  V defined as the transition region.

While RS-232-C designates 23 circuits, the number actually in use depends upon the type of modem.

**Table 2-9. Model 64100A RS-232-C Interface Connector  
Pin Assignments**

Signal	Direction	Pin Number	Circuit	Description
<b>Development Station</b>	<b>Modem</b>			
		1	shield gnd	Protective Ground
→	→	2	TXD	Transmitted Data
←	←	3	RXD	Received Data
→	→	4	RTS	Request to Send
←	←	5	CTS	Clear to Send
		6	DSR	Data Set Ready
		7	signal gnd	Signal Ground (common return)
←	←	8	CARDET	Carrier Detect
		9	---	unassigned
		10	---	unassigned
		11	---	unassigned
		12	---	unassigned
		13	---	unassigned
		14	---	unassigned
		15	TXCLK	Transmit clock
		16	---	unassigned
		17	RXCLK	Receive clock
		18	---	unassigned
		19	---	unassigned
→	→	20	DTR	Data Terminal Ready
		21	---	unassigned
		22	---	unassigned
		23	---	unassigned
		24	---	unassigned
		25	---	unassigned

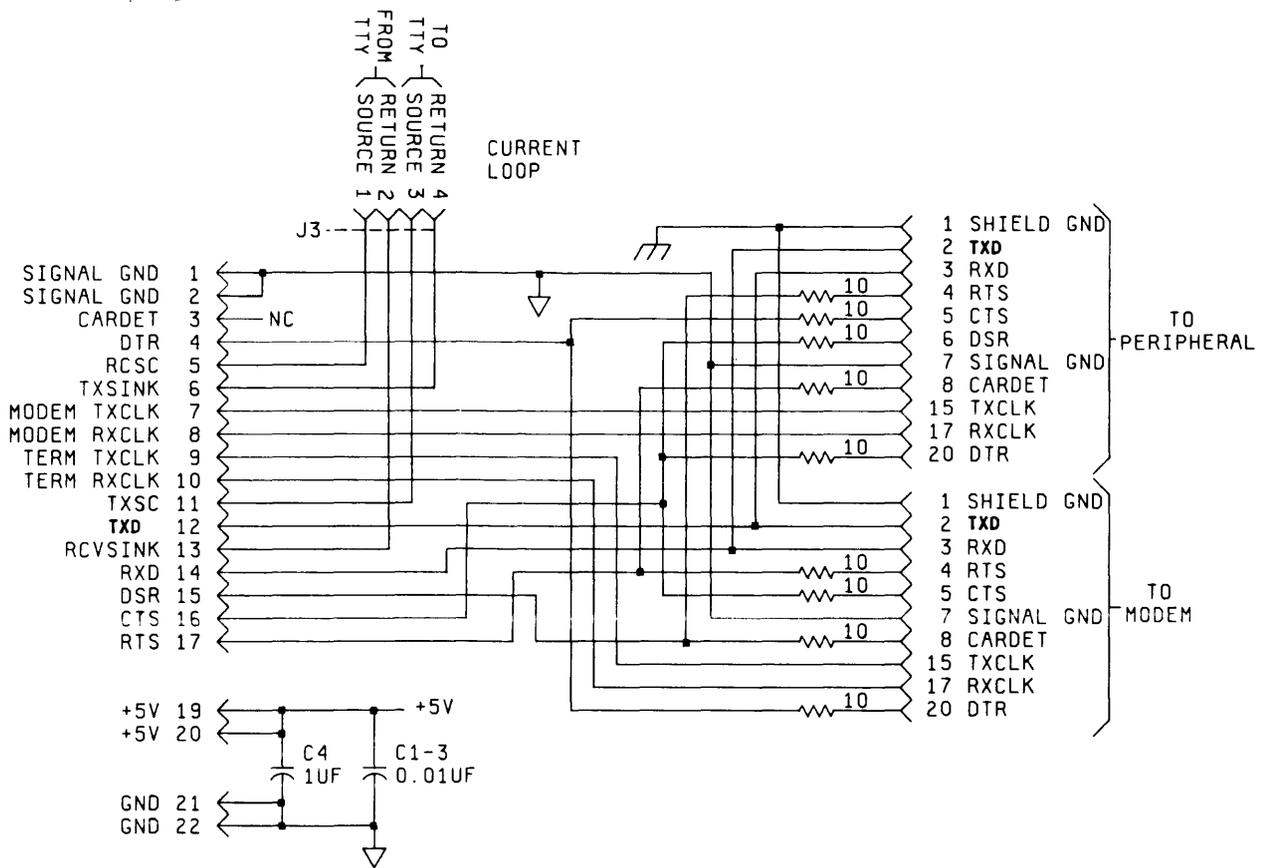


Figure 2-33. Model 64100A RS-232-C/Current Loop Schematic

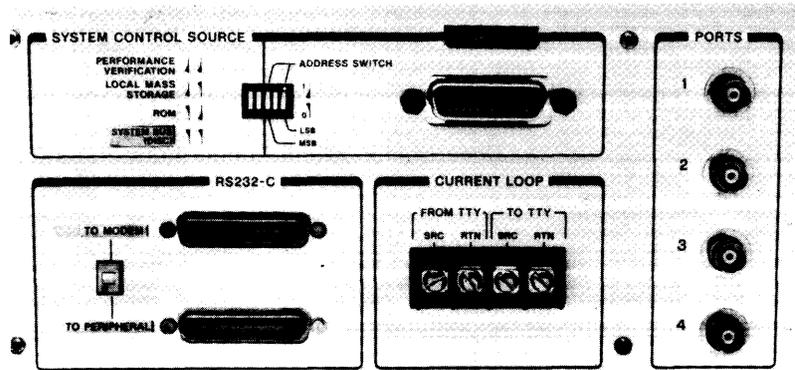


Figure 2-34. RS-232-C/Current Loop Interface

Table 2-10. EIA RS-232-C Interface Voltages

		Negative voltage (-3 to -25)	Positive voltage (+3 to +25)
<b>Data Circuits</b>	Binary State	1	0
	Signal Condition	Mark	Space
<b>Control Circuits</b>		Off	On

## RS-232-C Communication Considerations

The Model 64000 provides for asynchronous serial communication between the Model 64000 and external communications devices. Communication is controlled by five switches on the I/O board (first board in the card cage). Figure 2-35 shows the location of five switches. Table 2-11 shows the required switch positions to evoke the appropriate serial communications.

Switch S1 is set to either 20 mA or 60 mA depending on the requirements of the TTY. The TTY is connected to the rear panel TTY terminals for half-duplex or full-duplex communications.

Switch S2 provides for internal receive or transmit clock selection.

Switch S3 selects I LOOP (TTY) or RS-232-C operation. Switch S4 is an 8-bit multifunction switch. Table 2-12 shows the individual bit functions and the settings required to obtain these functions.

Bits 2 thru 5 of Switch S5 control the baud rate (see table 2-13). Bit 1 controls the RTS line for full and half-duplex operation. For half-duplex operation, Bit 1 is set to the off position. The RTS output is then driven by the USART. For full-duplex operation, Bit 1 is set to the on position. The RTS line is pulled up to +12V.

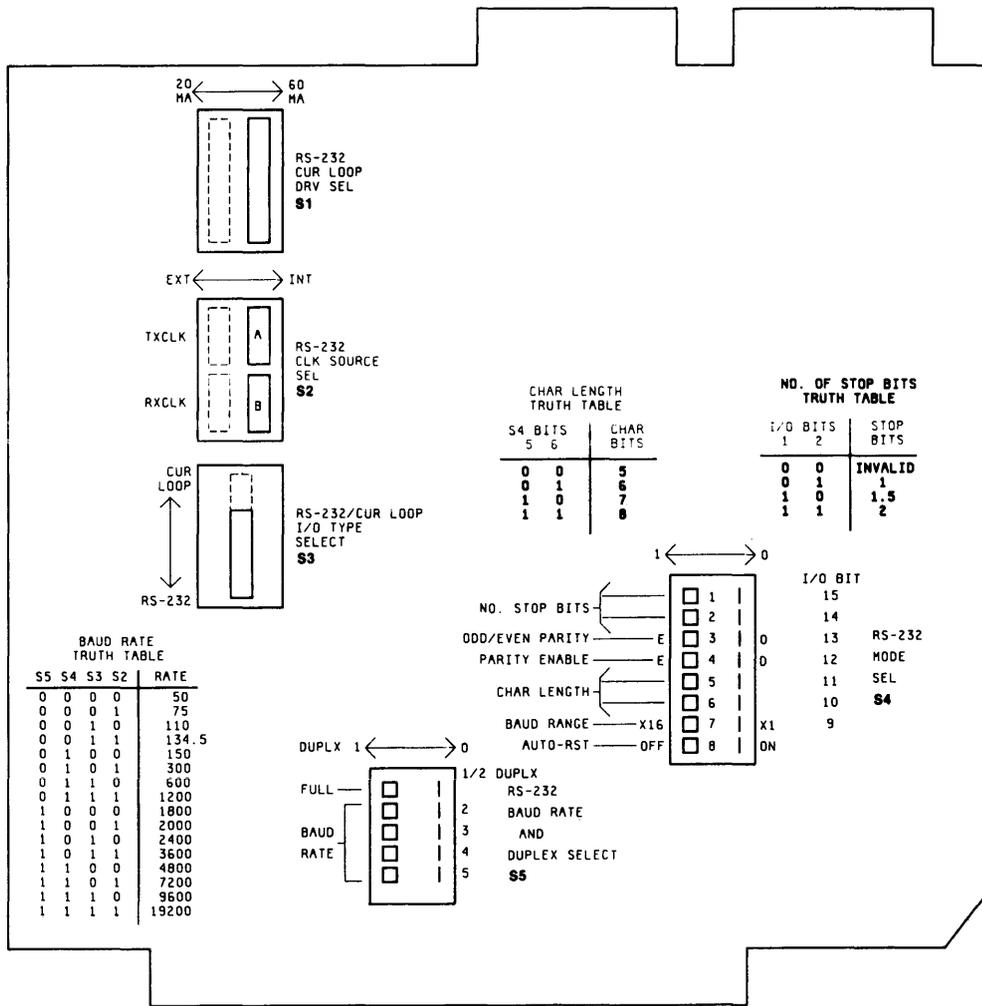


Figure 2-35. I/O Board Switch Identification

**Table 2-11. I/O Switch Functions**

Switch	Position	Name	Functions
S1	left right	Current Loop Drive Select  20 mA 60 mA	Selects appropriate current operation for TTY if current loop selected.
S2	left right	Ext clock select Int clock select	Provides clock selection.
S3	up down	Current Loop operation RS-232 operation	Selects current loop or RS-232C ASYNC operation.
S4	See Table 2-12	Mode Select	Selects Auto Reset, Stop Bit Qualifier, Parity and Character length.
S5	See Table 2-13	Baud Rate	Selects baud rate (bit 2 to 5). Selects full or half-duplex operation (bit 1).

**Table 2-12. S4 Bit Functions**

Bit	Function	Comments
1 (msb) 2	# of stop bits	00 = invalid, 01 = 1 bit 10 = 1 1/2 bits 11 = 2 bits
3 4	Odd/even Parity Parity enable/ disable	1 = even, 0 = odd 1 = enable, 0 = disable
5 (msb) 6	Word (Character) Length	00 = 5 01 = 6 10 = 7 11 = 8
7	Clock Mode	1 or divide by 16
8	Auto Reset	On/Off

**Table 2-13. S5 Baud Rate Selection**

Baud Rate	Switch Position			
	S5 Bits			
	MSB 5	4	3	LSB* 2
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
300	0	1	0	1
600	0	1	1	0
1200	0	1	1	1
1800	1	0	0	0
2000	1	0	0	1
2400	1	0	1	0
3600	1	0	1	1
4800	1	1	0	0
7200	1	1	0	1
9600	1	1	1	0
19200	1	1	1	1

\*Bit 1 controls the RTS line. In the "OFF" position, the RTS line is pulled to +12V for full-duplex operation. In the "ON" position, the RTS line is driven by the USART for half-duplex operation.

## Development Station RS-232-C Requirements

The Model 64100A can receive two types of files: 1) source or listing files; and 2) absolute, relocatable or PROM record files.

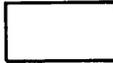
When operating at 1200 baud or below, it is not necessary that handshake protocol be used, as no loss of information will occur. Above 1200 baud it is mandatory that the handshake protocol be observed.

When receiving source or listing files, the 64100A looks for a carriage return, line feed, or carriage return/line feed as the end of the record.

When receiving absolute, relocatable or PROM record files, the following diagram must be adhered to in order for the 64100A to process the data.

 First byte is the number of words in the record.

 Record

 Last byte is the checksum of the data in the record (excluding the word count and the checksum).

The length of a record must not exceed 256 bytes.

Errors encountered during RS-232-C communications will be displayed on the CRT as:

checksum=xxx, parity=xxx, size=xxx, overrun=xxx

### NOTE

---

If framing errors=xxx, check the baud and parity switch settings (located on Display Controller Board). If error occurs on every byte of data, baud and/or parity switches are probably not set correctly. Occasional framing errors indicate probable hardware incompatibility.

---

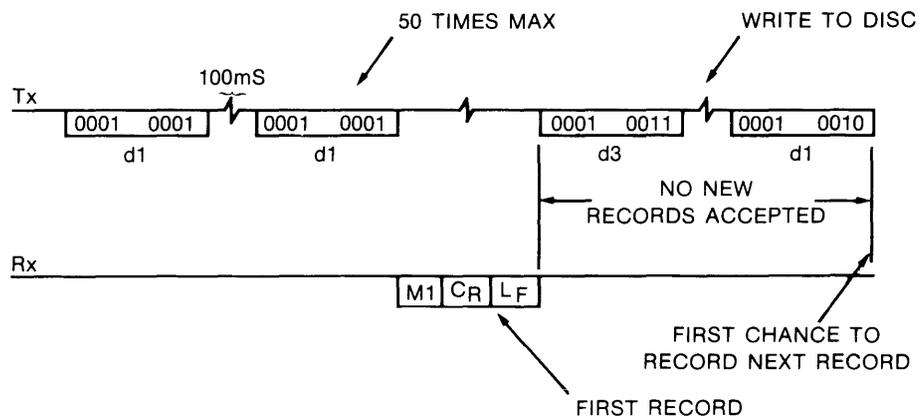
To terminate the file, a record beginning and consisting solely of E<sub>T</sub> (binary 4) is expected for source files or a null (binary 0) for other file types. If the system has received an end of record, no other information is received, and the system will automatically time out after 10 seconds.

### Software Handshake Conventions

In receive mode, the 64000 will output an X-ON (ASCII DC-1) until data is received. Also, after each record is read, it will generate an XX-OFF (ASCII DC-3) while storing the record followed by an XX-ON to signal ready. If used, this can allow the 64000 to run at maximum speed; otherwise, 1200 baud is the maximum advised speed.

In transmit mode, the 64000 will listen to the X-ON, X-OFF convention described above. Once an X-OFF is received it will wait for an X-ON before it continues to transmit. This convention is not necessary, and if it is not used, transmission will continue as if the receiving end can maintain the selected baud rate. Software handshake timing is shown in figure 2-36.

PROTOCOL	ASCII	BINARY	HEX
X ON	DC-1	0001 0001	11
X OFF	DC-3	0001 0011	13



**NOTE:** RECEIVER TIMES OUT (AFTER 3 SECONDS). TIMER WILL BEGIN ONLY AFTER FIRST RECORD IS RECEIVED.

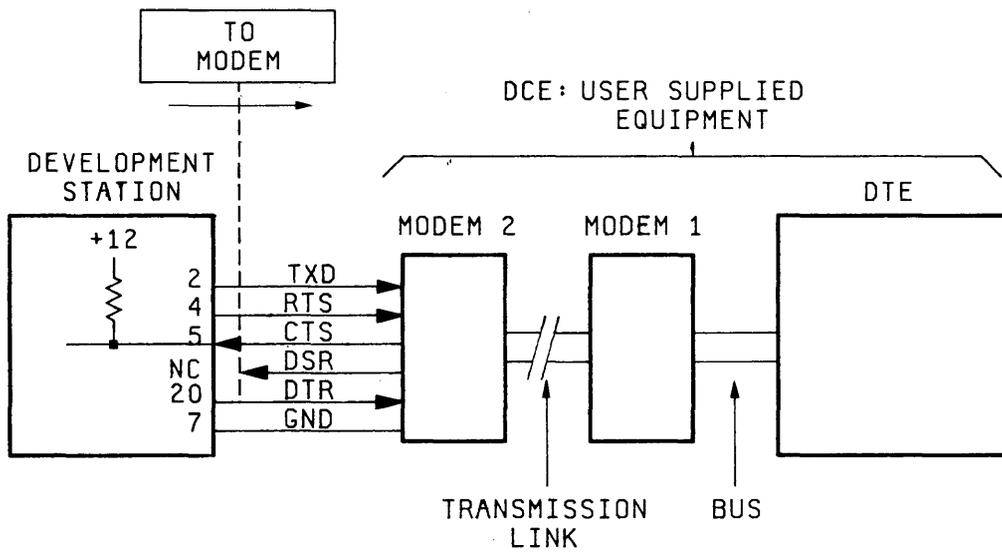
INITIATED COPY RS-232 TO <FILE>

Figure 2-36. Software Handshake Timing

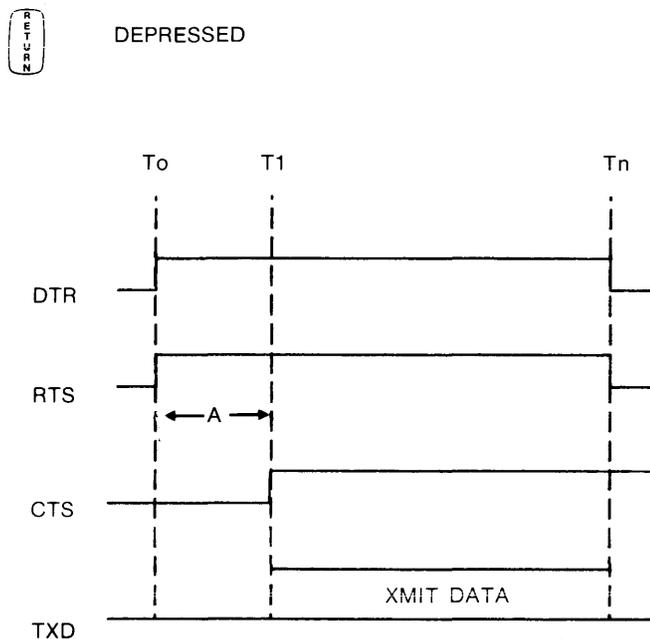
Development Station as Terminal Talker (see figures 2-37 and 2-38).

Syntax: copy <FILE> to rs232

Equipment Connection:



**Figure 2-37. Terminal Talker Equipment Connection**



**Figure 2-38. Terminal Talker Timing Diagram**

Sequence of Major Events

- a. The modem DSR line is not connected to the development station and therefore DSR is ignored as an input.
- b. When RETURN is pressed ( $T_0$ ), the RTS and DTR line goes true (+12V).

**NOTE**

---

RTS can be set true (+12V) at all times by setting Bit 1 to a logical "1" on Switch S5 (on I/O board).

---

- c. The development station will not send data until CTS is raised true. Modem sets CTS true ( $T_1$ ). Time A (Modem strap option) is set by user.

**NOTE**

---

The development station TXD output (pin 2) idles in a marking state (logical "1", ~ -12V) between transmission. In the event a CTS line is not connected to the development station, an internal pull-up circuit will bias the CTS input to +12V. This automatically results in a constant CTS true.

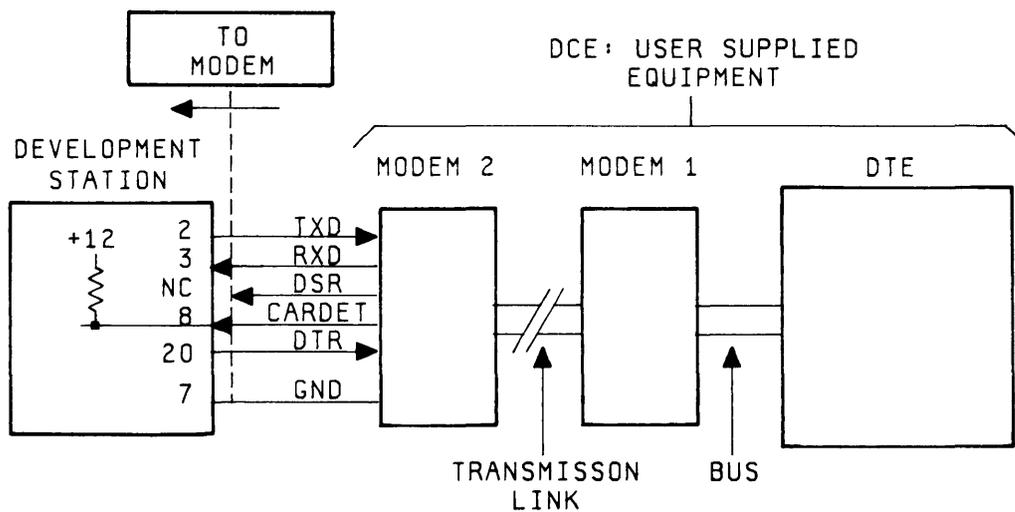
---

- d. The development station transmits data; user's DTE receives data.
- e. When data transmission ends ( $T_N$ ), RTS line goes false.

Development Station as Terminal Listener (see figures 2-39 and 2-40).

Syntax: copy rs232 to <FILE>

Equipment Connection:



**Figure 2-39. Terminal Listener Equipment Connection**

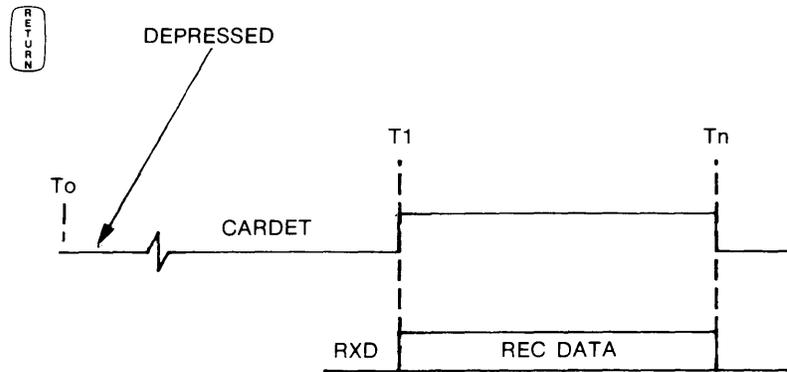


Figure 2-40. Terminal Listener Timing Diagram

Sequence of Major Events

- a. At  $T_0$ , the  key is depressed indicating a desire to receive data.
- b. At  $T_1$ , user modem 2 detects carrier and provides a CARDET true signal. The development station senses CARDET. This true is required for the development station to receive data.

**NOTE**

---

If no connection to CARDET exists, an internal pull-up circuit automatically sets CARDET true (+12V). This results in the development station being in a constant state to receive data.

---

- c. At the end of the received message ( $T_n$ ), the modem drives CARDET false and the development station input is disabled.

Development Station as Modem Talker (see figures 2-41 and 2-42).

Syntax: copy <FILE> to rs232

Equipment Connection:

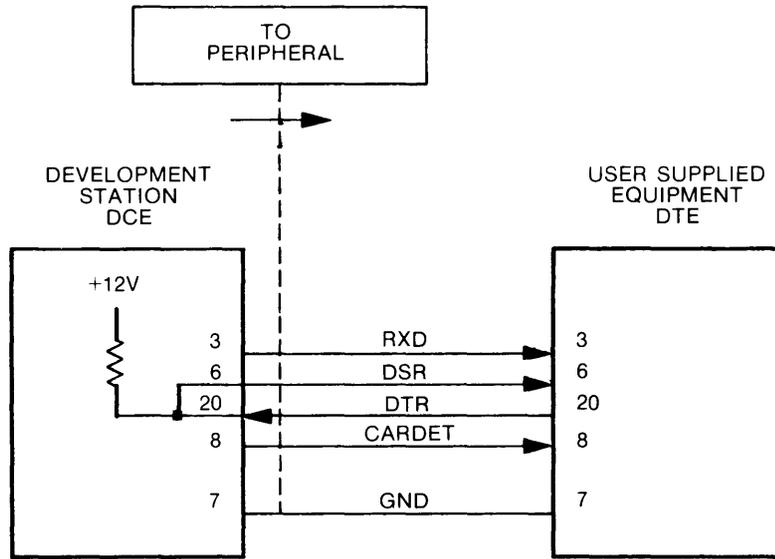


Figure 2-41. Modem Talker Equipment Connection

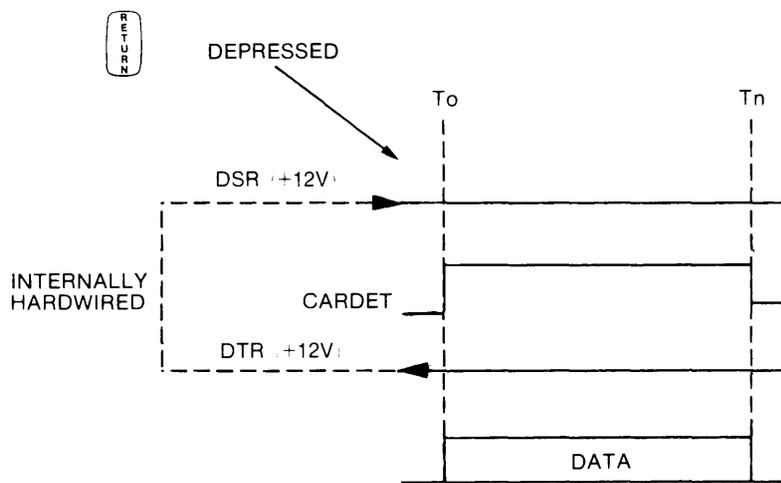


Figure 2-42. Modem Talker Timing Diagram

### Sequence of Major Events

- a. DTR is true from user's DTE. DSR is provided to the DTE by returning DTR.

#### NOTE

---

If no connection to DTR exists, DTR is set true (+12V) by an internal pull-up circuit.

---

- b. When  (T<sub>0</sub>) is pressed, a true CARDET is given the DTE. The development station instantaneously begins data transmission which is outputted on Pin 3 (R<sub>X</sub>).

#### NOTE

---

The CARDET signal is generated by the development station. The development station requires a true DTR signal to transmit. If no connection is made to DTR, the DTR line is set true by an internal pull-up circuit.

---

- c. CARDET is lowered (false) following completion of transmitted message (T<sub>N</sub>).

#### NOTE

---

The development station will place R<sub>X</sub> data (Pin 3) in a steady mark state (-12V) between messages.

---

Development Station as Modem Listener (see figures 2-43 and 2-44).

Syntax: copy rs232 to <FILE>

Equipment Connection:

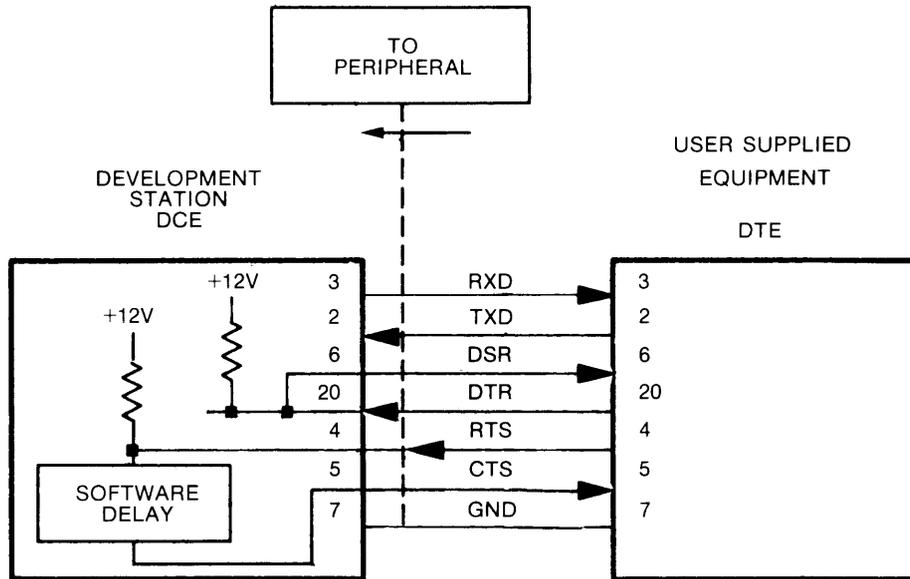


Figure 2-43. Modem Listener Equipment Connection

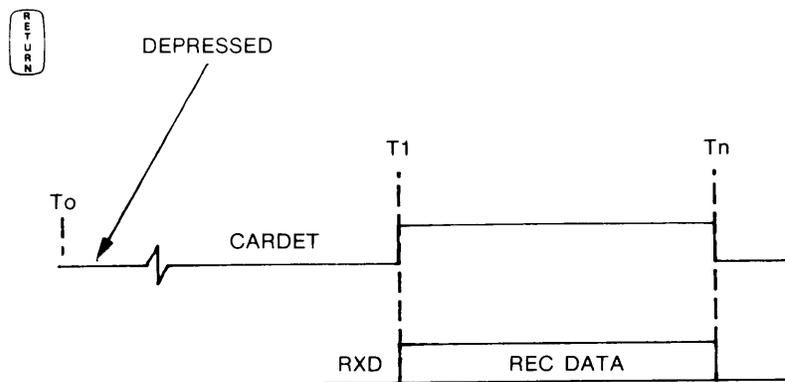


Figure 2-44. Modem Listener Timing Diagram

### Sequence of Major Events

- a. DTE DTR line true (+12V). Model 64100A connects DTR to DSR, effectively returning the DTE's own DTR signal as DSR. If DTR is not connected, an internal pull-up circuit will raise DSR to +12V automatically.
- b. DTE RTS signal goes true. RTS signal ( $T_0$ ) is received by Model 64100A and results in a software driven CTS true.

### NOTE

---

The RTS-CTS turn around is an automatic software function performed by Model 64100A. The duration of the RTS to CTS delay is approximately 100 ms (maximum).

If no RTS connection exists, an internal pull-up circuit will automatically result in a true CTS signal applied to the DTE.

---

- c. DTE equipment transmits and the Model 64100A receives data on Pin 2.
- d. At  $T_N$ , DTE RTS goes low (false) and data transmission ends. Model 64100A CTS goes low and xmit data terminates.

### Current Loop Operation

The 64000 System operates to and from a TTY by using the same commands used in RS-232 operation:

copy <FILE> to rs232

copy rs232 to <FILE>

The only differences are the switch setting on the I/O board. To operate with a TTY, set S1 to 20 mA or 60 mA. Set S3 to ILOOP. Set S4 function table 2-12 , number of stop bits, parity, character length, etc., and S5 Baud Rate, table 2-13 to desired position. The equipment should be configured as shown in figure 2-45.

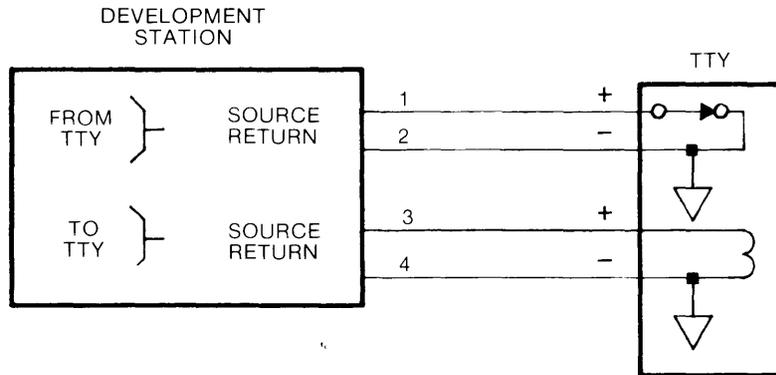


Figure 2-45. Current Loop Equipment Connection

### Executing Remote Monitor Commands

When in Monitor mode, the operating system monitors the RS-232-C serial I/O port for monitor commands. If a command is received it will be executed, if possible, if it is in the proper format. There are certain assumptions that are made. These are:

1. The serial communication link is a two-wire system. That is, only serial data transmit and serial data receive (plus ground) are used and control signals like data terminal ready (DTR) are not used.
2. That the control switch on the 64100A is set to the "to peripheral" position.

The serial data format assumes that an allowable monitor command is preceded by the backwards slash (\). For example, to copy a file to the printer, the copy command becomes:

\copy NAME:source to printer

Note the backward slash (\) header. This command would be executed just as if it were typed in on the keyboard of the development station by the user. Note also that commands are executed in the order they are received.

It is possible to determine if the command was executed correctly by sending enquire (ENQ) to the system. There are two possible responses by the system to such an inquiry. These are:

1. Acknowledgement (ACK) which signals that the preceding command was successfully executed.
2. Negative acknowledgement (NAK) which signals that the preceding command was not successfully executed.

Consider, for example, the following sequence of events: If a command is received on the serial port and is successfully executed, then an operator at the development station tries unsuccessfully to execute a Monitor command, then an ENQ is received over the serial port — the response will be NAK. Remember, the response of ACK or NAK is to the last command. In the case of the above, the last command was the unsuccessful try at the console. Thus it is clear that when using the serial I/O port to execute Monitor commands and query the system, the individual using the serial port is responsible for determining whether the response of the system to an ENQ is valid or not.



