

# INSTALLATION AND SERVICE MANUAL

## 12745D DISC CONTROLLER (13037) TO HP-IB ADAPTER KIT

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Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

# **PRINTING HISTORY**

New editions incorporate all update material since the previous edition. Updating Supplements, which are issued between editions, contain additional and revised information to be incorporated into the manual by the user. The date on the title page changes only when a new edition is published.

First Printing ...... SEP 1983

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#### SAFETY CONSIDERATIONS

#### **KEEP WITH MANUAL**

**GENERAL** - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

#### **SAFETY SYMBOLS**



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.



Indicates hazardous voltages.



Indicates earth (ground) terminal.

#### WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

#### CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

#### SERVICING

#### WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by servicetrained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

To install or remove a fuse, first disconnect the power cord from the device. Then, using a small screwdriver, turn the fuseholder cap counterclockwise until the cap releases. Install the proper fuse in the cap — either end of the fuse can be installed in the cap. Next, install the fuse and fuseholder cap in the fuseholder by pressing the cap inwards and then turning it clockwise until it locks in place.

**GENERAL INFORMATION** 

#### 1-1. INTRODUCTION

This section contains a general description of the Hewlett-Packard 12745D Disc Controller (13037) to HP-IB Adapter Kit, a list of equipment furnished, a list of documentation, and a list of specifications.

#### 1-2. DESCRIPTION

The HP 12745D Adapter Kit is designed for use with the HP 13037B, 13037C, or 13037D Disc Controller. The adapter kit allows the user to communicate with a system containing 13037-compatible disc drive components and using the Hewlett-Packard Interface Bus (HP-IB). The HP 12745D maintains the use of the HP 13037 command set in its adaption to HP-IB format and preserves the ability of the HP 13037 to control up to eight disc drives.

The adapter kit consists of a printed-circuit assembly (PCA) and two cable assemblies which are housed in the HP 13037 cabinet and an HP-IB interface cable. The adapter kit PCA draws power from the disc controller power supply.

The circuitry on the adapter kit PCA consists entirely of digital logic which performs the following two functions: command interpretation and data transfer. Command execution and setup of the data path are the main functions of two high-speed algorithmic state machines. The actual data transfers are performed by asynchronous handshake logic. A double-buffering technique is incorporated to allow a steady-state data transfer rate over the HP-IB that is lower than the burst rate required by the controller.

#### 1-3. EQUIPMENT SUPPLIED

The following equipment is supplied with the HP 12745D Adapter Kit. The kit is illustrated in figure 1-1.

- HP-IB Adapter Kit PCA, part no. 12745-60010.
- Cable Assembly, part no. 12745-60011.
- Flat Cable Assembly, part no. 12745-60004.
- HP 10833B HP-IB Interface Cable, part no. 8120-3446.

#### 1-4. DOCUMENTATION

Documentation available for the adapter kit is listed in the following paragraphs.

#### 1-5. DOCUMENTATION SUPPLIED

The following publication is supplied with the adapter kit:

HP 12745D Disc Controller (13037) to HP-IB Adapter Kit Installation and Service Manual, part no. 12745-90911.

#### 1-6. ASSOCIATED DOCUMENTATION

The following associated documentation may be ordered from a Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the back of this manual.

 HP 13037D Disc Controller Installation and Service Manual, part no. 13037-90911.

#### 1-7. HP-IB DOCUMENTATION

The Hewlett-Packard Interface Bus is compatible with the information contained in the following document:

• IEEE Standard No. 488-1975, IEEE Standard Digital Interface for Programmable Instrumentation.

#### 1-8. SPECIFICATIONS

Specifications for the HP 12745D Adapter Kit are provided in table 1-1.

General Information 12745

Table 1-1. HP 12745D Specifications

#### **ELECTRICAL CHARACTERISTICS**

COMPATIBLE DISC CONTROLLER: 13037B, 13037C, 13037D

COMPATIBLE DISC DRIVES: Any combination of 7906, 7920,

7925 up to eight total

**DATA TRANSFER RATES** 

Unbuffered mode: 0.75 Mbyte < data rate < 1 Mbyte Buffered mode: 0 < data < 1 Mbyte

AVAILABLE HP-IB ADDRESSES: 0 ≤ address ≤ 7

TYPICAL POWER CONSUMPTION: 3.0A at 5V

#### **ENVIRONMENTAL LIMITS**

#### AMBIENT TEMPERATURE

Operating: 0°C to 55°C (32°F to 131°F) Nonoperating: -40°C to 75°C (-40°F to 167°F)

ALTITUDE

Operating: 4 572 m (15,000 ft) max Nonoperating: 15 300 m (50,000 ft) max

RELATIVE HUMIDITY: 0 to 95% at 25°C to 40°C

(77°F to 104°F) without condensation

#### PHYSICAL CHARACTERISTICS

#### **PCA DIMENSTIONS**

Width: 346 mm (13.6 in.) Depth: 292 mm (11.5 in.)

WEIGHT (APPROXIMATE)

Net weight PCA and cables: 2.3 kg (5 lb) Shipping weight: 2.3 kg (7 lb)

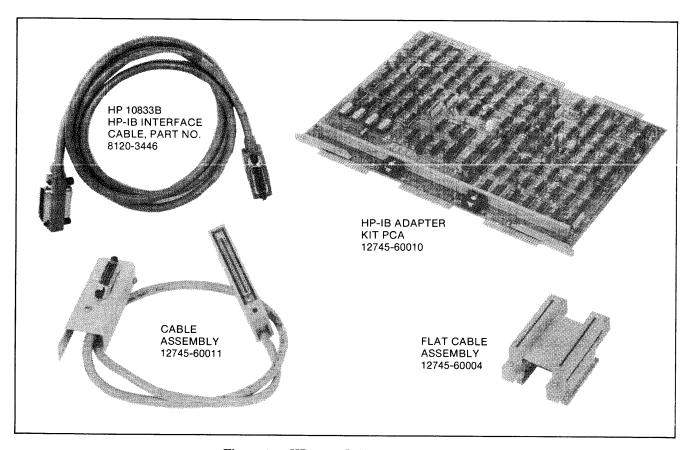


Figure 1-1. HP 12745D HP-IB Adapter Kit

# INSTALLATION

#### 2-1. INTRODUCTION

This section contains unpacking, inspection, repacking, and installation instructions for the HP 12745D Adapter Kit. Information regarding connection to the HP-IB is also supplied.

#### 2-2. UNPACKING AND INSPECTION

When the shipment arrives, check to ensure receipt as specified in the carrier's documents. If the shipping carton is damaged, ask that the carrier's agent be present when the kit is unpacked.

Open the shipping carton and inspect each item for damage. Also check the rigid foam-plastic cushioning, if used, for any signs of deformation which could be indicative of rough handling during transit.

If visual examination reveals any damage to the equipment, follow the damage claim procedure described in paragraph 2-3. Retain the shipping carton and packing material for examination during settlement of any claim.

#### **WARNING**

To prevent electrical shock, do not apply power if there are any signs of shipping damage to any part of the equipment.

#### 2-3. CLAIMS PROCEDURE

If the shipment is incomplete or if the equipment is damaged and fails to meet specifications, immediately notify the nearest Hewlett-Packard Sales and Support Office. If the damage occurred in transit, notify the carrier as well. Hewlett-Packard will arrange for repair without waiting for settlement of claims against the carrier. In the event of damage in transit, retain the shipping container and packaging material for inspection.

#### 2-4. INSTALLATION

#### WARNING

To avoid the possibility of mechanical or electrical hazards, the following installation instructions are intended for service-trained personnel only. Do not

proceed further with these instructions unless qualified to do so.

The following steps are suggested for preparing and installing the HP 12745D Adapter Kit in an HP 13037 Disc Controller.

- a. Ensure that the disc controller can supply the power required to operate the adapter kit PCA. (Refer to paragraph 2-5.)
- b. Ensure that the bus termination on the adapter kit PCA is correct. (Refer to paragraph 2-6.)
- c. Install the components of the adapter kit in the disc controller. (Refer to paragraph 2-7.)
- d. Connect the disc controller to the HP-IB. (Refer to paragraph 2-8.)
- e. Verify operation of the adapter kit using the appropriate diagnostic program. (Refer to paragraph 2-9.)

#### 2-5. POWER REQUIREMENTS

The adapter kit PCA draws 3 amperes at 5 volts from the disc controller power supply. To accommodate this additional load, an HP 13037B Disc Controller must have a serial number prefixed 1740 or greater. For 13037B Disc Controllers having serial numbers prefixed 1625 through 1735, contact the nearest Hewlett-Packard Sales and Support Office for updating information.

#### 2-6. IMPEDANCE MATCH

Proper operation of the adapter kit PCA requires that there be a correct impedance match on the bus going to the disc controller. Four termination resistor packs for this purpose are supplied installed in socket locations U12, U22, U32, and U42 on the PCA. See figure 2-1. The resistors must be in place if the PCA is to be installed in the disc controller of a single-CPU system. In a multi-CPU system, the resistors must be removed before the PCA is installed in the controller.

#### 2-7. ADAPTER KIT INSTALLATION

After ensuring that a) the disc controller can supply the necessary power for the adapter kit PCA, and b) the bus termination is correct, the components of the adapter kit should be installed as follows: Installation 12745

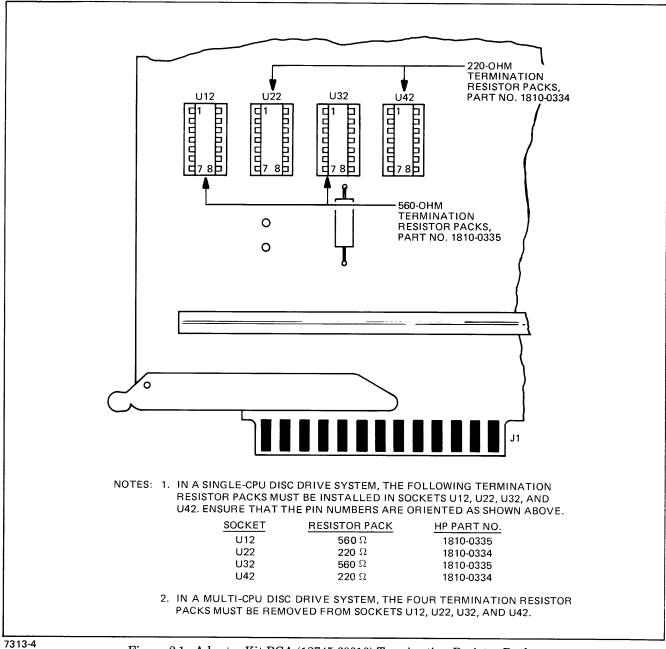


Figure 2-1. Adapter Kit PCA (12745-60010) Termination Resistor Packs

- Set the Power switch on the disc drive(s) to OFF.
- Set the Power switch on the rear panel of the disc b. controller to OFF.
- Disconnect the power cord from the rear panel of the disc controller.
- Remove the disc controller from the system cabinet as follows:
  - (1) Undo the two fasteners on the disc controller front panel and remove the panel.
  - (2) Remove the four rack-mounting flange screws that secure the disc controller to the cabinet.

- (3) Slide the disc controller out of the cabinet and support it on a flat surface level with the controller.
- (4) Remove the top cover of the controller.
- (5) Disconnect the system cables from the PCA's in the controller.
- Remove the following components from the controller:
  - Jumper cable, part no. 13037-60021, connected between the error correct PCA and the microprocessor PCA.
  - Microprocessor PCA.

12745 Installation

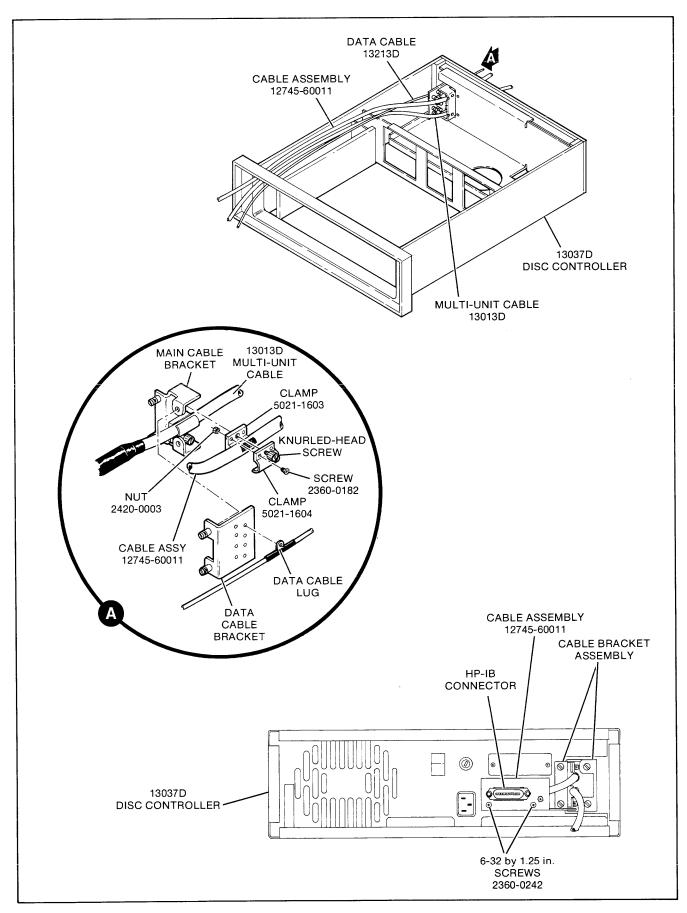


Figure 2-2. Cable Assembly (12745-60011) Installation in HP 13037D

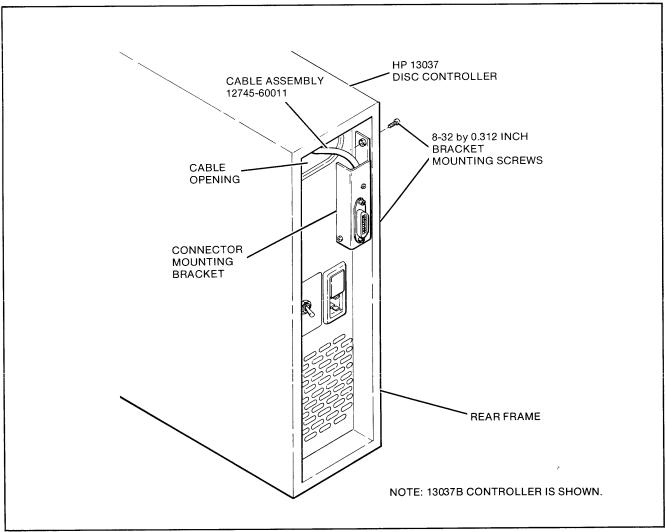
- Error Correct PCA.
- Device Controller PCA.
- f. If the adapter kit is being installed in an HP 13037B or HP 13037C Disc Controller, proceed to step p, otherwise proceed to step g.
- g. Disconnect the cable bracket assembly from the rear of the HP 13037D Disc Controller (see figure 2-2) and carefully pull the attached multi-unit and data cables back through the opening about 8 to 10 inches.
- Separate the two cable brackets (see figure 2-2, view A).
- i. Locate and completely remove the clear piece of shrink tubing located near the HP-IB connector end of the 12745-60011 Cable Assembly to expose the small area of shield braid. Use extreme care to prevent damaging the cable.
- j. Locate the package of hardware attached to the cable assembly. The package includes the following:
  - (1) Two 6-32 nuts, part no. 2420-0003.
  - (2) Two 6-32 by 0.312 in. screws, part no. 2360-0182.
  - (3) One clamp, part no. 5021-1603.
  - (4) One clamp, part no. 5021-1604.
  - (5) Two 6-32 by 1.25 in. screws, part no. 2360-0242.
  - (6) Two 8-32 by 0.312 in. screws, part no. 2510-0043. The screws are used if the kit is used in earlier versions of the disc controller and may be discarded when installing the kit in an HP 13037D Disc Controller.
- k. Mount the hardware on the 12745-60011 Cable Assembly oriented as shown in figure 2-2, view A. Make sure that the 5021-1604 clamp makes firm contact with the exposed shield braid.
- Attach the data cable bracket to the main cable bracket with the two attached captive screws.
- m. Carefully pull the cables toward the front of the controller and secure the cable bracket assembly to the controller with the two attached captive screws.
- n. Position the cables in the channel provided and lying to the right of the fan.
- o. Secure the 12745-60011 Cable Assembly to the rear panel of the controller with the two 6-32 by 1.25 in. screws (see figure 2-2). Then proceed to step t.

- p. Locate the package of hardware attached to the 12745-60011 Cable Assembly. Discard all of the parts except the two 8-32 by 0.312 in. screws, part no. 2510-0043.
- q. Remove the bottom cover of the controller.
- r. Install cable assembly 12745-60011 in the controller as follows. See figure 2-3 for installation details.
  - (1) Place the controller on its side.
  - (2) From the front of the controller, feed the 24-pin connector end of cable assembly 12745-60011 through the opening in the rear panel of the controller.
  - (3) Align the connector mounting bracket with the two holes in the rear frame of the controller and attach the bracket to the frame with the two 8-32 by 0.312 in. screws from the package in step p.
- Replace the bottom cover of the controller and proceed to step t.
- t. Refer to figure 2-4 and replace the PCA's removed in step e as follows:

CONTROLLER SLOT	PCA
3	Device Controller
4	Error Correct
5	Microprocessor

- u. Connect jumper cable 13037-60021 between the center printed-circuit connectors (J2) on the error correct PCA and the microprocessor PCA.
- v. Install the adapter kit PCA in slot 1 of the controller.
- w. Connect flat cable assembly 12745-60004 between the left-hand printed-circuit connectors (J1) on the adapter kit PCA and the device controller PCA.
- x. Connect the plug on the end of cable assembly 12745-60011 to the right-hand printed-circuit connector (J3) on the adapter kit PCA.
- y. Ensure that all of the system cables are correctly installed and replace the top cover.
- z. Reinstall the controller in the system cabinet following in reverse order the instructions given in step d.
- aa. Set the CPU number and HP-IB address thumbwheel switches on the adapter kit PCA (see figure 3-1). Then replace the controller front panel.
- bb. Reconnect the power cord to the rear panel of the controller.

12745 Installation



7313-5B

Figure 2-3. Cable Assembly (12745-60011) Installation in HP 13037B or HP 13037C

#### 2-8. CONNECTION TO HP-IB

#### CAUTION

The HP 12745D uses a short data settling time. To assure data integrity, limit total cable length of any bus including the HP 12745D to one metre per equivalent load connected (maximum 15 metres). The length in metres equals the sum of the equivalent loads. The equivalent load of the HP 12745D is 1. The length of cable assembly, part no. 12745-60011 (0.9 metre), and the equivalent load of the controller-in-command must be included in the calculation of total cable length.

The 24-pin connector installed on the rear frame of the controller provides the interface to the HP-IB. Use the HP 10833B HP-IB Interface Cable (part no. 8120-3446) to connect the controller to the HP-IB. Pin connections for the HP-IB connector are shown in figure 2-5.

#### 2-9. PERFORMANCE CHECK

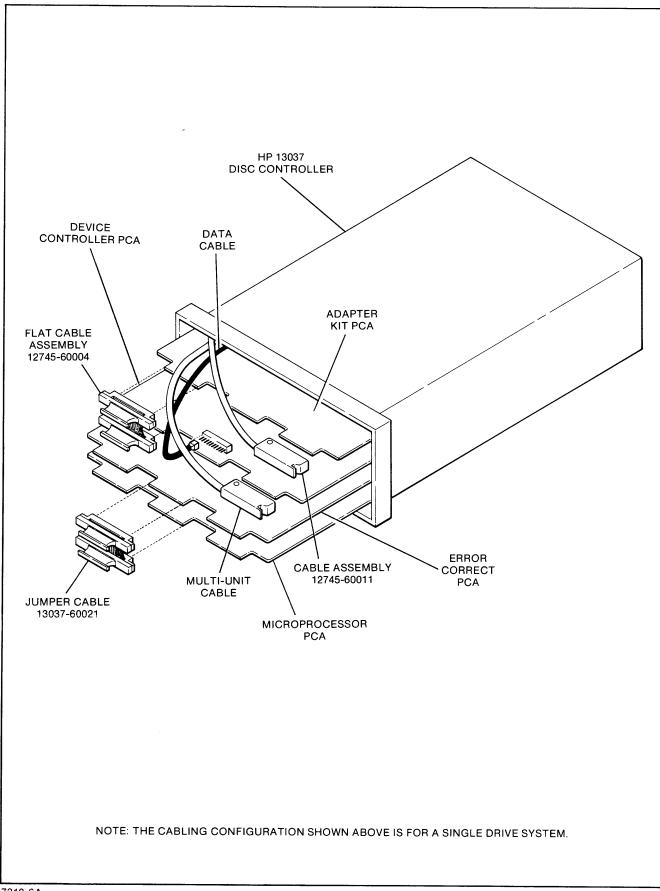
To verify proper operation of the adapter kit requires the use of a diagnostic test program. Refer to the documentation supplied with the diagnostic for loading and operating instructions. In addition, the user should refer to section III of this manual for information regarding the controls and indicators on the adapter kit PCA and details of the HP-IB instruction set.

#### 2-10. REPACKAGING FOR SHIPMENT

The following paragraphs provide instructions for repackaging the adapter kit for shipment. Included are instructions for shipping the kit using the original packaging or new packaging.

# 2-11. SHIPMENT USING ORIGINAL PACKAGING

The same containers and materials used in factory packaging can be used for reshipment of the kit. Alternatively, the correct containers and packing materials



7313-6A

Figure 2-4. HP 12745D Installation Details, Single Drive System

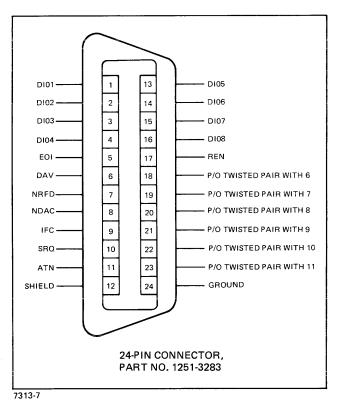


Figure 2-5. Pin Connections for Cable Assembly (12745-60011) HP-IB Connector

may be obtained from Hewlett-Packard Sales and Support Offices. Use the following instructions as a guide when packaging the kit with the original factory packaging materials.

- If any part of the kit is being sent to Hewlett-Packard for servicing, attach a tag specifying the return address, type of service or repair required, and model number.
- Seal the shipping container securely and mark it "FRAGILE" to ensure careful handling.
- In any subsequent correspondence with Hewlett-Packard, refer to the kit by model number.

### 2-12. SHIPMENT USING NEW PACKAGING

The following instructions should be used as a guide when packaging the kit with commercially available materials.

- Wrap the components in heavy paper or sheet plastic. If the components are being sent to Hewlett-Packard for servicing, attach tags specifying the return address, type of servicing or repair required, and model number.
- Use a strong shipping carton. A double-wall carton constructed of 158.9-kilogram (350-pound) test material is adequate.
- Use sufficient shock-absorbing material to provide a firm cushion and to prevent movement inside the container.
- Seal the shipping container securely and mark it "FRAGILE" to ensure careful handling.
- In any subsequent correspondence with Hewlett-Packard, refer to the kit by model number.

# **OPERATION AND PROGRAMMING**

SECTION

#### 3-1. INTRODUCTION

This section provides operating instructions and software requirements for the HP 12745D Adapter Kit. Included are a description of the adapter kit PCA controls and indicators, and details of the software required to operate a 13037-interfaced disc drive via the HP-IB.

#### 3-2. CONTROLS AND INDICATORS

Thumbwheel switches S1 and S2, mounted on the edge of the adapter kit PCA, require setting before the HP 12745D is placed in operation. See figure 3-1 for the location and function of these switches. An assembly of five LED's mounted adjacent to switch S2 indicates the operational status of the PCA. The readout function of each LED is described in figure 3-1.

#### 3-3. SOFTWARE REQUIREMENTS

The information provided in the following paragraphs describes the software required to operate a 13037-interfaced disc drive via the Hewlett-Packard Interface Bus (HP-IB). The primary intent of the description is to provide a brief explanation of the various commands executed by the HP-IB-controller system and to show how they are presented over the HP-IB. For a complete description of the HP 13037 instruction set, refer to the HP 13037D Disc Controller Installation and Service Manual, part no. 13037-90911.

The operations are arranged in four categories as follows:

- Sense operations which detect the state of the controller and the disc drive.
- Control operations in which the controller and/or disc drive is modified.
- Write operations which record information on the media.
- Read operations which retrieve data from the media.

The commands that make up each category are described in paragraphs 3-4 through 3-38. Included in the description of each command is the HP-IB sequence necessary to implement the command. An explanation of the abbreviations used in the descriptions together with the required coding, where applicable, are detailed in table 3-1.

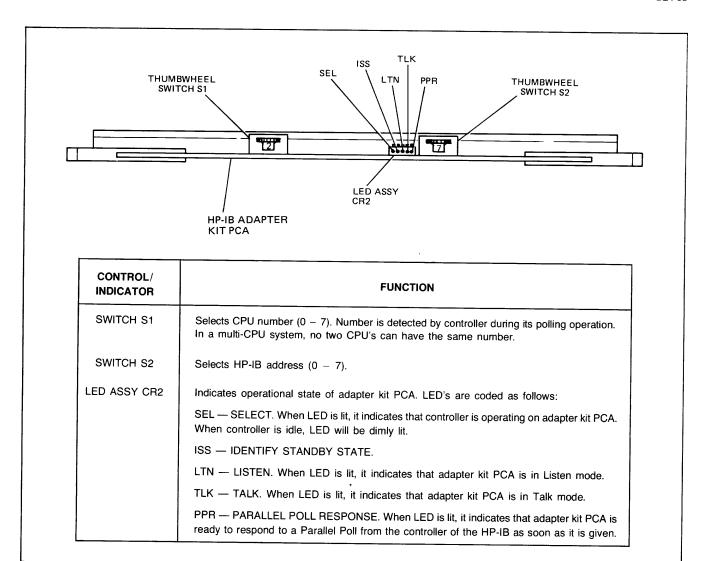
Note: In the command descriptions, "subsystem" refers to the group of components comprising the user's 13037-interfaced disc drive(s).

All commands are executed as described, with the following exceptions:

- When a power on or a momentary power interruption occurs to the controller power supply, a command hold-off condition will result in which:
  - (1) All disc commands and data to be written are ignored. However, there is a handshake across the HP-IB.
  - (2) All requests for data or status from the disc drive are answered by sending one byte tagged with EOI.
  - (3) The identify command executes normally.
  - (4) DSJ will execute normally giving a value of 2 to indicate to the bus controller the power up condition.
  - (5) Universal clear, hard clear, or DSJ request will take the HP-IB interface out of the hold-off condition.

The hold-off condition is included to avoid any erroneous operation following a power interruption.

• If the bus controller attempts to address a disc drive that is reserved by another CPU, the operation will indicate that the unit is "unavailable". The unit is reserved by setting the "hold" bit (H) to 1.



7313-8

Figure 3-1. Adapter Kit PCA (12745-60010) Controls and Indicators

Table 3-1. HP-IB Command Set Abbreviations and Coding

ATN DEV. CLR DEV. CLR DISP DISP Displacement of error correction patterns. DON'T C DON'T C DON'T C DON'T CATE LOT Attention line false, EOI true, end of data. Encoded head — sector to be cold loaded from. ID1 Identification byte 1. ID2 Identification byte 2. LCOUNT Least significant byte of sector count. LCYL Least significant byte of cylinder address. LEAST Significant byte of of status 2. BYTE CONTONING OPERATION OF CONTONING MOOUNT MOST Significant byte of sector count. MOYL Most significant byte of vorid displacement. MOST Significant byte of overd displacement. MOST Significant byte of overd displacement. MOST Significant byte of status 2. PATT MOST Significant byte of status 2. PATT Error correction pattern to be used. PCG Primary command group.  PPR Attention line true, EOI true — parallel poll response PRI. LTN Primary listen. PRI. TLK Primary listen. PRI. TLK Primary talk. PXXXXXXX HP-IB parity bit. Ignored by 12745D. SEC. CLR Secondary device specified jump. SEC. OP1 Secondary opcode type 1. SEC. OP2 Secondary opcode type 2. SEC. OP3 Secondary opcode type 3. SEC. RPL Secondary read back loop. SEC. RSTA Secondary read back loop. SEC. RSTA Secondary write data. SEC. WDAT Secondary write data. SEC. WDAT Secondary write loopback. SI Status 1 information. UNIT UNLISTEN Unlisten.	CODE
DEV. CLR DISP DISP DISP Displacement of error correction patterns. DON'T C DSJ Device specified jump.  EOT Attention line false, EOI true, end of data. HD-S ID1 ID2 LGOUNT LCYL LEAST significant byte of sector count. LCYL LEAST significant byte of view displacement. LPATT1-3 LEAST significant byte of correction pattern. LS2 MASK MCOUNT MCYL MDISP MOST significant byte of sector count. MCYL MDISP MOST significant byte of found displacement. MOST significant byte of found displacement. MOST significant byte of sector count. MOYL MOST significant byte of sector count. MOST significant byte of correction pattern. MSA MSS significant byte of sector count. MOST significant byte of ord displacement. MOST significant byte of sector count. MOST significant byte of ord displacement. MOST significant byte of ord displacement. MOST significant byte of word displacement. MOST significant byte of status 2. PATT PCG PATT PCG PTIMED PRICE	
DON'T C DSJ EOT Attention line false, EOI true, end of data. HD-S Encoded head — sector to be cold loaded from. ID1 Identification byte 1. ID2 LCOUNT LCYL Least significant byte of sector count. LCYL LEAST significant byte of word displacement. LPATT1-3 LS2 MASK Byte controlling operation of controller. MCOUNT MCVL MDISP MOST significant byte of sector count. MOST significant byte of word displacement. MPATT1-3 MSA MSS MSS MSS MSS MSS MOST significant byte of status 2. Error correction pattern to be used. PCG Primary command group.  PPR Attention line true, EOI true — parallel poll response Primary listen. PRI. LLK Primary talk. Primary talk. Primary talk. PSEC. OP1 Secondary device specified jump. SEC. OP1 Secondary opcode type 1. SEC. OP2 SEC. OP3 SEC. RDAT Secondary opcode type 2. SEC. OP3 SEC. RDAT Secondary read data. SEC. RPL Secondary read back loop. SEC. RSTA Secondary write loopback. S1 UNIT Drive unit (0-7) to which command applies.	P0000100
DSJ Device specified jump.  Attention line false, EOI true, end of data.  Encoded head — sector to be cold loaded from.  ID1 ID2 Identification byte 1.  ID2 Least significant byte of sector count.  LCYL Least significant byte of word displacement.  LPATT1-3 Least significant byte of sector count.  LCYL Least significant byte of word displacement.  LPATT1-3 Least significant byte of correction pattern.  LS2 Byte controlling operation of controller.  MCOUNT Most significant byte of sector count.  MCYL Most significant byte of cylinder address.  MDISP Most significant byte of word displacement.  MPATT1-3 Most significant byte of cylinder address.  MS2 Most significant byte of correction pattern.  MSA My secondary address.  MS2 Most significant byte of status 2.  PATT Error correction pattern to be used.  PCG Primary command group.  PPR Attention line true, EOI true — parallel poll response primary listen.  Primary listen.  Primary talk.  Pxxxxxxx HP-IB parity bit. Ignored by 12745D.  Sec. CLR Secondary device specified jump.  SEC. OP1 Secondary opcode type 1.  SEC. OP2 Secondary opcode type 1.  SEC. OP3 Secondary opcode type 2.  SEC. OP3 Secondary opcode type 2.  SEC. RDAT Secondary read data.  SEC. RPL Secondary request status.  Secondary request status.  SEC. RPL Secondary write data.  SEC. WDAT Secondary write data.  SEC. WDAT Secondary write loopback.  S1 UNIT Drive unit (0-7) to which command applies.	
Attention line false, EOI true, end of data.  HD-S ID1 ID2 LCOUNT LCYL LDISP LPATT1-3 LS2 MASK MCOUNT MCYL MDISP MPATT1-3 MSA MS2 PATT PCG PATT PCG PTR PRILTIN PCG PCS	
HD-S ID1 ID2 ID2 ID3 ID4 ID5 ID5 ID6 ID7 ID7 ID8 ID8 ID9 LCOUNT LCYL LDISP LD8 LD8 LD8 LD8 LD8 LD9 LD8 LD9	
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LCYL LDISP LPATT1-3 Least significant byte of cylinder address. Least significant byte of word displacement. Least significant byte of status 2.  MASK MCOUNT MCYL MOST MOST MOST MPATT1-3 MSA MS2 MASK MS2 MOST MOST MOST MOST MOST MOST MOST MOST	00000010
LDISP LPATT1-3 Least significant byte of word displacement. Least significant bytes of correction pattern. Least significant byte of status 2.  MASK MCOUNT MCYL Most significant byte of sector count. MCYL MDISP Most significant byte of cylinder address. MDISP Most significant byte of word displacement. MPATT1-3 MSA My secondary address. MS2 Most significant byte of status 2. PATT Error correction pattern to be used. PCG PRIL LTN PRIL LTN PRIL TLK Primary listen. PRIL TLK Primary talk. PXXXXXXX SEC. CLR Secondary device specified jump. SEC. OP1 SEC. OP2 Secondary opcode type 1. SEC. OP2 SEC. OP3 SEC. RDAT SEC. RDAT SEC. RDAT SEC. RPL Secondary read data. SEC. RPL Secondary write data. SEC. WLP Secondary write loopback. S1 UNIT Drive unit (0-7) to which command applies.	
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MCOUNT MCYL MOST significant byte of cylinder address. MDISP Most significant byte of word displacement. MPATT1-3 MSA MS2 MOST significant byte of correction pattern. MSA MS2 MOST significant byte of status 2. PATT Error correction pattern to be used. PCG Primary command group.  PPR Attention line true, EOI true — parallel poll response PRI. LTN PRI. LTN PRI. TLK Primary listen. PRI. TLK Primary talk. Pxxxxxxx HP-IB parity bit. Ignored by 12745D. SEC. CLR SEC. DSJ Secondary device specified jump. SEC. OP1 Secondary opcode type 1. SEC. OP2 Secondary opcode type 2. SEC. OP3 Secondary opcode type 3. SEC. RDAT SEC. RPL Secondary read data. SEC. RPL Secondary read back loop. SEC. RSTA Secondary write data. SEC. WLP Secondary write loopback. S1 UNIT Drive unit (0-7) to which command applies.	
MCYL MDISP Most significant byte of cylinder address. MPATT1-3 MSA MS2 Most significant bytes of correction pattern. MS2 Most significant byte of status 2. PATT PCG Primary command group.  PPR Attention line true, EOI true — parallel poll response PRI. LTN PRI. TLK Primary listen. PRI. TLK Primary talk. Pxxxxxxx HP-IB parity bit. Ignored by 12745D. SEC. CLR SEC. DSJ Secondary device specified jump. SEC. OP1 SEC. OP2 Secondary opcode type 1. SEC. OP2 SEC. OP3 Secondary opcode type 2. SEC. RDAT SEC. RPL SEC. RPL SEC. RSTA SEC. RSTA SEC. WDAT SEC. WLP Secondary write data. SEC. WLP Secondary write loopback. S1 UNIT  Most significant byte of word displacement.  Most significant byte of word displacement.  Most significant byte of word displacement.  Most significant byte of correction pattern.  Most significant byte of status 2.  Error correction pattern.  Most significant byte of status 2.  Error correction pattern.  Most significant byte of status 2.  Error correction patter.  Primary listen.  Primar	
MDISP MPATT1-3 MSA MS2 MS2 Most significant bytes of correction pattern. MSA MS2 Most significant byte of status 2.  PATT PCG PFIMATY PRIL LTN PRIL TLK Primary talk. Pxxxxxxx HP-IB parity bit. Ignored by 12745D. SEC. CLR SEC. DSJ SEC. OP1 SEC. OP1 SEC. OP2 SEC. OP3 SEC. RDAT SEC. RPL SEC. RPL SEC. RSTA SEC. WLP SEC. WITH SEC. OP1 SEC. OP2 SEC. WLP SEC. WLP SEC. WITH SEC. WLP SEC. WITH Most significant byte of word displacement. Mysecondary address.  Mysecondary address.  Mysecondary address.  Mysecondary address.  Most significant byte of word displacement. Most significant byte of word displacement. Mysecondary address.  Mysecondary address.  Mysecondary status 2.  Error correction pattern.  By secondary bit used. Secondary opened by 12745D.	
MPATT1-3 MSA MS2 MS2 PATT PCG PR RIL LTN PRIL TLK Pxxxxxxx SEC. DSJ SEC. OP1 SEC. OP2 SEC. OP3 SEC. RDAT SEC. RPL SEC. RSTA SEC. RSTA SEC. WLP Most significant bytes of correction pattern. My secondary address. My secondary address. My secondary address. My secondary elears. SEC It ue — parallel poll response primary listen. Primary listen. Primary listen. Primary talk. HP-IB parity bit. Ignored by 12745D. Secondary device specified jump. Secondary device specified jump. Secondary opcode type 1. Secondary opcode type 2. Secondary opcode type 3. Secondary read data. Secondary read back loop. Secondary write data. Secondary write data. Secondary write loopback. Status 1 information. UNIT Drive unit (0-7) to which command applies.	
MSA My secondary address.  MS2 Most significant byte of status 2.  PATT Error correction pattern to be used.  PCG Primary command group.  Attention line true, EOI true — parallel poll response PRI. LTN Primary listen.  PRI. TLK Primary talk.  Pxxxxxxx HP-IB parity bit. Ignored by 12745D.  SEC. CLR Secondary clear.  SEC. DSJ Secondary device specified jump.  SEC. OP1 Secondary opcode type 1.  SEC. OP2 Secondary opcode type 2.  SEC. OP3 Secondary opcode type 3.  SEC. RDAT Secondary read data.  SEC. RPL Secondary read back loop.  SEC. RSTA Secondary write data.  SEC. WDAT Secondary write data.  SEC. WLP Secondary write loopback.  S1 Status 1 information.  UNIT Drive unit (0-7) to which command applies.	
MS2 PATT PCG PTT PCG PTIMARY COMMAND ATTERING AND ADDRESS OF SEC. OP2 SEC. OP2 SEC. OP3 SEC. RDAT SEC. RPL SEC. RSTA SEC. WLP SEC. WLP SI SEC. WLP SI SEC. WLP SI SEC. WLP SEC. COR SECRET CORRECTED STAT SECONDARY OF SECUNDARY OF	
PATT PCG Primary command group.  Attention line true, EOI true — parallel poll response PRI. LTN PRI. TLK Primary listen. Primary talk. Pxxxxxxx HP-IB parity bit. Ignored by 12745D. SEC. CLR SEC. DSJ Secondary clear. SEC. OP1 SEC. OP2 SEC. OP2 SEC. OP3 SEC. OP3 SEC. RDAT SEC. RDAT SEC. RPL SEC. RSTA SEC. WDAT SEC. WLP SEC. WLP SEC. WLP SEC. WINT SEC. WIN	P11 Address
PCG Primary command group.  Attention line true, EOI true — parallel poll response PRI. LTN Primary listen.  PRI. TLK Primary talk.  Pxxxxxxx HP-IB parity bit. Ignored by 12745D.  SEC. CLR Secondary clear.  SEC. DSJ Secondary device specified jump.  SEC. OP1 Secondary opcode type 1.  SEC. OP2 Secondary opcode type 2.  SEC. OP3 Secondary opcode type 3.  SEC. RDAT Secondary read data.  SEC. RPL Secondary read back loop.  SEC. RSTA Secondary write data.  SEC. WDAT Secondary write data.  SEC. WLP Secondary write loopback.  S1 Status 1 information.  UNIT Drive unit (0-7) to which command applies.	
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Pxxxxxxx HP-IB parity bit. Ignored by 12745D.  SEC. CLR Secondary clear.  SEC. DSJ Secondary device specified jump.  SEC. OP1 Secondary opcode type 1.  SEC. OP2 Secondary opcode type 2.  SEC. OP3 Secondary opcode type 3.  SEC. RDAT Secondary read data.  SEC. RPL Secondary read back loop.  SEC. RSTA Secondary request status.  SEC. WDAT Secondary write data.  SEC. WLP Secondary write loopback.  S1 Status 1 information.  UNIT Drive unit (0-7) to which command applies.	P01 Address
SEC. CLR SEC. DSJ Secondary device specified jump. SEC. OP1 SEC. OP2 SEC. OP3 SEC. RDAT SEC. RPL SEC. RPL SEC. RSTA SEC. RSTA SEC. WDAT SEC. WLP SE	P10 Address
SEC. DSJ SEC. OP1 SEC. OP2 SEC. OP3 SEC. RDAT SEC. RPL SEC. RSTA SEC. WDAT SEC. WLP	
SEC. OP1 SEC. OP2 SEC. OP3 SEC. RDAT SEC. RDAT SEC. RPL SEC. RSTA SEC. RSTA SEC. WDAT SEC. WLP SEC. WL	P1110000
SEC. OP2 SEC. OP3 SEC. RDAT SEC. RPL SEC. RSTA SEC. WDAT SEC. WLP	P1110000
SEC. OP3 SEC. RDAT SEC. RPL SEC. RSTA SEC. WDAT SEC. WLP SEC. WLP SEC. WLP Secondary read back loop. Secondary request status. Secondary write data. Secondary write loopback. Status 1 information. UNIT Drive unit (0-7) to which command applies.	P1101000
SEC. RDAT SEC. RPL Secondary read data. SEC. RSTA SEC. WDAT SEC. WLP SEC. WLP Secondary write data. SEC. WLP Secondary write loopback. S1 Status 1 information. UNIT Drive unit (0-7) to which command applies.	P1101001
SEC. RPL SEC. RSTA SEC. WDAT SEC. WLP SEC. WLP Secondary read back loop. Secondary request status. Secondary write data. Secondary write loopback. Status 1 information. UNIT Drive unit (0-7) to which command applies.	P1101010
SEC. RSTA SEC. WDAT SEC. WLP Secondary write data. SEC. WLP Secondary write loopback. Status 1 information. UNIT Drive unit (0-7) to which command applies.	P1100000
SEC. WDAT SEC. WLP Secondary write data. SEC. WLP S1 Secondary write loopback. Status 1 information. UNIT Drive unit (0-7) to which command applies.	P1111110
SEC. WLP Secondary write loopback.  S1 Status 1 information.  UNIT Drive unit (0-7) to which command applies.	P1101000
S1 Status 1 information.  UNIT Drive unit (0-7) to which command applies.	P1100000
UNIT Drive unit (0-7) to which command applies.	P1111110
	P0111111
UNTALK Untalk.	P1011111
UNV. CLR Universal clear.	P0010100

#### 3-4. SENSE OPERATIONS

#### 3-5. DEVICE SPECIFIED JUMP



To obtain a quick indicator that is useful in software branching.

#### **HP-IB SEQUENCE**

(ATN) (ATN) (EOT) (ATN)

PRI. TLK SEC. DSJ DSJ BYTE UNTALK

PPR IS UNAFFECTED

#### RESULT

When requested, one byte is sourced by the adapter kit PCA. In general, the values are:

00H-A request will show S1 field = 0H. Indicates normal completion.

01H — A status request will show S1 field  $\neq$  0H. Success or failure of operation depends on expected status. Full status request may be necessary.

02H — Power on has occurred since last DSJ or hard clear. Retry all operations.

#### 3-6. IDENTIFY

#### **PURPOSE**

To uniquely identify the HP-IB peripheral as a 13037 controller.

#### **HP-IB SEQUENCE**

 (ATN)
 (EOT)
 (ATN)

 UNTALK
 MSA
 1D1
 1D2
 PCG

 PPR IS UNAFFECTED

RESULT

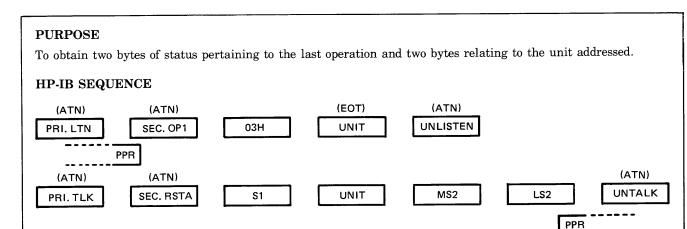
The adapter kit PCA will source two bytes over the HP-IB.

First byte = 00H

Second byte = 02H

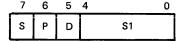
Status and DSJ are not affected.

#### 3-7. REQUEST STATUS



#### RESULT

a. First byte received:



S = 1 indicates a spare track

P = 1 indicates a protected track

D = 1 indicates a defective track

S1 indicates:

- 00H Normal Completion. This status is transmitted in one of two situations:
  - (1) When command has been fully executed without error.
  - (2) At completion of a REQUEST STATUS operation whenever the operation immediately follows another REQUEST STATUS operation or when it is the first operation issued after CPU is selected. For the latter case, the U field will be zero.
- 01H Illegal Opcode. Operation has been received by the controller which contains an operation code which is not one of the controller's command set.
- 02H Unit Available. Controller transmits this status after a WAKEUP operation for a specific unit and that unit has become available.
- 07H Cylinder Compare Error. During verification of address of sector previous to first sector to be read from or written to, the contents of cylinder address field of that sector do not match contents of controller's cylinder address register. This status is transmitted only after the sequence of events listed below. When this status is received, the system should issue a Recalibrate operation and then retry data transfer sequence.
  - (1) Addresses do not compare as described below.
  - (2) Controller generates a seek to address in its cylinder address register and head sector address register.
  - (3) Controller again attempts to verify a sector.
  - (4) Addresses still do not compare.
  - (5) The S Bit is not set at new track address.

- 08H Uncorrectable Data Error. This status is generated by the error correction circuits and is transmitted in one of three cases:
  - (1) Immediately following a data transfer (or VERIFY) command if error is uncorrectable.
  - (2) In response to a REQUEST SYNDROME OPERATION whenever a Possibly Correctable Data Error has proved uncorrectable. U field will be zero.
  - (3) During verification of address of sector previous to first sector to be read from or written to, controller is unable to read (verify) any of 16 consecutive sectors without error.
- 09H Head-Sector Compare Error. Similar to Cylinder Compare Error, including controller's recovery attempt sequence described for that status, except that head and/or sector address field of disc sector does not compare with corresponding field in controller's head sector address register. The system need not issue a RECALIBRATE OPERATION when this status is received.
- 0AH I/O Program Error. Indicates that an illegal HP-IB secondary has been received.
- OCH End of Cylinder. A multiple-sector data transfer must continue beyond end-of-logical-cylinder, but file mask will not allow controller to automatically seek to next logical cylinder and continue.
- 0EH Overrun. Detected by adapter kit PCA whenever instantaneous data rate of controller exceeds that of HP-IB. The overrun is reported at end of sector in which it occurred. The contents of that sector, either on disc (write) or in I/O buffer (read), should be considered invalid.
- 0FH Possibly Correctable Data Error. This status is generated by the error correction circuits and is transmitted in one of two cases:
  - (1) Immediately following a data transfer (or VERIFY) operation if error is possibly correctable.
  - (2) In response to a REQUEST SYNDROME operation if error is in fact correctable. The U field will be zero. In this case, proceed as described in REQUEST SYNDROME operation.
- 10H Illegal Access to Spare Track. The same conditions and sequence of events described for a Cylinder Compare Error or Head-Sector Compare Error have occurred, except that S Bit is set at new track address. This error usually results from trying to directly access (via a SEEK command) a spare track in active use. The addresses will not compare because of the way in which spare tracks are set up and this status merely differentiates between this situation and other address errors.
- 11H Defective Track. During verification of track status of sector previous to first sector to be read from or written to, the D Bit is found to be set but File Mask will not allow automatic seeking to a spare track.
- 12H Access Not Ready During Data Operation. While in process of transferring data to or from disc, the track center detector in drive detected head motion. The transfer should be retried.
- 13H Status-2 Error. The controller is unable to complete an operation due to some condition in disc drive. The Status-2 byte may be examined for reason. Examples of Status-2 Errors are:
  - (1) An Initialize Operation, but Format switch is off or Protected switch is on.
  - (2) An operation is issued to a drive which is Not Ready (heads unloaded) or for which a Drive Fault has occurred.
- 16H Attempt to Write on Protected Track. During verification of track status of sector previous to first sector to be written to using a Write operation, the P Bit is found to be set and the Format switch is off.

- 17H Unit Unavailable. This status is returned in two cases:
  - (1) A CPU has requested a Unit whose hold bit has been set by another CPU.
  - (2) The U field of the operation is greater than 12 (octal).

Note: This status is not set for REQUEST SECTOR ADDRESS operation whether unit is held by another CPU or not. This is because the operation only accesses the "current sector" counter in disc drive without changing any operating parameter of drive or controller.

1FH — Drive Attention. Controller sends status of an interrupt to CPU which last accessed the unit requesting (or CPU 0 if this is first interrupt after power-on or hard clear).

Conditions causing a unit to request an interrupt to the disc controller and set the drive attention status include:

- Seek completion
- Drive becomes ready (heads load)
- Drive becomes not ready (heads unload)
- Seek check
- Drive fault
- b. The second byte returned contains the unit for which the last operation applies. If S1 is equal to 1FH, the second byte contains the number of the interrupting unit.

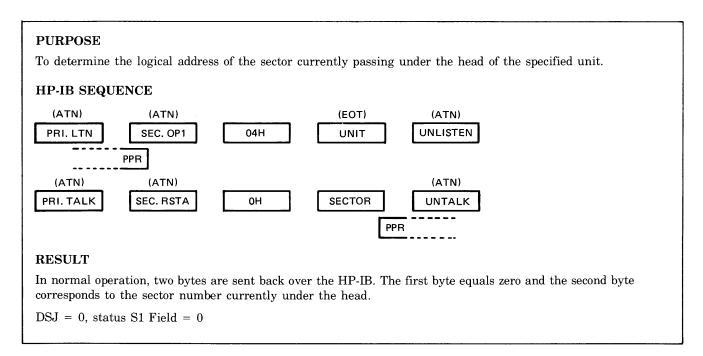
The third and fourth bytes contain status pertaining to the unit requested. Note that these two bytes do not necessarily reflect the same unit indicated by the second byte returned in a multi-unit subsystem.

- c. The third byte contains the following bit encoded status:
  - Bit 8 True if any bit marked \* is true in byte 4.
  - Bit 7-2 Unit identifying number, the following codes have been reserved:

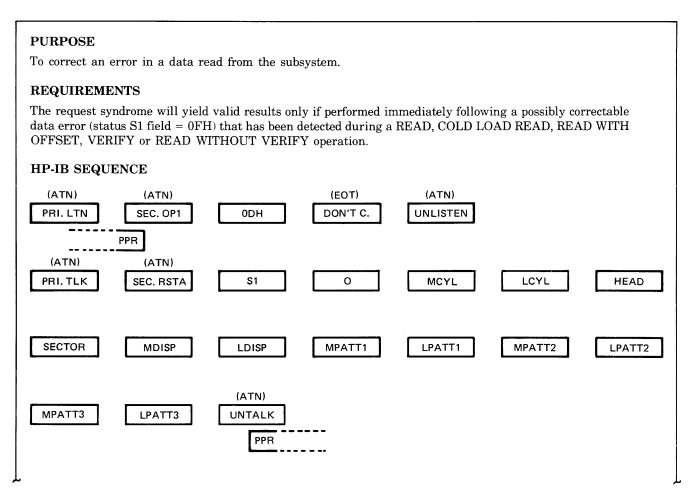
Bit Number 7 6 5 4 3 2 7906 0 0 0 0 0 0 0 7920 0 0 0 0 0 1 Bit 1 Reserved

- d. The fourth byte contains the following bit encoded status:
  - Bit 8 Attention B17 set if unit is requesting an interrupt (S1 = 01F).
  - Bit 7 Protect switch set on surface which is currently addressed.
  - Bit 6 Format switch on unit is on.
  - Bit 5\* Drive fault on unit.
  - Bit 4 First status operation to this unit since the last head load.
  - Bit 3\* Seek check hardware seek failure within unit occurred.
  - Bit 2-1\* Unit ready indication. These bits are encoded in the following manner:
    - 00 Normal unit available
    - 01 Unit busy
    - 10 Unit not present or power off
    - 11 Unit present heads not loaded

#### 3-8. REQUEST SECTOR ADDRESS



#### 3-9. REQUEST SYNDROME



#### RESULT

In normal operation the subsystem returns 14 bytes. The first byte indicates the status resulting from the error correction algorithm. If equal to 0FH, the error is correctable. Uncorrectable errors give a status of 08H. The second byte is null. Bytes 3 and 4 are linked together to indicate the cylinder, Byte 5 the head, and Byte 6 the sector in which the error occurred. Bytes 7 and 8 form a bit word that indicates the beginning word within the sector where the first bit error occurred. Since the first 16 bit data word is numbered zero, the displacement (Bytes 7 and 8) should be added to the CPU's Data Buffer address of sector to obtain the first word to be corrected. If the displacement is negative or greater than 125, the error occurred during either the preamble or postamble and should not be corrected. In addition, if a full sector was not transferred, the CPU must check to ensure that displacement is within buffer. Bytes 9 through 14 are combined to form three 16-bit correction words. One correction word is "exclusive or'd" with one data word, starting with the first correction word and the data word determined by the displacement. This operation will correct the errors.

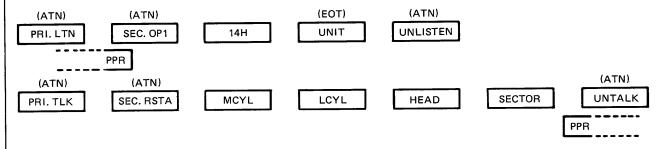
DSJ = 0 following normal completion.

#### 3-10. REQUEST DISC ADDRESS

#### **PURPOSE**

To obtain the current logic address being used by the controller. The operation may be used at any time but is generally used following any data transfer or verify operation which aborted with an error. The logical address returned will point to the logical address at which the error occurred.

#### **HP-IB SEQUENCE**



#### RESULT

The subsystem returns four bytes. Bytes 1 and 2 contain the logical cylinder address. Byte 3 contains the logical head address. Byte 4 contains the logical sector address. The operation will terminate immediately once all bytes have been transferred. DSJ byte will be set to 00H.

#### 3-11. LOOPBACK

#### **PURPOSE**

To verify that the HP-IB cabling and the read-write buffers of the adapter kit PCA are operating correctly.

#### REQUIREMENTS

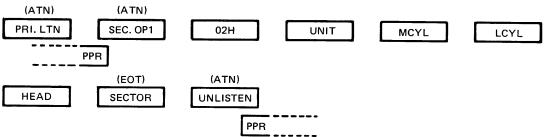
Data must be transferred to the adapter kit PCA following the appropriate HP-IB commands. No more than 512 bytes can be sent.

#### **HP-IB SEQUENCE** (ATN) (ATN) (EOT) (ATN) PRI. LTN SEC. WLP DATA DATA DATA DATA UNLISTEN **PPR PPR** (ATN) (ATN) (EOT) (ATN) PRI. TLK SEC. RLP DATA DATA DATA DATA UNTALK PPR RESULT Upon sending the HP-IB loopback read commands, the adapter kit PCA will source the data originally sent by the CPU. DSJ or STATUS will not be affected.

#### 3-12. CONTROL OPERATIONS

#### 3-13. SEEK

# PURPOSE To position the heads on a unit to the desired physical address. The physical address is stored in controller memory so that subsequent data transfers originate at that location. HP-IB SEQUENCE



#### RESULT

In normal operation the heads are moved to the physical address on the desired unit. The operation will terminate (parallel poll response enabled) as soon as the heads arrive on the target cylinder.

If the REQUEST STATUS operation is performing immediately at the termination of the seek operation, the S1 field will be set to 01FH, the DSJ byte will be set to 01H.

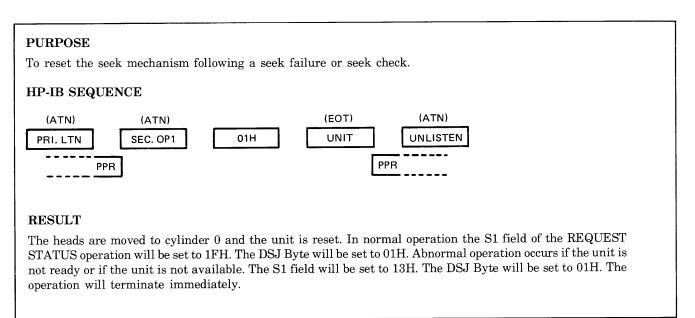
Abnormal operation occurs if the unit is not ready or if the unit is not available. The S1 field will be set to 13H. The DSJ Byte will be set to 01H. The operation will terminate immediately.

A seek failure can occur because of the following reasons:

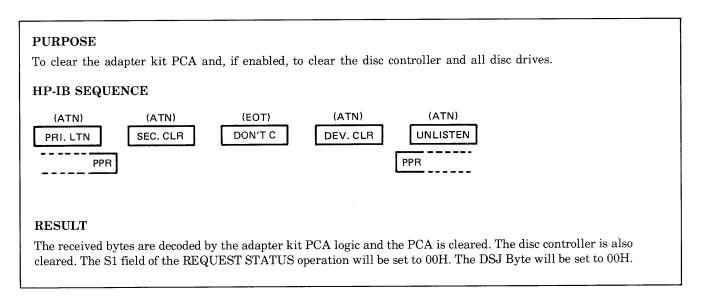
- Failure of the seek mechanism (seek check)
- Correct cylinder cannot be found or is out of bounds (cylinder miscompare)
- Correct head-sector address cannot be found or is out of bounds (head-sector miscompare)

Only the seek check will be reported in the S2 word if the status operation immediately follows the seek operation. The cylinder miscompare and the head-sector miscompare status will be updated during any data access operation following the seek operation.

#### 3-14. RECALIBRATE



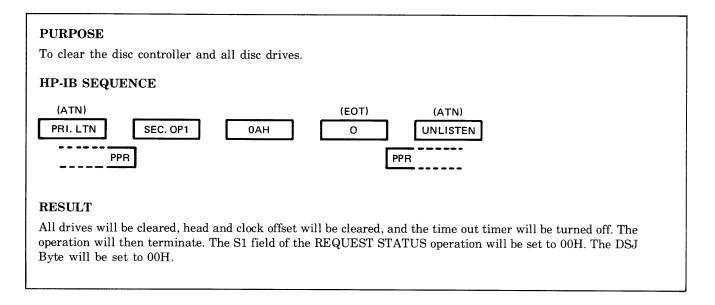
#### 3-15. HARD CLEAR



#### 3-16. UNIVERSAL CLEAR

# PURPOSE A command in the HP-IB protocol that sets all HP-IB devices to a known state. HP-IB SEQUENCE (ATN) UNV. CLR PPR RESULT Same as HARD CLEAR. (Refer to paragraph 3-15.)

#### 3-17. CLEAR

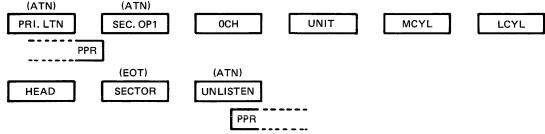


#### 3-18. ADDRESS RECORD

#### **PURPOSE**

To set a logical address in the disc controller without transmitting it to a unit. This command is used during the sparing procedure to record the target address on a defective track. In multi-CPU systems this operation is used to restore a logical address whenever another CPU might have accessed the controller (such as during a SEEK or RECALIBRATE operation).

#### **HP-IB SEQUENCE**



#### RESULT

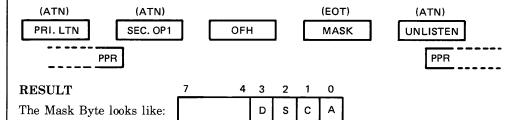
The four bytes are recorded in the controller address register. The operation will then terminate. The S1 field will be set to 00H. The DSJ Byte will be set to 00H.

#### 3-19. SET FILE MASK

#### **PURPOSE**

To set the mode of operation for the disc subsystem. This operation determines if cylinder mode, surface mode, sparing or auto-seek is enabled.

#### **HP-IB SEQUENCE**



The D, S, C, and A Mask Bits are stored in the controller for later reference. These four bits have the following meaning in the mask:

- A Bit Enables an automatic seek at the end of logical cylinder. An incremental or decremental seek is determined by the D Bit of the mask.
- C Bit Enables cylinder mode if set. A logical cylinder consists of all available surfaces. End of logical cylinder occurs when last sector on last surface has been transferred.

Enables surface mode if not set. A logical surface consists only of one surface. End of logical cylinder occurs when last sector on surface has been transferred.

- S Bit If set, allows automatic seek to spare track.
- D Bit This bit is referred to only if the A Bit is set. If the D Bit is set to 1, a decremental seek at the end of logical cylinder will occur. Otherwise, an incremental seek at the end of logical cylinder will occur.

Upon correct termination the S1 field will be set to 00H and DSJ Byte will be set to 00H.

#### 3-20. END



This operation is used to avoid a timeout if no other operation is expected to be sent and the controller is waiting for a command from the currently selected CPU. This operation should follow any string of operations once they have been completed.

#### **HP-IB SEQUENCE**



#### RESULT

The controller is allowed to continue polling and the parallel poll response is disabled.

#### **3-21. WAKEUP**

#### **PURPOSE**

This operation checks if the specified unit is available and not reserved by another CPU in a multi-CPU environment.

#### **HP-IB SEQUENCE**



#### RESULT

The controller checks its internal registers to determine if the unit is reserved by another CPU. If it is not reserved the operation will terminate immediately. The S1 field of the STATUS REQUEST operation will be set to 17H. The DSJ Byte will be set to 01H. If the unit is reserved by another CPU the operation will terminate when that CPU releases the desired unit. The S1 field and DSJ Byte will be updated as described above.

#### 3-22. VERIFY

#### **PURPOSE**

To determine if a data error is present within a specified number of sectors. The controller will perform this check automatically including track boundaries and sparing, if necessary, and enabled.

#### **HP-IB SEQUENCE**



#### RESULT

After verifying that the heads are at the correct logical address (including sparing, if necessary, and enabled), the subsystem begins checking the data and CRC code for each sector starting from the address set.

By the last SEEK operation or ADDRESS RECORD operation, the controller will continue to check data with the CRC code for data errors until either a data error is found or until the requested number of sectors are verified. The operation will then terminate at that point. None of the data verified is transferred. The status words and the DSJ Byte will be updated according to the result of the VERIFY operation.

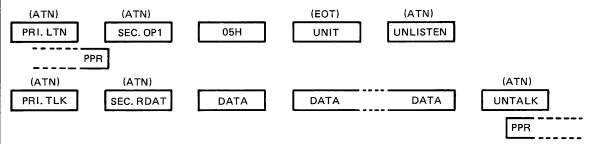
#### 3-23. READ OPERATIONS

#### 3-24. HIGH SPEED READ

#### PURPOSE

Read data from a previously set address to the CPU. This is the normal method of reading data in a high performance computer system (HP-IB bandwidth from 750 kilobytes per second to 1 megabyte per second).

#### **HP-IB SEQUENCE**



#### RESULT

After verifying that the heads are at the correct logical address (including sparing, if necessary, and enabled), the subsystem begins reading from the address set by the last SEEK operation or ADDRESS RECORD operation. The controller continues to transfer 256 bytes per sector until the subsystem is unaddressed to talk. The last sector does not have to be completely transferred. Automatic seeking and sparing will occur, if necessary, and enabled. Once the subsystem is unaddressed to talk, the operation will terminate.

Note: Because the subsystem must assume that the transfer is continuing until it has been notified otherwise by the unaddress command, the length of time needed to unaddress the subsystem becomes important. If too much time is taken, the internal logical address used by the controller will be incremented unnecessarily. This might result in status 1 errors. If the length of time to unaddress cannot be shortened, the REQUEST DISC ADDRESS operation may be used to determine if these errors are included in the data buffer previously read.

Normally the status 1 field will be set to 00H and the DSJ Byte will be set to 00H.

Abnormal operation will result from the occurrence of any one of the following:

- An overrun (I/O system bandwidth insufficient)
- A data error
- A unit error

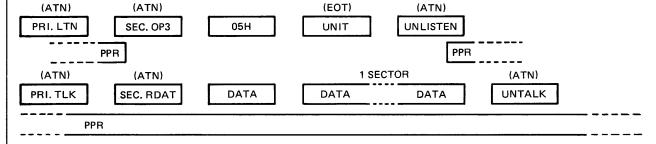
In all cases the transfer will be aborted, a dummy byte will be sent tagged with EOT, and the operation will terminate immediately. The status 1 field will be updated according to the type of error and the DSJ Byte will be set to 01H.

#### 3-25. LOW SPEED READ

#### PURPOSE

To allow reading of data in a low speed (one sector burst) mode. This allows use with a low performance computer or calculator system (HP-IB bandwidth less than 750 kilobytes per second).

#### **HP-IB SEQUENCE**



#### RESULT

The subsystem will read one sector of data from the disc into buffer storage. When this has been performed, a parallel poll response on the HP-IB will be enabled indicating that 256 bytes of data are available. The data is then read from the buffer storage to the CPU. Less than one sector may be transferred if desired. The operation terminates with an "UNTALK" command. Normally the status 1 field will be set to 00H and the DSJ Byte will be set to 00H.

Note:

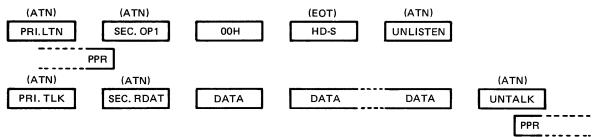
Because only one sector is transferred, the internal logical address used by the controller will be incremented automatically at the end of each LOW SPEED READ operation if no error is encountered. Therefore, only one SEEK operation need be issued at the beginning of a multiple sector transfer when multiple LOW SPEED READ operations are being issued to contiguous sectors.

#### 3-26. COLD LOAD READ

#### **PURPOSE**

The operation will load data into computer main memory using a minimal number of operation bytes.

#### **HP-IB SEQUENCE**

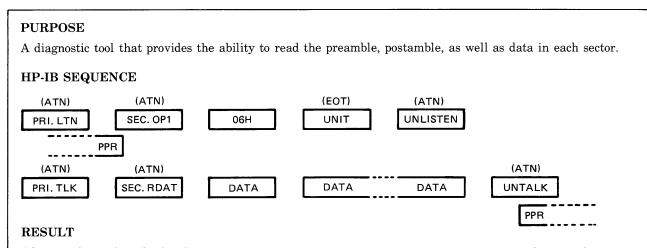


#### RESULT

After using a seek to unit 0, cylinder 0 and the head and sector specified, the controller sets the file mask to sparing enabled, surface mode enables, and no auto seek at end of cylinder enables. The subsystem then begins reading, starting at the specified sector. The subsystem continues to transfer 256 bytes per sector until the "untalk" HP-IB command is sent. The last sector does not have to be completely transferred. Sparing will occur automatically if necessary. Once the subsystem is unaddressed to talk, the operation will terminate. The status S1 field will be set to 00H and the DSJ Byte will be set to 00H.

Abnormal results occur for the same reasons as given for HIGH SPEED READ. (Refer to paragraph 3-24.)

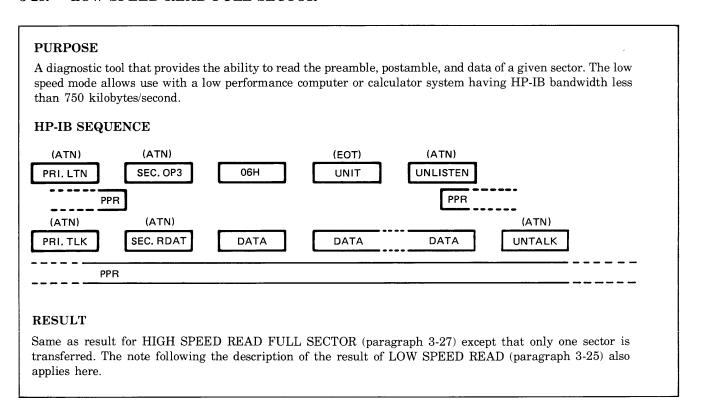
#### 3-27. HIGH SPEED READ FULL SECTOR



After verifying that the heads are at the correct logical address (without sparing), the subsystem begins reading from the address set by the last SEEK operation or ADDRESS RECORD operation. The controller then transfers 276 bytes per sector (sync word, cylinder address, head-sector address, 128 data words, CRC word and 6 ECC words). The controller continues to transfer 276 bytes per sector until the subsystem is unaddressed to talk. The last sector does not have to be completely transferred. Automatic seeking and sparing will occur, if necessary, and enabled. Once the subsystem is unaddressed to talk, the operation will terminate. This operation has the same unaddress restrictions as a HIGH SPEED READ operation. (Refer to paragraph 3-24.)

Normal completion sets DSJ = 00H. Abnormal operation will result for the same reasons as given for HIGH SPEED READ operation (refer to paragraph 3-24) with DSJ set equal to 01H.

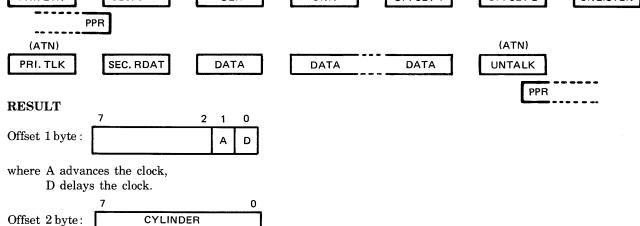
#### 3-28. LOW SPEED READ FULL SECTOR



#### 3-29. HIGH SPEED READ WITH OFFSET

OFFSET

#### **PURPOSE** This operation is used only in error recovery situations when the data must be recovered and normal rereads and the REQUEST SYNDROME operation have failed. In this operation the heads may be moved off track center and the separator clock may be advanced or delayed in order to read data. **HP-IB SEQUENCE** (ATN) (ATN) (EOT) (ATN) PRI. LTN SEC. OP1 OEH UNIT **OFFSET 1** OFFSET 2 UNLISTEN

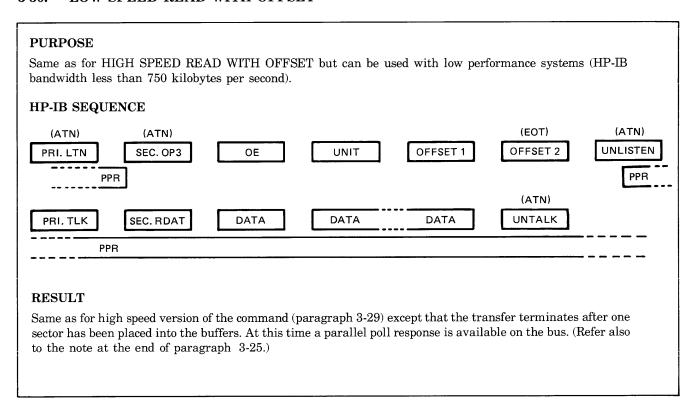


The controller will then transmit the cylinder offset to the desired unit together with the advance or delay ( $\pm 10$  nanoseconds with respect to the data) of the separator clock. A cylinder offset of zero is on the track center. Offset parameters in the range of  $\pm 63$  increments will be executed. Note that negative offset is expressed in two's complement form. Since each offset operation requires a minimum of 1.5 milliseconds to complete, the target sector will have passed under the heads by the time the offset is complete, thus requiring an extra rotation of the disc. After verifying that the heads are at the correct logical address (including sparing, if necessary, and enabled), the subsystem begins reading from the address set by the last SEEK operation or ADDRESS RECORD operation. The controller continues to transfer 256 bytes per sector until the subsystem is unaddressed to talk. The last sector does not have to be completely transferred.

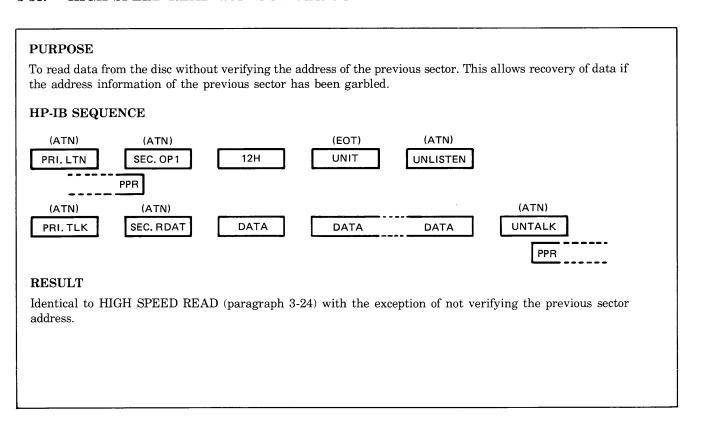
The restrictions to unaddressing and the abnormal temination modes that apply for the HIGH SPEED READ operation also apply here. (Refer to paragraph 3-24.)

At the termination of the operation all offsets will be removed. This requires a minimum of 1.5 milliseconds.

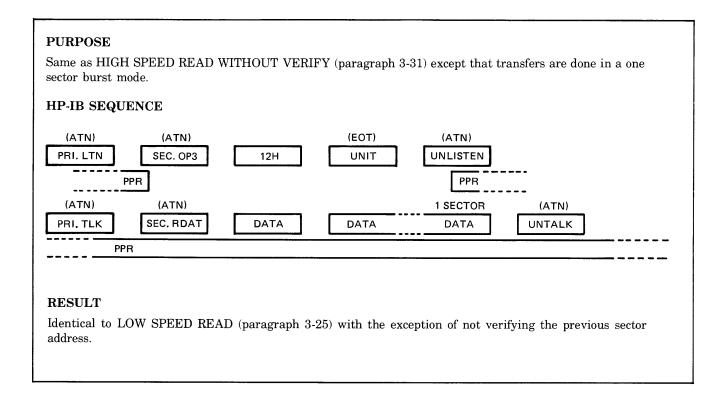
#### 3-30. LOW SPEED READ WITH OFFSET



#### 3-31. HIGH SPEED READ WITHOUT VERIFY

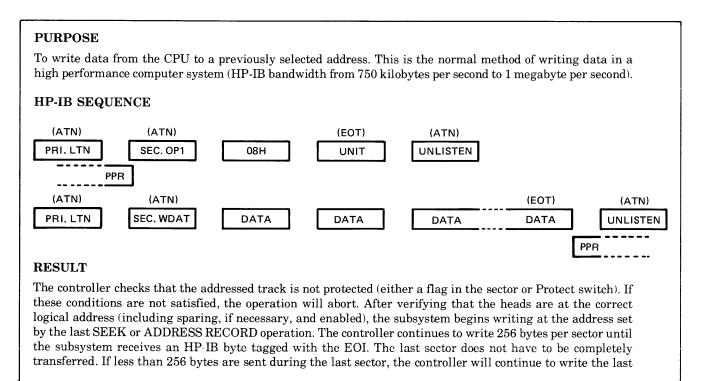


#### 3-32. LOW SPEED READ WITHOUT VERIFY



#### 3-33. WRITE OPERATIONS

#### 3-34. HIGH SPEED WRITE DATA



word sent into the remainder of the sector. Automatic seeking and sparing will occur during the transfer if necessary and if enabled. Once the EOT message is received by the subsystem, the operation will terminate.

Normally the status 1 field will be set to 00H and the DSJ Byte will be set to 00H.

Abnormal operation will result from the occurrence of any one of the following:

- An overrun (I/O system bandwidth insufficient)
- Track addressed is flagged, protected, or defective
- Surface is protected by the Unit Protect switch(es)
- A unit error

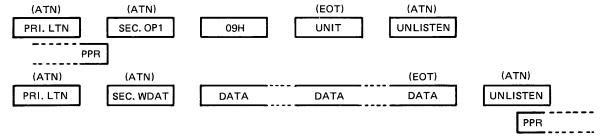
In all cases the transfer will be aborted. The subsystem will continue to accept data (and discard it immediately) after the error occurs and until the EOT message is received indicating the end of the transfer. The operation will then terminate. The status 1 field will be updated according to the type of error and the DSJ Byte will be set to 01H.

#### 3-35. HIGH SPEED WRITE FULL SECTOR

#### **PURPOSE**

This is a diagnostic tool that provides the ability to write the preamble, postamble, as well as data in each sector.

#### **HP-IB SEQUENCE**



#### RESULT

The controller checks that the Format switch is on and the Protect switch is off. If these conditions are not satisfied, the operation will abort.

The operation will continue normally irrespective of the state of the S, P, or D flags associated with the addressed track. Without verifying that the heads are at the correct logical address (without sparing), the subsystem begins writing at the address set by the last SEEK or ADDRESS RECORD operation. The controller continues to write 276 bytes per sector (1 sync word, 1 cylinder address word, 1 head-sector address word, 256 data bytes, 1 CRC word and 6 ECC words) until the subsystem receives a byte tagged with the EOT message. The last sector does not have to be completely transferred. If less than 276 bytes are sent during the last sector, the controller will continue to write the last word into the remainder of the sector.

It is strongly recommended that the scope of any write full sector operation be limited to one track to avoid sparing and/or switching to an undesired track and destroying it. This may occur because all address verification and status checks are off. In addition, a track boundary must not be crossed during a multiple sector transfer whenever tracks are being flagged spare or defective since the automatic track sparing algorithm may not work on these tracks.

Once the EOT message is received by the subsystem, the operation will terminate normally. The DSJ Byte will be set to 00H.

In high speed mode, the PCA passes the command to the disc controller prior to receipt of the data. Because the controller does not verify the previous sector (thus guaranteeing a one sector setup time) it may demand data and an overrun can occur while the first half of the swing buffer is being filled. If the operation is retried, successful completion should result.

Abnormal operation is identical to that of a HIGH SPEED WRITE operation. (Refer to paragraph 3-34.)

#### 3-36. HIGH SPEED INITIALIZE

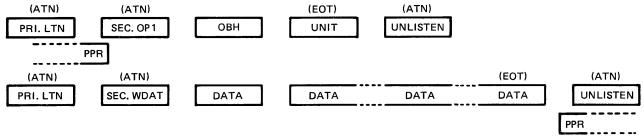
#### **PURPOSE**

Used to initialize disc media surface so that tracks can be marked as spare, defective, or protected. This operation should be performed on all new media.

#### **PROCEDURE**

- a. Sparing: The VERIFY operation should be used to determine if defective tracks exist. In a situation where a defect is found and the data is to be saved, the REQUEST SYNDROME can be used to correct errors. The corrected information is transferred to the spare track in the following manner: 1) read and correct the data, 2) seek to the physical track used as a spare, 3) do an ADDRESS RECORD operation using the location of the defective track, and 4) do an INITIALIZE operation followed by the data being transferred. When implementing the INITIALIZE, the S Bit should be set. To mark the defective track as such and to complete sparing one must: issue a SEEK to the defective track, issue an ADDRESS RECORD using the location of the spare track, and finally issue an INITIALIZE operation with the D Bit = 1 followed by a data stream.
- b. Protection: A track can be protected by issuing a SEEK followed by a VERIFY followed by an INITIALIZE operation with the P Bit set.

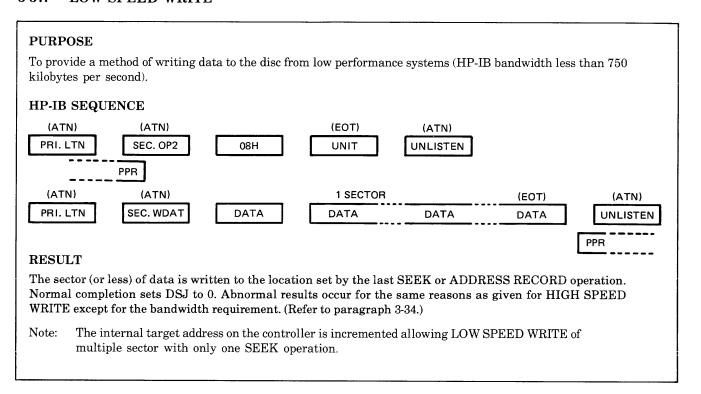
#### **HP-IB SEQUENCE**



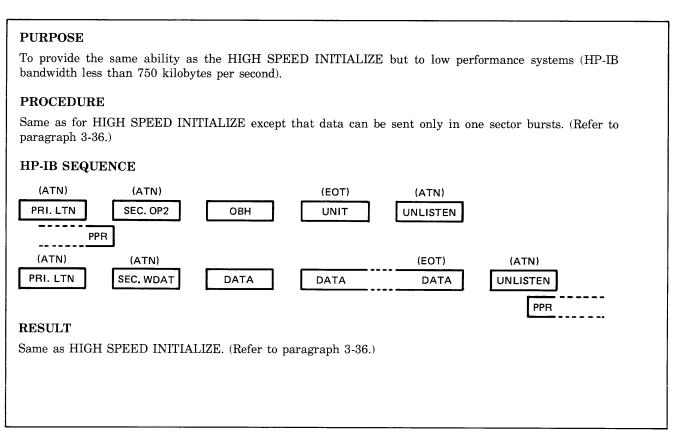
#### RESULT

- a. Sparing: Whenever a data operation (that verifies) is issued to the defective track and the automatic track sparing is enabled, all requests to the physically defective track will be rerouted to the spare.
- b. When protected, a track can be read from but not written to.
  - DSJ Byte is set to 00H for a normal completion. Abnormal completion is identical to HIGH SPEED WRITE. (Refer to paragraph 3-34.)
- c. In high speed mode, the PCA passes the command to the disc controller prior to receipt of the data. Because the controller does not verify the previous sector (thus guaranteeing a one sector setup time) it may demand data and an overrun can occur while the first half of the swing buffer is being filled. If the operation is retried, successful completion should result.

#### 3-37. LOW SPEED WRITE



#### 3-38. LOW SPEED INITIALIZE



#### IV

PRINCIPLES OF OPERATION

#### 4-1. INTRODUCTION

This section explains the principles of operation of the HP 12745D Adapter Kit. The circuit description presented consists of a discussion of a functional block diagram of the adapter kit PCA (figure 4-1).

#### 4-2. OPERATING PRINCIPLES

The HP 12745D Adapter Kit is designed for use with the HP 13037 Disc Controller and allows user communication of the disc drive via the HP Interface Bus (HP-IB). To achieve this interface, the HP 12745D provides two main functions. First, it provides the ability to transfer controller commands, status, and data information via the HP-IB; and second, it provides a full sector data buffer that can be used in a burst transfer mode.

To perform these functions, the adapter kit PCA employs five logic modules. See figure 4-1. Each module provides a specific portion of the total capability of the PCA. In general, communication between the modules occurs using asynchronous handshakes. The internal operation of each module is either asynchronous, synchonous, or both, depending upon the particular function involved. A functional overview of the operation of each module is provided in the following paragraphs.

#### 4-3. HP-IB MODULE

The HP-IB module is composed of two major sections. One section provides the proper handshakes for data or commands coming from or going to the adapter kit PCA over the HP-IB. The other section interprets commands coming over the HP-IB and translates them into control lines that govern the operation of the other four modules. The HP-IB module conforms to a subset of IEEE Standard No. 488-1975, IEEE Standard Digital Interface for Programmable Instrumentation.

#### 4-4. BUFFER MODULE

The purpose of the buffer module is two-fold. First, it provides operation of a high-speed data transfer mode at less than the 937-kilobyte burst rate of the controller; and second, allows slow-speed transfers on a sector at a time basis.

The buffer module consists of two 256 by 9 bit arrays, labelled Buffer A and Buffer B. The buffering scheme is bidirectional, that is, it handles both HP-IB-to-controller and controller-to-HP-IB transfers.

The buffers are structured such that one is available for accepting data while the other can be sourcing any data it may contain. This process is called "double-buffering". When the accepting side is full and the sourcing side has been depleted, the buffers change roles, and the transfer continues. The buffers are organized in bytes, requiring packing and unpacking on the controller side, but compatible with the byte-oriented HP-IB. The ninth bit in each buffer is used to tag the last byte in a data transfer.

Read and write buffer operations are performed by asynchronous handshake and timing circuits. The three-wire handshake of the HP-IB is converted into a two-wire handshake going to the buffer. A similar handshake is derived from the controller signals.

#### 4-5. WRITE MODULE

The write module contains logic that sets up data transfers to the controller. Also, upon receipt of a strobe signal from the controller, the module handshakes data out of the buffer.

The write module is divided into two principle parts. The first part is an algorithmic state machine. Using a set of input command signals, the machine cycles through a series of states, branching as appropriate for the inputs. The decision inputs are based mainly on the state of the HP-IB module, as determined by previous HP-IB primary and secondary commands. The result of these branching decisions is a series of output control lines that a) direct the remainder of the write module circuits, and b) provide flags that are sent to the 13037 port module. The second part of the write module consists of circuits that handshake data (or commands) out of the buffer and pack it into the 16-bit output latch of the 13037 port module.

#### 4-6. READ MODULE

The read module, like the write module, contains an algorithmic state machine that derives its control lines mainly from the primary and secondary commands of the HP-IB module. In addition to sending flags to the 13037 port module, output control lines from the state machine govern the operation of three groups of logic within the read module. The first group handles the unpacking of controller data and the handshaking of the data into the buffer module. The second group of logic is used to detect if the buffering is fast enough to stay ahead of the controller. If it is not, an error condition will be signalled to the HP 13037. The third group of logic handles the sourcing and handshaking of

information other than data or status onto the HP-IB. This other information, labelled identity code and device specified jump, is explained in section III of this manual.

#### 4-7. 13037 PORT MODULE

The 13037 port module is the final interconnect between the other four modules and PCA edge connector J1 to the controller. The data output consists of a 16-bit bidirectional bus. Latches are used to hold data while packing or unpacking the 16-bit words. There is a group of eight control and status lines coming from the controller. These lines are decoded to provide control lines within the module. In the idle state, only the Select control line is monitored. When not busy, the

controller polls through the eight possible CPU numbers. Upon matching a number with the unit in question, a Select occurs. At this time, the internal input control lines are examined to determine if the controller wishes to perform a function. Also, after Select, the output control lines are enabled so that the controller can examine any pending requests or information from the interface. When finished, the CPU is deselected and all port activity (except for polling) is curtailed.

The HP 13037 transmits data at a rate of 468 thousand words per second and control signals can switch much more rapidly. Because of transmission line effects, proper impedance termination of the lines is necessary. Termination details are discussed in section II of this manual.

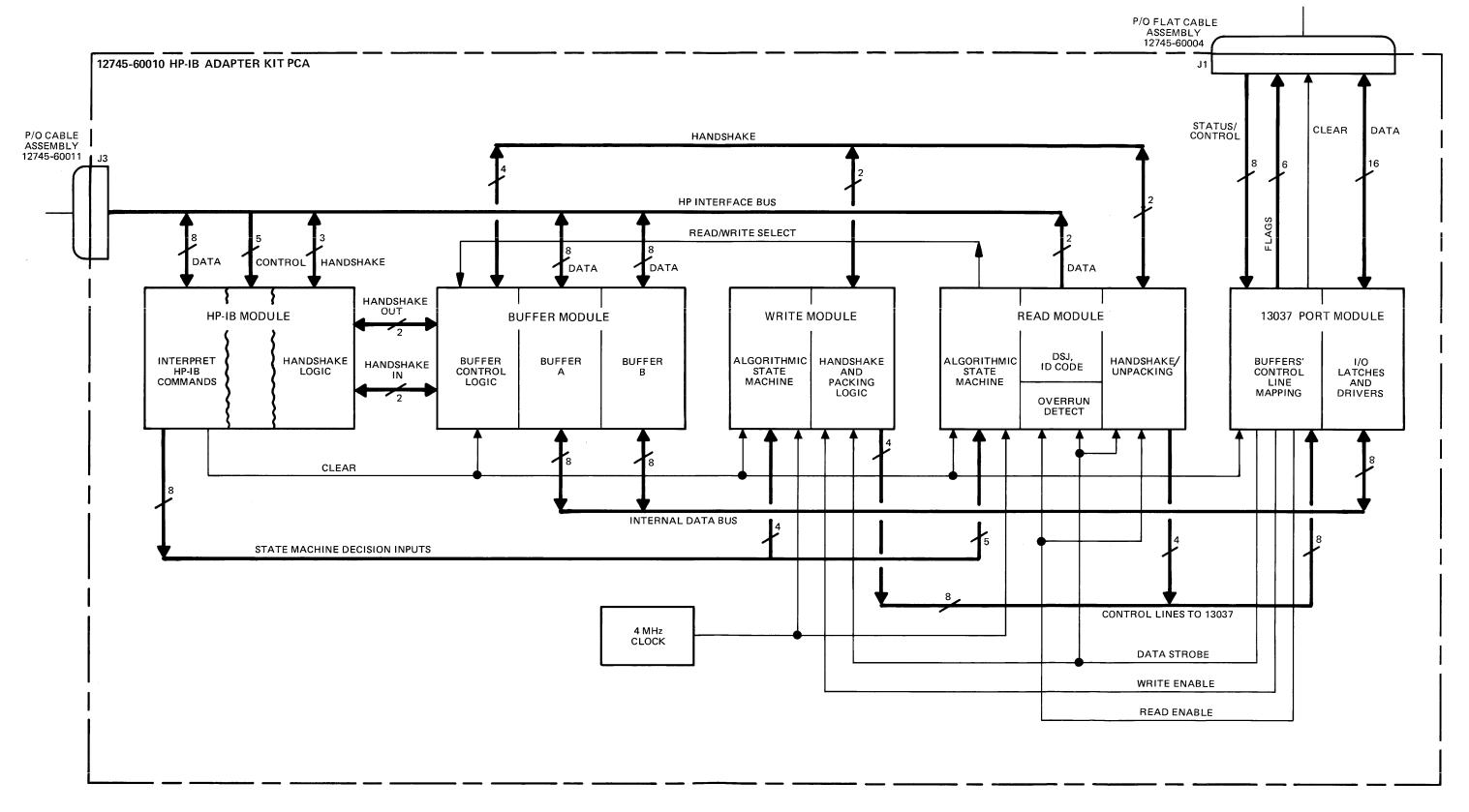


Figure 4-1. Adapter Kit PCA (12745-60010) Functional Block Diagram

# **SERVICE**

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#### 5-1. INTRODUCTION

This section includes general servicing information, maintenance reference material, and troubleshooting information.

#### **WARNING**

The service and troubleshooting procedures provided in this section are for service-trained personnel. To avoid potentially serious electrical shock, do not proceed further in this section unless qualified to do so.

#### WARNING

Use extreme caution when working on the HP 13037 Disc Controller with the top cover removed. Hazardous voltages are present inside the mainframe whenever the ac power cord is connected to an active ac power source. It is essential that all WARNINGS and CAUTIONS stated in the cabinet and other documents be observed.

#### **CAUTION**

Do not attempt to remove or install the adapter kit PCA or interconnecting cables without first removing power from all devices.

#### 5-2. PREVENTIVE MAINTENANCE

There are no extensive procedures required for maintaining the 12745D. Cleaning and inspection of the adapter kit PCA should be included in the HP 13037 Disc Controller preventive maintenance procedure, as described in the HP 13037D Disc Controller Installation and Service Manual, part no. 13037-90911.

#### 5-3. DIAGNOSTIC TEST PROGRAM

Diagnostic test programs for use with disc drive systems are available from Hewlett-Packard. Step-by-step instructions for loading the diagnostic program and running the diagnostic tests are contained in documentation supplied with the program. It is recommended that the user of a disc drive system employing a non-HP CPU have available a disgnostic test program with capabilities similar to those offered by Hewlett-Packard.

#### 5-4. TROUBLESHOOTING

Troubleshooting consists of performing the diagnostic test program described in paragraph 5-3. Generally, malfunctions can be isolated to a replaceable assembly when performing the diagnostic. The suspected faulty assembly should be replaced and the diagnostic test continued until the malfunction is cleared. If necessary, further troubleshooting should be performed as decribed in the *HP 13037D Disc Controller Installation and Service Manual*, part no. 13037-90911. In general, this troubleshooting consists of checking: a) the ac input power to the controller, b) the controller power supply output voltages, and c) the system interconnecting cables and connectors.

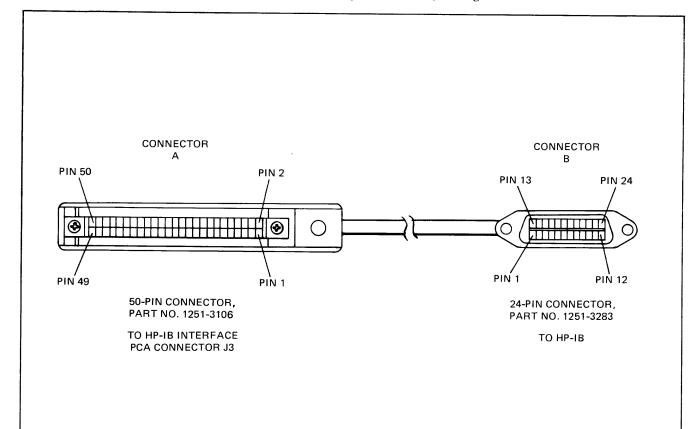
#### 5-5. REPLACEMENT PROCEDURES

Replacement of the adapter kit PCA is accomplished by following the installation and operating instructions contained in sections II and III of this manual. Be sure to check the configuration of the termination resistor packs (refer to paragraph 2-6) and the settings of switches S1 and S2 (refer to paragraph 3-2) if a replacement adapter kit PCA is being installed.

#### 5-6. SIGNAL DATA

Table 5-1 is a wiring list for cable assembly 12745-60011 connected between adapter kit PCA connector J3 and the HP-IB. Table 5-2 gives signal and pin number assignments for adapter kit PCA connectors J1 and J2.

Table 5-1. Cable Assembly (12745-60011) Wiring List



#### **WIRING LIST**

	T				
CONNECTOR A PIN ASSIGNMENT	SIGNAL	CONNECTOR B PIN ASSIGNMENT	CONNECTOR A PIN ASSIGNMENT	SIGNAL	CONNECTOR B PIN ASSIGNMENT
50	DIO1	1	49	DIO5	13
48	DIO2	2	47	DIO6	14
46	DIO3	3	45	DIO7	15
44	DIO4	4	43	DIO8	16
42	EOI	5	41	REN	17
40	DAV	6	39	GND (6)	18
38	NRFD	7	37	GND (7)	19
36	NDAC	8	35	GND (8)	20
34	IFC	9	33	GND (9)	21
32	SRQ	10	31	GND (10)	22
30	ATN	11	29	GND (11)	23
28	SHIELD	12	27	GND LOGIC	24

Notes: 1. Pins 1 through 26 are not used on Connector A.

2. In "SIGNAL" column, GND (n) is other wire of twisted pair associated with referenced Connector B pin number.

12745 Service

Table 5-2. Adapter Kit PCA Connectors J1 and J2 Pin Assignments

J1/J2 PIN	SIGNAL	J1/J2 PIN	SIGNAL
1	SPARE	26	SPARE
2	SPARE	27	IBUS3
3	IFIN0	28	CLEAR
4	IFIN2	29	ENID
5	IFIN1	30	SPARE
6	IFIN3	31	IFCCK
7	XFRNG	32	SPARE
8	IBUS4	33	GND
9	CMRDY	34	SPARE
10	IBUS5	35	SPARE
11	EOD	36	SPARE
12	IBUS6	37	IBUS8
13	IFVLD	38	IBUS12
14	IBUS7	39	IBUS9
15	GND	40	IBUS13
16	GND	41	IBUS10
17	SPARE	42	IBUS14
18	SPARE	43	IBUS11
19	GND	44	IBUS15
20	GND	45	ENIR
21	IBUS0	46	OVRUN
22	SPARE	47	DTRDY
23	IBUS1	48	INTDR
24	SPARE	49	GND
25	IBUS2	50	GND

Note: Pin assignments for J1 and J2 are identical.

# REPLACEABLE PARTS

VI

#### 6-1. INTRODUCTION

This section provides a listing of all field-replaceable parts for the HP 12745D, as well as replaceable part ordering information.

Replaceable parts for the HP 12745D are listed in table 6-1. The replaceable parts listings provide the following information:

- HP PART NO. The Hewlett-Packard part number for each replaceable part.
- DESCRIPTION. The description of each replaceable part.
- UNITS PER ASSEMBLY. The total number of each part used in the HP 12745D.

Table 6-1. HP 12745D Replaceable Parts

HP PART NO.	DESCRIPTION	UNITS PER ASSEMBLY
12745-60010	HP-IB Adapter Kit PCA	1
12745-60011	Cable Assembly	1
12745-60004	Flat Cable Assembly	1
8120-3446	10833B HP-IB Interface Cable	1
	NO. 12745-60010 12745-60011 12745-60004	NO.  12745-60010  HP-IB Adapter Kit PCA  12745-60011  Cable Assembly Flat Cable Assembly  8120-3446  10833B HP-IB

#### 6-2. ORDERING INFORMATION

To order replaceable parts for the HP 12745D, address the order to your local Hewlett-Packard Sales and Support Office. Sales and Support Offices are listed at the rear of this manual. Specify the following information for each part ordered:

- Hewlett-Packard part number.
- Complete description for each part as provided in the replaceable parts listing.