HP 13255

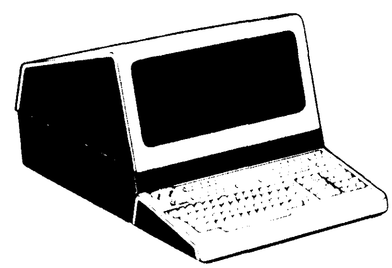
PROCESSOR (8085A-2) MODULE

Manual Part No. 13255-~~91252~~ 91249

PRINTED

FEB-14-82

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT *hp* *PACKARD*

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1.0 INTRODUCTION

1.0.1 The Memory Controller Module has been designed to be used in the 2647F terminal. It is used to provide all random access memory space required for the terminal environment; this includes variable space as well as basic program and work space. It is accessed by the processor through the terminal bus.

1.0.2 The Memory Controller consists of control and timing circuitry and up to four banks of eight 64K socketed MOS RAM chips each for a total possible capacity of 256K bytes.

1.0.3 The memory mapping of the Memory Controller is as follows: there are two optional mapping possibilities. Which is selected depends on the presence or absence of jumper W1. If W1 is absent, the board is strapped as a 128K byte board which answers to the addresses for variable space and basic space. If W1 is present, then the Memory Controller is strapped to be used in a RAM based terminal environment, answering to the terminal code addresses as well as the above mentioned variable and basic spaces. These addresses are determined by the state of the three most significant address bits, ADDR16, ADDR17, and ADDR18 as described below.

2.0 OPERATING PARAMETERS

A summary of operating parameters for the Memory Controller is contained in tables 1.0 through 5.0.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/- 0.100 Inches	Weight (Pounds)
02640-60252	Memory Controller Module	12.5 x 4.0 x 0.7	.55
Number of Backplane Slots Required: 1			

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NOTE: This document is part of the 2647F DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION

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Number of Backplane Slots Required: 1			

Table 2.0 Reliability and Environmental Information

Environmental:	(X) HP Class B	( ) Other:
Restrictions:	Type tested at product level	
Failure Rate:	1.997	(percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
1.2 A	0.1 A	0.1 A	0 mA N/A
115 volts ac @ A N/A		220 volts ac @ A N/A	
Clock Frequency: 4.915 MHz			

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In (Closed)	Out (Open
Switch		
A	Data Bit = 0	Data Bit = 1
B		
C		
D		
E		
F		
G		
H		
J		
K		
L	The switches are located on the Processor PCA and are read by firmware to determine the operating mode of the terminal. (refer to tables 6.0, 6.1, and 6.2 for accessing these bits.)	
M		
N		
P		
Q		
R		
S		
T		
U		
V		
W		
X		
Y		
Z		

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915MHz System Clock
-4	-12	-12 Volt Power Supply
-5	$\overline{ADDR0}$	Negative True, Address Bit 0
-6	$\overline{ADDR1}$	" " " " 1
-7	$\overline{ADDR2}$	" " " " 2
-8	$\overline{ADDR3}$	" " " " 3
-9	$\overline{ADDR4}$	" " " " 4
-10	$\overline{ADDR5}$	" " " " 5
-11	$\overline{ADDR6}$	" " " " 6
-12	$\overline{ADDR7}$	" " " " 7
-13	$\overline{ADDR8}$	" " " " 8
-14	$\overline{ADDR9}$	" " " " 9
-15	$\overline{ADDR10}$	" " " " 10
-16	$\overline{ADDR11}$	" " " " 11
-17	$\overline{ADDR12}$	" " " " 12
-18	$\overline{ADDR13}$	" " " " 13
-19	$\overline{ADDR14}$	" " " " 14
-20	$\overline{ADDR15}$	" " " " 15
-21	$\overline{I/O}$	Negative True, Input Output/memory
-22	GND	Ground, Common Return (Power and Signal)

Table 5.0 Connector Information (Cont.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B	$\overline{\text{POLL}}$	Negative True, Polled Interrupt Identification Request
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Read/Write Type Cycle
-R	$\overline{\text{ATN2}}$	Negative True, CTU and Polled Interrupt Request
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
* -T	N/A	Not Used
* -U	N/A	Not Used
* -V	ADDR16	Positive True, Address Bit 16
* -W	ADDR17	" " " " 17
* -X	ADDR18	" " " " 18
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	ATN	Negative True, Data Comm Interrupt Request

NOTE "*" Designates Signals That Are Unique To The 2647F. These Signals Have Been Redefined And Do Not Exist In Any Other 264X Protocol.

Table 5.1 Connector Information (Keyboard)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	+5V	+5V Volt Power Supply
-2	$\overline{\text{BBUS0}}$	Negative True, Buffered Data Bus Bit 0
-3	$\overline{\text{BBUS1}}$	" " " " " " 1
-4	$\overline{\text{BBUS2}}$	" " " " " " 2
-5	$\overline{\text{BBUS3}}$	" " " " " " 3
-6	$\overline{\text{BBUS4}}$	" " " " " " 4
-7	$\overline{\text{BBUS5}}$	" " " " " " 5
-8	$\overline{\text{BBUS6}}$	" " " " " " 6
-9	$\overline{\text{BBUS7}}$	" " " " " " 7
-10	BADDR0	Positive True, Column Address Bit 0
-11	BADDR1	" " " " " 1
-12	BADDR2	" " " " " 2
-13	BADDR3	" " " " " 3
-14	$\overline{\text{READ . }\overline{\text{COL15}}}$	Negative True. Enables Reading Columns 0-13. Not Asserted for Columns 14 & 15
-15	COM	Common Return

Table 5.1 Connector Information (Keyboard Cont'd)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	COM	Common Return
-B	Beep	Triggers Beeper Circuit
-C	-12V	-12 Volt Power Supply
-D	Chassis GND	Grounds the Switchplate
-E		Not Used
-F		Not Used
-H		Not Used
-J	COL OUT EN	Strobes Column's Previous State Into Input Register
-K	LED EN	Strobes Data Into LED Latches
-L		Not Used
-M	PWR ON	Resets the Terminal
-N	+5V	+5 Volt Power Supply
-P		Not Used
-R		Not Used
-S	+12V	+12 Volt Power Supply

Table 6.0 Module Bus Pin Assignments

Function Performed: Read Switches A through H on Keyboard section of 8085A-2 processor PCA

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: ADDR 0,1,2,3=(0111)
ADDR 7=0

Data Bus Bit Interpretation

B7 When set to 1, Switch H is open

B6 When set to 1, Switch G is open

B5 When set to 1, Switch F is open

B4 When set to 1, Switch E is open

B3 When set to 1, Switch D is open

B2 When set to 1, Switch C is open

B1 When set to 1, Switch B is open

B0 When set to 1, Switch A is open

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
1	ADDR 3
1	ADDR 2
1	ADDR 1
0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments

Function Performed: Read Switches J through R on Keyboard section of 8085A-2 processor PCA

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: ADDR 5 = 0
ADDR 7 = 1

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
1	ADDR 7
X	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Data Bus Bit Interpretation

B7 When set to 1, Switch R is open

B6 When set to 1, Switch Q is open

B5 When set to 1, Switch P is open

B4 When set to 1, Switch N is open

B3 When set to 1, Switch M is open

B2 When set to 1, Switch L is open

B1 When set to 1, Switch K is open

B0 When set to 1, Switch J is open

Table 6.2 Module Bus Pin Assignments

Function
Performed: Read Switches S through Z on Keyboard section of 8085A-2 processor PCAions may

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: ADDR 7 = 1
ADDR 5 = 1

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
1	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Data Bus Bit Interpretation

B7 When set to 1, Switch Z is open

B6 When set to 1, Switch Y is open

B5 When set to 1, Switch X is open

B4 When set to 1, Switch W is open

B3 When set to 1, Switch V is open

B2 When set to 1, Switch U is open

B1 When set to 1, Switch T is open

B0 When set to 1, Switch S is open

Table 6.3 Module Bus Pin Assignments

Function Performed: Read data comm switches on Keyboard PCA (Refer to figure 1 in module section 13255-91018 for physical location of data comm switches and their positions.)

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: ADDR 0,1,2,3=(1111)
ADDR 7 = 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
1	ADDR 3
1	ADDR 2
1	ADDR 1
1	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Data Bus Bit Interpretation

Switch 1

Position	0	1
B7	1	0

B6 Not assigned, always 0

Switch 2

Position	0	1	2
B5	0	0	1
B4	0	1	0

Switch 3

Position	0	1	2	3	4	5	6	7
B3	0	0	0	0	1	1	1	1
B2	0	0	1	1	0	0	1	1
B1	0	1	0	1	0	1	0	1

B0 Not assigned, always 0

Table 6.4 Module Bus Pin Assignments

	Value	Bus Signal
Function Performed: Output a column's previous state into the Keyboard input register		
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4)=(0011)	X	ADDR 12
	0	ADDR 11
	0	ADDR 10
	1	ADDR 9
	X	ADDR 8
Function Specifier: ADDR 5 = 1	0	ADDR 7
ADDR 7 = 0	X	ADDR 6
	1	ADDR 5
	1	ADDR 4
	X	ADDR 3
	X	ADDR 2
Data Bus Bit Interpretation: Each data bit is associated with a switch in a column. If the bit is set to 1, it indicates that the switch was previously depressed. The column to which the value is applied is specified by a subsequent switch read as indicated in table 6.5	X	ADDR 1
	X	ADDR 0
	B7	BUS 7
	B6	BUS 6
	B5	BUS 5
	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
	B1	BUS 1
	B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.5 Module Bus Pin Assignments

Function Performed: Read switches in column "n" as determined by BADDR0, BADDR1, BADDR2, and BADDR3

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: BADDR 0,1,2,3 are used to specify which keyboard column is to be read. The column number specified by these bits must be less than 14 (decimal).
ADDR 7 = 0

Data Bus Bit Interpretation: Each data bit is associated with a switch in a column. If the switch is depressed, the data bit is 1. (refer to figure 1 of module section 13255-91018 for a cross-reference of key numbers to the physical switches on the keyboard.)

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
BADDR3	ADDR 3
BADDR2	ADDR 2
BADDR1	ADDR 1
BADDR0	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Column Address (BADDRX)				DATA BUS BIT (BBUSX)							
3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	007	006	005	004	003	002	001	000
0	0	0	1	017	016	015	014	013	012	011	010
0	0	1	0	027	026	025	024	023	022	021	020
0	0	1	1	037	036	035	034	033	032	031	030
0	1	0	0	047	046	045	044	043	042	041	040
0	1	0	1	057	056	055	054	053	052	051	050
0	1	1	0	067	066	065	064	063	062	061	-
0	1	1	1	077	076	075	074	073	072	071	070
1	0	0	0	107	106	105	104	103	102	101	100
1	0	0	1	117	116	115	114	113	112	111	110
1	0	1	0	127	126	125	124	123	122	121	120
1	0	1	1	137	136	-	134	133	132	131	130
1	1	0	0	147	-	-	144	-	142	141	140
1	1	0	1	157	-	-	154	-	152	151	150

Table 6.6 Module Bus Pin Assignments

Function Performed: Write LED latch and trigger alarm generator (Beep)

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: ADDR 5 = 0
ADDR 5 = 0

Data Bus Bit Interpretation

B7 When set, Beeper is triggered

B6 When set, LED #7 is turned on

B5 When set, LED #6 is turned on

B4 When set, LED #5 is turned on

B3 When set, LED #4 is turned on

B2 When set, LED #3 is turned on

B1 When set, LED #2 is turned on

B0 When set, LED #1 is turned on

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
0	ADDR 7
X	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.7 Module Bus Pin Assignments

Function Performed: Output Reset control

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4)=(0011)

Function Specifier: ADDR 7 = 1

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
1	ADDR 9
X	ADDR 8
1	ADDR 7
X	ADDR 6
X	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Data Bus Bit Interpretation

B7 Not Used

B6 Not Used

B5 Not Used

B4 Not Used

B3 Not Used

B2 When set to 1, the RESET TERMINAL key is "disabled, preventing" hardware reset of the terminal

B1 When set to 1, the RESET TERMINAL key is "enabled, allowing" hardware reset of the terminal

B0 Not Used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 9), schematic diagram (figure 10), the timing diagrams (figures 1,2, and 3), and the parts list (02640-60249).

The 8085A-2 Processor PCA is the main controller in the terminal. It also acts as the hardware interface between the processor and the keyboard. It consists of a clock generator, processor/address logic, loader ROM/ Bus cont logic, mode latch/ interrupts, address/ data drivers, request state machine, bank select logic, keyboard decoding logic, keyboard switches/ bus driver-receiver, power on logic, and the beeper.

3.1 CLOCK GENERATOR.

3.1.1 The clock generator runs from a 19.66 MHz hybrid crystal oscillator and is capable of producing either a 9.8304 MHz clock or a 4.915 MHz clock signal to the processor. The 9.8304 MHz signal is used for normal terminal operation. The 4.915 MHz signal can be generated by grounding Test Point "GO SLOW", and is used primarily for R&D development.

3.1.2 The two NAND gates (U67) connected to the output of the oscillator are there to allow dissabling of the crystal, as well as the insertion of another clock at U67 pin 5 for DTS70 Testing.

Under normal terminal operation "GO SLOW" is not grounded. This clears flip flop U28 and places a "0" on the input of U43 pin 4. The 19.6608 MHz oscillator signal then travels to the divide by 2 clock input of the flip flop U45 Pin 1. After dividing, the flip flop outputs two 9.8304 MHz signals directly to the processor.

When the PCA is being used in connection with development systems for R&D development the "GO SLOW" Test Point must be grounded. This produces a "1" at the input of the NOR gate U37 Pin 9. The result is U43 Pin 5 is pulled low forcing the input to the second flip flop U45 Pin 1 to be the output of the first flip flop U28 Pin 9. The first flip flop (U28) divides the 19.6608 MHz signal down to 9.8304 MHZ. The second flip flop (U45) then divides the signal down again to 4.915 MHz.

3.2 PROCESSOR/ADDRESS LOGIC

3.2.1 The processor/address logic consists of two parts. The first is the 8085A-2 processor itself. It contains 16 address lines allowing up to 64K of addressing. It has 8 of the address lines multiplexed as data lines to the processor. The second section is the Address logic which consists of two transparent latches to assure the addresses are transmitted to and remain as long as possible to the rest of the board and terminal.

3.2.2 The 8085A-2 Processor takes a clock input (U51-1,2) and divides it by two to produce a 4.915Mz signal at pin 37 under normal operation. This signal then gets buffered out to the backplane to be used as the system clock. NOTE: There can be no other source driving the blackplane (P1-3)

3.2.3 Every machine cycle will be one of five types listed below.

MACHINE CYCLE	STATUS			CONTROL		
	$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	0	1	1	0	1	1
MEMORY READ	0	1	0	0	1	1
MEMORY WRITE	0	0	1	1	0	1
I/O WRITE	1	0	1	1	0	1
INTR ACKNOWLEDGE	1	1	1	1	1	0

ALE (U51-30) occurs during the first clock state of a machine cycle. The falling edge of ALE guarantees the addresses are valid.

READY (U51-35) is used to add wait states to the processor. If during a read or write cycle READY is low, the processor will wait an integral number of clock cycles for READY to go high before continuing with the read or write.

INTR (U51-10) is used to interrupt the processor. It is sampled only during the next to the last clock cycle of an instruction. If it is high, the program counter will be inhibited from incrementing and an INTA (Interrupt acknowledge) will occur.

INTA (U51-11) occurs in response to a high on the INTR line. During the interrupt acknowledge cycle INTA goes low, external logic provides a restart instruction to the processor depending on what caused the interrupt.(See section 3.4 for details on interrupts).

RESET IN (U51-36) forces the program counter to zero when low. The processor is held in the reset condition as long as this line is low.

A8-A15 are the high order address lines.

AD1-AD7 are the lower 8 address lines as well as the data lines. The lower 8 bits of the address appear on the first clock cycle of a machine cycle and are guaranteed valid on the falling edge of ALE. During the second clock cycle the 8 lines become the data input or output depending on whether the processor is reading or writing.

NOTE: For more details on the 8085A-1, refer to INTEL`s "MCS 80/85 FAMILY USER`S MANUAL".

3.2.4 The 16 addresses are latched into 2 transparent 8 bit latches. (U41,U42) by the falling edge of ALE. Once latched, the addresses remain there until ALE goes high the next machine cycle.

3.2.5 A memory mapped I/O is used. Memory references between 32k and 36k (A15-A12 = 1000) and Bank Select being 111 (ADDR18-ADDR16) are interpreted by the hardware as I/O operations. For firmware writing simplicity, address bits 8 and 4 are interchanged during an I/O operation.

U44 is used to detect if addresses are in the 32k-36k range. If bank selects (ADDR18-ADDR16) are 111 then (not)IOEN (U73-5) will be low. If both these situations occur, U73-4 will go high. This causes U72 to swap BADDR4 with BADDR8 and to pull (not)I/O on the backplane low.

(not)I/O on the backplane will also become active low whenever ALE is strobed. This is used by the 2647F ROM assembly in each machine cycle for the required deselecting of the power down ROMS. When this occurs, U73-2 will go high.

3.3 LOADER ROM / BUS CONTROLLER LOGIC

3.3.1 The logic in this portion of the circuit is used to serve three purposes. First, it generates the signal used to enable the bi-directional data bus driver (U12), second, it supplies the logic that is necessary to down load code into RAM for a RAM based terminal, and third it supplies the logic to clock the mode latch.

3.3.2 The logic used to down load code to RAM in a RAM based unit is not present in a typical production P.C. board. In order for terminal code to be down loaded to RAM through floppy disc, the following parts must be inserted on the processor board.

1. 1-LS244 in U11
2. 1-2532 EPROM (programed) in U21
3. 3-20ohm resistor packs in R3,R4,R5

When the parts are present and a jumper is installed the loader logic will be activated at power up until all code is loaded. The code then triggers the logic to deactivate itself. The loader is active when the data driver U11 is on. This is true only under the following conditions.

1. The jumper is installed.
2. A READ operation is being performed with the address less than 4K.
3. Flip Flop U34-5 is set.
4. No Interrupt acknowledge cycle is in progress.

Condition 1 is met when jumper is installed in lower left-hand corner of board. This will pull U73-8 low as well as U610-12. If condition 3 is met U610-11 will also be low. This makes LDAC go high which creates an additional wait state to the processor. Required for the slower EPROMs.

Condition 2 is met when the processor addresses lower then 4K (U44-8 goes low) and a READ operation is performed (notRD goes low). The result is that U43-11 goes low.

Condition 3 is met when PON clocks the flip flop U34. It remains set until all the code is loaded and the software performs an "OUT CO" instruction. This causes IO/M (U51-34) high,(not)WR low, BADDR15 high, and (not)ADDR14 low. The result is U43-3 goes low which clears the flip flop U34. Condition 4 occurs only if an interrupt occurs and (not INTA) goes low (U33-2). When all 4 conditions are met, the loader ROM will be active and the data from the EPROM will be driven onto the processor data bus (D0-D7).

3.3.3 The address and data driver to the backplane (U12) is enabled when (not)BUSEN is low. (not)BUSEN goes low when

1. S1 or (not)RD is low. And...
2. Any one of conditions 1,2,3 from above is not met.

If either S1 or (not)RD is low, U48-3 will be low. If any one of conditions 1,2,3 from above is not met, U33-3 will be low. When U48-3 and U33-3 are both low, the address and data bus driver will be active.

3.3.4 The mode latch (U22) is clocked whenever MODCLK (U73-13) goes from a low to a high. This occurs when the software does an "OUT 80" instrúction. When this happens, the processor pulls (not)WR high, IO/(not)M high, BADDR15 high , and BADDR14 high. This will cause U55-6 to go low as well as U73-11. The result is that MODCLK goes high for one machine cycle.

3.4 ADDRESS/DATA DRIVERS

3.4.1 This section provides many of the signals to the backplane bus. The address lines (not)ADDRO - (not)ADDR15 as well as the bank select lines ADDR16 -ADDR18 are always driving the backplane. Data is transmitted as well as received through the bi-directional driver (LS640). Many of the other control signals are also driven with a continuously enabled driver U66 (S241).

3.4.2 The data driver/receiver (U12) is enabled when (not)BUSEN goes low (refer to section 3.3.3). U12-1 determines if data is to be driven onto or received from the backplane. When S1 is high, the processor is reading data. U12-1 is high and data flows from the backplane into the processor (when the device is also enabled). When S1 is low, the processor is writing and data flows from the processor to the backplane.

3.4.3 The 2647F is the only 4X terminal in which the system clock is generated from the processor. It is mandatory that no other clock is driving the backplane (the power supply control board's system clock must be disconnected from the backplane). The terminal must use the processor's clock when the 8085A-2 processor is being used. This is needed to maintain syncronization between the 8085A and the other modules in the terminal.

3.5 MODE LATCH / INTERRUPTS

3.5.1 This section of the logic serves two main functions. First, it uses the "OUT 80" instruction to set conditions in the logic. The software writes a set of logic conditions into the accumulator. It follows this with the OUT, which writes what's in the accumulator into the mode latch(U22). Secondly, the logic which detects, prioritizes, and executes interrupts to the procerror, resides in this section.

3.5.2 When an "OUT 80" instruction is executed, MODCLK clocks the data bits D0-D7 into the LS273 U22. These bits are interpreted as follows.

DATA BIT	MEANING
D0	1=Timer running
D1	1=Timer re-enable 0=Timer interrupt acknowledged
D2	1=Bank select bit BS1 set
D3	1=Bank select bit BS0 set
D4	1=Data comm interrupt held off
D5	1=Timer interrupt held off
D6	1=Poll interrupt(read with next input operation)
D7	1=Bank select bit BS2 set

3.5.3 The 8085A supports hardware vectored priority interrupts on five levels. This has been allocated as follows:

PRIORITY	INTERRUPT ADDR	SOURCE	CAN FIRMWARE DISABLE
Lowest	30	10 mSec Timer	Yes
	40	Data Comm	Yes
	50	(not)ATN2	No
	60	NOT USED	--
Highest	70	Test Point	No

The 10mSec Timer and data comm interrupts can be disabled by an Out80 instruction in the firmware. The disables provide a method of masking undesired interrupts so that interrupts may be re-enabled during processing of interrupts of intermediate priority. Lower priority interrupts are masked off at entry to the interrupt processing routine, then interrupts are enabled, thus providing that higher priority interrupts may be acknowledged. Subsequent interrupts from the device currently being processed may be considered either higher or lower than the interrupt currently being processed, according to whether it itself is masked.

3.5.4 The mode latch can disable the timer and data comm. interrupts by setting bits D5 and D4 respectively in the mode latch (U22). The disable signals go to U38-10 and U38-5 respectively and prevent the timer or data comm. interrupts from being detected. U18,U19,U110,and U111 form a divide by 49152 circuit which divides the 4.915 Mhz. system clock down to 100Hz (10 millisecond period). At Power On U22-12,9 comes up low which clears out the entire counter timer. When the mode latch is then set with U22-12 high, the timer begins counting clock pulses. After 10 milliseconds U19-10 goes from a high to a low. If the TIM RE-EN (U22-9) has been set high, U110-8 will be clocked low, causing a timer interrupt. Whatever is requesting an interrupt will pass its interrupt through the holding latch (U36) into the priority encoder (U35). If any of the inputs to the priority encoder are low, an interrupt signal is sent to the processor from U35-15. The encoder prioritizes the interrupts and places the interrupt address of the highest priority interrupt on its output (U35-6,7,9). The interrupt will be unable to reach the processor if the bank selects are being switched and latched into U56 in the bank select portion of the logic. The software expects that data to be there regardless of an interrupt so U510-10 will go low holding off any interrupts to the processor until U56 finishes latching its bank select data. When the processor finally gets the interrupt signal, it then performs an interrupt acknowledge cycle by pulling (not)INTA low (U51-11). When this occurs, U36 latches in the interrupts. U22 then drives the interrupt address onto the processor data bus. The processor then jumps to the vectored address that holds the routine for that specific interrupt source (ie. timer, data comm., test point, or (not)ATN2).

3.6 BANK SELECT LOGIC

3.6.1 This portion of the logic is the most difficult to understand The algorithm is complex and the timing is critical. It is not advised that any changes to this portion of the circuit is made without first carefully understanding its entire operation and then testing it thoroughly.

This logic provides the processor with the ability to address more than the 64K of memory the processor alone only addresses. The software is used to set logic bits called bank select bits, to increase the address lines from 16 to 19. The new address lines ADDR16, ADDR17, and ADDR18 are generated through the logic in this circuit which in turn is set from the firmware. Because an additional 3 address lines are now available, a total of 8 (2 raised to the third power) banks of 64K is now available for the terminals architecture. The 2647F is designed with the architecture structure listed below.

ADDR18 (BS2)	ADDR17 (BS1)	ADDR16 (BS0)	ROM OR RAM	MAIN PURPOSE
0	0	0	ROM	MAIN CODE
0	1	0	ROM	MAIN CODE
1	0	0	RAM	STACK,VAR,BUFFER
1	1	0	RAM	WORK SPACE
1	1	1	RAM	DSPLY MEM.,I/O

```
64K --------   --------   --------   --------   --------
    |      |   |      |   |      |   |      |   |      |
    |      |   |      |   |      |   |      |   |Disply|
    |      |   |      |   |      |   |      |   |Memory|
48K |------|   |------|   |      |   |      |48K|------|
    |      |   |      |   |Common|   | Work |   |      |
    |      |   |      |   |Memory|   |Space |36K|------|
    | Main |   |      |   |      |   |      |   | I/O  |
    | Code |   | Main |   | ie.  |   | ie.  |32K|------|
    |      |   | Code |   | Stack|   | Basic|   |      |
    |      |   |      |   |Variab|   |      |   |      |
    |      |   |      |   |Buffer|   |      |   |      |
    |      |   |      |   |      |   |      |   |      |
    |      |   |      |   |      |   |      |   |      |
    |      |   |      |   |      |   |      |   |      |
    |      |   |      |   |      |   |      |   |      |
 0K --------   --------   --------   --------   --------
      000        010        100        110        111
      ROM        ROM        RAM        RAM        RAM
```

The bank select logic algorithm was created to minimize the amount of additional firmware needed to switch to alternate banks of 64K. The hardware actually reads some of the software coming from ROM to the processor and anticipates the need to write or read to an alternate bank of memory. Once anticipated, it switches to the necessary banks for the proper number of memory cycles before returning to the original bank. The processor itself (8085A) has no knowledge of what bank the information it is reading from or writing to.

A different bank of 64K can be reached several different ways (see flow chart, figure 4)

1. Any stack operation will automatically read or write to the stack on bank 100 and return to the bank specified by the mode latch. (see figure 5 and section 3.6.2)

2. As long as the previous instruction was not an OUT with A=0 (the 8 bits in the second byte of the OUT is specified as ABCDEFGH) any memory access with the addresses above 48K will go to the common page (100) until either an address is below 48K or and OUT is performed with A=0. If below 48K, it returns to mode latch bank select bits BS2,BS1,BS0. If any OUT instruction occurs following a >48K access see 3 or 4 below. (see figure 6 and section 3.6.3)

3. If an OUT is read with A=0 and B=1 the following instruction will execute its memory read or write on the bank specified by OPQ in the accumulator (the accumulator's 8 bits are specified as JKLMNOPQ) and return to the bank specified by the mode latch. (see figure 8 and section 3.6.4)

4. If an OUT is read with A=0 and B=0 the following instruction will execute its memory read or write on the bank specified by FGH of the second byte of the OUT instruction. It will return to the bank specified by the mode latch. (see figure 7 and section 3.6.5)

These four ways of changing banks with the bank select logic can best be understood through 4 examples. The following four sections each explain one of the 4 approaches listed above. The examples of software code were made up for illustration purposes only.

NOTE: The OUT instruction contains 2 bytes
One is the OUT itself
The other is the 8 bits ABCDEFGH in the second byte of the OUT.

- The 8 bits in the accumulator are specified JKLMNOPQ

3.6.2 EXAMPLE 1 (Changing the bank select using stack operations.)

When the software must "CALL" a routine it must save the current program counter in RAM so that when it "RETURN"s it can call back that address to the program counter within the processor and resume. When a "CALL" instruction is read from ROM into the processor the bank select logic recognizes it as a CALL instruction by decoding the processor data bus (D0-D7) in a PROM (U71). The PROM only reads the bus during an op-code fetch (U58-12,13 are both high). If the instruction read is a Stack operation, like a "CALL" the PROM (U71) outputs a high on U71-12. Because U48-4 is also high at this time, U69-15 becomes low. A low input signifies the counter (U69) should load the initial count from its inputs (U69-11,12,14) into the counter on the next rising edge of its CLK input (U69-7).Refer to figure 5. The initial count originates from the PROM also (U71). The initial count determines the number of machine cycles needing to be performed before switching to the COMMON bank (100). This depends on the stack instruction being executed. The PROM contains this info for each instruction and has the following interpretation.

PROM OUTPUTS (71)			NUMBER OF ADDITIONAL MEMORY CYCLES BEFORE SWITCHING TO ALTERNATE BANK.
04	03	02	
1	1	1	0
0	1	1	1
0	0	1	2
0	0	0	3

For this example a CALL instruction has 5 cycles. The first is the opcode fetch to read the CALL, the second and third is to read the new address, and the fourth and the fifth is to move the address in the program counter to the stack (bank 100). In this case, because we have already read the op-code, there are just 2 more cycles needed before switching to bank 100. From the table it shows the values 04=0, 03=0, and 02=1. When the fourth cycle occurs, U69-13 goes high. This causes U57-1 to go high which multiplexes 1B,2B,and 3B (100) to the output 1Y, 2Y,and 3Y. The bank select 100 is driven onto the backplane through the enabled driver U68-1. The bank remains at 100 until the next instruction is fetched. When this occurs, U58-11 goes low during the opcode fetch. U411-8 will then go low causing the counter U69 to clear. This results in the U571 to return to its low state causing the original bank select values from the mode latch (BS0,BS1,BS2) to be driven onto the backplane (000 or 010). This example is true for all stack operations. The only differences are the number of cycles the logic must wait before switching to the common bank (100).

3.6.3 EXAMPLE 2 Changing bank select by addressing above 48K. (Refer to figure 6).

If memory is accessed above 48K, the bank select bits will switch to the common page 100 for that accesss. For example, the instruction "STA F000" moves the contents of the accumulator to F000 ,which is above 48K. When F000 is placed on the address bus, BADDR14 and BADDR15 are both high. This causes U33-8 to be low, which in turn makes U57-1 high. This selects the 1B,2B,3B values 100 (U57-10,6,3). The bits 100 are driven onto the backplane through U68-4,6,8. The memory access is then performed on the common bank. This is all provided that U68-1 is enabled. If the previous instruction to the STA was an OUT with A=0, then a different bank other than 100 is trying to be accessed. When this occurs, U48-11 will be high, which disables U68-1 and enables U68-19, hence the bank select bits will come from U56.

3.6.4 EXAMPLE 3 Changing bank select by using OUT instruction with A=0 and B=1 (Refer to figure 8)

This method is taken when the bank select bits are to originate from the lower 3 bits in the accumulator OPQ. To illustrate this, suppose the following code is read from ROM

```
OUT 4F
MOV A,M
STA FOOO
```

The purpose of this is to move from memory (Address in H,L registers) on the bank specified by the lower three bits in the accumulator to the accumulator and then move that from the accumulator to location F000.

When the OUT instruction writes the contents of the accumulator to location 4F4F (01001110100111), U510-6 goes high as well as REQ (U58-9). The result is the multiplexer U56 clocks in the inputs depending on which set of inputs is selected (U56-10). In this case BADDR14=1 and data bits D2,D1,D0 are clocked into the multiplexer. D2,D1,D0 are the lower three bits of the accumulator OPQ. These bits become the bank select bits during the following instruction. The OUT has also caused U59-5 to go high, which makes the counter U69 ready to load the count value (U69-15 low) on the next (not)MEMCYC (U69-7). The opcode MOV is read next from ROM. The PROM (U71) decodes MOV similarly as in EXAMPLE 1 and places the value 111 on the inputs to the counter (U69-14,12,11). At the end of the MOV opcode fetch, the counter clocks these values which causes OH (U69-13) to go high. The flip flop U59 also clocks a high to its output pin 9. Because U48-12,13 are both high now, U68-19 is enabled, which drives the outputs of U56 to the backplane. The bank selects are now set at OPQ and are ready for the processors next machine cycle. The next cycle is to read from memory. This is now done on the new bank OPQ. Following this read from the changed bank, the processor is ready to do an opcode fetch of the STA. An opcode fetch causes the signals S0 and S1 to be high. U58-11 then goes low, which clears the flip flop U59-13 and the counter U69-9. This in turns disables U68-19 and re-enables U68-1. The opcode is then read from the bank specified by the mode latch (U5711,5,2).

3.6.5 EXAMPLE 4 Changing the bank select by using the OUT instruction with A=0 and B=0
(Refer to figure 7)

This approach is used when the bank select bits are to originate from the lower 3 bits on the address bus during an OUT operation. The sequence of steps is almost identical to EXAMPLE 4, except that because B=0, BADDR14 is now low instead of high. When U56 gets clocked during the write cycle of the OUT operation, C1,B1,A1 (U56-9,4,3) are now clocked into the multiplexer. These bits are simply the lower three addresses BADDR2,1,0. Because the address bus is simply the second byte of the OUT instruction repeated a second time (0606 for figure 7), BADDR2,1,0 is really FGH in the second byte of the OUT (100 for this example). All other operations are the same as in EXAMPLE 3.

3.7 REQUEST STATE MACHINE

3.7.1 This portion of the logic is used to provide the "READY" signal to the processor, which if not active, will cause the processor to wait indefinitely until "READY" returns to its normal high state. The signal (not)REQ is also generated in this section. When low, it tells the other modules as well as its own that the processor is ready to write or read. Addresses are stable during a request and data is valid during the entire cycle of a write request. Figure 1 shows the relationship of (not)REQ to the other relevant signals on the backplane. It should be noted that data must be valid on the backplane 115 nanoseconds prior to the rising edge of T3 for a memory read, Not on the rising edge of (not)REQ (like the other 4X processor protocol required).

3.7.2 The processor can enter into a wait state by two possible methods. Either an external module can pull (not)WAIT low (U410-12) or the processor module can (U410-13). Due to timing requirements, the processor module will always insert at least 1 wait state in every machine cycle. (Refer to figure 3) ALE is strobed every machine cycle. When this occurs, it toggles U210-5 high. The rising edge of SYS CLK during T1 then toggles U211-6 low, causing the processor to enter into a wait state after T2. Provided Test Point 4 "EPROM" is not grounded or the "LOADER ROM" active (LDACT is high), U311-10 will remain high. U211-6 going low causes U311-8 to therefore go low also. The result is the flip flop U210-5 will be cleared. The rising edge of T3 then toggles U211-6 back, which returns the processor to the ready state. The net result is 1 wait state is added to the machine cycle.

If either Test Point 4 ("EPROM") is grounded or the loader ROM is active, LDACT (U47-5) is high, then two wait states will be added to each machine cycle. This occurs because U311-10 is now low. Unlike the last case when U211-5 goes high, the flip flop U210-5 is not cleared. Another clock cycle later causes flip flop U211-7 to go low. The flip flop U210-5 is finally cleared and READY returns to its active state the following rising edge of SYS CLK. (see figure 3). The net result is 2 wait states are added to each machine cycle.

In order for an external module to create a wait state, it must pull (not)WAIT low 120 nanoseconds prior to the rising edge of the processor generated wait state (see figure 2).

3.7.3 A request is generated whenever a (not)RD or (not)WR cycle is performed. If either of these signals is low U210-12, the input to the flip flop is also low (see figure 2). The rising edge of T2 clocks the output U210-9 low, which when ORed with the input, produces a low on U411-3. This is the asserted time of (not)REQ. When (not)RD or (not)WR returns high during T3, the input U411-2 also returns high, which in turn returns (not)REQ P1-Y to the inactive high state.

3.8 POWER ON LOGIC

3.8.1 The firmware can disable the keyboard reset before and after critical sections of the code. If enabled, the PON signal (P1-D) is pulled low by the user pressing the reset key, which resets the hardware, and the processor begins at location 00 when released.

3.8.2 The reset can be disabled by the firmware writing to the keyboard as shown in table 6.7. This causes MODE SEL U45-13 to go low, which resets the flip flop output U45-9. With U410-10 now low, any reset to the keyboard is no longer passed through U410-8. The result is the reset is held off until enabled. When the firmware sets the flipflop output U45-9, the keyboard reset is then enabled. A high to U410-9 (RESET key pressed) causes the flipflop output U28-5 to go high on the next system clock. U410-5 will then go high, provided a memory cycle is not in progress (U410-4 high). U47-10 will go low pulling PON low on the backplane.

On the system clock following the release of the reset flipflop, U28-5 is pulled low. The capacitor C10 then begins charging up. This is to assure that bouncing in the reset line is not transmitted to the backplane. After charging up to the threshold of U67, the backplane PON is returned to its active high state.

3.9 KEYBOARD DECODING LOGIC

3.9.1 This section of the logic is used to provide some of the control signals for both the interface logic as well as the keyboard itself. The keyboard can only be addressed when the bank selects are 111 and memory is being addressed between 32k and 36k. The keyboard module is specified by (not)ADDR11,10,9,4 = 1100. As mentioned earlier, addresses 4 and 8 are swapped during an I/O operation. The addresses 5 and 7 are then used to specify which keyboard function is to be performed.

3.9.2 IO (U39-6) will go high when the processor is addressing between 32K and 36K and the bank select bits are set at 111. U55-8 is activated low when the processor has address bit BADDR8,9,10,11 = 1100. When these two signals are active, the decoder is finally enabled when the (not)LREQ signal (U39-5) is strobed low. Tables 6.0 through 6.7 indicate the function specifiers for each keyboard function (ie. Table 6.2 indicates the function specifier ADDR 7 =1 AND ADDR 5 =1 in order to perform the function of reading keyboard switches S through Z). Transistor Q1 is used to guarantee that LED EN is below ground when off, to assure no flickering occurs of the LEDs on the keyboard.

3.10 BEEPER

3.10.1 The function of this section is to provide a 800 Hz signal to the keyboard speaker when triggered by the firmware. Table 6.6 shows that when BADDR 5 =0 and BADDR 7 = 0 and the keyboard is addressed, the decoder (U39) pulls (not)LED EN low (U37-2). When (not)BUS7 is also low (U37-2), the flip flop is clocked (U110), causing the output to go high (Pin 5). The 800 Hz signal originating from the timer interrupt counter is passed through U29-6 and driven to the speaker (P2-B) through the current limiting resistor R25. (not)Q of the flipflop (U110-6) goes low when the flipflop is clocked. After approximately 100 milliseconds, the capacitor C9 has charged up triggering U511-5 low and reseting the flipflop to its original state. This will cause U29-4 to go low, which prevents the 800 Hz signal from passing through. The net result is a 100 millisecond signal of 800 Hz is sent to the speaker.

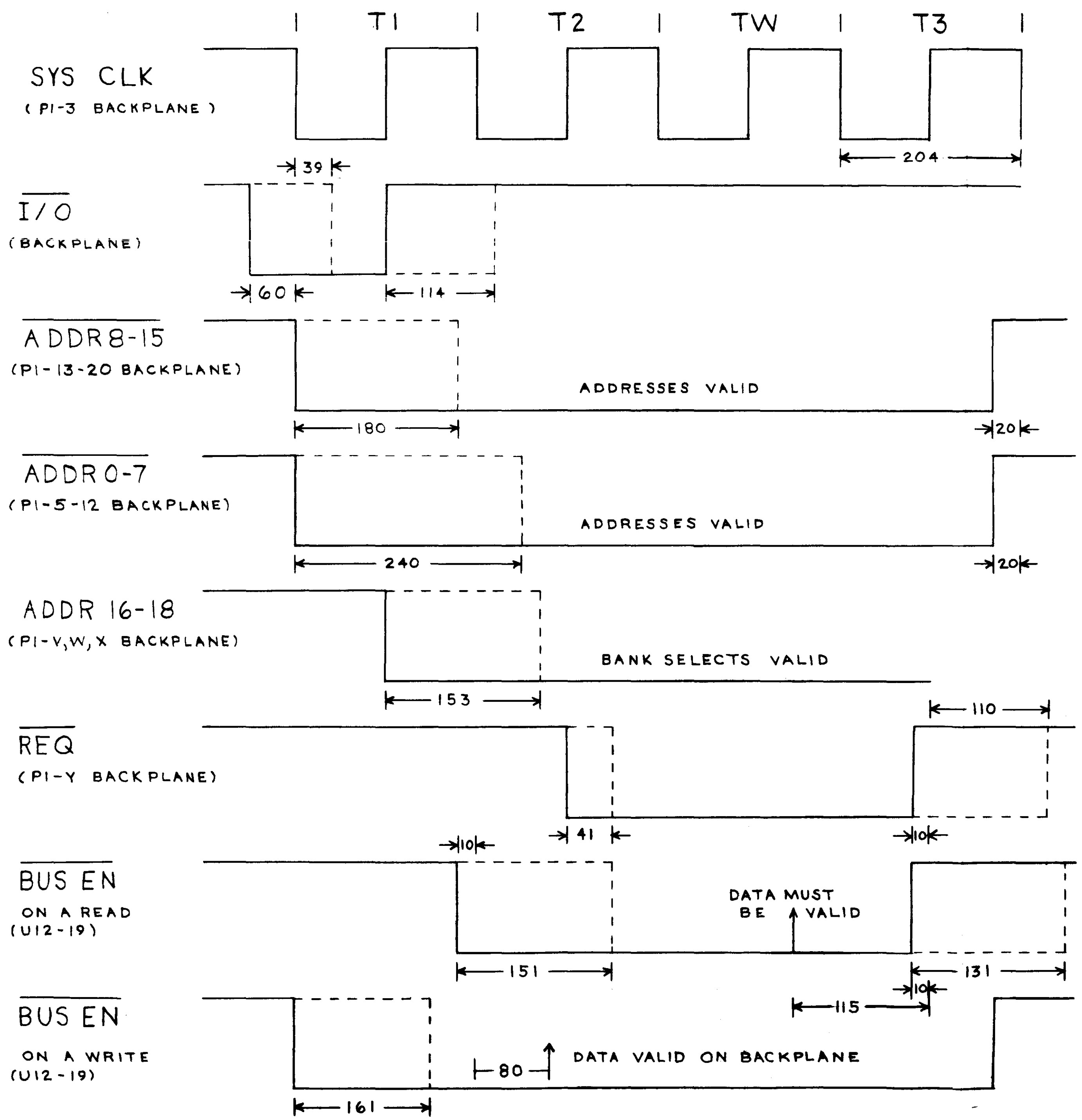
3.11 KEYBOARD SWITCHES / BUS DRIVER-RECEIVER

3.11.1 This section of the logic contains two main functions. First, it has 24 option switches (A through Z), which are set by the user. Their function is dependent on the software written for the terminal. The switches are separated into three groups of eight. Each set of eight is driven through a LS240 onto the keyboard data bus when enabled.

Enabling is done according to the function specifiers in tables 6.0 through 6.2. When the switch is open, it is at a logic 1, and when closed it is at a logic 0.

3.11.2 The second function of this section is to drive and receive data from the backplane to the keyboard data bus. Any time the processor is writing, S1 will be low. This causes U13-1,19 to go low, which then drives the backplane data onto the keyboard data bus, even if the processor is not writing to the keyboard. This will not create any problems because the keyboard ignores the data bus unless a keyboard function signal is active (ie. MODE SEL). The data is inverted onto the keyboard data bus. The processor reads from the keyboard through the buffer U23. When the keyboard module is addressed, U38-12,13 are both low. If a read is being performed by the processor, (not)RD is also low causing U311-2 to then go high. As long as test point "KYB DIS" is not grounded, U311-3 will then go low enabling the driver U23. Data is noninverted from the keyboard data bus onto the backplane. If a problem is suspected with the keyboard section of this PCA, "KYB DIS" can be grounded which disconnects the keyboard section of the PCA. The keyboard interface used on the other 4X products can be installed in the backplane to confirm if the -60249 keyboard logic is the cause of the original problem.

FIGURE 1: PROCESSOR BOARD TIMING

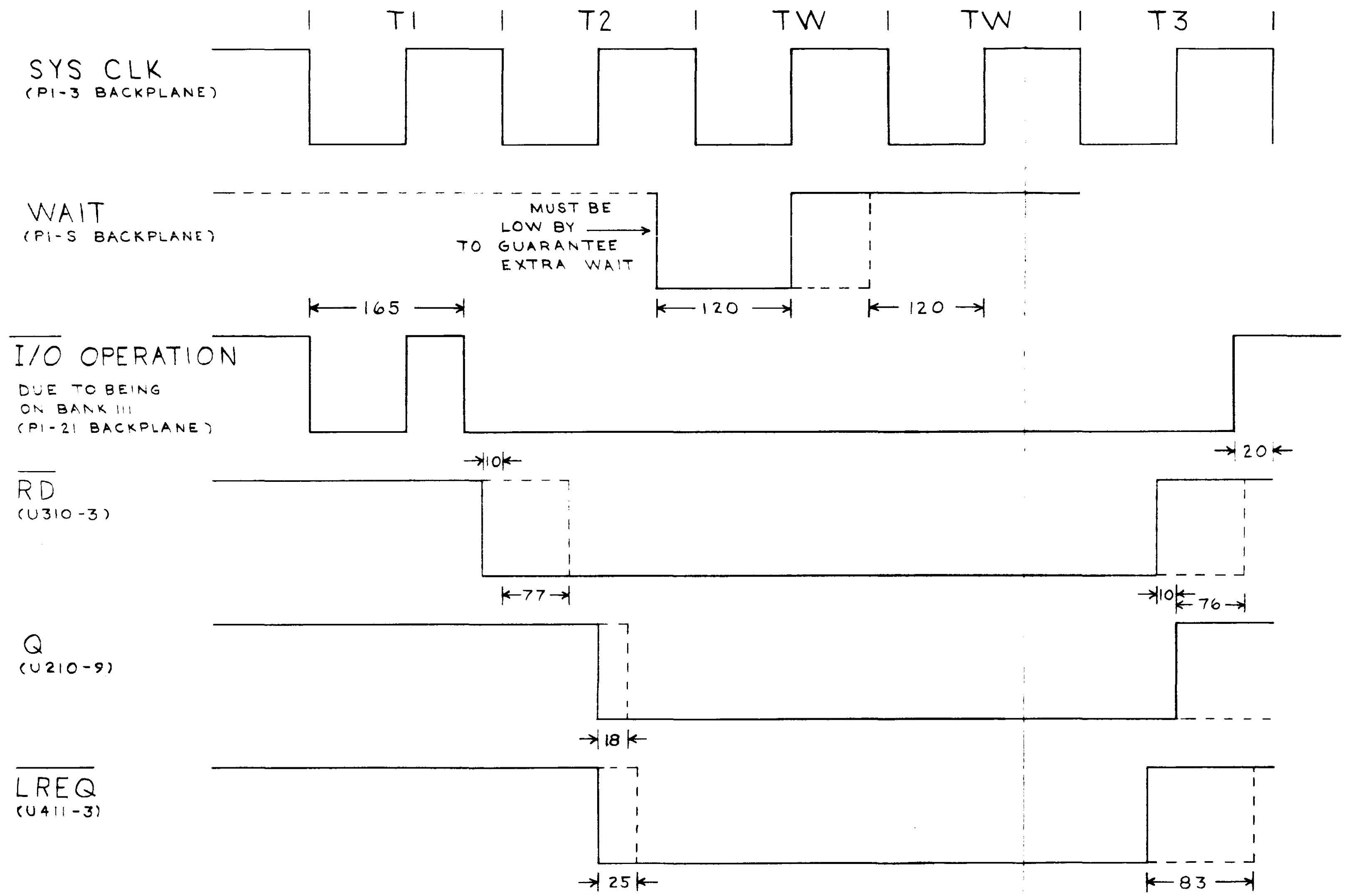


NOTES:

1) ALL TIMES IN NANOSECONDS
2) —— = EARLIEST TIME
3) - - = LATEST TIME

Figure 1
02640-60249 Timing Diagram
FEB-14-82 13255-91249

FIGURE 2: PROCESSOR BOARD TIMING (2 WAIT STATES)



NOTES:

1) ALL TIMES IN NANOSECONDS
2) —— = EARLIEST TIME
3) - - = LATEST TIME

Figure 2
02640-60249 Timing Diagram
FEB-14-82 13255-91249

FIGURE 3: READY STATE MACHINE

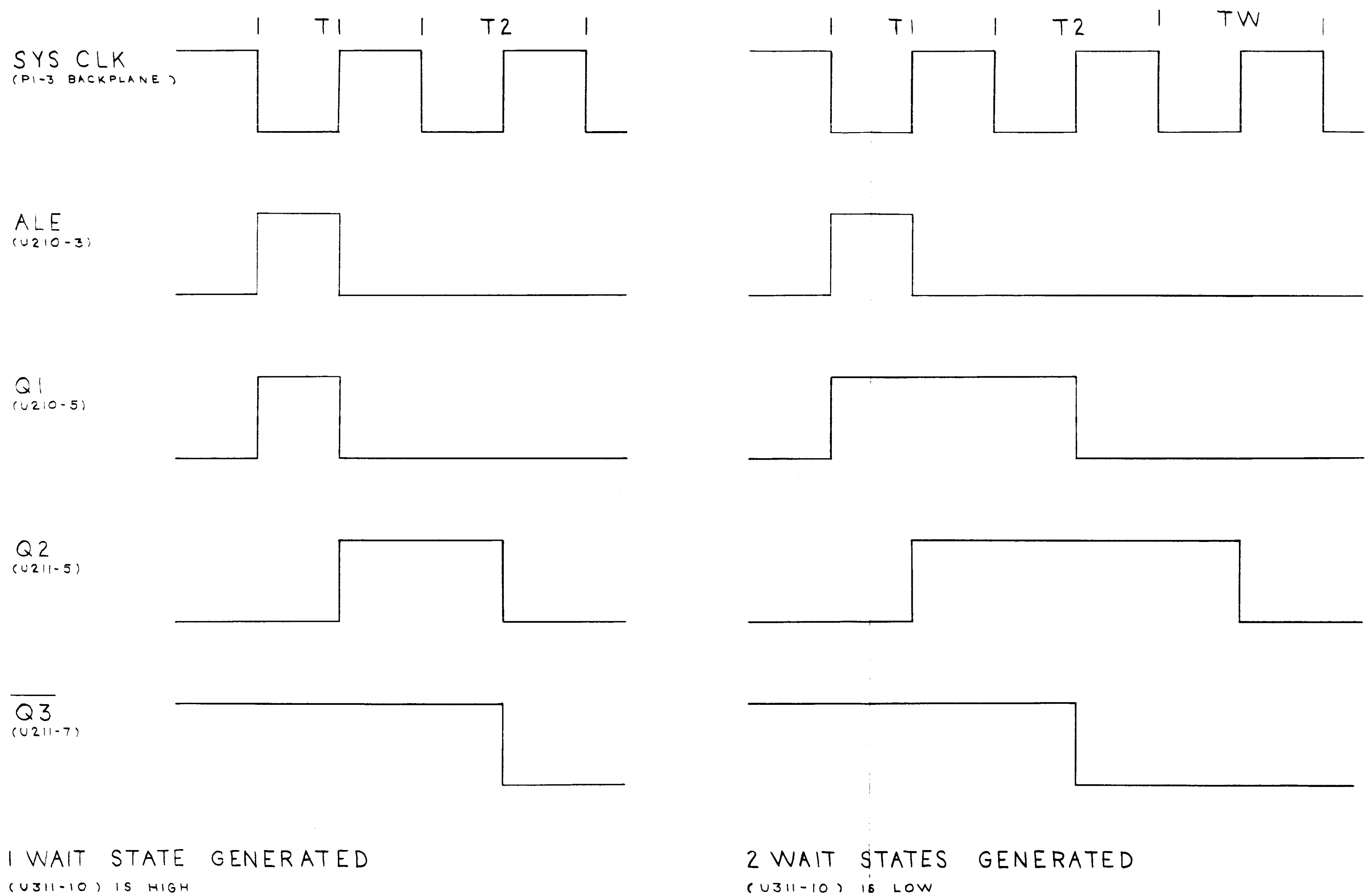
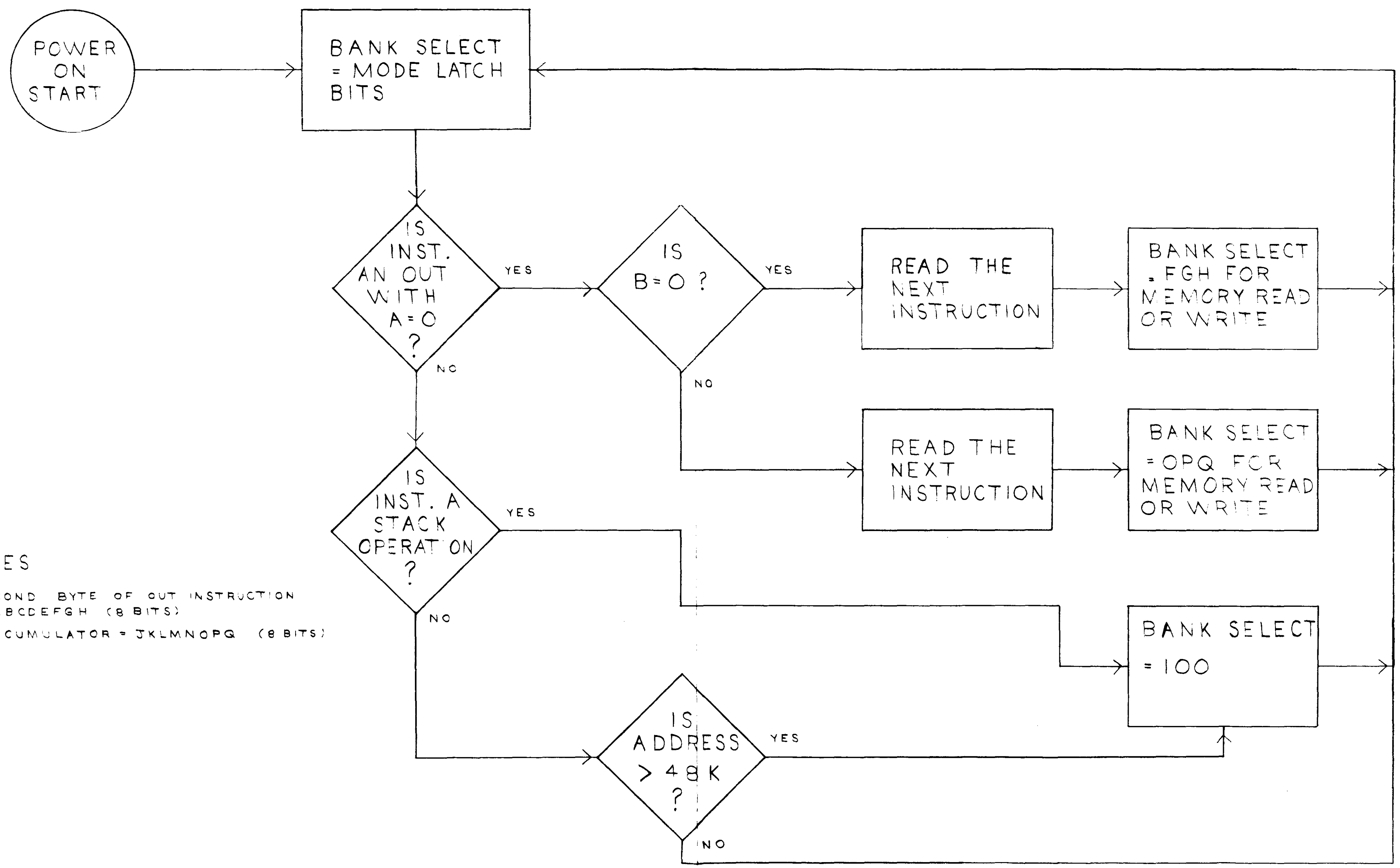


Figure 3
02640-60249 Timing Diagram
FEB-14-82 13255-91249

FIGURE 4: BANK SELECT ALGORITHM



NOTES

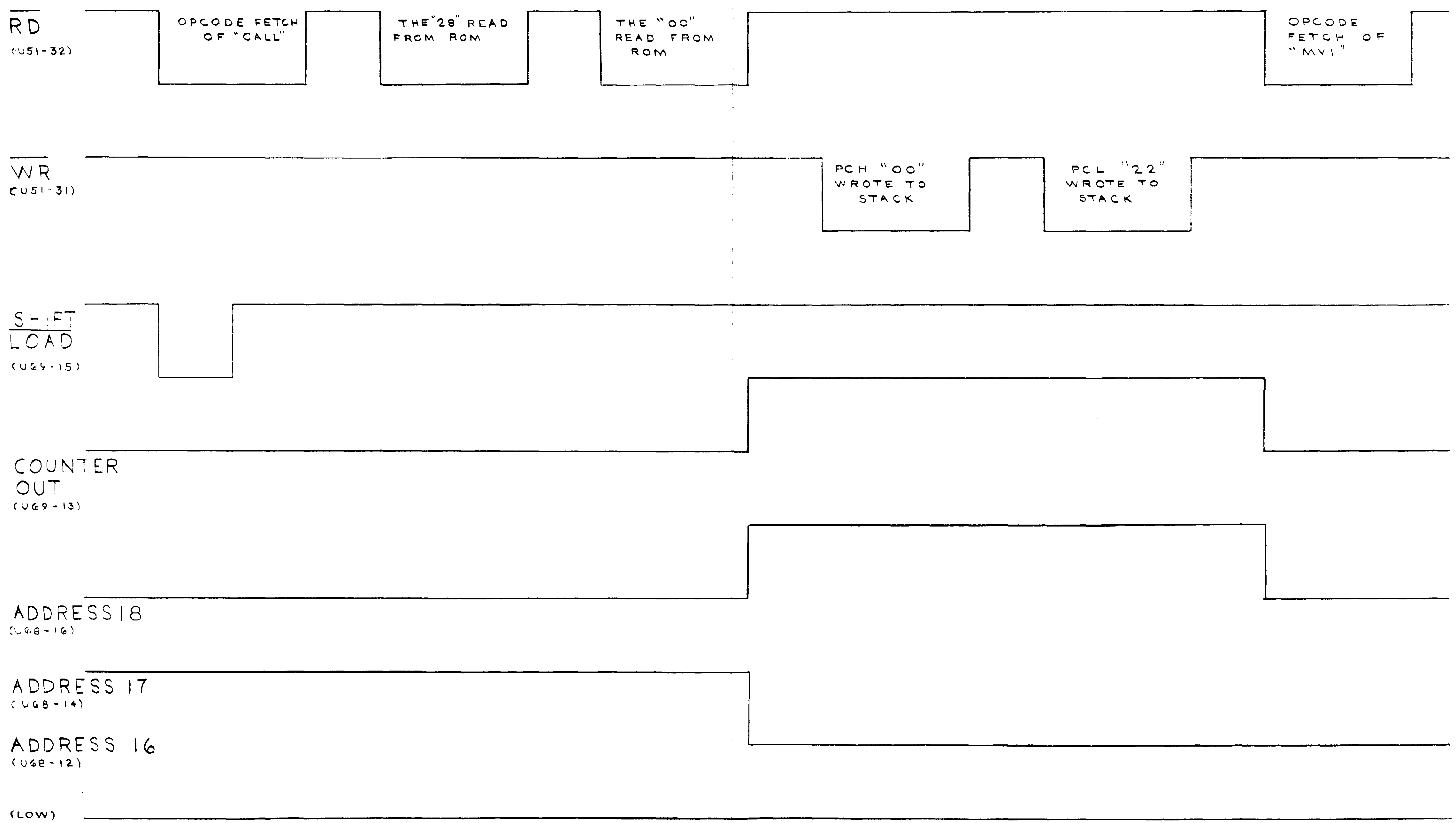
1) SECOND BYTE OF OUT INSTRUCTION = ABCDEFGH (8 BITS)

2) ACCUMULATOR = JKLMNOPQ (8 BITS)

Figure 4
02640-60249 Bank Select Algorithm
FEB-14-82 13255-91249

EXAMPLE 1

FIGURE 5 : CHANGING BANK SELECT USING STACK OPERATION



SOFTWARE NOTES

ADDRESS	INSTRUCTIONS
0022	CALL 0028
–	–
0028	MVI A, FF

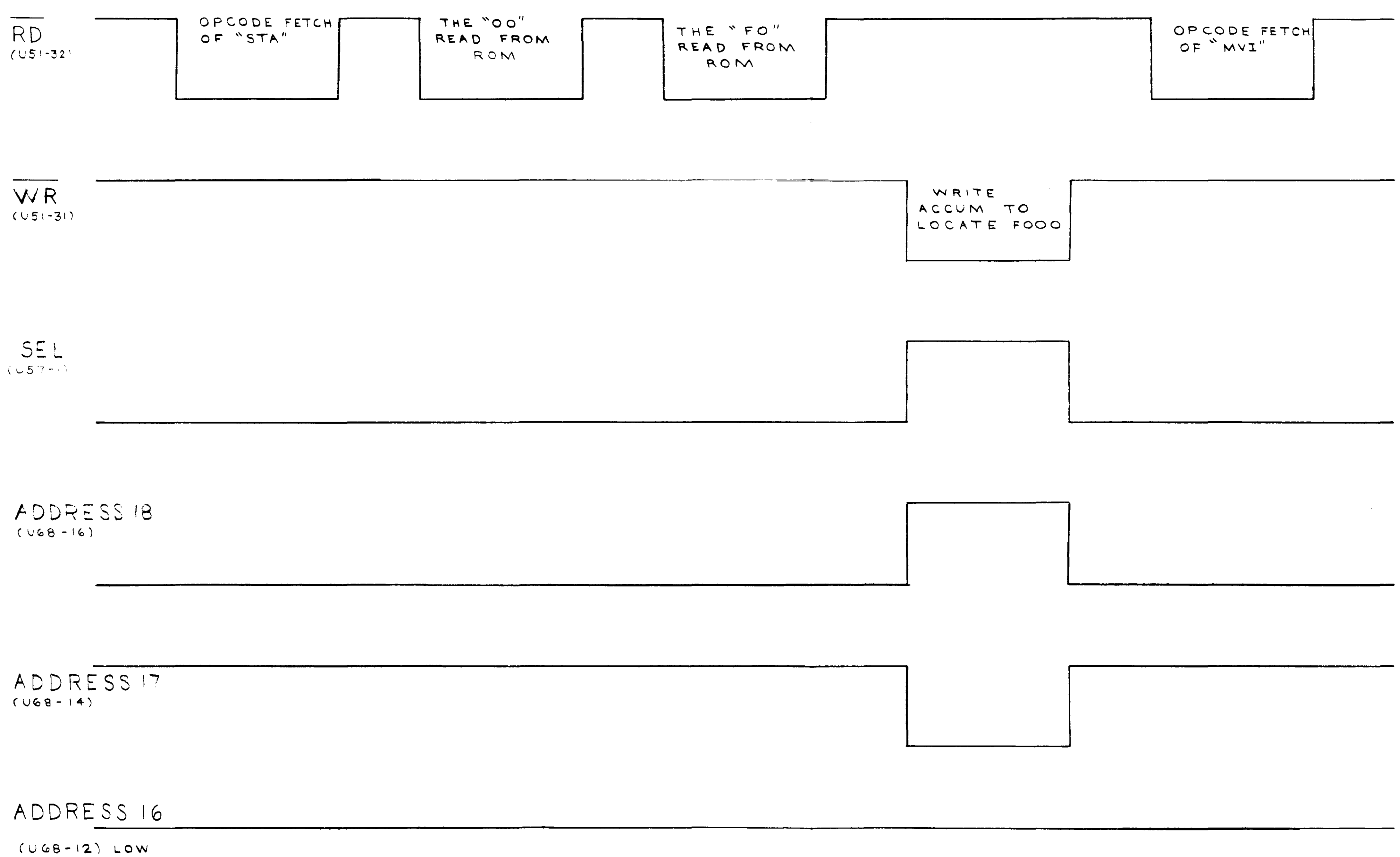
GIVEN MODE LATCH

BS2 = 0
BS1 = 1
BS0 = 0

Figure 5
02640-60249 Bank Select
FEB-14-82 13255-91249

EXAMPLE 2

FIGURE 6: CHANGING BANK SELECT BY ADDRESSING ABOVE 48K



SOFTWARE NOTES

ADDRESS	INSTRUCTION
0010	STA F000
0014	MVI A,FF

GIVEN MODE LATCH

BS2 = 0

BS1 = 1

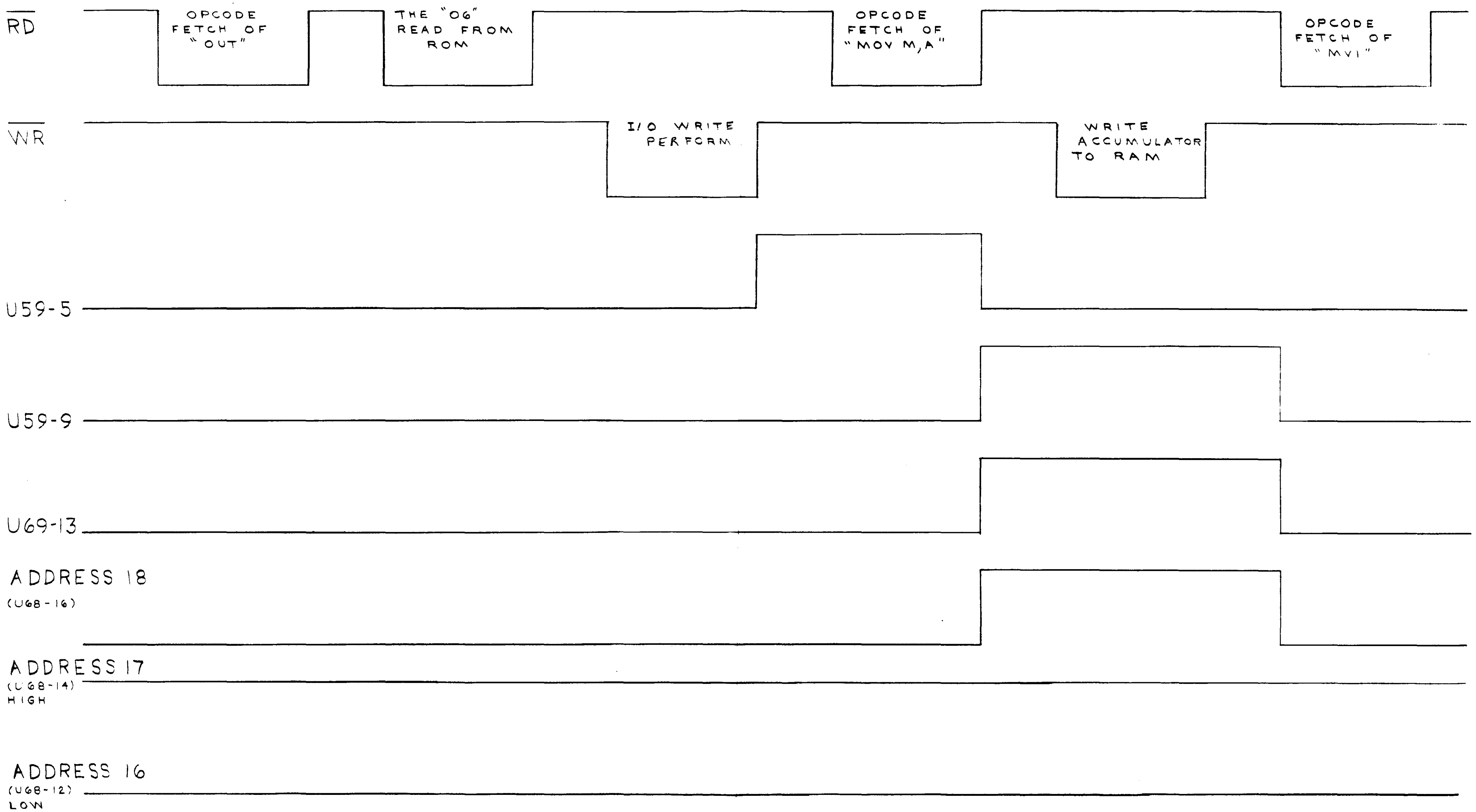
BS0 = 0

Figure 6
02640-60249 Bank Select
FEB-14-82 13255-91249

EXAMPLE 3

SECOND BYTE OF OUT INSTRUCTION
= ABCDEFGH (8 BITS)

FIGURE 7: CHANGING BANK SELECT BY USING OUT INSTRUCTION WITH A=0, B=0



SOFTWARE NOTES GIVEN MODE LATCH

ADDRESS	INSTRUCTION	
0040	OUT 06	BS2 = 0
0042	MOV M,A	BS1 = 1
0043	MVI A,FF	BS0 = 0

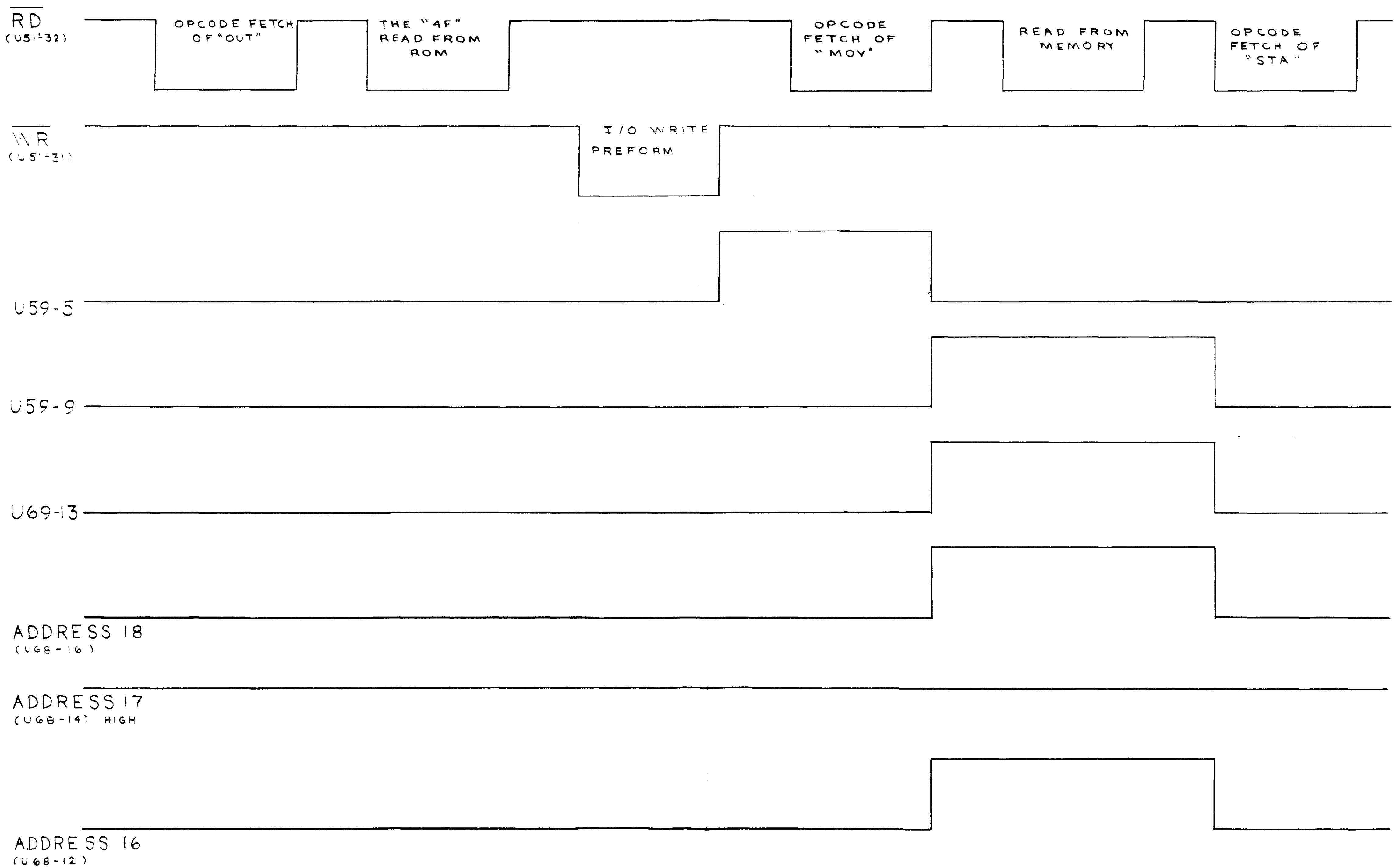
06 = 00000110
HEX = BINARY

Figure 7
02640-60249 Bank Select
FEB-14-82 13255-91249

EXAMPLE 4

SECOND BYTE OF OUT INSTRUCTION = ABCDEFGH
8 BITS IN ACCUMULATOR = JKLMNOPQ

FIGURE 8 : CHANGING BANK SELECT BY USING OUT INSTRUCTION WITH A=0, B=1



SOFTWARE NOTES

ADDRESS	INSTRUCTION
0030	OUT 4F
0032	MOV A,M
0033	STA F000

GIVEN MODE LATCH
BS2 = 0
BS1 = 1
BS0 = 0
ACCUMULATOR = 00000111

Figure 8
02640-60249 Bank Select
FEB-14-82 13255-91249

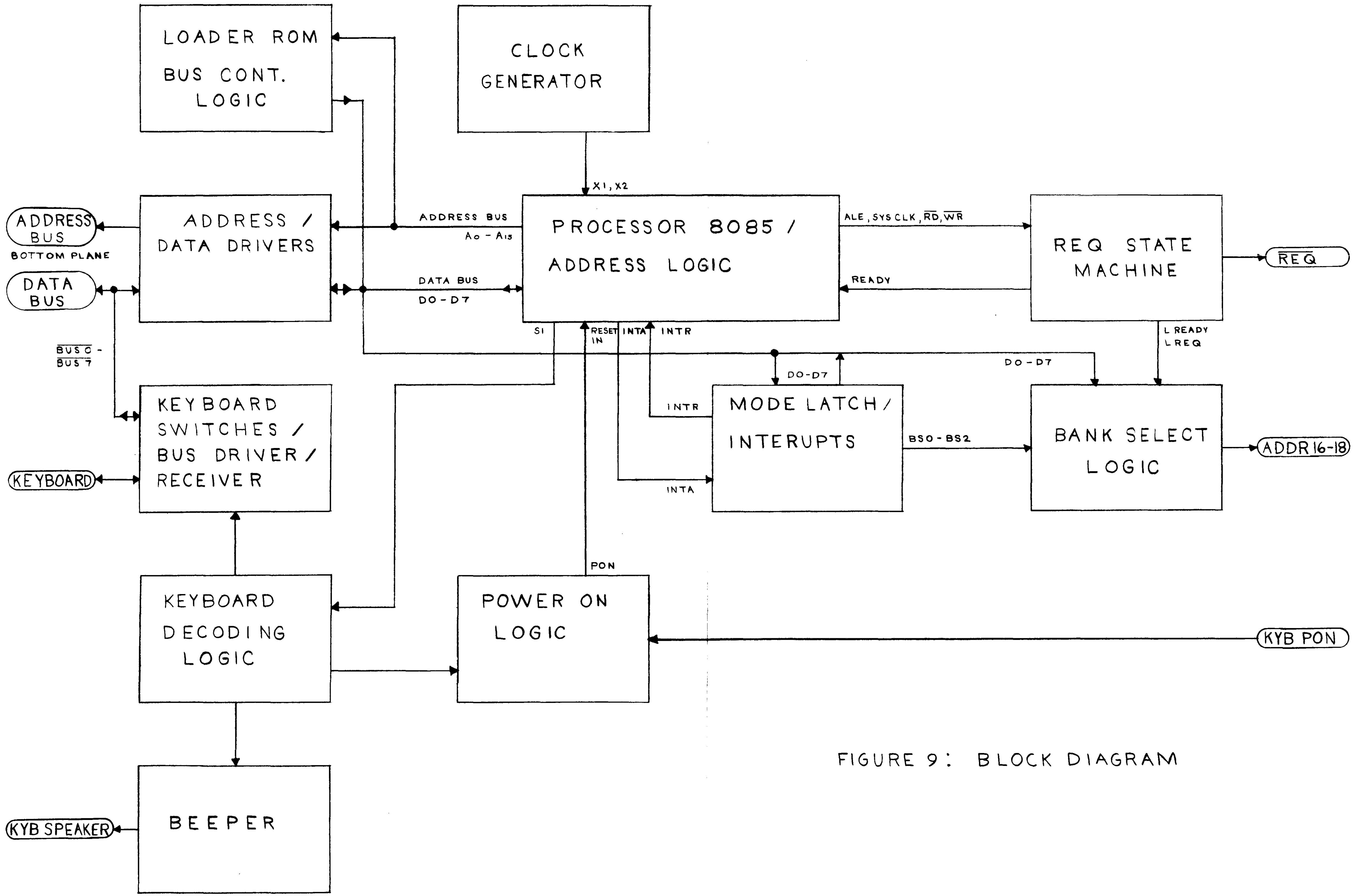


FIGURE 9: BLOCK DIAGRAM

Figure 9
02640-60249 Block Diagram
FEB-14-82 13255-91249

1. RESISTANCE AND CAP. VALUES ARE IN OHMS AND MICROFARADS

2. (X-Y-Z) X=SCHEMATIC PAGE Y=ROW Z=COLUMN

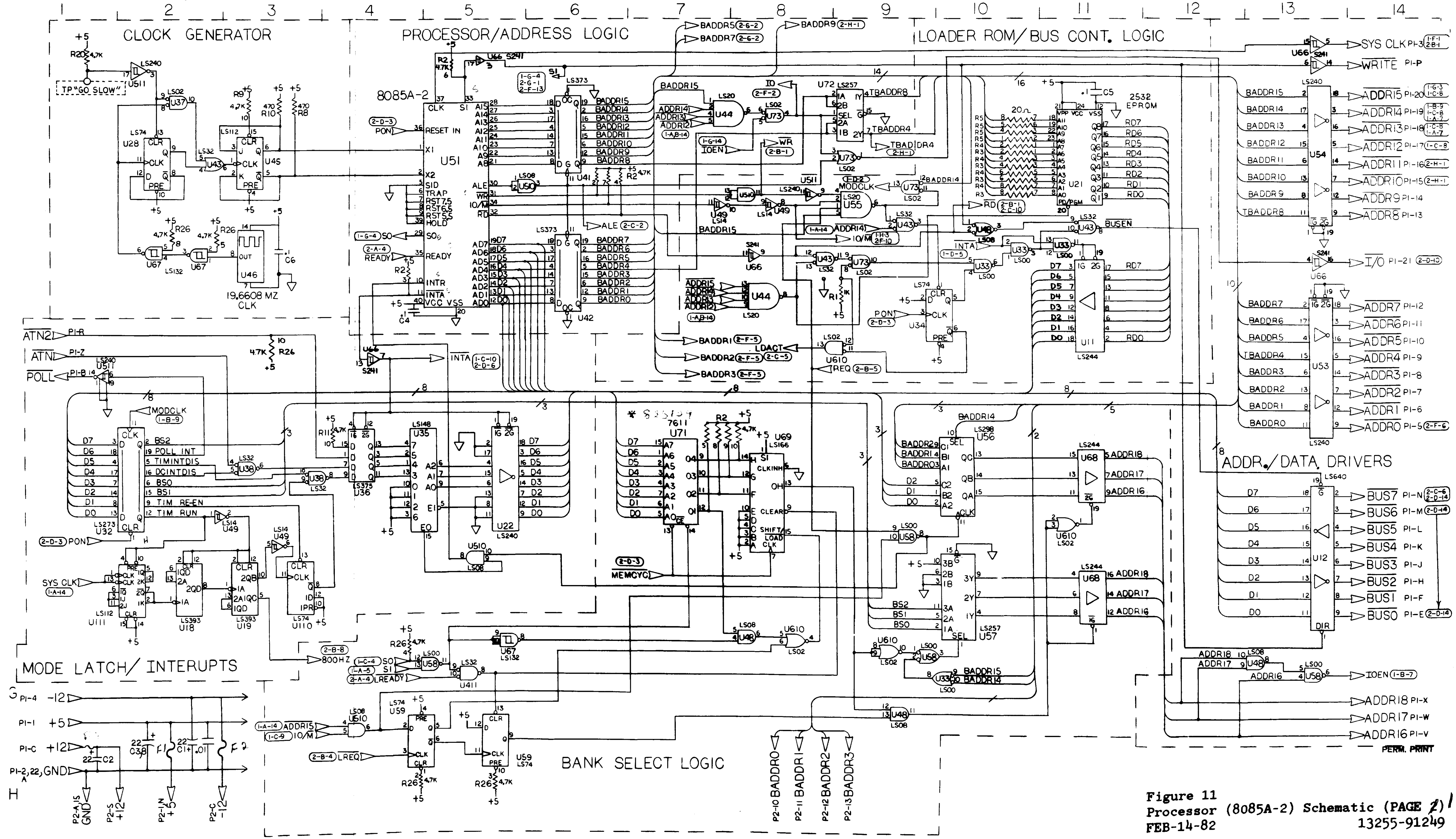


Figure 11
Processor (8085A-2) Schematic (PAGE 1)
FEB-14-82 13255-91249

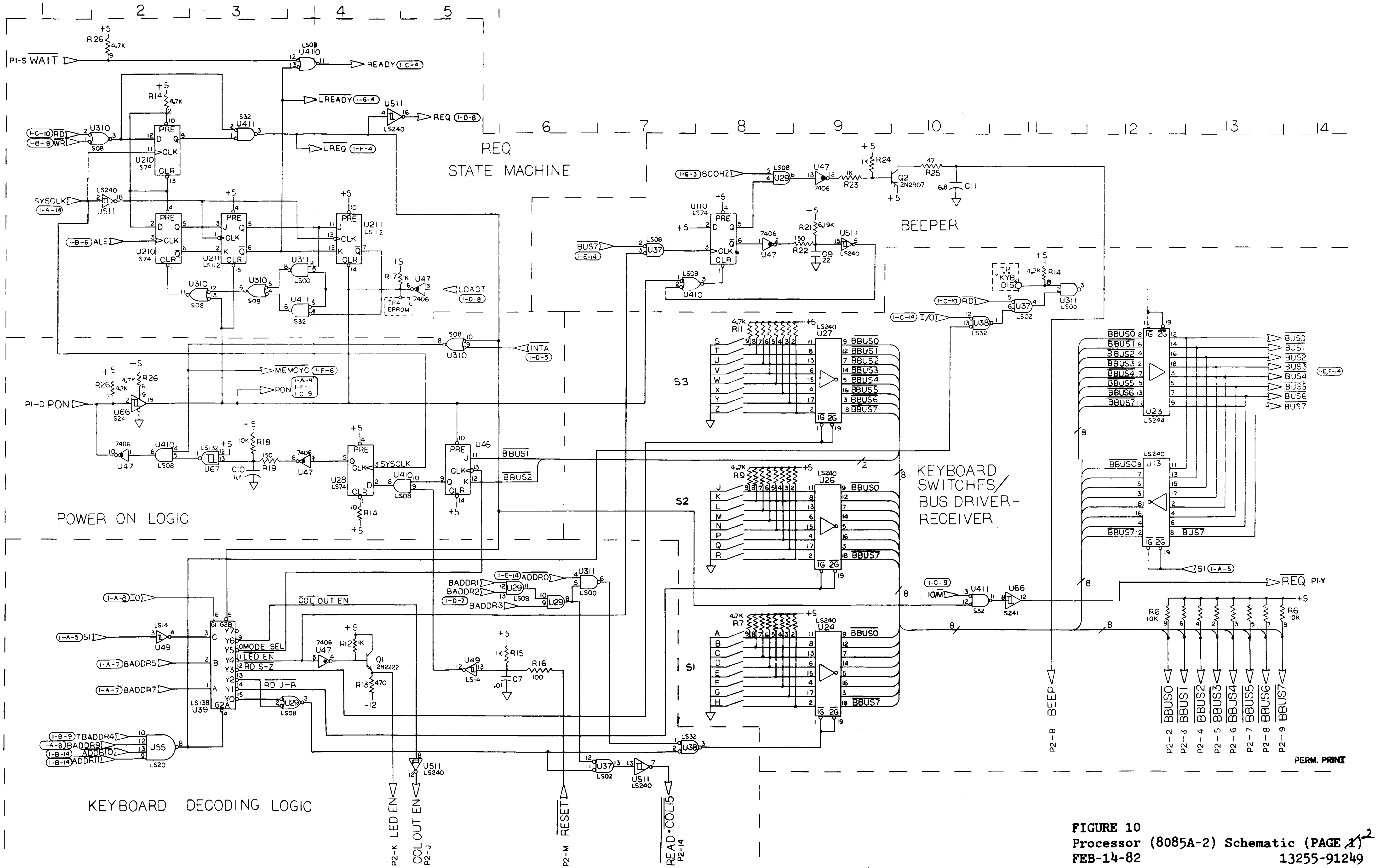
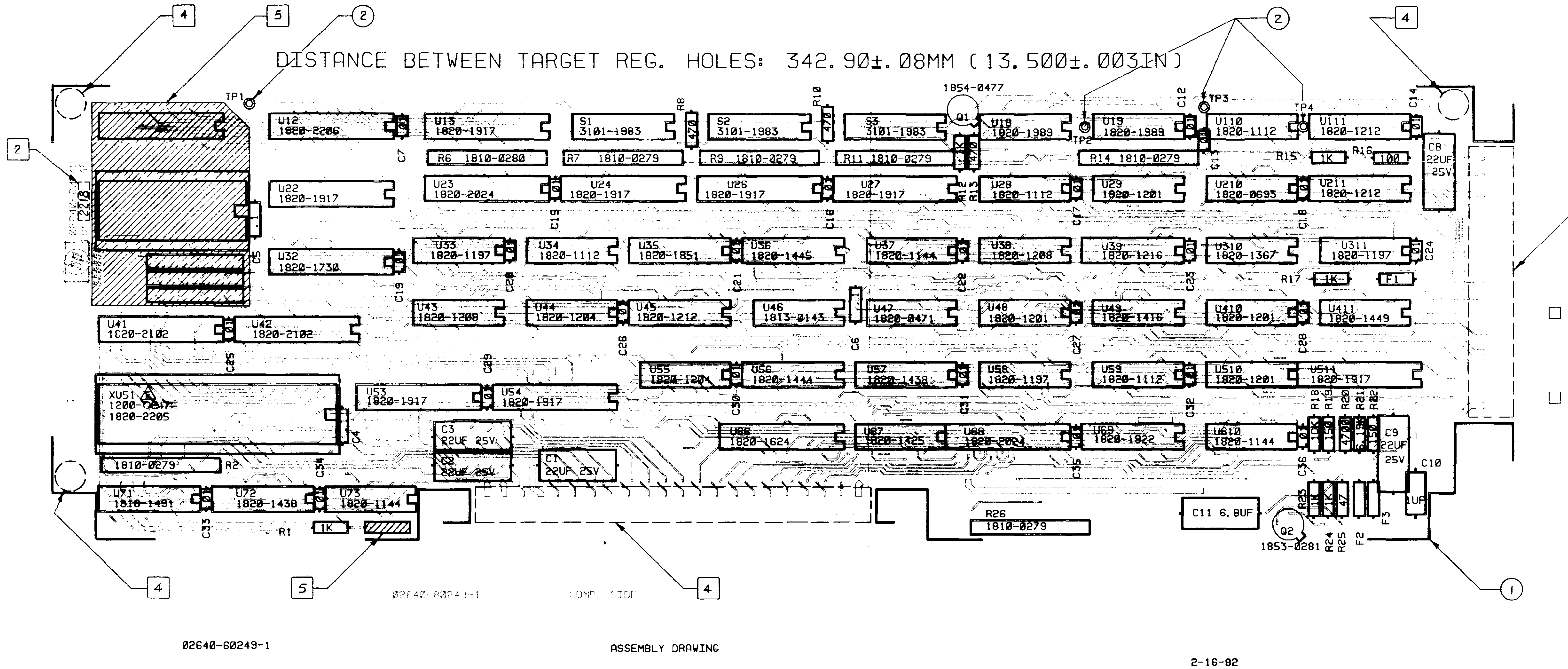


FIGURE 10
Processor (8085A-2) Schematic (PAGE ~~1~~ 2)
FEB-14-82 **13255-91249**



NOTES :

1. *UNLESS OTHERWISE SPECIFIED;*
   ALL RESISTANCE IN OHMS.
   ALL CAPACITANCE IN MICROFARADS.
2. *MARK DATE CODE (OPER. 33)*
3. *SCHEMATIC DIAGRAM D-02640-60249-51 & -52.*
4. *MASK INDICATED AREAS PRIOR TO WAVE SOLDER.*
5. *NO COMPONENTS TO BE LOADED IN SHADED AREA. DO NOT MASK THIS AREA.*

Figure 12
Processor (8085A-2) Component Location Diagram
FEB-14-82 **13255-9149**

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60249	9	1	PROCESSOR/KEYBOARD IF PCA	28480	02640-60249
C1	0180-2879	7	5	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C2	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C3	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C4	0160-4557	0	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C6	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C7	0160-4554	7	25	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C9	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C10	0160-4844	8	1	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-4844
C11	0180-0116	1	1	CAPACITOR-FXD 6.8UF+-10% 35VDC TA	56289	150D685X9035B2
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C23	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C24	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C25	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C26	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C28	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C29	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C30	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C31	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C32	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C33	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C34	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C35	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C36	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
F1	2110-0423	8	3	FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
F2	2110-0423	8		FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
F3	2110-0423	8		FUSE 1.5A 125V NTD .281X.093	28480	2110-0423
Q1	1854-0477	7	1	TRANSISTOR NPN 2N2222A SI TO-18 PD=500MW	04713	2N2222A
Q2	1853-0281	9	1	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
R1	0683-1025	9	6	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	1810-0279	5	6	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R6	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R7	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R8	0683-4715	0	3	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R9	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R10	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R11	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R12	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R13	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R14	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R15	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R16	0683-1015	7	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R17	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R18	0683-1035	1	1	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R19	0757-0284	7	2	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
R20	0683-4725	2	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R21	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-6191-F
R22	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
R23	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R24	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R25	0683-4705	8	1	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R26	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
S1	3101-1983	9	3	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
S2	3101-1983	9		SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
S3	3101-1983	9		SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
TP1	0360-0535	0	4	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U12	1820-2206	3	1	IC MISC TTL LS	01295	SN74LS640N
U13	1820-1917	1	8	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U18	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U19	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U22	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U23	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U24	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U26	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U27	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U28	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U29	1820-1201	6	4	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U32	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U33	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U34	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U35	1820-1851	2	1	IC ENCDR TTL LS	01295	SN74LS148N
U36	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
U38	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U39	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U41	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U42	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U43	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U44	1820-1204	9	2	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U45	1820-1212	9	3	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U46	1813-0143	8	1	IC-OSCILLATOR 9.6608 MHZ	34344	K1148-19.6608MHZ
U47	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
U48	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U49	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U51	1820-2205	2	1	IC MICPROC NMOS 8-BIT	34649	P8085A-2
U53	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U54	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U55	1820-1204	9		IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U56	1820-1444	9	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
U57	1820-1438	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U58	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U59	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U66	1820-1624	7	1	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U67	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U68	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U69	1820-1922	8	1	IC SHF-RGTR TTL LS PRL-IN SERIAL-OUT	01295	SN74LS166N
U71	1816-1491	7	1	IC- ROM 256 X 4 7611-5	34371	HM1-7611-5 PROGRAMMED
U72	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U110	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U111	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U210	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U211	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U310	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U311	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U371	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U410	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U411	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U510	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U511	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U610	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U732	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
XU51	1200-0817	4	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0817
				MISCELLANEOUS PARTS		
	0460-1282	8		TAPE- .5W POLY BRZ	28480	0460-1282
	0890-0043	8		TUBING-FLEX	28480	0890-0043

MANUFACTURERS CODE LIST   AS OF 06/05/82

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
01961	PULSE ENGINEERING INC	SAN DIEGO	CA	92111
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34344	MOTOROLA INC	FRANKLIN PARK	IL	60131
34371	HARRIS SEMICON DIV HARRIS-INTERTYPE	MELBOURNE	FL	32901
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
50088	MOSTEK CORP	CARROLLTON	TX	75006
55576	SYNERTEK	SANTA CLARA	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
91637	DALE ELECTRONICS INC	COLUMBUS	NE	68601