IBM Customer Engineering Handbook

1410 Data Processing System

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IBM

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1410 Data Processing System

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CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM Equipment:

1. Do not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your Manager if you MUST work alone.
2. Remove all power AC & DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked in off position.
4. When it is absolutely necessary to work on equipment having exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in the immediate vicinity.
   b. Rings, wrist watches, chains and bracelets shall not be worn.
   c. Safety glasses shall be worn.
   d. Only insulated pliers or screwdrivers shall be used.
   e. Keep one hand in pocket.
   f. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   g. Avoid contacting ground potential (metal floor strips, machine frames, etc.)
5. Safety glasses must be worn when working on live equipment, soldering, drilling, driving pins and all other conditions that may be hazardous to the eyes.
6. Special safety instructions for handling Cathode Ray Tubes and extreme high voltages must be followed as outlined in CEM's.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Do not lift machines or devices weighing in excess of 60 lbs.
11. All safety changes must be ordered and installed in the prescribed manner.
12. All safety devices such as guards, shields, signs, etc. shall be restored after maintenance.
13. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
14. All machine covers must be in place before machine is returned to customer.
15. Maintain good housekeeping in area of machines while performing and after completing maintenance.
16. Avoid wearing loose clothing that may be caught in moving machinery.

KNOWING SAFETY RULES IS NOT ENOUGH
OBSERVE THEM — FOLLOW THEM
USE GOOD JUDGMENT

THINK SAFETY *WORK SAFELY*

FORM 124-0002-1

Standard Technique
LAY VICTIM IN PRONE POSITION

Elbows bent, one hand on the other. Head on hands, face to one side. Kneel at victim's head on either or both knees.

1 PLACE HANDS

Fingers spread, thumbs touching, heels of hands just below a line between armpits.

2 APPLY PRESSURE

Rock forward slowly until arms are vertical. Keep elbows straight.

3 RELEASE PRESSURE

Rock back slowly. Grasp victim's arms just above elbows. Continue backward.

4 LIFT ARMS

Raise arms until tension is felt for maximum chest expansion. Lower arms to complete cycle.

REPEAT CYCLE 12 TIMES PER MINUTE

Photos Courtesy American National Red Cross

Artificial Respiration
GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects—Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. **Blow** until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

Continue rescue breathing until he breathes for himself.

Thumb and finger positions

Final mouth to mouth position

MACHINE VOLTAGES PRESENT WITH POWER OFF

The following voltages are present under a POWER OFF condition:

1. -48 vdc at:
   - TB 3 and 5 of all dc power supplies
   - Output of -48v supply
   - All thermals
   - Power supply contactor panel
   - TB M on memory array
   - 1414-1,2,3 CE panels
   - 1411A relay gate
2. 115 vac at:
   - All convenience outlets
   - 1411A relay gate
   - Convenience outlet isolation transformer
   - Plenum strips
   - Convenience outlet isolation transformer
3. 208 vac at:
   - T2 and emergency off switches.
4. 24 vac at:

MACHINE VOLTAGES PRESENT WITH DC OFF

The following voltages are present under a DC OFF condition:

1. -48 vdc at:
   - All locations listed under POWER OFF condition
2. 115 vac at:
   - All locations listed under POWER OFF condition
   - Typewriter motor
   - TB pins 4 and 5 of memory array
3. 208 vac at:
   - All locations listed under POWER OFF condition
4. 24 vac at:
   - T2 and emergency off switches

MACHINE SERIAL NUMBERS

Machine Type	Name	Serial Number
1411	CPU	
1415	Console	
1414-1	I/O Sync	
1414-2	I/O Sync	
1414-3	I/O Sync	
1402-2	Rdr/Punch	
1403	Printer	
7631	File Ctrl	
1301	Disk File	
1405	Disk File	
729	Mag Tape Unit	
7330	Mag Tape Unit	
1311	Disk	
1442	Card Reader	

CUSTOMER ENGINEERING MANUALS OF INSTRUCTION

729 II, IV Magnetic Tape Units (Relay)	223-6845-2
1009 Data Transmission Unit	225-6560-0
1011 Paper Tape Reader	227-5546-0
1014 Remote Inquiry Unit	225-6583-0
1014 Adapter to 1414-4, -5, -6	R23-9913-0
1301 Disk Storage	227-5582-2
1403 Printer	225-6492-1
1405 Disk Storage	227-5542-0
1412/1210 Magnetic Character Reader	225-6486-1
1419 Magnetic Character Reader	225-6575-0
7330 Magnetic Tape Unit	223-6943-0
7750 Programmed Transmission Control, Introduction	223-2533-0
7750 Process and Control Storage	223-2540-0
7750 PTC Process Control	223-2570-0
7750 PTC Power Supply and Distribution	223-2579-0
7750 PTC Channel Adapter	223-2544-0
I-O Printer (Modified Selectric)	225-6595-0
60-Cycle SMS Power Supply	225-6478-1
Transistor Component Circuits	223-6889-2
Transistor Theory and Application	223-6783-2

CUSTOMER ENGINEERING MAINTENANCE MANUALS

729 II, III, IV Magnetic Tape Units (Relay)	223-6868-3
1009 Data Transmission Unit	225-6561-0
1011 Paper Tape Reader	227-5545-1
1014 Remote Inquiry Unit	225-6584-0
1301 Disk Storage	227-5581-3
1301 Reference Manual Supplement	R27-5651-0
1403 Printer	225-6493-2
1403 Reference Manual - Print Quality Supplement	225-6581-0
1405 Disk Storage	227-5541-1
1410 DPS Data Flow Diagram	223-2521-0
1410 Reference Card (Instruction Coding)	X24-6502-3
7330 Magnetic Tape Unit	223-6967-2
I-O Printer (Modified Selectric)	225-1726-0

CUSTOMER ENGINEERING INSTRUCTION-MAINTENANCE MANUALS

729 II, IV, V, VI Magnetic Tape Units (NOR)	223-6988-2
1402 Card Read Punch	231-0002-1
1410-1401 Compatibility	223-2597-0
1410 Core Storage	223-2555-0
1410 System Fundamentals and Functional Units	223-2589-0
1411 Input-Output Operations	223-2692-0
1412/1210 Magnetic Character Reader	225-6500-2
1414-1, -2 I-O Synchronizer	223-2554-0
1414-3, -4, -5, -6, -8 I-O Synchronizer	223-2590-0
1414-4, 5 I-O Synchronizer, 1009 Adapter	R23-2557-0
1415 Console, 1411 CE Console	223-2648-0
7223 Model 3 Console Card Reader	223-2562-0
7631 File Control	Z22-2766-0
Standard Modular System	223-6900-2

GENERAL PUBLICATIONS FOR THE 1410

Systems Reference Library -- 1410 Bibliography	A22-0523-0
1410 Reference Manual (General Information)	A24-1407-2
1410 Installation -- Physical Planning	C24-1437-2
Console Error Report Pad	229-3104-0

CHARACTER CODING

Standard BCD Interchange Code

	1 Collating Number	2 Graphics	3 Card Code			4 BCD Code B	A	8	4	2	1	5
NN	00	Blank	No Punches			No Bits						
	01	.	12	3	8	B	A	8		2	1	
	02	口)	12	4	8	B	A	8	4			
SC	03	[	12	5	8	B	A	8	4		1	
	04	<	12	6	8	B	A	8	4	2		
	05	ǂ	12	7	8	B	A	8	4	2	1	GM
NN	06	& +	12			B	A					
	07	$	11	3	8	B		8		2	1	
	08	*	11	4	8	B		8	4			
SC	09	]	11	5	8	B		8	4		1	
	10	;	11	6	8	B		8	4	2		
	11	△	11	7	8	B		8	4	2	1	MC
NN	12	-	11			B						
	13	/	0	1			A				1	
	14	,	0	3	8		A	8		2	1	
	15	% (	0	4	8		A	8	4			
SC	16	~	0	5	8		A	8	4		1	WS
	17	\	0	6	8		A	8	4	2		
	18	##	0	7	8		A	8	4	2	1	SM
NN	19	ↄ		2	8		A					SB
	20	# =		3	8			8		2	1	
	21	@'		4	8			8	4			
SC	22	:		5	8			8	4		1	
	23	>		6	8			8	4	2		
	24	✓		7	8			8	4	2	1	TM
	25	?	12	0		B	A	8		2		PZ
	26	A	12	1		B	A				1	
	27	B	12	2		B	A			2		
	28	C	12	3		B	A			2	1	
	29	D	12	4		B	A		4			
	30	E	12	5		B	A		4		1	
	31	F	12	6		B	A		4	2		
	32	G	12	7		B	A		4	2	1	
	33	H	12	8		B	A	8				
	34	I	12	9		B	A	8			1	
	35	!	11	0		B		8		2		MZ
	36	J	11	1		B					1	
	37	K	11	2		B				2		
	38	L	11	3		B				2	1	
	39	M	11	4		B			4			
	40	N	11	5		B			4		1	
	41	O	11	6		B			4	2		
	42	P	11	7		B			4	2	1	
	43	Q	11	8		B		8				
AN	44	R	11	9		B		8			1	
	45	ǂ	0	2	8		A	8		2		RM
	46	S	0	2			A			2		
	47	T	0	3			A			2	1	
	48	U	0	4			A		4			
	49	V	0	5			A		4		1	
	50	W	0	6			A		4	2		
	51	X	0	7			A		4	2	1	
	52	Y	0	8			A	8				
	53	Z	0	9			A	8			1	
	54	0		0				8		2		
	55	1		1							1	
	56	2		2						2		
	57	3		3						2	1	
	58	4		4					4			
	59	5		5					4		1	
	60	6		6					4	2		
	61	7		7					4	2	1	
	62	8		8				8				
	63	9		9				8			1	

Two-of-Five Code

Digits	Bits 0	1	2	4	8
0			X		X
1	X	X			
2	X		X		
3		X	X		
4	X			X	
5		X		X	
6			X	X	
7				X	X
8	X				X
9		X			X

Qui-Binary Code

Card Code	BCD	True Add	Complement Add
0	8-2	Q0 B0	Q8 B1
1	1	Q0 B1	Q8 B0
2	2	Q2 B0	Q6 B1
3	1.2	Q2 B1	Q6 B0
4	4	Q4 B0	Q4 B1
5	1.4	Q4 B1	Q4 B0
6	2.4	Q6 B0	Q2 B1
7	1.2.4	Q6 B1	Q2 B0
8	8	Q8 B0	Q0 B1
9	1.8	Q8 B1	Q0 B0

MFI CODES FOR 1410

MFI Code	Feature	MFI's Required for Feature
S1	10K storage or greater	S1
S10	10K storage only	S1,S10
S2	20K storage or greater	S1,S2
S20	20K storage only	S1,S2,S20
S4	40K storage or greater	S1,S2,S4
S40	40K storage only	S1,S2,S4,S40
S6	60K storage or greater	S1,S2,S4,S6
S60	60K storage only	S1,S2,S4,S6,S60
S8	80K storage or greater	S1,S2,S4,S6,S8
S80	80K storage only	S1,S2,S4,S6,S8,S80
Z0	1401 compatibility on 10K 1410	Z0
Z1	1401 compatibility on 20K or greater 1410	Z0,Z1
L1	Overlap on first channel	L1
L10	Overlap on 10K machine only	L1,L10
L2	Tape or file on second channel (includes overlap on second channel)	L1,L2
B1	Basic I/O Buffer	B1
B2	Basic print Buffer	B1,B2
B3	100 print positions, alphanumeric chain	B1,B2,B3
B4	Additional 32 alphanumeric print positions	B1,B2,B3,B4
B5	Any serial device on basic I/O Buffer (includes a six buffer core array)	B1,B5
B6	500 cps paper tape reader	B1,B5,B6
B8	First 1014 Remote Inquiry	B1,B5,B8
B9	Additional (two-ten) 1014's	B1,B5,B8,B9
B20	First 5 channel telegraph translator	B1,B5,B20
B21	First section of telegraph receive-receive adapter	B1,B5,B20,B21
B21A	Second section of telegraph receive-receive adapter	B1,B5,B20,B21,B21A
B22	Telegraph send-receive adapter	B1,B5,B20,B22
B23	First section of telegraph send-send adapter	B1,B5,B20,B23
B23A	Second section of telegraph send receive adapter	B1,B5,B20,B23,B23A
B24	Western Union Attachment	B21,B21A,B22,B23, B23A
B40	51 column card feature	B1,B40
B41	100 print positions, numeric chain	B1,B2,B41
B42	Additional 32 print positions, numeric	B1,B2,B41,B42
B43	1009 Attachment	B1,B5,B43
B50	Basic Model 5 or 6 I/O Buffer and Controls	B50
B51	Model 5 I/O Buffer	B50,B51
B52	Model 6 I/O Buffer	B50,B52
B53	Column binary feature	B1,B53
B54	Space suppress feature	B2,B55
B55	Model 8 I/O Buffer	B2,B55
B56	High Speed Printer	B2,B56

MFI Code	Feature	MFI's Required for Feature
F0	1405 or 1301 (either channel)	F0
F1	1405 or 1301 on first channel	F0, F1, F8 or F9
F2	1405 on first channel	F0, F1, F2, F8
F3	1301 on first channel	F0, F1, F3, F9
F5	1405 or 1301 on second channel	F0, L2, F5, F8, or F9
F6	1405 on second channel	F0, F5, F6, L2, F8
F7	1301 on second channel	F0, F5, F7, F9, L2
F8	1405 on either or both channels	F0, F8
F9	1301 on either or both channels	F0, F9
K1	I/O Buffer on second channel	K1
K5	Serial device on second channel	K1, K3
K53	Column binary feature on second channel	K1, K53
M0	Any tape system to either channel	M0
M1	Any tape on the first channel	M0, M1
M2	729 Mod 2 (either channel)	M0, M6, M1 or M5, M2
M3	7330 units (either channel)	M0, M1 or M5, M3
M4	729 Mod 4 Tape Units (either channel)	M0, M6, M1 or M5, M4
M5	Any tape on second channel	M0, L2, M5
M6	729 II or IV on either channel	M0, M6
R0	1311 File	F3, F7
R1	1311 File on first channel	F3, R0
R2	1311 File on second channel	F7, R0
SCN0	1311 scan feature	R1 or R2
SCN1	1311 scan feature on first channel	SCN0
SCN2	1311 scan feature on second channel	SCN0
A0	1412 attachment either channel	A0
A1	1412 attachment channel 1	A0, A1
A2	1412 attachment channel 2	A0, L2, A2
C1	program addressable clock	C1
H1	corporate simplex interface on channel 1	L1, Y1
H2	corporate simplex interface on channel 2	L2, Y1
P1	Paper tape punch on channel 1	P1
P2	Paper tape punch on channel 2	P2
Y1	priority processing on channel 1	Y1
Y2	priority processing on channel 2	K1, K5, Y1

ABBREVIATIONS USED IN ALD'S

A+S	Add or subtract
AW	A channel word mark
B	B cycle
B 1-9	B channel has a character containing a digit from 1 to 9
BW	B channel word mark
CMP	Compare
CND	Condition
Coml at	Commercial at
CPR	Computer
CR Disable	Control register disable
D	D cycle
INTR	Interrupt
Last ex- Next to Last	Last execute cycle and next to last logic gate
LIROC	Last instruction readout cycle
MDL	Mpy div last latch
N	No scan
RA	Zero and add
RC	Adder carry
RS	Zero and subtract
RST	Reset
S	Complement latch
T	True latch
TLU	Table look up
TW	Shielded or grounded half of a twisted pair
U	Units latch
Y	Body latch
X	Extension latch
+	Or
.	And
1	1st scan
2	2nd scan
3	3rd scan

OP CODE LENGTHS

Op Code/Instr	Function	Acceptable Lengths		
A (A) (B)	Add	1	6	11*
S (A) (B)	Subtract	1	6	11*
? (A) (B)	Zero and Add	1	6	11*
! (A) (B)	Zero and Subtract	1	6	11*
@ (A) (B)	Multiply	1	6	11*
% (A) (B)	Divide	1	6	11*
J (I) d	Branch if Internal Ind On	1	7*	
R (I) d	Branch if I/O Status Ind On (Ch 1)		7*	
X (I) d	Branch if I/O Status Ind On (Ch 2)		7*	
B (I) (B) d	Branch if Char Equal	1	6	12*
W (I) (B) d	Branch if Bit Equal	1	6	12*
V (I) (B) d	Branch on WM and/or Zone	1	6	12*
D (A) (B) d	Move Data	1	6	12*
Z (A) (B)	Move Char and Suppr Zeros	1	6	11*
E (A) (B)	Move Char and Edit	1	6	11*
C (A) (B)	Compare	1	6	11*
T (A) (B) d	Table Lookup	1	6	12*
G (C) d	Store Addr Reg		7	
, (A) (B)	Set Word Mark	1	6	11*
¤ (A) (B)	Clear Word Mark	1	6	11*
/ (I) (B)	Clear Storage and Branch	1	6	11*
. (I)	Halt and Branch	1	6	
N	No Op	-	-	--
M (X) (B) R/W	Read or Write without WM			10
L (X) (B) R/W	Read or Write with WM			10
U (X) d	Control Unit		5	
K d	Stacker Sel and Feed	2		
F d	Control Carriage	2		
Y (I) d	Priority Test		7	

* Indicates interruptible length

SIGNIFICANCE OF TAG BITS

Hundreds		Tens		Index with	Locations	
B-Bit	A-Bit	B-Bit	A-Bit	Register	From	To
8	4	2	1			
			X	1	00025	00029
		X		2	30	34
		X	X	3	35	39
	X			4	40	44
	X		X	5	45	49
	X	X		6	50	54
	X	X	X	7	55	59
X				8	60	64
X			X	9	65	69
X		X		10	70	74
X		X	X	11	75	79
X	X			12	80	84
X	X		X	13	85	89
X	X	X		14	90	94
X	X	X	X	15	95	99

BRIEF OP CODE DESCRIPTIONS

This section contains a short description of each op code. The following abbreviations are used:

CA	complement add
Chg	change
Dd	dividend
Dv	divisor
fd	field
Gt V	greater value
HO	high order
Inv	inverted
M'cand	multiplicand
Mult'r	multiplier
nc	no change
NZ	no zone
Om	omit
SF	standard form
Sn	sign
TA	true add

Operation	Format	Function	Effect on Zones and Sign				Word Mark			Special Effects
			A	B	Eff	Results	A	B	Stop	
Add (two fd)	A (A) (B)	Add Num A fd to B fd	Z	nc	--	Om B fd	nc	nc	B	If B fd > A fd add 0 to extra HO Pos B
			Sn	nc	SF	Chg	HO	HO	--	If B fd < A fd, HO of A fd not processed
			+	+	TA	+	--	--		
			+	-	CA	Sn Gt V	--	--		
			-	+	CA	Sn Gt V	--	--		
			-	-	TA	-	--	--		
Add (one fd)	A (A)	Used to double A fd	Z	nc	--	In A fd	HO	--	A	A fd must have a WM in HO position
			Sn	nc	nc					
Subt (two fd)	S (A) (B)	(B) - (A)	Z	nc	--	In B fd	HO	HO	B	Notation - same as (add two fd)
			Sn	nc	SF	Chg				
			+	-	TA	-	--	--		
			+	+	CA	Sn Gt V	--	--		
			-	-	CA	Sn Gt V				
			-	+	TA	+				
Subt (one fd)	S (A)	Num (A) always	Z	nc	--	In A fd	HO	--	A	A fd must have WM in HO position
Zero & Add (two fd)	? (A) (B)	Stores A fd in B fd	Z	nc	Chg NZ	Om B fd	HO	HO	B	Sign of result in B fd same as sign of A fd
			Sn	nc	Chg SF	Use A fd Sn				If A > B, HO Pos A not processed

Operation	Format	Function	Effect on Zones and Sign	Word Mark	Special Effects
Zero & Add (one fd)	? (A)	Strip A fd of all zones except sign	A B Eff Results Z Chg -- NZ In A fd Sn Chg -- SF Sn to SF	A B Stop HO -- A	Also changes (blank, 8-3, 8-4, etc to num equiv (0, 3, 4, etc.)
Zero & Subt (two fd)	! (A) (B)	Stores Num A in B fd with opposite sign	Z nc Chg NZ In B fd Sn nc Chg Inv A fd Sn (SF)	HO HO B	Notation same as zero and add
Zero & Subt (one fd)	! (A)	Strips A fd of zones and change sign	Z Chg -- NZ In A fd Sn Chg SF (inv sign)	HO -- A	Same as zero & add (one field)
Multiply	@ (A) (B)	A fd M'cand repetitively added to B fd (Prod) (Mult'r in HO Pos B)	Z nc Chg NZ In B fd Sn S + + + of results - - + in B fd + - - - + -	HO HO B (when 0 is in Mult'r)	B length - add 1 to sum of digits in M'cand & Mult'r digit of 5 or greater causes compl add A and B addresses are units position of respective fields

Operation	Format	Function	Effect on Zones and Sign	Word Mark	Special Effects
Divide	% (A) (B)	Dd (B fd) divided by Dv (A fd) Result in HO of B fd	A B Eff Results Z nc Om Note In HO of Sn nc SF Note B fd - + - + - - (like signs-same sign)	A B Stop HO HO B cycle, TA,B-channel B bit	A address-Units of Dv B address-HO Pos of Dd B length -- add 1 to sum of Dd, & Dv digits

NOTE: To insure that the quotient field contains zeros and the sign bit configuration is AB, move dividend into B field by using a ZERO AND ADD instruction.

Operation	Format	Function	Mod	Function of Mod	Special Considerations
Branch (unconditional)	J (I) blank	When executed causes branch to (I) address	Blk	Must be in format or branch will not take place	
Branch (conditional)	J (I) d	Branches if indicator tested is "on"	Blk	Unconditional	Compare indicators are turned off by next comp table lookup, or test character and branch, and are set to that operation. Overflow indicators are turned off by this branch test if successful.
			9	Carriage channel 9	
			@	Carriage overflow (Channel 12)	
			/	Compare unequal	
			S	Compare equal (B = A)	
			T	Compare low (B < A)	
			U	Compare high (B > A)	
			V	Zero balance	
			W	Divide overflow	
			Z	Arithmetic overflow	
			Q	Branch inquiry	
			1	Overlap in process on channel 1	
			2	Overlap in process on channel 2	
			R	Printer carriage busy	
			K	Causes CPU to branch to the I address immediately when a TM is read.	This branch test op code is used on T005 diagnostic
Priority Test	Y(I) d	Test for interrupt cause	E	Unconditional branch and turn-on priority alert mode.	
			X	Unconditional branch and turn-off priority alert mode.	

Operation	Format	Function	Mod	Function of Mod	Special Considerations
			Q	Branch if inquiry priority request.	
			S	Branch if channel 1 seek priority request.	
			T	Branch if channel 2 seek priority request.	
			U	Branch if I-O unit priority request.	
			1	Branch if channel 1 overlap priority request.	
			2	Branch if channel 2 overlap priority request.	
			N	Branch if outquiry priority request.	
Branch if I/O status indicator ON	R (I) d X (if channel 2)	Conditional branch Executed if status indicator designated by Mod in ON	1 Bit	Branch if I/O unit not ready (mechanical)	Internally set at end of 1 time. If ind is ON, operation is ended No data transferred
			2 Bit	Branch if I/O unit is "busy" (mechanical)	Set if I/O devices are in a busy condition, before any data transfer (During 1 ph)
			4 Bit	Branch if I/O data check (data transfer)	Set ON after transfer of data involving I/O devices if parity error was detected.
			8 Bit	Branch if I/O condition	Set during move or load instruction (end-of-file, cd lever, etc)
			A Bit	Branch if I/O has no transfer	Set ON if no data was available to transfer
			B Bit	Branch if I/O has wrong length record	Set ON if record written to/from storage is not correct length

Operation	Format	Function	Mod	Function of Mod	Special Considerations
			All (≠) Bits	Branch if any indicator is ON.	Used to branch to a test program area, to determine and indicate exact status.
			@	Read back check (write disk check)	
Branch if character equal	B (I) (B) d	Compare bit configuration of the character at B address to the (d) character. Branches if equal	d	Character of Mod used to compare.	This instruction also sets the Hi-Lo-equal indicator. Hi is set if B character higher than (d) WMs do not affect this test as only one character is used.
Branch if bit is equal	W (I) (B) d	Branches if bit in B character matches bit in d character	d	Any legitimate character or bit configuration can be used.	If ANY bit in B matches ANY bit in d, a branch will be executed.
Branch on WM or Z equal	V (I) (B) d	Branches if character at (B) has WM or zone combination specified by (d)	1 Bit 2 Bit 1 & 2	A one bit in Mod characters tests for a WM. A two bit compares zone bits Allows both or either comparison	Characters possible for modifier: Br on Wm - 1 Br on Z - 2,B,K,S Br on both- 3,C,L,T NOTE: This branch is a test of one character so no WMs are needed or affected.

Data Move Operation and General Data Operations

Data Moving - Concerns moving data left to right (reverse scan) or right to left (forward scan) from the A field to the B field with or without word marks. Data can be moved by fields or by records. If a data field is moved, the operation can be programmed to stop at: A-fd WM, B-fd WM, A- or B-fd WM. If a record is moved the operation can be programmed to stop at: first WM in either A- or B-fd, first RM in A-fd, First GM/WM in A-fd, first RM or GM/WM in A-fd.

Operation	Format	Function	d Character Control Bits	Control by Mod	Special Considerations
Move Data	D (A)(B) d	Data is moved L-R, or R-L, from A field to B field, under control of d.	1	Trans Num portion of data field	Blank d - (No 1,2,4) Scan for WMs, RMs, or GM-WMs
			2	Trans Zone portion of data field	1....Only the part of A field transferred replaces corresponding B field. Rest of B field is unchanged.
			4	Trans WMs from A field to B field	2....If move is L-R A address specifies high order of A-fd
			8 Bit No A Bit No B Bit	Stop trans, or scan at first WM sensed in either field	
			(L to R Move) A Only B Only A & B	Stop at A-fd RM Stop at A-fd GM-WM Stop at A-fd RM or GM-WM	3....If move is R-L A address specifies units position of A-fd.

Operation	Format	Function	d Character Control Bits	Control by Mod	Special Considerations
			No 8 Bit No A Bit No B Bit (R to L Move) A Only B Only A & B	Trans or scan only one position. Stop at A-fd WM Stop at B-fd WM Stop 1st WM either fd	When scan operation is designated, no data is transferred.
Move Characters and suppress 0's	Z (A)(B)	Moves data in A fd to B-fd	Special Functions and WM notes High order 0's and commas are replaced by blanks.	A-fd must have WM to define length of fd moved to B-fd. B-fd WM removed (in this area).	Special char not recognized as significant digit A-fd is unchanged.

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Operation	Format	Function	Mod	Mod Affect	Word Marks	Notes
Comparing	C (A)(B)	Data in A field compared to data in B field. Result sets a (B < A) or (B=A) or (B > A) indicator.		No Modifier	Operation is terminated by either an A-fd or B-fd word mark. If A-fd is shorter than B-fd, A-fd must have WM. In this case Hi-ind is on.	Compare indicators must be tested before the next: 1. Compare 2. Branch if char equal 3. Table lookup (Once B=A ind is set OFF, cannot be set ON for rest of operation.)
Table Lookup	T(A)(B) d	Causes search for a table argument that is higher than, lower, or equal to the search argument. Search type controlled by d modifier. Search ended by first argument satisfying modifier.	b 1 2 3 4 5 6 7	Search to end of table Search for lower Search for equal Search for equal or lower Search for higher Search for higher or lower Search for equal or high Stop on any	A-fd WM over HO position. B-fd WM over each table argument HO position. A-fd WM stops compare.	Table fd includes argument in LO positions, function in HO positions. Comparison resumes one position to left of B-fd WM. Each table field must be as long as or longer than search fd. Short table fd ends operation and sets Hi latch.
Editing	E(A)(B)	Move characters and edit. For detailed explanation, refer to Section in Reference Manual (Form A24-1407-2)				

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Miscellaneous Oper	Format	Function	Mod	Mod Function	Word Marks	Notes
Store address Reg (This Instruction cannot be indexed)	G(C) d	Contents of register specified by the "d" are stored in the C-field.	A B E F T	Store A Reg Store B Reg Store E Reg Store F Reg Store RTC	WMs in C field have no effect Zones in C-fd are not disturbed	C address specifies Lo order position where the register will be stored. 5 digit field is stored. HO digit will be 0 or 9. Hours read out as continental time. Minutes read out as 100ths of hour. Example: 1:30 pm = 01350
Set Word Mark	,(A)(B)	Sets WM in specified A & B address locations		No Modifier		Data characters in the specified locations are undisturbed.
	,(A)	Sets WM in specified A address loc only				
	, (No address)	Sets WMs in locations specified by AAR and BAR (chained from previous operation)				
Clear Word Mark	¤ (A)(B)	Same functions as Set WM for two addresses, one address or no address except this function CLEARS the WMs in the specified positions.				

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Miscellaneous Oper	Format	Function	Mod	Mod Function	Word Marks	Notes
Clear Storage	/ (B)	Clears data & WMs (R to L) form the specified B address, to and including the nearest 100s position.		No Modifier	WM are cleared in the areas specified	If no address, chained contents of B register are used as B address
Clear Stg and Branch	/ (I)(B)	Same effect as CLEAR STORAGE except next Inst from I address			WMs are cleared in area specified.	THIS IS AN UNCONDITIONAL BRANCH
Halt	.	Stops. Start key starts program with the next sequential instruction.				
Halt-Branch	. (I)	Stops. Start key starts program at I address				Unconditional Branch After Halting
No Operation	N	Can be substituted for the operation code of any instruction to make the instruction ineffective.			WMs not affected	

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I/O Unit	Op Code	X Ctl Field		d Modifier	Operation	Notes
Card Reader	M or L	%10	(B)	R Read	Initiate feed cycle. Trans 80 characters from read buffer to core storage. Read card into read buffer. Stack card in NR pkt.	If L op code is used, word separator characters are read into storage as WMs and are associated with the following data character
	M or L	%11	(B)	R Read	Same as above. Except Stack 1.	
		%12	(B)	R Read	Same as above. Except 8/2 pkt.	
		%19	(B)	R Read	Trans 80 characters from read buffer to core storage. THERE IS NO CARD FEED OR STACK/SEL OPERATION.	A GM-WM must appear in the core storage pos to immediate right of data record. This stops operation when sensed.
	K or 4		------	0 Sel NR 1 Sel Rd 1 2 Sel Rd 8/2	Initiate feed cycle. Read card into read buffer. Stack card in designated pocket.	SHOULD BE USED ONLY AFTER A READ CARD INST WITH 9 IN UNITS OF CONTROL FIELD.
Card Punch	M or L	%40	(B)	W Punch	Transfer 80 characters from core storage to punch buffer. Punch a card-stack in NP pkt.	If L op-code is used, WMs are translated to word separators and are punched to left of its associated character.
		%44	(B)	W Punch	Same as above, except pkt 4.	
		%48	(B)	W Punch	Same as above, except pkt 8/2.	

*See notes, page 36

I/O Unit	Op Code	X Ctl Field		d Modifier	Operation	Notes
1403 Printer	M or L	%20	(B)	W	Transfer 100 or 132 characters to print buffer. Print a line.	Word marks in CPU are ignored.
		%20	(B)	W	Transfer 100 or 132 characters to print buffer. Print a line.	WMs over characters are translated as word separators and print as a blank to left of associated character.
	M	%21	(B)	W	Transfer 100 or 132 char record to print buffer. Print a line.	Prints "1" for each position that contained a WM. All other positions print nothing.
I/O Printer	M or L	%TO	(B)	R	Unlocks keyboard so keyed data may be read into storage.	L-mode: WMs erased and entered. M-mode: WMs in storage undisturbed.
	M or L	%TO	(B)	W	Transfer data from CPU to I/O printer and print.	WMs printed in L-mode only.
Card Reader (with column binary feature)		Read instruction is normal format. Special test branch instruction -- J(I)M -- must be executed prior to read instruction. Program will branch if card in 1414 buffer is a col binary card. 160 position input field must be provided for col binary card.				
Card Punch (with column binary feature)	M or L	%8n	(B)	W	Punch card in column binary mode.	B-field is 160 positions. "n" may be 0, 4, or 8.

I/O Unit	Op Code	X Ctl Field		d Modifier	Operation	Notes
1405, 1301 or 1311	M or L	%F0	(B)	R	Initiate seek of selected arm and module to address stored in (B) location.	Format of address: AMDDTTR0 ‡
1405, 1301 or 1311	M or L	%F1	(B)	R	Read or write single record. 200 characters in M-mode. 176 characters with WMs in L-mode.	(B) address must be same as used in seek instruction: AMDDTTR0 ‡ (176 pr 200 pos) ‡
1405, 1301	M or L	%F2	(B)	R or W	Read or write full track. 1000 characters in M-mode. 880 characters with WMs in L-mode.	Same as M/L %F1 except record area must be 1000 pos for M-mode and 880 pos for L-mode.
1405, 1301 or 1311	M or L	%F3	(B)	W	Read back check. Compares data written to source data.	Must follow each file write before any other file operation.
1405	M	%F4	(B)	W	Write indelible address	Writes 7 char address from (B) location in storage (arm is not written). Write address switch must be ON.
1011	M or L	%P1	(B)	R	Reads paper tape in move or load mode. On completion of transfer scan, 1011 will "go" to fill buffer again.	1011 tape read will stop when 80 character buffer is filled or any character encoded as EOR is read.

Note: For detailed information about 1301 instructions see IBM 7631 File Control CE Instruction-Maintenance Manual, Form Z22-2766-0. 1311 instructions are covered in detail in 1411 Input-Output Operations CE Instruction-Reference Manual, Form 223-2692-0 .

I/O Unit	Op Code	X Ctl Field		d Modifier	Operation	Notes
1014	M or L	%Qn	(B)	R or W	Read or write up to 80 character record to selected 1014	"n" position of X-ctl field may be 0 or 1. Each group may have 10-1014's.
1009	M or L	%D0	(B)	R or W	Data Transmission Unit. Communicates directly with other 1400 and 7000 systems. Also reads and writes to 7701 or 7702 Mag Tape Trans Terminals.	1 1009 adapter per 1414-4 or 5
Telegraph	M or L	%Ln	(B)	R or W	Read or write variable length record from remote telegraph units	n=0, 1, or 2. Each group may have variable number of remote units.
7223-3 (console card reader)	M or L	%Z0	(B)	R	Read 80 char card into CPU	Not buffered
729 and 7330	M or L	%Un	(B)	R or W	Read or write magnetic tape in M-mode or L-mode	"$" modifier: read tape to end of storage or IRG. "X" modifier: write tape to end of storage.

I/O Unit	Op Code	X Ctl Field		d Modifier	Operation	Notes
729 and 7330	U	% Un	---	x	Unit control operation. Tape unit designated by "n" performs operation specified by "x".	"x" modifiers: B-backspace tape record E-skip and blank tape M-write tape mark R-rewind U-rewind and unload A-start tape and immediate disconnect. CPU continues and tape reads under control of TAU. Used in T005 diagnostic.
Reader	K	---	---	d	Initiates feed cycle and selects card into pocket designated by "d" (no transfer scan)	0-normal read pocket 1-1pocket 2-8/2 pocket 4,8 controls punch stacker selection in 1401 mode
1403 Printer	F or 2	---	---	d	Cause carriage to execute space or skip operation specified by "d"	1-immediate skip to channel 1 2-immediate skip to channel 2 3-immediate skip to channel 3 4-immediate skip to channel 4 5-immediate skip to channel 5 6-immediate skip to channel 6 7-immediate skip to channel 7 8-immediate skip to channel 8

I/O Unit	Op Code	X Ctl Field	d Modifier	Operation	Notes
					9-immediate skip to channel 9 0-immediate skip to channel 10 #-immediate skip to channel 11 @-immediate skip to channel 12 A-skip after print to channel 1 B-skip after print to channel 2 C-skip after print to channel 3 D-skip after print to channel 4 E-skip after print to channel 5 F-skip after print to channel 6 G-skip after print to channel 7 H-skip after print to channel 8 I-skip after print to channel 9 ?-skip after print to channel 10 .-skip after print to channel 11 ¤-skip after print to channel 12 J-1immediate space K-2 immediate spaces L-3 immediate spaces /-1 space after print S-2 spaces after print T-3 spaces after print

I/O Unit	Op Code	X Ctl Field		d Modifier	Operation	Notes
I/O No-Operation	M or L	XXX	(B)	Q or V	Used in interrupt testing. Forces setting of status indicators for sel unit making them available for testing. No data are transferred.	Standard I/O instruction format except for d modifier. "d" mod: Q-Input status indicators V-Output status indicators

Notes on I/O Operation Codes

* Each I/O instruction must be followed by a R(I) ‡ before the next I/O instruction on that channel. A specific "R(I)d may be used as long as the branch is executed. R(I) ‡ for Channel 1, X(I) ‡ Channel 2.

Hundreds position of X Ctl Field for I/O operations may be:
% Channel 1 non-overlapped
@ Channel 1 overlapped
¤ Channel 2 non-overlapped
* Channel 2 overlapped

COMMON OP CODE GROUPING CHART

		1410 Op Codes																												
	COMMON OP CODE GROUPING LINES	?	!	A	S	@	%	E	Z	C	W	V	/	.	,	¤	U	D	J	B	R	X	G	T	M	L	K	F	N
Instruction Read-Out	Percent Type Op Codes																X								X	X				
	Not Percent Type Op Codes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		X	X	X	X	X		X						
	Addr Dbl Op Codes	X	X	X	X								X		X	X			X		X	X								
	Not Addr Dbl Op Codes					X	X	X	X	X	X	X		X			X	X		X			X	X	X	X	X	X		
	1 Addr Plus Mod Op Codes																X		X		X	X	X							
	2 Addr No Mod Op Codes	X	X	X	X	X	X	X	X	X			X		X	X							X							
	2 Addr Plus Mod Op Codes										X	X						X		X				X	X	X				
	2 Address Op Codes	X	X	X	X	X	X	X	X	X	X	X	X		X	X		X		X				X	X	X				
	Addr Type Op Codes	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				
	2 Char Only Op Codes																										X	X		
	C Cycle Op Codes					X	X																	X						
	No C or D Cy Op Codes							X	X	X	X	X	X	X	X	X		X	X	X										
	No D Cy at 1 Ring 6 Ops	X	X	X	X			X	X	X	X	X	X	X	X	X		X		X				X						
	No Index On 1st Addr Ops																X						X		X	X				

1410 Op Codes

	COMMON OP CODE GROUPING LINES	?	!	A	S	@	%	E	Z	C	W	V	/		,	⌑	U	D	J	B	R	X	G	T	M	L	K	F	N
Operational	Reset Type Op Codes	X	X																										
	Add or Subr Op Codes			X	X																								
	Mpy or Div Op Codes					X	X																						
	Add Type Op Codes	X	X	X	X																								
	Arith Type Op Codes	X	X	X	X	X	X																						
	E or Z Op Codes							X	X																				
	Compare Type Op Codes									X										X				X					
	Branch Type Op Codes *										X	X	X	X					X	X	X	X							
	No Branch Op Codes	X	X	X	X	X	X	X	X	X					X	X	X	X					X	X	X	X	X	X	
	Word Mark Op Codes														X	X													
	M or L Op Codes																								X	X			

* Not a line name, a grouping only.

1410 Op Codes

	COMMON OP CODE GROUPING LINES	?	!	A	S	@	%	E	Z	C	W	V	/	.	,	⌑	U	D	J	B	R	X	G	T	M	L	K	F	N
Control	1st Scan First Op Codes	X	X	X	X	X	X	X	X	X	X	X	X		X	X				X			X	X					
	A Cy First Op Codes	X	X	X	X	X	X	X	X	X					X	X		X						X					
	Std A Cycle Op Codes	X	X	X	X	X	X	X	X	X								X						X					
	B Cy First Op Codes										X	X	X							X									
	A Reg to A Ch On B Cy Ops	X	X	X	X	X	X	X	X	X			X	X	X	X		X						X					
	Op Mod to A Ch On B Cy Ops										X	X					X		X	X	X	X					X	X	
	Load Mem On B Cy Op Codes	X	X	X	X	X	X	X	X									X											
	Rgen Mem On B Cy Op Codes									X	X	X		X					X	X	X	X		X			X	X	
	Stop at F on B Cy Op Codes	#	#			#	#						X	X				#	X		X	X							
	Stop at H on B Cy Ops										X	X								X									
	Stop at J on B Cy Op Codes	X	X			X	X	X	X									X											
	RO B AR On Scan B Cy Ops							X	X	X	X	X	X	X	X	X		X	X	X	X	X		X					
	RO A AR On A Cy Ops	X	X	X	X			X	X	X					X	X		X											

# Indicates accelerator feature timing.

Percent-Type Op Codes (13.14.10) — +S at 11D1G23G

Converts Asm Ch 8, 4 bits to 0, 4 for input to address channel
Sets ADDRESS TYPE OP CODES
Sets NO INDEX ON FIRST ADDRESS OPS
I 1, LGC sets special advance to I 3
Prevents reset of AAR and CAR

Not-Percent-Type Op Codes (13.14.10) — +S at 11D1G23E

Sets ADDRESS TYPE OP CODES
Sets READ FIRST ADDRESS TO AAR AND CAR
40 Assists in preventing NOT INTERRUPT START to I cycle control at I 6
Assists in setting START INTERRUPT to I cycle control at I 6

Address-Double-Type Op Codes (13.14.14) — +S at 11D1F23D

Assists in setting INDEX BAR to SET BAR at I 5 on index
Assists in setting FIRST ADDRESS SET BAR AND DAR and SET BAR

Not-Address-Double-Type Op Codes (13.14.14) — +S at 11D1F21G

Block reset of BAR at I 1 and I 5-A ring 2
Block reset of DAR at I 1

One-Address-Plus-Mod Op Codes (13.14.10) — +S at 11D1G23D

Block reset of DAR at I 6
OP MODE CHAR TIME at I 6 if not 1401
SET OP MOD REGISTER at I 6 LGD if no B ch WM and not 1401
CHECK OP MOD SET at I 6, LGF
LAST INSTRUCTION READ OUT CYCLE at I 7 with B ch word mark

Two-Address-No-Mod Op Codes (13.14.11) — +S at 11D1G24K

LAST INSTRUCTION READ OUT CYCLE at I 11 with B ch word mark

Two-Address-Plus-Mod Op Codes (13.14.11) — +S at 11D1G24P

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OP MOD TIME at I 11 if not 1401 mode
SET OP MOD REGISTER at I 11, LGD if no B ch WM and not 1401
CHECK OP MOD SET at I 11, LGF
LAST INSTRUCTION READ OUT CYCLE at I 12 with B ch WM

Two-Address Op Codes (13.14.12) — +S at 11D1G22C

SET I CYCLE CONTROL at I 6 or I 7 or I 8 or I 9 with no B ch WM
Sets READ SECOND ADDRESS TO BAR AND DAR

Address-Type Op Codes (13.14.12) +S at 11D1G22D

SET I CYCLE CONTROL at I 1 or I 2 or I 3 or I 4 with no B ch WM

Two-Characters-Only Op Codes (13.14.12) +S at 11D1H10A

Sets NO BRANCH OP CODES
Sets OP MOD TO A CHANNEL ON B CYCLE OPS
NOT ADDRESS DOUBLE OP CODES if not 1401
Sets REGEN MEMORY ON B CYCLE OP CODES S
Prevents setting E CHANNEL CONDITION
OP MOD CHARACTER TIME at I 1 if not 1401
SET OP MOD REGISTER at I 1, LGD if no B ch WM
E CHANNEL RESET at I 1, LGC
E CHANNEL STATUS SAMPLE A at I 2, LGD if not 1401
E CHANNEL STATUS SAMPLE A DELAY at I 2, LGE with B ch WM
E CHANNEL UNGATED SAMPLE A at I 2, LGD
LAST EXECUTE CYCLE I/O at last instr read-out cycle if not 1401
I/O INTERLOCK CHECK at I OP, error sample if not 1401
SET E 1 REGISTER at LGB or LGS if no A ch WM
RESET E 2 FULL AT F OR K OPS at LGB or LGS if no A ch WM
E CHANNEL MOVE MODE at LGE, last instr read out cycle
LAST INSTRUCTION READ OUT CYCLE at I 2 with B ch WM
CHECK OP MOD SET at I 1, LGF
FORMS STACKER GO at LGE, last instr read out cycle if E ch ready and not busy
E CHANNEL CORRECT LENGTH RECORD at E ch ungated sample A
Prevents RESET AAR and RESET CAR

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C Cycle Op Codes (13.14.12) +S at 11D1B16K

LAST INSTRUCTION READ OUT CYCLE CONDITION at I 1 or 1401 and I 3

No C or D Cycle Op Codes (13.14.12) +S at 11D1G22E

LAST INSTRUCTION READ OUT CYCLE at I 1 with B ch WM

No D Cycle at I Ring 6 Ops (13.14.13) +S at 11D1B16P

LAST INSTRUCTION READ OUT CYCLE at I 6 with B ch WM

No Index on First Address Ops (13.14.13) +S at 11D1J16Q

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INDEX NOT REQUIRED at I 1 through I 5
Prevent SET TENS POSITION INDEX TAGS at I 1 through I 5
Prevent SET HUNDREDS POSITION INDEX TAGS at I 1 through I 5
Sets NOT ADDRESS DOUBLE TYPE OP CODES

Reset Type Op Codes (13.14.01) +S at 11D1F20H

Sets ADD TYPE OP CODES
Sets ARITHMETIC TYPE OP CODES
Sets STOP AT J ON B CYCLE OP CODES
RESET ADD OR RESET SUBTRACT, LAST INSTR READ OUT CYCLE at last instruction read-out cycle

RESET ADD OR RESET SUBTRACT, UNITS OR BODY, B CYCLE, 1401 (at units or body time in B cycle if 1401 mode)
RESET ADD OR RESET SUBTRACT, EXTENSION, B CYCLE, 1401 (at extension time in B cycle if 1401 mode)

Add or Subtract Op Codes (13.14.01) +S at 11D1F20R

Sets ADD TYPE OP CODES
Sets ARITHMETIC TYPE OP CODES
ADD OR SUBTRACT, B CYCLE during B cycle
Assists in setting ADD OR SUBTRACT, B CYCLE, 1st SCAN, TRUE, B CD WM, NOT ADDER CARRY
Assists in setting ADD OR SUBTRACT, B CYCLE, 1st SCAN, TRUE, B CH WM, ADDER CARRY
Assists in setting ADD OR SUBTRACT, B CYCLE, 1st SCAN, TRUE, UNITS, 1401
Assists in setting ADD OR SUBTRACT, B CYCLE, 1st SCAN, TRUE, B CH WM, BODY OR EXTENSION, 1401
TRUE ADD B during 1st scan
COMPLEMENT ADD B during 3rd scan
GATE A CHANNEL TO ZONE ADDER during body

Multiply or Divide Op Codes (13.14.01) +S at 11D1G08H

Sets ARITHMETIC TYPE OP CODES
Sets STOP AT J ON B CYCLE OPS
Sets ADD TYPE OR MULTIPLY OR DIVIDE OR E OR Z OPS
Sets LOAD MEMORY ON B CYCLE OPS
Sets C CYCLE OP CODES
NOT ADDRESS DOUBLE OP CODES if not 1401
TRUE ADD B on 1st or 3rd scan
A CHANNEL INSERT PLUS ZERO during extension if true

A CHANNEL INSERT PLUS ZERO during MQ if complement
A CHANNEL INSERT PLUS NINE during extension if complement
A CHANNEL INSERT PLUS NINE during MQ if true
AAR READ OUT CONTROL ARITHMETIC with body control and A cycle control
CAR READ OUT CONTROL ARITHMETIC with units control and A cycle control
DAR READ OUT CONTROL ARITHMETIC with NO or 1st or 2nd or 3rd scan control and D cycle control
SET C CYCLE CONTROL at D cycle and I 1 or 1401 and I 3
Prevent LAST INSTRUCTION READ OUT CYCLE at I 6 or 1401 and I 8
Prevent 1401 I CYCLE NEXT at I 6 or 1401 and I 8
LAST INSTRUCTION READ OUT CYCLE CONDITION at I 6 or 1401 and I 8 with D cycle
SET D CYCLE CONTROL at I 6 or 1401 and I 8 with B ch WM

Add-Type Op Codes (13.14.02) +S at 11D1F20D

Sets ADDRESS DOUBLE TYPE OP CODES if not 1401
Sets READ OUT AAR ON A CYCLE OPS
Sets ADD TYPE OR MULTIPLY OR DIVIDE OR E OR Z TYPE OPS
Sets NO D CYCLE AT I RING 6 OPS
Set NOT ZERO BALANCE latch off at last logic gate of last instruction read out
Set ZERO BALANCE latch on at LGD with UNITS on
RESET ADD OR RESET SUBTRACT OR ADD OR SUBTRACT, B CYCLE, NOT B CH WM
RESET ADD OR RESET SUBTRACT OR ADD OR SUBTRACT, 1st SCAN, B CYCLE, NOT A CHANNEL WORD MARK, NOT B CHANNEL WORD MARK
RESET ADD OR RESET SUBTRACT OR ADD OR SUBTRACT, 1st SCAN, B CYCLE, A CHANNEL WORD MARK, NOT B CHANNEL WORD MARK
RESET ADD OR RESET SUBTRACT OR ADD OR SUBTRACT, 1st SCAN, B CYCLE, TRUE, EXTENSION

RESET ADD OR RESET SUBTRACT OR ADD OR SUBTRACT, 1st SCAN, B CYCLE, UNITS OR BODY
Sets LAST INSTRUCTION READ OUT CYCLE CONDITION at D cycle, I 1 or 1401 & I 3

Arithmetic-Type Op Codes (13.14.02) +S at 11D1F20C

BAR READ OUT CONTROL ARITHMETIC at B cycle, body or extension or mq control
DAR READ OUT CONTROL ARITHMETIC at B cycle, units control
SET D CYCLE CONTROL at I 1 or 1401 and I 3, with B channel WM
LAST INSTRUCTION READ OUT CYCLE prevented at I 1 or 1401 and I 3
1401 I CYCLE NEXT prevented at I 1 or 1401 and I 3
USE B CHANNEL WM at B or D cycle. NO or 1st or 2nd or 3rd scan
Sets STOP AT J ON B CYCLE OP CODES
Sets WM OR E OR Z OR W OR V OR C OR CLEAR OR . OPS

46

Compare-Type Op Codes (13.14.03) +S at 11D1G23H

NOT ADDRESS DOUBLE TYPE OP CODES if not 1401
COMPARE OP CODES, FIRST SCAN if 1st scan
USE NO WORD MARK, if B cycle
USE NO ZONES if B cycle
USE NO NUMERIC if B cycle

Branch-Type Op Codes
(This is an op code grouping but not an actual op code grouping line. The two ALD lines listed below are controlled by branch type op codes.)

J or R or X or B Op Codes (13.14.07) -S at 11D1E25R

Sets REGEN MEMORY ON B CYCLE OP CODES
Sets READ OUT BAR ON SCAN B CYCLE OPS
Sets NOT PERCENT TYPE OP CODES

W or V or Clear Op Codes (13.14.03) +S at 11D1D24D

Sets FIRST SCAN FIRST OP CODES
Sets B CYCLE FIRST OP CODES
Sets WM OR E OR Z OR W OR V OR C OR CLEAR OR . OPS
Sets NOT PERCENT TYPE OP CODES
Sets TWO ADDRESS OP CODES

47

No-Branch Op Codes (13.14.04) +S at 11D1B22C

NO BRANCH CONDITIONS if last instruction read-out cycle

Word Mark Op Codes (13.14.05) +S at 11D1G21H

Sets NO BRANCH OP CODES
Sets COMMON OP CODE GROUPING
Sets WM OR E OR Z OR W OR V OR C OR CLEAR OR . OPS
Sets READ OUT AAR ON A CYCLE OPS

ADDRESS DOUBLE OP CODES if not 1401
SET B CYCLE CONTROL if A cycle
WORK MARK OP, A CYCLE if A cycle
LOAD MEMORY if A or B cycle
LAST EXECUTE CYCLE if B cycle
WORD MARK OPS, B CYCLE if B cycle
USE B CHANNEL NUMERIC if A or B cycle
USE B CHANNEL ZONES if A or B cycle

M or L Op Codes (13.14.05) +S at 11D1H10H

48
Sets PERCENT TYPE OP CODES
E CHANNEL IN MODE at I 11, LGF, % or @, $ or R op mod
COMPUTE DISABLE CYCLE at I 10, I/O % or , E or F channel in process
READ TAPE CALL E CHANNEL if E ch tape call, $ or R op mod
WRITE TAPE CALL E CHANNEL if E ch tape call, W or X op mod
Set F CHANNEL READ LATCH on if I 11, LFG, ¤ or *, $ or R op mod
SET E 1 REGISTER if E ch select unit 1 or 4, % or @, I 5, LGB or LGS
ADDRESS CHECK prevented if B or E or F cycles
Assists in setting 1401 MOVE OR LOAD TAPE DELAY
READ TAPE CALL F CHANNEL if F ch tape call, $ or R op mod
WRITE TAPE CALL F CHANNEL if F ch tape call, W or X op mod
FILE OP if E ch select unit F, % or @
FILE OP if F ch select unit F, ¤ or *
RESET E 2 FULL at I 6, LGB or LGS, E ch unit 1, % or @
E CHANNEL UNGATED SAMPLE A at I 12, LGD, % or @, not E ch sel unit F

E CHANNEL STATUS SAMPLE A DELAY at I 12, LGE, % or @, B channel WM, not E ch sel unit F
E CHANNEL STATUS SAMPLE A at I 12, LGD, % or @, not 1401, not E ch sel unit F
SET GROUP MARK at any last input cycle, 1401
RESET EAR at I 6, LGF, not I/O %, not I/O¤, not I/O*
RESET FAR at I 6, LGF, not I/O %, not I/O¤, not I/O@

First-Scan-First Op Codes (13.14.06) +S at 11D1E22G

SET FIRST SCAN CONTROL at last instruction read-out cycle

Standard A Cycle Ops • A Cycle (13.14.06) -S at 11D1G19G

49
Sets B CYCLE CONTROL
Sets STOP AT F
Sets REGEN SECOND SCAN CONTROL
Sets REGEN THIRD SCAN CONTROL
Sets USE A CHANNEL WORK MARK
Sets REGEN EXTENTION CONTROL
Sets REGEN UNITS AND BODY CONTROL
Sets REGEN FIRST SCAN CONTROL
REGEN MEMORY if no check test
Sets USE A CHANNEL ZONES
Sets USE A CHANNEL NUMERIC
Sets USE A CHANNEL WM

B Cycle First Op Codes (13.14.07) — +S at 11D1D22H

SET B CYCLE CONTROL on last instruction read-out cycle

A Register to A Channel on B Cycle Ops (13.14.07) — +S at 11D1E26D

GATE A DATA REGISTER TO A CHANNEL if B cycle

Op Modifier to A Channel on B Cycle Ops (13.14.07) — +S at 11D1C25C

GATE OP MODIFIER TO A CHANNEL if B cycle

50

Load Memory on B Cycle Ops (13.14.08) — +S at 11D1E26E

LOAD MEMORY if B cycle

Regenerate Memory on B Cycle Ops (13.14.08) — +S at 11D1F24C

REGEN MEMORY if B cycle and not any check test

Stop at F on B Cycle Op Codes (13.14.08) — +S at 11D1K23C

STOP AT F if B cycle

Stop at J on B Cycle Op Codes (13.14.09) — +S at 11D1E24E

STOP AT J if B cycle

Read-Out BAR on Scan B Cycle Ops (13.14.09) — +S at 11D1E24C

READ OUT BAR if LG spec A, B cycle control, 1st or 2nd or 3rd scan, and not console inhibit address register read-out

Read-Out AAR on A Cycle Ops (13.14.09) — +S at 11D1B22D

READ OUT AAR if LG spec A, A cycle control, not cons inhibit addr reg read-out

51

Stop at H on B Cycles (13.14.08) — +S at 11D1B25K

STOP AT H ON B CYCLE AND FIRST SCAN if B cycle and 1st scan

A Cycle First Ops (13.14.06) — +S at 11D1D20E

SET A cycle control at last instruction RO

Special Features

The 1410 is not compatible with a 1401 program that makes use of the following special features:

1. Column Binary Feature
2. Compressed Tape Feature
3. Punch Feed Read Feature
4. The Serial I/O Adapter, including provisions for attaching the following units:
   a. IBM 1009 Data Transmission Unit
   b. IBM 1011 Paper Tape Reader
   c. IBM 1012 Paper Tape Punch
   d. IBM 1412 Magnetic Character Reader
   e. IBM 1419 Magnetic Character Reader

Read and Write Tape Operations (with word marks)

When writing tape in the load mode, if a word separator character is encountered in core storage, the 1401 will write one word separator on tape while the 1410 will write two word separator characters on tape.

When reading tape in the load mode on the 1401, any number (one or more) of word separator characters read in succession from tape are eliminated and a word mark is placed over the first non-word separator character that follows the word separator characters.

When reading tape in the load mode on the 1410, a pair of adjacent word separator characters on tape are read into core storage as one word separator character and no word mark is placed over the next non-word separator character.

When reading in 1401 Mode, if an IRG is encountered before a GMWM is encountered, a GMWM is inserted at that point.

Carriage Controls

A 1401 system will not execute an immediate skip to channel X when the carriage is already at that channel, but a 1410 operating in the 1401 mode will execute the instruction.

B-Address Register

At the completion of a card or print operation, the setting of the B-address register will be different on the 1401 and a 1410 operating in the 1401 mode. The following chart shows a comparison of the B-address register contents at the completion of the specific operation.

Operation	B-Add Reg 1401	B-Add Reg 1410 (1401 Mode)
1	081	082
2	*333	335
3	081	082
4	181	183
5	181	183
6	181	183
7	181	183

* = 335 for an unbuffered printer

Stacker Selection

In the 1401 system, approximately 10 ms of compute time is available at the completion of a card read for initiating a stacker select operation. For a 1410 system operating in the 1401 mode, the amount of available time to do the same thing may vary from 8 to 82 ms. No incompatibilities arise unless:

1. The program between the read and stacker instructions takes longer than 8 ms on the 1410 system and the stacker instruction is too late to be effective. This results in a stacker instruction that is effective on a 1401 but not on a 1410.
2. A stacker instruction in a 1401 program is too late to be effective on a 1401 but early enough to be effective on a 1410 (because of faster internal processing speed or longer available time). This condition results in a stacker instruction that is not effective on a 1401 but is effective on a 1410 system.
3. When reading cards with I/O check stop switch off into N/R pocket and just selecting invalid cards, stacker select will not function after a reader error. Result is invalid cards in N/R pocket with good cards.

Due to faster internal processing speed, the likelihood of (1) possibility is low. The (2) situation may arise if the programs are tested and debugged on the 1410 in 1401 mode. The stacker select may work in this case but on later runs on a 1401, failures to select will occur.

Input Characters (Incorrect Parity)

The 1401 system corrects any input character of incorrect parity by adding or removing the C-bit, forcing the character valid. The 1410 system inserts an asterisk (*) in core storage in place of all invalid (incorrect parity) input characters.

1402 Card Read-Punch Character Set

The 1410 system punches an A-bit in core storage as an 8-2 combination in a card column and reads an 8-2 combination in a card column as an A bit

The 1401 system punches an A-bit in core storage as a zero in a card column and regards an 8-2 combination in a card column as an invalid character.

A no-charge RPQ (#898148) is available on the 1401 system which makes the 1401 operate as described above for the 1410.

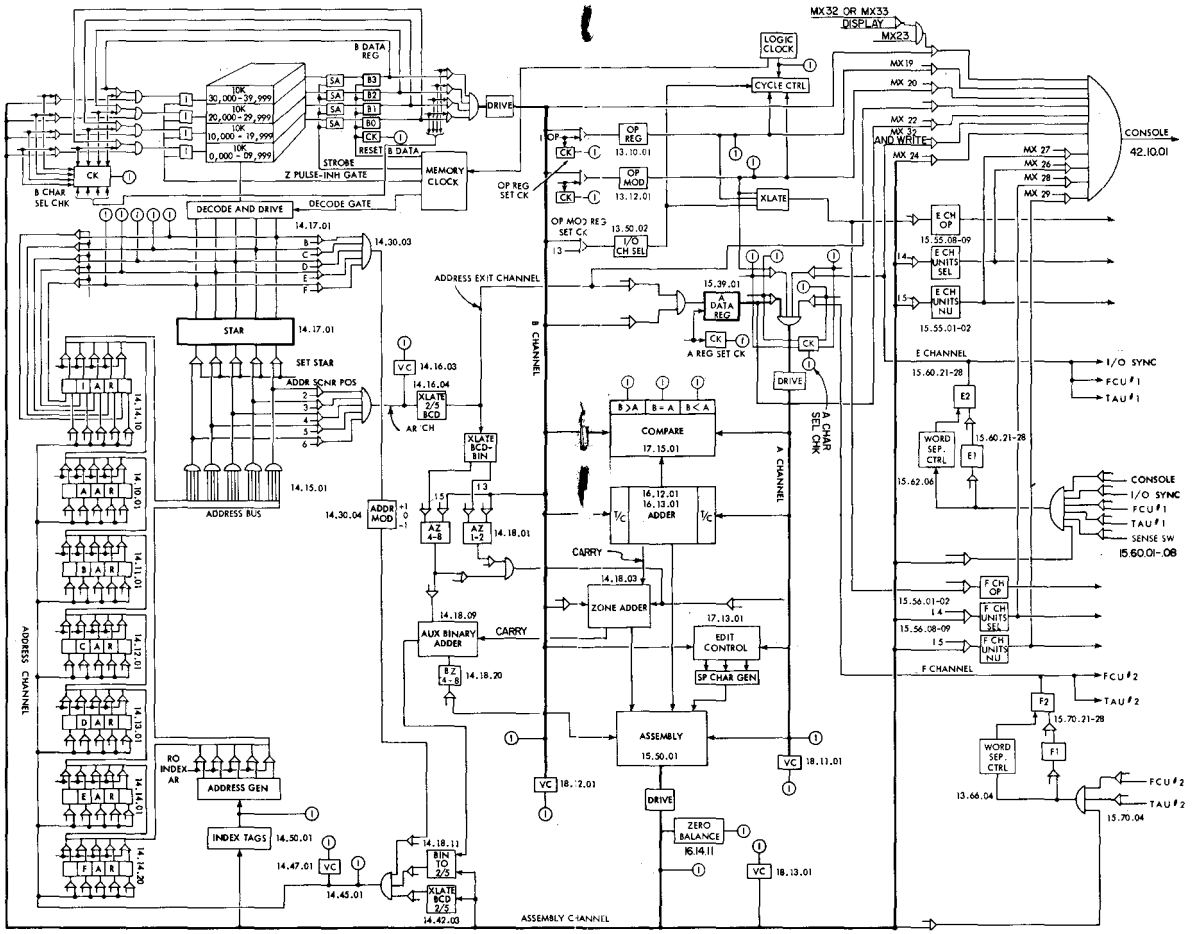
Single Character Edit

If the specified A-field in an edit operation contains a word mark in the units position (a single character field), the 1401 system will not transfer this single-character field to the B-field.

The 1410 will transfer and edit this single-character field.

Divide Blanks

On a 1401 system divide operation if the B-field contained blanks to start with and if the divide operation quotient result is zero, these blanks remain in the quotient result. A 1410 system operating in the 1401 mode converts all blanks of this type to zeros.



IBM 1410 Data Processing System Data Flow

Card Position When System Stops

Because the 1410 makes use of an intermediate storage area on data transfers between core storage and the reader or punch, the 1401 read release and punch release instructions do not cause actual card-feed motion on the 1410 system operating in the 1401 mode.

Following a system stop operation the position of the cards in the hoppers and stackers of an IBM 1402 Card Read-Punch may not be the same in a 1410 system as they are in a 1401 system.

Process Overlap

A 1401 program utilizing the Process Overlap feature will run on the 1410 in the 1401 mode only by installation of EC 250780.

Card Read/Punch Operations

The 1401 puts a "set-up" character in core storage position 100 and any read instruction leaves an ampersand in core storage position 000. A 1410 system operating in the 1401 mode does not do this.

MLP Cards

MLP cards containing 8 & 9 punches in MLP control column will read on a 1401 system 1402 but will cause a validity check on a 1410 system 1402.

1410 - 1401 ADDRESS CONVERSION

The chart on the following page will facilitate conversion between 1410 and 1401 addresses.

To convert from a 1410 address to a 1401 address, find the high-order two or three significant digits (two digits for addresses up to 09999, 3 digits for addresses of 10,000 or over) on the top section of the chart. Substitute the accompanying character.

Convert the units position in the same manner, using the same column on the lower portion of the chart.

The digit portion of the tens position will be the same as the 1410 address. The zone portion of the tens position, if present, will indicate index register reference.

To convert from 3-character 1401 addresses to a 1410 address, start with the units position and the lower position of the sheet and work the same method in reverse.

Examples

1410 Address to 1401 Address:

1410 Address 14785 = P8E

	147	8	5
Work left to right	Found in 4th col at top of chart	Remains the same	Found in 4th col at bottom of chart
	P	8	E

1401 Address to 1410 Address:

1401 Address M3K = 10432

	M	3	K
Work right to left	Found in 3rd col at top of chart	Remains the same	Found in 3rd col at bottom of chart
	104	3	2

FOR HIGH ORDER OF 1401 ADDRESS

High Order 1410	High Order 1401	High Order 1410	High Order 1401	High Order 1410	High Order 1401	High Order 1410	High Order 1401
1-1		40-0		80-0		120-0	
2-2		41-1		81-1		121-1	
3-3		42-2		82-2		122-2	
4-4		43-3		83-3		123-3	
5-5		44-4		84-4		124-4	
6-6		45-5		85-5		125-5	
7-7		46-6		86-6		126-6	
8-8		47-7		87-7		127-7	
9-9		48-8		88-8		128-8	
10-‡		49-9		89-9		129-9	
11-/		50-‡		90-‡		130-‡	
12-S		51-/		91-/		131-/	
13-T		52-S		92-S		132-S	
14-U		53-T		93-T		133-T	
15-V		54-U		94-U		134-U	
16-W		55-V		95-V		135-V	
17-X		56-W		96-W		136-W	
18-Y		57-X		97-X		137-X	
19-Z		58-Y		98-Y		138-Y	
20-0̄		59-Z		99-Z		139-Z	
21-J		60-0̄		100-0̄		140-0̄	
22-K		61-J		101-J		141-J	
23-L		62-K		102-K		142-K	
24-M		63-L		103-L		143-L	
25-N		64-M		104-M		144-M	
26-O		65-N		105-N		145-N	
27-P		66-O		106-O		146-O	
28-Q		67-P		107-P		147-P	
29-R		68-Q		108-Q		148-Q	
30-0̄		69-R		109-R		149-R	
31-A		70-0̄		110-0̄		150-0̄	
32-B		71-A		111-A		151-A	
33-C		72-B		112-B		152-B	
34-D		73-C		113-C		153-C	
35-E		74-D		114-D		154-D	
36-F		75-E		115-E		155-E	
37-G		76-F		116-F		156-F	
38-H		77-G		117-G		157-G	
39-I		78-H		118-H		158-H	
		79-I		119-I		159-I	

FOR UNITS POSITION OF 1401 ADDRESS

0-0	0-‡	0-!	0-?
1-1	1-/	1-J	1-A
2-2	2-S	2-K	2-B
3-3	3-T	3-L	3-C
4-4	4-U	4-M	4-D
5-5	5-V	5-N	5-E
6-6	6-W	6-O	6-F
7-7	7-X	7-P	7-G
8-8	8-Y	8-Q	8-H
9-9	9-Z	9-R	9-I

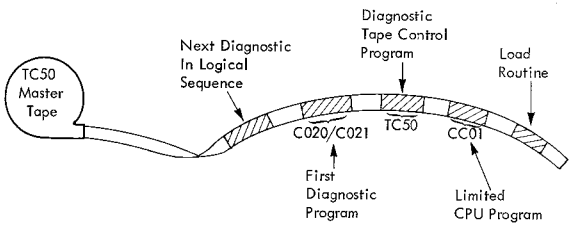
TENS POSITION OF 1401 ADDRESS

Tens Position 1410	Tens Position 1401	Index Register 1	Index Register 2	Index Register 3
0-0		0-‡	0-!	0-?
1-1		1-/	1-J	1-A
2-2		2-S	2-K	2-B
3-3		3-T	3-L	3-C
4-4		4-U	4-M	4-D
5-5		5-V	5-N	5-E
6-6		6-W	6-O	6-F
7-7		7-X	7-P	7-G
8-8		8-Y	8-Q	8-H
9-9		9-Z	9-R	9-I

1410 DIAGNOSTIC PROGRAM INDEX

Identification	Title		Application With	Vol No.
CC01A	Limited CPU Instruction test		Tape Systems Only	1.00
TC50A	Diagnostic Tape Control Program		Tape Systems Only	1.00
C020B	CPU Error Detection		10 or 20K Only	2.02
C020B	Phase 2		10 or 20K Only	2.02
C020B	Phase 3		10 or 20K Only	2.02
C020B	Phase 4		10 or 20K Only	2.02
C021B	CPU Error Detection		40K Minimum	2.01
C022B	Alarm Program		All	2.00
CU01B	CPU Reliability		40K Minimum	2.01
CU06B	Super Scramble		All	2.00
CS30A	Memory Discrimination	HI	10K Only	2.02
CS31A	Memory Address Placement	HI	10K Only	2.02
CS32A	Worst Case 2D Plane Pattern	HI	10K Only	2.02
CS33A	Worst Case In Line Plane Pattern	HI	10K Only	2.02
CS34A	Worst Case Alt Plane Pattern	HI	10K Only	2.02
CS35A	Memory Discrimination	LO	10K Only	2.02
CS36A	Memory Address Placement	LO	10K Only	2.02
CS37A	Worst Case 2D Plane Pattern	LO	10K Only	2.02
CS38A	Worst Case In Line Plane Pattern	LO	10K Only	2.02
CS39A	Worst Case Alt Plane Pattern	LO	10K Only	2.02
CS41B	Memory Reliability Test	HI	20K Only	2.02
CS42B	Memory Reliability Test	LO	20K Only	2.02
CS43B	Memory Reliability Test	HI	40, 60, 80, 100K Only	2.01
CS44B	Memory Reliability Test	LO	40K Only	2.01
CS46B	Memory Reliability Test	LO	60,80,100K Only	2.01
ST02B	System Test		40K, O'Lap,Priority	3.01
ST03A	System Test		10, 20K Only	3.00
ST01B	System Test		20K Minimum	3.00
T020A	Tape Operations Test		729/7330 Tape Units	4.00
T021A	Multi-Chan Interchange Test		729/7330 Tape Units	4.00
T021B	Phase 2		729/7330 Tape Units	4.00
T022B	Tape Record Gap Test		729/7330 Tape Units	4.00
T022B	Phase 2		729/7330 Tape Units	4.00
MP01A	Priority Test		Priority Feature	3.00
M003D	Program Addressable Clock Test		Prog Addr Clock	8.01
M005C	1410 Teletype Test		A.T.&T. or W.U. TTY	7.01
M009C	1009 Data Transmission Unit Test		1009 DTU, 7701/7702	7.01
M010C	1014 Remote Inquiry		1014 Remote Inquiry	7.01
M011A	1410/1401 CPU Compatibility		1401 Compat Feat	2.00
M012A	1410/1401 I/O Compatibility		1401 Compat Feat	2.00
M013A	1410/1401 1405 Compatibility		1405 Disk File	6.15
M014A	1410/1401 Topsy Compatibility		1401 Compat Feat	2.00
DA03C	1301 Reliability Test		1301 Disk File	6.02
DA05C	1301 Mechanical Hydraulic Test		1301 Disk File	6.02
DA04D	7631 Electronic Operation Test		1301 Disk File	6.02
DA01C	1301 Write Addr & Surface Analysis		1301 Disk File	6.02
DR02A	1405 Reliability Test		1405 Disk File	6.15
DR04A	1405 Arm Speed Test		1405 Disk File	6.15
DR03A	1405 Arm Alignment Test		1405 Disk File	6.15
DR01A	1405 Home Addr & Surface Analysis		1405 Disk File	6.15
HL01B	LS Hypertape Reliability		7341 Hypertape	8.04
HL03A	Hypertape Topsy		7341 Hypertape	8.04
HL04A	LS Hyper Interchange		7341 Hypertape	8.04
HL05A	LS Hyper Gap Test		7341 Hypertape	8.04
RP01A	1402 Card Reader-Punch Test		1402-2 Reader-Punch	5.00
RP51A	1402 Card Reader 51 Column Cards		51 Column Feature	8.01
RC01C	Reader-Punch Column Binary Test		Column Binary Feature	7.01
RS01D	Serial Card Reader Test		1442 Model 3	8.01
RT01A	1011 Paper Tape Reader Test		1011 Paper Tape Reader	7.01
RB01A	1412 Read Compare Test		1412 MICR	8.02
RB03A	1412 Stacker Select Test		1412 MICR	8.02
RB04A	1412 Engage-Disengage Test		1412 MICR	8.02
RB05A	1412 Document Spacing Test		1412 MICR	8.02
RB06A	1412 Error Indicators Test		1412 MICR	8.02
RB10A	Stacker Sel & Field Verification		1419 MICR	8.02
W001E	1403 Printer Test		1403 Printer	5.00
W002E	1403 Forms Control Test		1403 Printer	5.00
WT01B	1415 Console I/O Printer Test			5.00
SF01A	1301 Shared File Program		1301 Shared File	6.02
UP51A	Utility Punch Program		Tape Systems Only	1.00
PC01C	7750 Program Transmission Ctrl Test		7750 PTC	8.03
PC02A	Force Load 7750 PFLD Programs		7750 PTC	8.03
Z001B	I/O Status Condition Test		Run From Cards Only	3.00

SEQUENCE OF DIAGNOSTIC PROGRAMS ON TC50 MASTER TAPE



LOAD ROUTINE

The load routine is described in detail in the TC50 manual, CE Diagnostic Engineering Publication, 1410/7010, Volume 1.00 (12/1/63), Page 35, Appendix I.

1410/7010 MEMORY ALLOCATION CHART

Top 09999 or 39999	
1517 - Top	
1460 - 1516	Channel 4 Control Card *
1403 - 1459	Channel 3 Control Card *
1346 - 1402	Channel 2 Control Card *
1289 - 1345	Channel 1 Control Card *
1256 - 1288	System Control Card *
1255	ǂ
1250 - 1254	Test Ident. and Suffix
1245 - 1249	Control Constants for TC50
1215 - 1244	Control Constants for TC50 *
1004 - ?	Special Tads Followed by ǂ *
1000 - 1003	Standard Tads
334 - 999	Reserved for Use by Load Programs (Must not be disturbed)
302 - 333	
301	Timer Interrupt Branch Loc.
300	
280 - 299	(7010) Floating Point Acc. *
200 - 279	(7010) Floating Point Arithmetic Word Area *
102 - 199	
101	Priority Interrupt Loc. *
100	
25 - 99	Index Registers *
9 - 24	
8	(7010) Relocate & Protect Br. Loc.
2 - 7	
1	
0	

1. * If a Program does not test or use this feature, it may be used as needed by the program

2. Diagnostic Read In at location 1000 and Start operating at location 2000 (with the exception of some memory programs). Any address between 1000-09999 (39999 for 7010) may be included in the program

RUNNING PROCEDURE

A. Make a TC50 diagnostic tape ready on tape drive 0 of any channel.
   1. Display memory location 00000
   2. Alter to:
      RL%B000011$. For E channel tape
      XL□B000011$. For F channel tape
   3. Depress Tape Load Button

B. Set to RUN, COMPUTER RESET, START

The above procedures will load a very short load routine. This load routine will load CC01. Upon successful completion, CC01 will load and initiate the search section of TC50. Appendix I of TC50 contains a description and listing of the short load routine that is the first record of the TC50 diagnostic tape.

C. Upon initial loading, TC50 Search will type: "OPTION?" -- Upon Completion of that selection, "OPTION" will be typed again.
At this time use the inquiry button to enter one of the following:

1. *Program identity, ie., "CU01." Designated program will run in its entirety.

or 2. *Left portion of a program identity.
All programs adjacent on the tape, having the designated portion of the identity will be run in their entirety, i.e., if "C" were entered, all programs with a "C" identity would be run; if "CU" were entered, all programs with a "CU" identity would be run; if "CU0" were entered, all programs with a "CU0" identity would be run; etc.

or 3. Nothing (Just request / release)
All programs on the tape will be run in sequence starting at the point the tape is located when this entry is made.

or 4. $
Entering a dollar sign will select the reliability mode described in Section 1.01.00.S0 of the TC50 write-up.

* Note: Normally, when a program identity or a portion of a program identity is entered, the diagnostic tape is rewound before the search of the tape is started. If a word mark is entered along with the first character of the identity, the rewind will be inhibited.

Operating Hints and Comments

The operation of the search section of TC50 requires very little knowledge of the program. Knowing the various available options should be sufficient. A selected program must be re-selected to be rerun.

TAD'S

Standard TAD'S

A. Most diagnostic programs will use all four standard TAD's.

1. TAD's are an integral part of almost all diagnostic programs, and are automatically read in with each program. They are located in memory positions 01000 through 01003. They are preset in the OFF (Not 1) condition. To set a TAD to the ON condition (character 1), the Program Alter Routine will normally be used. (See "Internal TAD Routine.")

2. Functions

TAD	Mem Addr	OFF 1	ON 1
TAD 0	01000	Typeout	Bypass Typeouts
TAD 1	01001	Do not repeat routine	Repeat the routine
TAD 2	01002	Bypass error halts	Halt on error
TAD 3	01003	One program pass	Repeat the prograr

Special TAD's

Most diagnostic programs will use some special TAD's. Special TAD's are used by individual programs as required. They also will automatically be read in with each program. They will be located in memory starting at position 01004.

Some programs may have several special TAD's. Consult individual program write-ups for details.

Internal TAD Routine

All diagnostics contain a J(I)Q instruction. To use:

1. Depress Inq key. Program will stop and an I will be typed.
2. Enter 5 digit address of location to be altered. Depress Inq Rel key.
3. Depress Inq key. An I will be typed.
4. Enter the desired information. (Memory will be altered starting at the address entered in item (2).)
5. Depress Inq Rel key. Program will continue to run.

Note: Inq Cancel may be used if a mistake is made in either item (2) or (4).

PROGRAM MAINTENANCE OF DIAGNOSTICS

Refer to the TC50 Manual for the following:

1. Tape search operation
2. Straight duplication
3. Normal update/edit operation
4. System and channel control card information located in Appendix I, Volume 1.

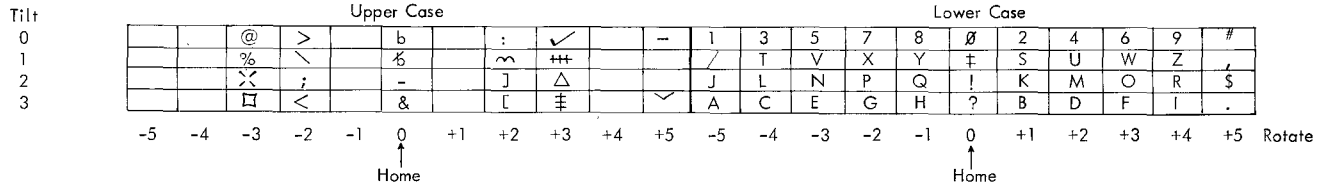
1415 TYPE-OUT FORMAT

	Print-Out Ident	IAR	AAR	BAR	Op Code	Op Modifier	A Data Reg	B Channel	Assembly Channel	Channel 1 Unit Sel Reg	Channel 1 Unit Num Reg	Channel 2 Unit Sel Reg	Channel 2 Unit Num Reg
NORMAL STOP (Double Space)	S	XXXXX	XXXXX	XXXXX	X	X	X	X	X	X	X	X	X
HALF-CYCLE (Double Space)	C	XXXXX	XXXXX	XXXXX	X	X	X	X	X	X	X	X	X
ERROR STOP (Double Space)	E	XXXXX	XXXXX	XXXXX	X	X	X	X	X	X	X	X	X
ADDRESS SET (Single Space)	B	XXXXX											
ADDRESS SET (Single Space)*	#	XXXXX											
STORAGE SCAN SET (Single Space)	#	XXXXX											
DISPLAY (Single Space)	D	XXXXX											
	D	XXXXXXXX											
ALTER (Single Space)	A	XXXXXXXX											
CONSOLE INQUIRY (Single Space)	I	XXXXXXXX											
CONSOLE REPLY (Single Space)	R	XXXXXXXX											

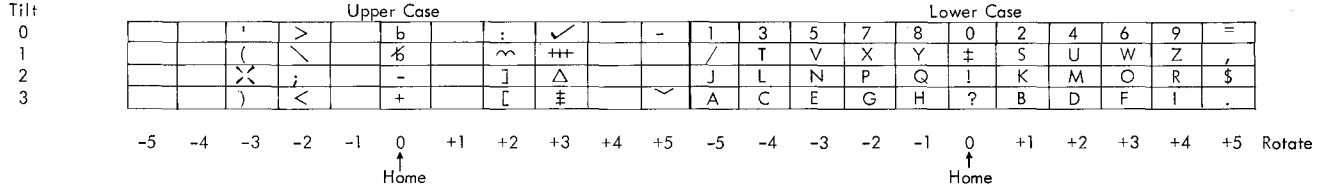
*With address entry switch off normal.

Standard BCD Elements

Type Arrangement A -- Report Writing



Type Arrangment H -- Program Language



PRINTER MAGNET - CONTACT CHART

Character	BCD Code	Case	Rotate	Tilt	Magnets Rotate	Magnets Tilt	Energized Ck	Contacts Rotate	Contacts Transferred	Transferred Ck
b output b input	C BA8 21 BA84 1	U L U	0 +3 -3	0 3 3	1 2 2A	1 2	C	1 2 2A 5 1 2 2A	C C	C C
< H	C BA8 21 BA84 1	L U L	-2 +2 -3	3 3 3	1 2A 5 1 2A 5 2A 5	1 1 1	C C C	2 1 2 1 2	1 2 1 2 1 2	C C C
# & output & input	C CBA CBA8421	U U U	0 +3 0	3 3 3	2A 1 2 2A	1 2	C	1 2 2A 5 1 2 2A	1 2 1 2	C C
$ *]	BA8 21 CB 8 21 CB 84 1	L U L	+5 -3 +3	2 2 2	1 2A 5 2A 1 2A 5	1 1 1	C C C	1 2 2A 5 2 1 2	1 2 1 2 1 2	C C C
! Δ output - input	CB 842 B 8421	U U	-2 +3	2 2	2A 1 2 2A	1 2	C	1 2 2A 5 1 2 2A	1 2 1 2	C C
/ - output - input	C A 1 C A8 21 CA84 1	L U L	-5 +5 +3	1 1 1	2A 5 1 2A 5 2A 5	1 1 1	C C C	1 2 2A 5 2 1 2	1 2 1 2 1 2	C C C
% ?	C A8421 A84 1	U L	+2 +3	1 1	2A 1 2A	1 2	C	1 2 2A 5 1 2 2A	1 2 1 2	C C
\ + output & input	C A 8 21	U L U	+5 -3 +2	0 0 0	1 2A 5 1 2A 2A 5	1 2 1 2	C C	1 2 2A 5 1 2 2A	C C	C C
@ : >	C 84 1 842	U U U	+5 -3 +2	1 0 0	1 2A 5 1 2A 2A 5	1 2 1 2	C C	1 2 2A 5 1 2 2A	C C	C C
✓ ? A	C CBA8 2 1 BA 2 1	U L L	+3 0 -5	0 3 3	2A 1 2 2A 5 2 2A	1 2	C C C	1 2 2A 5 1 2 2A 5 2 2A 5	C C C	C C C
B	CBA 21	L	+1	3	2 2A 5	1	C	1 2 2A 5	C	C
C D E	CBA 21 CBA 4 1 CBA 42	L L L	-4 +2 +3	3 3 3	2 2A 5 2A 5 2A 5	1 1 1	C C C	2 2A 5 2 2A 5 2 2A 5	1 2 1 2 1 2	C C C
F G	BA 421 BA8 1	L L	-2 +4	3 3	2A 5 2A 5	1 1	C C	2 2A 5 2 2A 5	1 2 1 2	C C
H I	CBA 2 1 CB 2 1	L L	-1 -5	2 2	1 5	1 2	C C	1 2 2A 5 1 2 2A 5	1 2 1 2	C C
J K L	CB 2 21 CB 4 1 CB 4 21	L L L	+1 -4 +2	2 2 2	2A 5 2A 5 2A 5	1 1 1	C C C	1 2 2A 5 1 2 2A 5 1 2 2A 5	1 2 1 2 1 2	C C C
M N	CB 42 1 B 42 1	L L	-3 +3	2 2	2A 5 2A 5	1 1	C C	1 2 2A 5 1 2 2A 5	1 2 1 2	C C
O P Q	CB 421 CB 8 1 B 8 1	L L L	-2 -1 +4	2 2 1	2A 2A 5 2A 5	1 2 1 2	C C	1 2 2A 5 1 2 2A 5	1 2 1 2	C C
R	B 8 1	L	+4	1	2A 5	1 2	C	1 2 2A 5	1 2	C
S T U	C A 2 21 C A 4 21 C A 4 1	L L L	+1 -4 +2	1 1 1	2 2A 5 2 2A 5 2 2A 5	1 2 1 2 1 2	C C C	1 2 2A 5 1 2 2A 5 1 2 2A 5	1 2 1 2 1 2	C C C
V W X	C A 42 1 C A 42 21 C A8 42 1	L L L	-3 +3 -2	2 2 2	2A 5 2A 5 2A 5	1 2 1 2 1 2	C C C	1 2 2A 5 1 2 2A 5 1 2 2A 5	1 2 1 2 1 2	C C C
Y Z	C A8 42 21 C A8 1	L L	+2 +4	2 1	2A 5 2A 5	1 2 1 2	C C	1 2 2A 5 1 2 2A 5	1 2 1 2	C C
Ø 1 2	C C A8 2 1 C A 2 21	L L L	0 +1 -4	0 1 1	2A 2 2A 5 2 2A 5	1 2 1 2 1 2	C C C	1 2 2A 5 1 2 2A 5 1 2 2A 5	1 2 1 2 1 2	C C C
3 4 5	C 21 C 4 1 C 4 21	L L L	+1 +4 +3	0 0 0	2A 5 2A 5 2A 5	1 2 1 2 1 2	C C C	1 2 2A 5 1 2 2A 5 1 2 2A 5	1 2 1 2 1 2	C C C
6 7 8	C 42 1 C 42 21 C 8 1	L L L	-2 +2 +1	0 0 1	2A 5 2A 5 2A 5	1 2 1 2 1 2	C C C	1 2 2A 5 1 2 2A 5 1 2 2A 5	1 2 1 2 1 2	C C C
9 =	C 8 21 C 84 1 C A 1	L U L	-1 +5 +5	1 0 0	2A 5 1 2A 5 2A 5	1 2 1 2	C C	1 2 2A 5 1 2 2A	C C	C C

CONSOLE MATRIX CONTROL

Matrix Location	Coordinates		Function
1	X1	Y1	T Th pos IAR
2	X1	Y2	Th pos IAR
3	X1	Y3	H pos IAR
4	X1	Y4	T pos IAR
5	X1	Y5	U pos IAR
6	X1	Y6	Space
7	X2	Y1	T Th pos AAR
8	X2	Y2	Th pos AAR
9	X2	Y3	H pos AAR
10	X2	Y4	T pos AAR
11	X2	Y5	U pos AAR
12	X2	Y6	Space
13	X3	Y1	T Th pos BAR
14	X3	Y2	Th pos BAR
15	X3	Y3	H pos BAR
16	X3	Y4	T pos BAR
17	X3	Y5	U pos BAR
18	X3	Y6	Space
19	X4	Y1	Op register
20	X4	Y2	Op modifier register
21	X4	Y3	Space
22	X4	Y4	A data register
23	X4	Y5	B data channel
24	X4	Y6	Assembly
25	X5	Y1	Space
26	X5	Y2	Unit select channel 1
27	X5	Y3	Unit number channel 1
28	X5	Y4	Unit select channel 2
29	X5	Y5	Unit number channel 2
30	X5	Y6	Special character (D-A-I-R)
31	X6	Y1	Space
32	X6	Y2	I/O cycles -- no word mark control*
33	X6	Y3	I/O cycles -- word mark control (disp or alter)
34	X6	Y4	Carriage return
35	X6	Y5	Special character (S-C-E-B-#-D)
36	X6	Y6	Space
Home	X6	—	—

*Read or write ops and first char of display or alter.

Coordinates		Function (Address Set)
X1A	Y1	Type T Th pos
X1A	Y2	Type Th pos
X1A	Y3	Type H pos
X1A	Y4	Type T pos
X1A	Y5	Type U pos
X1A	Y6	Carriage return (MX 6A)

C E PANEL LIGHTS

CYC A, B	12.12.01.1-.02.1
C, D	12.12.06.1-.07.1
E, F	12.12.66.1-.67.1
I, X	12.12.04.1-.05.1
A CH SEL A,d	15.38.02.1
E	15.38.03.1
F	15.38.05.1
B WM to 1	15.30.01.1-.08.1
A WM to 1	15.39.01.1-.08.1
ASSM WM to 1	15.50.01.1-.08.1
OP C to 1	13.10.01.1-03.1
MOD C to 1	13.12.01.1-.03.1
ADDR 8 to 1	14.45.01.1-.05.1
MATRIX H	45.30.01.1
X1A	45.20.05.1
32,33	45.20.09.1
INDEX	14.50.01.1-.02.1
STOR ADDR REG	14.17.01.1-15.1
1414 MOD 3 & 4	51.45.01.1-.06.1

1415 INDICATOR LIGHTS

CPU	I ring op-12		11.20.01.1-.07.1
	A ring 1-6		14.70.01.1-.06.1
	Clock A-K		11.10.11.1-.19.1
	Scan N,1,2,3		12.30.01.1-.02.1
	Sub scan U		16.30.02.1
	B		16.30.04.1
	E		16.30.06.1
	MQ		16.30.07.1
	Cycle A, B		12.12.01.1-.02.1
	C, D		12.12.06.1-.07.1
	E, F		12.12.66.1-.67.1
	I, X		12.12.04.1-.05.1
	Carry in		16.20.21.1
	Carry out		16.14.06.1
	A compl		16.20.15.1
	B compl		16.20.10.1
Status B to A			17.14.01.1-.03.1
	Overflow		16.45.02.1
	Divide overflow		16.45.01.1
	Zero balance		16.14.12.1
Channel control		CH 1	CH 2
	Interlock	15.62.01.1	15.63.02.1
	RBC interlock	13.72.01.1	13.73.03.1
	Read, write	15.62.01.1	15.63.01.1
	Ovlp, unovlp	13.60.04.1	13.64.08.1
Channel status			
	Not ready	12.62.01.1	13.65.05.1
	Busy	12.62.02.1	13.65.05.1
	Data check, cond	12.62.04.1	13.66.01.1
	Wrong length record	13.63.03.1	13.66.06.1
	No transfer	13.72.04.1	13.73.04.1

System check	
A channel	18.11.03.1
B channel	18.12.03.1
Assm channel	18.13.03.1
Add channel	18.14.03.1
Add exit	18.14.02.1
A, B, Op, mod set	18.14.04.1-.07.1
A char select	18.14.01.1
B char select	15.30.10.1
I/O interlock	18.14.11.1
Address check	18.14.11.1
RBC interlock	13.74.02.1
Inst check	18.14.11.1
System controls	
1401 compat	12.65.10.1
Priority alert	19.10.07.1
Off normal	40.10.03.1
Stop	11.10.02.1
Priority switch lamps	19.10.01
Power Indicator lights	98.15.10.0

1415 SWITCHES

Check test	18.14.10.1
Computer reset	12.65.01.1
Mode	40.10.01.1
Program reset	12.65.01.1
Power On, Off, dc	98.15.10.0
Start	12.15.02.1
Stop	12.15.03.1
C E switches	40.10.01.1-.03.1
1401 comp	12.65.10.1
1401 I/O check reset	13.65.01.1
1401 I/O check stop	12.15.04.1
Priority switch	19.10.01
Sense bit switches	15.60.01.08

C E SWITCHES

Address stop	12.15.04.1
Addr stop -- scope sync	14.17.17.1-.19.1
B ch char sel	15.30.10.1
Transfer add to star	14.71.30.1
1414 Mod 3 & 4	51.45.07.1-.15.1

1411 LATCHES

1st I-O Cyc Ctl	13-70-03	C Cyc Ctl	12-12-20
1st Trgr Check	18-14-06	CAR U 0, 1, 2, 4, 8	14-12-01
1 SCN	12-30-01	CAR T 0, 1, 2, 4, 8	14-12-02
1 SCN Ctl	12-30-03	CAR H 0, 1, 2, 4, 8	14-12-03
2 SCN	12-30-02	CAR TH 0, 1, 2, 4, 8	14-12-04
2 SCN Ctl	12-30-04	CAR TTH 0, 1, 2, 4, 8	14-12-05
3 SCN	12-30-02	Carry	16-20-21
3 SCN Ctl	12-30-04	Carry Ctl	16-20-21
1401 Br Ltch	12-60-19	Chck OP Mod *	18-14-05
1401 Cd-Pr in Proc	13-70-02	Chck OP Reg *	18-14-04
1401 Cd Pr Error Spl	13-70-03	Clock Pulse *	11-10-02
1401 File Add Comp	13-65-02	Comp	16-20-15
1401 File WLR	13-65-02	Comp B	16-20-10
1401 File VC	13-65-02	Compl Ctl	16-20-15
1401 I-O End	13-70-02	Console WM Char	15-60-09
1401 I-O Pch	13-70-02	D Cyc	12-12-07
1401 I-O Prt	13-70-01	D Cyc Ctl	12-12-21
1401 I-O Rd	13-70-01	DAR U 0, 1, 2, 4, 8	14-13-01
1401 Inq Error	13-65-08	DAR T 0, 1, 2, 4, 8	14-13-02
1401 Process Chk	13-65-03	DAR H 0, 1, 2, 4, 8	14-13-03
1401 Rd Error	13-65-01	DAR TH 0, 1, 2, 4, 8	14-13-04
A Cyc	12-12-01	DAR TTH 0, 1, 2, 4, 8	14-13-05
A Cyc Ctl	12-12-20	Dec Ctl	17-12-04
A Data Reg 1	15-39-01	Delayed Interrupt	19-10-06
A Data Reg 2	15-39-02	Div Ovrflw	16-45-01
A Data Reg 4	15-39-03	E 1 Reg 1	15-60-21
A Data Reg 8	15-39-04	E 1 Reg 2	15-60-22
A Data Reg A	15-39-05	E 1 Reg 4	15-60-23
A Data Reg B	15-39-06	E 1 Reg 8	15-60-24
A Data Reg C	15-39-07	E 1 Reg A	15-60-25
A Data Reg WM	15-39-08	E 1 Reg B	15-60-26
A Ring 1	14-70-01	E 1 Reg C	15-60-27
A Ring 2	14-70-02	E 1 Reg WM	15-60-28
A Ring 3	14-70-03	E 1 Reg Full	15-41-10
A Ring 4	14-70-04	E 1 Reg WD Sep	15-41-11
A Ring 5	14-70-05	E 2 Reg 1	15-60-21
A Ring 6	14-70-06	E 2 Reg 2	15-60-22
AAR U 0, 1, 2, 4, 8	14-10-01	E 2 Reg 4	15-60-23
AAR T 0, 1, 2, 4, 8	14-10-02	E 2 Reg 8	15-60-24
AAR H 0, 1, 2, 4, 8	14-10-03	E 2 Reg A	15-60-25
AAR TH 0, 1, 2, 4, 8	14-10-04	E 2 Reg B	15-60-26
AAR TTH 0, 1, 2, 4, 8	14-10-05	E 2 Reg C	15-60-27
ADDR CH ERR	18-14-03	E 2 Reg WM	15-60-28
ADDR Chck	18-14-11	E 2 Reg Full	15-41-10
ADDR Exit Err	18-14-02	E 2 Reg Wd Sep	15-41-11
Asterisk Fill	17-12-05	E Ch 1st Char 2nd Addr	13-72-01
B Cyc	12-12-02	E Ch 2nd Add Xfr	13-72-01
B Cyc Ctl	12-12-21	E Ch E O 2nd Add Xfr	13-72-01
B Data Reg Char O	36-11-01	E Ch Busy	12-62-02
B Data Reg Char 1	36-11-02	E Ch Check	12-62-04
B Data Reg Char 2	36-11-03	E Ch Cond	12-62-04
B Data Reg Char 3	36-11-04	E Ch Corr Lng Rec	13-63-03
BAR U 0, 1, 2, 4, 8	14-11-01	E Ch Disc	13-42-11
BAR T 0, 1, 2, 4, 8	14-11-02	E Ch E O Rec	13-63-01
BAR H 0, 1, 2, 4, 8	14-11-03	E Ch Ext E O Xfr	13-42-11
BAR TH 0, 1, 2, 4, 8	14-11-04	E Ch File Add Xfr Gate	13-72-02
BAR TTH 0, 1, 2, 4, 8	14-11-05	E Ch File St Gte	13-72-01
Bin Reg A1 Bit	14-18-02	E Ch File Strobe	13-72-02
Bin Reg A2 Bit	14-18-01	E Ch Input Mode	15-62-01
Bin Reg A4 Bit	14-18-01	E Ch Int E O Xfr	13-63-01
Bin Reg A8 Bit	14-18-02	E Ch Int E O Xfer Del	13-65-05
Bin Reg B4 Bit	14-18-20	E Ch Last Inp Cyc	13-63-02
Bin Reg B8 Bit	14-18-20	E Ch Load Mode	15-62-02
Body	16-30-04	E Ch No Xfr	13-72-04
Body Ctl	16-30-04	E Ch Not Rdy	12-62-01
Br To 0001 Ltch	12-60-14	E Ch Move Mode	15-62-02
Br To AAR Ltch	12-60-14	E Ch Output Mode	15-62-01
C Cyc	12-12-06	E Ch Ovlp	13-60-04

* - denotes trigger

1415 LATCHES AND TRIGGERS

Addr Set rtne	41-10-02
Clock 1 Cons	45-10-01
Clock 2 Cons	45-10-01
Clock 3 Cons	45-10-01
Clock 4 Cons	45-10-03
Cons Bcksp Ctl	45-50-13
Cons Carr Rtrn Comp	44-10-03
Cons Char Ctl	45-50-10
Cons Chck Strobe	45-50-01
Cons Cyc Start	41-10-01
Cons Error Ctl	45-50-12
Cons Inquiry Req	41-30-01
Cons Output Error	45-50-11
Cons Prtr Not Busy	45-50-08
Cons Prtr Strobe	45-50-02
Cons Stop Print	44-10-02
Cons Strobe Gate	45-50-02
Cons WM Ctl	45-50-09
Ptr Strobe Reset	45-50-02
Display WM Ctl	45-30-01
Display Routine	41-10-03
Full Line Cond Altr	41-20-01
Function Ctl	45-50-14
Lock Cond Proceed	45-50-16
MX Gate ltch	45-20-06
Prtr E O Line	45-50-15
Prtr Last Col	45-50-15
Type Start	45-50-03
Type Start Ctrl	45-50-01
Rd OP Intlk Cons	41-30-02
Storage Scn Routine	41-10-03
X 1A	45-20-05
X 1	45-20-05
X 2	45-20-05
X 3	45-20-05
X 4	45-20-06
X 5	45-20-06
X 6	45-20-06
Y 1	45-20-02
Y 2	45-20-02
Y 3	45-20-03
Y 4	45-20-03
Y 5	45-20-04
Y 6	45-20-04
WM Cond Alter	41-20-01
WM Period	45-50-11

1414 LATCHES AND TRIGGERS

Adv by 2	53-33-05
After 9 CAM	52-10-14
Auto Space	53-55-01
Block Data Reg	51-50-01
Brush SS Ltch	52-10-10
Buff Full PT	55-10-02
Busy Ctl PT	55-10-01
Busy PT	55-10-02
Carriage Moving	53-55-03
CB A-1	52-20-02
CB Ltch	52-10-10
CCC Reg A-1	53-50-01
*CE Check	51-14-01
CE GO	51-50-03
CE Reader Rdy	52-11-01
Chain Home	53-30-01
Channel 12-7	53-53-01
Channel 6-1	53-53-02
Clock 000-100	51-30-03
Clock Check	51-30-01
*Clock Error	51-30-01
Compare A	53-33-03
Compare B	53-33-03
Compare 8	53-33-02
Compare 4	53-33-02
Compare 2	53-33-01
Compare 1	53-33-01
Ctl Bit Serial	51-50-05
*Data Reg A-1 Int Buff	51-10-02
*Data Reg A Prt Buff	53-10-01
*Data Reg B Prt Buff	53-10-01
*Data Reg C Prt Buff	53-10-01
*Data Reg 8 Prt Buff	53-10-02
*Data Reg 4 Prt Buff	53-10-02
*Data Reg 2 Prt Buff	53-10-02
*Data Reg 1 Prt Buff	53-10-02
Data Reg A-1 PT	55-10-03
Delay Forms	53-51-06
Delay Latch	53-23-03
Delay Rst	53-55-03
E O File	52-11-01
E O File Dly	52-11-01
*E O Scan	51-32-01
E O Xfr 1	51-40-12
E O Xfer 2	51-40-12
Emitter Delay	53-52-02
Equal Compare	53-10-01
Error PT	55-10-06
Fast or Slo Skip	53-54-01
*Five Ring 1-5 Prt	53-21-01
Five Ring Adv	53-23-02

Form Check	53-42-01
*Hammer Check Reg	53-10-01
Hammer Row Bit Reg	53-10-02
Holdover 132	53-40-02
*Home, Printer	53-22-01
Indicator Ch 9	53-56-01
Indicator Ch 12	53-56-01
Insert C Bit	53-11-05
*LX Data Reg	51-10-01
*LY Data Reg	51-10-01
Man Reg Rst	53-50-02
Man Reg Space	53-50-02
Multi-Rd Fd Latch	52-10-08
No Xfr	51-40-12
Parity 1	51-18-01
Parity 1 Prt	53-44-02
Parity 2	53-44-01
Parity 2 Prt	53-44-02
PCH Check 1	52-12-02
PCH Check 2	52-12-02
PCH FD	52-10-15
PCH Priority Request	52-10-01
PCH Data Reg	51-10-01
PCH Request	52-10-15
*PCH SCN	52-10-02
PCH SCN CB Latch (2F&3J)	52-10-14
PCH Stack Sel	52-13-01
Punch FD	52-10-14
PCH Xfr	52-10-15
PCH Xfr Check	52-12-01
Print Error	53-12-01
Print in Process	53-51-06
*PRT Line Cmplete Reg	53-10-01
PS 1-32	53-32-01
PSS 1	53-31-01
PSS 2	53-31-01
PSS 3	53-31-01
PSS Tgr	53-30-01
Rd Fd	52-10-09
Rd Fd Ltch	52-10-08
Rd Pls 1 Int Buff	51-30-05
Rd Pls 2 Int Buff	51-30-05
Rd Priority Request	52-10-01
Rd Request	52-10-07
Rd Request PT	55-10-06
*Rd Scn	52-10-02
Rd Scn PT	55-10-07
Rd Xfr Req PT	55-10-06
Rd Xfr Request	52-10-09
Rdy Print	53-40-01
Ready	51-40-04
*Read Check	52-12-01
Read In, Prt	53-40-01
Read Request	51-40-01

Ring Check Tgr	51-32-02
Ring Err 1	51-32-02
*Ring Err 2	51-32-02
Scan Call, Prt	53-40-01
Scan Req PT	55-10-07
*Scan, Prt	53-40-01
Serial Scn Latch	51-50-06
Single Line	53-42-01
Stacker 1	52-13-02
Stacker 2	52-13-02
Stacker 4	52-13-01
Stacker 8	52-13-01
Start Latch	53-42-01
Start Latch CE	51-50-03
Stop Latch CE	51-50-03
Strobe	51-40-43
Strobe Pls Int Buff	51-30-05
Switch Bounce	53-42-01
Sync Chck	53-43-01
Sync Ctl 1	55-10-01
Sync Ctl 2 Pt	55-10-01
Sync Holdover	53-12-01
*Ten Ring 0-7	51-32-01
*Ten Ring 0-4 Prt	53-20-01
*Ten Ring 5-9 Prt	53-20-02
Ten Ring AC	51-32-02
Ten Ring Adv Prt	53-23-02
*Three Ring 1 Prt	53-22-01
*Three Ring 2 Prt	53-22-01
*Three Ring 3 Prt	53-22-01
Three Ring Adv Prt	53-23-02
Time Pls 1	51-30-02
Time Pls 2	51-30-02
Turn Off Rings	53-23-01
*Unit Ring 0-9	51-31-01
*Unit Ring Error	51-31-02
*UX Data Reg	51-10-01
*UY Data Reg	51-10-01
*Validity Latch	52-12-02
Wr Pls Int Buff	51-30-05
Z Pls Int Buff	51-30-05
1st Rd Data Reg	51-10-01
2nd Rd Data Reg	51-10-01
1401 CCC Reg Rst	53-50-03
1401 Rd Ltch	52-10-08
51 Col Cd Proceed	52-10-11

LATCH LOCATIONS -- 1414-I-II-VII **

A Reg VRC	60-50-51	R-W Reg 1 Bit	60-40-50
Backspace	60-60-40	R-W Reg 2 Bit	60-40-50
Backward	60-60-40	R-W Reg 4 Bit	60-40-50
Check Character	60-40-61	R-W Reg 8 Bit	60-40-51
Compare Check	60-50-30	R-W Reg A Bit	60-40-51
Disconnect	60-60-31	R-W Reg B Bit	60-40-51
Erase	60-60-31	R-W Reg C Bit	60-40-52
Error Latch	60-50-50	R-W Reg VRC	60-50-50
First Bit	60-40-60	Rewind	60-60-02
First Character	60-40-60	Rewind Unload	60-60-02
Forward Stop Delay	60-30-56	Skew Error	60-50-51
Gate On Final Amps	60-30-52	Turn On TI	60-60-50
Go	60-60-11	Write	60-60-30
Load Point	60-60-02	Write Condition	60-60-30
No Echo Latch	60-50-50	Write Delay	60-30-11
Odd Redundancy	60-40-61	Write Disc Delay	60-30-11
Read Condition	60-60-20	Write Tgr Release	60-60-31
Read Delay	60-30-10	Write TM	60-40-31
Read Disc Delay	60-30-10	CE Switches	60-68-05
Read Only	60-60-20	Indicators	60-68-60,62

**For 1414-VII, ALD page numbers start with 90. Thus: 90-XX-XX.

Name	ALD Page	Level	Test Point	Possible Cause
Address Exit VC	18.14.02.1	+S	*11D2C10H	Not 2 of 5 on channel
Address Ch VC	18.14.03.1	+S	*11D2C10D	Not 2 of 5 on channel
B Channel VC	18.12.03.1	-S	11D2B12A	Even bits
Op Reg Set	18.14.04.1	-S	11D2C17F	No set pulse during I op
Op Mod Reg Set	18.14.05.1	-S	11D2C20F	No set pulse
Instruction Check	18.14.11.1	-S	11D2C17C	Fail to set cycle control
Address Check	18.14.11.1	-S	11D2K15C	Zones in other than tens or hundreds
A Reg Set	18.14.07.1	-S	11D2D6F	Fail to reset or set A Reg
A Character Select	18.14.01.1	-S	11D2C03A	More than one gate to a channel
A Channel VC	18.11.03.1	-S	11D2B12B	Even bits
B Reg Set	18.14.06.1	-S	11D2C24F	Detect failure to start memory clock
B Character Select	15.30.10.1	-S	11C3E08D	More than one char gated to B channel
Assem Ch VC	18.13.03	-S	11C4C25A	Even bits
I/O Interlock	18.14.11	-S	11D2F16D	No R (I) ‡ given since last I/O op
1401 Card Print	18.14.08	-S	11D2F17R	Data check on sel I/O unit
1401 Punch Print	18.14.08	-S	11D2F17Q	Condition on punch or printer

(1401 errors do not have a console indicator.)

*-Trigger output.

Error Detection Summary may be found under Service Aids.

Name	ALD Page	Level	Test Point	Possible Cause
Address Exit VC	18.14.02.1	+S	*11D2C10H	Not 2 of 5 on channel
Address Ch VC	18.14.03.1	+S	*11D2C10D	Not 2 of 5 on channel
B Channel VC	18.12.03.1	-S	11D2B12A	Even bits
Op Reg Set	18.14.04.1	-S	11D2C17F	No set pulse during I op
Op Mod Reg Set	18.14.05.1	-S	11D2C20F	No set pulse
Instruction Check	18.14.11.1	-S	11D2C17C	Fail to set cycle control
Address Check	18.14.11.1	-S	11D2K15C	Zones in other than tens or hundreds
A Reg Set	18.14.07.1	-S	11D2D6F	Fail to reset or set A Reg
A Character Select	18.14.01.1	-S	11D2C03A	More than one gate to a channel
A Channel VC	18.11.03.1	-S	11D2B12B	Even bits
B Reg Set	18.14.06.1	-S	11D2C24F	No X or Y current or strobe
B Character Select	15.30.10.1	-S	11C3E08D	More than one char gated to B channel
Assem Ch VC	18.13.03	-S	11C4C25A	Even bits
I/O Interlock	18.14.11	-S	11D2F16D	No R (I) ‡given since last I/O op
1401 Card Print	18.14.08	-S	11D2F17R	Data check on sel I/O unit
1401 Punch Print	18.14.08	-S	11D2F17Q	Condition on punch or printer

(1401 errors do not have a console indicator.)

*-Trigger output.

Error Detection Summary may be found under Service Aids.

Name	Ref Pin	Logic
I cycle	11C1H22H	12.12.04.1
A cycle	11C1H22A	12.12.01.1
B cycle	11C1H22C	12.12.02.1
C cycle	11C1E24D	12.12.06.1
D cycle	11C1D03H	12.12.07.1
X cycle	11C1G22A	12.12.05.1
Logic gates		
A	11C2J12A	11.10.10.01
B	11C2J12C	11.10.11.1
C	11C2J16A	11.10.12.1
D	11C2J16C	11.10.13.1
E	11C2J21A	11.10.14.1
F	11C2J21C	11.10.15.1
G	11C2J22C	11.10.16.1
H	11C2J23C	11.10.17.1
J	11C2J24C	11.10.18.1
K	11C2J25C	11.10.19.1
R	11C2J26C	11.10.20.1
S	11C2K20C	11.10.21.1
T	11C2K17C	11.10.22.1
U	11C2K16C	11.10.23.1
V	11C2K15C	11.10.24.1
W	11C2K14C	11.10.25.1
X	11C2K13C	11.10.26.1
Y	11C2K12C	11.10.27.1
LL gate	11C2F09H	11.10.06.1
I op	11C1H07A	11.20.01.1
1	11C1J11A	11.20.02.1
2	11C1K11C	11.20.02.1
3	11C1K12C	11.20.03.1
4	11C1K13C	11.20.03.1
5	11C1H14C	11.20.04.1
6	11C1H14E	11.20.04.1
7	11C1K16C	11.20.05.1
8	11C1K17C	11.20.05.1
9	11C1K18C	11.20.06.1
10	11C1C26C	11.20.06.1
11	11C1K20C	11.20.07.1
12	11C1K21C	11.20.07.1
1st address	11C1J16C	11.20.11.1
2nd address	11C1K16K	11.20.11.1
Units ltch	11C2D16A	16.30.02.1
Ext ltch	11C2D16C	16.30.06.1
A ring		
1	11C1E03C	14.70.01.1
2	11C1D04C	14.70.02.1
3	11C1D05C	14.70.03.1
4	11C1H17H	14.70.04.1
5	11C1D07C	14.70.05.1
6	11C1D08C	14.70.06.1

Name	Ref Pin	Logic
No scan	11C1G24D	12.30.01.1
1st scan	11C1E26A	12.30.01.1
2nd scan	11C1E26C	12.30.02.1
3rd scan	11C1E26H	12.30.02.1
Last Instr RO	11C1H23B	12.12.51.1
Last Execute Cycle	11C1H12G	12.13.05.1

1414 INTEGRATED BUFFER CE PANEL INDICATORS

Integrated buffer:	
Read	51.45.04
Punch	51.45.04
Options	51.45.04
Buffer address:	
End of scan	51.45.01
Units and tenths	51.45.01
Buffer register:	
Check search	51.45.02
Clock check	51.45.01
Data reg (BCD)	51.45.03
Ring check	51.45.01
YU, YL, XU, XL	51.45.02
Print address:	
Home	51.45.05
Ring	51.45.05
Print buffer:	
Print	51.45.06
Print register:	
Data reg (BCD)	51.45.06
Hammer check	51.45.06
Print line complete	51.45.06

1414 TAPE INDICATORS

Char counter	XX.68.62.1
Delay counter	XX.68.62.1
Inst ring	XX.68.62.1
Read clock	XX.68.60.1
SPC ring	XX.68.62.1
Write clock	XX.68.60.1
Checks	
A reg VRC error	XX.68.61.1
Comp error	XX.68.61.1
Echo error	XX.68.61.1
Error latch	XX.68.61.1
R/W reg VRC error	XX.68.61.1
Skew error	XX.68.61.1
Registers	
A reg	XX.68.60.1
B reg	XX.68.61.1
LRCR	XX.68.60.1
R W	XX.68.60.1

Other indicators

Bksp	XX.68.61.1
Bkwd	XX.68.61.1
Check char	XX.68.61.1
DC on	XX.68.62.1
Disc	XX.68.61.1
Erase	XX.68.61.1
First char	XX.68.61.1
Fwd stop relay	XX.68.62.1
Go	XX.68.61.1
Load point	XX.68.62.1
No echo	XX.68.62.1
Odd red	XX.68.62.1
RDD	XX.68.61.1
Read	XX.68.61.1
Read cond	XX.68.61.1
Read delay	XX.68.61.1
Rewind	XX.68.62.1
Rewind unload	XX.68.62.1
WDD	XX.68.61.1
WR cond	XX.68.61.1
WR delay	XX.68.61.1
Write	XX.68.61.1
WR rel	XX.68.62,1
WTM	XX.68.61.1

1402 READER PUNCH INDICATORS

Chips	51.03.14
End of file	51.03.12
Fuse	51.03.11
Power	51.03.12
Punch check	51.03.12
Punch ready	51.03.13
Punch stop	51.03.15
Reader check	51.03.12
Reader ready	51.03.13
Reader stop	51.03.12
Stacker	51.03.11
Transport	51.03.11
Validity	51.03.12

1403 PRINTER

End of forms	01.06.1
Forms check	01.06.1
Print check	01.06.1
Print ready	01.06.1
Sync check	01.06.1

TAPE UNIT INDICATORS

729	TU 12.00.1
	00.06.1
7330	73.04.01.0

1414 INTEGRATED BUFFER SWITCHES AND JACKS (CE)

Bit switches	51.45.07
Buffer mode	51.45.12
Buffer select (DK-1&4)	51.45.14
Buffer select (DK - 2)	51.45.10
Buffer select (DK - 3)	51.45.15
Carriage space	51.45.09
Check stop	51.45.09
Ground jack	51.45.09
Intg buffer sync	51.45.08
Marginal check jacks	98.14.11
Off line	51.45.09
Off line mode sw (DK-1, 2 & 3)	51.45.11
Power on & off	98.14.10
Print buffer sync	51.45.08
Remote start recept	51.45.13
Single cycle	51.45.09
Single or cont operation	51.45.09
Start, stop, reset	51.45.13
Sync jack	51.45.09

SERVICE AIDS

1411 Error Check Switches

All 1411 operations are thoroughly checked with error detection circuits. You should develop the habit of testing the operation of these check circuits before starting to analyze any machine problem. Switches to test the check circuits are located on the console. To test:

Press "Check Switch # 1" and the "Start" key; all error lights should come on.

Compute Reset, and press "Check Switch # 2" and "Start" key; again, all error lights should light.

Compute Reset, press "Check Switch #3" and "Start" key; again, all error lights should light.

Address Sync

Address switches on the 1411 CE panel may be set to cause an output at the sync hub, on the same panel, for any chosen core address. This address can be further conditioned by:

The scan switch on the 1411 CE Panel

and/or

Any condition you choose to wire to Pin "H" of the block at 2D, Logic 14.17.18.

CE "AND" Circuit

1411 -- The "Minus OR" (plus AND) block at 3G, Logic 14.17.18, is available for switching together any pulses. This may be used to manufacture a sync pulse, or to force the machine to stop on certain conditions, etc.

1414-3, -4 Sync Hub AND Circuit

On ALD 51.50.04 additional inputs can be AND'ed with the address sync output available at the CE panel sync hub.

Master Error Circuit

When a problem exists that may be detected more readily by disabling the master error circuit, it is possible to accomplish this by connecting a jumper from ground (any Pin J) to pin G of 1411D2E22 (Logic 18.14.08.1)

If this method is used, care must be taken to insure that the jumper is not left in place when the machine is returned to the customer.

Forcing The Machine To Stop

The machine normally stops at the end of some cycle. Stopping the machine at the time an error occurs during a cycle can be accomplished by removing the "Error Sample" input (taping pin) to block 2F, Logic 18.14.08.

Caution: Never force a stop with 2nd clock pulse on! This could damage core storage circuit resistors.

Forcing Signals

A solid +S signal can be forced by wiring the required pin to ground.

Caution: Because some emitter followers are returned to a minus voltage through a very low impedance, care must be used in grounding emitter followers. However, if a -S level is desired, place a 4700-ohm resistor in series with the jumper circuit to provide a proper load. Check to see that the pin is held sufficiently negative.

Voltage Jumpers

Exercise care when working around the wiring side of any chassis to prevent dislodging any voltage jumpers. These can be easily dislodged because they have clip-on terminals.

Shorted DE Logic Blocks

When a shorted DE Block is encountered, always check the preceding card. If the short was caused by a down level, the preceding circuit may be damaged.

Core Storage

When X, Y, inhibit, etc., lines are suspected of being open, they may be tested with an ohmmeter, but machine power must first be turned off. Also, if a burnt core is suspected and the core location is visible, the lines through or around the core will be a light copper color near the core itself. The rest of the line will be reddish copper due to the insulating material.

Insulating Pins

Do not overlook the value of insulating pins when troubleshooting. Inputs to "+AND" switches can be forced all the time by using a card extender and pulling the desired wire loose. This method can enable scoping of some circuits, in a static state, which are normally active only when some infrequently occurring input is available.

POWER SUPPLY TIPS

If trouble is in an individual power supply, note the following:

There is a 90% chance it is the SMS card (low or no adjustment of output voltage).)

If voltage is high with no adjustment, then one of the series regulator transistors is shorted (or SMS card is bad).

With power supply removed you may wire 110 vac into TB 1 pins 1 & 2. Output may not reach full value but should be close and adjustable. (Remove over-voltage device).

Visually inspect unit for crimped wires or cable chafing on screw ends. (Unit may work in opened position, but not in closed.)

An open diode in rectifier circuit will show up as low voltage under load. Output voltage ripple will be excessive. Also this may be detected by feeling the diodes, they will be quite warm if operating normally. If one is colder, it is open. Remove power before touching any component.

A shorted diode in rectifier circuit will probably pop the circuit breaker in the primary of the input transformer, but not necessarily; it may pop the over-current circuit breaker, due to over-voltage spikes on the output. With the over-voltage device removed, the spikes will be visible.

A shorted or open series regulator transistor can be detected by scoping or feeling the resistors in their emitter circuit. Remove power before touching any component.

Check voltages after machine has been on 15 minutes. Voltage may drift slightly between cold and warm state.

Do not ground heat sink (may ground to holding screws at corners of unit).

Marginal Check Jacks* (98.11.17)

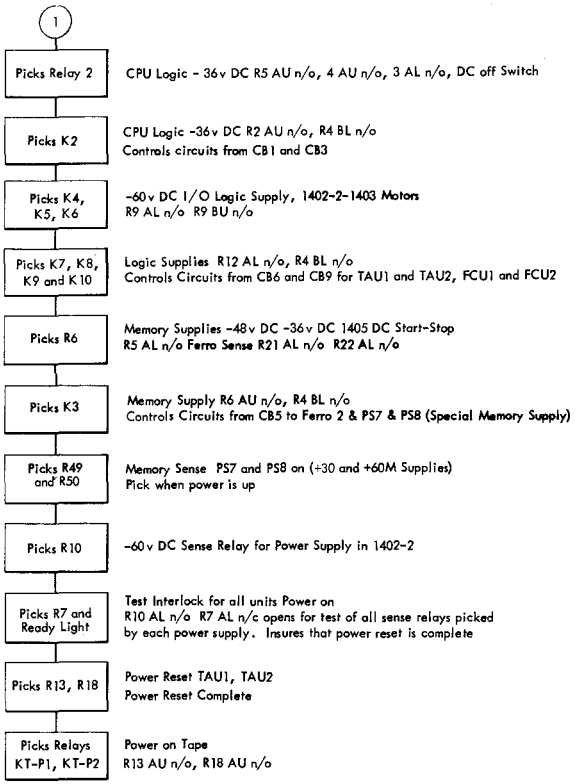
Jack	Chassis
J1	11B2
J2	11B3
	11B4
J3	11C (all)
J4	11D (all)

* Only +12vdc is affected.

1.5 megacycle oscillator for marginal checking - P/N 370823.

Circuit Type	Line Symbol	Voltage Reference	Voltage Level (Nom) Positive	Negative	Current Level Positive	Negative
Current switch	+N	0	+0.8	-0.8		
	+P	-6	-5.2	-6.8		
Ctdl	+T	0	+6.0	-6.0		
	+U	-6	0.0	-12.0		
Ctrl	+R	0	+12.0	0.0		
Sdtrl*	+S	0	0.0	-12.00		
Sdtdl	+Y	0	0.0	-6.0		
Indicators	M		0.0	-36.0		
Relays	-W		0.0	-48.0		
Cores	+Z		+6.0	-6.0		
Special	+C		+0.5	-0.5	0 ma	13.5 ma
Console and Memory	V		0.0	-36.0		
1403	U		0.0	-12.0		
1403	T		+6.0	-6.0		
1403	U		0.0	-12.0		
1403	T		+6.0	-6.0		
Accelerator	B		+6.0	0.0		

* Any +S level lower than -6.60v, or any -S level higher than -6.85v may cause failure and should be corrected.



PUNCH MAGNET DRIVER CHART (1414 -3, -4 PANEL A4)

Tens	Matrix Switch	Units x0	x1	x2	x3	x4	x5	x6	x7	x8	x9
0x	A08	F11	E05	E05	E05	E04	E04	E04	E03	E03	E03
1x	A08	F02	F02	G02	G02	H02	H02	J02	J02	K02	K02
2x	A08	F03	F03	G03	G03	H03	H03	J03	J03	K03	K03
3x	A08	F04	F04	G04	G04	H04	H04	J04	J04	K04	K04
4x	A08	F05	F05	G05	G05	H05	H05	J05	J05	K05	K05
5x	A09	F06	F06	G06	G06	H06	H06	J06	J06	K06	K06
6x	A09	F07	F07	G07	G07	H07	H07	J07	J07	K07	K07
7x	A09	F08	F08	G08	G08	H08	H08	J08	J08	K08	K08
	A09	F09	F09	G09	G09	H09	H09	J09	J09	K09	K09

HAMMER DRIVE CHART - 1414 - III, IV (PANEL 3)

Column	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
	53.62.05.1				53.62.04.1						53.62.03.1						53.62.02.1						53.62.01.1					
									B										B									
Row H		130	121	118	112	103	100	91	L	88	82	73	70	61	58	52	43	L	40	31	28	22	13	10	1			
									A									A										
		127	124	115	109	106	97	94	N	85	79	76	67	64	55	49	46	N	37	34	25	19	16	7	4			
									K									K										
	53.62.10.1				53.62.09.1						53.62.08.1						53.62.07.1						53.62.06.1					
									B										B									
Row J		131	122	119	113	104	101	92	L	89	83	74	71	62	59	53	44	L	41	32	29	23	14	11	2			
									A									A										
		128	125	116	110	107	98	95	N	86	80	77	68	65	56	50	47	N	38	35	26	20	17	8	5			
									K									K										
	53.62.15.1				53.62.14.1						53.62.13.1						53.62.12.1						53.62.11.1					
									B										B									
Row K		132	123	120	114	105	102	93	L	90	84	75	72	63	60	54	45	L	42	33	30	24	15	12	3			
									A									A										
		129	126	117	111	108	99	96	N	87	81	78	69	66	57	51	48	N	39	36	27	21	18	9	6			
									K									K										

View from Card Side of Gate

PRINTER SCOPING TECHNIQUE--1403

Tiedown of home pulse:

Remove the card at location 14A1E22 (53.40.01, 2H), insert it on a card extender, and pull extender wire to isolate pin Q, the carriage stopped line. Then jumper from pin P at 14A1F15 (53.30.01, 5E), chain home, to pin Q on the card in the extender.

ERROR DETECTION SUMMARY

Program Checks

I/O Interlock: (18.14.11) Program failed to use R(I)‡ or R(I)d that branched between I/O operations on same channel. CPU stops at I3 for M/L/U op codes, and at I op for F/K op codes.

Address Check: (18.14.11) Address has zone bits in the ten thousand, thousands, or units position.
Reverse scan past highest storage address except during move, load, clear op, or display or alter operations.
Forward scan through address 00000.

RBC Interlock: (13.74.02) Program failed to follow a file write op with a read back check before attempting another file op on that channel.

Instruction Check: (18.14.11) The five (5) actual logic lines that can bring up Instruction Check are:

1. No "Stop at--" for the logic clock.
*2. Both the logic clock and extention ring running (LGA and LGR).
3. The TLU mod = 8, A, or B bit.
4. No cycle control latch on at LLG.
*5. More than one cycle control latch on at LLG, except E, or F with A, B, C, D, I or X.

Program Errors that will cause an instruction check:

1. TLU mod = 8, A, or B bit.
2. Undefined mod for J or Y op code. (Neither the branch or no branch is set. Result: No I or B cycle control latch on) Stop I7 LGA.
3. Illegal op codes (No op code grouping lines available to set I cycle control for I2) Stop - I1 LGA.
4. No Word Mark (I op or LIRO) or improperly placed Word Mark will prevent setting I cycle control.
   If a stop occurs in either I op LGA or during the cycle, the improperly placed WM is read out of core.

* Not on early machine.

Machine Errors that will cause an instruction check:

1. No "Stop at ---" line for Logic Clock. No Stop - with no clock lights on.
2. Both clocks running (LGA and LGR ON).
3. Failure to set some cycle control latch. (A, B, C, D, E, F, I, X) Stop - LGA with the last-cycle light ON.
4. More than one cycle control ON. (A, B, C, D, X, I) Stop - same as Item 3.
5. Both E and F cycle control ON. Stop - same as Item 3

Note: An E or F cycle control ON with A or B or C or D or I or X ON is correct.

Both a Branch and the No Branch latches ON cause both I and B cycle control.

Neither Branch or No Branch ON will fail to set I or B cycle control. (Op Codes J, Y, R, X, B, V, W).

Failure to set B > A, B=A, B < A or setting more than one will cause the above Branch, No Branch failure.

Process Checks

A Channel VC: (18.11.03) Even parity detected on A channel.

B Channel VC: (18.12.03) Even parity detected on B channel. (Selected B character is only character checked. Failure to regen an unselected character not detected until it is selected to B Channel.)

Assembly Channel VC: (18.14.03) Even parity detected on assembly channel.

Address Channel: (18.14.03) Checked to insure 2 out of 5 bits on Channel. Checked every logic gate except LG "A" in 1401 mode. Bits inserted to satisfy validity when actual data is not gated to channel.

Address Exit Channel: (18.14.02) Checked at every sample time for correct (2 of 5) parity. Zero (2 and 8 bit) inserted on channel to satisfy validity on cycles that data is not gated from address registers.

A Register Set: (18.14.07) Checks to insure A-reg reset pulse on every cycle that A-reg is to read in. (Reset at LGC, Set at LGD.)

B Register Set: (18.14.06) Insures that B reg receives reset pulse very storage cycle. Detects failure to start memory clock (no B reg reset pulse developed). If there is a failure in X, Y, or strobe pulses, B reg resets but no data reads in. This error is detected by B-ch VC.

Op Register Set: (18.14.04) Insures that op reg receives set pulse at every I op time. Occurs if a blank is defined as an op code (WM/blank combination) for both 1410 or 1401 mode if EC251766 is installed.

Op Modifier Set: (18.14.05) Insures that op mode receives set pulse on proper cycles. This is I1 for "2 character op codes," I6 for "1 address plus mod op," and I11 for "2 address plus mod op."

A Character Select: (18.14.01) Insures that one and only one input is gated to A channel every cycle. (Op mod is gated to satisfy A channel VC on cycles that other A data is not required on A channel.)

B Character Select: (15.30.10) Insures that one and only one character is selected to read out to B channel and that character is gated to regen or load (B character select switch on CE panel in other than normal position when running attempted).

1401 Mode Differences

I/O Interlock: Not set.

Instruction Check: Blocked for 1401 I/O instructions (op codes 1 through 7).

Op Modifier Set Check: Blocked in 1401 mode.

Manual Operations

Display or Alter: Blocks A channel VC, B channel VC, Assembly channel VC, and address check when wraparound occurs.

Storage Scan: On load operations, B channel VC is blocked. On load or regen, op mod set check and address check are blocked.

Address Set: All error circuits blocked by blocking master error sample.

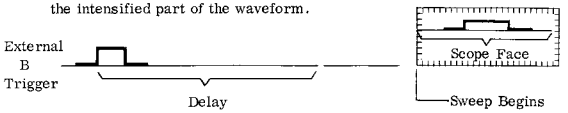
1411 DC DISTRIBUTION

Module	Voltage	Destination
1	-12	11B2
2	-12	11D1
3	-12	11D3
4	-12	11B3
5	-12	11C3
6	-12	11C2
7	+30 (spec)	11B3
8	+60 (spec)	11B3
9	-6	11B4
10	+30	11B3
11	-36	11B3
12	+12M	All frames
13	-12	11D4
14	-48	Relay circuits

OSCILLOSCOPE DELAYED SWEEP

Usual method: Sweep occurs at the end of the delay.

1. Connect the external sync to time base B.
2. Set the horizontal display control to B intensified by A.
3. Turn the A time base stability-triggering level controls fully clockwise.
4. Adjust the time base B stability-triggering control in the normal manner for a trace.
5. Adjust the time base A time/cm control and the delay time multiplier until the desired part of the waveform is intensified. (Make certain time base B is greater than time base A.)
6. Set the horizontal display control to A delayed by B to see the intensified part of the waveform.

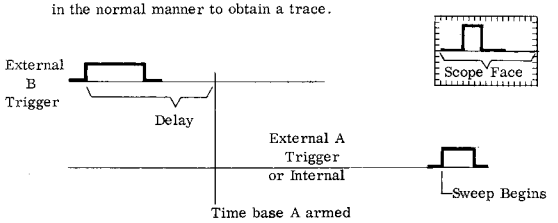


Occasionally, when the usual method is used, a jittery trace or unstable waveform on the scope results. In these instances another sync method may be used to stabilize the trace.

Jittery trace method: double sync is used.

The sweep occurs as a result of a time base A triggering pulse, internal or external, after the time base B delay is completed.

1. Set up the scope as in the usual method.
2. Connect the second external trigger to the time base A trigger input and, if external trigger is used, set the triggering mode control to external; if not, set the triggering mode control to internal.
3. Adjust the time base A stability-triggering level control in the normal manner to obtain a trace.



CE SEVEN CARD LOADER L1A

Store at 00000: RL%1100011$R (for channel 1 reader)

(or) XL□1100011$X (for channel 2 reader)

Computer reset and start.
Program Entry Point: Address set to 00400
Program Read-In Area: 00601 - 00680

AUTOCODER FIVE CARD LOADER

Store at 00247: M%1100257$..
Address set to: 00247
Start
Program Entry Point: Address set to 00281
Program Read-In Area: 00200 - 00279

To run 1410 Autocoder (AV-906) using tape PR-108 (assuming a standard I/O pool (20K, 1402, 1403, tape units 12, 13, 14, and 15)

Mount PR-108 on TU 2
Mount work tapes on TU 3, 4, and 5
Store at 00001 L%B200011$..
Computer reset and start

To Load Storage Print Program

Store at 00001 L%1100300$J00308b.
Computer reset and start

1401 LIST/PUNCH PROGRAM (SELF LOADING)

Mount tape on TU 11 (first record on tape must be the 1401 List/Punch program)
Store at 19000 L%U1001RB001.
Set compatibility switch to 1401
Address set to 19000
Start

Sense Switches

B	ON	Bypass printing
C	ON	Bypass punching condensed deck
D	ON	Bypass punching symbolic deck
E	ON	Writes out on tape 4

Accelerator

1. Memory cycle 4.0 usec.
2. Logic gate 0.677 used.
3. Cycle length for arithmetic operations:
   a. Stop at J changed to stop at F.
   b. Stop at K changed to stop at G.

SERIAL I/O CHASSIS DESIGNATIONS

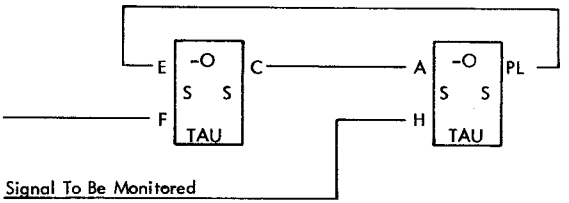
Chassis designations in the 1414 Models 4, 5, and 6 for the telegraph feature have been changed as follows:

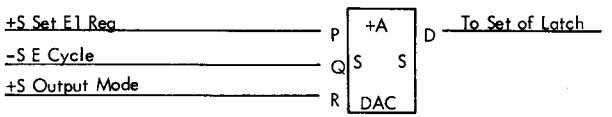
Feature	Old	New
TGL Basic (Send/Receive)	14CA	14L9
TGL Optional (Receive/Receive)	14CB	14R9
TGL Optional (Send/Send)	14CC	14S9

SIGNAL MONITORING

A circuit may be wired temporarily to monitor signals in the 1410 System by using spare circuits in the machine or by placing a circuit card in a blank socket. The signal to be monitored is wired to Pin H(See below).When the signal goes minus the latch will be set (Pin PL goes plus) and remains on until reset. The latch can be reset by touching a ground lead to Pin A. This circuit can be quite helpful in finding intermittent failures.

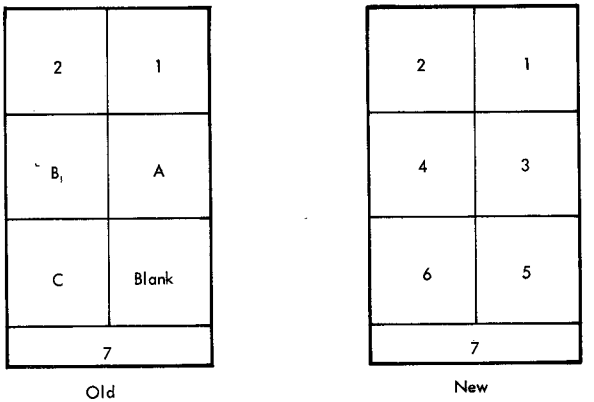
The signal to be monitored can also be gated by using another circuit to add conditions to the turn on of the monitoring latch (See below). For example, if the E1 Register is suspected of turning on at some time other than during an E cycle, the AND circuit in the Figure could be used to verify the fact. Note: If the signal to be monitored is a "Y" level (DEJ, DEK, etc.), cards with -A or +O logic should be used.



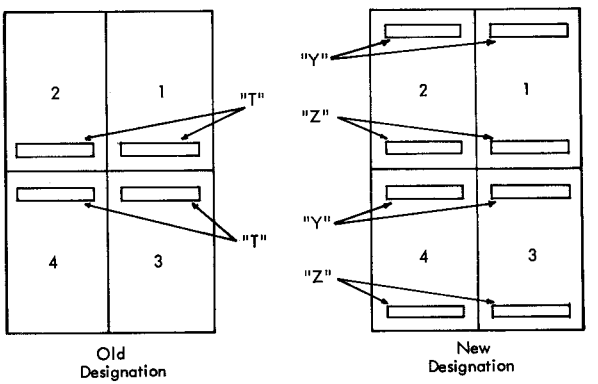


Signal Monitoring

PANEL DESIGNATION CHANGES

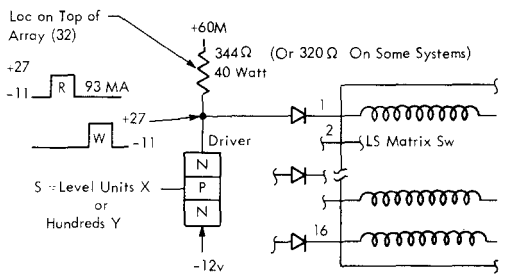


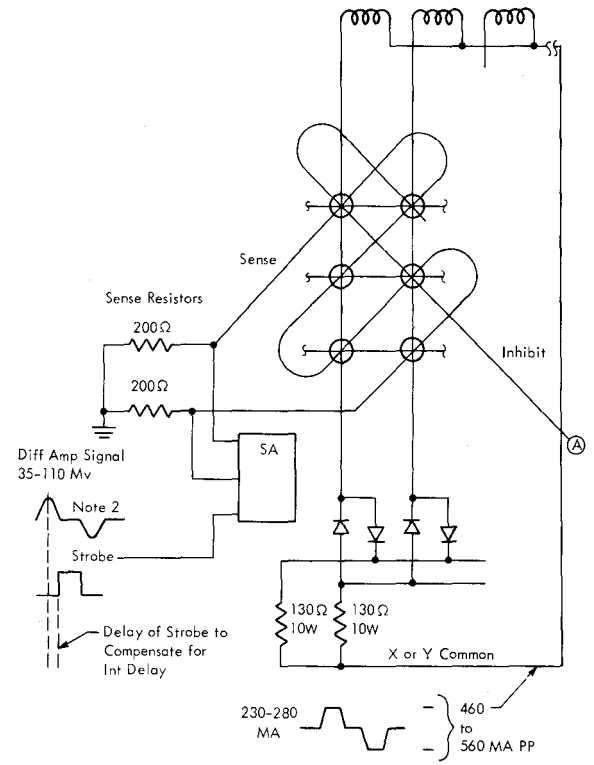
1414 Models 1 and 2 Panel Redesignation



1411 T Row Panel Designation Change

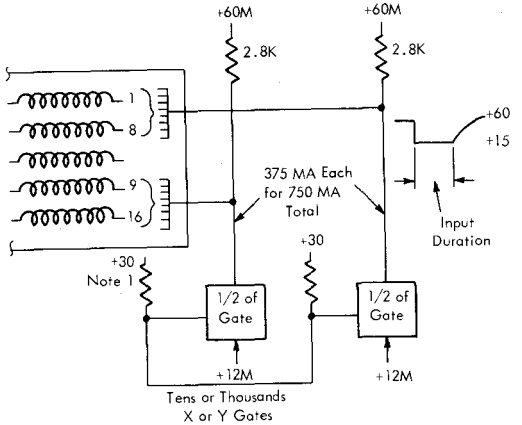
CORE STORAGE

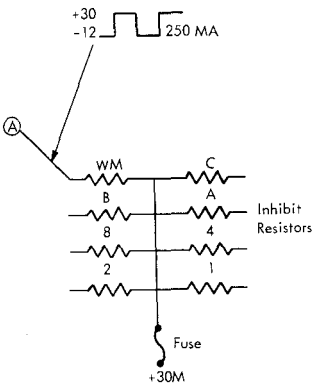




Note 1 +30 ± 2% at the Chassis
± 4% at the Power Supply

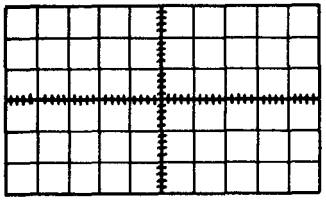
Note 2 Sense Output AVG 90 Mv, 35 Mv is a Borderline Condition

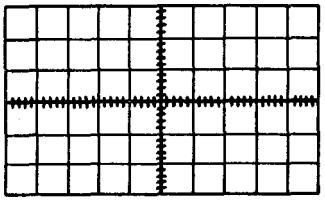


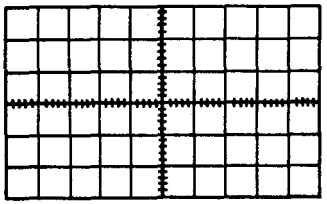


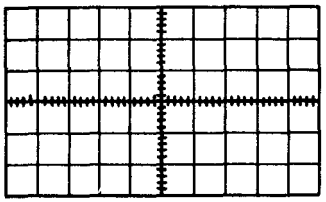
SCOPE NOTES

Use these reticules to save important or unusual pulses for future reference.









Notes

DETACH CARD ALONG PERFORATION

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Circle one of the comments and explain in the space provided:

Suggested Addition (page ___) Suggested Deletion (page ___) Error (page ___)

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