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IBM System/360 Model 25 Functional Characteristics

This reference publication augments the IBM System/360 Principles of Operation, Form A22-6821. It describes the relationship of the Model 25 to other System/360 models: system capabilities, system control panel, input/output channels and integrated I/O attachments, operations, instruction timings, and system features.

The reader should have a knowledge of the System/360 as defined in the IBM System/360 Principles of Operation. IBM publications relating to the Model 25 are IBM System/360 Model 25, 1401/1460 and 1440 Compatibility Features, Form A24-3512, and IBM System/360 Model 25 Configurator, Form A24-3511. Other literature applicable to the Model 25 is listed in the IBM System/360 Bibliography, Form A22-6822, and the IBM System Summary, Form A22-6810.



First Edition (January 1968)

Significant changes or additions to the specifications contained in this publication will be reported in subsequent revisions or Technical Newsletters.

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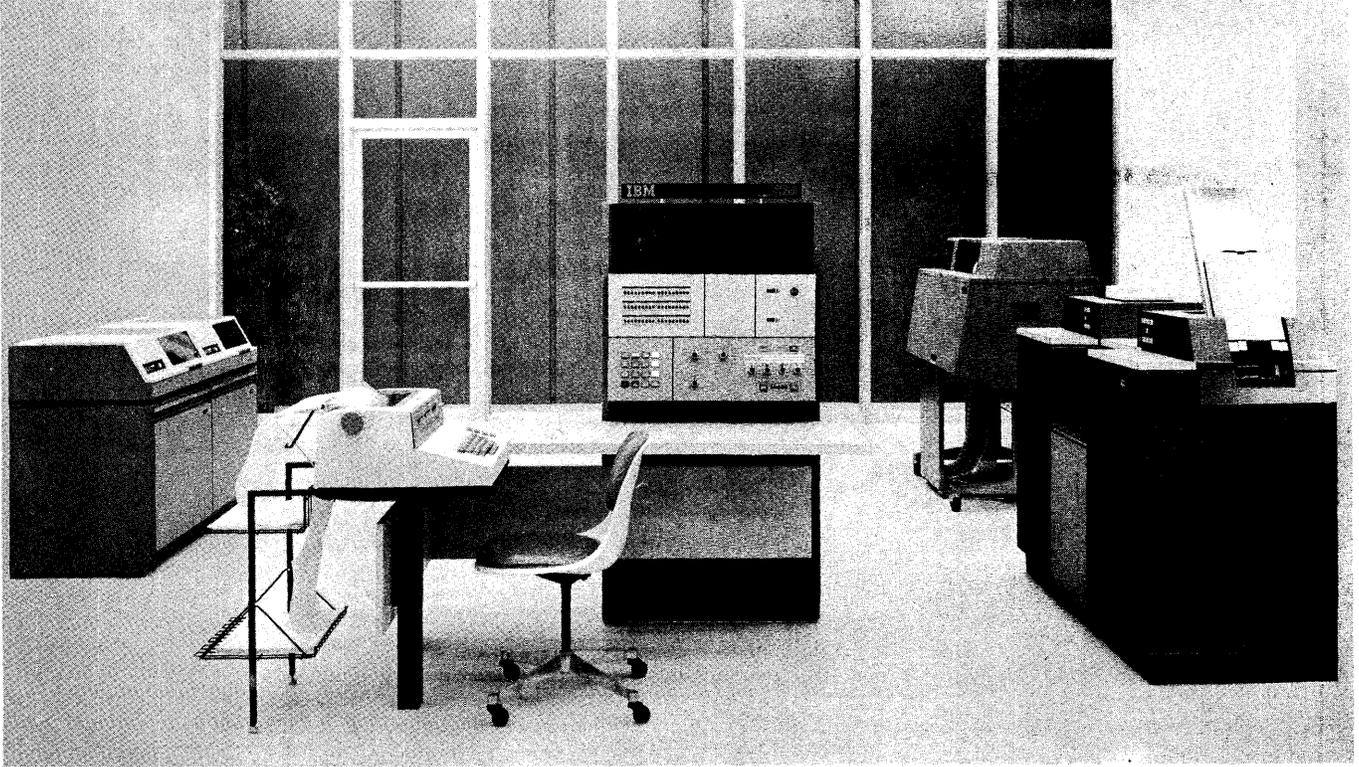


Figure 1. IBM System/360 Model 25

The various models and input/output configurations of the IBM System/360 series of data processing systems cover the entire range of commercial and scientific data handling requirements. Within the storage capacity, processing speed, and types of I/O devices that can be attached, compatibility is maintained throughout the System/360 line.

The operating performance of the System/360 Model 25 lies in a range between the Model 20 and the Model 30. Some overlapping of system capabilities (within the storage and input/output facilities of the Model 25) allows for expansion of your computing system to match your company's growth.

The console printer-keyboard, which is required on all models, provides for low-speed, low-volume input/output. Considerable job flexibility is provided with the integrated attachment features for the IBM 1403 Printer, IBM 2540 Card Read-Punch, and up to four IBM 2311 Disk Storage Drives. With program storage of 16K, 24K, 32K, or 48K, and the wide choice of I/O equipment that can be attached, the Model 25 provides data handling capabilities for diversified applications in virtually all data processing fields.

Several programming support systems are available for the Model 25. Refer to the IBM System/360 Bibliography, Form A22-6822, for abstracts of the IBM publications that apply to the Model 25.

Additional special and optional features are available for specialized tasks such as emulation of the IBM 1401, 1440, and 1460 data processing systems, program-controlled communications between CPU's, etc.

This publication is intended as a reference for users of the System/360 Model 25: only items that are unique to the Model 25 are discussed in detail. For this reason, a comprehensive knowledge of the System/360 series is necessary. This information can be found in the IBM System/360 Principles of Operation, Form A22-6821.

SYSTEM FEATURES

The System/360 Model 25 central processing unit (CPU) is available in four program-storage sizes.

<u>System/360 Model</u>	<u>Program-Storage Capacity</u>
D25	16,384 bytes (16K)
DC25	24,576 bytes (24K)
E25	32,768 bytes (32K)
ED25	49,152 bytes (48K)

Each model of the System/360 Model 25 is equipped with the following standard or required features.

- System Control Panel
- IBM 1052 Printer-Keyboards (Model 7)
- Standard Instruction Set (fixed-point operations)
- Commercial Instruction Set (decimal operations).

Optional and special features available for the Model 25, which are described in detail later in this publication and/or in the System/360 Principles of Operation, include:

- Scientific Instruction Set (floating-point operations)
- Universal Instruction Set (standard, commercial, and scientific instruction sets, plus the storage protection feature)
- 1403 Attachment Feature
- 2311 Attachment Feature
- 2540 Attachment Feature
- Multiplexer Channel (32 subchannels)
- Selector Channel
- 1401/1460 Compatibility
- 1440 Compatibility
- Direct Control
- External Interrupt
- Interval Timer
- Storage Protection

Some of these features are mutually exclusive: the installation of one precludes the use of another. This is the case, for example, with the multiplexer and selector channels. Some options require the presence of other features (i.e., storage protection feature is necessary for the universal instruction set). Still other features have subfeatures, etc. Information that clarifies these various features is in applicable sections of this publication. Also, refer to the IBM

System/360 Model 25 Configurator, Form A24-3511, for an overall view of system features. The IBM System/360 Input/Output Configurator, Form A22-6823, lists the control units and input/output devices that can be attached to the Model 25 through the multiplexer or selector channel interface.

INPUT/OUTPUT ATTACHMENTS

The System/360 Model 25 provides for integrated attachment of a group of commonly used I/O devices. An integrated attachment is an I/O control unit that is incorporated within the processing unit. It provides for the control and the data transfer for a specific I/O device.

These attachments do not connect to a standard I/O channel, but they are program-controlled as if they were. The devices are addressed using channel and device addresses, and they respond with the same status conditions.

System/360 input/output multiplexer or selector channel special features are also available to handle a wide range of additional I/O devices.

The following are the specific devices for which integrated attachments are provided. These features are described in detail in the Integrated I/O Characteristics section.

1. IBM 1052 Printer-Keyboard (Model 7): This device and its integrated attachment in the processing unit are required features on the Model 25.
2. IBM 1403 Model 2 or 7 Printer: The Model 2 provides a print line with 132 print positions; the Model 7 has 120 print positions. The maximum printing speed for the Model 2 is 750 lines per minute. The maximum printing rate for the Model 7 is 600 lines per minute. Refer to the Printing Speeds section for determination of various printing rates. The integrated attachment for this device is a special feature.
3. IBM 2311 Model 1 Disk Storage Drive: Up to four 2311s can be attached to the system through a single integrated attachment special feature.
4. IBM 2540 Model 1 Card Read-Punch: The card-reader portion of this device reads cards at a maximum rate of 1000 card per minute; the card punch operates at a maximum rate of 300 cards per minute. The integrated attachment for this device is a special feature.

The Console Printer-Keyboard, the 1403, the 2540 Reader, and the 2540 Punch are assigned to channel 0 and operate in multiplex mode. The 2311s are assigned to channel 1 and operate in burst mode as if on a selector channel.

Note: The console printer-keyboard and the integrated 1403 and 2540 attachment features are not attached via the multiplexer channel but appear to the program to be on this channel. The integrated 2311 attachment feature does not require a selector channel feature, although it appears to the program to be on the selector channel. Thus, the presence or absence of selector or multiplexer channel features is completely independent of the integrated I/O attachment features.

INPUT/OUTPUT CHANNEL

In addition to the integrated I/O devices, the Model 25 can also have a standard I/O interface channel for connecting additional I/O devices. The channel special feature may be installed as channel 0 and function as a multiplexer channel, or as channel 1 and function as a selector channel. The two types of channel cannot be installed simultaneously. With either type of channel installed, the integrated Console Printer-Keyboard, 1403, and 2540 are addressed as if they were on channel 0, and the integrated 2311s are addressed as if they were on channel 1. Up to eight control-unit positions are provided for connecting I/O devices on the installed channel. Either of the following maximum configurations is possible.

1. Channel 0 with eight control-unit positions, plus all of the integrated devices assigned to that channel, and the maximum of four 2311s attached to channel 1 through the integrated attachment.
2. Channel 1 with eight control-unit positions, plus a maximum of four 2311s connected to channel 1 through the integrated attachment, and all of the other integrated devices assigned to channel 0.

With the multiplexer channel, 32 unit control word positions (UCWs) are provided to address up to 152 devices: eight UCWs can address up to 16 devices each; 24 UCWs can address one I/O device each.

When the selector channel feature is installed, up to 256 I/O device addresses can be used.

Channel Interface

When the multiplexer or selector channel special feature is present, a standard I/O interface is provided for attaching a wide variety of I/O devices to System/360. The interface is a standard set of electrical connections through which signals are sent that allow for exchange of data and control information between the CPU and attached I/O devices. The interface is called standard because any present or future device can be attached to the system as long as it complies with the specifications of the interface.

Control of I/O functions, determined by instructions in the CPU program, and the transfer of data between CPU and I/O devices, are handled through channels. These channels coordinate the operation of I/O devices through program control.

The selector channel is usually used for high-speed data rate I/O devices because although operations are initiated by the CPU (which also reads data into or out of core storage), selector-channel data-transfer operations overlap CPU operations. CPU facilities are used for multiplexer Channel data-transfer operations.

The maximum data rate for either channel feature is 30,000 bytes per second (30KB).

Selector Channel

A selector channel is used to sustain operation of one device at a time. A variety of devices can be attached to a selector channel, but it is most useful when used with high-speed I/O devices.

Multiplexer Channel

The data-handling capability of the multiplexer channel is normally lower than that of the selector channel, although the multiplexer channel can handle nearly the same data rates of I/O devices attached to the selector channel when operating in burst mode. In this mode, the channel is temporarily assigned to a single device. The advantage of the multiplexer channel is that it can service the data flow and control requirements of several slow-speed I/O devices at one time. This kind of operation is accomplished in multiplex mode (sometimes called data interleaved mode). For example, the data sent from two serial

card readers to the CPU can be handled at one time in multiplex mode by the multiplexer channel.

IBM 2025 PROCESSING UNIT

The IBM 2025 Processing Unit (CPU) contains core storage and facilities necessary to perform arithmetic and logical processing of data and to control communications and data transfers between the CPU and external devices.

Major internal components of the 2025 processing unit are:

- Core Storage
- Local Storage
- Arithmetic-Logic Unit
- Addressing Registers
- Data Registers
- Error-Detection Circuits

Core Storage

Core Storage consists of three distinct areas: program storage, control storage, and auxiliary storage. Provisions are made to store or read out one or two bytes during a single storage access cycle. Although the core storage read/write cycle time is 900 nanoseconds, two cycles are required to read or store a byte or halfword (2 bytes) in either program or auxiliary storage. The first of these two cycles is necessary to obtain information needed to control the data access. Thus, the total time required per access is 1800 nanoseconds or 1.8 microseconds. This is not true, however, for sequential processing of microprogram steps in control storage. The address for the next control word to be executed is retained or appropriately updated as a function of the access. Therefore, the time necessary to read out a control word (2 bytes) is always 900 nanoseconds.

Program Storage: This area of core storage is accessible by the user's programs. It contains from 16,384 to 49,152 byte locations, depending upon the model. This storage is used to contain the instructions and data areas required for problem programs. These positions are addressed from location 0 up through the highest installed program storage address.

Certain locations of program storage are permanently assigned as follows to ensure program compatibility within System/360 as

described in System/360 Principles of Operation, Form A22-6821.

<u>Decimal Address</u>	<u>Length</u>	<u>Purpose</u>
0	Doubleword	Initial program-loading PSW
8	Doubleword	Initial program-loading CCW1
16	Doubleword	Initial program-loading CCW2
24	Doubleword	External old PSW
32	Doubleword	Supervisor-call old PSW
40	Doubleword	Program old PSW
48	Doubleword	Machine-check old PSW
56	Doubleword	Input/output old PSW
64	Doubleword	Channel-status word
72	Word	Channel-address word
76	Word	Not used
80	Word	Timer
84	Word	Not used
88	Doubleword	External new PSW
96	Doubleword	Supervisor-call new PSW
104	Doubleword	Program new PSW
112	Doubleword	Machine-check new PSW
120	Doubleword	Input/output new PSW
128-159	-----	Diagnostic scan-out area, beginning at address 128.

The remaining byte locations of program storage can be used for programming functions as outlined in the IBM System/360 Principles of Operation.

Control Storage: This core storage area is used exclusively to contain the microprogram routines necessary to interpret problem-program instructions, and to control all system functions for the mode of operation being executed. This area is reserved for control-program purposes and is not available to the problem programmer. Refer to the System Control section.

Auxiliary Storage: This core storage section is used for the general registers and floating-point registers, temporary work areas for various CPU functions, storage for unit control words (UCWs) for channel and I/O attachment features, etc. This area ranges from 2,048 to 4,096 bytes, depending upon the program-storage capacity of the system. Of these auxiliary-storage areas, only the general and floating-point registers are addressable by the problem program. As in other System/360 models, the 16 general registers have a capacity of one word (four bytes) each. The four

floating-point registers are doubleword registers.

Local Storage

The Model 25 utilizes a high-speed (180-nanosecond) unit for local storage. This system component is used for intermediate storage of the data being operated upon by the current control program step. It also holds addresses and other information required for internal processing and input/output operations. Generally, information is transferred from core storage, placed in local storage, used in some arithmetic, logic, or addressing function by the ALU or other data-flow component, and then returned to local storage. Depending upon the operation, the information may be retained in local storage, transferred back to core storage, or directed to an input/output device or some other point in the system data flow.

During the execution of microprogram (control-program) steps, local storage can accept or read out a byte of information as many as four times within the primary system cycle of 900 nanoseconds. A serial-by-byte capability permits the local storage to accept halfwords from core storage, and buffer the core-storage address into the ALU as specified by the microprogram step.

Arithmetic-Logic Unit (ALU)

The arithmetic-logic unit in the Model 25 is used to produce both arithmetic and logical combinations from input data from a variety of sources within the system. The data path through the ALU is one byte wide. The ALU inputs, the destination of the result, and the control of the ALU are determined by the control-program step being executed.

Associated with the ALU is an arithmetic modifier that effectively doubles the data width through the ALU circuitry for some operations.

Addressing Registers

Core storage (program, control, and auxiliary areas) are all accessed by a common set of storage-address registers. The address used depends upon the function being performed. In some instances, it is

derived from the contents of the preceding control word and the contents of an address-backup register. For other functions, the core-storage address is obtained from a local storage area. For sequential control-word processing, the core-storage address is developed from the address of the previous control-program step.

Because only the program storage section of core storage may be accessed directly by the programmer, and because the control-program area (and certain auxiliary-storage locations) must not be violated, provision is made to prevent inadvertent accesses to these areas.

Data Registers and External Facilities

Several special registers and other facilities that are external to local storage are used as sources and destinations for data and control information. These registers contain CPU status information, the settings of switches A, B, C, and D on the system control panel, status and data being transferred between the CPU and the channel or attachment devices, status and data associated with various special features, and similar data. These registers are not addressable by the problem programmer.

Error-Detection Circuitry

Tests are made for core-storage address validity, data parity (both within the CPU and during I/O data transfers), and other system malfunctions during system operation. Error-recovery microprogram routines included in the control program attempt to correct the error condition when this is possible. If the error-recovery attempt is unsuccessful, the system operation in progress is terminated. In many instances, the problem program or supervisor program also includes error-test routines, but these routines are application dependent and are not considered part of the computing system.

SYSTEM/360 MODEL 25 DATA FLOW

Figure 2 is a simplified schematic of the Model 25 data flow. The manner in which the various elements of the data flow are used for a given application depends upon the control-program step being executed.

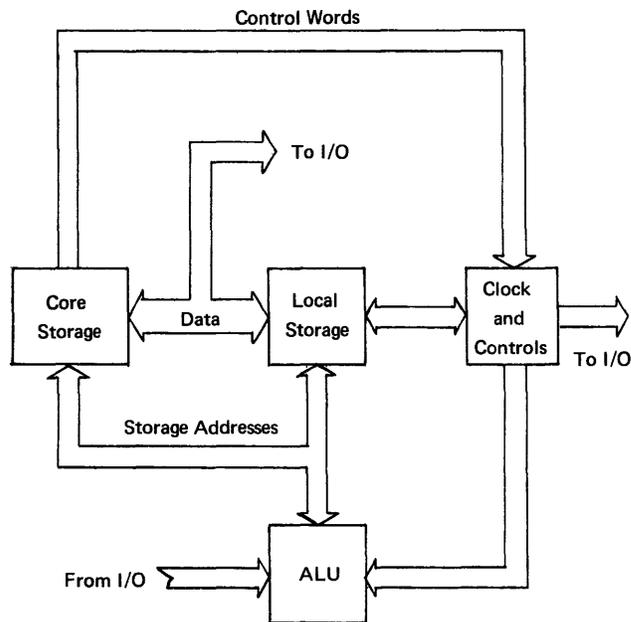


Figure 2. System/360 Model 25 Data Flow

SYSTEM CONTROL

As in other System/360 models, this system performs internal data manipulations and input/output operations by executing microprogram routines. In the Model 25, 16,384 bytes of core storage are reserved as microprogram (or control) storage. This section of core storage is standard on all models and is in addition to the program-storage area for a particular model. This area cannot be used for application-program purposes.

Control programs for the Model 25 can be easily reloaded into control storage (see the System Initialization section). These microprograms are prepared by IBM so that engineering changes can be implemented quickly and with minimum inconvenience to users of the Model 25. This also ensures problem-program compatibility between System/360 models within storage and input/output capabilities.

The control program for a mode of operation, System/360 mode for example, is especially written to:

1. Interpret problem-program instructions
2. Perform arithmetic and data-handling functions within the CPU
3. Initiate I/O operations and control any code translations required for the device
4. Handle data errors and other exceptional conditions

5. Perform other data manipulations required for efficient completion of the job.

Priority of System Operations

The Model 25 is designed to take advantage of the possibility of overlap between CPU operations and input/output functions. Also, the priority of operations within the CPU are ordered so that functions having the highest urgency are given the highest priority. This method of handling data and control requirements allows for maximum system throughput while reducing the likelihood of data overruns. (A data overrun is a condition where information is presented to the CPU from, for example, a magnetic tape unit, but because of other higher-priority system requirements, the information is lost.)

The highest priority (level 4) is given to the functions of System Reset, Initial Program Load (IPL), and Control Storage Load (CSL). These operations are allowed to immediately interrupt any other system function.

Priority level 3 is used for high-speed data transfers between the CPU and I/O devices attached to the channel, such as magnetic tape. This level is allowed to interrupt any operation having a lower priority.

Priority level 2 is reserved for data chaining operations for the integrated 2311 disk attachment feature.

Priority level 1 handles such medium-priority system functions as channel-status transfers and data chaining, and input/output transfers for the integrated 2540 attachment feature.

The lowest priority, level 0, is used to handle system operations that are either buffered or are not subject to data overruns. Among these are 1403 and 2540 status and chaining, and CPU instruction processing.

Because of the high data rate of the 2311 devices, a special share-cycle priority is assigned to handle data transfers between core storage and the integrated 2311 disk attachment feature. This priority is allowed to interrupt any other level of operation except level 4 (System Reset, IPL, or CSL). Each interruption to handle a byte of disk-file data requires only two cycles out of every

seven. This permits operation of a 2311 unit in conjunction with any I/O device attached to the channel (except magnetic tape or other high-speed unbuffered devices).

When the priority level assigned for a feature or operation is either not active or not included with the system (absence of the integrated 2311 attachment feature, for example), that level is bypassed.

The priority structure in the Model 25 is organized so that coincident or pending requests for status or data-handling service are queued: stacked up in order of their occurrence and/or significance until they can be accepted by the CPU.

MODEL-DEPENDENT IMPLEMENTATION OF SYSTEM/360 FUNCTIONS

The concept of compatibility between System/360 models is not applied for some detail functions. Neither the frequency of occurrence nor the usefulness of results warrants identical action on all models. These functions are concerned with the handling of invalid programs and machine malfunctions. They are identified in the System/360 Principles of Operation under Functions that may Differ Among Models. Wherever model dependency exists, the System/360 definition allows choice of implementation, or specifies that the outcome of the operation is unpredictable. The intent is that the user should ignore results that are defined to be unpredictable, and should not base his programs on any function where choice of implementation is permitted.

Considering any particular installation and operation, the results are not truly unpredictable: the action and result may depend upon system components or the input data.

However, writing a program based on the information contained in this section is in violation of the rules of compatibility of System/360. If the program depends on a function that is model-dependent, it may not produce the same results on another model of System/360. Even if a program allows for the model-dependent implementation of all other models, difficulties may be encountered if and when new System/360 models are introduced. Furthermore, a mandatory engineering change may in some instances require changes in a program that makes use of such model-dependent information.

The system control panel contains the switches, indicators, and other manual controls necessary for operation and control of the system. Other device-dependent controls are located on certain input/output units. The system control panel is made up of four sections (Figure 3).

1. Displays
2. Operator Control Section
3. Operator Intervention Section
4. Customer Engineering controls

The system is manually controlled with pushbutton switches and rotary switches. Two of the rotary switches control the mode of operation and check-control. Four hex-coded switches are used for addressing and for entering manual data. One rotary switch is used for diagnostic control.

INDICATORS OR DISPLAYS

Several indicators are available for displaying data and status information. The remaining lights are used as multipurpose indicators to display the Storage Address Register and other manually selected registers and locations.

Byte-0 and Byte-1 Indicators

The byte-0 and byte-1 indicators are used to display a variety of data and address information, depending on the operation in progress. Refer to the descriptions of the keys and switches on the system control panel.

Mode/Zone Register Indicators

Data Cycle, File: This light is on during a file-share cycle. This means a byte of information is being transferred between main storage and a 2311 device through the integrated 2311 disk attachment feature.

Bit 0: Indicates operation in 1400 emulator mode.

Bit 1: Not used.

Bits 2, 3, and 4: Show the current mode of operation for addressing incoming and outgoing external lines and registers.

Bits 5, 6, and 7: Indicate the bit structure that is decoded as the zone location for local-storage addressing.

CPU STATUS INDICATORS

Address Match: This light turns on when the address set up in switches A, B, C, and D matches the address being used to access core storage, and the Mode switch is in the SAR delayed stop position.

Alter/Display Printer-Keyboard (PR-KB): Turns on to indicate that the console printer-keyboard is executing an alter/display routine.

CSL: Pressing the CSL switch turns on this light and starts the control storage load (CSL) routine. The indicator resets when the control-program load routine is completed.

System Checks

PWR CHK (Power Check): Should any dc supply fall below its sensed output level (and/or circuit-breaker or thermal sensor trip), the machine sequences down to its normal power-off status and the power-check light turns on.

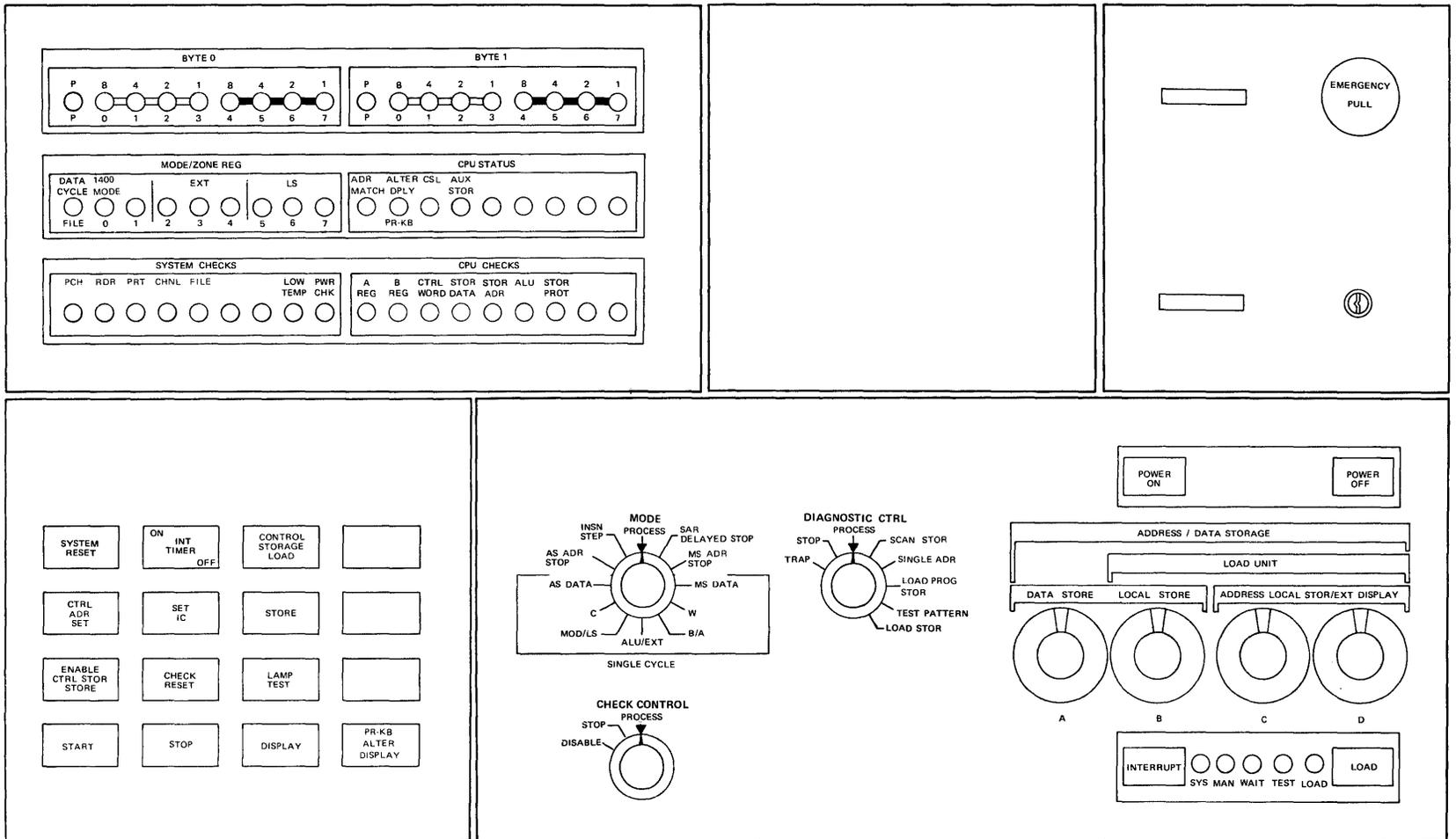
Power restart cannot be activated until the power-check light is reset by pressing the power-off switch and/or resetting the tripped circuit breaker or manually operating the thermal-reset switch.

PCH (Punch): Turns on for any punch condition in the integrated 2540 attachment feature that requires operator attention.

RDR (Reader): Turns on for any reader condition in the integrated 2540 attachment feature that requires operator attention.

CHNL (Channel): A microprogram-detected channel error or a bus-in parity error turns this light on.

Figure 3. System Control Panel



FILE: This indicates that an error has been detected during operation of a 2311 device through the integrated 2311 disk attachment feature.

LOW TEMP (Low Temperature): When power is turned on initially, this light comes on and remains on until the array is at proper operating temperature (about 2 minutes, depending upon room temperature). The purpose of this light is to indicate to the operator that the system is not yet up to optimum operating temperature.

CPU Checks

Parity Indicators: These lights, when on, indicate that incorrect parity was detected at the data-flow component named. The parity indicators are:

A REG	A-register
B REG	B-register
CTRL WORD	Control word
STOR DATA	Storage data
STOR ADDR	Storage address

ALU: Turns on when an error is detected in the arithmetic-logic unit (ALU) circuits during an ALU cycle. The ALU check is not a parity check but an actual bit check.

Storage Protect: Turns on to indicate that data read out of the storage-protect buffer had incorrect parity.

OPERATOR CONTROL SECTION

This section of the system control panel contains the controls required by the operator when the CPU is operating under control of the supervisor portion of the programming environment being used [Disk Operating System (DOS), Tape Operating System (TOS), etc.]. Under supervisor program control, a minimum of direct manual intervention is required because the supervisor program performs operations such as store and display.

The main functions provided by the operator control panel (OCP) are the control and indication of system status (wait, manual, etc.), operator-to-machine communication (primarily via the console printer-keyboard), and initial program loading.

The switches and indicators in the OCP section of the system control panel are present on all System/360 models. On the Model 25, they have the following functions.

Switches

Emergency-Pull Switch: Pulling this switch turns off all power beyond the primary power box except EPO (Emergency Power-Off) control voltage on every unit that is part of the system or that can be switched onto the system. Therefore, the switch controls the system proper and all off-line and shared control units and I/O devices. The contents of core storage can be affected when this switch is operated.

The switch latches in the out position and can be restored to its in position by maintenance personnel only.

When the emergency-pull switch is in the out position, the power-on key is ineffective.

Power-On Key: This key is pressed to initiate the power-on sequence of the system.

As part of the power-on sequence, the system is reset in such a manner that the system performs no instructions or I/O operations until explicitly directed. The contents of core storage are preserved.

The power-on key is backlighted to indicate when the power-on sequence is completed. The key is effective only when the emergency pull switch is in.

If the power-on light glows pink, the power-on sequence for the system cannot be completed because of a malfunction in a power supply or an I/O device.

Power-Off Key: The power-off key is pressed to initiate the power-off sequence of the system.

The contents of core storage are preserved. The key is effective only while power is on the system, and it overrides the power-on key.

Interrupt Key: The interruption key is pressed to request an external interruption.

The interruption is taken when not masked off and when the CPU is not in the stopped state. Otherwise, the interruption request remains pending. Bit 25 in the interruption-code portion of the current PSW is made 1 to indicate that the interrupt key is the source of the external interruption. The key is effective only while power is on the system.

Load Key: The load key is pressed to start initial program loading. The key is

effective only while power is on the system.

When the load key is operated, the following functions occur.

1. An automatic system reset is performed.
2. The CPU clock is started.
3. The basic test microprogram is performed.
4. The clear UCW microprogram is run to reset all the flag bytes in the UCW area of auxiliary storage.
5. The load microprogram is begun. This routine analyzes switches B, C, and D to determine the address of the program-loading I/O device (load-unit address). When this routine is completed, the Initial Program Load (IPL) PSW has been successfully set up, and the load light is turned off.

Note that the system mask is reset when the load key is pressed. The system mask in the IPL PSW is then effective as soon as the IPL PSW is set up.

The load key does not change the system operating mode already determined by the CSL function and the contents of control storage.

Load Unit Switches: Three rotary switches (B, C, and D) provide the I/O address bits used for initial program loading (see Figure 4).

All three are 16-position rotary switches labeled with the hexadecimal characters 0-F. The channel address (0 or 1) is loaded from switch B, and the unit addresses from switches C and D.

These switches have other functions, as described under Operator Intervention Section.

Indicators

System: This indicator is on whenever the customer or CE use-meter is recording time.

Manual: Whenever the CPU clock is stopped or the CPU is in a soft-stop loop, this indicator is on. The soft-stop loop is a microprogram routine used to handle all exceptional conditions and interruptions in the CPU. The first time through the loop, all pending interruptions are handled. After this, only the integrated I/O devices, the interval timer, instruction step, and certain console functions are handled. Pressing the stop key is one way to enter the soft-stop loop.

Wait: This light is on when the CPU is in the wait state (i.e., CPU clock is running but instruction execution is not taking place). If an interruption occurs, the CPU is taken out of the wait state and processing occurs, depending on the program being executed.

Test: This light is on when either the mode switch, the diagnostic-control switch, or the check-control switch is not in the process position.

Load: Whenever an initial program load (IPL) microprogram is in progress, this indicator is on. It turns on after the load key has been pressed and released, and turns off when the initial PSW is successfully loaded.

OPERATOR INTERVENTION SECTION

This section of the system control panel contains the controls required for the operator to intervene in normal programmed operation.

Many of these keys are described as being intended for customer engineering use only. Indiscriminate operation of these controls will seriously affect or terminate the problem-program application in progress.

Pushbutton Keys

System Reset Key: This key resets the CPU clock and the various registers and controls in the CPU and I/O units necessary to prepare the system for another job. In addition, a system-reset microprogram is initiated when the CPU clock is started upon release of the switch.

It is not necessary to press this key when the load key is operated because the load key also initiates a system reset.

Control Address Set Key: This key is effective only when the CPU clock is stopped. When the switch is pressed, the contents of the four address switches (A, B, C, and D) are used as the address for the next storage-access cycle. For 16K systems, this address is from 4000-7FFF (switch-A positions 4-7); for 24K or 32K systems, this address is 8000-BFFF (switch-A set to 8-B); and for 48K systems, it is C000-FFFF (switch-A positions C-F). This key is for customer engineer use only.

Enable Control Storage Store Key: This key must be pressed and held during a store into the control-storage area of core storage (refer to Store Operation). The store operation is successfully completed when the new data is displayed in the byte-0 and byte-1 indicators. This key is for customer engineering use only.

Start Key: Pressing the start key generates a clock-start signal to start the machine. The processor continues to operate in the mode selected by the setting of the mode switch.

CSL key: Pressing this key causes a system reset, and initiates a microprogram used to load the control-storage and auxiliary storage areas of core storage with new information to change system operating modes (from System/360 mode to 1400 emulator mode). The data source for a CSL function is the input device specified by switches A, B, C, and D. The CSL light (CPU status) is on while in the CSL routine, and is reset upon CSL completion. Refer to the System Initialization section for further information.

Set IC Key: This switch is effective when the CPU is in either a soft-stop or a hard-stop state. The Set-IC (instruction counter) key causes a branch to the soft-stop routine that gates the contents of switches A, B, C, and D into the instruction counters. This address must be valid for the installed program storage area. At the end of the Set-IC routine, the system enters a soft-stop state.

Check Reset Key: Pressing this button resets the check latches in the processing unit to the no-error state.

Stop Key: Pressing the stop key with the system in process mode causes a branch into the soft-stop routine at the end of the current instruction, and turns on the manual light.

When this key is pressed, the system enters the stopped state when:

1. The instruction being processed has been completed,
2. All pending interruptions have been serviced, and

3. Any I/O operation in progress has been finished.

Note: Any time the system enters the soft-stopped state (such as when the stop key is pressed), the hexadecimal address for the next System/360 instruction (problem program instruction) is printed on the console printer-keyboard. This notation is also printed when the system-reset key is pressed. This provides a permanent record of each occurrence of a stop.

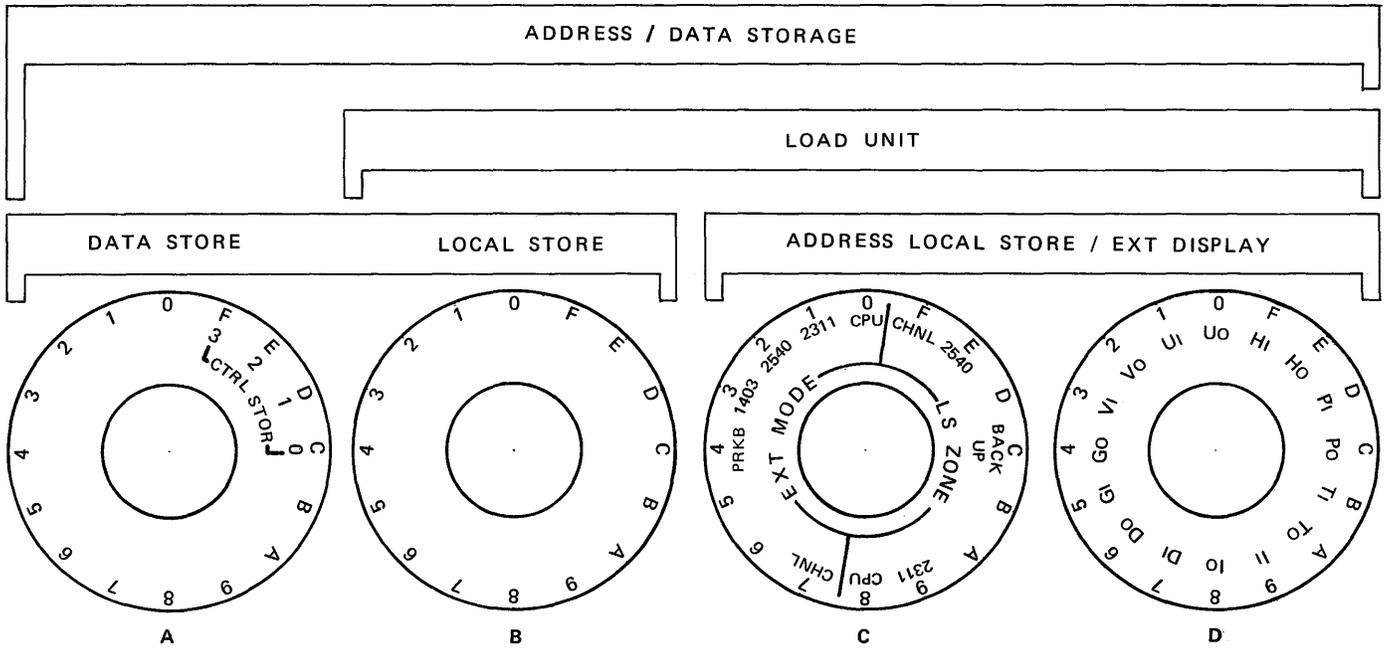
If data or command chaining is involved, it is completed before the CPU clock is stopped. The system light stays on as long as any I/O unit is engaged in an I/O operation; that is, until device-end is accepted for the last command in a chain for that I/O device.

Note that the machine environment is not destroyed when the stop key is pressed, and the program that was in progress can be restarted (by pressing the start key). The address of the next instruction is displayed in the byte-0 and byte-1 indicators.

When the system is stopped by pressing the stop key, the multiplexer channel is allowed to accept share-request traps (microprogram branches), and the selector channel is allowed to accept data cycles. This provision permits input-terminal and multisystem operations even though the 2025 program in progress has been manually interrupted.

Interval Timer Switch: This switch is present only if the interval-timer feature is installed. The switch activates the interval timer.

Display Key: This key is operative only when the CPU is in the stopped state. When the mode switch is in the MS-data or AS-data position, the display pushbutton causes the address in switches A, B, C, and D to access storage, read out the two data bytes, and display them in the byte-0 and byte-1 display indicators. The halfword accessed is then available on the core-storage bus-out lines (R0 and R1). R0 displays in byte-0 and R1 in byte-1. Refer to the Mode Switch and Console Procedures sections for a detailed description of display operations.



Switch A For 16K Systems



Switch A for 24K and 32K Systems

Note:
 The Full View of Switch A Shows Control Storage Positions For 48K Systems,
 The Partial Views of Switch A Are Used For 16K, 24K, and 32K Systems.

Figure 4. Control Panel Switches A, B, C, and D

Lamp Test Key: When this key is pressed, all console indicators (except PWR CHK and LOW TEMP) should light. The lamp-test key can be pressed at any time with no effect on system operation.

Store Key: Any core storage or local storage location can be altered from the console. The store switch is effective when the mode-control switch is in any of three positions:

- MS Data
- AS Data
- Mod/LS

The detailed store operation is described in the Mode Switch and Console Procedures sections.

PR-KB Alter/Display Key: Pressing this key causes a console printer-keyboard request. When the request is honored, the console printer-keyboard unlocks, the PR-KB alter/display indicator and the proceed light turn on. The console printer-keyboard is then used for alter/display. (See Manual Alter/Display.)

Address/Data Switches

These four switches (A, B, C, and D) are used to address a location in any storage area and can be manipulated without disrupting CPU operation (Figure 4). For specific functions, they specify the data to be stored in the location designated by the mode switch. Refer to Mode Switch and Console Procedures for more information.

CUSTOMER ENGINEERING CONTROLS

The Mode switch, Check Control Switch, and the Diagnostic Control switch are intended primarily for customer engineering use. When processing problem programs, these switches should all be set to the Process position.

MODE SWITCH

The mode of system operation is controlled by the setting of this switch. The positions of the switch put the machine into either an operating mode or a single-cycle mode.

Operating Mode Positions

MS Address Stop: The machine is in a normal operating mode. When the address in switches A, B, C, D matches the address of the core-storage location being accessed, the machine stops at the completion of the microword in progress. The address-match indicator is turned on. The byte-0 and byte-1 indicators display the address of the next microprogram step to be executed. The match occurs for addresses that specify either program or control storage.

Process: This is the normal operating position for the system. If the clock stops with the switch in this position, byte-0 and byte-1 display the contents of the storage-address register.

Instruction Step: In this position, the machine performs one instruction for each operation of the start button. At the conclusion of the instruction, the machine goes to a soft-stop routine. In single-instruction operation, the console printer-keyboard prints out the next instruction address after each instruction is executed. If the clock stops (for some other reason) with the switch in this position, the storage address register is displayed in byte 0 and byte 1. Except for a machine check, I/O overruns do not occur when the switch is in this position.

AS-Address Stop: The machine is in normal operating mode. When the address in switches A, C, and D matches the auxiliary-storage address present in bits 0-3 and 8-15 of the storage-address register (M0-register bits 0-3 and M1-register bits 0-7), the machine stops at the completion of the microword in progress. The address-match indicator is turned on. The byte-0 and byte-1 indicators display the address of the next microprogram step to be executed. The auxiliary-storage area of core storage is addressed by the four high-order bits and the eight low-order bits of the storage-address register; the second of the four normal hexadecimal digits is not relevant.

SAR Delayed Stop: At this switch setting, the machine operates normally in run mode until the address in switches A, B, C, D compares to the address in the storage-address register. The machine completes the macro instruction in progress. It then goes to a soft-stop routine, similar to single-cycle and/or instruction-step operation. The address-match indicator turns on. If the clock stops with the switch in this position, the storage-address register is

displayed in the byte-0 and byte-1 indicators

The mode switch can be switched between these first five positions during system operation, with no effect on normal machine operation except as described for the switch settings.

Single-Cycle Mode Positions

When the mode switch is in any of the remaining positions, pressing the start key causes the CPU to operate for only one cycle (overruns occur for operations involving nonbuffered devices). During this cycle, the CPU performs the function specified by the control word being executed. At the end of the cycle, the display in byte-0 and byte-1 is the storage-address register, except for the alter/display storage and auxiliary-storage positions.

Alter/Display Functions, Mode Switch: The store pushbutton is effective only when the mode switch is in one of the following positions (see Store Operation).

- MS Data
- AS Data
- MOD/LS

The display pushbutton is effective only when the mode switch is in one of the following single-cycle positions (see Display Operation).

- W
- B/A
- C
- ALU/EXT
- MOD/LS
- AS Data
- MS Data.

All of the preceding single-cycle positions except AS-data and MS-data display the storage-address register in the byte-0 and byte-1 indicators unless the display key is pressed. When the display key is held pressed, the byte-0 and byte-1 indicators display the contents of the data-flow component addressed by the Mode switch, as follows.

Mode Switch Position	Operations Information Displayed	Operations Possible
W	Storage-address back-up registers (W0 and W1 registers)	Single cycle or display

C	Contents of the control-word register (C0 and C1 registers)	Single cycle or display
B/A	B-register and A-register (components that feed the ALU)	Single cycle or display
MOD/LS	ALU modifier and the byte of local storage, selected by switches C, D	Single cycle, store, or display
ALU/EXT	Output of the arithmetic/logic unit, the external location selected by switches C, D.	Single cycle or display

Note: These functions are more fully detailed in the Console Procedures section.

CHECK-CONTROL SWITCH

This 3-position rotary switch provides a stop-on-error function for the CPU. It is used for customer engineering purposes. The switch positions and the action taken are as follows.

Switch Position	Action
Process	This is the normal operating position.
Disable	In this position, all machine checks are ignored, but the appropriate check latch is set.
Stop	A machine check detected while the switch is in this position causes a hard stop (clock stop) at the completion of the control word in progress.

DIAGNOSTIC CONTROL SWITCH

Process: This is the normal position when the machine is operating, or when no scan-diagnostic functions are being performed. When the switch is taken out of the Process position, the system is put into a test status.

Scan and Load Positions

The circuitry scan and load operations are started by pressing System Reset, then Start. This starts the scan or load operation at address 0000. The scan continues until the system-reset key is pressed, or the diagnostic control switch is moved to the single-cycle position. If the scan or load operation is to be started at an address other than 0000, switches A, B, C, and D are set to the desired address. Pressing control-address set key places the address into the storage-address register. Pressing the start key initiates a clock-start, and the operation continues until terminated as indicated.

Scan Storage: Every position of storage is read and regenerated in sequence. A parity error on storage data or a storage address causes a hard stop. The check-control switch must be in the stop position.

Load Program Storage: The data in switches A, B, C, and D is loaded into every position of program storage. When the control storage area is addressed, the locations are accessed in sequence, but the store lines are not activated. A storage scan should follow the load program to determine if the data is stored properly.

Single Address: When the switch is in this position, the storage address specified by switches A, B, C, and D (set into the storage-address register by the control-address set key) is used each cycle to address a single storage location. As with the other scan or load positions of this switch, the start key must be pressed to initiate the function.

Test Pattern: A test pattern of 1's and 0's is loaded into every position of program, auxiliary, and control storage (except the CSL area). The program continues to loop until the system-reset key is pressed.

Load Storage: Operation with the switch in this position is similar to Load Program Storage except that program, control, and auxiliary storage are loaded from the contents of switches A, B, C, and D. The CSL area is not affected.

Stop: This position is used by the Customer Engineer for diagnostic purposes.

Trap: This position is used by the Customer Engineer for diagnostic purposes.

USE METER (CPU)

The 2025 system control panel has two separate meters that record time whenever the system is in operation (i.e., initiating, executing, or completing instructions or commands, including those to I/O or assignable units). The position of a key switch determines whether the customer meter or the customer engineering (CE) meter operates. The Customer Engineer sets this switch to cause the CE meter to record time spent during system maintenance.

The system light is on when the system is in operation. It indicates that one of the CPU meters is running. When the stop key is pressed, this light stays on (and the CPU meter continues recording elapsed time) until any previously initiated operation involving an I/O or assignable unit has been completed; that is, until device-end occurs for the last command in a chain for that device. Thus, the CPU customer meter stops (as do other use meters that depend upon it) when there are no further operations in progress, or after the system has been stopped.

The CPU use meter operates for a minimum of approximately one second each time it is started.

CONSOLE PROCEDURES

Display Operations

Any core-storage location can be displayed from the system control panel. Several address and data registers can also be displayed. The position of the Mode switch specifies the source of the information to be displayed, as follows.

MS Data	Core storage (program storage or control storage, depending upon the address being used)
AS Data	Auxiliary storage
C	C-register (control register)
MOD/LS	Arithmetic modifier and local storage
ALU/EXT	Arithmetic-logic unit and external facilities
B/A	B-register and A-register (the inputs to ALU and core storage)
W	W-register (storage-address register backup register)

Only those data-flow components the user may need to display are discussed in this section. Other functions of the Mode switch (C, B/A, and W) are used by the Customer Engineer.

Display Program Storage: Set the Mode switch to the MS-Data position. Set switches A, B, C, and D to the program-storage address to be displayed: for 16K systems, this address is from hexadecimal 0000 through 3FFF; for 24K systems, this is 0000-5FFF; for 32K systems, use 0000 through 7FFF; and for 48K systems, use 0000-BFFF. When the display key is pressed, the addressed halfword is displayed in the byte-0 and byte-1 indicators.

Display Control Storage: This procedure is identical to the display of program storage except that switches A, B, C, and D are used to address a control-storage location. For 16K systems, this is hexadecimal 4000-7FFF; for 24K or 32K systems, use 8000-BFFF; and for 48K systems, use C000 through FFFF.

The procedure for displaying control storage is intended for customer engineering use only.

Display Auxiliary Storage: Set the Mode switch to the AS-Data position. Set switches A, C, and D to the auxiliary storage address to be displayed (switch B is not used). This address is from 0x00 through 7xFF for 16K systems; 0x00-BxFF for 24K or 32K systems; and 0x00-FxFF for 48K systems.

Normally, only the general and floating-point registers, and the MPX UCW areas of auxiliary storage, can be displayed by the user. These areas are shown in Appendix A.

Local Storage Alter/Display

To perform either of these operations, the mode-control switch must be set to the modifier/alter-display local-store position (MOD/LS).

Any position in local storage can be displayed and/or altered from the system control panel. The location to be accessed is selected by switches C and D. Switches A and B supply the byte of data for an alter-local-store operation. The multiple labeling on the knob of switch C is to enable selection of core-storage addresses, local-storage zones, or the external-mode address for the various manual operations. Multiple labeling on the switch-D knob is for selection of bytes U0, U1, V0, V1, etc. in local storage.

Switch C, bits 1, 2, and 3, supplies three bits for zone selection that are the equivalent of mode-register bits 5, 6, and 7. These are gated into the mode-register bit circuits.

Switch D, bits 0, 1, 2, and 3, supplies the bits that are decoded to select the actual byte.

Display Local Storage: After switches C (zone) and D (byte) have been set to select the desired local-storage location, and the Mode switch is set to the MOD/LS position, press the display key. The byte-0 lights indicate the contents of the arithmetic modifier, and the byte-1 indicators show the contents of the addressed LS location.

Store Local Storage: Set the mode switch to the MOD/LS position. Set switches C (zone) and D (byte) for the desired local-storage location. Set switches A and

B to the new data to be entered. The newly entered information is displayed in the byte-1 indicators. (The arithmetic modifier cannot be altered.)

Note: Except for customer engineering diagnostic purposes, the contents of local storage must not be disturbed.

ALU/External Display

The data displayed in byte-0 and byte-1 is the M0 and M1 registers whenever the mode switch is turned to this position, or when single-cycling the machine in this mode.

During the operation of the display switch, the ALU output is gated through the LS assembler and is displayed in the byte-0 indicators. The byte-1 indicators display the contents of the external address specified by switches C and D.

Switch C, bits 1, 2, and 3, correspond to the information normally set up in the mode-zone register in positions 2, 3, and 4. Switch D, bits 0-3, are decoded for actual byte addressing within any mode.

The store switch is ineffective in this mode position. Upon release of the display switch, byte-0 and byte-1 indicators again display the M0 and M1 register.

Store Operations

Information can be manually stored into any core-storage location. A halfword (two bytes) is always affected. If a single byte is to be changed, the remainder of the halfword must be reentered. Information can be stored in the program or auxiliary-storage areas by using the procedure given in the following. If a change is to be made to the control-storage section of core storage (for customer engineering use only), the Enable Control Storage Store key must be held pressed during the store operation. The store operation must be preceded by a display operation of the location to be altered.

It is advisable to display any location (in which data is manually stored) so that the store operation can be verified.

Program-Storage Store Operation: To alter the contents of a halfword in the program-storage area:

1. Set the Mode switch to MS-Data
2. Turn switches A, B, C, and D to the

location to be altered.

3. Press the display key. The byte-0 and byte-1 indicators show the present contents of this halfword location.
4. Set the data halfword into switches A, B, C, and D. If only part of the halfword is to be changed, the unchanged portion must be included as part of the two bytes.
5. Press the store key. The byte-0 and byte-1 lights indicate the new information that has been entered into the location specified in Step 2.
6. Steps 2 through 5 must be repeated for each halfword to be changed.

Auxiliary-Storage Store Operation: The procedure to alter auxiliary storage is similar to the steps given in the Program-Storage Store Operation section. A halfword in auxiliary storage can be altered as follows.

1. Set the Mode switch to AS-Data.
2. Set switches A, C, and D (switch B is not used) to the address of the location.
3. Press the display key.
4. Enter the new data into switches A, B, C, and D.
5. Press the store key.
6. Steps 2 through 5 must be repeated for each halfword to be changed.

Note: Except for changes to the general and floating-point registers, and customer engineering diagnostic purposes, the auxiliary-storage area must remain undisturbed after it has been initialized using the control storage load (CSL) procedure.

Control Storage Store Operation: Control storage can be altered as shown for program storage, except that the Enable Control Storage Store key must be held while the Store key is pressed.

Note: Except for customer engineering diagnostic purposes, the control storage area must remain undisturbed after it has been initialized using the control storage load (CSL) procedure.

SYSTEM INITIALIZATION

There are two classes of initialization for the Model 25. First, control storage load initialization is required when modes of operation are changed (System/360 mode to 1400 emulator mode). This is called Control Storage Load (CSL). The second type of

initialization is Initial Program Load (IPL), used to prepare the system for another job in the current system operating mode.

Control Storage Load (CSL)

All Model 25 computing and input/output operations are controlled by microprogram routines stored in the control-storage area of core storage. Whenever system maintenance is performed (depending upon the cause and service steps involved), the system should be reinitialized by using the CSL procedure. Similarly, when operating modes are changed, the CSL procedure must be used.

A small portion of control storage is reserved for a routine to read control-program and auxiliary-storage information from an input device. If this special microprogram is disturbed, a limited amount of manual data must be entered by the Customer Engineer. Then, the normal CSL procedure can be used to complete system initialization.

CSL for System/360 Mode (Using Integrated 2540): When the system has been initialized to 1400 mode, the following procedure is used.

1. Press the system reset key.
2. Set switches A and B to 0.
3. Set switches C and D to the 2540 reader unit address.
4. Press the Control Storage Load (CSL) key.
5. Place the CSL card deck in the 2540 reader and press the reader start key. The CSL indicator remains on until the CSL routine is completed.

CSL for System/360 Mode (Using a Channel Input Device): If the CSL records are located on a device attached to the

multiplexer or selector channel, the following procedure is used.

1. Set switch A to 0.
2. Set Switch B to 2.
3. Set switches C and D to the unit address of the channel input device being used.
4. Place the CSL records (cards, tape, etc.) in the input device, and make the device ready.
5. Press the CSL key. The CSL indicator remains on until the CSL routine is completed.

CSL for 1400 Emulator Mode: This procedure is given in the System/360 Model 25, 1401/1460 and 1440 Compatibility Features publication, Form A24-3512.

Initial Program Load (IPL)

This procedure is used after a successful CSL operation. Initial program loading is discussed in detail in the System/360 Principles of Operation. The step-by-step method of starting system operation is given here for the Model 25.

1. Set switches A, B, C, and D to the hexadecimal representation of the unit address for the input device.
2. Place the object-program records (disk, cards, etc.) in the input device, and make the device ready.
3. Press the IPL key.

An automatic system reset is generated as a function of the IPL operation. After the object program has been entered into core storage, system operation is under control of the application being executed.

This section describes the function and operation of the special and optional features that are available for this system. Features are also shown on the IBM System/360 Model 25 Configurator, Form A24-3511. Consult the IBM System/360 Principles of Operation for uses and programming considerations of these special features.

Because of the complexity of some major special features, they are described in separate sections.

INSTRUCTION SETS

The standard and commercial instruction sets are provided on all models to perform fixed-point and decimal arithmetic operations. Refer to the IBM System/360 Principles of Operation for a description of the various instructions.

Scientific Instruction Set

This feature provides 44 additional instructions used for floating-point calculations. With this feature, the four floating-point registers in auxiliary storage can be accessed.

Universal Instruction Set

When the standard, commercial, and scientific instruction set features are combined with the storage protection feature, the universal instruction set is obtained. The storage protection feature provides two additional instructions.

DIRECT CONTROL

Control of a variety of special equipment (including another processing unit or non-IBM devices) is possible with this feature. Two instructions: Read Direct and Write Direct, and six distinct interruption lines are included with this feature.

Direct control is used to pass controlling and synchronizing information between the CPU and special external devices. Data transfers are normally handled over the multiplexer or selector channel facilities.

If this feature is installed, the external interruption special feature cannot be installed.

EXTERNAL INTERRUPTION

This feature provides fast program response for time-dependent operations for which the data-transfer function is already provided. This feature has six distinct interruption lines.

If the direct control feature is installed, this feature cannot be installed.

INTERVAL TIMER

This feature provides the ability to decrement a program-controlled count at a fixed rate. Automatic program interruption occurs when the count passes from positive to negative through zero.

A value placed in a fixed core-storage location by the programmer is decremented by one, 300 times per second. When the value goes from positive to negative, a timer interruption occurs. For example, for a hex value of 004650 (18,000 in decimal), an interval timer interruption occurs at the end of one minute of CPU running time ($18,000/300 = 60$ seconds).

The storage locations used to store the value to be decremented are at hex address 50-53, although the Model 25 (consistent with other System/360 models) uses only the high-order 24 bits of this word (hex locations 50-52). The maximum interval timer cycle is 15.5 hours. Because the ac line frequency is used as the basis for the decrement, timer accuracy resolution is 16.66ms for 60 Hz systems (20ms for 50Hz systems).

This feature can be used for job accounting by measuring the duration of time for each job, for an interruption to

prevent a runaway job from gaining control of the system, for time stamping, and for polling particular operations on a regular basis (for example, every minute, every half hour, etc.).

STORAGE PROTECTION

This feature provides the facility to protect against inadvertent alteration to blocks of 2,048 bytes of storage specified by the programmer. With this feature, a programmed protection key prevents writing data into a protected area of core storage, thereby preventing one program from destroying another. Protection against reading data from an input/output device

into a protected area is also provided. This applies to channel operations as well as to operations involving the integrated I/O attachment features. Protection keys and patterns are established in the supervisor mode.

Storage protection is not effective for manual display and alter functions initiated from the system control panel.

Fetch protection (against undesired accesses to core storage) is not available on the Model 25.

The two additional instructions provided with this feature are Set Storage Key and Insert Storage Key. These instructions are used to assign and inspect the keys, respectively.

INTEGRATED INPUT/OUTPUT CHARACTERISTICS

The Console Printer-Keyboard, the 1403, the 2540 Reader, and the 2540 Punch attached through their integrated attachments can operate in overlap or time-share fashion with each other and with devices attached through the standard interface on channel 0. At the same time one of the 2311s attached through the integrated attachment on channel 1 can be operating. If the standard I/O interface is assigned to channel 1, one of the 2311s or one of the devices attached to the standard interface can operate with the integrated devices on channel 0. (The limitation with channel 1 is due to its function as a selector channel.)

INTEGRATED DEVICE ADDRESSING

Each I/O device connected to the system must have an address that is unique to the device. The same address must not be assigned to more than one device and the device cannot respond to more than one address. Sixteen bits of the address

developed from the I/O instruction define address of the device as four hex digits. The high-order eight bits define the channel (00 and 01 hex define channels 0 and 1, respectively, for the Model 25). The remaining two hex digits define the device address. On channel 0, the integrated devices may be assigned addresses from 00 to FF.

For purposes of System/360 standardization, the integrated devices are assigned addresses at the factory but these may be changed by the Customer Engineer when required. These addresses are defined under the respective device headings.

The addressing for the integrated attachment 2311s on channel 1 is limited to 90 through 93 for the four devices. The 9 defines the control unit in this case and must be the same for all of the devices. If less than four 2311 devices are installed, any of the four low-order digit addresses (0 through 3) may be used. The standard interface, if used on channel 1, can use any address except the 9X series.

CONSOLE PRINTER-KEYBOARD (IBM 1052 MODEL 7)

The Console Printer-Keyboard (PR-KB) is a Model 25 required feature and is physically attached to the processing unit frame as an integral unit. The keyboard allows entry of information into the processing unit for either initiation or alteration. The printer allows the production of a visual record of information from the processing unit. It may serve as an output unit, a record of operation, or as a logout of error conditions. The keyboard and the printer are controlled by the attachment built into the processing unit.

To the programmer the printer-keyboard appears to be attached to channel 0, but it is not physically connected to the standard interface and need not be included in the count of control units attached. For program-controlled operations, the printer-keyboard is controlled with the normal channel instructions. After the operation is initiated, other programmed instructions are handled in the normal manner. Data is transferred as required with multiplex share cycles. For manually initiated operations, normal programmed instructions are suspended until the operation is completed.

When the attachment requires a share cycle for the transfer of data or status, the share cycle is executed upon completing processing for the current instruction and all higher priority requests. If simultaneous requests for data service occur for the printer-keyboard and any other I/O unit on channel 0, the request for the other unit is honored first.

In addition to program-controlled operations, the printer-keyboard can perform alter/display and logout functions. The alter/display function is initiated when the Alter/Display key is operated (CPU console). The primary function of the alter/display operation is to alter and subsequently display the contents of a storage address or group of sequential addresses. The display feature can be used without alteration when it is necessary to examine stored information. In this case, the stored information is not changed. During the alter/display operations, all I/O operations in progress and trapping functions are allowed in the normal manner.

The logout function provides a hard copy printed output of CPU machine errors that may occur. The logout function is initiated through the machine-check trap.

Status or sense information is not applicable to the logout and alter/display functions. These functions are not executed until any current printer-keyboard program-controlled operation is completed to the point of device-end status. The status and sense conditions for the operation must remain in the attachment UCW until after the manual operation is completed.

If an alter/display (or logout) operation is started, CPU instruction execution is delayed until after the operation is completed.

KEYS AND INDICATORS

Certain keys and indicators are not used when the PR-KB is attached to the System/360 Model 25. These unused items are all on the upper portion of the console and are indicated by an asterisk (*) in Figure 5.

INDICATORS (FIGURE 5)

INTVTN REQD (Intervention Required)

This indicator is on when:

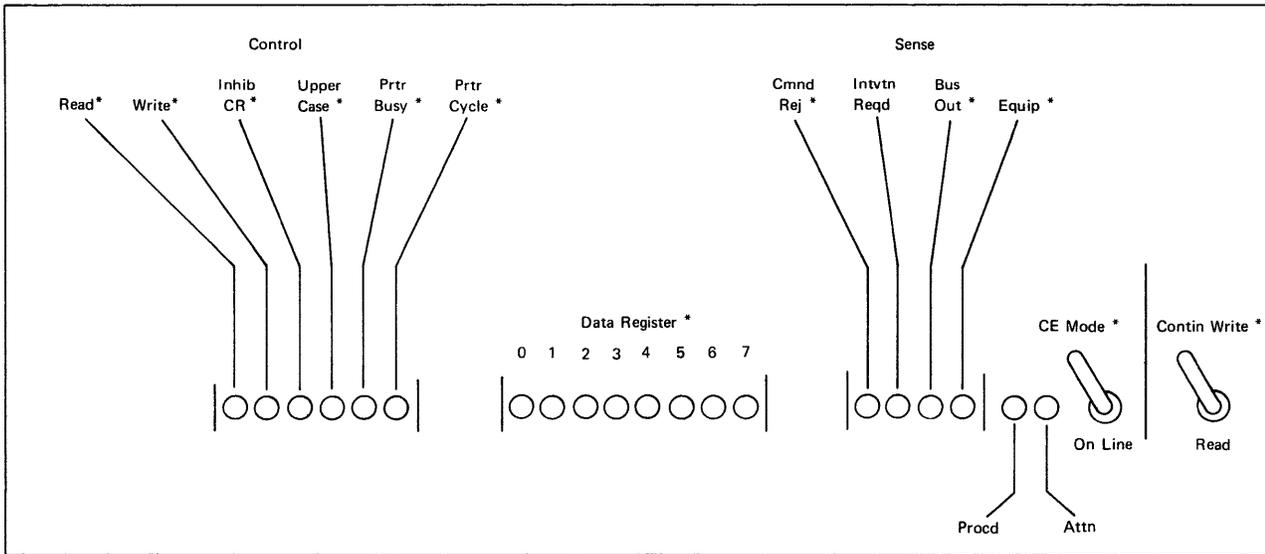
1. The forms switch indicates that the printer is out of forms, or
2. The printer not-ready switch is operated.

Note that the PR-KB enters the not-ready state when the forms switch indicates that an out-of-forms condition exists.

To return to the ready state, forms must be loaded and then the ready-key must be operated.

PROCD (Proceed)

The proceed indicator is used in two separate instances: a PR-KB read-command operation and an alter/display operation. For a read command operation, the Proceed light turns on each time the attachment is in a condition in which a character (or function) key can be operated.



* Indicators or switches marked with an asterisk are not used.

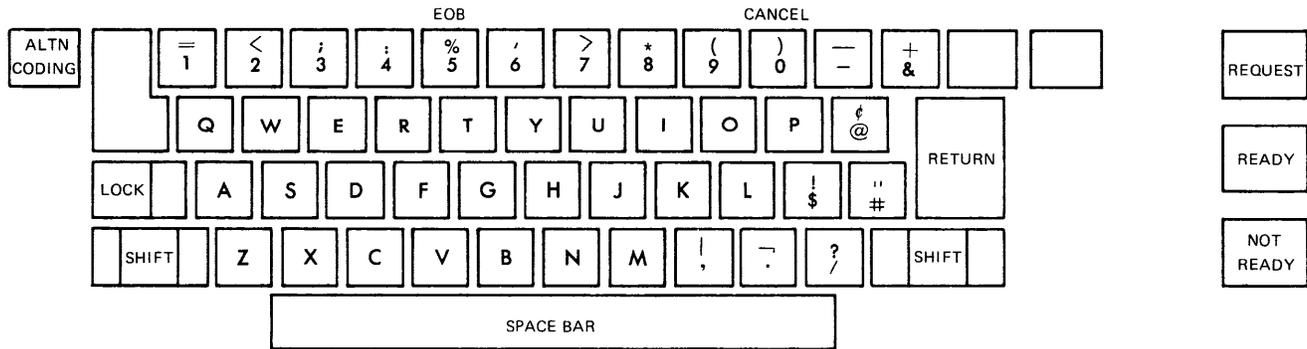


Figure 5. IBM Console Printer-Keybaord

For an alter/display operation, the proceed indicator and the alter/display indicator on the CPU console are both on when the attachment is in a condition to allow the operator to perform the required keying for the alter/display operation.

In either operation (read command or alter/display), the proceed light must be on before data can be entered from the keyboard.

ATTN (Attention)

The Attention indicator is turned on when the request key is operated. It is turned off when the PR-KB request generated by the request-key operation has been accepted by the attachment. The attention status is not set on in the attachment until any PR-KB operation that is in progress is completed.

Alter-Display Indicator (On CPU Console)

The alter-display indicator lights as a result of operation of the alter-display key, but only after the attachment is in a condition to allow performance of the alter-display operation.

KEYS (FIGURE 5)

REQUEST

Pressing this key causes attention status to be set on in the attachment as soon as any other current PR-KB operation is completed. The attention status is subsequently presented to the CPU (via the CSW), and, if the CPU program provides for this operation, a read command is issued to the PR-KB. Operation of the request key causes the attention light to turn on and attention status to be set in the attachment even if the PR-KB is in a not-ready condition. See also the Attn(Attention) indicator description.

READY

Operating this key causes the PR-KB to enter the ready state (if forms are in place). A not-ready-to-ready device-end is then presented to the CPU.

Operating this key causes no action if the PR-KB is already in the ready state.

NOT READY

Operating this key causes the PR-KB to go into the not-ready state. If the PR-KB is already in a not-ready state when this key is operated, no action occurs.

ALTN (Alternate) CODING

This key must be held down in its operated position for the EOB or cancel keys to be operative.

EOB

Operating the EOB key can be used to either:

1. terminate a read command operation, or
2. conclude the current manual keying during an alter/display operation. (The alter/display operation, however, is not terminated.)

The alternate key must be held in its operated position for the EOB key to be effective.

When a read command operation is terminated by pressing the EOB key, a carrier return and line feed are initiated at the PR-KB.

CANCEL

Operating this key cancels a keyed message and performs the same functions as the EOB key. However, when the key is operated during a read command (not alter/display), unit-exception status is set on in the attachment status byte.

The alternate coding key must be held in its operated position for the cancel key to be effective.

Alter/Display Key (on CPU Console)

Operating this key causes a request for a PR-KB alter/display operation. Keying-in for the operation can be started, however, only after the alter/display and proceed indicators are both on. (See the Manual Alter/Display section.)

ADDRESSING, CONSOLE PRINTER-KEYBOARD

The integrated console printer-keyboard attachment is addressed as if it were connected to channel 0. The sixteen-bit address developed from the I/O instruction identifies the attachment and the printer-keyboard. The device address is not limited by the usual channel-0 UCW addressing requirements because the attachment has its own UCW that is not device address dependent. In theory, the printer-keyboard may have any address from:

<u>Binary</u>	<u>Hex</u>
0000 0000	00
to	to
1111 1111	FF

In practice, the integrated PR-KB is assigned an address of 1F to standardize with other System/360 usage. This addressing makes use of one of the channel-0 subchannel addresses and prevents its use for the channel. If channel configurations require use of the subchannel, the PR-KB address can be changed by the customer engineer.

Under no condition should an address assigned to any other I/O device be assigned to the console printer-keyboard.

PROGRAM-CONTROLLED OPERATIONS

CHANNEL COMMANDS

Valid commands for PR-KB operations are:

Code Bits	Command Name
0123 4567	
0000 0001	Write
0000 0011	No-Op
0000 0100	Sense
0000 1000	TIC
0000 1001	Write with ACR (Automatic Carrier Return)
0000 1010	Read

Any command code (issued to the PR-KB) with a bit structure other than those listed results in unit-check status (bit 6) and command reject sense (bit 0) indications.

Write

The write command is accepted by the PR-KB attachment only if:

1. The PR-KB is operational. (That is, the forms switch indicates that forms are in place, and the not-ready switch has not been operated. The intervention required indicator on the console is off when operational.)
2. The write command has a valid format (i.e., data count ≠ 0, data address valid, etc.), and
3. The PR-KB is not performing some other operation.

If the PR-KB is not operational, unit-check status is in the CSW:

1. Stored for the Start I/O initiating the write command, or
2. Stored on a subsequent (I/O interruption or a Test I/O) if chaining to the write command was performed.

If the write command is accepted, the write latch is set on. A console share request occurs because the write latch is on and the PR-KB is in a state in which it can accept a character.

During the resulting share cycle, the first character of the message is read out of program storage and sent to the PR-KB.

If the character is a data character, it is translated from EBCD Interchange Code to the tilt/rotate code used to position the type element. If it is a function character (space or new line), the appropriate function magnet is activated.

The CCW data address (now in the PR-KB UCW) is incremented by 1 and the CCW data count (now in the UCW) is decremented by 1 for either a data or function code.

A share-reset condition is developed to reset the PR-KB share-request control. Another share-cycle request does not occur until the printer starts the operation for the character or function code just received. As soon as the print or function (space or new line) operation is started, a printer-busy condition occurs. At this point, another share-cycle request is initiated by the attachment. A share request is initiated because the write latch is on and the printer-busy condition exists. The entire cycle is then repeated.

During each share cycle, a test is made to determine if an intervention-required condition exists before:

1. A character is sent to the PR-KB from program storage, and before
2. CSW address and count updates are performed in the UCW.

If an intervention-required condition exists, the operation (including any chaining) is terminated. Unit-check, channel-end, and device-end are set on in the PR-KB status byte (in the UCW) and the intervention-required sense bit is set on in the PR-KB sense byte (in the UCW). Unit-check, channel-end, and device-end are set into channel-0 IB (Interrupt Buffer) if no other device already has status pending in the IB. A subsequent I/O interruption operation (or Test I/O instruction execution to the PR-KB) stores this status in the CSW. (If, however, another device already has status in the IB, the attachment circuits are conditioned to cause a share request when the IB becomes available.)

A zero-data count is checked-for during each write-share cycle after data is transferred and address and count updates are performed. If a zero-count condition is detected and data chaining is indicated,

a branch is made to a chain-data microprogram routine to load the new CCW. If data chaining is not indicated:

1. A zero-count condition is set in the UCW,
2. Channel-end and device-end are set on in the PR-KB unit status (and the write latch is reset) in the next share cycle.

If command chaining is indicated, the unit-status byte is set to 00 and a branch is made to a chain-command microprogram routine to load the new CCW.

Note, however, that an IL (Incorrect Length) indication is given if the SLI flag is off for any write command except write commands that have the CD (chain data) flag on. This IL indication occurs because the PR-KB requests one more share cycle after the data count (for a write command) has been decremented to zero.

If the end-of-line switch is activated, the carrier-return function is automatically initiated. In this case another share cycle is not requested until after the carrier return is completed.

The keyboard is held restored throughout the write operation.

No-Op (No Operation)

No-op is an immediate command. This command is processed whether or not the PR-KB is operational. If it is not operational, unit-check and intervention required are not set on when a no-op is executed.

Channel-end and device-end are set in a CSW stored for a Start I/O that initiates a no-op (if command chaining is not indicated).

Sense

The sense command is processed whether or not the PR-KB is operational; unit-check is not the response to the sense command, so that the sense command can be executed. The sense byte is read from the UCW (in auxiliary storage) and placed in the program storage location specified by the address in the sense command.

The data count in the sense command should equal one. If the count is greater than one, an IL (Incorrect Length) indication is a result of the operation if the SLI flag is off in the sense command.

Channel-end and device-end status are presented together in the CSW stored for a sense operation.

TIC

The transfer-in-channel command functions in the normal manner for PR-KB operations.

Write with ACR (Automatic Carrier Return)

The write with ACR command functions basically in the same manner as a write command. However, a carrier return is performed after the data count reaches zero. The carrier-return function is performed as follows.

1. In the share cycle that occurs after the last character for the command has been sent to the printer, an NL (New Line) character is automatically generated and sent to the printer by the microprogram, and channel-end is set on in the PR-KB status byte,
2. The carrier-return function is performed by the printer,
3. When the printer-busy condition occurs, another share cycle is requested (the write latch is still on) to set device-end in the unit-status byte.

If the end-of-line switch is operated after the last character is printed, two carrier returns occur: one for the end-of-line switch indication, the second for the write-with-ACR command.

Read

The read command is accepted by the attachment only if:

1. the PR-KB is operational (i.e., the interventions-required indicator is off),
2. the read command has a valid format, and
3. the PR-KB is not performing some other operation.

If the PR-KB is not operational, unit-check status is in the CSW:

1. stored for the Start I/O initiating the command, or
2. stored on a subsequent I/O interruption (or a Test I/O) if chaining to the read command was performed.

If the read command is accepted, the read latch is set on and the proceed indicator (on the PR-KB) lights.

Operation of a character key then results in a share-cycle request. A 6-bit pattern (plus a parity bit) is sent from the keyboard. Each bit-pattern sent to the CPU, however, is set into the A-register in the CPU. The bits are:

A-Register Bit From PR-KB Attachment

P (parity)	C (Check)
0	UC*
1	UC*
2	B
3	A
4	8
5	4
6	2
7	1

*Bits 0 and 1 = 11 if the character bit pattern from the attachment is for an uppercase (UC) character; bits 0 and 1 = 00 if the bit pattern is for a lowercase (LC) character.

If a parity check is detected (in the A-register), the PR-KB unit-check status and equipment-check sense bits are set on, but the operation is not terminated until its normal ending point. A machine check is not indicated and no machine-check trap is taken. A character is printed by the PR-KB whether or not a parity check is detected. (The character that is printed is unpredictable for a parity-error condition.)

The character bit pattern received by the CPU is translated to the appropriate EBCD Interchange Code bit pattern and stored in program storage. The translation is effected by the microprogram routines in conjunction with a translation table in auxiliary storage. The EBCD Interchange Code bit pattern is then sent back to the PR-KB to set up for printing; the keyboard is restored after printing.

The operation is similar if the space or carrier-return key is operated. Pressing or releasing the shift key, however, does not cause a share request. A character or function key must be operated to cause a share request.

If the end-of-line switch is operated after a character is printed, a carrier return occurs (during which the keyboard is held restored) but a carrier-return character bit pattern is not sent to program storage.

If the EOB key is pressed (while the alternate-code Key is held operated), the

read operation is terminated. (If the data count ≠ 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation.) The EOB-character bit pattern is not sent to program storage and nothing is printed as a result of an EOB-key operation.

If the cancel key is pressed (while the alternate-code key is held operated), unit-exception status is set on. (If the data count ≠ 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation.) A bit pattern is not sent to program storage and no character is printed for a cancel-key operation.

If the data count is equal to zero, the operation is terminated the next time any key is operated. The character bit pattern is not sent to program storage and nothing is printed as a result of the operation. If any key other than the EOB or cancel key is operated, an IL is indicated in the CSW stored when the SLI flag is off.

If an intervention-required condition occurs during the data transfer, the read operation is terminated with unit-check, channel-end, and device-end as the ending status. The intervention-required sense bit is set on.

A carrier return is performed by the attachment at the end of a read command in the same manner as for a write-with-ACR command.

STATUS BYTE

The status byte for the console is kept in auxiliary storage location 0XFA. The PR-KB status is stored in the CSW only for channel-initiated, not-ready-to-ready device-end, and attention-status operations (i.e., not for alter/display or logout functions).

Attention, Bit 0

This bit is set on when the request key is pressed, but only if no other PR-KB operation is in progress. If another operation is in progress, pressing the request key causes the attention-status bit to be set on after status for the other operation has been cleared at the UCW (i.e., accepted by the CPU program). If the other operation is for a logout or an alter/display operation (for which operations status is not presented), attention is not set on until the logout or alter/display is completed.

- After attention status is set on:
1. If an I/O interruption for the PR-KB is processed, the CSW stored contains attention (CSW bit 32).
 2. If a Start I/O is executed for the PR-KB before the I/O interruption can be processed, the CSW stored for the Start I/O contains attention (CSW bit 32) plus busy (CSW bit 35).
 3. If a Test I/O is executed for the PR-KB before the I/O interruption is executed, the CSW stored for the Test I/O contains attention (CSW bit 32).
 4. If a Halt I/O is executed for the PR-KB before the I/O interruption can be processed, the CSW is not stored and the condition code = 0 (interruption pending).

The preceding items 1, 2, and 3 clear the status at the PR-KB. Item 4 does not clear the status.

Status Modifier, Bit 1

Control Unit End, Bit 2

Unit-status bits 1 and 2 are not used for PR-KB operations.

Busy, Bit 3

Busy (bit 35) is set in the CSW stored as a result of execution of a Start I/O for the PR-KB only for the following conditions:

1. A program operation (other than a no-op command) has been completed to the point at which channel-end has been accepted by the CPU (an I/O interruption or Test I/O instruction has been processed to store the channel-end in a CSW) but device-end is now outstanding. Device-end (CSW bit 37) accompanies busy in the CSW for the Start I/O, and the status at the PR-KB is cleared.
2. Attention-status (for a request-key operation) is outstanding for the PR-KB (i.e., the attention has not yet been cleared by an I/O interruption or Test I/O operation). Attention (CSW bit 32) accompanies the busy bit in the CSW stored for the Start I/O.
3. A device-end for a not-ready-to-ready sequence (the ready switch has been operated to place the PR-KB in a ready condition) is outstanding. Device-end (CSW bit 37) accompanies busy in the CSW stored for the Start I/O.

4. A program operation has been completed to the point at which channel-end has been accepted by the CPU (an I/O interruption or Test I/O instruction has been processed to store the channel-end in the CSW) but device-end is not yet available. The busy bit alone is presented in the CSW for the Start I/O, and the PR-KB status is not affected.

Busy is in a CSW stored as a result of execution of a Test I/O instruction only if the Test I/O for the PR-KB is executed after channel-end for a command has occurred and stored in the CSW, but before device-end for that same command has been set on.

Channel-End, Bit 4

Channel-end is set on in the attachment for any of the following conditions.

1. A zero data count has occurred for a write, write-with-ACR, read, or sense command. (For write or write-with-ACR, channel-end is set on during the share cycle after the one in which the zero data count is detected.)
2. At initial selection during execution of a no-op command when that command is accepted by the attachment.
3. The EOB key or the cancel key has been operated during a read instruction.
4. If a count greater than 1 is specified in a sense command, the operation is terminated after one byte is transferred.

If channel-end alone is available through channel-0 IB or has been stacked, it is cleared by an I/O interruption (or by a Test I/O) and stored in the CSW.

Channel-end and device-end are indicated in the CSW stored as a result of a Start I/O that initiates a no-op when command chaining is not specified.

Device-End, Bit 5

Device-end is set on for any of the following.

1. After a carrier return is mechanically started at the PR-KB by the control unit for a terminated read or write with ACR command.

2. On the share cycle following the one in which a zero data count condition occurs for a write (with no ACR) command.
3. When the attachment accepts a no-op command.
4. When the ready switch is operated to put the PR-KB in a ready condition.
5. During the share cycle in which a sense byte is sent to the CPU.

If a device-end has been generated or stacked, it is cleared during initial selection routines for a Start I/O if channel-end for the operation has already been stored in the CSW by an I/O interruption or Test I/O operation. Busy accompanies device-end in the CSW stored for the Start I/O.

Test I/O clears any outstanding device-end. A Halt I/O does not clear a device-end at the PR-KB.

Unit-Check, Bit 6

Unit-check is set for any of the following reasons.

1. When a character with even parity is sent from the keyboard to the CPU during a read command operation, equipment check, sense bit 3, is also set on for this condition.
2. When the forms switch indicates that the PR-KB is out of paper or is in a not-ready condition (i.e., intervention light on the console is on), but then only:
 - a. during a read or write (with or without ACR) command operation, or
 - b. at initial selection for a read or write (with or without ACR) command, or
 - c. during execution of a Test I/O instruction to the PR-KB.
(Intervention Required, sense bit 1, is also set on for this condition.)
3. If a command byte not defined for the PR-KB is sent to the attachment. (Command reject, sense bit 0, is also set for this condition.)

Unit Exception, Bit 7

This bit is set on if the cancel key is operated, but only during a read command operation. The read operation is terminated (channel-end status is set on). If the count is not zero and the SLI flag is off for the read command, incorrect-length status (CSW bit 41) is also indicated during a subsequent I/O interruption or Test I/O operation.

CHANNEL-STATUS BYTE FOR PR-KB

The channel status byte for PR-KB operations is set up in the special UCV used for the PR-KB. The channel status byte portion of the CSW is stored as a result of processing a Test I/O instruction, if an interruption condition is outstanding for the PR-KB, or as a result of an I/O interruption executed for the PR-KB.

PCI (Program Controlled Interruption), CSW Bit 40

A PCI indication is given as defined by System/360 architecture. Specifically:

1. The PCI does not affect the progress of the current PR-KB operation.
2. PCIs are not stacked. If one or more PCI in a chain has not been processed (prevented by the system mask), only the latest PCI is processed when allowed.
3. A PCI bit in a CCW causes the PCI to remain pending (until processed) throughout the chain if the PCI cannot be taken when first detected.

IL (Incorrect Length), CSW Bit 41

1. IL is set in the CSW (stored by a Test I/O or I/O interruption) as a result of a read command during which the EOB (or cancel) key is operated when the count does not equal zero and the SLI flag is off. Any chain is terminated.
2. IL is set in the CSW (stored by a Test I/O or I/O interruption) as a result of a read command during which the count equals zero and any key other than the EOB or cancel is operated and the SLI flag is off. Any chain is terminated.

3. IL is set for a read command for which an intervention-required condition occurs (out of forms or not-ready switch is operated), and the count does not equal zero when either:
 - a. The SLI flag is off, or
 - b. The SLI flag is on and data chaining is also specified (CD flag on).
 Any chaining is terminated.

4. IL is set for any write command if the SLI flag is not on for that operation. This results from the attachment requesting one more data cycle after the CCW data count has decremented to zero. Any command chaining is terminated along with the operation when the IL indication occurs. If, however, the chain-data flag is on in the current write command, the IL indication does not occur for that write command. The last write command in the data chain, however, should have its SLI flag on to avoid the IL indication.
5. IL is set for a sense command if the data count specified is greater than 1 and the SLI flag is off.

Program Check and Protection Check, Bits 42 and 43

Program check and protection check are set as defined for channel 0.

Channel Data Check, Bit 44

This bit is not set for PR-KB operations. (Even-parity detected on a character from the keyboard during a read operation results in unit-check-status and equipment-check-sense indications.)

Channel Control Check, Bit 45

This bit is set as defined for channel 0.

Interface Control Check, Bit 46

The only PR-KB condition for which an interface control check indication is given is when a share cycle is requested but no operation is indicated by the attachment circuitry when an attempt is made to execute the false share cycle. That is:

1. A not-ready-to-ready sequence has not been performed,
2. The request key has not been operated,
3. No program controlled operation is in progress,
4. No status is outstanding for the PR-KB, and
5. No logout or alter/display operation is indicated in the attachment circuitry.

Chaining Check, Bit 47

This bit does not apply to Model 25 operations.

SENSE BYTE (PR-KB)

The PR-KB sense byte is kept in auxiliary storage location 00F7. Unit-check status is set whenever any one or more of the following bits is set.

Command Reject, Bit 0

This bit is set on if a command not defined for the PR-KB is issued.

Intervention Required, Bit 1

This bit is set on only for a read or write command in which:

1. The not-ready switch has been operated to place the PR-KB in a not-ready condition, or
 2. The forms switch indicates that the PR-KB requires forms loading.
- Any command other than a read or a write is processed (even though either or both of the two preceding conditions exist) and intervention required is not set on.

Bus-Out Check, Bit 2

This bit is not set for PR-KB operations.

Equipment Check, Bit 3

This bit is set on when even parity is detected on a character code sent from the PR-KB to the CPU during a read command

operation only. The even parity is detected in the CPU A-register.

Bits 4-7

These bits are not set for PR-KB operations.

MANUAL ALTER/DISPLAY

This facility provides for altering or displaying the contents of:

1. auxiliary storage,
2. main storage.

Two advantages provided by this facility are:

1. Current I/O operations (data transfers and chaining) are not caused to overrun, as they might if alter/display operations were initiated from the system console.
2. A printed copy that specifies the operation (alter or display), the location(s) accessed, and the data used is provided by the PR-KB.

Note Good operating practice dictates that the contents of the storage positions to be altered be displayed prior to altering. This ensures that the correct locations are addressed, and provides a hard copy printout of the contents of storage prior to the alteration.

Setup

To initiate an alter or display operation, the operator must first press the PR-KB alter/display button (on the CPU console) and then wait for both the PR-KB proceed light and the alter/display light to turn on.

When these lights turn on, the operator should type a two-character sequence (in lowercase), depending upon the desired operation. These characters are called the operation characters and can be:

First Character Specifies

a	alter operation
d	display operation
c	*continue

Second Character Specifies

a	auxiliary storage
m	main storage (program)
p	current PSW

*Note: If the first character typed is a "c", the operation is ended and a return is made to process the next CPU instruction.

Addressing

Next, the operator must type an address for:

<u>Area</u>	<u>Address Format</u> <u>(lowercase hexadecimal)</u>
auxiliary storage	xxxx
main storage	xxxx

No address is used to display the current PSW.

Count

A one-byte count is required for display of main or auxiliary storage locations. The count byte is entered as two hexadecimal (lowercase) digits after the address. A count byte equal to 00 results in display of a maximum of 256 bytes from the addressed location. Lesser count-byte values correspond to the number of bytes to be displayed.

A byte count is not used for displaying the current PSW or for altering program or auxiliary storage locations.

Execution of Alter or Display

After the operation characters, address, and count (if any) have been typed, the EOB key must be operated for the operation to be executed. However, it is good practice to examine the typed input message so that its accuracy can be verified before the EOB key is operated. If the operation is for display, the contents of the specified locations are then printed in uppercase.

After the EOB key is pressed:

1. for a display operation, the data is printed.
2. for an alter operation, the data to be stored must be typed.

End Operation

The cancel key can be pressed at any time to end the operation (and return for a retry) except when characters are being printed for a display operation, in which case the keyboard is locked.

At the end of a display printout, a return is made to the beginning of the routine so that the operator can perform another display, or an alter, operation.

An alter operation is normally ended by operating the EOB key after the required data has been typed. However, the cancel key can be used.

Note that an exit is not made from the alter/display routine until, at the beginning of an alter or display operation, the first operation character typed is c (continue). Therefore, the operator can perform as many alter and/or display operations as desired without exiting from the routine. Until the exit is accomplished, however, CPU instruction processing is stopped.

CPU instruction processing is resumed when, after an exit is made from the alter/display routine via a continue operation, the start key on the CPU console is pressed.

During an alter operation, data is altered on a byte basis. For example, assume that the byte data to be entered is af, but that the operator types bf instead of af. The bf is stored. The operator should then press either the EOB or the cancel key to return to the beginning of the routine for a retry of the entire operation.

If the error is noticed before the f is typed, the byte is not stored. If the cancel key is then operated (before the f is entered), a return to the beginning of the routine is made, and the operation can be retried. In either case, the entire manual operation must be repeated to store the af.

MESSAGE FORMATS

The microprogram initiates a line feed and carrier return after sixteen halfwords have been printed on a line (for either alter or display). Data is column-justified and blanks are provided between halfwords for either display or alter data. Also, the routine provides for offsetting two spaces at the left margin if an odd starting

address is specified for alter or display of auxiliary or main storage (see following formats).

All input typing is in lowercase; all output printing of hexadecimal alpha characters is in uppercase. In the following formats, x designates a valid hexadecimal digit.

Alter Storage

The second operation character can be a (auxiliary) or m (main).

Input message: aa xxxx (EOB)
Address-----↑

Input data xx xxxx xxxx.....xxxx
(odd address): xxxx (EOB)

Input data xxxx xxxx xxxx.....xxxx
(even address): xxxx (EOB) ↑
16th halfword-----↓

Display Storage

The second operation character can be a (auxiliary) or m (main).

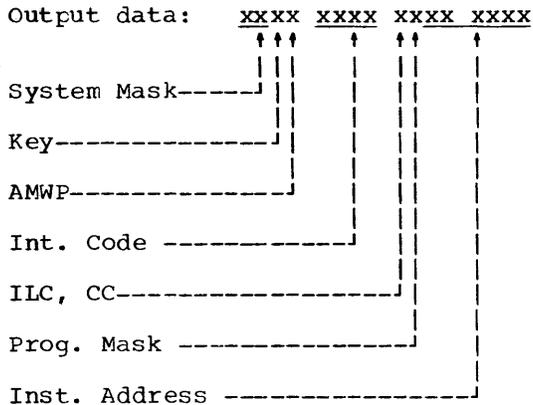
Input message: dm xxxx xx (EOB)
Address-----↑
Count-----↑

Output data:

1. odd address
odd count xx xxxx xxxx xxxx
2. odd address
even count xx xxxx xxxx xx
3. even address
odd count xxxx xxxx xxxx xx
4. even address
even count xxxx xxxx xxxx xxxx

Display Current PSW

Input message: dp (EOB)



ERRORS (ALTER/DISPLAY)

The PR-KB prints the error message, INVALID CHARACTER, if any one of the following operator errors is made.

1. An operation character is other than:
First character: a, d, or c
Second character: a, m, or p.
2. A two-digit address is typed for an auxiliary or main storage location.
3. A count byte is typed for a storage (auxiliary or main) alter operation.
4. A count byte is not typed for a main or auxiliary storage display operation.
5. A character other than a valid hexadecimal digit is typed for an address, count byte, or input alter data.
6. A key other than EOB or cancel is operated at the end of typing the input message.
7. The EOB key is operated during alter data input after only the first hexadecimal digit of a byte is typed for main or auxiliary storage.
8. The main or auxiliary storage address is invalid for the system. (INVALID CHARACTER is typed after the storage access by the invalid address is attempted.)

Note that storage protection is not operative for PR-KB alter/display operations.

LOGOUT

The PR-KB logout is a microprogram supported function that prints out the information contained in the diagnostic logout area of customer program storage (i.e., locations 128-159, decimal notation, in the Model 25). Existing macroprograms are not affected by this logout. The format and contents of the diagnostic logout area are machine dependent. Macroprograms (such as the 2030 SEREP) that act on this information are not applicable to the Model 25.

In general, the function of such macroprograms is provided by the PR-KB logout microprogram. Subsequent to execution of the PR-KB logout microprogram, a System/360 machine-check interruption is initiated. Existing restart procedures and macroprograms that do not act directly on the diagnostic logout area (such as BPS, DOS, OLTEP, etc.) are applicable to the Model 25 within the limits of storage size.

The program storage byte locations and contents of the diagnostic area are:

<u>Address</u> <u>(decimal)</u>	<u>Contents</u>
128	MC Reg
129	MMSK Reg
130,131	Address where check occurred.
132	BA
133-135	Not used (zeros)
136,137	PR-KB Diagnostic Conditions
138,139	Not used (zeros)
140	2540 Diagnostic Conditions 1 (RPD1)
141	2540 Diagnostic Conditions 2 (RPD 2)
142	2540 Feed Stop Conditions
143	2540 Feed Stop and Read Check Conditions
144	1403 Diagnostic Conditions (PRD)
145-147	Not used (zeros)
148	2311 Counter Hi (CHI)
149	2311 Counter Lo (CLI)
150	2311 SERDES (SDI)
151	Not used (zeros)
152	Channel Indicator Byte
153	Channel - Unit Address
154-159	Not used (zeros)

SUGGESTED RESTART PROCEDURES FOR INTEGRATED PR-KB ON SYSTEM/360 MODEL 25

An I/O error causes an interruption condition. The condition causing the interruption is indicated in the CSW (Channel Status Word). The CSW (a double word) is located in CPU main storage

locations 40 through 47 (hexadecimal). Bit 38 of the CSW, when on, indicates a unit-check condition. This bit is bit 6 of the byte at main storage address 44 (hexadecimal).

When unit-check is detected by the program, a sense command should be executed for the PR-KB. Sense information sent from the attachment provides more detailed information concerning the cause of the unit-check. As a result of program analysis of the sense information, an error message should be made available to the operator to indicate the condition.

The following information describes the minimum actions that should be performed when the program detects unit-check status in the CSW.

The actions are related to particular sense indications that can occur. These bits are analyzed by the program. The choice of action(s) to be taken by the operator must be established at the installation.

Command Reject (Sense Bit 0)

Provide an operator message and exit from this error recovery procedure. Command reject occurs because of a programming error and indicates that a command not valid to the PR-KB was received at the attachment.

Intervention Required (Sense Bit 1)

The PR-KB enters a not-ready condition (intervention-required light on) because one of the following has occurred.

1. The not-ready key is operated. (Possible operator error.)
2. The PR-KB has run out of forms.

The intervention-required light on indicates the operator should:

1. load new forms if the PR-KB is out of forms and then press the ready key, or
2. press the ready key if the PR-KB is not out of forms.

Bus-Out Check (Sense Bit 2)

Not used for PR-KB operations.

Equipment Check (Sense Bit 3)

Provide an operator message to indicate failure to read the input message and do one of the following.

1. If there is no additional error recovery procedure, continue operation but consider the PR-KB inoperative.
2. If there is an additional error recovery procedure defined, exit to it. If the additional error recovery procedure fails, continue the operation but consider the PR-KB inoperative.

Equipment check is indicated for read operations only, and it indicates that bad parity was detected on a bit pattern sent from the keyboard to the CPU. The read command operation, however, is not terminated until its normal ending point, even if equipment check occurs.

Sense Bits 4, 5, 6, and 7

These bits are not used for PR-KB operations.

A single 1403 Printer, Model 2 or Model 7, can be attached directly to the System/360 Model 25 central processing unit by means of this integrated attachment.

Data is transferred to the 1403 attachment from the CPU for printing. Forms-control information is also transferred from the CPU to control the printer carriage.

To the program, the integrated 1403 appears to be on channel 0.

IBM 1403 PRINTER MODEL 2

The IBM 1403 Printer Model 2 has 132 print positions. The forms-control carriage operates at 33 inches/second for spacing or skipping of eight or fewer lines. It operates at 75 inches/second when skipping more than eight lines. Print speed, at single-line spacing, is a nominal 600 lines per minute.

IBM 1403 PRINTER MODEL 7

The IBM 1403 Printer Model 7 has 120 print positions. The maximum record length for the 1403 Model 7 is the same (132 bytes) as that for the 1403 Model 2, even though the 1403 Model 7 has only 120 print positions. Therefore, where the CCW SLI (Suppress Length Indication) flag is concerned, programming for these printers is identical.

The forms-control carriage speed is fixed at 33 inches/second for all line spacing and skipping operations. Print speed, at single-line spacing, is a nominal 600 lines per minute.

PRINTED FORMAT

Printed characters are spaced horizontally ten to the inch. Vertical line spacing is either six or eight lines per inch, under operator control.

The standard type style is 0.095 inches high by 0.062 inches wide.

SPECIAL FEATURES

INTERCHANGEABLE CHAIN CARTRIDGE ADAPTER (SPECIAL FEATURE)

The interchangeable chain cartridge adapter can be installed on either the 1403 Model 2 or Model 7. This feature permits the operator to insert an interchangeable chain cartridge with a different type font, or special-character arrangement. After installation, the change of cartridges can be made quickly by the operator without using special tools. Printer operation is not affected.

Note, however, that if special-character changes are made, each repeated character set on the chain should have 48 graphics because a graphic set count-length of 48 (30 in hexadecimal) is fixed in the standard printer attachment. (For an exception, see the Multiple Character Set Special Feature section.)

.079-INCH HIGH TYPE

The .079-inch high font is available for all printers described in this publication. The letters are shorter than those of the .095-inch type. The user, therefore, has a choice of type size. The two type styles should not be intermixed on a chain because the base lines of the type-slugs are not the same and wavy printing would be produced.

MULTIPLE CHARACTER SET (MCS) SPECIAL FEATURE

This special feature is available for the 1403 Model 2 only (not the Model 7) and requires that both the interchangeable chain cartridge adapter and the MCS adapter be on the 1403.

DESCRIPTION

CHAIN ARRANGEMENT CONSIDERATIONS

Two basic chain arrangements are available: the AN and HN chains. Each of these chains contains five identical graphic sets. Each set consists of 10 digit, 26 alphabetic capital-letter, and 12 special-character graphics (Figure 6). The AN and HN special graphics are the same as those supplied with the A and H chain arrangements for IBM 1400 systems, with two exceptions: in the AN arrangement, the plus sign (+) replaces the ampersand (&). In both the AN and HN arrangements, the ampersand (&) replaces the record mark (#).

Note that a 48-character chain (AN or HN) is used by the 1403 Printer Model 2 or 7, attached to the System/360 Model 25 with the integrated printer attachment. Graphic substitutions and type-font changes can be made if the Interchangeable Chain Cartridge special feature is installed in the 1403. However, the chain graphic-set count length is fixed at 48 in the standard attachment; the significance of this fixed count is described in following sections. Certain chains that have other than 48 graphics per set can be used when the Multiple Character Set special feature is installed. This special feature is for the 1403 Model 2 only (not the Model 7). (See the Interchangeable Chain Cartridge and Multiple Character Set sections for further details.)

In the following descriptions, the word graphic is frequently used. Any "graphics" shown in text or in figures, however, do not necessarily conform in either dimension or shape to the graphics on a chain. Refer to the type catalog in the IBM Sales Manual for specifications for the actual graphics.

Figure 6 is provided for reference purposes to show the printout representation of the available chains for System/360. An EBCD Interchange Code chart is shown in Appendix B.

Graphic Positions

An AN-chain has five identical sets of graphics; each set has 48 unique graphics. The graphics and the sequence in which these graphics are mounted on the chain are the same for all five sets. For example, all sets begin with the graphic 1 and end with the graphic #.

Hexadecimal numbers (graphic-position numbers) are associated with specific graphic positions in a set. Numbering begins at 01, for the first graphic in any of the five sets, and proceeds sequentially through 30 (48 in decimal notation). For example, the first eleven graphic-position numbers and associated graphics for any of the five sets are:

Graphic-Position Number:
01 02 03 04 05 06 07 08 09 0A 0B
1 2 3 4 5 6 7 8 9 0 #
Graphic (above)

The graphic-position numbers determine, during printing, which graphics are available for printing at specific print-line positions. Assume, for example, that:

1. The chain and printer controls are synchronized,
2. The mechanical portion of a printing operation is started, and
3. The printer-control circuitry indicates that graphic-position 01 is in position to cause printing at print-position one.

In other words, the graphic 1 is in position to print at print-line position one.

Whether the 1 prints is determined by the contents of position one of the PLB (Print Line Buffer). If PLB position one contains 01, a match occurs and the graphic 1 is printed; if PLB position one contains any bit pattern other than 01, the 1 is not printed. Printing at print-line position one is delayed; in this case, until another chain graphic, whose graphic-position number matches the contents of PLB position one, has been moved into the proper position.

The significant point here is that the contents of a PLB position must match the desired graphic-position number (determined by the printer controls in synchronism with the chain) before printing at the associated print-line position can occur. This means that PLB positions are loaded with bit patterns that correspond to graphic-position numbers and not with the bit patterns of data-record codes.

The bit patterns that are loaded into the PLB are read out of auxiliary storage module 7. Module 7 is loaded at CSL time (see the Loading the Printer Translator section). Data-record bit patterns, sent from program storage during a write command operation, are used to address auxiliary storage module 7 (module 9 on 24K systems).

For example, the EBCD Interchange Code bit-pattern for the character 1 is 11110001 (F1 in hexadecimal). The bit pattern, in the location specified by module-7 address F1, is 00000001 (01 in hexadecimal). This bit pattern matches graphic position number 01, which specifies the location of the graphic 1 on the chain. When a data record bit pattern of F1 is used to address module 7, the bit pattern 01 is stored into the PLB location associated with that F1 in the data record. Printing occurs after all locations of the PLB have been similarly loaded with the proper graphic-position bit patterns.

Nonprinting Bit Patterns

A bit pattern of 00 must be loaded into each position of auxiliary storage module 7 whose address corresponds to a data bit pattern for which no printing and no data check is desired. Normally, the characters null (bit pattern 00) and blank (bit pattern 40) in a data record should cause no printing. For these characters, then, 00 is loaded into the auxiliary storage module 7 locations specified by addresses 00 and 40.

A code of FF in a position of auxiliary storage module 7 results in setting a data-check condition (if block-data check is not in effect) when a data-record code addresses that position. Printing for the associated position does not occur. For example, a data bit pattern of 59 (hexadecimal) does not correspond to any character bit-pattern in the EBCD Interchange Code. Normally, then, FF should be loaded into location 59 of auxiliary-storage module 7. If a data-record bit pattern of 59 subsequently accesses the FF, a data-check condition is set on in the printer controls.

Any bit pattern greater than the maximum graphic-position number (hexadecimal 30 in the standard printer attachment) accessed from auxiliary storage module 7 during PLB loading, causes no printing and a data check (if block-data check is not in effect.)

Graphic-Set Count Length

A fixed graphic-set count length of 48 (30 in hexadecimal) is in the standard printer attachment. This means that a maximum of 48 usable graphic-position bit patterns can be loaded into auxiliary storage module 7. (Other codes produce the results described in the preceding section.)

Each character in the standard EBCD Interchange Code is associated with only one unique bit pattern. Also, only one graphic-position number can be loaded into an auxiliary-storage module-7 location. Therefore, only one graphic-position number can be read out of module 7 for any specific data-record bit pattern used to address the particular module-7 location.

For example, if the graphic 1 were repeated every 12 positions on a specially designed chain, only one of the graphic-position numbers (which should be 01) could be loaded into auxiliary-storage location F1 (EBCD Interchange Code bit pattern for a 1). Then, during printing, even if one of the other 1s (say, at chain positions 0D, 19, or 25) were in position to print, their graphic-position numbers would not be in the PLB. This results because when a data bit pattern of F1 is used to address auxiliary storage module 7, only the bit pattern 01 at the addressed location can be read out to the PLB. Therefore, the 1 at chain-position 01 has to be at a print position for which the PLB contains 01 before a 1 can be printed. The other 1-graphics on the chain would never print.

Because of the preceding considerations, printing speed does not increase if several of the same graphics are placed within a set on the chain. See the Printing Speeds section for details.

Dualed Graphics

The AN and HN chains are identical except for four special-character graphics on each chain. These graphics, and their bit patterns are:

AN		Corresponding HN	
Graphic	Bit Pattern	Graphic	Bit Pattern
#	7B	=	7E
@	7C	'	7D
%	6C	(4D
▣	4C)	5D

These graphics are at the same relative positions in their respective chain sets. For example (the first row is Position, the second row is AN, and the third row is HN):

01	02	03	04	05	06	07	08	09	0A	0B	0C	etc.
1	2	3	4	5	6	7	8	9	0	#	@	etc.
1	2	3	4	5	6	7	8	9	0	=	'	etc.

Auxiliary storage module 7 can be loaded with one total bit pattern so that if either chain (AN or HN) is on the printer, printing of all graphics can be achieved.

Data Record Bit Pattern

Low	High															
	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
X0	00				00	16										0A
X1							0D						25	19		01
X2													26	1A	0E	02
X3													27	1B	0F	03
X4													28	1C	10	04
X5													29	1D	11	05
X6													2A	1E	12	06
X7													2B	1F	13	07
X8													2C	20	14	08
X9													2D	21	15	09
XA																
XB					2F	23	17	0B								
XC					30	24	18	0C								
XD					18	30	22	0C								
XE					2E			0B								
XF																

Notes:

1. Load 00 to print a blank code.
2. Load FF to print a blank for a code and cause a data check.

Graphic

Chain Position		01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
	→	1	2	3	4	5	6	7	8	9	0	#	@	/	S	T	U	V	W	X	Y	Z	&	,	%
											=	'													(
19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30		
J	K	L	M	N	O	P	Q	R	-	\$	*	A	B	C	D	E	F	G	H	I	+	.	▯		

Arrangement AN-HN repeated on chain 5 times. Count length 30 (Hex)

Figure 7. Print Translation for Dualled 48AN-48HN Chains

Figure 7 shows the bit patterns in auxiliary storage module 7 for this arrangement. In this case, the special graphics # @ % ▯ of the AN chain are said to be dualled, respectively, with the special graphics = ' () of the HN chain.

The overall bit pattern is set up in auxiliary storage module 7 to specify the same graphic-position number for both graphics of each pair of dualled graphics. For example (see Figure 7) when the data-record bit pattern (7B) for a # on the AN chain is used to address module 7, 0B is read out and stored into a PLB position. The same action occurs when 7E (the bit pattern for the = on the HN chain) is used to address module 7.

Consequently, no matter which chain (AN or HN) is on the printer, a graphic (# or =) is printed after either 7B or 7E is used to read 0B out of module 7 and store that 0B into a PLB position.

Folding

Some I/O devices, such as certain communications terminals, operate on both upper and lowercase alphabetic character bit patterns. The bit patterns for the upper and lowercase characters are different:

Upper- case	EBCDIC Bit Pattern	Lower- case	EBCDIC Bit Pattern
A	1100 0001	a	1000 0001
B	1100 0010	b	1000 0010
J	1101 0001	j	1001 0001
K	1101 0010	k	1001 0010
S	1110 0010	s	1010 0010
T	1110 0011	t	1010 0011

The AN or HN chains, however, have no lowercase alphabetic graphics. If codes generated by I/O devices that use both uppercase and lowercase are expected in print records, auxiliary storage module 7 can be loaded as shown in Figure 8.

Data Record Bit Pattern

Low	High															
	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
X0	00				00	16										0A
X1							0D		25	19			25	19		01
X2									26	1A	0E		26	1A	0E	02
X3									27	1B	0F		27	1B	0F	03
X4									28	1C	10		28	1C	10	04
X5									29	1D	11		29	1D	11	05
X6									2A	1E	12		2A	1E	12	06
X7									2B	1F	13		2B	1F	13	07
X8									2C	20	14		2C	20	14	08
X9									2D	21	15		2D	21	15	09
XA																
XB					2F	23	17	0B								
XC					30	24	18	0C								
XD					18	30	22	0C								
XE					2E			0B								
XF																

Notes:

1. Load 00 to print a blank for a code.
2. Load FF to print a blank for a code and cause a data check.

Graphic

Chain Position	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
	1	2	3	4	5	6	7	8	9	0	#	@	/	S	T	U	V	W	X	Y	Z	&	,	%
											=	')
	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
	J	K	L	M	N	O	P	Q	R	-	\$	*	A	B	C	D	E	F	G	H	I	+	.	▣

Arrangement **Dualed AN-HN with Alpha Folding** repeated on chain 5 times. Count length 30 (Hex)

Figure 8. Print Translation for Dualed 48AN-48HN with Alpha Folding

As an example, either data-record bit pattern 1100 0001 (for A) or 1000 0001 (for a), used to address module 7, causes bit pattern 25 to be stored in the appropriate PLB position. Hence, A is subsequently printed for either the uppercase or lowercase data-bit pattern.

Multiple Character Set (Special feature for 1403 Model 2)

The method of printing and the use of auxiliary storage module 7 and the PLB are basically the same with this feature as with the standard 1403 attachment already described. However, when MCS (Multiple Character Set) is installed:

1. Any announced chain can be used on the 1403 Model 2, or
2. Chains, with other than 48 graphics per set, can be custom-designed according to application needs.

Chains with other than 48-graphic sets can be used with MCS because the graphic-set count-length is not fixed at 48 with MCS as it is in the standard printer attachment. The count length can be 16,40,48,60,120, or 240 when MCS is used and must be specified at CSL time when auxiliary storage module 7 is loaded. No count lengths other than those just listed, however, can be used. (The hexadecimal equivalents to these count lengths are 10, 28, 30, 3C, 78, and F0, respectively.)

Data Record Bit Pattern

Low	High															
	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
X0	00				00	4D	0C									0A
X1						13							31	2B		01
X2													32	2C	14	02
X3													33	2D	15	03
X4													34	2E	16	04
X5													35	2F	17	05
X6													36	30	18	06
X7													37	0D	19	07
X8													38	0E	1A	08
X9													39	0F	1B	09
XA																
XB					1D	11	0B	10								
XC				1C	1E	4E	12									
XD																
XE																
XF																

Notes:

1. Load 00 to print a blank for a code.
2. Load FF to print a blank for a code and cause a data check.

Graphic



Shaded Areas Represent Repeated Graphics

Chain Position		01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
	→	1	2	3	4	5	6	7	8	9	0	,	-	P	Q	R	#	\$	@	/	S	T	U	V	W
	→	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30
	→	X	Y	Z	▣	.	*													J	K	L	M	N	O
	→	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47	48
	→	A	B	C	D	E	F	G	H	I	+														
	→	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60
	→				&	%																			
	→	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78
	→																								

Arrangement PCS-AN repeated on chain 2 times. Count length 78 (Hex)

Figure 9. Print Translation for PCS-AN Chain (with MCS)

Figure 9 shows an example using a PCS-AN chain arrangement. For this chain, counting starts at 01 and proceeds through 78 (120 in decimal) because the chain has 120 graphics per set. Two sets of graphics are on the chain. Also note, in Figure 9, that graphic position bit patterns for every graphic position on the chain are not in module 7.

A unique data record bit pattern applies to each distinct graphic (assuming that folding is not used). A specific bit pattern can access only one byte from

module 7, but only one graphic-position bit pattern can be stored at a byte location in module 7. For example, the graphic-position bit pattern 01, for the graphic 1, is stored at module 7 location F1. Consequently the 1 graphics at chain positions 1F, 3D, and 5B (see Figure 9) never print. The MCS feature is provided primarily for use of various chains, not necessarily for increase of print-speed. (See the Printing Speeds section for details regarding attainable print speeds.)

LOADING THE PRINTER TRANSLATOR

The CPU auxiliary storage module 7 is loaded with the translate table for either the 48AN or 48HN chain during the CSL routine. When the MCS feature is used with the 1403 Model 2, the UCS Utility Loader program is used to enter the translate table into auxiliary storage module 7 as required. These translate tables substitute the graphic position on the printer chain for the actual character bit coding. Five cards are punched with the hole configurations that identify the printing characters. The order of the punching identifies the order of the characters on the printing chain.

The cards also contain a length count to indicate the number of graphics in the character set. The count is stored in OXA6 and OXA7 and is transferred into the printer control during system reset. The count length is always entered as 48 when the MCS feature is not installed. The following paragraphs discuss the card formats.

Auxiliary Storage Load Cards (5)

- Columns 1 and 2 contain the punched hole patterns that correspond to the auxiliary storage starting address at which data from the card is to be loaded. Column 1 of cards 1 through 4 contains 12-11-0 punching (translates to 70, hexadecimal). Column-2 punching in cards 1 through 4 is:

Card	Punching	Translates to Address
1	12-0-9-8-1	00
2	No punches	40
3	12-0-8-1	80
4	12-0	C0

Column 1 of card 5 contains 12-0-9-8-1 punching (translates to 00, hexadecimal); Column 2 of card 5 contains 11-0-6 (translates to A6, hexadecimal).

- Column 3 of all five load cards contains 11-0-9-8-1 punching (translates to 20, hexadecimal). This column specifies that auxiliary storage is to be loaded.
- The number of halfwords to be loaded from the card is specified in column 4 of that card. Cards 1-4 contain 11-0-9-8-1 punching (translates to 20, hexadecimal) in column 4; card 5 contains 12-9-1 punching (translates to 01, hexadecimal) in column 4.

- Card columns 5-68 of cards 1-4 contain punching that corresponds to the bit patterns to be loaded into the print translator. That is, if a card column contains 12-9-1 punching, a bit pattern of 0000 0001 (01, hexadecimal) is loaded into the auxiliary storage location to which that card column pertains. The punching in the columns is dependent upon the character/bit pattern correspondence desired and the position of a graphic on the chain.

The card-column/module-7 correspondence is:

CARD 1

Column	Module 7 Address (=data record bit pattern)
5	00
6	01
7	02
8	03
....
68	3F

CARD 2

Column	Module 7 Address (=data record bit pattern)
5	40
6	41
....
68	7F

CARD 3

Column	Module 7 Address (=data record bit pattern)
5	80
....
68	BF

CARD 4

Column	Module 7 Address (=data record bit pattern)
5	C0
....
68	FF

- The punching in any of these card columns represents (when translated):
- A graphic position number of a graphic on the chain,
 - FF or some bit pattern greater than the chain count length (to cause no printing and data checks for desired data record codes), or
 - 00 (to cause no printing and no data checks for desired data record codes).

For example, Card 1, column 5 punching is 12-0-9-8-1 to load 00 (hexadecimal) into auxiliary storage location 7X00. Card 4, column 6 punching is 9-1 to load the graphic-position number 31 (for the A on a PCS-AN chain) into auxiliary storage location 7XC1.

See the EBCDIC chart in Appendix B to determine the punching to be used for any standard graphic; see Figure 6 to determine the graphic position number on announced chains. (Counting starts at 01 for the leftmost character in the first row of each set of a chain, and proceeds to the right in a hexadecimal counting sequence.)

- Columns 5 and 6 of card 5 contain coded count lengths to be set in auxiliary storage locations OXA6 and OXA7. These count lengths are coded in the following ways:

<u>Column 5 Punching</u>	<u>For Count Length of*</u>
12-0-8-1	16
No punches	40
11-0-9-8-1	48
12-11-9-8-1	60
12-9-8	120
12-0-9-8-1	240

<u>Column 6 Punching</u>	<u>For Count Length of*</u>
11-0-9-8-7	16
11-7	40
12-0-9-8-7	48
12-3	60
12-0-7	120
12-9-8-7	240

*If MCS is not installed, counts of other than 48 are ignored.

- Column 69 in cards 1 through 5 is blank.
- The hexadecimal starting address for the card can be punched directly in these four columns for operator convenience. These punch patterns, however, are not used by the routine.
- Column 74 of cards 1 through 5 is punched 11-7 (i.e., the code for the letter P, which signifies a patch card).
- Columns 75-76 of cards 1 through 5 are blank.
- Columns 77-80 of cards 1 through 5 are punched with the sequence number of the card (this is not required).

PRINTER KEYS AND INDICATORS

START KEY

Operating the start key puts the printer in a ready condition (device-end status is presented to the CPU) if no interlock or stop condition exists. The interlock

conditions are listed in the Bit 1 (Intervention Required) section. A second start key is located at the rear of the printer for operator convenience.

STOP KEY

Operating this key puts the printer in a not-ready condition. Any printer operation that is already in progress when the stop key is pressed is completed in the normal manner. That is, any current data chaining or single command (if data chaining is not in force) is completed. Command chaining, however, is stopped at the end of execution of the current command. A second stop key is located at the rear of the printer for operator convenience.

SINGLE-CYCLE KEY

Operating this key puts the printer in a ready condition (a not-ready to-ready device-end is presented to the CPU) under the same conditions as for the start key. The printer then remains ready until a write command is executed. At initial selection for the next command (after the single write command is executed), unit-check status (bit 6) is presented to the channel because sense bit 1 (intervention required) is on. If another single-cycle operation is desired, the single cycle can be operated again. (The start key must be operated to return to normal continuous operation.)

Note that for a single-cycle operation, the printer goes to a not-ready condition only after a write command is executed. Therefore, if the single-cycle key is operated, commands (such as a control command to skip) are processed until a write command is executed. The write command puts the printer in a ready condition.

If a command is being executed when the single-cycle key is operated, the printer may go not-ready at the end of the command being executed, or after execution of the next write command.

CHECK-RESET KEY

Operating this key resets the following conditions:

- PLB (Print Line Buffer) Parity Check.

The PLB is the printer data buffer. A PLB parity check can occur when data (i.e., graphic-position numbers) is read into or out of the PLB.

2. Print-Hammer Check. A print hammer has fired when it has not been directed to fire; or, a hammer has not fired when it has been directed to fire; or, a PLB position bit pattern (which has not caused a data check) does not compare to any graphic position on the chain.
3. Sync Check. The type array is out of synchronism with the printer controls (i.e., chain counter).
4. Coil-Protect Check. A hammer driver cannot be reset.
5. Forms Check. Forms-feed trouble has occurred; the carriage-stop key has been operated; the carriage brush mechanism has been opened; or a manual shift has been made from 6 to 8 LPI (Lines Per Inch), 8 to 6 LPI, 8 to neutral, etc.

In addition, operating the check-reset key turns off the following indicators:

1. Print Check
2. Sync Check
3. Forms Check.

RESTORE KEY

Operating this key positions the carriage at channel 1 (carriage home position). A channel-1 hole should be used to indicate the start of a new form. Operation of this key does not cause the carriage to move if the printer is in a ready condition. However, whether the printer is ready or not, operation of the restore key causes the 1403 use meter to stop recording time. (See 1403 Use Meter.)

SPACE KEY

Operating this key causes a carriage single-space operation. Operation of the key does not cause the carriage to space if the printer is in a ready condition. However, whether the printer is ready or not, operation of the space key causes the 1403 use meter to stop recording time. (See 1403 Use Meter.)

CARRIAGE-STOP KEY

Operating this key terminates any carriage operation 9 milliseconds after the key is operated. The forms-check condition is set on when this key is operated.

PRINT-READY INDICATOR

This indicator is on when the printer is in a ready condition.

PRINT CHECK INDICATOR

This indicator turns on when any of the following conditions exist:

1. PLB Parity Check
 2. Print-Hammer Check
 3. Coil-Protect Check.
- (See Check-Reset Key for causing conditions.)

SYNC-CHECK INDICATOR

This indicator turns on when a sync-check condition exists. (See Check-Reset Key for causing condition.)

FORMS-CHECK LIGHT

This light indicates paper feed trouble or that the carriage-stop key has been operated. This light must be turned off by the check-reset key before the print start key is effective.

END-OF-FORMS LIGHT

When an end-of-forms condition occurs, unit-check (status bit 6) is sent to the channel at the next initial selection. Subsequently, intervention required (sense bit 1) is sent during a sense operation. Also, the printer-ready light turns off and the printer end-of-forms light turns on when the end-of-forms condition occurs.

To reset the printer, the operator must press the printer start key. The remaining lines of the form are then printed under program control. (The operator does not press the start key for each remaining line

to be printed. He presses the start key only once.) Alternately, the single-cycle key can be used. In this case, one line of print occurs for each operation of the single-cycle key.

When a hole is sensed in channel 1 (either space or skip to or by channel 1) of the carriage tape, the operation is terminated with the end-of-forms light on. Therefore, you must provide a carriage tape with a hole in channel 1 for proper ending of the printing operation. If there is no hole in channel 1, printing continues even though there are no forms in the printer. (Printing does not occur for any command following one in which the channel-1 hole is sensed.) If a skip to a channel other than channel 1 is specified, that skip is completed, even though forms-check is set when channel 1 is sensed.

ADDRESSING, 1403 PRINTER ATTACHMENT

The one-byte unit address of the 1403 used with the printer attachment control is set into auxiliary storage by the CSL routine. This address is used to select the printer prior to each command.

The integrated 1403 is normally addressed 0E for compatibility with other System/360 usage. This permits the maximum interchange of programs when required. This addressing makes use of one of the channel-0 subchannel addresses and prevents its use for the channel. If channel configurations require the use of the subchannel, the 1403 address can be changed by the customer engineer to any address between 00 and FF that is not used by another channel-0 device. The integrated 1403 has its own subchannel (UCW) that is not dependent on the address assignment.

COMMANDS, 1403 PRINTER ATTACHMENT

The following commands are for a Write operation with various carriage functions:

<u>Command Byte</u>								<u>Function</u>
<u>0</u>	<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>5</u>	<u>6</u>	<u>7</u>	
0	0	0	0	0	0	0	1	Write and No Space After Print
0	0	0	0	1	0	0	1	Write and Space 1 Line After Print
0	0	0	1	0	0	0	1	Write and Space 2 Lines After Print
0	0	0	1	1	0	0	1	Write and Space 3 Lines After Print
1	0	0	0	1	0	0	1	Write and Skip to Channel 1 After Print
1	0	0	1	0	0	0	1	Write and Skip to Channel 2 After Print
1	0	0	1	1	0	0	1	Write and Skip to Channel 3 After Print
1	0	1	0	0	0	0	1	Write and Skip to Channel 4 After Print
1	0	1	0	1	0	0	1	Write and Skip to Channel 5 After Print
1	0	1	1	0	0	0	1	Write and Skip to Channel 6 After Print
1	0	1	1	1	0	0	1	Write and Skip to Channel 7 After Print
1	1	0	0	0	0	0	1	Write and Skip to Channel 8 After Print
1	1	0	0	1	0	0	1	Write and Skip to Channel 9 After Print
1	1	0	1	0	0	0	1	Write and Skip to Channel 10 After Print
1	1	0	1	1	0	0	1	Write and Skip to Channel 11 After Print
1	1	1	0	0	0	0	1	Write and Skip to Channel 12 After Print

The following commands are for independent carriage operations:

Command Bytes								Function
0	1	2	3	4	5	6	7	
0	0	0	0	1	0	1	1	Space 1 Line Immediately
0	0	0	1	0	0	1	1	Space 2 Lines Immediately
0	0	0	1	1	0	1	1	Space 3 Lines Immediately
1	0	0	0	1	0	1	1	Skip to Channel 1 Immediately
1	0	0	1	0	0	1	1	Skip to Channel 2 Immediately
1	0	0	1	1	0	1	1	Skip to Channel 3 Immediately
1	0	1	0	0	0	1	1	Skip to Channel 4 Immediately
1	0	1	0	1	0	1	1	Skip to Channel 5 Immediately
1	0	1	1	0	0	1	1	Skip to Channel 6 Immediately
1	0	1	1	1	0	1	1	Skip to Channel 7 Immediately
1	1	0	0	0	0	1	1	Skip to Channel 8 Immediately
1	1	0	0	1	0	1	1	Skip to Channel 9 Immediately
1	1	0	1	0	0	1	1	Skip to Channel 10 Immediately
1	1	0	1	1	0	1	1	Skip to Channel 11 Immediately
1	1	1	0	0	0	1	1	Skip to Channel 12 Immediately

The following commands are for operations that cause no printing or carriage motion:

Command Byte								Function
0	1	2	3	4	5	6	7	
0	0	0	0	0	0	1	0	Diagnostic Print Line Buffer Read
0	0	0	0	0	1	1	0	Diagnostic Print Check Read
-	-	-	-	1	0	1		Diagnostic Write
0	0	0	0	0	0	1	1	No-Op
0	1	1	1	0	0	1	1	Block Data Check
0	1	1	1	1	0	1	1	Allow Data Check
1	1	1	0	1	0	1	1	Gate Load Command UCS
1	1	1	1	0	0	1	1	Load UCS and Fold
1	1	1	1	1	0	1	1	Load UCS and No Fold
0	0	0	0	0	1	0	0	Sense

Note: A dash (-) in the Diagnostic Write command byte indicates that these modifier bits can be set to any of the values used by the Write commands.

WRITE COMMAND

Execution of a write command causes addressing of the print translator (auxiliary storage module 7) by bit patterns from the data record. The graphic position numbers then read out of the print translator are stored in the PLB. PLB loading ends when the CCW data count is decremented to zero or when the PLB is fully loaded if the print record is 132 bytes. (The maximum CCW data count is 132 for either the 1403 Model 2 or Model 7, but only the first 120 bytes are used to specify printing in the Model 7.)

After transfer to the PLB is completed, the printer control scans the PLB and compares the graphic-position numbers to a counter that specifies which graphics are in position to print. A hammer driver is addressed in conjunction with an associated position of the PLB. If an equal compare occurs, the specified hammer is fired so that printing for that print-line position occurs. When all positions have been compared to the counter or have had an opportunity to compare, printing of the line is complete.

If any carriage operation associated with the write command is to be performed, it is done at this time. The command is completed when all printing and carriage motion are finished.

Channel-end is presented to the attachment after loading of the PLB is completed. Device-end is presented after the mechanical portion of the print operation, and carriage movement, if any, is completed. Device-end, for the carriage movement, is set at the beginning of carriage settling time.

CARRIAGE-CONTROL COMMANDS

The carriage operations can be initiated by separate commands rather than by modifiers associated with a write command. The initial status byte for these control commands contains channel-end if the command is accepted by the printer controls. Channel-end status is given at initial selection (command immediate) because no data transfer occurs.

The carriage operation is initiated. Device-end status is presented to the channel at the beginning of carriage settling time.

If a skip immediate command is given and the carriage tape is already at the channel

specified, the command is accepted. However, whether or not carriage movement occurs depends upon the previous command. When the carriage tape is at the channel specified (i.e., the brush for that channel is at a position one place past the sensed carriage tape hole), carriage movement for the skip immediate command occurs only if a write (with no space) command is accepted just before the skip immediate command. Otherwise, carriage motion does not occur for the skip immediate command. Note, however, that when the carriage tape is already at the channel specified by a write and skip command, skipping does occur after the line is printed.

DIAGNOSTIC PRINT-LINE-BUFFER READ

This command transfers the data in the PLB to the CPU. The initial status byte is all zeros if the command is accepted by the printer controls. Both channel-end and device-end are presented to the channel after all of the data has been transferred from the PLB to the CPU.

DIAGNOSTIC PRINT-CHECK READ

This command transfers error-check information corresponding to each position of the PLB to the CPU. The initial status byte is all zeros if the command is accepted by the printer controls. Both channel-end and device-end status are presented to the channel after all of the check data has been transferred.

The data transferred signifies:

Bit	Significance
5	Print Line Complete bit of PLB
6	Print Hammer Check
7	PLB Parity Check

DIAGNOSTIC WRITE

This command causes data to be transferred to the PLB. Printing does not start until the chain reaches home position. One print scan is taken but no hammer drivers are turned on. Channel-end status is presented to the channel after the data transfer is completed. Device-end status is presented after one print scan is completed. No carriage motion occurs.

NO-OP

This command performs no function in the printer controls. The initial status byte contains channel-end and device-end (command immediate).

BLOCK DATA CHECK (MCS ONLY)

This command causes the printer controls to ignore incomparable bit patterns that normally cause a data check. An incomparable bit pattern is either of the following graphic-position bit patterns read out of the print translator:

1. FF, or
2. A bit pattern greater than the graphic-set count-length set in the printer controls.

After the block-data check command is executed, the block-data-check condition remains in force until either machine power is turned off, or the allow-data-check command is executed. Channel-end and device-end are presented to the channel at initial selection for this command (command immediate). The block-data-check command must be either preceded by the gate-load command or it must be the first command of a chain for acceptance by the printer controls.

ALLOW DATA CHECK (MCS ONLY)

This command resets the block data check and permits the printer controls to recognize and indicate to the CPU that a data check has occurred due to an incomparable bit pattern. The status byte presented to the channel at initial selection for this command contains channel-end and device-end (command immediate). The allow-data-check command must be either preceded by the gate-load command or it must be the first command of a chain for acceptance by the printer controls.

GATE LOAD COMMAND (MCS ONLY)

This command is used as an interlock command for the block-data-check, allow-data-check, load-UCS-and-fold, and load-UCS-and-no-fold commands. The gate-load command must precede these commands or they will not be accepted by

the printer controls. The gate-load condition remains in force until one of the load commands or a write command is accepted. The block-data-check command or allow-data-check command should be given between the gate-load command and the load commands.

The status byte presented at initial selection for the gate-load command contains channel-end and device-end (command immediate). This command must be given as the first command of a command chain. If it is in any other position in a chain, it is rejected. (Unit check, due to command reject, is presented in the initial status byte.)

LOAD UCS AND FOLD (MCS ONLY)

This command is used with the UCS Utility Loader program to load the printer translate table into auxiliary storage module 7 when the MCS feature is used with the 1403 Model 2. The command performs no function when used with a system not having the feature. In the latter case, the command presents channel-end and device-end in the initial selection status byte (command immediate). This command must be preceded by the gate-load command or it will not be accepted.

LOAD UCS AND NO FOLD (MCS ONLY)

This command is used with the UCS Utility loader program to load the printer translate table into auxiliary storage module 7 when the MCS feature is used with the 1403 Model 2. The command performs no function when used with a system not having the feature. In the latter case, the command presents channel-end and device-end in the initial selection status byte (command immediate). This command must be preceded by the gate-load command or it will not be accepted.

SENSE

This command transfers one byte of sense data from the printer controls to the CPU. The data transferred is defined in the Sense Byte, 1403 Printer section. Channel-end and device-end are presented to the channel after the sense byte has been transferred to the CPU.

STATUS BYTE, 1403 PRINTER

The printer status byte is presented to channel 0 (i.e., to the CPU via the integrated attachment):

1. during an initial selection sequence when the channel sends a command byte to the 1403 attachment.
2. after the end of an operation at the printer (such as channel-end after data transfer and device-end after the mechanical portion of the operation) by means of an I/O interruption operation.
3. during an I/O interruption operation initiated by the 1403 attachment when the printer goes from the not-ready to the ready state. (That is, device-end is generated as a result of a not-ready-to-ready transition.)
4. during initial selection for a Test I/O instruction when status is outstanding in the printer attachment.

The status conditions are reset when the status is accepted by the channel, with the following exceptions.

1. If the unit-check (bit 6) status is caused by an intervention-required condition, unit-check is reset only after the 1403 has been restored to the ready condition.
2. Busy status is reset only when device-end status is accepted by the channel.

The significance of the status-byte bits is as follows.

BIT 0, BIT 1, BIT 2

Not used.

BUSY (BIT 3)

Busy status is in a CSW stored as a result of execution of a Start I/O instruction only if:

1. The 1403 attachment has an outstanding device-end (due to a not-ready-to-ready transition; or due to the completion of a previous command), and
2. Channel-end, if any, for the operation has already been cleared by the channel (by an I/O interruption operation or by execution of a Test I/O instruction).

Busy status for the 1403 is never in a CSW stored for execution of:

1. A Test I/O instruction (except when the

Test I/O is executed after channel-end has been cleared but before device-end has occurred),

2. A HALT I/O instruction, or
3. An I/O interruption operation.

CHANNEL-END (BIT 4)

Channel-end status is presented to the channel when data transfer, if any, to or from the printer has been completed. For control commands, channel-end is presented when the command is accepted by the printer attachment.

DEVICE-END (BIT 5)

Device-end status is given when a previous command has been completed or the printer is put in a ready condition. The printer is free to accept another command after this status is accepted by the channel (unless a unit-check condition, due to an intervention required, occurs before the next command is accepted).

UNIT-CHECK (BIT 6)

Unit-check status is given when the printer requires program or operator intervention due to one of the following conditions (see Sense Byte, 1403 Printer section).

1. Command Reject (Sense bit 0)
2. Intervention Required (Sense Bit 1)
3. Equipment Check (Sense bit 3)
4. Data Check (Sense bit 4)
5. Channel 9 (Sense bit 7)

The unit-check status bit can be given at initial selection, with channel-end status, or with device-end status.

UNIT EXCEPTION (BIT 7)

Unit-exception status is given when a hole is sensed in channel 12 of the carriage control tape during a carriage space operation. This bit is not set during carriage skip operations. It is presented only with device-end status.

SENSE BYTE, 1403 PRINTER

The intervention-required sense bit is reset when the responsible condition is corrected. All other sense bits are reset the next time the program causes the 1403 to be selected, except when the selection is due to one of the following.

1. Test I/O instruction
2. Halt I/O instruction
3. Sense command
4. No-Op command.

COMMAND REJECT (BIT 0)

Command reject is given when a command other than those defined for the printer is given. Command reject is also given if certain command sequences are violated. See the Commands, 1403 Printer Attachment section for the response of the printer to all of the possible command bytes.

INTERVENTION REQUIRED (BIT 1)

Intervention required is given when the printer has gone into a not-ready condition because of any one or more of the following conditions:

1. The print-stop key is operated.
2. A write command is performed following a single-cycle key operation.
3. The chain interlock is open due to one of the following conditions:
 - a. Chain-motor thermal-fuse open
 - b. Hammer-unit thermal-fuse open
 - c. Cartridge interlock open
 - d. 60V controlled-fuse open.
4. The printer has run out of forms.
5. A forms-check has occurred due to one of the following conditions:
 - a. Forms jam
 - b. The carriage-stop key is operated.
 - c. The carriage brush mechanism is open, or a manual operation from 8 to 6LPI, 8 to neutral, 6 to 8 LPI, etc. is performed.
 - d. The carriage drive is not in the neutral or drive position.
 - e. The carriage tape is not present.
 - f. The printer initially ran out of forms, was made ready, and then a hole was sensed in channel 1 of the carriage tape.
6. A sync check has been detected because

the chain is not synchronized with the chain counter.

7. A coil-protect check has occurred because a hammer driver could not be reset.

Intervention required is reset when the printer is restored to the ready condition. Intervention required can be set on reset only when the printer is not busy executing a command.

BIT 2

Not used

EQUIPMENT CHECK (BIT 3)

Equipment check is given when a hammer check or a print-line-buffer parity check is detected.

DATA CHECK (BIT 4)

Data check is given when a bit pattern of FF or a bit pattern greater than the chain count is accessed from the print translator, and the block-data-check latch is not on (i.e., the printer is in the allow-data-check mode).

BIT 5, BIT 6

Not used.

CHANNEL 9 (BIT 7)

A hole has been sensed in channel 9 in the carriage control tape during a carriage-space operation. This bit is not set during carriage-skip operations.

PRINTING SPEEDS

Printing speeds attained with the integrated 1403 Printer depend upon a number of factors. In general, printing speed depends on the number of identical sets on the chain. This number is fixed at

5 for the basic printer, and provides a nominal single-line printing speed of 600 lines per minute (lpm). If MCS is used (1403-2 only), the maximum number of identical sets is 15. In this case, however, the maximum printing speed attainable is 750 lpm. Spacing and format also affect the printing speed. This section presents a method for determining nominal and absolute-minimum printing speeds for various chain configurations although the actual print speeds will usually be greater than the calculated nominal figures.

The following formulas are used to calculate the speed for a given character set on the chain for either the IBM 1403-2 or 1403-7.

Nominal:

$$\text{lpm} = \frac{60,000}{\left(\frac{240}{f} - 1\right)(1.665) + 21.7}$$

Absolute minimum:

$$\text{lpm} = \frac{60,000}{\frac{240}{f}(1.665) + 21.7}$$

f = Number of times the given character set appears on the chain. (This value is always 5 for the 1403-7.)

The value $\frac{240}{f}$ must result in a whole number.

Note: In any case, the maximum printing speed cannot exceed 750 lpm. Hence, if a calculated speed exceeds this limit, the 750 lpm figure is used.

This feature utilizes an end-of-print-line concept to permit immediate carriage movement when a printed line is complete. As a result, the printing speed is variable, and can be in excess of the calculated nominal speeds.

The formula applies for continuous printing with single line spacing. When skipping or multiple spacing operations are performed, the additional forms-movement time must be added to the denominator of the formulas. Figure 10 shows the forms-movement times to be added to the formula denominator.

Consider, for example, calculation of the speed (by nominal formula) for a 48AN chain configuration. The number of times the complete 48AN configuration appears on the chain is 5:

$$\frac{240}{48} = 5 \text{ presentations of 48 AN set.}$$

Therefore, f (in the formula) equals 5. For continuous printing and single-line spacing with the AN chain:

$$\frac{60,000}{\frac{(240 - 1)(1.665) + 21.7}{5}} = 600 \text{ lpm}$$

Now consider the same 48AN configuration but with spacing of two lines after each line printed. Figure 10 shows that the 21.7 factor, in the denominator of the nominal formula for the chain printer, is replaced by 25. Nominal speed at which printing occurs (assuming continuous printing and spacing) is then:

$$\frac{60,000}{\frac{(240 - 1)(1.665) + 25}{5}} = 542 \text{ lpm}$$

PROGRAMMING TIMING INFORMATION (1403)

Transfer of one data-record character to the printer requires 16.2 microseconds.

Transfer of an entire print record may take longer than 132 times 16.2 microseconds, however, because other I/O operations may delay the print data transfer.

Lines Skipped	Time Required (ms)*
2	25
3	30
4	35
5	40
6	45
7	50
8	55

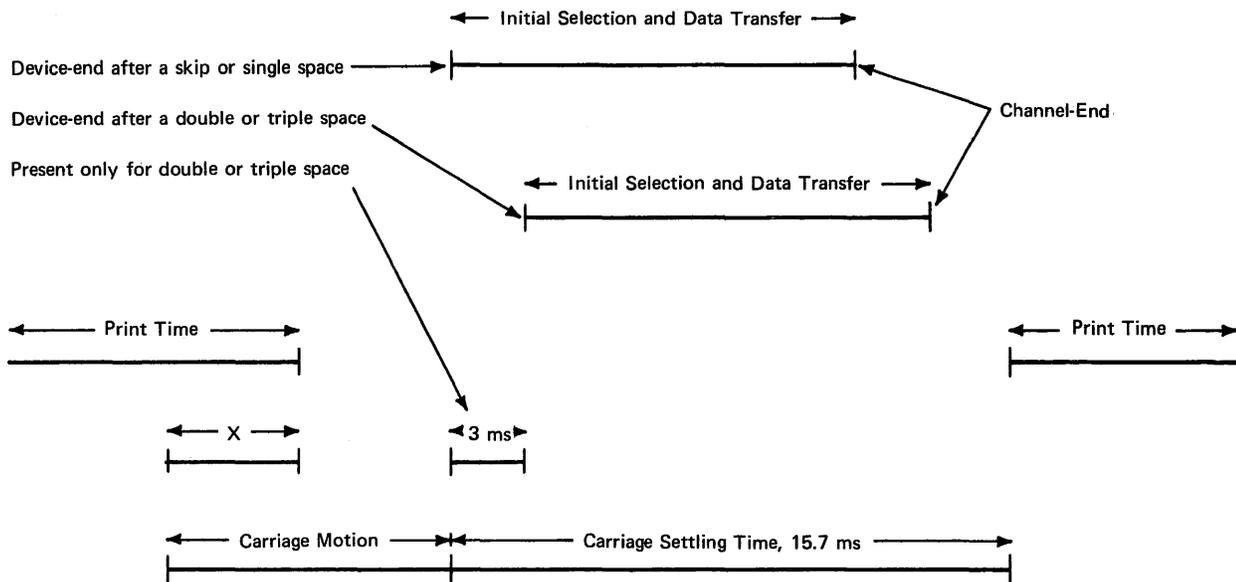
* Indicates the figure to be substituted in the speed calculation formula denominator for the 21.7 figure.

Additional value to be added to the 8-line figure of 55 is that which results by multiplying the number of spaces (in excess of eight) times 2.3ms (for the 1403-2) or 5ms (for the 1403-7)

Example:

<u>1403-2, 12 lines skipped</u>	<u>1403-7, 12 lines skipped</u>
55 + 4(2.3)	55 + 4 (5)
or 64.2ms	or 75ms

Figure 10. Form-Movement Times



Pre-energize: X = 1.67 ms (1403-2 and 1403-7)

Figure 11. Printer Timing Diagram

For a printer timing diagram refer to Figure 11. The minimum times from generation of channel-end to generation of device-end are (i.e., 750 lines per minute):

<u>Operation</u>	<u>Time (milliseconds)</u>
Write (no automatic space)	58.3
Write and single space	80
Write and skip	56.7 + carriage motion time

Between channel-end and device-end for a command-chained operation (not the chain). The condition code is set to 1; command chaining suppressed; the CSW are set to all zeros; channel-end for the operation will not subsequently be indicated. Device-end, after it occurs, will cause an I/O interruption. (Or, this device-end can be cleared by a Test I/O instruction.)

HALT I/O TO INTEGRATED 1403

The results of execution of a Halt I/O to the 1403 Printer are:

The device has outstanding status for an operation, or device-end for a not-ready-to-ready transition. The condition code is set to 0.

<u>Device Condition</u>	<u>Results of Halt I/O</u>
Not performing an operation.	The condition code is set to 1; the status portions of the CSW are set to all zeros.

The 1403 is not operational. The condition code is set to 3. Halt I/O cannot be executed during transfer of a print record from program storage. This results because CPU instruction processing is prevented during the print-record transfer.

POSSIBLE STATUS-BYTE BIT COMBINATIONS

This section lists the unit status combinations that can be presented to the channel from the 1403 attachment. For information concerning when and how unit status is stored in a CSW (Channel Status Word), refer to IBM System/360 Principles of Operation, Form A22-6821. In the following descriptions an asterisk (*) indicates that the combination is given only at initial selection for a Test I/O operation, or when status is presented in a sequence initiated by the 1403 attachment. A double asterisk (**) indicates that the combination is given only at initial selection for a command (not during execution of a Test I/O instruction or an I/O interruption).

1. 0000 0000

This combination is the response to the channel at initial selection when a write, a diagnostic read, or a sense command is accepted by the 1403 attachment. (This combination is then not stored in the CSW, because no CSW is stored for this condition.) It is also the response to a Test I/O instruction when the printer is ready, is not already busy performing an operation, and has no outstanding status to be presented to the channel. In this case, however, the all-zero status is not indicated in the CSW. Rather, the condition code is set to zero as a result of executing the Test I/O instruction.

This combination (00000000) can also be indicated in a CSW stored as a result of either of the following.

- A. A printer operation is being command-chained, and a Program Controlled Interruption, specified in a CCW in the chain, is indicated in the CSW stored by an I/O interruption before the chain of commands is completed.
- B. The printer operation is being command-chained, device-end status (with no unit-error status) for any but the last command in the chain has been cleared by the attachment, but then the next CCW read out results in a program error (protection check or program check is indicated in the CSW stored).

2. 0001 0000 (Busy Bit)

The busy bit alone is presented to the channel in response to any command (or Test I/O instruction execution) when:

- A. The printer is between channel-end and device-end (i.e., device-end has not yet occurred) for the last command of a chain (or for a single command if no chaining is indicated), and
- B. Channel-end for the command has already been cleared (i.e., stored in a CSW) by a previous Test I/O instruction or I/O interruption.

3. 0000 0001 and 0001 0001

Should not occur.

4. 0000 0010 (Unit Check Bit)

**Given at initial selection when a command is not accepted because one or more of the following sense bits is on as a result of the indicated condition (see appropriate sense bit description).

Bit Condition May Occur for

- 0 Any command
- 1 Any command other than sense

* Or, given if this same status was stacked at the 1403 attachment by the channel.

5. 0001 0010 (Busy and Unit-Check Bits)

**Given because combination 4 is outstanding in the 1403 attachment.

6. 0000 0011 and 0001 0011

Should not occur.

7. 0000 0100 (Device-End Bit)

* Given when a control or write command (either of which must have specified a carriage operation) is completed and channel-end for the operation has already been stored in a CSW.

* Or, given when the printer has gone from the not-ready to the ready state.

8. 0001 0100 (Busy and Device End Bits)

**Given for the same reasons as combination 7.

9. 0000 0101 (Device-End and Unit-Exception Bits)

* Given because a write or control command that causes a carriage space is completed and a hole is sensed in channel 12 of the carriage tape.

10. 0001 0101 (Busy, Device-End, and Unit-Exception Bits)

**Given for the same reason as combination 9.

11. 0000 0110 (Device-End and Unit-Check Bits)

* Given when a write or control command is completed (either of which must have specified a carriage operation) and one or more of the following sense bits is on as a result of the indicated condition.

Bit Condition May Occur for

3 Any write command
7 Any command causing a carriage space

* Or, given because the device goes from the not-ready to the ready state (creating device-end status) and then back to the not-ready state (before device-end is accepted).

* Or, given because a unit-check status (due to sense bit 0) is stacked by the channel at the attachment and the printer goes from the not-ready to the ready state before the unit check is accepted.

12. 0001 0110 (Busy, Device-End, and Unit-Check Bits)

**Given for the same reasons as combination 11.

13. 0000 0111 (Device-End, Unit-Check, and Unit-Exception Bits)

* Given because a write or control command (either of which caused a carriage space operation) is completed, and a hole is sensed in channel 12 of the carriage tape, and one or more of the following sense bits is on as a result of the indicated condition.

Bit Condition May Occur for

3 Any write command
7 A 9 hole was sensed in the carriage tape during a command that caused a carriage space operation.

14. 0001 0111 (Busy, Device-End, Unit-Check, and Unit-exception Bits)

**Given for the same reasons as combination 13.

15. 0000 1000 (Channel-End Bit)

**Given at initial selection of a control command that specifies a carriage operation.
* Or, given when data transfer is completed for a write command.

16. 0001 1000

Should not occur.

17. 0000 1001 and 0001 1001

Should not occur.

18. 0000 1010 (Channel-End and Unit-Check Bits)

* Given when data transfer (if any) is completed for a write command or given for a control command. For both situations, however, the following sense bit is on as a result of the indicated condition.

Bit Condition May Occur For

3 Any write command

19. 0001 1010

Should not occur.

20. 0000 1011 and 0001 1011

Should not occur.

21. 0000 1100 (Channel-End and Device-End Bits)

**Given at initial selection of a no-op, gate-load, allow-data-check, block-data-check, load-UCS-and-fold, or load-UCS-and-no-fold command when the command is accepted.

* Or, given when a command is completed, but channel-end and device-end have not yet been accepted by the channel.

22. 0001 1100

Should not occur.

23. 0000 1101 (Channel-End, Device-End, and Unit-Exception Bits)

* A write or control command that causes a carriage space is completed, no status has yet been accepted by the channel for the operation, and a hole is sensed in channel 12 of the carriage tape.

24. 0001 1101

Should not occur.

25. 0000 1110 (Channel-End, Device-End, and Unit-Check Bits)

* Given when a diagnostic read, a write, or a control command that causes a carriage space operation is completed, and one or more of the following sense bits is on as a result of the indicated condition.

Bit Condition May Occur for

3 Any diagnostic read or any write command.

7 Any command causing a carriage space during the operation of which a hole is sensed in channel 12 of the carriage tape.

26. 0001 1110

Should not occur.

27. 0000 1111 (Channel-End, Device-End, Unit-Check, and Unit-Exception Bits)

* A write or control command that causes a carriage space is completed, a hole is sensed in channel 12 of the carriage tape, and one or more of the following sense bits is on.

Bit Condition May Occur For

3 Any write command

7 A 9 hole was sensed in the carriage tape during a command that caused a carriage space

28. 0001 1111

Should not occur.

SUGGESTED RESTART PROCEDURES FOR 1403

An I/O error causes an interruption condition. The condition causing the interruption is indicated in the CSW (Channel Status Word). The CSW (a double word) is located in CPU main storage locations 40 through 47 (hexadecimal). Bit 38 of the CSW, when on, indicates a unit-check condition. This bit is bit 6 of the byte at main storage address 44 (hexadecimal).

When unit-check is detected by the program, a sense command should be executed for the 1403 that caused the unit-check. Sense information sent from the 1403 attachment provides more detailed information concerning the cause of the unit-check. As a result of program analysis of the sense information, an error message should be made available to the operator to indicate the condition. Depending on installation procedures, the error message can be printed out.

The following information describes the minimum actions that should be performed when the program detects unit-check status in the CSW.

The actions are related to particular sense indications that can occur. These bits are analyzed by the program. The choice of action(s) to be taken by the operator must be established at the installation.

Command Reject (Sense Bit 0)

Provide an operator message and exit from this error recovery procedure. Command reject occurs because of a probable programming error and indicates that a command or a command sequence not valid to the 1403 was received at the 1403 attachment.

Intervention Required (Sense Bit 1)

The printer enters a not-ready condition (ready light off) because one of the following has occurred:

1. The 1403 stop key is pressed. (Possible operator error.)
2. A mechanical interlock, such as the print unit, is open. (Possible operator error.)
3. A forms check. When the forms-check light is on, paper feed trouble has occurred or the carriage-stop key has been pressed. The program should provide an operator message and exit from this error recovery procedure. The operator should then perform one of the following.
 - a. Correct the not-ready condition, accept the record, and allow the application program to proceed without further retries of the command, or
 - b. Correct the not-ready condition and

restart the program from a logical restart point. The logical restart point should be determined at the installation and specified to the operator.

4. End of forms. If an end-of-forms has occurred, the end-of-forms light is on and the ready light is off. To reset the printer, press the printer start key. The remaining lines of the form are then printed under program control. (Note that the start key is pressed only once.)

When a hole is then sensed in channel 1 of the carriage tape (either space to, or skip to or by, channel 1), the operation is terminated with both the end-of-forms and forms-check lights on and the ready light off. Printing does not occur for the line at which the channel-1 hole is sensed. Therefore, a carriage tape with a hole punched in channel 1 should be on the carriage. If there is no hole in channel 1, printing continues even if no forms are in the printer. If no skip-to-channel-1 command is issued, lines are printed (after the last form) until the channel-1 punch is sensed.

The program should provide an operator message and exit from this error recovery procedure when the end-of-forms indication is detected. The operator should then perform a forms runout (as just described) and satisfy the requirements of the application program.

5. Sync check. This condition can occur whenever the print chain is out of synchronism with the print circuitry. Depending upon when the sync check occurs, one of the following conditions exists.
 - a. The sync check occurred when no printing was in progress (no line was printed).
 - b. The sync check occurred during a print operation and one line was printed.
 - c. The sync check occurred during printing and two lines were printed.Provide an operator message and exit from this error recovery procedure. The operator should then:
 - d. Correct the not-ready condition (press the check-reset key and then the start key) and allow the application program to proceed without further retries of the command, or
 - e. Correct the not-ready condition (press the check-reset key and then

the start key) and restart the program from a logical point.

6. Coil-Protect Check. A condition occurred that could cause possible damage to the print-hammer coils or hammer-driver circuits. A coil-protect check resets the printer to a not-ready condition and turns off the power (+60V Ctrl) to the hammer coils. Depending upon when the coil-protect check occurs, one of the following conditions exists.
- The check occurred when no printing was in progress (no line was printed).
 - The check occurred during a print operation (one line was printed). The line may be only partially printed.
 - The check occurred during carriage motion. The carriage motion may not have been completed.
- Provide an operator message and exit from this error recovery procedure. The operator should then:
- Correct the not-ready condition (press the check-reset key and then the start key) and allow the application program to proceed without further retries of the command, or
 - Correct the not-ready condition (press the check-reset key and then the start key) and restart the program from a logical point.
7. The single-cycle key is pressed (possible operator error).

If the error persists, call the Customer Engineer.

Bus-Out Check (Sense Bit 2)

Not used.

Equipment Check (Sense Bit 3)

Equipment check indicates that a program-resettable malfunction is detected in the printer controls.

Provide an operator message and exit from this error recovery procedure. The operator should then:

- Accept the record and indicate that the application program is to proceed without further retries of the command, or
- Cause the application program to restart from a logical point.

If the error persists, call the Customer Engineer.

Data Check (Sense Bit 4)

Data check indicates that a bit pattern read from the print translator (auxiliary storage module 7) is greater than the chain set count length or is equal to 1111 1111 (FF in hexadecimal) when block data check is not in effect. Printing does not occur in the print position to which the unmatching code applies. The entire line (except for the data check position) or only a portion of the line may be printed. Therefore, the last printed line may contain erroneous data and/or an incomplete record. Data check generally indicates that auxiliary storage module 7 was improperly loaded, or that a data record code (other than blank or null) sent from program storage accesses a bit pattern, from module 7, that is greater than the chain count length.

Provide an operator message and exit from this error recovery procedure. The operator should then:

- Accept the record and indicate that the application program is to proceed without further retry of the command, or
- Cause the application program to restart from a logical point.

If the error persists, call the Customer Engineer.

Parity Check (Sense Bit 5)

Not used.

Sense Bit 6

Not used.

Channel 9 (Sense Bit 7)

The carriage brushes sensed channel 9 during the previous carriage space. Accept the record and indicate that the program is to proceed without further retries of the command. Local installation practices may indicate other action to be taken.

USE METER (1403)

The use meter for the integrated 1403 printer records time when the CPU customer meter is operating and the printer is ready and has initiated a write command.

The 1403 use meter is stopped by manual operation of the carriage space or restore keys.

RESETS (INTEGRATED 1403)

A power-on reset places the integrated 1403 in a reset state; all 1403 check circuitry is reset, and the 1403 is placed in the not-ready state. A system reset places the 1403 in the same condition as a power-on reset, except that if the 1403 is ready when the system reset is given, it remains ready after the system reset is completed.

The Disk Attachment Control (DAC) feature for the IBM System/360 Model 25 provides for the attachment of up to four IBM 2311 Disk Storage Model 1 units without the need for a separate input/output control unit. The DAC is physically entirely contained within the Model 25 processing unit.

The addition of the feature provides the flexibility of direct access storage files to the system. The IBM 1316 Disk Packs used as data files are removable and interchangeable between the 2311 drive units. Appropriate data files can be placed on the 2311s for processing each application. The file data may be read sequentially or at random as required. Previous entries may be updated on the same file with the new computed data.

The DAC simulates both a system channel and an I/O control unit between the CPU and connected 2311 units. The combination eliminates the need for the channel interface controls, thus providing the necessary data transfer rate. Operations are programmed in the same manner as for I/O devices connected to a system channel. Where applicable, the CAW, the CCWs, the CSW, and the PSW perform identical functions as assigned for channel-connected control units. The DAC is permanently assigned to channel 1 in the Model 25. It has exclusive use of this channel assignment except when the selector channel feature option is installed. In the latter case, the DAC shares operating time with other connected I/O control units. All operations are executed in burst mode with the operating device having exclusive use of the channel until the operation is completed.

The DAC provides the following functions in the system.

1. Interprets and executes channel commands for the operation of the IBM 2311 Disk Storage units.
2. Translates data as it is moved between the serial-by-bit 2311 units and the parallel-by-bit system data flow.
3. Checks the validity of information that is transferred to or from the files.
4. Furnishes operating status information to the system.

DAC OPTIONAL FEATURES

FILE SCAN

The File Scan feature provides for an automatic, rapid search of the file for specific stated argument conditions. See the File Scan Feature section for a detailed description of the feature.

IBM 2311 DISK STORAGE

The IBM 2311 Disk Storage consists of two main components: the 2311 Disk Storage Drive and the IBM 1316 Disk Pack.

STORAGE MEDIUM (1316 DISK PACK)

Each disk pack consists of six 14-inch disks, mounted one-half inch apart on a central hub. Data is recorded on the inside ten disk surfaces. The two outer surfaces are covered by protective plates. The entire assembly of disks, hub, and protective plates rotates at 2,400 revolutions per minute (25ms per revolution). Each disk pack weighs about ten pound.

The two-piece plastic cover is designed to protect disks against damage. A built-in handle on the top cover makes carrying easy and efficient. A self-locking device in the handle permits removal of the top cover only when the pack is mounted on the disk storage drive.

The IBM 2311 Disk Storage Drive, with IBM 1316 Disk Packs, offers processing features that answer the needs of many data processing applications:

Storage capacity:

7.25 million bytes per disk pack.

High-speed accessibility:

75 milliseconds, average.

Data file removability:

Disk pack change time is about one minute.

Fast data transfer to the processor:

156,000 bytes per second.

Multiple unit growth potentials:
Up to four 2311s with 29 million bytes,
through the DAC control unit.

Compatibility between units:
1316s compatible between any 2311s used
on IBM System/360.

Large volume of data available at a single
access:
Over 36,000 bytes per cylinder.

ACCESS MECHANISM

When the 1316 disk pack is mounted in the
2311 disk storage drive, information is
written on and read from the ten disk
surfaces by magnetic read/write heads.
These read/write heads are mounted in pairs
between each two disks on a movable
comb-like access mechanism. When in
operation, the read-write heads float over
the disk surfaces on a thin film of air.

ACCESS TIME

Cylinder-to-cylinder (horizontal) access
time varies according to the number of
cylinders traversed. Access time from a
cylinder to an adjacent cylinder is 25ms.
Maximum access time (from cylinder 202 to
cylinder 000) is 135ms, and the average
time for random access is approximately
75ms (Figure 12).

Once the access mechanism has reached a
cylinder position, additional time is
required for disk rotation to the desired
record. At 2,400 revolutions per minute,
rotation time is 25ms, and one-half
revolution (12.5ms) is the average
rotational delay.

Because the access mechanism includes
one read/write head for each disk surface,
no vertical access motion is required.

Figure 12 shows the approximate times
for access mechanism movement in either
direction, excluding rotational delay.

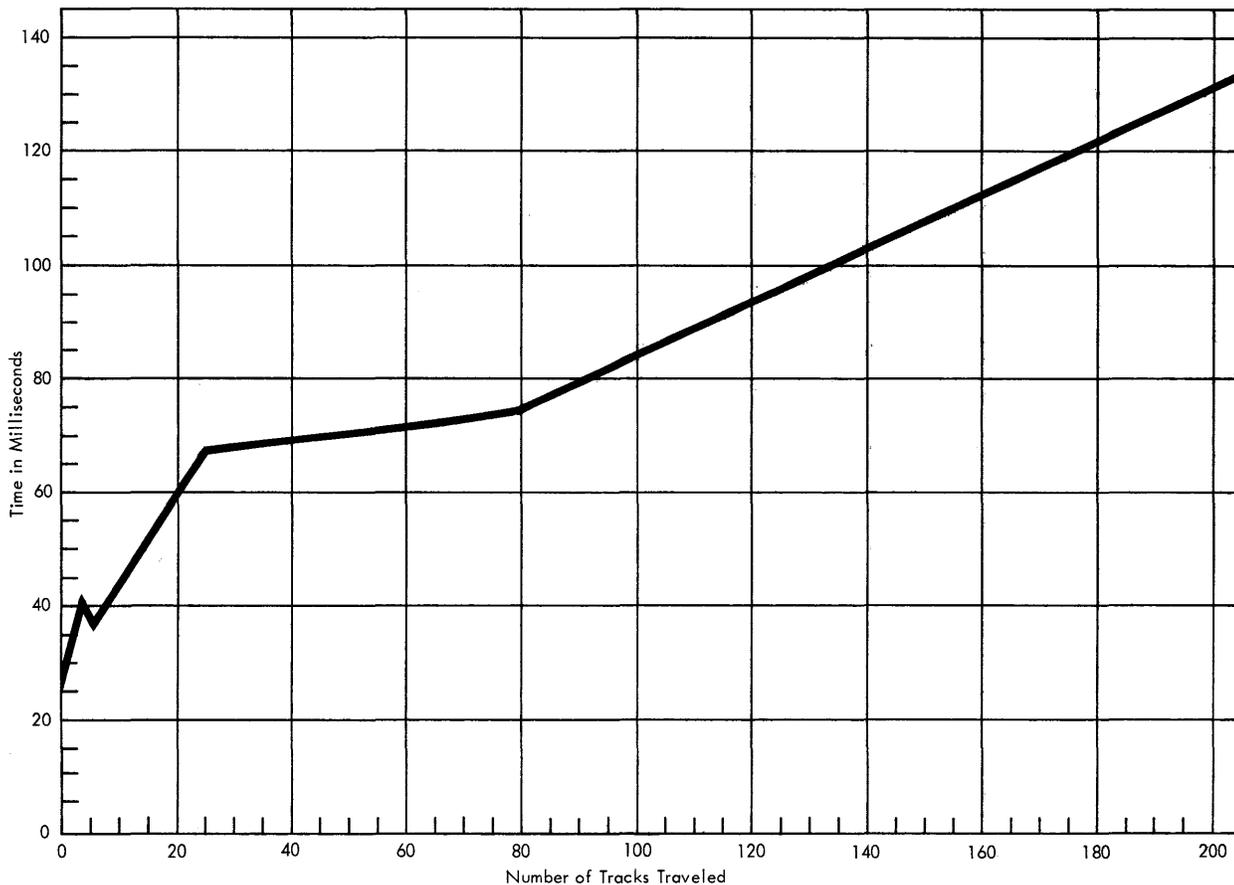


Figure 12. IBM 2311 Access Times

This may be used as an aid in programming for the most efficient utilization of the storage unit.

DATA RECORD ADDRESSING

As the access mechanism moves horizontally, it can be stop at any of the 203 positions. This provides 203 data tracks on each surface. Because all ten read/write heads are moved by a single access mechanism, a cylinder of ten data tracks is available at each access mechanism position.

The entire disk pack consists of 203 concentric cylinders of information. The numbering is from 000 (outermost cylinder) to 202 (innermost cylinder). Tracks in cylinders 200 through 202 are alternate tracks that can be used if any of tracks 000 through 199 become defective.

The address of an individual track in a specific disk module location consists of the cylinder number and the read/write head number.

DATA STORAGE CAPACITY

If IBM Programming Systems are not used, the first record on each track (R0) may contain application data.

Based on 200 tracks, with all records used for application data, a single IBM 1316 Disk Pack can contain over 7.3 million bytes, or over 14.7 million packed decimal digits.

IBM Programming Systems reserves the use of the first record on each track (record R0) to store various information about the track. This information is used by the Programming System and no application data is included. Using this format, based on 200 tracks, each 1316 disk pack can contain 7.25 million bytes, or 14.5 million packed decimal digits. Record R1 is the first application data record, and if R1 is the only data record on the track, it may contain up to 3625 bytes of information.

With the high-density recording techniques used in the 2311, minute contamination particles can effect data reading and writing and may cause loss of bits. Therefore, 203 tracks per disk surface are provided to ensure that the stated capacity, based on 200 tracks, is maintained for the life of the disk pack.

Because each data record has non-data components, such as Count Area and Gaps, track capacity for data storage varies with record design. As the number of separate records on a track increases, additional byte positions are used by gaps so that data capacity is reduced.

DATA FORMAT

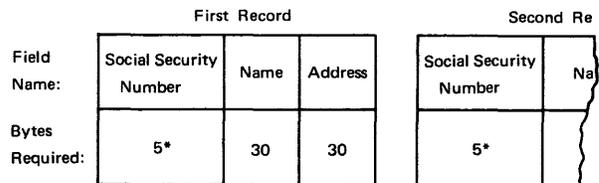
The basic unit of information representation in System/360 is the byte. A byte is made up of eight information bits and, in many devices, a parity bit for checking purposes.

The eight bits of each byte can each be set on (value of 1) or off (value of 0) to represent any one of 256 combinations.

The bit pattern in a byte can represent:

1. A single alphabetic, special, or numerical character in zoned format. (Bits 0 through 3 of the low-order byte in a zoned-format numerical field carry the sign of the field.)
2. Two packed-decimal digits. (The sign of a packed-decimal field is carried in bits 4 through 7 of the low-order byte.)
3. Part of a fixed-point or floating-point number.
4. Special information (such as status), where the value of each bit in the byte specifies the presence or absence of a particular condition.

A group of related bytes is a field; a series of related fields is a record; and a series of similar records is a logical file (Figure 13 The application determines which of the many possible ways records and logical files are to be organized. Further descriptions about System/360 information formats are in IBM System/360 Principles of Operation.



* Two Digits per Byte (Packed Format).

Figure 13. Records and Fields within a File

Information Transfer

Information is transferred one byte at a time between the CPU and the DAC.

Nine bit lines are provided to transfer a byte with parity between the CPU and the DAC. Nine bits (each set to a value of either zero or one) are transferred simultaneously (in parallel) between the CPU and the DAC. This transfer method is called parallel-by-bit.

Information is transferred between the DAC and a disk module serial-by-bit. The parity bit is not transferred to the disk pack. Instead, cyclic checking is used. Cyclic-check bytes are written with the data and checked when the data is read. (See Cyclic Checking.)

The DAC converts information from parallel-by-bit to serial-by-bit or from serial-by-bit to parallel-by-bit (Figure 14).

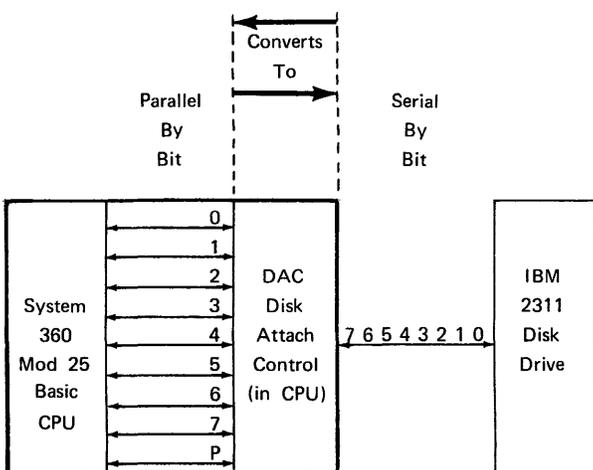


Figure 14. Data-Transfer Methods

Cyclic Checking

In the 2311, data is stored into and retrieved from areas that contain one or more fields. Capacity is more effectively used by associating 16 check bits (in two cyclic-check bytes) with each area, rather than one bit with each byte (Figure 15).

When data is transferred from the CPU to a disk pack, DAC removes the parity bit from each byte. The DAC then computes two cyclic-check bytes that are placed at the end of each area. The cyclic-check bytes are arithmetically coded from the

information to be placed in the associated area. Subsequently, when the area is read from the disk pack, the DAC recomputes the check information and compares it to the check bytes read from the associated area. Because the cyclic-check bytes are at the end of each area, the DAC cannot complete the check until the entire area is read.

With cyclic checking, the following types of errors can be detected.

1. Any error (i.e., dropping or picking up any number of bits) occurring within any 16-bit span.
2. All errors involving picking up or dropping any odd number of bits over any span.
3. Most errors involving an even number of bits over a span greater than 16 bits. If, however, two bits are dropped or picked up at 16, 32, 64, ... 16n (where n is an integer) increments, the error is not detected. This condition is rare.

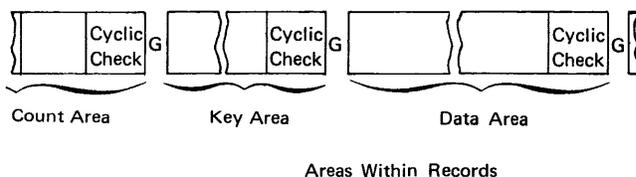


Figure 15. Cyclic-Check Bytes

TRACK FORMAT

A track is the smallest physically addressable recording area. Each track has a unique physical address. One or more records are written on a track, along with an area containing the physical address of the track. A track consists of the following area and records.

<u>Name</u>	<u>Symbol</u>
Home address	HA
Record zero	R0
Record 1	R1
Record 2	R2
Record 3	R3
Record n	Rn

The number of records that can be recorded on a track is a function of the record size and the characteristics of the 2311 disk storage unit. The schematic representation of a track is shown in Figure 16.

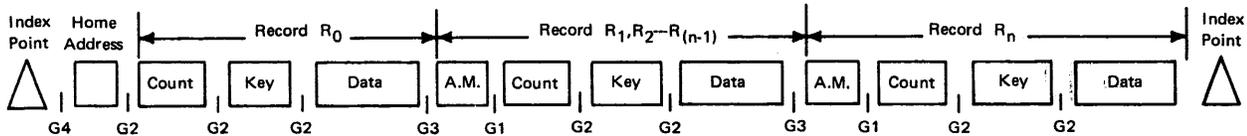


Figure 16. Track Format

Each record has a count area, a key area (use is optional), and a data area. A gap (G) separates each area.

Gaps

A gap is a string of one or more bytes written by the DAC to separate areas within a record. The length of the G1, G2, and G4 gaps is fixed. The length of the G3 gap varies with the combined length of the key area and the data area. Gaps are written by the DAC and not accessible to, or under control of, the system. There is no G3 gap after the last record on a track.

The gap configuration depends on the gap type. The G1 gap is always one byte. The G2 gap is always 18 bytes. The G4 gap is always 36 bytes. The G3 gap is variable and is computed by DAC circuitry. The length of G3 can be computed approximately by the formula:
 $G3 \text{ (bytes)} = 27 + .049 (KL + DL)$.

The factor 27 represents a correction for amplifier recovery time, geometric properties of the read/write elements, DAC-to-system turnaround time, surface velocity variations, oscillator drift, etc. for the 2311 disk storage unit. Some examples of the length of the G3 gap for representative cases are shown here.

<u>DL + KL</u>	<u>G3 Gap (Bytes)</u>
0 - 20	27
21 - 40	28
41 - 61	29

62 - 81	30
82 - 102	31
103 - 122	32
123 - 143	33
144 - 163	34
164 - 184	35
185 - 204	36
205 - 225	37
226 - 245	38
246 - 266	39
267 - 286	40
287 - 307	41
308 - 327	42
328 - 348	43
349 - 368	44
369 - 389	45
390 - 409	46
410 - 430	47
431 - 450	48
451 - 471	49
472 - 491	50

Index Marker

The beginning of a track is signaled with the index marker (index point) is detected. All tracks on a disk pack are synchronized by the same index marker. No index indication appears on individual record.

Many illustrations in this publication show an index marker at the beginning of a track. Note, however, that there is only one index marker per disk pack. The marker is automatically recognized by a special sensing device, and its detection does not depend upon any read/write head reading operation. The index-marker detection is followed by a G4 gap of 36 bytes.

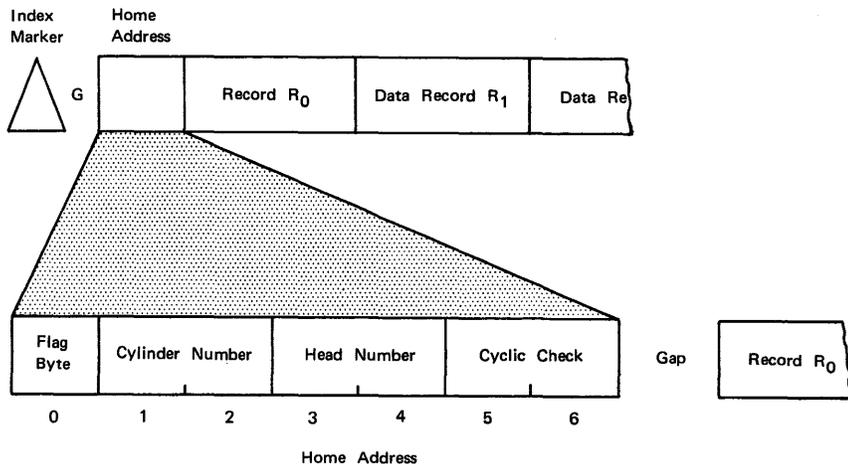


Figure 17. Home Address

Home Address (Seven Bytes)

The home address is the first information area on a track following index detection. The seven-byte home address defines the condition and location of the track (Figure 17). There is one home address for each track. The writing of home addresses is usually accomplished by utility programs. A home address is transferred from the CPU to the 2311 only by a write-home-address operation, and from the 2311 to the CPU only by a read-home-address operation.

Flag (One Byte)

The flag byte in the home address indicates the track condition. Normally, all eight bits of the flag byte are set to zero when the home address is first written. Bit significance is:

Flag Byte	Bit	Function or Setting
0		Zero
1		Zero
2		Zero
3		Zero
4		Zero
5		Zero
6		Track Condition: 0 indicates operative track. 1 indicates defective track.
7		Track Use: 0 indicates primary track. 1 indicates alternate track.

The flag byte of each record on the track is generated by the DAC as each record is

written. Home address flag-byte bits 6 and 7 are duplicated into every record flag byte written on the track. When a track is defective, the normal procedure is to assign an alternate track.

The address of the alternate track is written by the programmer in the track-descriptor record (R₀) of the defective track.

If a search or read operation (other than HA or R₀) is performed on the defective track, a check condition is signaled to the channel. The program can then read the track-descriptor record (R₀) of the defective track into main storage. The address of the alternate track is obtained from this record, and a seek to the alternate track can be performed. (For further information, see Suggested Error Recovery Procedures--byte 0, bit 6, Track Condition Check.)

A track that has both bits 6 and 7 of the flag byte set to 1 (i.e., 11) is defective.

Cylinder Number (Two Bytes)

The cylinder number (two bytes) identifies the cylinder within which data is stored. All bits in byte 1 of the home address (high-order byte of cylinder number) must be set to zero. Byte 2 is set to one of the values in the range of zero to 202.

Read/Write Head Number (Two Bytes)

The read/write head number (two bytes) specifies a particular read/write head. All bits in byte 3 of the home address (high-order byte of head number) must be set to zero. Byte 4 is set to one of the values in the range zero to 9.

The combination of cylinder and read/write head numbers is used to locate a specific track.

Note that no disk module address is used in any record. The module address is derived from the program instruction used to initiate the I/O operation. (See Input/Output Operations.)

Cyclic Check (Two Bytes)

Two bytes of cyclic-check information are appended to the home address. These bytes are used for error detection. (See Cyclic Checking.)

Gap

The home address field is followed by a G2 gap of 18 bytes.

Track-Descriptor Record (R0)

The first record (Figure 18) following the home address on each track is R0, the track-descriptor record. Although R0 can be used to store data, this practice is discouraged, because R0 is designed to enable the entire contents of a track to be moved to alternate tracks if a portion of the primary track becomes defective. A primary track is the original track on which data is stored. An alternate track contains data that has been repositioned from a defective primary track. This repositioning is independent of the file organization scheme used. R0 is not preceded by an address marker as are other data records on the track.

Count Area (Eleven Bytes)

The 11-byte count area is composed of the flag, cylinder number, read/write head number, record number, key length, data length, and cyclic-check bytes.

Flag (One Byte): Byte 0 of the count area is generated by the DAC as R0 is written. Bit significance is as follows.

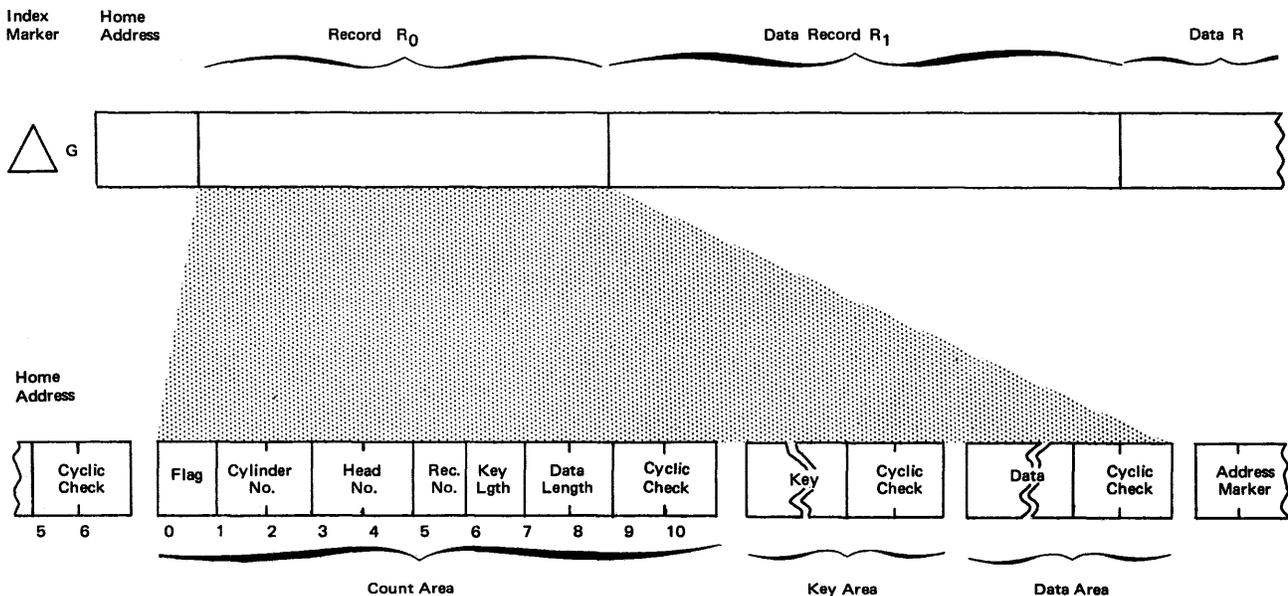


Figure 18. Track Descriptor Record (R0)

Flag Byte Bit	Function or Setting
0	Zero
1	Zero
2	Zero
3	Zero
4	Zero
5	Zero
6	Track Condition: 0 indicates operative track. 1 indicates defective track.
7	Track Use: 0 indicates primary track. 1 indicates alternate track.

The DAC causes bits 6 and 7 of flag bytes for all records written on a track to be set to the values of the corresponding bits in the home-address flag byte.

Record Identifier (Five Bytes): The ID (record identifier) is composed of the cylinder number, read/write head number, and record number bytes. In search ID operations, the ID of any record on a track (including R0) may be examined quickly enough to read the following key and data areas of that record without using a disk revolution.

Cylinder Number (Two Bytes): Bytes 1 and 2 of R0 contain the cylinder number of the track on which R0 is written. Byte 1 is set to zero; byte 2 is set to one of the values in the range zero to 202. In IBM programming systems, if the track is defective, the cylinder number of the alternate track is placed in these two bytes of R0 of the defective track. The cylinder number of the defective track is placed in the cylinder-number bytes of R0 of the alternate track. This arrangement provides a reference between the defective and alternate tracks.

Read/Write Head Number (Two Bytes): Bytes 3 and 4 contain the read/write head number for the disk surface on which the record is stored. Byte 3 is set to zero, and byte 4 can have a value in the range zero to 9. In IBM programming systems, if the track is defective, the head number of the alternate track is placed in these two bytes of R0 of the defective track. The head number of the defective track is placed in the head-number bytes of R0 of the alternate track.

Record Number (One Byte): Byte 5 of the count area designates the sequential number of the record on the track. For R0 the record number is zero.

Key Length (One Byte): Byte 6 specifies the number of bytes in the key area of the record (excluding cyclic-check bytes). If the record has no key, byte 6 is set to all

zeros. Byte 6 can indicate a key length from zero to 255. Because of its intended use with alternate track procedures, R0 normally has no key area.

Data Length (Two Bytes): Bytes 7 and 8 specify the number of bytes in the data area of R0 (excluding cyclic-check bytes).

A data length of zero indicates the end of a logical file. The DAC sends special indications to the CPU when an end-of-file record is read or written.

In IBM programming systems, the data length in R0 is set to eight. Hence, end-of-file does not occur when R0 is read.

Cyclic Check (Two Bytes): Bytes 9 and 10 are used for error detection as described in Cyclic Checking.

Gap: The count field is followed by G2 gap of 18 bytes.

Key Area (1 to 255 Bytes)

The length of the key area is recorded in the key-length byte of the R0 count area. Standard use of R0 by IBM programming systems does not include a key area. No additional gap is used when the field is omitted.

A more detailed description of key area can be found in the Key Area subsection of the Data Records (R1-Rn) section of this manual.

Data Area

IBM programming systems use this area of R0 to record the identifier of the last record on the track and the number of bytes still available for writing new records. The data field is followed by a G3 gap except when it is the last field of the track.

Data Records (R1-Rn)

One or more data records (Figure 19) can follow R0 on a track. Each record has a count area that is used to designate the track address, record number, and length of the key and data areas of the record. Because of this identification method, file organization can make use of variable-length records.

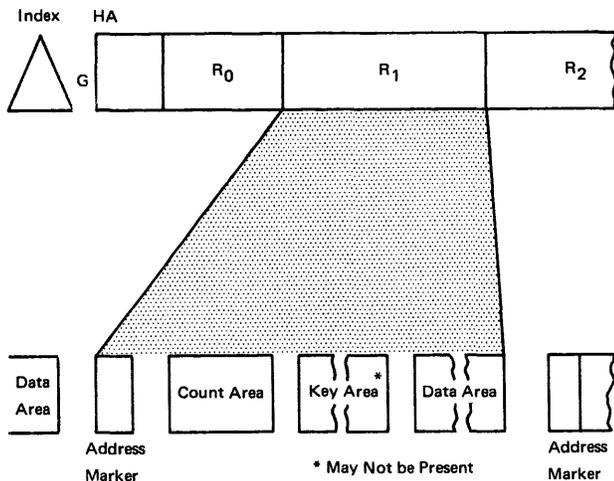


Figure 19. Record R1-Rn Format

Address Marker

This area (Figure 20) indicates the beginning of each record, except R0, which has no associated address marker. Address markers are supplied by the DAC as records are written. This area contains a bit configuration that can be detected by the DAC as the area preceding a count field of record R1-Rn. The address marker field is followed by a G1 gap of 1 byte.

Count Area (Eleven Bytes)

This 11-byte area (Figure 20) is composed of the flag, cylinder number, read/write head number, record number, key length, data length, and two cyclic-check bytes. Bytes 1 through 8 (i.e., not the flag or cyclic-check bytes) are developed in CPU main storage by the program used to write the record. As in R0, the ID (identifier) of a record is the cylinder number, read/write head number, and record number bytes of the count area.

Flag (One Byte): Byte 0 of the count area is generated by the DAC as each record is written on a track. This byte is not sent from the CPU. Bit significance in the flag byte is:

Bit Function or Setting

- | | |
|---|--|
| 0 | 0 for even records (i.e., R0, R2, R4, etc). 1 for odd records (i.e., R1, R3, R5, etc). This bit is used by the DAC when reading adjacent records (command chaining) to ensure that no single record is missed. The DAC signals a missing address marker (sense information) when two consecutive, identical bits are encountered (unless an index point intervenes). |
| 1 | Zero (must always be zero for 2841 compatibility) |
| 2 | Zero |
| 3 | Zero |
| 4 | Zero |
| 5 | Zero |
| 6 | Track Condition: 0 indicates operative track. 1 indicates defective track. |
| 7 | Track Use: 0 indicates primary track. 1 indicates alternate track. |

Bits 6 and 7 are set to the values of the corresponding bits in the home-address flag byte as each record is written on the track. The DAC forms this operation.

Cylinder Number (Two Bytes): Bytes 1 and 2 contain the cylinder number in which the record is stored. Byte 1 is set to zero, and byte 2 can have a value in the range of zero to 202.

Read/Write Head Number (Two Bytes): Bytes 3 and 4 contain the read/write head number for the disk surface on which the record is stored. Byte 3 is set to zero, and byte 4 can have a value in the range of 0 to 9.

Record Number (One Byte): Byte 5 designates the sequential number of the record on the track. The values represented by this byte can be from 1 to 255. (R0 has a record number of zero.)

Key Length (One Byte): Byte 6 specifies the number of bytes in the key area of the record (excluding cyclic-check bytes). If the record has no key, the key length is zero. The key-area length values represented by this byte can be from 0 to 255.

Data Length (Two Bytes): Bytes 7 and 8 specify the number of bytes (excluding cyclic-check bytes) in the data area of the record. A length (other than zero) represented by two bytes can be from 1 to track capacity.

Zero data length indicates the end of a logical file. Unit-exception status is sent to the CPU when an end-of-file record is read or written.

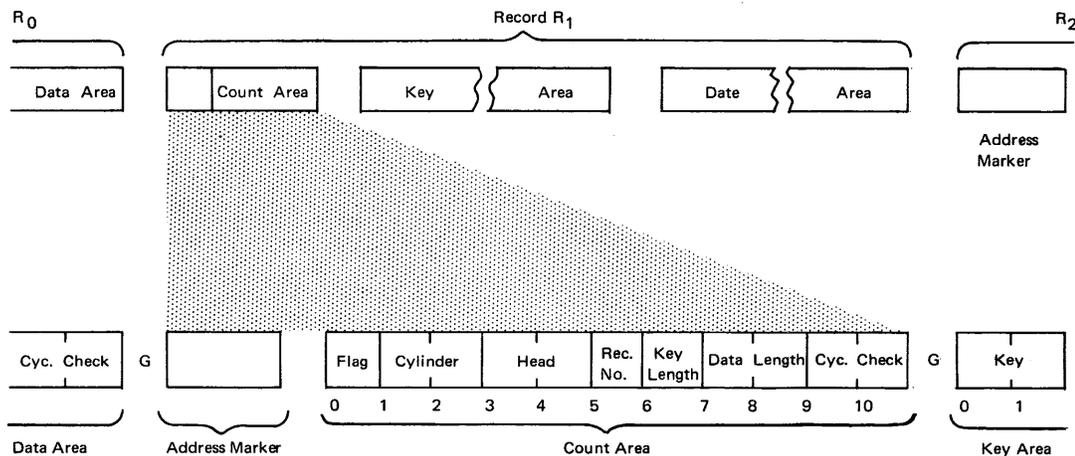


Figure 20. Address Marker and Count Area

Cyclic Check (Two Bytes): Bytes 9 and 10 are used for cyclic-checking information in the count area. (See Cyclic Checking.)

Gap: The count field is followed by a G2 gap of 18 bytes.

Key Area (1 to 255 Bytes)

The key area can contain record identifying information such as serial number, social security number, or policy number.

Commands are provided to search key areas for this identifying information. When the desired key is found, a read or write command can be issued, and the data area can be read or written during the same revolution that read the key. The data in the key area may be repeated in the data area.

For a search key operation, key information is sent from the CPU to the DAC. A comparison is then made between the key read from the track and the key in the DAC. If the comparison is made, the operation is completed. (See Search Commands.)

Key-area length ranges from 1 to 255 bytes. Two cyclic-check bytes are added to the key area by the DAC. If the key length in the count area of the record is zero, a key area is not written for that record.

When the key area is used, the cyclic-check bytes are followed by a G2 gap of 18 bytes. If the key area is omitted, no additional gap is used.

Data Area

This area contains the information identified by the count and key areas. Data information is organized and arranged by the programmer.

Two cyclic-check bytes are added to the data area by the DAC. If the data length in the count area is zero, end-of-file is indicated by unit-exception status. The data area then contains two cyclic-check bytes only. This data field is not sent from the channel when the record is read.

If the data length is zero, indicating end-of-file, the data area contains two check bytes only. The byte of zeros is not transferred to the channel when this record is read, but the end-of-file indicator is set on. In IBM programming systems, the data area of R₀ contains eight bytes (plus two cyclic-check bytes).

The data area is followed by the variable-length G3 gap as computed in the DAC except for the last record on the track. The last record has, in effect, the remaining area of the track.

RECORD CAPACITIES

Record zero can be followed by any number of records, as long as the allowable track-byte capacity is not exceeded. Because each record has some non-data areas (count fields and gaps), the net data-storage capacity of tracks varies with the number of records. With one record per track, each track has a data capacity of

Track Capacity Basis in Bytes, When R ₀ is Used as Specified By IBM Programming Systems.	Basic Track Capacity	Bytes Required by Data Records			
	When R ₀ is Used for	Data Records (except for last record)		Last Record	
	Data	Without Key	With Key	Without Key	With Key
3625	3694	61+1.049D _L	81+1.049(K _L +D _L)	D _L	20+(K _L +D _L)

Figure 21. Track-Capacity Computation

Record R ₀ used as specified by IBM Programming Systems. No application data; K _L =0; D _L =8	Number of Equal Length Records Per 2311 Track																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	Without Key	3625	1740	1131	830	651	532	447	384	334	295	263	236	213	193	177	162	149	138	127
With Key	3605	1720	1111	811	632	512	428	364	315	275	244	217	194	174	158	143	130	119	108	99

Figure 22. Equal Length Record Capacity

3625 bytes when the key length is zero. When the key area is used, the combined key and data area capacity is 3605 bytes. In these cases, it is assumed that the R₀ record is used as specified by the IBM programming systems; i.e., R₀ has no key and the data length is eight bytes.

Figure 21 shows the formulas to compute the byte requirements for additional records on the track. These formulas are shown for use with and without the key area. The last record is computed with a different formula because no G3 gap is included, and the remaining gaps and count field for one record are not included in the 3625 or 3605 byte area. The fixed numeric value in the formulas represents the bytes required for the count fields and the gaps. The 1.049 factor adjusts the key and data area lengths to include the computed G3 gap variable. The sum of the computed lengths for the records placed on a track must not exceed 3625 bytes when not using the key area, or 3605 when using the key area.

Figure 22 charts the byte size of equal length records (up to 20) that can be placed on a track. This assumes that R₀ is used as specified.

SWITCHES AND INDICATORS

Start/Stop Switch: This switch is lighted when it is in the start position.

With the 2311 properly connected in a processing system, press the switch to the start position to supply power to the disk drive motor and other 2311 components. When the disk motor has come to speed

(approximately 90 seconds), and other components are ready for operation, the read/write heads are moved into position and the access mechanism performs an automatic seek cycle.

Pressing the start/stop switch to the stop position (light out) causes the access mechanism to retract from the disk pack and removes power from the disk drive motor.

Automatic braking stops disk pack rotation in about 30 seconds.

Select Lock Indicator: When on, this light indicates a machine condition which requires Customer Engineering attention. This condition causes the disk storage drive to be disabled and stops the usage meter.

Enable/Disable Switch: When the CPU is in the stopped state, this switch enables or disables the communication of the storage drive with the CPU. It also enables or disables the usage meter.

If the CPU is running when the switch setting is changed, the storage-drive status and usage-meter status remain unchanged until the CPU is placed in the stopped state. (See also **Select Lock Indicator**.) If the switch is switched to enable while the CPU is in the wait or stopped state, a device-end is generated, just as though power had been turned on.

Ready Light: This is a green light with the drive number imprinted on it. It lights when the 2311 is up to speed and ready to access data.

The following conditions must exist before the 2311 can be in a ready state:

1. Cover closed
2. Disk pack properly installed on the drive
3. Drive motor on and up to speed.

of the CPU, the channel-interface control sequence is not required. Data, control, and status information need only be transferred between the disk-storage portion of the external storage and main storage.

ADDRESSING, DISK ATTACHMENT CONTROL

The DAC is limited to the control of four 2311 Disk Storage Drives connected directly to the control unit interface in the CPU. No additional 2311s can be attached to the system through the channel because of the data transfer rate of the channel. The 16 address bits developed from the I/O instruction identify the DAC and the disk drive for the operation.

The program views the disk attachment as if it is a channel with an attached control unit and disk drives. The sixteen bits of the I/O address are assigned as follows.

Channel Number (Bits 16 to 23)

01 Hex (Channel 1)

Control-Unit Number (Bits 24 to 27)

0-F Hex (Assigned at Installation)

Bit 28 set to 0 for system compatibility

Device Number (Bits 29 to 31)

000 Unit 1
001 Unit 2
010 Unit 3
011 Unit 4.

If less than the full complement of 2311s are installed, the units may be assigned any of the four addresses at installation. Use of any of the remaining addresses in programming results in the presentation of the Intervention Required status.

DISK-STORAGE OPERATION

Before reading or writing data on the disk storage can take place, the access mechanism (head array) must be addressed with a seek command to select the desired track. If the mechanism is not addressed, the address from the last-addressed track reads out to compare with the address from the new data commands and is signaled as an error. When the next record is located on the same track, the addressing is not required.

Disk storage uses the standard System/360 channel instructions and commands. The disk attachment control (DAC) simulates the channel and the control unit. Because the DAC is an integral part

The complex format of the storage requires the use of several commands in a command-chain sequence to search for the record and then process it. The transfer-in-channel command and the status-modifier bit allow the search commands to loop until the correct record is found and then proceed with the commands for data movement. A variety of commands and command sequences (chains) can be used with the 2311. This section is a brief, general description of operations basic to most 2311 programs. Detailed information regarding use of specific commands and handling of unusual conditions is presented in other sections of this manual.

Disk initialization, consisting of writing the home address and record R0, must be performed before a disk pack can be used for application data. If any defective tracks are found, they must be flagged, and alternate tracks must be assigned. Also, if the disk pack contains an IPL (initial program load) record, that record must be placed on the pack at track zero in cylinder zero.

Generally, 2311 operations (whether for initialization or for application runs) include the following two steps.

1. First, a set file mask command is issued. This command transfers a file mask used to prevent execution of commands that should not operate on the file area accessed. For example, the file mask can be set up to prevent execution of all write commands.
2. Next, a seek operation is performed to access the desired disk pack area. A specific track and cylinder can be accessed through use of the seek or seek-cylinder command (in the DAC these two commands perform the same function). A specific read/write head (within the currently selected cylinder) can be accessed by the seek/head command.

An operation that does not require a search (such as a write home address command) can now be executed as long as it is permitted by the file mask. If, however, a specific record must be found, some type of search must be performed first.

If an equal comparison is not obtained for any ID on the track, the search can be programmed to continue to the next track.

(This operation can be performed through a new seek to the next track or through use of the multiple/track mode. (See Multiple Track Operation for further details.) A no-record-found sense indication is available in the DAC if the ID cannot be found on the track (non-multiple-track mode operation). The unit-check status bit is set on in the CSW when a no-record-found condition occurs. Subsequent inspection of the sense information (placed in main storage via a sense command) would indicate that the no-record-found condition exists.

INPUT/OUTPUT INSTRUCTIONS, DAC

Four input/output channel instructions are used to initiate operations or to test the disk attachment control.

Start I/O

This instruction initiates all disk storage operations. After the initial setup, a sequence of chained channel commands is

transferred to the DAC from stored CCWs. The commands are listed under Operation Commands, DAC.

Test I/O

This instruction is used to determine the status of a 2311 unit or the DAC. The execution of a Test I/O causes the appropriate condition code to be set. If condition code 1 is set, a status byte has been transmitted to the CPU.

If status is pending or unit-check status is not presented, outstanding sense information is not disturbed. If status is not pending and unit-check status is presented, the new sense information replaces the outstanding sense information. (See the Status Information, DAC section).

Command Type	Command Name	Hex Code	
		Single Track	Multi-Track
Control	No Operation	03	--
	Recalibrate	13	--
	Restore	17	--
	Set File Mask	1F	--
	Seek	07	--
	Seek Cylinder	0B	--
	Seek Head	1B	--
	Space Count	0F	--
Sense	Sense I/O	04	--
Read	Read Home Address	1A	9A
	Read Count	12	92
	Read Record Zero	16	96
	Read Data	06	86
	Read Key and Data	0E	8E
	Read Count, Key and Data	1E	9E
	Read IPL	02	--
Write	Write Home Address	19	--
	Write R0	15	--
	Write Count, Key and Data	1D	--
	Erase	11	--
	Write Data	05	--
	Write Key and Data	0D	--
Search	Search Home Address Equal	39	B9
	Search ID Equal	31	B1
	Search ID High	51	D1
	Search ID Equal or High	71	F1
	Search Key Equal	29	A9
	Search Key High	49	C9
	Search Key Equal or High	69	E9
	* Search Key and Data Equal	2D	AD
	* Search Key and Data High	4D	CD
	* Search Key and Data Equal or High	6D	ED

* Used with File Scan feature.

Figure 23. Disk Attachment Control Commands

Halt I/O

This instruction is used to terminate the data transfer between the DAC and the processing unit. Operation of the 2311 device continues to its normal stopping point, and the DAC presents busy status until the operation is completed. The ending status for the operation causes an interruption when the operation is over. However, no interruption occurs if the Halt I/O is given prior to the transfer of a command to the DAC.

Test Channel

This instruction requests the operating status of the DAC as a pseudo channel, or the channel itself if other devices are attached.

OPERATION COMMANDS, DAC

Figure 23 lists the channel commands recognized by the DAC for control of the attached 2311 units. These commands are presented to the DAC in the first byte of each channel command word (CCW) from the processing unit. Any other command configuration except that of the

transfer-in-channel command is considered invalid by the DAC. The search-key-data commands are also invalid when the associated special feature is not installed.

The commands are chained to execute the desired sequence of events. The transfer-in-channel command (Figure 24) is used to repeat search commands until the desired area is located. A read or write command is then given for the desired data. Each of the channel commands is acted upon in the same manner as a control unit connected to a System/360 channel. The usual status is returned after initialization and at the completion of the command. Sense information is developed for unusual conditions and is available through the sense command. The conditions that set the sense bits are discussed in the Sense Conditions, DAC section. A parity error that occurs during the transfer of the CCW causes a machine check.

TIC Command Code		
Decimal	Hexadecimal	Binary
X8	X8	XXXX1000
Positions Marked "X" Are Ignored		

Figure 24. Operation Code for TIC Command

The No-Operation (No-Op) command is the only command that is ever processed as an immediate command. There are conditions of operation when the DAC is performing automatic functions that the No-Op command cannot return the device-end status with the initial status. Commands such as Restore are not processed as immediate commands, even though they perform no operation.

The suppress-length-indication (SLI) bit must be set with commands of Restore and Recalibrate because the byte count of zero causes an incorrect-length interruption. The commands of No-Op and Space-Count may cause this interruption under some conditions (see the command descriptions).

In normal operation, a repeated search or read command continues to operate in the same track until the index point is passed twice. If bit 0 of the command code in the CCW is set to one, the DAC advances the head selection each time the index point is passed until the end of the cylinder is reached. This procedure allows a more rapid search or read sequence to be performed. The latter operation is defined as Multiple-Track (M-T) operation.

CONTROL COMMANDS

Control operations do not involve a transfer of data records between the 2311 and the CPU. However, in certain operations, control bytes are transferred between the CPU and the DAC to enable the operation to take place. These bytes are parity checked during transfer.

No Operation (No-Op) (03)

No-Op (Figure 25) causes no action at the DAC. This command is the only command that may be processed as an immediate command by the DAC. Normally, channel-end and device-end statuses are presented by the DAC at initial selection in response to a No-Op. However, when the 2311 is completing a format-write operation, and the No-Op is chained to it, this does not occur. In this latter case, zero initial status is given. Channel-end and device-end are presented to the channel after the control unit has completely erased the remainder of the track.

No-Operation Command Code		
Decimal	Hexadecimal	Binary
03	03	00000011

Figure 25. Operation Code for No-Op Command

No-Op should not be used indiscriminately because it resets orientation information in the DAC. For example, a No-Op inserted between a read-count command and a read-data command changes the operation so that the data field read is in the next record (i.e., the one after the record in which the count field is read). Also, any no-record-found (sense byte 1, bit 4) and missing-address-marker (sense byte 1, bit 6) indications are suppressed by insertion of No-Ops after search commands in command chains.

Because a No-Op CCW has a data count field of zero, the SLI flag should be on to avoid an incorrect-length check.

Recalibrate (13)

This command (Figure 26) causes the designated module access mechanism to seek to head zero and cylinder zero. Channel-end is generated about 15 milliseconds after the DAC has accepted the command. Device-end is presented to the channel when the operation is completed.

Recalibrate Command Code		
Decimal	Hexadecimal	Binary
19	13	00010011

Figure 26. Operation Code for Recalibrate Command

The file-mask setting affects the recalibrate command in the same way as it does the seek commands.

Note that recalibrate is not an immediate command (i.e., at initial selection, the DAC returns a zero-status byte if the recalibrate CCW is accepted). Therefore, the SLI flag should be on in any recalibrate CCW because the count field is zero.

Restore (17)

This 2321 data-cell command has no meaning for the 2311 device. When a Restore command is given, the DAC presents zero initial status followed immediately by final status of channel-end and device-end.

The Restore command is not an immediate command; an initial zero status byte is normally presented. Because no data transfer occurs, the SLI bit is

The Restore command is performed regardless of the state of the file-protect mask. required in the Restore CCW.

Set File Mask (1F)

Execution of the set-file-mask command (Figure 27) causes one byte of data to be transferred from main storage to the DAC.

This byte specifies the write and seek commands that the 2311 is allowed to execute (see Figure 27). If a seek or write command that violates the mask is subsequently issued (i.e., following the set file mask CCW in the same chain), that command is not executed. Unit-check is then presented to the channel by the DAC. A subsequent sense command obtains sense information with the file-protect and command-reject bits set on if the command was a write. If the command not executed was a seek, only the file-protect sense bit is set on.

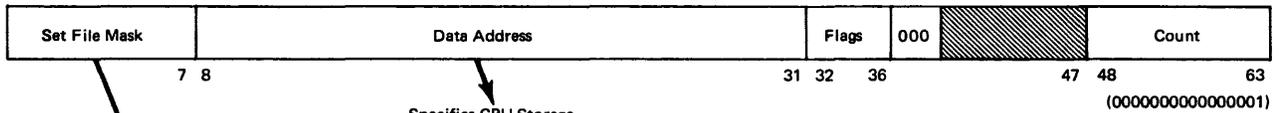
The file-protect indication takes precedence over the end-of-cylinder indication. Hence, when file-protect is detected, the end-of-cylinder sense bit is not set.

The set file mask command can be issued once at any point in a command chain. At the completion of the chain, the file mask is reset to all zeros.

A system reset (resulting from pressing the CPU system-reset key) or a selective reset (i.e., malfunction reset initiated internally by the channel to reset a unit(s) that has a malfunction) causes any file mask in the DAC to be reset to all zeros. If a Start I/O is subsequently issued, and a set file mask CCW is not in the chain then used:

- All seek commands are permitted.
- Write count-key-data, write key-data, and write-data commands are permitted.
- Write home address and write R0 are not permitted (i.e., bits 0 and 1 of the mask are set to zeros).
- Any command not controlled by the file mask is permitted.

If an attempt is made to issue a set file mask command more than once in any CCW chain, unit-check status is signaled by the DAC. A subsequent sense operation indicates command-reject and invalid-sequence.

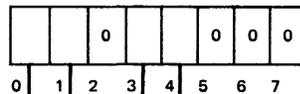


Specifies CPU Storage Location of the Mask Byte.

Set File Mask Command Code

Decimal	Hexadecimal	Binary
31	1F	0001 1111

Mask Byte



B ₀	B ₁	Permit Write Commands
0	0	All Except Write Home Address and Write Record R ₀
0	1	None
1	0	Write Data or Write Key & Data
1	1	All

B ₃	B ₄	Permit Seek Commands
0	0	All
0	1	Seek Cylinder or Seek Head
1	0	Seek Head
1	1	None

For the 2311, bits 2,5,6 and 7 of the mask must be zero. If these bits are not zero, the mask is considered to be invalid and a unit check signal is generated. A subsequent sense command indicates command reject.

Figure 27. Set File Mask Command

Seek Commands

Three seek commands (Figure 28) are used with the 2311:

1. Seek
2. Seek cylinder
3. Seek head.

After a start I/O instruction has selected the proper disk unit, a seek CCW is used to locate the proper area in the module. When necessary, and depending on the seek command used, the access mechanism in the module is moved to the specified cylinder, and the designated head is selected.

Command	Seek Command Code		
	Decimal	Hexadecimal	Binary
Seek	07	07	00000111
Seek Cylinder	11	0B	00001011
Seek Head	27	1B	00011011

Figure 28. Operation Codes for Seek Commands

Execution of a seek CCW results in transfer of a seek address from main storage to the DAC.

A seek address is composed of six bytes:
Bin Number (BB)
Byte 0 = 0

Byte 1 = 0
 Cylinder Number (CC)
 Byte 2 = 0
 Byte 3 = 0 through 202*
 Head Number (HH)
 Byte 4 = 0
 Byte 5 = 0 through 9

*A cylinder byte of 255 is used to test the detection of Seek Incomplete. While any seek address with this cylinder number results in an incomplete seek, it is not considered an invalid address by the DAC when executing a seek-cylinder operation.

Any seek address other than those outlined above is considered invalid by the DAC. Every valid seek address defines and locates only one track.

When only the head number bytes (HH) of the seek address differ, the selected tracks can be accessed without any mechanical motion of the access mechanism. Tracks with different cylinder and head numbers can be accessed by movement of the head array.

Any seek CCW count field (bit positions 48 through 63) should specify a 6-byte field. If the count is greater than six, the DAC operates on the first six bytes transferred, and, if the seek CCW SLI flag bit is zero, a wrong-length record is signaled to the CPU (i.e., incorrect length, bit 41, in the CSW is set on). If the count is less than six, the seek command is not executed, and the seek-check and command-reject sense bits are set on. In this case, unit-check, channel-end, and device-end conditions are set in the CSW.

The six bytes sent from main storage must indicate a valid cylinder and head address. If the address is not valid, the seek-check and command-reject sense bits are set on. Unit-check, channel-end, and device-end are presented.

If the seek address is valid, channel-end is presented to the channel after the address is transferred. If no mechanical motion is required, device-end is presented with channel-end. If mechanical motion is necessary, device-end is made available after the mechanical movement is completed.

If a parity error occurs during transfer of the seek address, the command is not executed. A machine-check condition results.

If the 2311 is unable to complete the seek for any other reason, the DAC presents unit-check, channel-end, and device-end. The seek-check sense bit is also set.

A seek command does not have to be preceded by any other CCW to be executed. However, see Set File Mask for the effect the file mask has on seek commands.

The three different seek commands enable restriction by the file mask and provide compatibility with other direct-access devices (see Set File Mask). For the 2311, Seek and Seek Cylinder have the same effect. Seek Head is used when the file mask permits seeks only on the cylinder where the access mechanism is already positioned.

The valid addresses are shown in Figure 29.

	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Binary	00000000	00000000	00000000	00000000 to 11001010	00000000	00000000 to 00001001
Hexadecimal Equivalent	00	00	00	00 to CA	00	00 to 09

Figure 29. Six-Byte Seek Address

Seek (07)

All six seek-address bytes referenced by the CCW are used to determine the cylinder and track to be accessed. For the 2311, bytes 0, 1, 2, and 4 must be zero.

Seek Cylinder (0B)

Only the four low-order bytes (bytes 2 through 5) referenced by the CCW are used to determine the seek address. (All six bytes must constitute a valid seek address. Bytes 0, 1, 2, and 4 must be zero.)

Seek Head (1B)

Only the two low-order bytes (bytes 4 and 5) referenced by the CCW are used to determine the seek address. (All six bytes must constitute a valid seek address.)

If the file mask is set to allow only seek-head commands, byte 3 must correspond to the cylinder at which the access mechanism is positioned. Otherwise, the command is rejected with a unit-check and command-reject.

Space Count (OF)

This command (Figure 30) provides a means of bypassing a defective area on a track to recover data immediately following on that track. This command can be used for two different situations:

1. A defective home address or record-zero area.
2. A defective count area, other than record zero.

Space Count Command Code		
Decimal	Hexadecimal	Binary
15	OF	00001111

Figure 30. Operation Code for Space-Count Command

Defective Home Address or Record R0: This situation sets unit-check and data-check, or data check, in the count field to interrupt the program. In this case, record R1 is read by the following command chain:

Space Count (SLI bit on)
Read Count Key Data.

If two successive space-count commands are followed by read CKD, record R2 is read. (If space count is the first command in a chain, it searches for index point, then counts over the home-address and record-zero areas. The function is the same if a No-Op is the first command and space-count the second command in a chain.)

Defective Count Area (Record N): This situation sets the "data check in count field" sense bit. In this case, key and data for record-N are read by the following command chain:

Read Home Address
Search ID (record N-1)
Transfer-in-Channel (to repeat search if unsuccessful)
Read Data (record N-1; Skip and SLI flag bits on)
Space Count (over record-N count area)
Read Key Data (record-N).

The space-count CCW must contain a count of three bytes and the main storage address where the record-N key length and data length are located.

The space-count address-mark search uses a less stringent address-mark test than is used by other commands. The less stringent address-mark test is an aid in recovering address marks that would normally be missing. If index-point occurs before an

address mark is found, no-record-found is set. If index-point occurs while spacing over the eleven bytes, track-overflow is set. The three bytes of data are used by the DAC for key length (the first byte) and data length (remaining two bytes) if the space-count command is followed by a read key and data, or a read data.

Command Sequence: When space count is chained from a read, search, or space-count command, it searches for the next address marker. It then spaces over the count area of that record, reading the values of the key length and data length from main storage.

If the last command in the previous chain is a read count key data (instead of read key data), record N+1 is read normally and record-N is ignored. The space-count CCW key length and data length are ignored when the next command in the chain reads the count area.

The space-count command is rejected, with invalid-sequence and command-reject bits set, if it is chained from a write command. Also, a space-count command sets the file mask so that a following write command in the same chain is rejected.

Programming Note 1: The space-count command often can be used to recover a record with a bad address marker that is missed by other commands, because a less stringent address-marker detection check is used for space-count than is used for other commands. If the sequence:

Search ID (rec n-1)
TIC *-8
Read Count, Key and Data
gives a missing-address-marker indication on the read count, key and data, and the sequence:
Search ID (rec n-1)
TIC *-8
Read data (Skip and SLI bits on)
Space count
Read count, key and data
gives no such indication, then the missing record probably can be recovered using the space-count command.

Programming Note 2: The read-data command in the preceding examples is not essential, but is desirable to reduce the probability of falsely detecting an address marker on the following space-count command, because the space-count command uses a relaxed address-marker checking scheme.

Programming Note 3: The space-count command does not itself post the missing address marker indication, but it does not prevent the missing address marker check on subsequent operations. The space-count command inverts the internally stored flag

bit 0 (when chained from Read, Search, or Space Count) from the current value to compensate for passing one address marker. When missing address marker checks are occurring and the programmer wants to suppress them, he can void the checking by inserting a No-Op after a Space Count. Be careful not to insert the No-Op before the space-count command, because this will cause the Space Count to be executed as if it were not chained from a read, search, write, or space-count command.

Programming Note 4: In a sequence such as:
(Any read or search)
Space count

Read key and data (or read data)
the key length and data length transferred to the DAC during the space count must be correct to execute the read key and data command properly. If the counts are incorrect, the DAC generally reads in gaps, etc. as though they were data, and also probably does not sync correctly in the data field.

In sequences such as:
(Any Read or Search)

Space Count
Read Count, Key and Data (or Read Count or Space Count)
the key length and data length transferred during the (first) space-count command are ignored (not used).

Programming Note 5: If HA, R0, and R1 are all defective, two space-count commands chained together can be used to recover record 2. The CCW sequence would be:

Space Count
Space Count
Read Count, Key and Data
where the first space count was not chained from a read, search, write, or space count command.

Programming Note 6: Space count is intended for use in 2311 data recovery only. Its definition may be subject to change and is not necessarily compatible with other direct-access device control units.

SENSE COMMAND (04)

The sense command (Figure 31) should be sent to the DAC whenever unit-check status is detected, even if the sense information is not to be used. The DAC sends one to six sense bytes as specified by the count (bits 48 through 63) in the sense command. The sense bytes are placed in main storage starting at the data address specified in the sense command. That is, sense byte 0 is placed in the first address byte

specified, sense byte 1 in the next higher sequential byte, etc.

Sense I/O Command Code		
Decimal	Hexadecimal	Binary
04	04	0000100

Figure 31. Operation Code for Sense Command

Sense Bytes

Unit-check status (bit 6 of the status byte) indicates that the I/O device or control unit has detected programming errors (such as invalid command sequences), equipment malfunctions, or conditions requiring operator or program intervention. The conditions causing unit-check are detailed by sense information. For the 2311, there are six sense bytes, numbered 0 through 5. The data-address portion of the sense command specifies the address in CPU main storage into which the sense bytes are to be placed. When a sense command is sent to the DAC, the sense bytes returned pertain to the module for which the unit-check occurred.

Note, however, that only sense bytes 0 and 1 have any significance to the programmer. Bytes 2 and 3 are provided to assist the Customer Engineer when he uses diagnostic programs to locate equipment malfunctions. Bytes 4 and 5 are all zeros; they are dummy bytes inserted for control-unit compatibility with other control units.

Any information in sense bytes 0, 1, and 2 is reset to all zeros whenever an initial-status byte of zero is given in response to a Test I/O instruction, or a command other than Sense or No-Op. Also, whenever another unit-check is generated, any outstanding sense information is reset and replaced by the new sense information. It is important to issue a sense command after every unit-check indication even if the sense information is of no interest. If a sense command is not executed, expected future interruptions may not occur, and some access paths may not be available.

The conditions that set the sense bits are discussed in the Sense Conditions, DAC section.

READ COMMANDS

Chaining requirement: None.

Execution of a read command results in transfer of information from the 2311 to main storage. On all read commands, the DAC checks (with the cyclic-check bytes) the validity of each area of a record as the record is read from a track. A parity bit is added to each byte as it is sent to the CPU.

If a data check is detected, the command is terminated at the end of the field in which the error occurs. The appropriate sense bits are set (i.e., data check in count field and/or data check) and unit-check, channel-end, and device-end are set in the CSW. Note that a data check is not set for the key field in a read data command. Also, data check is not set for an HA field on a read R0 command.

If an overrun is detected, the operation is terminated and unit-check, channel-end, and device-end are set in the CSW.

No read command needs to be preceded by any other CCW to be executed although read commands are normally chained from search commands. Read IPL, however, cannot be preceded by a set file mask command in the same chain.

Read Home Address (Read HA) (1A-9A)

This command (Figure 32) causes the DAC to search for the index point. Detection of the index point causes the flag, cylinder, and head bytes of home-address information to be transferred from the 2311 to CPU storage. Five bytes should be transferred, including the flag byte. If the channel count is less than five, only that number of bytes is transferred.

Read HA Command Code		
Decimal	Hexadecimal	Binary
26	1A	00011010

Read HA Command Code Multiple Track		
Decimal	Hexadecimal	Binary
154	9A	10011010

Figure 32. Read Home Address Command Codes

Read Count (12-92)

This command (Figure 33) causes bytes 1 through 8 of the count area following the next address marker to be transferred from the 2311 to main storage. The number of bytes of information to be read should always be eight. If the channel count is less than eight, only that number of bytes is transferred.

Chaining requirement: None. The count area of R0 cannot be read by a read-count command because R0 has no address marker.

Read Count Command Code		
Decimal	Hexadecimal	Binary
18	12	00010010

Read Count Command Code, Multiple-Track		
Decimal	Hexadecimal	Binary
146	92	10010010

Figure 33. Read Count Command Codes

Read Record Zero (Read R0) (16-96)

This command (Figure 34) causes the DAC to search for the index point. Detection of the index point causes the DAC to read (internally) the home address and the following gap. When these areas have been

passed, record R0 (count, key, and data) is transferred from the 2311 to main storage.

Chaining Requirement: None. A Read R0 command chained from a Search HA or Read HA is executed immediately and does not cause a search for index marker.

Read R0 Command Code		
Decimal	Hexadecimal	Binary
22	16	00010110

Read R0 Command Code Multiple-Track		
Decimal	Hexadecimal	Binary
150	96	10010110

Figure 34. Read Track-Descriptor Record (R0) Commands Codes

Read Data (06-86)

A read data command (Figure 35) transfers the data area of a record from the 2311 to main storage.

The data area to be transferred is either of the following:

1. The data area of the record following the next address marker encountered on the track.
2. The data area of a record that has been command chained from an operation on the count or key areas of the same record.

Chaining requirement: None. The data area of record 0 cannot be read by the read data command.

Read Key and Data (DE-8E)

This command (Figure 35) transfers the key and data areas of a record from the 2311 to main storage. If key length is zero, this command operates like a read-data command. The key and data areas to be transferred are from either of the following:

1. The key and data areas of the record following the next address marker encountered on the track.
2. The key and data areas of a record that has been command chained from an operation on the count area of the same record.

Chaining requirement: None. The key and data areas of record 0 cannot be read by a read key and data command.

Read Count, Key, and Data (1E-9E)

This command (Figure 35) transfers the entire record (count, key, and data) following the next address marker (AM) from the 2311 to main storage. Record 0 is bypassed because it is not preceded by an address marker.

Chaining requirement: This command is normally chained from a search for the ID of the preceding record. The count, key, and data areas of record 0 cannot be read by a read count, key, and data command.

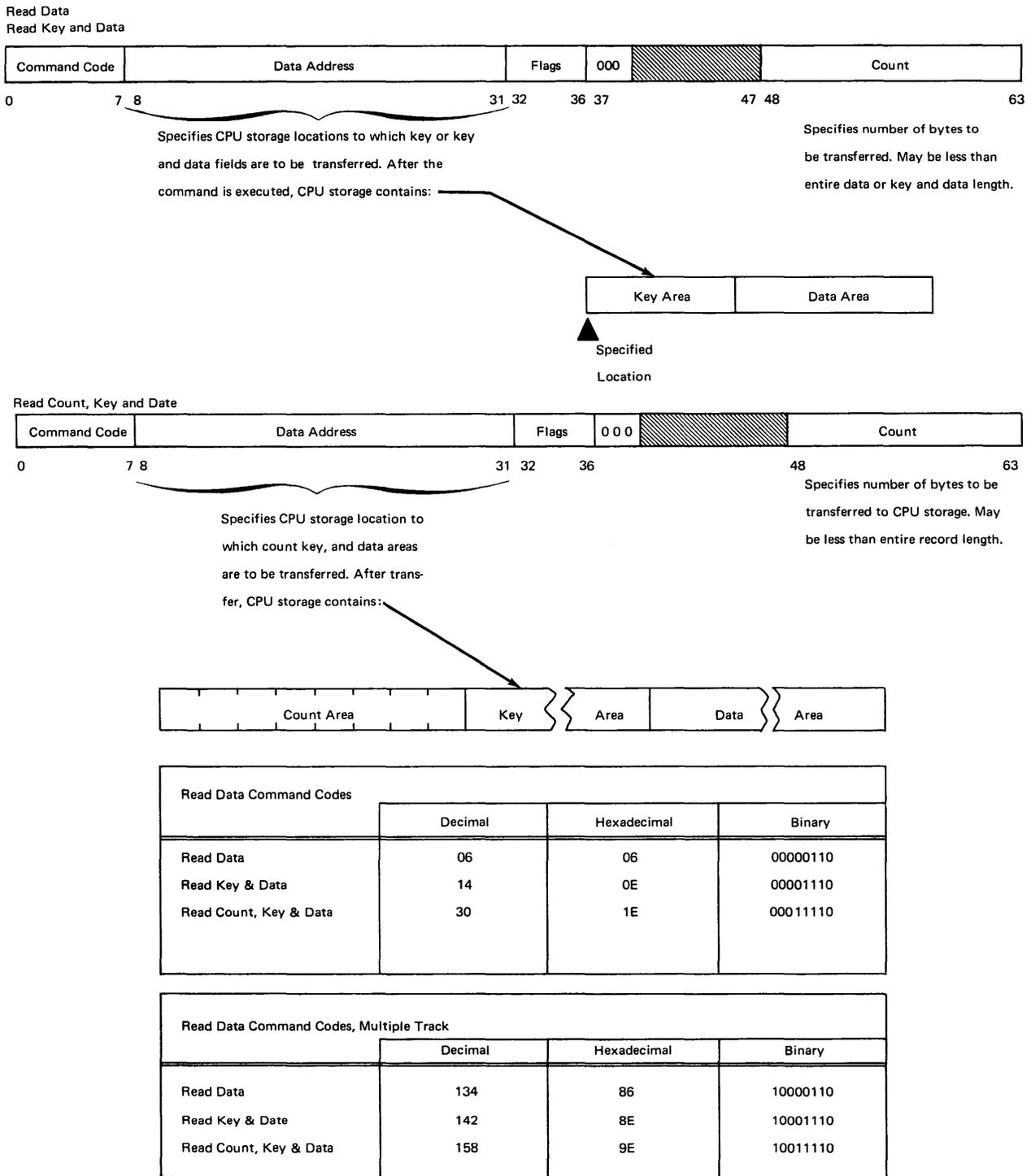


Figure 35. Read Data, Read Key Data, and Read Count Key Data Command Codes

Read IPL (Initial Program Load) (02)

The read IPL command (Figure 36) causes the addressed 2311 to seek to cylinder-0 head-0. The DAC then searches for index point. After index point is detected, the read IPL command operates as if it were a read data command. The data area to be read is in the first record after R0.

The IPL operation is initiated when the load key on the system console is pressed.

Chaining requirement: The read IPL command cannot operate on record 0. A read IPL cannot be preceded by a set file mask command in the same command chain.

Read IPL Command Code		
Decimal	Hexadecimal	Binary
02	02	0000 0010

Figure 36. Read IPL Command Code

WRITE COMMANDS

A write command is used to transfer information from CPU storage to a specified 2311. A write command is normally command chained from a successful search command to ensure that the area to be written is the correct one. If a write command is not chained from a successful search command, and invalid sequence condition is set in the CSW, and the write operation is not initiated.

The Write CCW specifies the CPU storage location of the information to be transferred and the number of bytes to be transferred. This command transfers the specified number of bytes and writes them on the addressed direct-access storage device. When the transfer is complete, the DAC generates cyclic-check bytes, appends them to the information just transferred, and signals channel-end and device-end.

If the new data area is shorter than the data area written when the track was formatted, the DAC writes valid zeros in the remainder of the data area. A data check in record areas that must be passed over but not written terminates any write command before data is written.

To verify that data was written correctly and can be retrieved correctly, a read operation is recommended after each

write operation while the original data is still available in main storage. The programmer should provide a satisfactory means for recovering from a data error if the read operation is not used after writing.

Write commands can be grouped into formatting-write commands (used to initialize tracks) and data-write commands.

Formatting-Write Commands

A format-write command is used to initialize tracks and records and to establish the lengths of the areas within each record. If a command other than a format write is command chained from a format-write command, the DAC retains the command and executes it after the track has been erased and the index marker detected.

Detection of a parity check or an overrun condition during a format-write operation causes a unit-check to be signaled to the CPU at the end of the operation. The DAC writes valid zeros from the time the overrun condition is detected until the end of the record.

Write Home Address [Write HA (19)]

This command causes the DAC to search for the index marker (Figure 37). When the index marker is detected, the specified data is transferred from CPU storage to the 2311. The DAC transfers the five bytes of home-address data from the CPU and adds two bytes of cyclic check. At this point, channel-end and device-end are signaled.

If the CCW count is less than five, the DAC records valid zeros until five bytes have been written. If the CCW count is greater than five, the DAC transfers only the first five bytes of information from CPU storage. A Write HA command is normally used to establish track identity within a storage device. Each track must be initialized with a home address before a data operation involving that track can take place.

Chaining requirement: Execution of this command depends upon a correct set file mask command preceding it in the same command chain.

Write Track-Descriptor Record [Write R0 (15)]

This command transfers the specified data from CPU storage to the 2311 (Figure 38).

The first eight bytes transferred from CPU storage make up the count area. The flag byte is generated by the DAC. The remaining data is written in the key and data areas as specified by the key length and data length stated in the count area. The DAC writes the correct cyclic check at the end of each area. Channel-end and device-end are signaled after the cyclic check for the data area is written.

The CCW count field (bits 48-66) specifies the number of bytes to be transferred from CPU storage. The count should be eight (bytes) plus key length plus data length. If the CCW count specifies a shorter area than the one written when the track was formatted, the DAC fills in the remainder with valid zeros.

Chaining requirement: This command must be chained from a successful search HA or from a write HA.

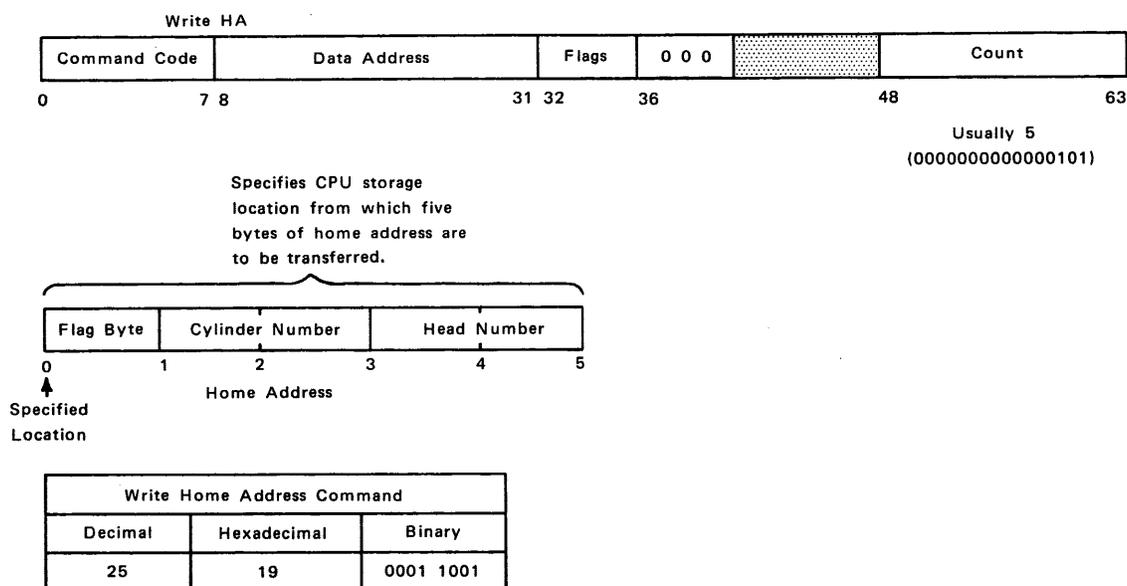


Figure 37. Write Home Address Command Code

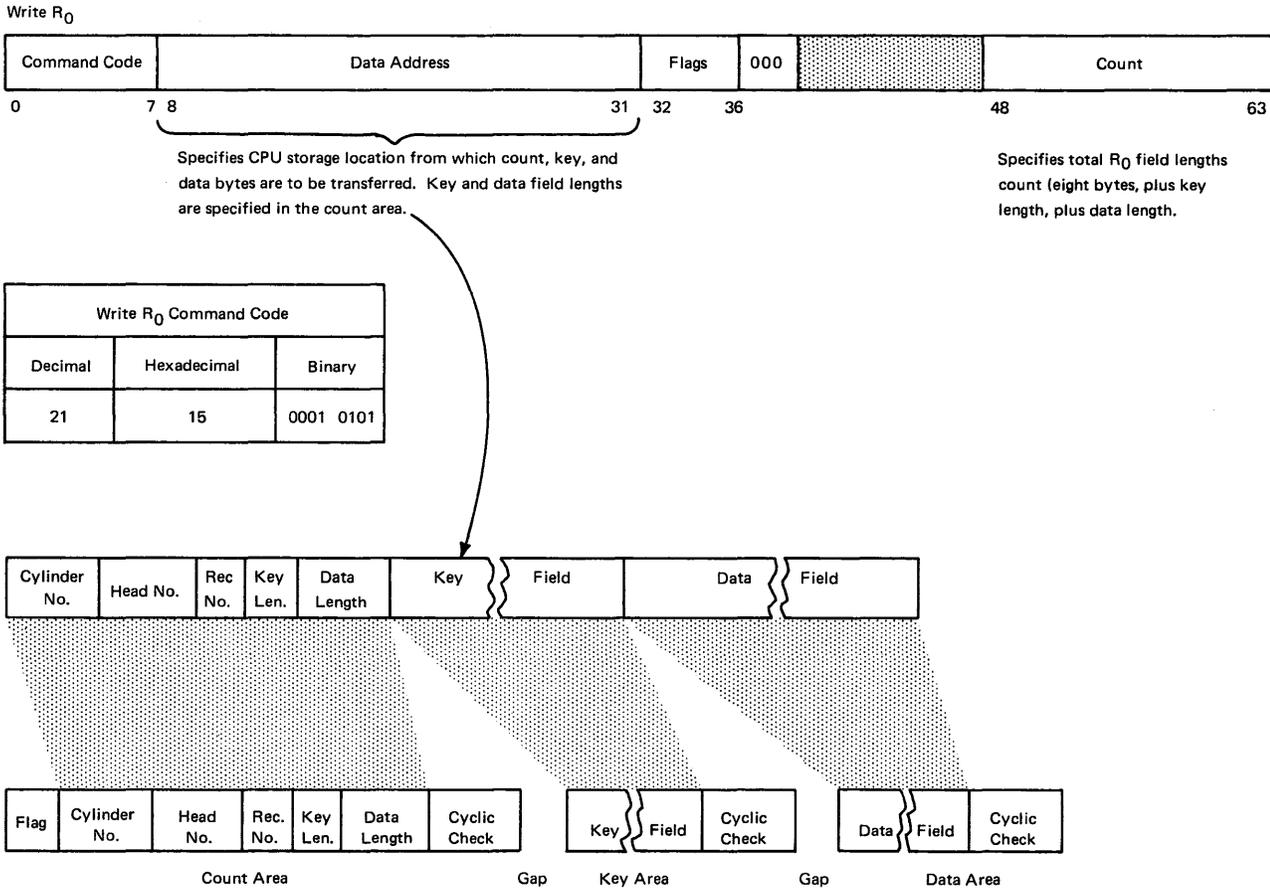


Figure 38. Write Record Zero (R₀) Command Code

Write Count, Key and Data (ID)

This command transfers the specified data from CPU storage to the 2311 (Figure 39). The DAC writes an address marker immediately before the count area.

The first eight bytes transferred from CPU storage make up the count area. The flag byte is generated by the DAC. The remaining data is written in the key and data areas as specified by the key length and data length stated in the count area. The DAC writes the correct cyclic check at the end of each area. Channel end and device end are signaled after the cyclic check for the data area is written.

The CCW count field (bits 48-63) specifies the number of bytes to be

transferred from CPU storage. The count should be eight (bytes) plus key length plus data length. If the CCW count specifies a shorter area than the one written when the track was formatted, the DAC fills in the remainder with valid zeros.

Chaining requirement: This command must be chained from a successful Search Equal Identifier or Search Equal Key command, or from a Write R₀ or another Write Count, Key and Data command. The search must not be a truncated search, or one in which the CCW count is less than the length of the area. A Read Data or a Read Key and Data CCW may be inserted between a Search CCW and a Write Count, Key and Data CCW.

Write Count, Key and Data

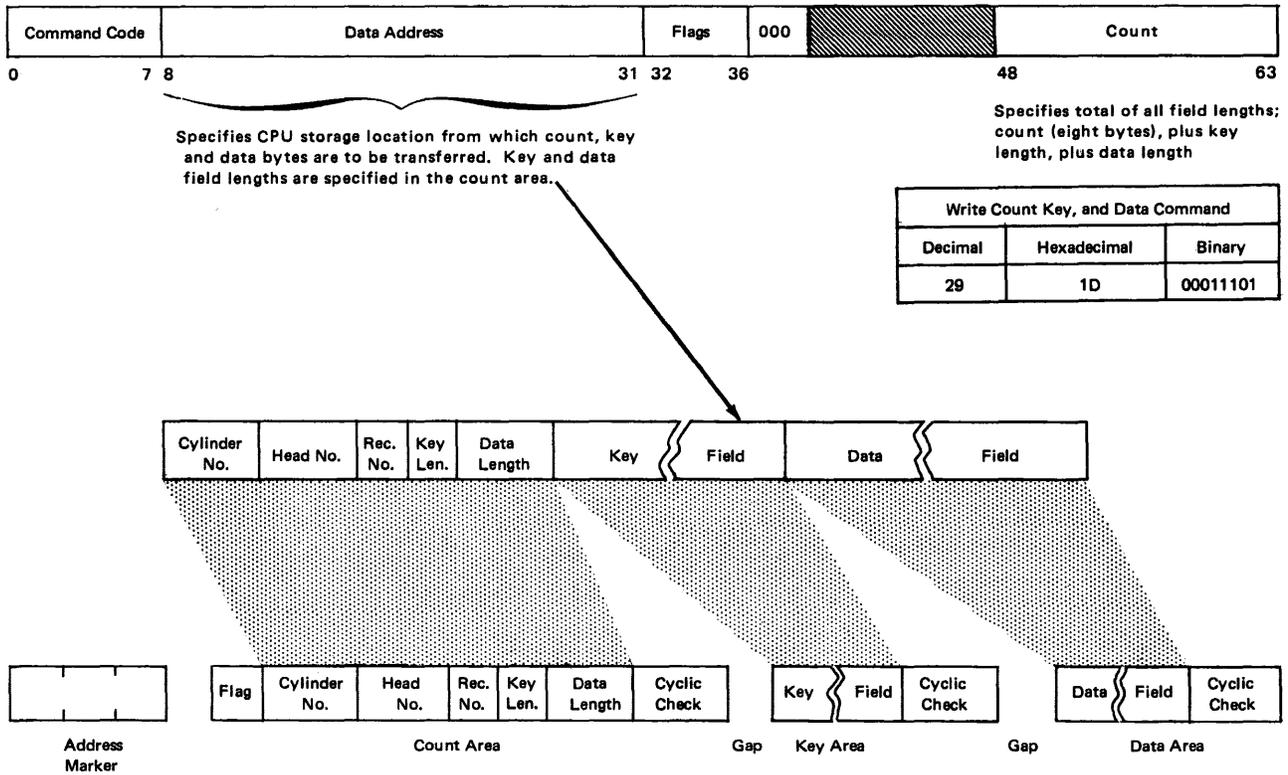


Figure 39. Write Count, Key, and Data Command Code

Erase (11)

This command is used to erase the end of a track after a track overflow has occurred (Figure 40).

Erase Command Code		
Decimal	Hexadecimal	Binary
17	11	0001 0001

Figure 40. Erase Command Code

During execution of this command, no address marks are written. Data is written on the selected storage device, but cannot be recovered.

The DAC remains busy during execution of this command.

Data-Write Commands

Chaining requirement: This command must be chained from a successful Search Equal Identifier or Search Equal Key command, or from a Write R0 or a Write Count, Key, and Data command. The search must not be a truncated search, or one in which the CCW count is less than the length of the area to be searched. A Read Data or a Read Key and Data CCW may be inserted between a Search CCW and an Erase CCW.

A data-write operation is used for normal record updating after the track has been formatted. Detection of a parity check or an overrun condition causes a unit-check to be signaled to the CSW at the completion of the command. A data check that occurs in record areas that must be passed over but not written, terminates any write command before data is written.

Write Data (05)

This command (Figure 41) transfers the specified data from CPU storage to the 2311. Writing occurs only in the data area of the record. The number of bytes to be written is specified by the Write Data CCW and may be less than the data length specified in the count area when the record was formatted. If the CCW count specifies a shorter data area than the one written when the track was formatted, the DAC fills in the remainder with valid zeros. When the number of bytes specified by the CCW has been written on the direct access storage device, the DAC appends the cyclic check and signals channel-end and device-end.

Chaining requirement: A Write Data command must be chained from a successful Search Equal Identifier command or from a Search Equal Key command. An invalid-sequence condition is signaled if the Write Data command is not properly chained. The Search command preceding the Write Data command must not be truncated.

Write Data Command Codes			
	Decimal	Hexadecimal	Binary
Write Data	05	05	00000101
Write Key & Data	13	0D	00001101

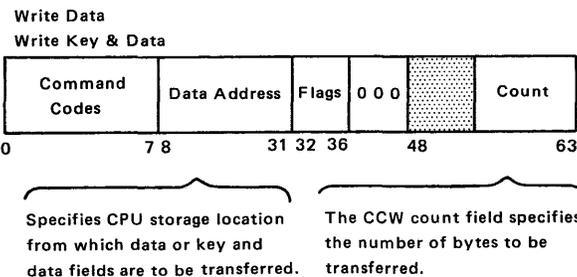


Figure 41. Write Data and Write Key and Data Command Codes

Write Key and Data (0D)

This command (Figure 37) transfers the specified data from CPU storage to the 2311. Writing occurs in the key area and data area of the record. The number of bytes to be written is specified by the Write Key and Data CCW. The lengths of the key and data areas may be less than the lengths specified in the count area when the record was formatted; the DAC fills in the remainder with valid zeros.

The number of bytes specified in the CCW count should be key length plus data length. If the record was formatted with a key length of zero, this command causes the number of bytes specified in the CCW count to be written in the data area, as in a write-data command. If a key area is needed in a record formatted without one, the record must be re-formatted.

When the number of bytes specified in the CCW has been written on the direct-access storage device, the DAC appends the cyclic check and signals channel-end and device-end.

Chaining requirement: A Write Key and Data command must be chained from a successful Search Equal Identifier command. An invalid-sequence condition is signaled to the CPU. The Search command preceding the Write Key and Data command must not be truncated.

SEARCH COMMANDS

The purpose of a Search command is to locate and identify information or areas previously written on a 2311. During a search operation, the CPU operates in a write mode, sending information from CPU storage to DAC, while the DAC operates in a read mode, accepting information from the addressed 2311. The DAC compares the information coming from the 2311 with the information coming from CPU storage. The DAC remains busy during the execution of any search command.

If the search condition is satisfied, a status-modifier indication is sent, and the next CCW in the command chain is read from a position sixteen positions higher than the current (Search) CCW. This allows modification of a command chain as a function of the data recorded on the 2311.

On all search commands, command code bit 0 determines whether this is to be a multiple-track operation; that is, whether switching to the next read/write head is the cylinder is to occur when the index marker is detected. If bit 0 is not set (0), head switching does not take place; if bit 0 is set (1), head switching does take place. If head switching has occurred, the next track is used if the search command is repeated. This allows for sequential searching of an entire cylinder by repeating the search command once for each record to be searched.

The following command chain illustrates the procedure for reading a record

identified by a key stored at location a in the CPU.

Command Chain	Function
Search Key a	Compare key with search argument.
TIC* -8	Transfer back to search.
Read Data B	Read data area if status modifier was returned from search.

Search Home Address Equal (Search HA) (39-B9)

This command (Figure 42) causes the DAC to search for the index marker, then compare four bytes of home-address data coming from CPU storage with four bytes of home-address data coming from the 2311. The flag byte is not transferred or compared during the execution of this command.

Search Home Address Equal Command Code			
	Decimal	Hexadecimal	Binary
MT Bit Off	57	39	0011 1001
MT Bit On	185	B9	1011 1001

Figure 42. Operation Codes for Search Home Address Equal Command

If a logical comparison is equal, channel-end, device-end, and status-modifier are signaled to the CPU. If the logical comparison is unequal, then channel-end and device-end are signaled.

If the CCW count is greater than four bytes, the search operation is completed when the DAC count equals zero. The DAC terminates the command with a channel-end and device-end. The status modifier is generated if the logical comparison was satisfied.

If the CCW count is less than four bytes, the logical comparison between the data coming from CPU storage and the data coming from the 2311 continues until the CCW count reaches zero. At the time the DAC count reaches zero, a channel-end and device-end are generated. A status modifier is generated if the search condition was satisfied on the short field.

If a parity check, overrun, or data check is detected, unit-check, channel-end, and device-end signals are signaled to the CPU at the completion of the command.

A Search Home Address command does not have to be preceded by any other CCW to be executed.

Search Identifier (Search ID)

Search ID commands (Figure 43) cause a comparison to be made between five bytes of data from CPU storage and the five-byte record identifier portion (Figure 44) of a count area from the 2311.

Command	Search ID Command Code		
	Decimal	Hexadecimal	Binary
Search ID Equal	49	31	00110001
Search ID High	81	51	01010001
Search ID Equal or High	113	71	01110001

Command	Search ID Multipule Track Command Code		
	Decimal	Hexadecimal	Binary
Search ID Equal	177	B1	10110001
Search ID High	209	D1	11010001
Search ID Equal or High	241	F1	11110001

Figure 43. Search ID Command Codes

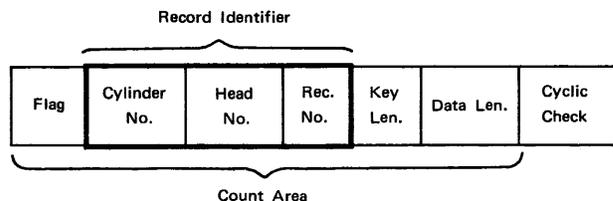


Figure 44. Identifier (ID)

If the CCW count is greater than five bytes, the search operation is completed when the DAC count equals zero. The DAC terminates the command with a channel-end and device-end. The status modifier is generated if the logical comparison was satisfied.

If the CCW count is less than five bytes, the logical comparison between the data coming from core storage and the data coming from the 2311 continues until the CCW count reaches zero. When the DAC count reaches zero, a channel-end and device-end are generated. A status modifier is generated if the search condition was satisfied on the short field.

If a parity check, overrun, or data check is detected during a search-ID operation, unit-check, channel-end, and device-end signals are generated at the completion of the command.

A Search ID command does not have to be preceded by any other CCW to be executed.

If command code bit 0 (multiple track) is 0, the search is confined to one track. It can be repeated until either the search condition is satisfied or until two index markers are sensed, at which time unit-check (no record found), channel-end, and device-end signals are generated.

If the multiple track bit is a 1, the search can be repeated until the search condition is satisfied or until the end-of-cylinder is detected. At this time a unit-check (end-of-cylinder) signal is generated.

Search ID Equal (31-B1)

This command is used to compare the ID from the 2311 with the ID from CPU storage, and indicates, when it is satisfied, that the ID from the 2311 is equal to the ID from CPU storage.

Search ID High (51-D1)

This command is used to compare the ID from the 2311 with the ID from CPU storage, and indicates, when it is satisfied, that the ID from the 2311 is higher than the ID from CPU storage.

Search ID Equal or High (71-F1)

This command is used to compare the ID from the 2311 with the ID from CPU storage, and indicates, when it is satisfied, that the ID from the 2311 is either equal to or higher than the ID from CPU storage.

Search Key

A search-key command (Figure 45) causes the DAC to compare a key area from CPU storage with a key area read from the 2311. The key to be searched is either the key of the record following the next address marker, or, if this command is chained from a

read-count or search ID command, the key searched is in the same record in which the ID is read or searched. A search-key command passes over R0 unless chained from a search ID command that has searched the ID of R0.

Command	Search Key Command Codes		
	Decimal	Hexadecimal	Binary
Search Key Equal	41	29	00101001
Search Key High	73	49	01001001
Search Key Equal or High	105	69	01101001

Command	Search Key Command Codes, Multiple Track		
	Decimal	Hexadecimal	Binary
Search Key Equal	169	A9	10101001
Search Key High	201	C9	11001001
Search Key Equal or High	233	E9	11101001

Figure 45. Search Key Command Codes

If the CCW count is greater than the key length written when the track was formatted, the search operation is terminated with the number of bytes specified by the key length in the count area transferred to the DAC. If the search has not yet been successful, the DAC then terminates the operation and signals channel-end and device-end. A status-modifier signal is sent with channel-end and device-end at any time the search is successful and the search conditions are satisfied.

If the CCW count is less than the key length written when the track was formatted, the search operation is terminated when the number of bytes specified by the CCW have been transferred to the DAC. If the search has not yet been successful, the DAC terminates the operation and signals channel-end and device-end. A status-modifier signal is sent with channel-end and device-end at any time the search is successful and the search conditions are satisfied. If an overrun condition is detected, the operation is terminated and the cause is signaled immediately. If a parity check or data check occurs, unit-check, channel-end, and device-end are signaled at the end of the area in which the error occurred.

A search-key command does not have to be preceded by any other CCW to be executed.

If the multiple-track bit is 0, the search can be confined to one track. It can be repeated until either the search condition is satisfied or until two index markers are sensed. At this time a

unit-check (for no-record-found), channel-end, and device-end are signaled. If the multiple-track bit is 1, the search can be repeated until either the search condition is satisfied or until an end-of-cylinder condition is detected.

The search-key command never returns a status modifier if the key length of the record to be searched is zero.

Search Key Equal (29-A9)

This command is used to compare the key area from the 2311 with the key area from CPU storage, and indicates, when it is satisfied, that the key area from the 2311 is equal to the key area from the CPU. If the logical comparison is unequal or if the record has no key area, only channel-end and device-end are signaled.

Search Key High (49-C9)

This command is used to compare the key area from the 2311 with the key area from CPU storage, and indicates, when it is satisfied that the key area from the 2311 is higher than the key area from the CPU. If the logical comparison is equal or low or if the record has no key area, only channel-end and device-end are signaled.

Search Key Equal or High (69-E9)

This command is used to compare the key area from the 2311 with the key area from CPU storage, and indicates, when it is satisfied, that the key area from the 2311 is either equal to or higher than the key area from the CPU. If the comparison is low or if the record has no key area, only channel-end and device-end are signaled.

STATUS INFORMATION, DAC

An understanding of the System/360 channel functions is assumed throughout this document. Only those points requiring further definition or those where the DAC has an option are discussed. When presented, status is accepted immediately.

INITIAL STATUS CONDITIONS

The initial status condition is condition code one for all immediate commands and for the Test I/O, unless one or more of the following conditions exists. If more than one condition exists, the first condition listed determines the initial-status byte to be stored in the channel status word (CSW).

1. The DAC is busy. A status byte indicating control unit busy is stored in the CSW in this case. The DAC is busy if:
 - a. Chaining is terminated and writing or erasing is still in progress on the file.
 - b. A Halt I/O has occurred and the operation is still in progress.
2. A status condition is pending in the DAC that is not specifically associated with the device (see the Status Pending in the DAC section). In this case, the pending status is presented, and the busy bit is included in the status byte if the instruction was other than a Test I/O.
3. The device is busy (unavailable). The busy bit alone appears in the status byte. (This does not apply when busy (pending status) appears with other status bits. When busy occurs with bits other than status modifier, the device is defined to be busy because of the included outstanding status. The status is cleared and the device must be readdressed to determine if it is available.)

Channel-end occurred without device-end for the device; device-end has not yet been generated.
4. Status is pending in the device. The pending status is presented and the busy bit is included if the instruction was other than Test I/O.
5. A unit-check condition exists at the device (e.g., seek-check or intervention-required). Unit-check is indicated except for the following cases:
 - a. Valid commands in the sense group (xxxx0100) are accepted so that the commands may be executed to permit sensing of the sense indicators.
 - b. A 2311 seek check. A recalibrate command is accepted so that the command may be executed.
6. The command is rejected. Unit-check occurs.

PENDING STATUS CONDITIONS

A pending status condition may exist in either the DAC or the device.

Status Pending in the DAC

Status is pending in the disk attachment control if control-unit-busy was presented and a control-unit-end has not been accepted.

Status Pending in the Device

A status condition pending in the 2311 device does not cause the device or DAC to appear busy.

The only status that can be pending in the 2311 is device-end. When unit-check occurs with device-end (and not channel-end), it is not generated until the device-end is presented on the interface. The device-end and unit-check conditions then become pending in the DAC if not accepted. Status is pending if:

1. Channel-end occurs alone for the operation. Device-end is pending.
2. The device has gone from the not-operational state to the ready state. Device-end is pending.

ADDRESS ASSOCIATED WITH PENDING STATUS

All status conditions in the DAC are associated with a specific device address, except for control-unit end. Control-unit end is associated with the DAC base address. Status can be cleared by addressing any of the 2311 devices attached to the DAC.

STATUS BYTE (CSW)

The eight bits of status information are called the status byte. The status byte contains information that reflects the status of the DAC and the selected 2311 file device attached to the DAC. The significance of each status-byte bit is as follows.

Bit Name

Notes

0	Attention	Not used
1	Status Modifier	Used with Search and control-unit busy.
2	Control-Unit End	Normal definition
3	Busy	Addressed access mechanism is moving or used in conjunction with status modifier to indicate control-unit busy.
4	Channel-End	Normal definition.
5	Device-End	Indicates that an access mechanism is free for use.
6	Unit-check	Indicates that a control-unit or programming error on file-hardware check has been detected.
7	Unit-Exception	End-of-file.

Attention (Bit 0)

Not used

Status Modifier (Bit 1)

This bit is set whenever a Search High, Search Equal, or a Search Equal-High command has been executed and the condition has been satisfied. The status-modifier is also set whenever the DAC is addressed while it is busy. This bit, in conjunction with the busy bit, signifies control unit busy.

Control Unit End (Bit 2)

This bit is set if a control-unit-busy status has already been presented and the busy condition has been terminated. It is also set with unit-check when unit-check occurs after device-end.

Busy (Bit 3)

Device Busy: The busy bit indicates that the selected device is busy. It is set when a new command chain is initiated while the selected 2311 access mechanism is still in motion (due to a previous seek command). Busy is also given in response to any command except Test I/O if there is outstanding status for the device.

Control Unit Busy: The busy bit, in conjunction with the status-modifier bit, indicates that the DAC is busy. It is set when a new command chain is initiated while the DAC is causing a track to be erased following a format-write or erase command.

Channel-End (Bit 4)

This bit is set at the end of each command.

Device-End (Bit 5)

This bit indicates that an access mechanism is free for use. After a seek or restore command, this signal is presented to the

processing unit together with the unit address to indicate a seek complete. It is generated simultaneously with channel-end at the end of all other commands. Device-end is also generated when an attached device goes from the not-ready to the ready condition.

Unit-Check (Bit 6)

This bit is set whenever an unusual or error condition is detected in the DAC or the selected file device. Sense bytes 0, 1, and 2 (see the Sense Conditions, DAC section) provide detailed information concerning the nature of the condition. Channel-end and device-end are usually presented with unit-check unless the unit-check is presented during initial selection.

	Status Byte	Sense Byte 0	Sense Byte 1	Sense Byte 2
Bit 0	Attention	Command Reject	Data Check in Count Field	Unsafe
Bit 1	Status Modifier	Intervention Required	Track Overrun	
Bit 2	Control Unit End		End-of-Cylinder	
Bit 3	Busy	Equipment Check	Invalid Sequence	Selected Status
Bit 4	Channel End	Data Check	No Record Found	Cyclic-Code Check
Bit 5	Device End	Overrun	File Protected	Unselected File Status
Bit 6	Unit Check	Track-Condition Check	Missing Address Marker	
Bit 7	Unit Exception	Seek Check		

Figure 46. Sense-Byte Summary

Unit Exception (Bit 7)

This bit indicates that an end-of-file has been detected during one of the following operations.

- Read Initial Program Load
- Read R0
- Read Count, Key and Data
- Read Key and Data
- Read Data
- Write Key and Data

Write Data
Search Key and Data.

It is not set for the following operations:

Read Count
Write Count, Key and Data
Search Key Commands
Search ID Commands.

Unit exception results from a data-length of zero. The key field (if any) is transferred.

SENSE CONDITIONS, DAC

Six bytes of sense-condition information are provided by the DAC to completely identify the setting of unit-check. These six bytes are transferred to the system by issuing a sense command (Figure 46).

Command Reject (Bit 0)

When this bit appears with the file-protected bit (bit 5, sense byte 1), the write-inhibit portion of the file mask has been violated. When it appears with invalid-sequence (bit 3, sense byte 1), then one of the following has occurred.

1. A write command has not been preceded by the necessary search or write command.*
2. A set-file-mask command has been issued in a chain in which a previous set file mask was given.*
3. Head switching is being attempted in a chain without a previous seek.
4. A space-count command has been chained from a write command.*
5. A formatting command is being attempted after R0 on a defective track.*

When command-reject occurs with seek-check (bit 7, sense byte 0), one of the following has occurred.

1. The DAC has detected an invalid seek address. No seek is initiated.
2. Less than 6 bytes of seek address were given. No seek is initiated.

When Command Reject occurs with none of the preceding items, one of the following has occurred.

1. An invalid command has been given, or a command associated with an uninstalled

- feature has been given.*
2. An invalid file mask has been given.
3. An IPL command has been given after a set file mask has been issued.*

Intervention Required (Bit 1)

This bit indicates that the specified file is:

1. Not physically attached to the system.
2. The specified file is physically attached to the system, but it is not available for use because the file motor is not on, a cover interlock is open, etc.

Bit 2

Not used.

Equipment Check (Bit 3)

This bit indicates that an unusual condition is detected in the DAC or 2311 unit. The conditions that are covered by the bit are defined in the Sense Byte 2 section.

Data Check (Bit 4)

This bit indicates that a data error has been detected in the information received from the file. Error-detection in the DAC is performed by the division of the message polynomial by a generator polynomial ($x^{16} + 1$) using mod-2 arithmetic.

The data-check bit is never set in the key field when executing a read-data command, nor is it set in HA when executing a read R0 command.

Data-check usually occurs when trying to read a record that overflows a track.

*Unit-check normally occurs alone in initial status in these cases. In most other cases, the unit-check occurs with channel-end and device-end.

Overrun (Bit 5)

This bit indicates that the DAC access to main storage was suppressed longer than allowed, or that a chained CCW was issued but it was received too late to be properly executed. Detection of an overrun during reading or writing causes an immediate stop of data transmission. During writing, the remaining portion of the record area is padded with valid zeros. During reading or searching, the indication is given as soon as it is detected.

Track Condition (Bit 6)

This bit is set whenever:

1. Any single track command other than Search HA, Read HA, or Read R0 is executed on a defective track. After seeking to a defective track, it is necessary to execute a single-track command if a track-condition interruption is desired; otherwise, none of the flag bytes on the defective track will ever be read and the interruption cannot occur.
2. Any multitrack command other than Search HA, Read HA, Read R0 switches to a defective track.
3. Any multitrack command (including Read HA, Read R0, or Search HA) attempts to switch from an alternate or defective track that has been found by the DAC to be alternate or defective. The DAC retains the alternate or defective track status only if a single track Read or Search operation has been executed on the track in the current CCW chain, and no control command other than the No-Op has been executed since the single track Read or Search command.

Seek Check (Bit 7)

This bit indicates that the file has been unable successfully to complete a seek because:

1. The transferred seek address is outside the valid address boundaries of the file. The unused bytes must contain zeros. It also sets command reject.
2. Less than six bytes of seek address are sent. It also sets command reject.

3. A hardware failure occurred resulting in the access mechanism failing to detent correctly.
4. The home address of the track does not compare with the geometric (seek) address. See the Multiple Track (M-T) operation and Flag Byte sections.

SENSE BYTE 1

Data Check in Count Field (Bit 0)

This bit indicates that a data error has been detected in a count field read from the file. Data check in sense byte 0 is also turned on. Error-detection is the same as described for data-check bit 4, byte 0. The operation is terminated at the end of the count field.

Track Overrun (Bit 1)

This bit indicates that writing has not been completed by the time the index point is detected. This type of error is created during a Write R0, Write Count, Key and Data, Write Key and Data, Write Data, or Space Count operation.

If this bad record is read with subsequent read commands, the track-overrun condition is not set. Data check is set if a data check occurs.

End-of-Cylinder (Bit 2)

This bit indicates that the CCW command chain has not been completed, but that the end-of-cylinder has been detected.

Invalid Sequence (Bit 3)

This bit indicates that an attempt has been made to execute an invalid sequence of CCWs. Invalid sequences are normally related to write operations. It also occurs if two set file mask CCWs are attempted in the same chain of CCWs, if head switching is attempted without prior seeking, or if space count is preceded by a write command. Command reject (bit 0, byte 0) is also turned on when an invalid sequence is encountered. Valid sequences are defined in the individual command descriptions.

No Record Found (Bit 4)

The no-record-found function is included in the DAC so that the programmer may use a sequence such as:

```
Search ID (Multitrack off)
TIC * - 8
Read Data
```

without the possibility of the program getting trapped in an endless loop, in case the desired record is not contained on the track being searched. The no-record-found function is implemented as follows.

1. An index-passed bit is turned on whenever index point is sensed on the file while the DAC is executing any single-track command other than a Read HA or Read R0 command.
2. The index-passed bit is turned off whenever the DAC performs a read operation in an HA or data-field area, any write command, a sense command, or any control command. The index-passed bit is also reset when chaining is broken.
3. A no-record-found condition occurs whenever the DAC senses index point while performing a single-track read or search operation other than read R0 or read HA and the index-passed bit is already on.
4. The no-record-found bit is set with missing address marker when either HA or R0 cannot be found on a track.
5. A no-record-found condition occurs while executing a space-count command under different conditions (see Space Count Command section).

The following programming notes apply.

1. Search HA posts no-record-found if two indexes are passed without satisfying the search.
2. Read Count, Key and Data, Read Key and Data, and Read Data commands reset the index-passed bit at the time the data field is read. Hence, no-record-found can occur while one of these commands is being executed; notably: no-record-found occurs when one of these commands is given and no address marker is detected on the track.
3. The programmer should ensure that spurious no-record-found conditions cannot occur. For example, in the sequence:

```
Read Count
Search Key
TIC * - 16
```

```
Search ID (of Count Field read above)
TIC * - 8
```

Read Key and Data

the index-passed bit is not reset prior to the Read Key and Data command, and index point is passed once after the key is located prior to orienting on the desired ID. If the index-passed bit is on at the time the desired key was found (this cannot be predicted if the sequence was started with random orientation), then the no-record-found condition does occur. The sequence may be corrected by inserting a Read HA or Read R0 immediately prior to the Search ID command. (This is the best method because the added command also eliminates unnecessary Search ID sequences between the located key and the end of the track.) Or No-Op may be inserted, or a Read HA or Read R0 can be included at the beginning of the sequence.

4. The index-passed bit is not reset when status-modifier is generated. If it were, the sequence:

```
Search (ID or Key) HI-EQ
TIC * +16
TIC * -16
Read Data
```

could not be used safely to locate a low record.

The no-record-found bit is set by the command sequence in the following examples (M/T bit off) if the desired record cannot be found.

1. No equal record -

```
Search Key Equal
TIC * - 8
Read Data
```
2. No high record -

```
Read HA
Read Count (RN)
Search Key High
TIC * -16
Search ID Equal (NN)
TIC * -8
Read Key and Data (RN)
```
3. No address marker on track -

```
Read Count, Key and Data
```
4. Blank track -

```
Any Search
Any Read
```
5. The following sequence using both M/T and single-track commands sets no-record-found if the search is not satisfied on the starting track.

```
Read Count, M/T off
Search Key, M/T on
TIC * -16
```

This example points out a difficulty that can occur by mixing multitrack and single-track commands.

7. One of the dc file voltages has been lost.

File Protected (Bit 5)

This bit indicates that a seek or write CCW or M/T read or search command was issued that violates the file mask (see the File Protection section). The command-reject bit also is set on by detection of this condition if a Write File Mask is violated. The file-protected bit is not posted for M/T commands that attempt to switch off defective or alternate tracks (the track-condition bit is set instead).

Bit 1, Bit 2

Not used.

Selected Status (Bit 3)

This bit indicates that microprogram decoding of file status yielded self-contradictory results.

Missing Address Marker (Bit 6)

This bit is set as follows.

1. With no record found: HA or R0 was not found by the DAC.
2. Alone: indicates that the two sequentially encountered flag bytes had identical values for bit 0. This indicates that an intervening address marker was missed. A missing address marker for the last record on the track cannot be detected by the DAC.

Cyclic-Code Check (Bit 4)

This bit indicates that the DAC circuitry used to generate and check the cyclic-code characters does not function properly.

Unselected Status (Bit 5)

This bit indicates that at least one of the file-status lines is on without any file module being selected. This indicates a file malfunction of some kind, because no line should be on prior to selection.

Bit 7

Not used.

Bit 6, Bit 7

Not used.

SENSE BYTE 2

Unsafe (Bit 0)

This bit is used to indicate that a file has given an unsafe indication. Some of the causes are:

1. More than one head has been selected.
2. The file is trying to read and write at the same time.
3. The write gate is off and write driver is on.
4. The write gate is on and the write driver is off.
5. The erase driver is off and the erase gate is on.
6. The erase driver is on and the erase gate is off.

SENSE BYTE 3

This byte is used to present the file interface lines to the system for file diagnosis. These interface lines are:

Sense Byte 3 2311

0	Ready
1	On Line
2	Unsafe
3	----
4	On Line*
5	End of Cylinder
6	----
7	Seek Incomplete

*Bit 4 is forced on for all files by the on-line signal.

SENSE BYTE 4

This byte is all zeros. It is a dummy byte inserted for control-unit compatibility with other control units.

SENSE BYTE 5

This byte is all zeros. It is a dummy byte inserted for control-unit compatibility with other units.

SPECIAL FUNCTIONS, DISK

END-OF-FILE DISK

The end-of-file indication is written by executing a Write Count, Key and Data CCW that has two bytes of zeros in the data-length (DL) portion of the count area. This command causes the DAC automatically to record one byte of zeros in the data portion of the end-of-file record. If the key-length (KL) portion of the count area is zero, the end-of-file record contains the contents of the count area and the data area (one byte of zeros). If KL is non-zero, the key whose length is specified by KL is written in the key area of the end-of-file record.

As a logical file is read, the count areas of the records are examined. Detection of a DL of zero in the count area causes generation of a unit-exception signal. The unit-exception signal is always generated at the normal ending time of the read operation that was scheduled. No data from the data area is transferred.

The unit exception is generated during the following operations:

- Read IPL
- Read R0
- Read Count, Key and Data
- Read Key and Data
- Read Data
- Write Key and Data
- Write Data
- Search Key and Data.

MULTIPLE-TRACK (M/T) OPERATIONS

The disk attachment control can select automatically the next sequentially numbered 2311 read/write head under control of bit 0 of the command byte. Head

switching does not take place at index point if bit 0 is 0. Head switching does occur at index point if bit 0 is 1. Whenever head switching is anticipated, a seek CCW (any type) must be given in the chain prior to the point where head switching is to occur so that the current head address is available to the DAC for incrementing. A recalibrate command must be followed by another seek command before head switching is attempted.

The M/T bit is recognized on all read and search commands. Therefore, a certain amount of discretion should be used when setting bit 0 to 1. For example, if during a search operation the desired record is on the first track searched but the search commences after that record is passed and the M/T bit is on, the head advances to the next track without even comparing the desired record. To avoid this condition, a single-track read home address or read R0 command should be placed ahead of the search to ensure that searching starts at R0 or R1 of the first track.

FILE PROTECTION

The DAC portion of the file-protection function utilizes a set file mask command and its associated controls. This control command (bit structure of 1F) causes one byte of data to be transferred from main storage to the DAC. When the transfer is completed, a channel-end and device-end signal is generated.

The data byte sent to the DAC describes which write and seek commands can be performed. Bits 0 and 1 describe the write commands that can be initiated. The significance of the file-mask bits is as follows.

File Mask Bits	Significance
<u>0 1 2 3 4 5 6 7</u>	
0 0 0 x x 0 0 0	Inhibit Write Home Address and Write R0
0 1 0 x x 0 0 0	Inhibit <u>all</u> Write and Erase commands
1 0 0 x x 0 0 0	Inhibit Write Home Address, Write R0, Write Count, Key and Data, and Erase commands
1 1 0 x x 0 0 0	Permit <u>all</u> Write and Erase commands
x x 0 0 0 0 0 0	Permit <u>all</u> Seek and Recalibrate commands

x x 0 0 1 0 0 0 Permit Seek CCHH and Seek
HH CCW&S

x x 0 1 0 0 0 0 Permit Seek HH CCW

x x 0 1 1 0 0 0 Inhibit all Seek commands

Note: For the DAC, file-mask bits 2 and 5-7 must be zero. If these bits are not zero, the mask is considered invalid and a unit-check signal is generated. When a subsequent sense command is executed, a command reject is signaled.

A set file mask command can be issued anywhere within a CCW chain. At the completion of the CCW chain, the file mask is reset to all zeros. A set file mask command can be issued only once within a given CCW chain. If an attempt is made to issue more than one set file mask command in a chain, a unit-check signal is generated in the status byte. A subsequent sense command signals command-reject and invalid-sequence.

The set file mask command resets the defective and alternate track indicators in the DAC. Thus, when it is included in a CCW chain, the set file mask command should be given prior to any read or search command.

If a write command is issued violating the file mask, the command is not executed and a unit-check signal is generated in the status byte. A subsequent sense command signals command-reject and file-protect.

If a seek command is issued violating the file mask, the command is not executed and a unit-check signal is generated in the status byte. A subsequent sense command signals file-protect.

File-protect takes precedence over an end-of-cylinder: the latter is not set with file-protect.

System reset causes the file-mask register to be set to all zeros. A subsequent Start I/O with no set-file-mask CCW, therefore, permits:

All Seek commands,
All Read commands,
All Restore commands,
Erase commands,
Write Count, Key and Data,
Write Key and Data, and
Write Data commands,

but does not allow:
Write Home Address, and
Write R0 commands.

TRACK ORIENTATION

Track orientation in the DAC is accomplished with fields and zones that uniquely define any portion of a track. Figure 47 illustrates the relationship of the fields and zones to the track format.

A break in a CCW chain, or issuance of a control command other than Erase, sets the DAC to a reset condition. Recognition of the next data command places the DAC in an initializing state relative to that field and zone required to perform the operation.

Initializing state HA (field H, zone A) is used for index detection.

Initializing state C1 is used for address-marker detection. This state is also used by a Search ID command for index detection.

Figure 48 illustrates the initializing states of fields and zones, and the command sequences required to perform a data command.

Record	HA				R0												R _n															
Field	H				C				K				D				C				K				D							
Zone	A	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4	A	B	*	1	2	3	4	1	2	3	4	1	2	3	4

Field Definition

- H Home-address area (including gaps)
- C Count area (including gaps)
- K Key area (including gaps)
- D Data area (including gaps)

Zone Definition

- 1 Pre-record gap (including address marker)
- 2 Record
- 3 Cyclic code
- 4 Post-record gap
- A Constant gap of 12-ones bytes in the count field, or 28 all-zeros bytes in the home-address field.
- B The 4.9% variable gap between records.

Notes: The index point immediately precedes the home-address area.
 * Location of the address marker.

Figure 47. Track Orientation

Command	Command Sequence	Initial Field and Zone State	Field and Zone State at End of Command
Read Count, Key and Data Read Key and Data	None	C1	D4
	None	C1	D4
	After Search ID	C4	D4
Read Data	None	C1	D4
	After Search ID	C4	D4
	After Search Key	K4	D4
Write Count, Key and Data	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
	Write R0	D4	D4
	Write Count, Key and Data	D4	D4
Write Key and Data	Search Equal ID	C4	D4
Write Data	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
Search ID	None	C1	C4
Search Key	None	C1	K4
	After Read or Search ID	C4	K4
Search Key and Data	None	C1	D4
	After Read or Search ID	C4	D4
Search Home Address	None	HA	H4
Read R0	None	HA	D4
	After Read or Search Home Addr	H4	D4
Write R0	Write Home Address	H4	D4
	Search Equal Home Address	H4	D4
Read Home Address	None	HA	H4
Write Home Address	None	HA	H4
Read Initial Program Load	None	C1	D4
Read Count	None	C1	C4
Erase	Search Equal ID	C4	D4
	Search Equal Key	K4	D4
	Write R0	D4	D4
	Write Count, Key and Data	D4	D4
No Operation	None	Reset Condition	

Figure 48. Track Orientation Field- and Zone-State Summary

DEFECTIVE DISK-PACK SURFACES

The disk attachment control has provisions to handle defective recording areas that may appear during the life of an IBM 1316 disk pack. These defective areas are handled by the Track Descriptor Record (R0). Implementation of the record-0 concept depends upon the availability of a

perfect recording area on each track that extends from the index point to the end of record R0.

Record 0 is always the first record on the track following the index point and the home address. Record 0 has the following format.

F ID KL DL CCB Gap Key CCB Gap Data CCB

where:

F - Flag byte: This 1-byte field is divided as follows:

- Bit 0 - Used for internal DAC control purposes.
- Bit 1 - Used for the record-overflow feature.
- Bits 2-5 - Not used.
- Bits 6-7 - Track-condition bits used to indicate the condition of the track. These bits are propagated from the home address to all records of the track. The significance of the track-condition bits is as follows.
 - Bit 6 = 0: Good Track.
 - Bit 6 = 1: Defective track
 - Bit 7 = 0: Original track.
 - Bit 7 = 1: Alternate track

ID - Identifier: The ID field contains the cylinder (CC), head (HH), and record (R) numbers. Cylinder and head numbers are two bytes each. They contain the actual track location for good tracks. The record number is one byte long. It contains the sequential position of the record on the track. (For R0, the record number is 0.)

KL - Key Length: This 1-byte field contains the length of the key area.

DL - Data Length: This 2-byte field contains the length of the data area.

CCB - Cyclic-Check Bytes: These two bytes are used for error-detection purposes. (See the Cyclic-Code Bytes section).

Gap - The gaps separate the various areas within a record.

Key - The key area (length defined by the KL field) is used to identify information contained in the data area.

Data - The data area (length defined by the DL field) contains the actual information associated with the record. An R0 record is not preceded by an address marker.

The special read R0 and write R0 commands operate only on record 0. The read R0 command operates like a Read Count, Key and Data command except that it does not set the track-condition indication (except when an attempt is made to switch from a defective or alternate track). The write R0 command operates the same as a Write Count, Key and Data command.

The alternate-track approach to the problem of defective areas permits an entire track to be repositioned independently of the way the file was originally organized. This is done by flagging the condition of the track in the home-address flag byte (bits 6-7). These track-condition bits are propagated by the DAC from the home-address area to all other records on that track. The four possible track conditions are as follows.

1. Original track good. In this case, the track-condition bits (6-7) are set to 00.
2. Original track defective. In this case, the data field of the track-condition bits are set to 10.
3. Alternate track good. The track-condition bits are set to 01.
4. Alternate track defective. The track-condition bits are set to 11. Such a flagged track posts all interruption conditions normally associated with either defective or alternate tracks. (This coding is not generally used.)

TRACK INITIALIZATION (DEFECTIVE-TRACK DETERMINATION)

The following procedure must be followed by track-initialization programs for the IBM 2311 files. This procedure is intended to write home addresses on each track and to analyze the condition of the recording surface. The program should be written to handle the tracks in cylinder mode to reduce running time.

1. Read home address. Verify that the track has not been previously flagged. This step must be bypassed by operator action when initializing the recording surface for the first time. Unless specifically optioned by the operator, no program should change the flagging of a previously flagged alternate or defective track.
2. Write home address and record zero (R0) with a maximum-length data field on all tracks. The data pattern should be hexadecimal 55.
3. Read home address and R0 of each track

to ensure that the data can be recovered successfully. If an error occurs, go to step 7.

4. Repeat step 2, using a data pattern of hexadecimal 00.
5. Repeat step 3. If an error occurs, go to step 7.
6. Rewrite home address and a standard length record 0 on all good tracks. Read and verify that these records can be recovered successfully. If an error occurs, go to step 7. The surface analysis is now complete.
7. When an error occurs, an analysis of the sense information must be made. If the error is a data-check in the count field and/or a data-check, steps 2, 3, 4, and 5 must be performed 20 times on the track in question. If a data-check (also includes a count-field data check) occurs a second time on the track, the track must be flagged as defective. Go to step 8. Other errors should be handled as defined in the Error Recovery Procedures, DAC section. If no error occurs, return to the program at point of exit.
8. Assign an alternate track.
9. Write home address and R0 on the defective track. Set the home-address flag byte to hexadecimal 02. The home address is the physical address of the defective track. The R0 count field contains the address of the alternate track. The content and length of the data field are not critical. However, the data-field length (DL) should be kept to a minimum (but greater than zero) to avoid spanning the track defect. No other records should be written on the track.
10. Read-check the home address and R0. If a data-check (also includes a count-field data check) or missing address marker and no-record found errors occur, go to step 14. Other errors should be handled as in the Error Recovery procedure, DAC section.
11. Seek the alternate track.
12. Write home address and record zero on the alternate track. Set the home-address flag byte to hexadecimal 01. This home address is the physical address of the alternate track. The R0 count field normally contains the address of the original defective track.
13. Return to mainline program.

14. Track flagging requires a perfect recording surface from the index point to the end of record zero. If attempts to write home address and R0 indicate that this area is defective, the recording medium (disk pack) must be replaced.

The basic requirement is one pass through the test (steps 2-5). An option should be provided to increase the number of tests to 16.

Additional requirements for programs that write the home address and R0 area (and in particular, Surface Analysis, Diagnostic, and other track utility programs such as UT069, UT098, and DASDI) are as follows.

1. Unless specifically optioned by action of the operator, no program should change the flagging of a previously flagged alternate or defective track.
2. Specific action on the part of an operator should be required to unflag a track.
3. Provision must be made to flag or unflag individual or groups of tracks.
4. Operating programs that have provisions for dynamically flagging tracks must perform the 14 steps given earlier in this section.

OPTIONAL FEATURES, DISK ATTACHMENT CONTROL

FILE SCAN FEATURE

The file-scan function provides a means of locating and selecting records on the basis of a comparison of selected parts of the key and data fields. Execution of the file-scan commands is similar to that of the search-key command, except that:

1. The comparison starts with the key and continues through the data field, and
2. For any bytes in the record on which a comparison is not desired, an FF (hex) byte should be inserted in the Scan argument (in main storage). For each FF byte received from the channel, the DAC passes over the corresponding byte of the record being scanned without comparing it.

The file-scan commands are normally used in the same way as the search key, with a Transfer in Channel (TIC) CCW causing re-execution of the command until a record

is found that satisfies the comparison criteria. When a record is scanned that satisfies the criteria, the DAC presents status-modifier with channel-end and device-end, causing the DAC to skip over one CCW (normally, the TIC), and to continue with the program.

The file-scan feature includes six new commands, three of which are single-track and three multitrack. These commands are for Search Key and Data operations.

Search Key and Data Equal (2D or AD)

Execution of this command causes the DAC to compare the key and data information of a record with the information sent to the DAC by the system. Any byte with an FF (hex) configuration from the system causes the comparison with the corresponding byte from the file to be suppressed. If the comparison is equal on all other bytes compared, status-modifier occurs with channel-end and device-end when the end of the logical record is reached; i.e., end of the data field except for overflow records. The key data compared is that of the record following the next address marker, unless the Search Key and Data is chained from a Read Count or Search ID CCW. In these cases, the key and data is that of the record whose count field was read or searched. When Search Key and Data is not chained from a Read Count or Search ID, and the index point is encountered before an address marker is found, then:

1. If the multitrack bit (bit zero of the command byte) is on, head switching occurs, (see the Multiple-Track Operations section).
2. If the multitrack bit is off, record one of the current track is compared. In this case, the no-record-found function may cause an interruption, if the index-passed bit is on (see the No Record Found (Bit 4) section).

When search-key data is chained from a Read Count or Search ID, a multitrack bit in the Search Key and Data CCW has no meaning.

If the record searched has a key length of zero, the comparison begins in the data field.

If the CCW count is less than the length (KL + DL) of the logical record, status-modifier is generated on the basis of the compare up to the point where the CCW count is exhausted. This allows the scan function to be applied to keys alone.

If overrun is detected, it is signaled immediately. If a data-check error occurs, it is signaled at the end of the field in which the error occurs.

Search Key and Data High (4D or CD)

This command operates like Search Key and Data Equal, except that status-modifier is set on the first unequal comparison where the byte on the file is numerically greater than the corresponding byte from the system. As in the case of Search Key and Data Equal command, the comparison is suppressed on all bytes where the channel byte has the hexadecimal value FF.

Search Key and Data High or Equal (6D or ED)

This Command operates like the other two file-scan commands, except that status-modifier is set if the data on the file is equal to or greater than the data from the channel.

Programming Notes, File Scan Feature

1. Normally, the sequence:
Read Count
Search Key and Data
TIC* - 16
--
--

is used with Search Key and Data command so that the ID of the desired record is in main storage when the desired record is found. Without terminating the chain, the channel program can search on this ID and then process the Key and Data of the located record as desired. If a cylinder search is desired, the M/T bit must be included in the Read Count CCW. Unless care is taken to ensure otherwise, execution of a Search ID sequence following the above sequence may cause a no-record-found indication. The No Record Found (Bit 4) section should be carefully studied to understand hazards in this area.

2. A search for a low, low or equal, or unequal record may be accomplished with the sequence:

Read Count
Search Key and Data (High-Equal,
High, or Equal, respectively)
TIC* + 16
TIC* - 24
--
--
--

ERROR RECOVERY PROCEDURES, 2311/DAC

ERROR MESSAGES, 2311 DISK ATTACHMENT CONTROL

The following two error messages should be included in the operating environment of all DAC users.

Message 1 (should be printed on all uncorrectable errors).

- a. Message code
- b. Error type - read, write, or control
- c. Unit designation, cell number, cylinder number, head number and head position; i.e., device addressed and seek address.
- d. Channel designation
- e. Status and sense bytes sent to CPU

Message 2 (should be printed periodically, upon completion of a run, or in response to operator request).

- a. Unit designation
- b. Number of entries into error routine
- c. Number of uncorrectable errors.

ERROR CONDITION TABLE, 2311/DISK ATTACHMENT CONTROL

This section gives the recommended corrective action for the error conditions that may occur when using IBM 2311 units

attached to the System/360 Model 25 through the disk attachment control. The recovery procedures are listed in the Action column. These are given in detail following the Error Condition Table (Figure 49).

RESETS, DAC AND/OR 2311 UNIT

The DAC senses a Selective Reset or a General Reset, either of which terminates all DAC activity and clears all internal registers. All status and error conditions are reset.

A General Reset also causes any device-ends pending in the 2311 units to be reset.

USE METER (2311)

The use meter on each 2311 operates when the 2311 is in the enabled state and the CPU customer meter is operating.

The 2311 changes to the enabled state upon the first stop or wait state that occurs after the enable/disable switch is set to the enable position. The unit changes to the disabled state upon the first stop or wait state that occurs after the switch is set to the disable position and any previously initiated operation involving the device has been completed.

Sense Bit and Name	Explanation	Error Type	Action
Byte 0, bit 0 (Command Reject)	The DAC has received an invalid command code.	Program error	1
Byte 0, bit 0 (Command reject) and byte 0, bit 7 (Seek Check)	The DAC has received an invalid seek address.	program error	1
Byte 0, bit 0 (Command Reject) byte 1, bit 3 (Invalid Sequence)	The DAC has received an invalid sequence of commands.	Program error	1
Byte 0, bit 9 (Command Reject) and byte 1, bit 5 (File Protected)	The DAC has received a command that violates the Inhibit Write portion of the File Mask.	Program error	1
Byte 0, bit 1 (Intervention Required)	The specified 2311 unit is: 1. Not on line, or 2. Not available for use due to cover interlock open, file motor off, etc.	Equipment error	2
Byte 0, bit 3 (Equipment Check) <u>and</u>	An unusual condition has been detected in the DAC or the file unit. The condition is indicated by sense-byte 2.	Equipment error	2
Byte 2, bit 3 (Unsafe) or Byte 2, bit 3 (Cyclic Code Check) or Byte 2, bit 4 (Selected Status) or Byte 2, bit 5 (Unselected Status)	A file malfunction has been detected. Circuitry used to generate the cyclic-code check did not function properly. Microprogram decode of the status byte yielded self-contradictory results. The status line from the files is on, but no file has been selected.		
Byte 0, bit 4 (Data Check)	The DAC has detected an error in the data field received from the file.	Equipment error	8
Byte 1, bit 6 (Missing Address Marker)	The DAC has received: 1. Two index points without an intervening address marker, or 2. Two successive count fields with equal bit conditions in bit 0 of the flag bytes.	Equipment error	5
Byte 0, bit 5 (Overrun)	The DAC access to main storage was suppressed longer than one byte time on the 2311, or a chained CCW was received too late to be properly executed.	Equipment error	3

Figure 49. Error Condition Table (Part 1 of 3)

Sense Bit and Name	Explanation	Error Type	Action
Byte 0, bit 6 (Track Condition Check)	<ol style="list-style-type: none"> 1. A Search, Read, or Write command was attempted on a flagged defective track (track-condition bit 6 was set to 1). Exceptions: HA and R0 operations. 2. Command chaining and multitrack code signals indicate that operations from an alternate track are to continue on the next higher-order track. 	Program error	6
Byte 0, bit 7 (Seek Check)	<p>The 2311 has been unable to complete the Seek because:</p> <ol style="list-style-type: none"> 1. The access mechanism failed to reposition properly, or 2. The home-address-compare failed after automatic head switching on a multitrack operation 	Equipment error	4
Byte 1, bit 0 (Data Check in Count Field) and byte 0, bit 4, (Data Check)	The DAC has detected an error in the count field received from the 2311.	Equipment error	8
Byte 1, bit 1 (Track Overrun)	The index point was detected before writing was completed.	Program error	1
Byte 1, bit 2 (End of Cylinder)	An end-of-cylinder was detected before the CCW command chain was completed while in multitrack mode.	Program error	1
Byte 1, bit 4 (No Record Found) and <u>not</u> byte 1, bit 6	<p>Two index points were detected while:</p> <ol style="list-style-type: none"> 1. Executing a chain of CCWs with no intervening Read or Write operation on the data field of any record. 2. Executing a Read HA or Read R0 CCW. <p>Note: This could be an expected condition on Search command chains.</p>	Program error or equipment error	7
Byte 1, bit 5 (File Protect)	The DAC has received a Seek, a multitrack Read, or multitrack search that violated the Seek File Mask.	Program error	1
Byte 1, bit 4 (No Record Found) and byte 1, bit 6 (Missing Address Marker)	Home address or R0 cannot be found on the track.	Equipment error	9

Action	Recovery Procedure
1	Exit with Program Error indication.
2	Repeat original sequence <u>once</u> .
	If the error condition still occurs, print <u>Message 1</u> for the operator and/or customer engineer notification. This is considered an uncorrectable error; the recovery procedure depends on the application.

Figure 49. Error Conditions Table (Part 2 of 3)

Action	Recovery Procedure
3	<p>Repeat the original sequence ten times if the error persists.</p> <p>After ten unsuccessful retries, print <u>Message 1</u> for the operator and/ or CE notification.</p>
4	<p>Issue a Recalibrate command.</p> <p>Seek to the original address.</p> <p>Repeat the original sequence ten times if the error persists.</p> <p>Print <u>Message 1</u> and exit with the error indication.</p>
5	<p>Repeat the original sequence ten times if the error persists.</p> <p>After ten unsuccessful retries, the error is said to be "hard". At this point, the hard-error recovery procedure may be employed at the user's option.</p> <p>Print <u>Message 1</u> and exit with the error indication and option information.</p>
6	<p>If this is an <u>alternate</u> track, use the defective-track address, plus 1, in the Seek command. (This is found in the ID field of the R0 count area.) Resume the operation after searching to the desired track position.</p> <p>If this is a <u>defective</u> track, use the alternate-track address in the Seek command. (This is found in the ID field of the R0 record.) Resume the operation after searching to the desired track position.</p>
7	<p>Issue a Read Home Address command to verify that the correct track has been reached. (Correct cylinder is sufficient on multitrack operation.)</p> <p>If the correct cylinder (and/or track) is found, perform Action 1.</p> <p>If the incorrect cylinder (and/or track) is found, perform Action 4.</p>
8	<p>Repeat the original sequence sixteen times if the error persists.</p> <p>After sixteen unsuccessful retries, issue instructions to Recalibrate, and then Seek to the original cylinder. Repeat first two steps sixteen times if the error persists.</p> <p>After sixteen unsuccessful retries of second step (a total of 256 entries for the data), the data-error is said to be "hard". At this point, the hard-error recovery operations may be employed at the user's option.</p> <p>Print <u>Message 1</u> and exit with the data-error indication and option information.</p>
9	<p>Issue a Recalibrate and then a Seek to the original address.</p> <p>Repeat the operation that failed.</p> <p>Repeat the first two steps twice if the error persists.</p> <p>Issue a Read HA to a different track in some cylinder.</p> <p>If the Read HA is successful, return to the original track and perform Action 3.</p> <p>If the Read HA is unsuccessful after two tries and causes the same error indication, print <u>Message 1</u> for operator and/or CE notification.</p>

Figure 49. Error Condition Table (Part 3 of 3)

A single IBM 2540 Card Read Punch can be attached directly to the IBM System/360 Model 25 through an integrated attachment in the processing unit. No external control unit is required. Only one 2540 can be controlled through the integrated attachment but this does not limit the system to one 2540. Other 2540s, controlled by the IBM 2821 Control Unit, can be attached to the system by means of the standard interface on either channel 0 or 1.

The 2540, by means of two independent card paths (the read feed and the punch feed) operated under program control, provides for:

1. Reading of punched-card data into the system.
2. Punching of system-output data into cards.

Data from cards in the read feed can be entered into the system at a maximum rate of 1000 cpm (cards per minute). System-output data can be punched into cards in the punch feed at a maximum rate of 300 cpm. These maximum rates are independent of the amount of data read or punched per card. A card can contain up to 80 columns of punched-hole information. Less than 80 columns can be read or punched per card, but this action does not increase reading or punching speed.

Reading and punching in the 2540 can be performed in either data-mode 1 or data-mode 2. In data-mode 1, each card column is translated between the EBCD interchange card code and the machine 8-bit code. The EBCDIC chart in Appendix B shows these translations. Each specific hole pattern in the card column corresponds to only one processing unit byte bit pattern. For example, the punched hole-pattern 12-11-1, when read from a card column, is translated into the processing-unit-byte bit pattern 1001 0001: no other punched hole-pattern translates to 10010001. During output punching, the data-record-byte bit pattern 10010001 is punched in a card column as 12-11-1.

The column binary feature (standard) provides the capability of reading (in the read feed only, not for PFR operations) or punching cards in data mode 2. In data mode 2, the punch positions in each card column correspond to specific bit positions in the processing-unit-byte bit pattern. Punch positions 12 through 3 in any column

always correspond to bits 2 through 7 in odd data-record bytes:

<u>Odd Byte Bits</u>	<u>Punch Positions in Column</u>
0 (always = 0)	--
1 (always = 0)	--
2	12
3	11
4	0
5	1
6	2
7	3

Similarly, punch positions 4 through 9 in any column always correspond to bits 2 through 7 in even data-record bytes:

<u>Even Byte Bits</u>	<u>Punch Positions in Column</u>
0 (always = 0)	--
1 (always = 0)	--
2	4
3	5
4	6
5	7
6	8
7	9

For example, card-column-one punching always applies to bytes 1 and 2 of the data record.

Data mode 2 operation, then, provides a way of reading (or punching) binary data from (or to) cards. Data mode 1, the standard 2540 reading and punching mode, is available whether or not the Column Binary feature is installed. The choice of modes is determined by programming according to the desired application.

Five radial stackers are provided in the 2540:

1. P1 and P2, for the exclusive use of the punch,
2. R1 and R2, for the exclusive use of the reader, and
3. RP3, to which cards can be stacked from either feed.

Cards can be program directed into the appropriate stackers, as determined by the application. Cards that cause a hole-count error after they are punched are automatically stacked in P1.

The punch hopper holds about 1350 cards; the read hopper and file-feed magazine hold about 3100 cards.

Additional capabilities are provided when the following special features are installed.

SPECIAL FEATURES

51-Column Interchangeable Read Feed

With this feature, the reader can feed and read 80-column or 51-column cards. (The feature is not available for the punch.) When this feature is installed:

1. Reading speed is at a maximum rate of 800 cpm for both 80-column and 51-column cards.
2. The card capacities of stackers R1, R2, and RP3 are reduced to about 800 cards for 51-column operation.
3. The read feed must be manually adjusted for one or the other of the two card widths. That is, both 51-and 80-column cards cannot be intermixed in the read feed (hopper, stackers, etc).

Installation of this feature requires modification of the 2540 only; the 2540 attachment feature in the processing unit is not modified.

PFR (Punch Feed Read)

A reading station is added to the punch feed when this feature is installed. This read station (a full complement of 80 brushes) allows the program to read a card and then, depending upon the data read, to punch additional data in that same card. If such prepunched cards are read in the punch feed, PFR commands must be used by the program to read the cards. Otherwise, punch checks are indicated. If the cards in the punch feed are not prepunched, the normal punch instructions can be used.

Only data mode 1 can be used to read cards at the PFR station. However, data mode 2 (column binary installed) can be used to punch cards whether or not the PFR feature is installed.

KEYS, SWITCHES, AND INDICATORS

Some of the keys, switches, and indicators are common to both the reader and punch; some are used exclusively by only one of these two units, as shown in the following paragraphs.

COMMON READER-PUNCH INDICATORS

Power Light

When on, this light indicates that dc voltage is present in the 2540.

Transport Light

This light is on when a jam is detected in the continuously running section of either the punch or read feed (i.e., the area over the stackers).

Stacker Light

This light is on when any one of the five stackers is full.

Fuse

This light indicates that a +20 volt fuse is blown in the 2540.

CARD-READER KEYS AND INDICATORS

Start Key

Pressing this key starts the motor and feeds the first card into the prestacker station if cards are on the file feed or in the hopper. If the end-of-file light is not on, the hopper jogger is open, the hopper is empty, and the start key is operated, a nonprocess runout is executed. The cards in the transport are then run out into stacker R1.

Stop Key

This key stops the reader motor, resets the end-of-file condition, and places the reader in a not-ready condition (reader ready light off).

End-of-File Key

Pressing this key sets up the 2540 run circuits so the last cards can be processed when the hopper becomes empty.

Feed-Stop Light

This light is on when the reader motor stops as a result of a jam, misfeed, or a card feed-clutch failure. It can be switched off only by a nonprocess runout and a clearing of the feed.

Reader-Ready Light

This light indicates that the reader is in ready status.

Reader Check Light

This light indicates a hole-count check, shift-register sync or address check (both of which are circuit malfunctions in the attachment), overrun condition, or clutch failure while reading. It is turned off when a new command (other than sense, Test I/O or No-Op) is sent to the 2540 attachment for the reader.

Reader Validity Light

This light indicates that an invalid hole pattern (more than one punch in rows 1-7 of a single card column) has been detected on a data mode 1 read operation for the reader. It is turned off when a new command (other than sense, Test I/O, or No-Op) is sent to the 2540 attachment.

End-of-File Light

This light indicates that the end-of-file key has been operated. The light is turned off when unit-exception status is set on for the first read command directed to the reader after the last card from the hopper has been stacked.

The end-of-file light is also turned off when the reader stop key is operated.

CARD-PUNCH KEYS AND INDICATORS

Start Key

Pressing this key starts the motor and feeds the first card as far as the prepunch station. If the hopper is empty and the start key is pressed, a nonprocess runout is initiated. The cards in the transport are then run out into stacker P1.

Stop Key

Operating this key stops the motor at the completion of a mechanical cycle. If the PFR feature is present, pressing the stop key turns off the end-of-file light. Also, whenever the stop key is operated, the punch is placed in the not-ready condition (punch-ready light is off).

Punch-Ready Light

This indicates that the punch is in a ready condition.

Feed-Stop Light

This light is on when the punch motor stops as a result of a jam, misfeed, or a punch-clutch failure. This light can be switched off only by doing a nonprocess runout and a clearing of the feed.

Chips Light

This light is on when the punch chip box is either full or missing.

Punch-Validity Light (PFR Only)

This light indicates that an invalid hole pattern (more than one punch in rows 1-7 of a single card column) has been detected on a PFR read operation for the punch. It is turned off when a new command (other than Sense, Test I/O, or No/Op) is sent to the 2540 attachment.

Punch-Check Light

This light indicates, for the punch, a hole-count check, shift-register sync check or address check (both of which are circuit malfunctions in the 2540 attachment), or clutch failure. It is turned off when a new command (other than sense, Test I/O, or No-Op) is sent to the attachment for the punch.

End-of-File Key (PFR Feature Only)

Pressing this key sets up the run circuits so that the last cards can be processed when the hopper becomes empty. Unit-exception is indicated only on a read; therefore, the last punch record, in non-PFR operation, could be punched when no card is under the punches, because unit-exception is not indicated for write commands.

End-of-File Light (PFR Feature Only)

This light indicates that the end-of-file key has been operated. The end-of-file light is reset when the last card reaches the pre-stacker station. It is turned off with a non-PFR command.

The end-of-file light is also turned off when the punch stop key is operated.

ADDRESSING, INTEGRATED 2540 ATTACHMENT

The integrated 2540 attachment is addressed as if it were connected to channel 0. The sixteen-bit address developed from the I/O instruction identifies the attachment and the reader or punch unit. The device address is not limited by the usual channel-0 UCW addressing requirements because the attachment has its own UCWs that are not device address dependent. In theory, the attachment may have any address from:

<u>Binary</u>	<u>Hex</u>
0000 0000	00
to	to
1111 1111	FF

In practice, the integrated 2540 is assigned an address of 0C for the reader and 0D for the punch, to standardize with other System/360 usage. This addressing makes use of two of the channel-0 subchannel addresses and prevents their use for the channel. If the channel configurations require the use of the subchannels, the 2540 addresses can be changed by the customer engineer.

Under no condition should an address assigned to any other I/O device be assigned to either the 2540 reader or punch.

IBM 2540 READER OPERATION

READER RUN-IN

Operation of the reader start key initiates three card-feed cycles (Figure 50) if all of the following conditions exist:

1. No cards are in the read feed.
2. No cover interlock is open.
3. No stacker-full switch is operated (reader or punch).
4. Cards are in the reader file-feed or hopper.
5. The reader-hopper jogger plate is in its operated position.

The three cards are fed in so that the first card stops at the prestacker position. At the end of the three feed cycles:

1. The reader ready light is on.

2. Device-end status is available in the 2540 reader attachment for presentation to the CPU. This device-end can be cleared by execution of an I/O interruption, a Test I/O instruction, or a Start I/O instruction. Busy status accompanies device-end in the CSW if the device-end is cleared by a Start I/O. Only device-end status, assuming no errors, appears in the CSW if the device-end is cleared by an I/O interruption or Test I/O.
3. Data from the first card fed from the hopper is in auxiliary storage. This data can be transferred to program storage by execution of a read command.

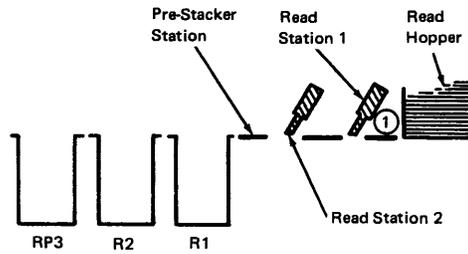
If an intervention required condition (such as a card jam) occurs during the run-in cycles, the not-ready-to-ready device end is not set on and the reader ready indicator does not light. Unit-check status is then the reader response to any Test I/O or Start I/O selection sequence directed to the 2540 reader, until the intervention-required condition is corrected and the reader is made ready.

Initial Setup

- No cards are in the read feed.
- No cover interlock is open.
- No stacker-full switch is operated.
- Cards are in the reader file feed or hopper.
- The reader-hopper joggler plate is in its operated position.
- The reader start key is operated.

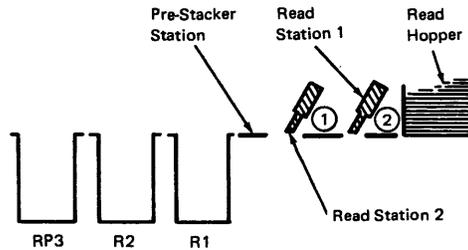
Feed-Cycle One

- Card ① is fed from the hopper.



Feed-Cycle Two

- Card ① is read at Read Station 1.
- Card ② is fed from the hopper.



Feed-Cycle Three

- Card ① is check-read at Read Station 2 and is stopped at the pre-stacker station.
- Card ② is read at Read Station 1; card ③ is fed from the hopper.
- The reader ready light turns on.
- Data from card ① is available in the reader area of auxiliary storage for transfer to program storage during a subsequent read command operation.

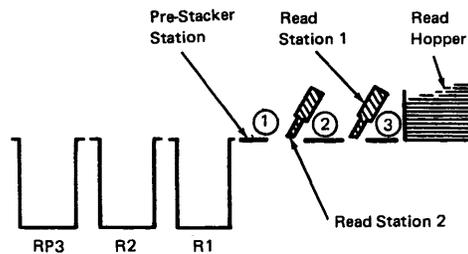


Figure 50. 2540 Reader Run-In Cycles

Data read from the cards is transferred into auxiliary storage. This transfer of data is accomplished with a series of microprogram traps. (A trap is a forced branch out of the current CPU microprogram operation in to some higher priority microprogram operation. When the higher priority operation is completed, a return is made to the interrupted routine.) Trap operations that have a priority higher than 2540 reader data-transfer traps can break into 2540 reader trap operations. In this case 2540 traps are delayed until the higher priority trap (such as for 2311 command chaining) is completed.

The priority circuits are designed to guarantee the reader a sufficient number of cycles for data transfer. An overrun should never occur except as a failure in the priority area.

The overrun can occur during reader run-in cycles. If such an overrun occurs, the not-ready-to-ready device-end is still made available to the CPU. However, during subsequent execution of a read command, unit-check (due to equipment check, sense bit 3) is presented with channel-end for that read command.

2540 READER--COMMAND EXECUTION

A read command can be acted upon as soon as the not-ready-to-ready device-end is cleared. If the read command is accepted by the reader attachment, the card data is moved from auxiliary storage to program storage. A stop can be indicated before the entire record is moved to program storage, in which case, transmission of data stops. The stop referred to is implemented by the CCW data count going to zero before the end-of-record is reached. The initial CCW count is less than 80 when operation is in data mode 1; less than 160 in data mode 2.

Channel-end is the response to the CCW data count going to zero (when data chaining is not indicated) or when the transfer reaches the end-of-record, whichever occurs first. For example, only column-one data might be sent to program storage (by a read and no feed or stacker selection command) to determine in what mode (data mode 1 or data mode 2) the entire record should be read. Here, data transfer would stop after only one byte is transferred to program storage. (The count of the first CCW would be 1, in this case.) Programming would determine, from the

column-one data, the proper mode to be used for reading of the entire record. By a read and feed command, programming could then dictate reading the entire record in the appropriate mode, and the operation would normally be stopped at the end of record.

In the case of a read command without a feed and stacker select, device-end is sent to the channel along with channel-end. If the read command includes a feed, device-end occurs when the feed is completed (at which time auxiliary storage contains the new card data).

A control command (feed and select stacker) is used after a read command (which did not specify a feed and stacker select) to write the next-card data into auxiliary storage. This command enables the programmer to stacker-select a card according to the information read from that card. In this particular operation, channel-end is sent to the channel immediately following the acceptance of the command byte. All necessary stacker selection information is contained in the modifier bits of the command. Device-end status is presented to the channel after the feed is completed. (Auxiliary storage then contains the new data.)

During a feed and stacker-select operation, the card stacked is the one from which the last data record was transferred to the processing unit.

A read following a read with no intervening feed can be executed, but a unit-check is sent to the channel with channel-end. The unusual-command-sequence sense bit is set for this condition.

Hole-count information for each of the 80 read brushes is generated and stored as the card feeds through the first read station. The hole count obtained at the second read station during the next card cycle is compared to that stored on the previous cycle. Failure to compare in any column causes an error (equipment check, sense bit 3) to be set on in the attachment. A unit-check accompanies channel-end of the next read command to indicate this error condition.

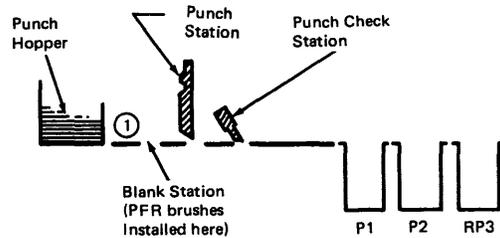
In data mode 1, a validity check is made on the data read from the card. If a card column contains more than one punch in rows 1 through 7 of a single card column, unit-check status (due to data check sense bit 4) is presented with channel-end. This check is not used in data mode 2 operations.

Initial Setup

- No cards are in the punch feed.
- No cover interlock is open.
- No stacker-full switch is operated (either punch or reader).
- Cards are in the punch hopper.
- The punch start key is operated.

Feed-Cycle One

- Card ① is fed from the hopper.



Feed-Cycle Two

- Card ① is fed to the pre-punch station.
- Card ② is fed from the hopper.
- The punch ready light turns on.
- Card ① is ready to be punched with data sent from program storage on a write command.

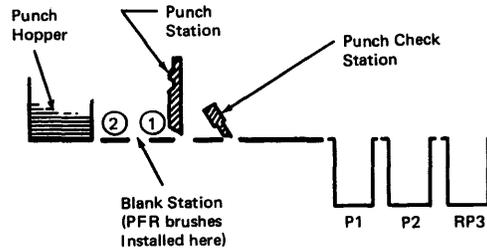


Figure 51. 2540 Punch Run-In Cycles

IBM 2540 PUNCH OPERATION

PUNCH RUN-IN

Operating the punch start key initiates two card-feed cycles (Figure 51) if all of the following conditions exist:

1. No cards are in the punch feed.
2. No cover interlock is open.
3. No stacker-full switch is operated (either punch or reader).
4. Cards are in the punch hopper.

The two cards are fed in so that the first card stops at the prepunch station. At the end of the two feed cycles:

1. The punch ready light is on.
2. Device-end status is available in the 2540 punch attachment for presentation to the CPU. (This device-end can be cleared by execution of an I/O

interruption, a Test I/O instruction, or a Start I/O instruction. Busy status accompanies device-end in the CSW if the device-end is cleared by a Start I/O. Only device-end, assuming no errors, appears in the CSW if the device-end is cleared by an I/O interruption or Test I/O.)

If an intervention-required condition (such as a card jam) occurs during the run-in cycles, the not-ready-to-ready device-end is not turned on and the punch ready indicator does not light. Unit-check status is then the reader response to any Test I/O or Start I/O selection sequence directed to the 2540 punch, until the intervention-required condition is corrected and the punch is again made ready.

Punch overrun can occur during punch run-in cycles even though no data is actually sent to the punch. This can happen because punch-trap operations are performed during run-in in the same manner

as during a write command to the punch. This condition is indicated by unit-check status (due to equipment check, sense bit 3) presented with the not-ready-to-ready device-end.

2540 PUNCH--COMMAND EXECUTION

After the not-ready-to-ready device-end (caused by completion of run-in) is cleared, a write command can be used to initiate punching in the first card. Less than the maximum record (80 bytes for data mode 1; 160 bytes for data mode 2) can be punched if the initial data count in the CCW is less than the maximum record count. Punching, however, always begins at column one of the card. For any card column to remain unpunched, the corresponding data record bit pattern (in data mode 1) from program storage must contain the bit pattern 0100 0000 (space). For data mode 2, punching occurs only for those bits (2 through 7) of the data record byte that are set to a value of one.

Channel-end is presented to the CPU after the CCW count goes to zero (and data chaining is not indicated) or when the end of record is reached, whichever occurs first. On completion of the punching, a device-end is presented to the channel.

The card punched stops just before the punch-check station brushes. On the next command, this card is fed through the punch-check station and then stacked. If no errors are detected, it is fed into the stacker specified by the modifier bits in the command whose execution caused it to be punched. (The stacker selection information is retained until the card is directed to the specified stacker.)

Hole patterns read by the punch-check brushes are compared to the data that should have been punched in the card. Failure to compare in any column causes a check indication (equipment check, sense bit 3) to be turned on. Unit-check accompanies device-end to indicate this error. Both the card in error and the card after it are stacked in the P1 pocket for any non-PFR equipment check. No automatic extra feed cycles are taken. The card following the error card is stacked in the feed cycle in which the punch is commanded to punch the next card.

IBM 2450 PUNCH-FEED-READ OPERATION

The PFR (Punch-Feed-Read) special feature on the punch can be used for card reading, with or without card punching, concurrently with card reading in the read feed.

Operating the start key makes the punch ready if conditions warrant (see the preceding section) and causes a run-in of the first card past the PFR station. A device-end interruption is initiated. As the card passes the PFR read station, data is read into the PFR section of auxiliary storage. The card then comes to rest in the prepunch station. A read command causes the data to transfer to program storage.

As a result of a CCW data count going to zero (no data chaining indicated) or when the end of record is reached (i.e., 80 bytes transferred), channel-end and device-end are sent to the channel. A PFR write, feed, and stacker-select command then causes the punch section of auxiliary storage to be filled by bytes sent from the CPU. Again, a partial transfer is possible, if desired, by a stop (from the CCW count going to zero when data chaining is not indicated), responded to in turn with channel-end.

All the cards in the punch feed are then fed. Data from the card passing the PFR brushes is read into the PFR section of auxiliary storage and the data record sent from program storage causes the appropriate punching in the card passing the punch station. Thus, on completion of punching the first card, the second card has been read and the PFR section of auxiliary storage contains the information from the second card. A device-end signal is transmitted to the channel ending that cycle, and a new read command can then be given to repeat the process.

A read command following a read command with no intervening write command is executed, but a unit-check is sent to the channel with channel-end. (The unusual command sequence sense bit is set on.)

A hole count is generated and stored from the punch-feed-read brushes and is combined with the hole count generated while punching the card. This total hole-count is compared with the hole count read at the punch-check brush station. The hole count generated at the punch-feed-read brushes, however, is combined with the hole count generated at the punch station only if a write command that causes the punch-feed-read data to be transferred from the card to the PFR area of auxiliary storage is executed.

Also, punched-hole data read at the PFR brushes is checked for validity in the same manner as data read in the read feed. That is, more than one hole in rows 1 through 7 of any single card column causes a unit-check status (due to data check, sense bit 4) indication with channel-end for the command.

The PFR area in auxiliary storage is separate from the area used for data to be punched. When the first card is fed in during a run-in operation, data from that card is automatically read into the PFR area of auxiliary storage.

If the first run-in card contains no punches, the PFR area of auxiliary storage contains blanks after run-in. This data remains in the PFR area of auxiliary storage until the first PFR write command is executed. If a read command is executed at any time before the PFR write command, the data sent to program storage from the PFR area of auxiliary storage is that read from the first run-in card, regardless of the number of cards that have been punched since run-in.

This action differs from a 2540 PFR operation on a 2540 attached to the system through a 2821 Control Unit. In the 2821/2540, a single buffer is shared for both PFR read data and punch data. Therefore, in the 2821 the first read command causes data from the last card punched to be sent to main storage.

In the integrated 2540 attached to System/360 Model 25, however, a PFR write command must be issued to read card data from the PFR brushes into the PFR area of auxiliary storage (except for the first card read during run-in). This data then remains in the PFR area of auxiliary storage until another PFR write command is issued to read a subsequent card.

Note also that read commands to a punch without the PFR feature cause a unit-check (due to command reject, sense bit 0) at initial selection. This is not the case for a 2540 attached to a 2821 control unit.

TERMINATION OPERATIONS

If the end-of-file key is operated (for the card reader), cards continue to feed under program control after the hopper empties. After the last card has been read and stacked in the selected stacker, unit-exception status is given at initial selection of the next read command.

The reader is then in a not-ready condition after status for the last command has been accepted by the channel. It must be returned to a ready condition before commands can be accepted.

If the end-of-file key (provided for the punch only if the PFR feature is used) for the punch is operated, the next valid read command (following the command used to read the last-card data) causes a unit-exception status indication at initial selection. If additional read commands are given without an intervening write, feed, and stacker select command, unit-exception status continues to be given at each initial selection.

When unit-exception status is indicated for a read command (for the punch with PFR), a card is still at the pre-check station. Here, a write command, either for PFR or a normal write command, must be given (codes to be sent can be blank codes) so that the last card can be check-read and stacked. The device-end, given after the last write command, is accompanied by unit-check status if a check condition occurred during execution of the last write command. The punch is then in a not-ready condition. It must be made ready to respond to subsequent commands.

If the end-of-file key has not been operated and the last card is fed from the hopper the Ready light on the affected unit (reader or punch) goes out. Then, place cards in the empty hopper and press the start key (reader or punch). The ready light should turn on.

Whenever either the reader or punch is made ready, a not-ready-to-ready device-end is presented for the affected device to the channel. This device-end must be cleared (by an I/O interruption or a Test I/O or Start I/O instruction) before an operation with that device can be initiated.

OPERATION COMMANDS

To save processing time and program-storage space, setting up specific data modes is accomplished by modifier bits in the eight-bit command byte of the CCW rather than by separate control codes.

In the following command descriptions, the type-letters establish command sequences that can be given. The first letter of a command type-code must match the last letter of the type code of the preceding command. Otherwise, the sequence is invalid. For example, the sequence:

Type AA
 Type AB
 Type BA
 is valid, while:
 Type AA
 Type BA

is invalid. This sequence rule has two exceptions:

1. The succession of two read and no stacker selection commands (type AB), and
2. A read and no stacker selection command (type AB) followed by a read, feed, and select stacker (type AA) command.

In either of these two cases, the commands are executed, but unit-check status (bit 6) and unusual-command-sequence sense (bit 6) are set on.

Also, the first command to the reader after initial run-in should be a read. (However, a sense, Test I/O, or No-Op command can be executed.) A feed and stacker select command given just after initial run-in is rejected.

If it is desired to stack a card as a result of the data read from that card, a read-and-no-feed or stacker-select command should be given first. The information can then be processed and the decision as to where to stack the card can be made. A feed and stacker select command should be given to send the card to the appropriate stacker.

In the following command descriptions, the "C" in the 2-bit position indicates data mode 1 if a "0", and data mode 2 if a "1". Reading is done only in data mode 1 for any punch-feed-read card reading operation (the 2-bit position is ignored). If column binary is not installed, operation is in data mode 1 regardless of the bit-2 value.

INCORRECT-LENGTH-RECORD CONSIDERATIONS

A maximum of 80 bytes can be transferred for any command specifying data mode 1. For data mode 2 commands, however, two bytes are transferred for each card column. Therefore, a maximum of 160 bytes (specified by an initial CCW data count of 160) can be transferred for a column-binary operation.

The first byte for a column-binary data transfer pertains to the top half (punch positions 12 through 3) of card column one; the second byte pertains to the bottom half (punch positions 4 through 9) of card column one; the third byte pertains to the

top half of card column 2; and so on. Therefore, when an odd number of bytes is to be transferred in a column-binary operation, the last byte pertains to the top half of the last card column used. (Reading or punching always begin at column one, unless columns are skipped. The SKIP flag in a CCW, however, pertains to 2540 reader operations only).

If less than 160 byte-transfers are required, the SLI (Suppress Length Indication) flag should be on in the command being executed (where the data count is initially less than 160) to avoid an incorrect-length indication. (The comparable CCW data count in data mode 1 is 80.) If data chaining is used, the last CCW in the chain should have its SLI flag on to avoid an incorrect-length indication if the total number of bytes transferred to or from the 2540 for the chain is less than the maximum record size (i.e., 80 bytes in data mode 1, 160 bytes in data mode 2).

If data mode 1 is specified in a read command and column binary cards (with more than one punch in card rows 1 through 7 of any single card column) are then read:

1. Unit-check status is indicated with channel-end, and
2. Sense bit 4 (data check) is sent to the CPU on a subsequent sense command operation.

If data mode 1 is specified in a write command and the data count in any CCW is greater than 80, an incorrect-length indication is in the channel status stored in the CSW.

A CCW data count greater than 160 causes the incorrect-length indication for a data mode 2 operation.

The incorrect-length indication is not given if the SLI flag is on in the CCW specifying a count greater than 80 (or 160 in data mode 2). However, if a CCW (with its data chain flag on) specifies a count greater than the maximum record size (80 or 160, depending upon mode), the incorrect length indication will be given regardless of the setting of the SLI bit.

READ FEED AND SELECT STACKER (TYPE AA)

<u>Stacker</u>	<u>Command Byte</u>
R1	00C 00010
R2	01C 00010
RP3	10C 00010

Validity

1. Valid for reader.
2. Invalid for punch with or without PFR.

reader area of auxiliary storage during the card-feed cycle.

Sequence

1. Should follow a type AA or a type BA command.
2. Can follow a read-and-no-feed or stacker selection (type AB) command. In this case, unit-check accompanies channel-end of the read, feed, and select stacker (type AA) command. Unusual command sequence (sense bit 6) is indicated on a subsequent sense operation.

Normal Ending Status

1. Channel-end is presented to the channel after the end of data transfer (i.e., CCW data count goes to zero, or the end-of-record is reached).
2. Device-end is presented to the channel after the end of the card feed cycle.

Unusual Status

1. Unit exception (bit 7) at initial selection if:
 - a. End-of-file is on, and
 - b. The last card has been stacked by the preceding command.
2. Unit-check (bit 6) alone at initial selection for
 - a. Intervention required (sense bit 1)
 - b. Command reject (sense bit 0).
3. Unit-check (bit 6) with channel-end

Action (Figure 52)

1. Reader data is sent to program storage.
2. The card, whose data is sent to program storage, is fed to the specified stacker.
3. The next-card data is read into the

Assume command code = 01000010

- Specifies data mode 1 and stacker R2.

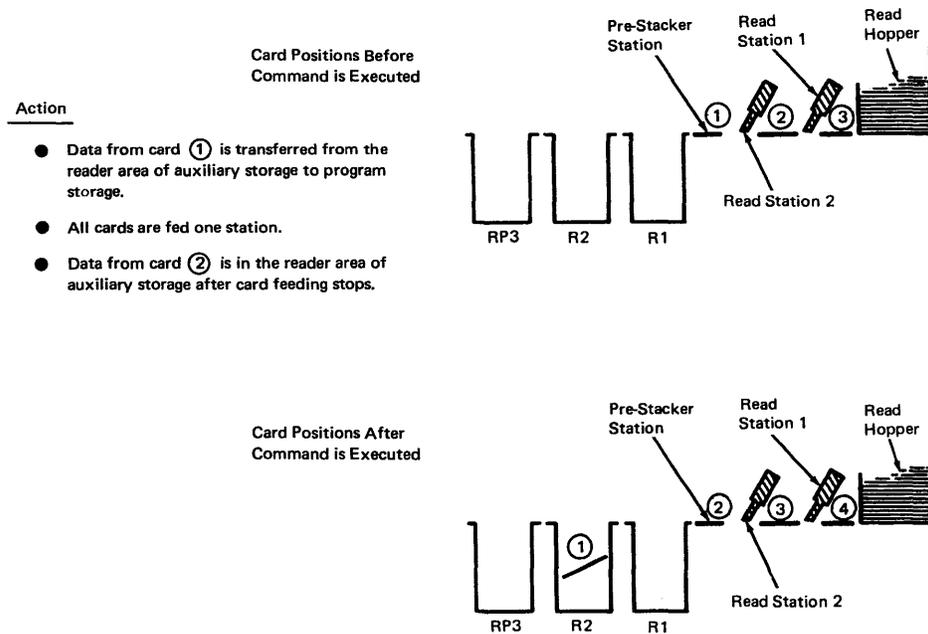


Figure 52. Read, Feed, and Select Stacker (Type AA)

- for:
- Equipment check (sense bit 3), or
 - Data check (sense bit 4). This check does not occur if column binary is installed and the operation is in data mode 2.
 - Unusual command sequence (sense bit 6) (See item 2 under Sequence.)

Action (Figure 53)

- Data is sent from the reader (or PFR, if PFR is installed and the command is sent to the punch) auxiliary storage area to the program storage area specified in the CCW.
- No card is fed.
- If the read and no feed or stacker selection command is issued to a punch without PFR, that command is rejected.

READ AND NO FEED OR STACKER SELECTION (TYPE AB)

Normal Ending Status

Command Byte

11C 00010

Channel-end and device-end are presented to the channel together after the end of data transfer.

Validity

- Valid to reader or punch (with PFR).
- Invalid to punch without PFR.

Unusual Status

- Unit-exception (bit 7) for the reader at initial selection if:
 - End-of-file is on, and
 - The last card has been stacked by the preceding command.
- Unit-exception (bit 7) for PFR at initial selection if:
 - End-of-file is on, and
 - The last card data has been sent to the CPU by a preceding read command.

Sequence

- Should follow a type AA or a type BA command.
- This command can follow itself. In this case, both commands are executed, but unit-check accompanies channel-end of the second command. Unusual command sequence (sense bit 6) is sent to the CPU on a subsequent sense operation.

Note: In this case, a card is still at the pre-check station. This card can be stacked by a write, feed, and select stacker command. Blank data codes can be sent for this command. This operation checks and stacks the

Assume command code = 11000010

- Specifies data mode 1.

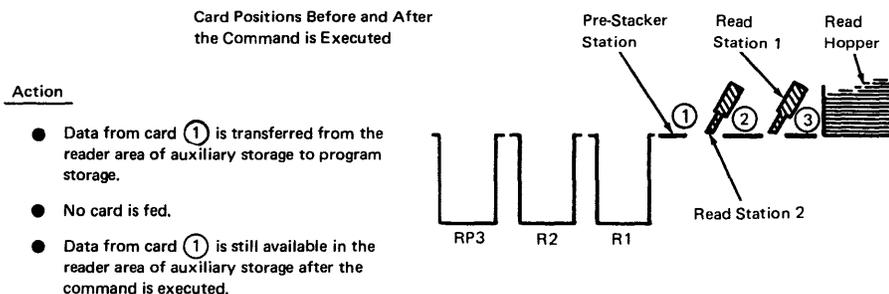


Figure 53. Read and No Feed or Stacker Selection (Type AB)

last card. Unit exception is given at each initial selection for read commands until the last card is stacked. After that card is stacked, the punch becomes not-ready.

FEED AND SELECT STACKER (TYPE BA)

Stacker	Command Fytc
R1	001 00011
R2	011 00011
RP3	101 00011

3. Unit-check (bit 6) alone at initial selection for:
 - a. Intervention required (sense bit 1), or
 - b. Command reject (sense bit 0) if the command is issued to a punch without PFR.

Validity

4. Unit-check (bit 6) with channel-end and device-end (they occur together) for:
 - a. Equipment check (sense bit 3), or
 - b. Data check (sense bit 4). This check does not occur for the reader if column binary is installed and the operation is in data mode 2. (PFR always operates in data mode 1.)
 - c. Unusual command sequence (sense bit 6). (See item 2 under Sequence.)

1. Valid for reader.
2. Invalid for punch (with or without PFR).

Sequence

1. Should follow a type AB or a type BB command.
2. Cannot be the first command to the reader after initial run-in.

Assume command code = 01100011

- Specifies stacker R2.

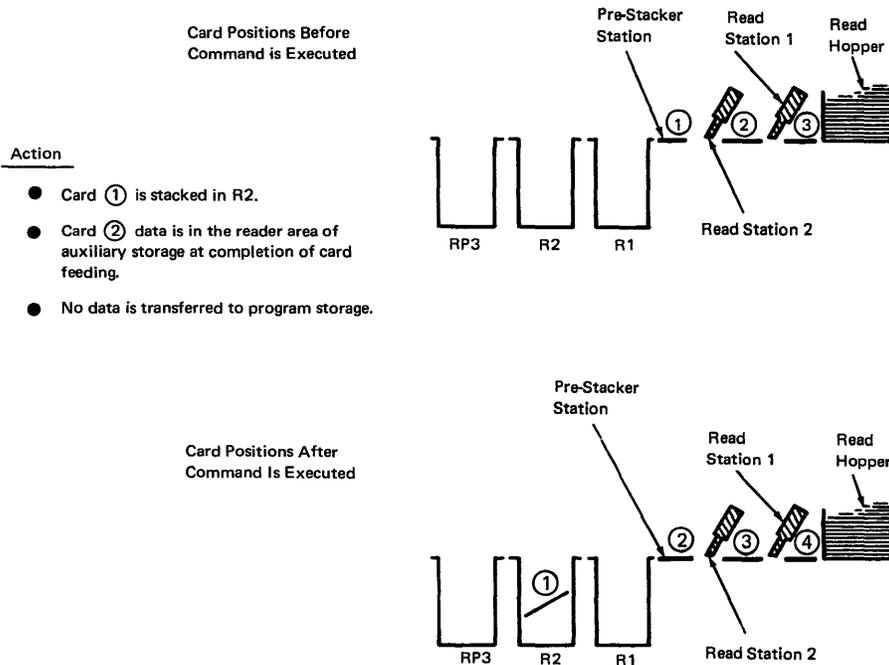


Figure 54. Feed and Select Stacker (Type BA)

Action (Figure 54)

1. The card stacked is the one whose data was sent to program storage on the preceding read command.
2. The data from the card passing the read station is read into the reader section of auxiliary storage. (The punched-hole patterns can be in data mode 1 or data mode 2; no check condition, if any, for mode is indicated until a read command is subsequently executed.)

Normal Ending Status

1. Channel-end is presented to the channel at initial selection (command immediate).
2. Device-end is presented to the channel after card reading (into auxiliary storage) is completed.

Unusual Status

1. Unit-check (bit 6) at initial selection for:
 - a. Intervention required (sense bit 1), or
 - b. Command reject (sense bit 0). The command is issued to the punch (with or without PFR); the command is the first to the reader after initial run-in; or, this command does not follow a type AB or a type BB command.
2. Unit-check (bit 6) does not occur with channel-end or device-end for this command.

PFR WRITE, FEED, AND SELECT STACKER (TYPE BA)

<u>Stacker</u>	<u>Command Byte</u>
P1	00C 01001
P2	01C 01001
RP3	10C 01001

Validity

1. Valid for the punch (with PFR only).
2. Invalid for the reader.

Sequence

Should follow a type AB or a type BB command.

Action (Figure 55)

A. First command after initial run-in:

1. Data is sent from program storage to the punch section of auxiliary storage.
2. A feed cycle is performed so that the data sent is punched into the card at the punch station.
3. Stacker selection specified by this command pertains to the card that is being punched. This stacker selection information is retained so that, on the next feed cycle, the card is stacked in the selected stacker.

B. Other than first command after initial run-in:

1. Data is sent from program storage to the punch area of auxiliary storage.
2. This data is punched in the card at the punch station.
3. Stacker selection specified by this command pertains to the card that is being punched.
4. The card punched by the preceding command is stacked as specified by that preceding command. If, however, data read at the punch check station does not compare with the total hole count from the data punched and the data read at the PFR brushes, the card read at the punch-check station is stacked in P1. The card punched on this command is also stacked into P1 on the next feed cycle.

C. If PFR is installed, data is read from the next card by the PFR brushes into the PFR area in auxiliary storage. The card read by these brushes stops at the pre-punch station.

Operation in data mode 2 (if column binary is installed) pertains only to the card being punched. The card read by the PFR brushes is always read in data mode 1. If column binary is not installed, the card is punched in data mode 1 regardless of the setting of bit 2 in the command byte.

ume command code = 10001001

- Specifies data mode 1 and stacker RP3.

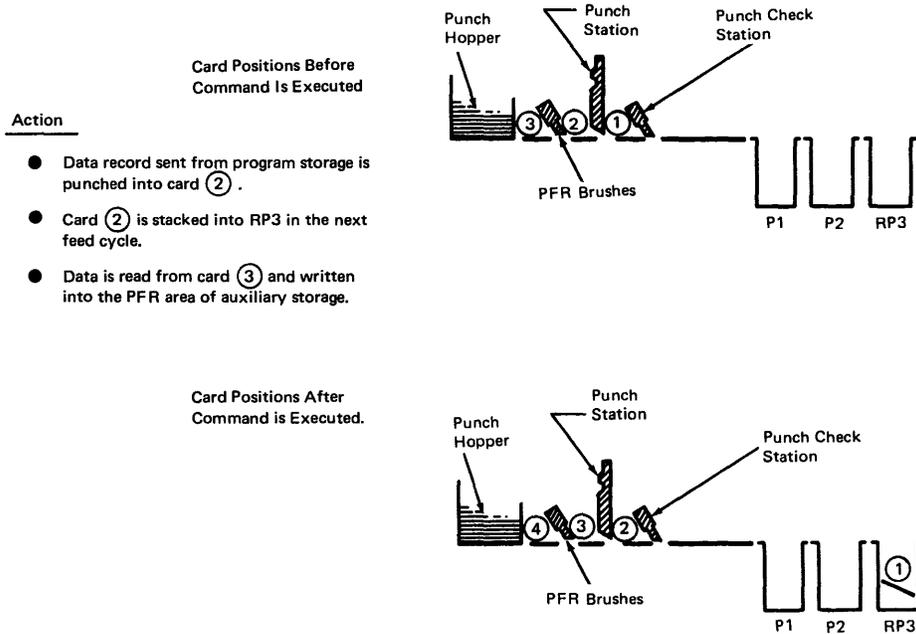


Figure 55. PFR Write, Feed, and Select Stacker (Type BA)

If PFR is not installed, this command functions in the same manner as the write, feed, and select stacker (type BB) command.

device-end for equipment check (sense bit 3). This indication specifies that the number of holes punched in the preceding card do not match the number of holes that should have been punched. Therefore, this check applies to the card punched on the preceding command. (Hole-count data from the PFR brushes and from the punch station are combined and compared with the punch-check-brush hole count, if PFR is installed.)

Normal Ending Status

1. Channel-end is presented to the channel after the end of data transfer from program storage to the punch area of auxiliary storage.
2. Device-end occurs after card punching is completed.

WRITE, FEED, AND SELECT STACKER (TYPE BB)

Unusual Status

1. Unit check (bit 6) alone at initial selection for:
 - a. Intervention required (sense bit 1), or
 - b. Command reject (sense bit 0). This command is sent to the reader or to the punch without PFR, or this command follows a type BA or a type AA command.
2. Unit-check (bit 6) is presented with

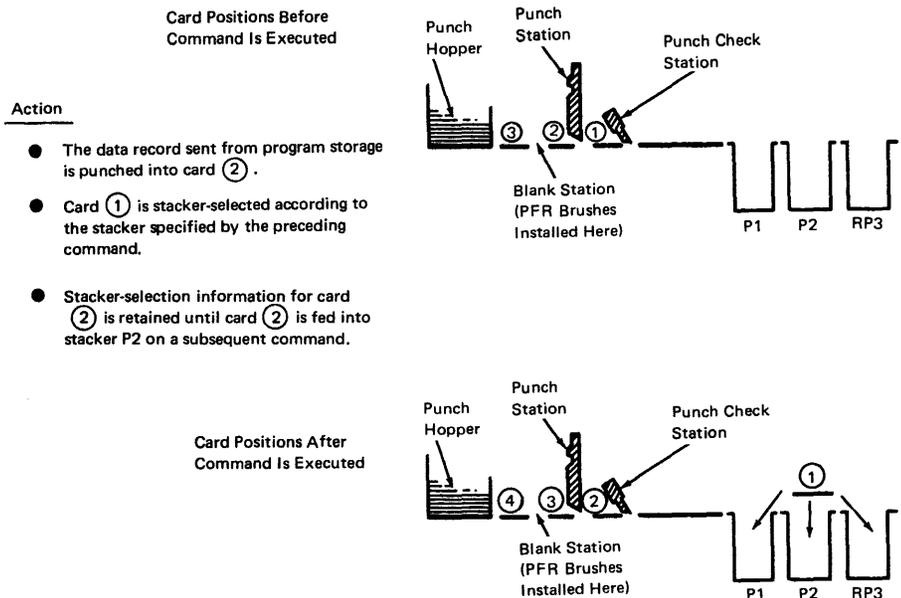
<u>Stacker</u>	<u>Command Byte</u>
P1	00C 00001
P2	01C 00001
RP3	10C 00001

Validity

1. Valid for the punch (with or without PFR)
2. Invalid for the reader.

Assume command code = 01000001

- Specifies data mode 1 and stacker P2.



Action

- The data record sent from program storage is punched into card ②.
- Card ① is stacker-selected according to the stacker specified by the preceding command.
- Stacker-selection information for card ② is retained until card ② is fed into stacker P2 on a subsequent command.

Card Positions After Command Is Executed

Figure 56. Write, Feed, and Select Stacker (Type BB)

Sequence

Should follow a type AB or a type BB command.

Unusual Status

The same as for the PFR write, feed, and select stacker (Type BA) command, except that this command does not cause a unit-check (due to command reject) if issued to the punch without PFR.

Action (Figure 56)

This command functions in the same manner as the PFR write, feed, and select stacker (Type BA) command except that card data is not read by the PFR brushes. If prepunched cards are punched by this command, hole-count checks occur because the prepunched hole patterns are not read by the PFR brushes.

SENSE AND NO-OP

The bit structures for these command are:

	<u>Operation Code Bits</u>							
	0	1	2	3	4	5	6	7
Sense	0	0	0	0	0	1	0	0
No-Op	0	0	0	0	0	0	1	1

Normal Ending Status

The same as for the PFR write, feed, and select stacker (Type BA) command.

The sense command should have an initial data count of 1, because the attachment returns only one sense byte for the device (reader or punch) addressed for the sense operation. Channel-end and device-end status are presented to the CPU after the sense byte is accepted by the CPU. Therefore, a sense operation is not an immediate operation.

INTEGRATED 2540 UNIT-STATUS BYTES

A unit-status byte indicates to the channel the condition or status of the input/output device involved. With the exception of busy and unit-check (caused by intervention required) any unit-status bits are reset in the attachment for the 2540 reader or punch when they have been accepted by the channel.

The unit-check caused by intervention required is reset only after the intervention required condition has been corrected.

Busy is reset only after device-end for an operation is cleared. If the device-end for an operation is cleared. If the device-end is cleared by a Start I/O, busy accompanies device-end in the CSW stored for the Start I/O operation. Busy is not indicated in the CSW stored as a result of executing a Test I/O to a device with outstanding status. If the device is busy performing an operation (channel-end for the operation has not yet occurred), when it is addressed for execution of the Test I/O instruction, the condition code is set to 2 and a CSW is not stored. If, however, the current device operation:

1. has progressed to the interval between channel-end and device-end, and
2. channel-end for the operation has already been cleared and stored in a CSW, and
3. the device (reader or punch) is addressed for execution of a Test I/O instruction,

then busy status is in the CSW stored as a result of execution of that Test I/O.

Note that the 2540 attachment presents separate status bytes to the channel: one for the reader, one for the punch. Only one unit-status byte, depending upon the unit involved, however, is presented to the channel at any specific time.

Bit 0--Attention

Not used.

Bit 1--Status Modifier

Not used.

Bit 2--Control Unit End

Not used.

Bit 3--Busy

Busy status, given at initial selection for a Test I/O instruction, indicates that the addressed device is performing a previously initiated operation, channel-end for the operation has already been stored in a CSW, but device-end for the operation has not yet occurred.

Busy status is in the CSW stored as a result of execution of a Start I/O instruction only if the device has outstanding status that does not include channel-end. (See the Integrated 2540 Status Byte Bit Combinations section.)

Bit 4--Channel-End

This bit indicates that data transfer, if any, between the addressed device (reader or punch) and the channel has been completed. The data transfer is completed at the end of the maximum record size for the operation (80 bytes for a data mode 1 record; 160 bytes in column binary, data mode 2) or when the channel specifies that the operation should be stopped (CCW data count has gone to zero).

Also, channel-end is presented to the channel as soon as a command for which no data transfer is required is accepted by the 2540 attachment for the addressed device. The commands that cause this action are called immediate commands and for the 2540 are:

1. For the reader
 - Feed and select stacker (Type BA)
 - No-Op
2. For the punch
 - No-Op

Bit 5--Device-End

This bit indicates that the reader (or the punch) has completed the previous command or has just been placed in the ready state. The device is then free to accept a new command.

The 2540 attachment attempts to present device-end (for the reader or punch) to the channel when the reader or the punch is made ready. This status must be accepted by the channel and indicated in a CSW before an operation for the affected unit can be initiated.

Device-end is presented to the channel with channel- end in the following instances.

1. For the reader
 - Read and no feed or stacker selection (Type AB) (after the end of data transfer for the command)
 - No-Op
 - Sense (after the sense byte has been transferred to the channel).
2. For the punch
 - Read and no feed or stacker selection (Type AB) (after the end of data transfer for the command; this command is used only when the punch has the PFR feature)
 - Sense (after the sense byte has been transferred to the channel)
 - No-Op.

Bit 6--Unit-Check

This bit indicates that the reader or punch requires program or operator intervention. It is a summary of sense bits 0, 1, 3, 4, and 6. See the descriptions of these bits for information concerning when unit-check is presented to the channel for the various commands.

Bit 7--Unit Exception (End of File)

This bit pertains to the reader or punch (with PFR) and indicates that the last card from the hopper has been read and stacked in the reader; or read but not stacked in the punch. These actions can occur only if end-of-file is on. (End-of-file is available in the punch only if the punch has the PFR feature installed.) Unit exception is given for read commands only; it is not given in punch write operations, even if PFR is installed. The unit-exception bit is reset under the following conditions.

1. For the reader
 - Pressing the stop key.
 - Acceptance of the unit-exception condition by the program.
2. For the punch

- Pressing the stop key.
- Any feed command. Note that for read commands, unit exception is present in the initial-selection status and the bit is not reset.

SENSE BYTES, 2540

The intervention-required sense bit is reset when the responsible condition is corrected. All other sense bits are reset the next time the program causes the 2540 to be selected, except when the selection is due to one of the following.

1. Test I/O instruction executed
2. Halt I/O instruction executed
3. Sense command initiated
4. No-Op command initiated.

The 2540 attachment provides two separate sense bytes: one for the reader, one for the punch. Only one byte or the other, however, is stored in the CSW on a sense command operation, depending upon which unit (the reader or the punch) is addressed for execution of this operation.

Bit 0--Command Reject

For the reader, command reject is set on for any of the following.

1. If a feed and stacker select command is given just after initial run-in, or if a feed and stacker select command does not follow a type AB or a type BB command.
2. Any write command, or any command operation byte bit-pattern not defined in this functional specification (for the 2540 reader) is issued to the reader.

For the punch, command reject is set on for any of the following.

1. A read, feed, and select stacker (Type AA) command is given.
2. A feed and select stacker (Type BA) is given.
3. A PFR write, feed, and select stacker (Type BA), or a write, feed, and select stacker (Type BB) command is given after any command type other than a type AB or a type BB command.
4. A read command is issued to a punch that does not have the PFR feature.

- 5 Any command byte bit-pattern not defined in this functional specification (for the 2540 punch) is issued to the punch.

In all cases, for both the reader and the punch, unit-check is presented to the channel at initial selection of the command for which the command-reject condition occurs.

Note also that if the column-binary feature is not installed, commands with bit 2 in the command byte set to 1 (i.e., data mode 2 is specified) are executed in data mode 1 and do not cause the command-reject indication.

Bit 1--Intervention Required

This bit indicates that some type of operator intervention is required. That is, for the addressed unit (reader or punch):

1. A stacker has become full (the stacker light is on),
2. The chip box has become full or is missing (punch only; the chips light turns on),
3. A feed check has occurred (in a portion of the feed that is not over the stackers; the feed-stop light turns on),
4. A transport check has occurred (a card feed problem over the stacker area has occurred; the transport Light turns on),
5. An empty-hopper condition occurs, or
6. The stop key for the affected unit is operated.

For all of these conditions, the unit is not ready and the ready light for that unit is off.

Unit-check status, due to an intervention-required condition, is returned to the channel only at initial selection (i.e., when a new command is issued to the affected device). Unit-check, however, is not reset, even though presented to the channel, until after the intervention-required condition is corrected. This unit-check is not returned to the channel during the selection sequence for a sense command, so that the sense command can be executed.

Bit 2--Bus-Out Check

This bit is not used for integrated 2540 operations.

In the 2540 attached to a 2821 Control Unit, bus-out check is turned on when a data byte or command byte with even parity is received from the channel by the 2821. Because the integrated 2540 on the System/360 Model 25 does not operate through the standard System/360 channel interface, data or command bytes are not handled in the same manner as in the 2540/2821. When such a parity check occurs in the integrated 2540 attached to the Model 25, the error is charged to the CPU, and a machine check occurs.

Bit 3--Equipment Check

Equipment check is set on, for the reader or punch, when:

1. A shift-register-sync error or an address check occurs (both of these are circuit errors in the 2540-attachment internal controls), or
2. A hole-count error is detected in the affected unit. This check, in the reader, is a result of a mismatch of the hole-patterns read from a card at the first read station compared to the hole-patterns read from the same card at the second read station.

In the punch, the hole count error is a result of a mismatch between the hole-patterns read from a card at the punch-check brushes compared to the number of holes that should have been punched in the card. If the punch has the PFR feature, the comparison is made between the:

- a. total hole count derived from the hole-patterns read at the PFR brushes and the holes punched at the punch station, and
 - b. the total hole-count read at the punch-check brushes.
3. Data overrun occurs. A data overrun can occur only when cards are being fed and is caused by an insufficient number of CPU cycles being made available for 2540 microprogram trap operations. The priority circuits are designed to guarantee the reader a sufficient number of cycles for data transfer. An overrun should never occur except as a failure in the priority circuits.

For the reader, overrun can occur:

- a. during run-in, or
- b. during any card-feed cycle in which a card is being read by the read brushes.

For the punch, overrun can occur;

- a. during run-in (even though no data is being punched or read), or
- b. during any card-feed cycle in which data is being punched.

In the reader, unit-check for this indication is sent only at channel-end for a read command and applies only to the card for which data is transmitted on the read. In punching, the unit-check indication is sent only with device-end on a write command and applies to the previous card punched. However, when punching, the unit-check may be sent with channel-end, if channel-end status has not been accepted within 170 milliseconds after completion of data transfer. If this occurs, the unit-check indication is also sent with device-end. In any case, the unit-check applies to the previous card punched.

For PFR only, the hole-count check is indicated by unit-check with device-end on the second write command (i.e., the command on which the card that was read at the PFR brushes is check-read at the punch-check brushes).

Bit 4--Data Check

This bit indicates that an invalid card code has been detected in the reader or in the punch (on PFR read operation only). The indication (i.e., unit-check) occurs with channel-end on a read command for both the reader and the punch (with PFR) and pertains to the card for which the data was sent to program storage. Data check indicates that more than one punch exists in rows 1 through 7 of any single card column. This check is not operative when data mode 2 is used. Data mode 2, however, is not used for PFR read operations.

The validity check is made when the data is read at the PFR brushes, not when a hole-count check is made at the punch-check brushes.

Bit 5--Overrun

Not used.

Bit 6--Unusual Command Sequence

On the reader or punch (with PFR), this indicates a read following a read with no intervening feed. Both read commands, however, are executed. (Unit-check is presented with channel-end of the second read command to indicate the condition.)

PROGRAMMING TIMING CONSIDERATIONS

CARD READING

The reader allows for either a 25-millisecond or a 20-millisecond maximum access time to the clutch on the 800-card-per-minute (51-column interchangeable read feed feature) and 1000-card-per-minute reader, respectively. That is, if a feed order is given to the card reader immediately following the clutch decision point (Figure 51) start of feeding is delayed for 25ms on the 800 cpm reader and 20ms on the 1000 cpm reader. If no cards have been fed for 30 seconds or more, the motor stops and a 500-millisecond clutch access is required on the next command.

To keep the reader running at maximum speed, a new feed command must be given after device-end but before the clutch-decision point. When the feed is given with a read command, the data transfer is completed before the clutch can be activated (Figure 57).

CARD PUNCHING

The punch allows a 50-millisecond maximum access time to the clutch. If no cards have been fed for 30 seconds or more, the motor stops and a 500-millisecond clutch access is required on the next command.

To keep the punch running at maximum speed, a new write command must be given and the data transfer completed before the clutch decision point following device-end (Figure 58).

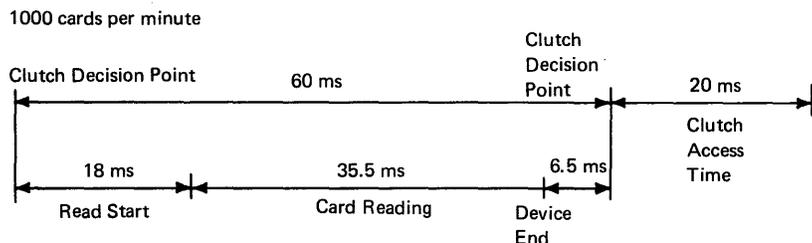
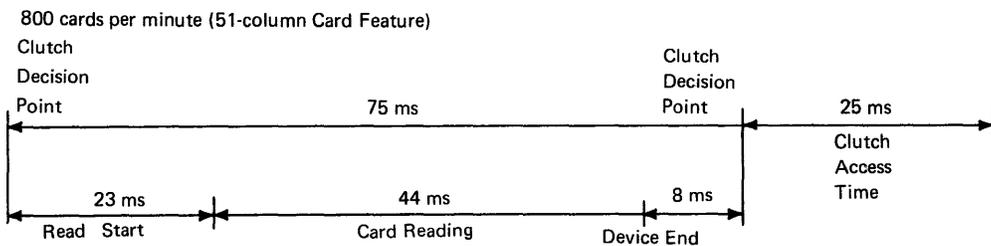


Figure 57. Card Read Timings (2540)

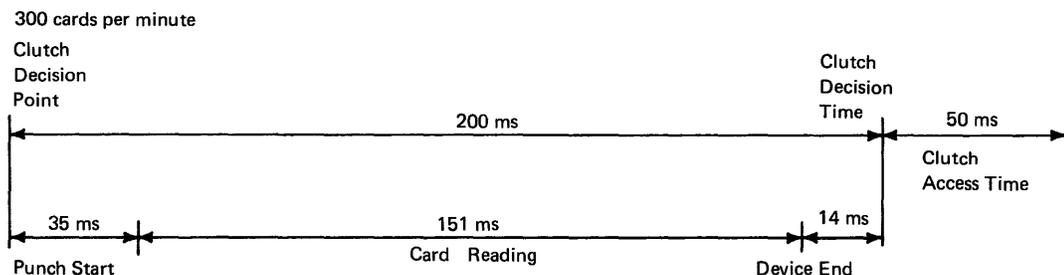


Figure 58. Card Punch Timings (2540)

CHANNEL-END TO DEVICE-END

The minimum time from generation of channel-end to generation of device-end is:

Reader

1. 1000 cpm 50ms
2. 800 cpm 63ms

Punch

300 cpm 175ms

HALT I/O INSTRUCTION TO 2540

The results of execution of a Halt I/O instruction to either the 2540 reader or punch are:

<u>Device Condition</u>	<u>Results of HALT I/O</u>
Not performing an operation	The condition code is set to 1; the status portions of the CSW are set to all zeros.

DATA TRANSFER RATE

Average data transfer time per byte is:

<u>Device</u>	<u>Data Mode 1</u>	<u>Data Mode 2</u>
From the reader:	$\frac{2.0\text{ms}}{80}$	$\frac{1.6\text{ms}}{160}$
To punch:	$\frac{3.4\text{ms}}{80}$	$\frac{4.3\text{ms}}{160}$

Between channel-end and device-end for a command-chained operation.

The condition code is set to 1; command chaining is suppressed; the status portions of the CSW are set to all zeros; channel-end, for the operation, will not subsequently be indicated. Device-end, after it occurs, will cause an I/O interruption, or this device-end can be cleared by a Test I/O instruction.

there is no outstanding 2540 unit status.

Note: Even if the addressed device is not ready, a sense command is accepted and the all-zero status is returned to the channel (but not stored in the CSW).

The device has outstanding status for an operation, or device-end for a not-ready-to-ready transition.

The condition code is set to 0.

2. 0001 0000 (Busy Bit)

The response to any command (or Test I/O instruction) issued to the reader or punch when the device is between channel-end and device-end for the operation, and channel-end has previously been stored in the CSW.

3. 0000 0001 (Unit-Exception Bit)

First occurs at initial selection in response to a read command to the reader or punch (with PFR), and indicates that the last card in the hopper has been read (data sent to program storage) and stacked in the reader; or read but not stacked in the punch.

INTEGRATED 2540 STATUS-BYTE BIT COMBINATIONS

The following are status combinations that can be sent to the CPU by the 2540 attachment. For information as to how status is placed in the CSW, refer to IBM System/360 Principles of Operation, Form A22-6821.

Note that there should never be a status combination that includes a 1 in bit positions 0, 1, or 2.

Those combinations that should not occur will occur only as a result of a machine malfunction.

4. 0001 0001 (Busy and Unit-Exception Bits)

Occurs only during initial selection when the command byte is not for a Test I/O instruction execution. This combination is caused by combination-3 status being stacked by the channel.

1. 0000 0000

This is the normal response to a valid command when the addressed device (reader or punch) is ready and not busy. This response indicates that the command is accepted. However, this status is not placed in the CSW when a command is accepted.

All-zero unit status can appear in the CSW:

- a. As a result of an I/O interruption to clear a PCI for the device when no ending unit status is outstanding for that device (i.e., the chain is still in progress), or
- b. If a CSW is stored as a result of channel error status conditions (such as program check or protection) when

5. 0000 0010 (Unit-Check Bit)

Occurs only at initial selection (if this status had not been stacked on a previous sequence). This combination indicates that the device could not accept the command because of sense bits 0 or 1.

6. 0001 0010 (Busy and Unit-Check Bits)

Occurs only:

- a. during initial selection, and
- b. for a command other than a Test I/O.

This combination is caused by combination 5 status being stacked by the channel.

7. 0000 0011

Should not occur.

8. 0001 0011

Should not occur.

9. 0000 0100 (Device-End Bit)

Indicates that:

- a. An operation involving mechanical motion has been completed, or
- b. The device has gone from the not-ready to ready state.

This combination is given only in response to a Test I/O, or when presenting status in a sequence initiated by the 2540 attachment.

10. 0001 0100 (Busy and Device-End Bits)

Same as 9 except that this combination occurs only:

- a. during initial selection, and
- b. for a command other than a Test I/O.

11. 0000 0101

Should not occur.

12. 0001 0101

Should not occur.

13. 0000 0110 (Device-End and Unit-Check Bits)

Indicates that:

- a. A punch operation has been completed and that sense bit 3 is on, or
- b. The device has gone from the not-ready to ready state and then reverted to the not-ready state before the 5-bit being accepted, or
- c. Unit-check status (due to sense bit 0) was stacked by the channel and the device went from the not-ready to the

ready state before the 6-bit was accepted.

This combination is given only in response to a Test I/O instruction, or when presenting status in a sequence initiated by the 2540 attachment.

14. 0001 0110 (Busy, Device-End, and Unit-Check Bits)

The same as combination 13 except that this combination occurs only:

- a. during initial selection, and
- b. for a command other than a Test I/O.

15. 0000 0111

Should not occur.

16. 0001 0111

Should not occur.

17. 0000 1000 (Channel-End Bit)

Indicates that the device is still performing the mechanical portion of the operation (i.e., device-end has not yet occurred). This combination is given only for a Test I/O instruction execution, or when status is presented in a sequence initiated by the 2540 attachment.

18. 0001 1000

Should not occur.

19. 0000 1001

Should not occur.

20. 0001 1001

Should not occur.

21. 0000 1010 (Channel-End and Unit-Check Bits)

Indicates (for the reader only) that:

- a. Data transfer has been completed for a read, feed and stacker select command,
- b. The reader is taking a feed, and
- c. Any one or more of sense bits 3, 4, and 6 is on.

This combination can also occur while punching if channel-end status has not been accepted within 170ms after completion of the data transfer. In this case, sense bit 3 would be on.

This combination occurs only as a result of execution of a Test I/O instruction or when the status presentation sequence is initiated by the 2540 attachment.

22. 0001 1010

Should not occur.

23. 0000 1011

Should not occur.

24. 0001 1011

Should not occur.

25. 0000 1100 (Channel-End and Device-End Bits)

Indicates that the device has completed an operation for which channel-end and device-end occur together. Or, if channel-end occurs before device-end in an operation, this combination indicates that channel-end was not cleared before device-end occurred.

26. 0001 1100

Should not occur.

27. 0000 1101 (Channel-End, Device-End, and Unit-Exception Bits)

This combination should not occur.

28. 0001 1101

Should not occur.

29. 0000 1110 (Channel-End, Device-End, and Unit-Check)

Indicates that the device has completed an operation but channel-end and device-end status has not yet been accepted by the channel and:

- a. One or more of sense bits 3, 4, and 6 is on for a read, or
- b. Sense bit 3 is on for a write.

This combination occurs only as a result of execution of a Test I/O instruction, or when status is presented in a sequence initiated by the 2540 attachment.

30. 0001 1110

Should not occur.

31. 0000 1111 (Channel-End, Device-End, Unit-Check, and Unit-Exception Bits)

Should not occur.

32. 0001 1111

Should not occur.

POSSIBLE COMBINATIONS OF SENSE BITS IN A SENSE BYTE

Assume, for these descriptions, that the previous command had been executed, and that the unit-check status was given with channel-end or device-end, except where noted.

<u>Previous Command</u>	<u>Sense Bits</u>
Read (reader or punch with PFR)	Any one or more of the following: B3 - equipment check B6 - unusualecommand (and possibly B1 - intervention required).
Feed and Stacker Select	Possibly B1- intervention required (the operator might have pressed the stop key). <u>Note:</u> There is no unit-check indication with channel-end or device-end for this command.
Write	B3 - equipment check (and possibly B1 - intervention required).

Restarts from Error Conditions

The 2540 uses the flexible System/360 command set; therefore, different external error conditions can each require different restart procedures, depending on whether the 2540 operation is reading, punching, or PFR. If the program provides some programmed message to indicate the 2540 sense conditions (such as PR-KB typeout), the operator can use this message to determine which specific restart procedure he should follow. To locate the error card for read-check and validity-check errors, the operator should be familiar with the type of processing used by the program: that is, whether the program is reading and stacking each card with a single command, or delaying the stacker selection until the data from the card is analyzed.

Figure 59 shows the various 2540 error indications and appropriate restart procedures for standard operations, and for PFR operations.

SUGGESTED 2540 OPERATING AND RESTART PROCEDURES

Initial Start

To begin operation with the 2540 reader:

1. Perform an NPRO (nonprocess runout) operation by opening the jogger gate, emptying the hopper, and pressing the reader start key to ensure that no cards are left in the feed.
2. Load the desired cards into the hopper of the file-feed magazine, and close the jogger plate. Card decks less than one-inch thick should be placed directly in the hopper with the card weight; larger decks can be placed in the file-feed magazine.
3. Press the reader start key.

To begin operation with the 2540 punch:

1. Perform an NPRO operation by emptying the hopper and pressing the punch start key.
2. Load the desired cards into the punch hopper.
3. Press the punch start key.

Jam Removal

For a description of how card jams can be cleared from the 2540, refer to IBM 2540 Component Description and Operating Procedures, Form A21-9033.

RESETS

During a power-on reset, both the punch and reader are reset to a not-ready condition. A system reset resets everything in the 2540 that a power-on reset affects, except reader-ready and punch-ready.

The system reset pertains only to units that are on-line. This reset should be given only when the devices are not in mechanical motion. If devices are in mechanical motion when a system reset is performed, results are unpredictable, and the system reset might cause errors that could go undetected.

If there is any doubt about the status of the devices at the time the reset is given, operations with the 2540 should be terminated. The program should then revert to the last checkpoint applicable to the 2540.

USE METER (2540)

and punch feeds) are cleared. Operation of this meter also requires that the customer meter on the 2025 CPU be operating.

The 2540 use meter records time from the acceptance of the first read or write command until both card transports (read

Indications	Restart Procedures
<p>Reader Feed Stop Light (Only) Sense Bit 1--Intervention Required (Only)</p> <p>Note: If read check/bit 3 or validity check/bit 4 indications accompany feed stop/bit 1, follow procedure for read check or validity check.</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker R1. 2. Open hopper jogger gate and remove cards from hopper. 3. Open covers and remove any jammed cards from read feed. Reconstruct any damaged cards. 4. With jogger gate still open, press reader start key to clear feed. 5. Remove cards just run out into stacker R1, place them and any reconstructed cards, in proper sequence, ahead of cards removed from hopper, and replace this deck in hopper or ahead of cards in file feed magazine. 6. Close jogger gate. 7. Press reader start key.
<p>Reader Feed Stop Light Reader Check Light Sense Bit 1--Intervention Required (Only)</p>	<p>This combination of error indications accompanies a 2540 read clutch failure; there may be cards in stacker R1 that have not been read. Restart the job from the last checkpoint.</p>
<p>Read Check Light Sense Bit 3--Equipment Check</p> <p>(If card is read and stacked with single command.)</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker R1. Determine (perhaps with aid from programmed message) which was last card read into processing unit, and correct any off-registration punching in it. Place this corrected card in stacker R1. 2. Open jogger gate and remove cards from hopper. 3. With jogger gate open, press reader start key to clear read feed. 4. Remove cards from stacker R1 and place them ahead of cards removed from hopper. Place this deck in hopper or ahead of cards in file feed magazine. 5. Close jogger gate. 6. Press reader start key.
<p>Read Check Light Sense Bit 3--Equipment Check</p> <p>(If stacker selection is delayed.)</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker R1. 2. Follow steps 2-6 of preceding procedure, correcting any off-registration punching in first card run out into stacker R1.
<p>Validity Check Light Sense Bit 4--Data Check</p> <p>(If card is read and stacked with single command)</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker R1. Determine (perhaps with aid from programmed message) which was last card read into processing unit (this card may be in another stacker) and correct any errors in this card. Place the corrected card in stacker R1. 2. Open jogger gate and remove cards from hopper. 3. With jogger gate open, press reader start key to clear read feed. 4. Remove cards from stacker R1 and place them ahead of cards removed from hopper. Place this deck in hopper or ahead of cards in file feed magazine. 5. Close jogger gate. 6. Press reader start key.

Figure 59. Restart Procedures - Standard and PFR Operation (Part 1 of 3)

Indications	Restart Procedures
<p>Validity Check Light Sense Bit 4--Data Check</p> <p>(If stacker selection is delayed.)</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker R1. 2. Open jogger gate and remove cards from hopper. 3. With jogger gate open, press start key to clear read feed. 4. Locate and correct invalid character(s) in first card in stacker R1. 5. Place corrected card ahead of cards in stacker R1. Place all cards in stacker R1 ahead of cards removed from hopper. Place this deck in hopper or ahead of cards in file feed magazine. 6. Close jogger gate. 7. Press reader start key.
<p>Validity Check Light Punch Check Light Sense Bit 3--Equipment Check Sense Bit 4--Data Check</p> <p>(If 2540 is performing PFR read operation.)</p>	<ol style="list-style-type: none"> 1. Remove card from punch hopper. 2. Press punch start key to clear punch feed. 3. Remove last three cards from stacker P1. 4. The first of these three cards may have to be reconstructed because it has been read and punched but not punch-checked. 5. The second card caused the validity check. Correct it as necessary. 6. Place these three cards, after any necessary corrections, in front of the cards removed from the hopper. Place this deck in the hopper. 7. Press the punch start key. 8. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the reading of the first card run out of the punch feed in step 3. Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.
<p>Punch Feed Stop Light (Only) Sense Bit 1--Intervention Required Only</p> <p>(If the 2540 is not performing PFR operations.)</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker P1. 2. Remove cards from hopper. 3. Open covers and remove any jammed cards from punch feed. 4. Press punch start key to clear punch feed. 5. Discard last card punched (2540 will repunch this card automatically). 6. Replace blank cards in hopper and press punch start key. Last card will be repunched automatically and 2540 enters ready status.

Figure 59. Restart Procedures - Standard and PFR Operation (Part 2 of 3)

Indications	Restart Procedures
<p>Punch Feed Stop (Only) Sense Bit 1--Intervention Required (Only)</p> <p>(If 2540 is performing PFR operation.)</p>	<ol style="list-style-type: none"> 1. Remove cards from stacker P1. 2. Remove cards from hopper. 3. Open covers and remove any jammed cards from punch feed. Press punch start key to clear feed. 4. Any card removed or run out from between punch station and punch check brushes should be reconstructed, because it has been punched but not punch checked. 5. Place reconstructed cards and cards run out into stacker P1 in proper sequence ahead of cards removed from hopper, and place this deck in hopper. 6. Press punch start key. 7. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the first card removed or run out to be read at the PFR station. <p>Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.</p>
<p>Punch Check Light Sense Bit 3--Equipment Check</p> <p>(If 2540 is not performing PFR operation and is using stacker P1.)</p>	<ol style="list-style-type: none"> 1. Remove cards from hopper. 2. Press punch start key to clear punch feed. 3. Remove last four cards from stacker P1. The last two cards are blank; the first two should be discarded. 4. Replace blank cards and cards removed from hopper in hopper. 5. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the first card removed from stacker P1 to be punched. <p>Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.</p>
<p>Punch Check Light Sense Bit 3--Equipment Check</p> <p>(If 2540 is not performing PFR operation and is not using stacker P1.)</p>	<ol style="list-style-type: none"> 1. Examine and correct, if necessary, error card, which is last card in stacker P1. (2540 automatically routes error cards to stacker P1.) 2. Place this card in appropriate stacker. 3. Press punch start key. 4. The 2540 will force the card following the error card into stacker P1, also. Place this card in the appropriate stacker. <p>Note: Because the error card and the card following it are both directed to stacker P1, the program can correct a non-PFR punch check without operator intervention by repunching both cards and directing them to appropriate stackers. The operator can then discard all cards in stacker P1 at the end of the job.</p>
<p>Punch Check Light Sense Bit 3--Equipment Check</p> <p>(If 2540 is performing PFR operation.)</p>	<ol style="list-style-type: none"> 1. Remove cards from punch hopper. 2. Press punch start key to clear feed. 3. Remove last four cards from stacker P1. The last two cards are correct; pre-punching in the first two must be reconstructed. 4. Place the two reconstructed cards, the two correct cards, and the cards removed from the hopper, in that sequence, in the hopper. 5. Reconstruct internal data in the system as necessary to restart at the Start I/O instruction that caused the first reconstructed card to be read at the PFR station. <p>Note: In some programs, reconstruction of internal data may not be provided for. In that case, restart the job from the last checkpoint.</p>

Figure 59. Restart Procedures - Standard and PFR Operation (Part 3 of 3)

INPUT/OUTPUT CHANNEL CHARACTERISTICS

The standard interface I/O channels for the Model 25 are identical to those of other System/360 systems. For a complete description of channel operation, refer to IBM System/360, Principles of Operation, Form A22-6821. For details on the channel standard interface, refer to IEM System/360, I/O Interface-Channel to Control Unit-OEMI, Form A22-6843. This publication covers the basic philosophy and defines the limitations imposed by the Model 25. The standard interface is not discussed. For information about I/O devices attaching to the standard interface, refer to IBM System/360, Bibliography, Form A22-6822.

The IBM System/360 Model 25 has the option of either a multiplexer channel or a selector channel as a special feature. It cannot have both. A multiplexer channel is best suited for operating a number of medium and low-speed devices simultaneously. The individual device requests time to transfer a byte of data as required. A multiplexer channel can also transfer data in multibyte and burst modes for those devices that require more data. In these modes, however, a single device has exclusive use of the channel during the transfer period. All other devices operating on the channel must wait until the operation is completed. If the wait exceeds their data transfer rate, the data requests cannot be handled, and these devices end their operations with an overrun error. The selector channel option is best suited when devices require a higher rate of data transfer. Devices on the selector do not time-share. Each device has exclusive use of the channel during the data transfer (burst mode). Any I/O device that does not exceed the selector channel data rate can overlap with all integrated I/O devices except 2311 files.

STANDARD I/O INTERFACE

The standard System/360 I/O channel interface is used to connect the CPU channel to any similarly equipped I/O device or device control unit. The interface is a cable connection having input data lines, output data lines, and control lines. These lines along with the channel controls and the controls in the device control unit can operate any connected I/O device. All of the devices

connected to the channel connect to the same group of lines. Selection of a specific device on the channel is made by addressing the device for an initial instruction. In the multiplexer channel the device can also request service and be honored through a priority connection system described under the Multiplexer Channel.

The standard System/360 is control-unit limited. This restriction also applies to the Model 25 multiplexer or selector channel. Only eight control-unit positions are available on the channel. A single control-unit position is needed for each of the following conditions.

1. An I/O device that has its own control unit (e.g., 1443 Printer)
2. A unit that services several I/O devices concurrently (e.g., a 2821 Control Unit with a 2540 Reader/Punch and 1403 Printers)
3. A control unit that is shared with several attached devices of which only one of the devices can operate at a time (e.g., a tape control unit with multiple Magnetic Tape Drives).

CHANNEL DEVICE ADDRESSING

Before a command for operation of an I/O device can be sent to its control unit, the device must be addressed. The address is derived from an I/O instruction and consists of the low-order 16 bits of the developed address. The channel address is contained in the eight high-order bits, and the device address is in the eight low-order bits, as follows.

	<u>Channel Address</u>	<u>Device Address</u>
Bit Position	16-23	24-31

The channel addresses are assigned as the following hex values.
Multiplexer Channel (Channel 0) 00
Selector Channel (Channel 1) 01.

The eight bits assigned to the device address can define 256 different addresses ranging as follows.

<u>Binary Value</u>	<u>Hex Value</u>	<u>Decimal Value</u>
0000 0000	00	0
to	to	to
1111 1111	FF	255

Limitations on the use of the device addresses are discussed under the individual channels.

INPUT/OUTPUT DEVICES FOR CHANNEL

The following devices are available for attachment to the System/360 Model 25. See IBM System/360 Model 25, Configurator, Form A24-3511, and IBM System/360 Input/Output Configurators, Form A22-6823, to determine what features are required for the particular application.

These IBM devices are listed in numerical order, although some require the presence of a control unit. Refer to the SRL publication pertaining to the individual device for further information.

- Card Readers, Card Punches, Printers, and Control Units
 - 1403 Printer Models 2, N1, 7
 - 1404 Printer Model 2
 - 1442 Card Read-Punch Model N1
 - 1442 Card Punch Model N2
 - 1443 Printer Model N1
 - 1445 Printer Model N1
 - 2501 Card Reader Model B1, B2
 - 2520 Card Read-Punch Model B1
 - 2520 Card Punch Model B2, B3
 - 2540 Card Read Punch
 - 2821 Control Unit
- *Magnetic Tape and Tape Control Units
 - 2401 Magnetic Tape Unit Model 1
 - 2415 Magnetic Tape Unit and Control Models 1, 2, 3, 4, 5, and 6
 - 2803 Tape Control Model 1

*Magnetic Tape Units cannot be installed on the Multiplexer Channel.
- Magnetic Character Readers
 - 1259 Magnetic Character Reader Model 2
 - 1412 Magnetic Character Reader
 - 1419 Magnetic Character Reader
- Optical Readers
 - 1231 Optical Mark Page Reader Model N1
 - 1285 Optical Reader
 - 1287 Optical Reader
 - 1418 Optical Character Reader Models 1, 2, 3
 - 1428 Alphameric Optical Reader Models 1, 2, 3
- Display and Display Control Units
 - 2260 Display Station
 - 2848 Display Control Models 1, 2, 3

- Paper Tape Readers and Controls Units
 - 2671 Paper Tape Reader
 - 2822 Paper Tape Reader Control
- Communication Terminals and Control Units
 - 1030 Data Collection System
 - 1050 Data Communication System
 - 1060 Data Communication System
 - 1070 Process Communication System
 - 2701 Data Adapter Unit
 - 2702 Transmission Control Unit
 - 2703 Transmission Control (32 lines max)
 - 2740 Communication Terminal
 - 2741 Communication Terminal
 - 7770 Audio Response Unit Model 3
 - 7772 Audio Response Unit
- Data Acquisition and Control System
 - 1801 Processor Control
 - 1802 Processor Control
 - 1826 Data Adapter Unit
 - 1827 Data Control Unit
 - Analog/Digital Input Features
 - Analog/Digital Output Features

MULTIPLEXER CHANNEL

The multiplexer channel of the Model 25 is composed of 32 subchannels, each of which is capable of controlling one I/O device. The operations performed on the various subchannels are executed concurrently with each other together with processing unit functions and integrated device operations. Each subchannel has its functional control data stored in a 64-bit Unit Control Word (UCW) contained in auxiliary storage.

The processing unit registers and special microprogram routines contained in control storage are used to perform the multiplexer channel operations. These operations consist of updating the main storage address to or from which data is moved, decrementing the count field for each byte transferred, and executing appropriate ending routines (such as storing the status). As each device requests service, its UCW is brought out of auxiliary storage, used, updated, and returned to storage when the operation is completed. Hence, the UCW carries a running record of the operation for the I/O device assigned. During the channel routine, the pertinent processing unit data is preserved in local storage. At the end of a channel routine, this data is returned to auxiliary storage and processing continues.

When channel-0 operates in either burst or multibyte mode, the processing unit operation is held up until the required data transfers are completed. Any previously started operations on the

integrated devices continue to operate in the normal manner through either file share cycles or trap routines. The times required for these share cycles and trap routines reduce the maximum data transfer speed of the multiplexer channel. The integrated devices that have a higher data transfer priority receive service first.

The multiplexer channel can handle the data rates for connected devices as specified in Figure 60. These figures express the data rates permissible in thousands of data bytes per second. They are representative of several worst-case combinations of I/O device overlap. Because all of the integrated I/O devices may not be installed, a specific case will be somewhat better than stated but not as high as the next level in the chart. Considering that most channel operations involve more than one device, the expressed data rates are the composite worst-case conditions for the connected devices. The lower data rates in the chaining column allow for the time required to obtain the new command (for data area) between data characters.

Degree of Overlap	Without Data Chaining	With Data Chaining
No Overlap with integrated attachments	27 KB	13 KB
Overlap with integrated Reader/Punch/Printer/Printer-Keyboard	11 KB	5.5 KB
Overlap with integrated Disk-File only	9.5 KB	4.2 KB
Overlap with integrated Reader/Punch/Printer/Printer-Keyboard/Disk-File	4.5 KB	2.2 KB

Figure 60. Maximum Tolerable Aggregate Interface Data Rates for Channel 0

MULTIPLEXER CHANNEL DEVICE PRIORITY

The priority on the multiplexer channel with which service requests are processed depends upon the sequence of the device attachment on the interface cable. The device that is electrically first on the cable select line has highest priority. If the first device does not have a request waiting, it passes the option along to the

next device in the electrical sequence. To reduce the overall interface cable length, the select line is routed out through the composite length of the cable and returned back to the channel interface. The normal connection with all devices connected in order along the outbound select line is shown in Figure 61. Here control unit A has the highest priority followed by B, C, and D. A limited amount of change in priority sequence can be made by connecting one or more of the control units on the return line instead of the outbound line. Figure 62 shows one example of sequence change with the original cable connections. Here control unit B has the highest priority followed by D, C, and A.

When the desired placement of I/O devices with the shortest cable routing does not lend itself to the required sequence, it is necessary to change the cable routing to one that does produce the desired sequence. In planning the connection, note that the first control unit on the interface cable must be either highest or lowest priority. The second unit can be either the alternate or next to the first unit as high or low. The third control unit can range from either extreme to third high or third low, depending on the first two.

The priority sequence for devices on the multiplexer channel is determined by the device requirements for data transfer. Devices operating in multiplexer mode (byte) fall into four basic groups as follows with devices arranged in data rate sequence within groups.

1. Highest priority must be given to unbuffered synchronous devices. These devices transfer data at a fixed rate, and failure to honor a request within the prescribed period results in an overrun error. This group includes input devices and certain output devices that have fixed data rates.
2. Unbuffered asynchronous devices are given priority just below that of the synchronous group. In this group, if a data byte does not reach the device within the prescribed time, the device can wait for data and does not overrun. This group contains mostly serial operating output devices that operate mechanically with the presence of the data.
3. Buffered synchronous devices are placed just below the unbuffered devices in priority. This group, because of a prestarted mechanical motion, must receive the data into or out of its buffer before the end of a prescribed time or the throughput is reduced. An

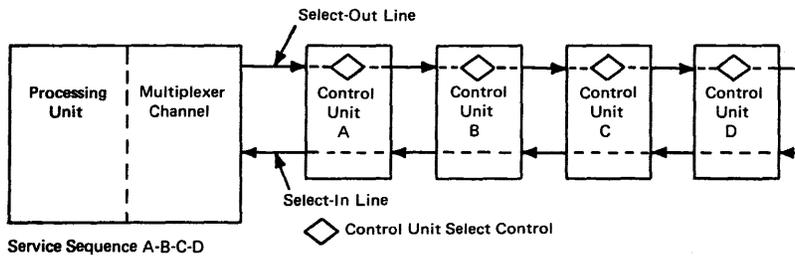


Figure 61. Priority Servicing, Normal Sequence

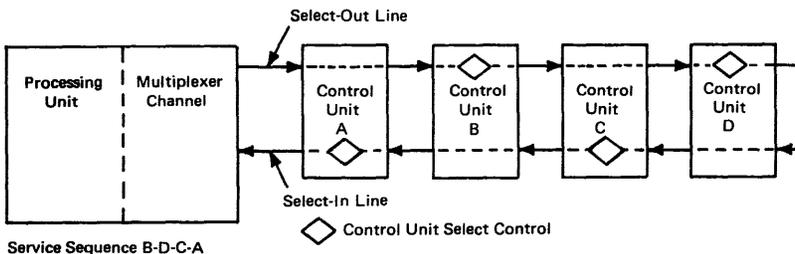


Figure 62. Priority Servicing, Selected Sequence

example of this group is the 2540 Reader-Punch operating through the 2821 Control Unit. Refer to the SRL publication for the particular I/O units for device dependent mechanical timings.

4. Lowest priority is assigned to devices that are buffered and operate asynchronously. These devices do not initiate their mechanical operation until the buffer is loaded. Waiting for data does not cause an overrun error. An example of this group is the 1403 Printer operating through the 2821 Control Unit.

The IBM 2520 Card Read-Punch does not fall into a single priority group because the reader is unbuffered synchronous (group 1) and the punch is buffered synchronous (group 3). In most cases it can perform both functions without overrun when it is placed between group 2 and group 3. In cases where one function is used more than the other, it may be desirable to change this assignment.

MULTIPLEXER CHANNEL DEVICE ADDRESSING

The multiplexer channel address (eight high-order bits of the 16-bit address) is 00 hex. Device addressing on the multiplexer channel depends upon how a

device and its control unit operate with the channel. The Model 25 multiplexer channel has 32 subchannels, each of which is associated with an individual device address. For devices that have their own control unit self-contained, and for control units that operate two or more devices simultaneously (such as the 2821), individual subchannel addresses are assigned to each device. These addresses are designated with a 0-bit in the high-order position of the device address. All of the 32 subchannels can be assigned to individual control units using the following addressing.

Subchannel (UCW)	Device Address	
	Binary	Hex
0	0000 0000	00
to	to	to
31	0001 1111	1F

For a third class of control units that can operate two or more devices of which only one can operate at a time, a single subchannel can be used with a special addressing scheme. The first eight subchannels also can be addressed and operated as shared subchannels. In this case, the 0-bit position of the device address is set to 1. The remaining three bits of the high-order byte are used to designate the subchannel instead of the normally used three bits in the low-order

Degree of Overlap	Without Data Chaining	With Data Chaining
No overlap with integrated attachments	30 KB	22 KB
Overlap with integrated Reader/Punch/Printer/Printer-Keyboard	30 KB	10 KB

Figure 63. Maximum Tolerable Aggregate Interface Data Rates for Channel 1

SELECTOR CHANNEL DEVICE PRIORITY

Devices on the selector channel do not have to be considered for their priority in receiving service because each device remains connected to the channel until the operation is completed. The devices may be

placed in appropriate locations and the interface cable routed for the shortest path. All devices are normally connected to the outbound select line, but they may be connected to the inbound line with the same result.

SELECTOR CHANNEL DEVICE ADDRESSING

The selector channel address (eight high-order bits of the 16-bit address) is 01 hex. Device addressing on the selector channel may in theory be any of the 256 possible bit combinations. The addressing is limited at two points by the integrated disk storage devices that are also assigned to channel 1 and addressed 9X (Hex). The value of X ranges from 0 to 3 for the four possible disk drives. The remaining addresses have no special significance in the processing unit, and may be assigned as required by the program for the selector channel devices.

APPENDIX A: AUXILIARY STORAGE MAPS

This Appendix shows the allocation of various auxiliary-storage areas for System/360 mode operation. For information on the usage of auxiliary storage while in 1400 emulator mode, refer to the 1401/1440/1460 Compatibility section.

Depending on the program-storage capacity of the system, there are from eight to sixteen 256-byte modules of auxiliary storage. Module 0 is used for CPU functions (general registers, etc.) and for storage of addresses and information relative to the integrated I/O attachment features. Module 2 is used for multiplexer-channel unit-control words. Modules 1 and 3-7 are used for operations involving the integrated attachment features. Modules 8-15 are reserved for special features. The 24K system is an exception (Figure 65).

Because Modules 0 and 2 are sometimes required by the operator or programmer, they are shown in this Appendix.

The coordinate at the top of these maps is in the form "x0" through "xF". The "x" can range from 0-F and is the tens position. The tens coordinate is given in the left margin.

Aux Stor Mod.	Usage	Rel. Byte Loc.	No. of Bytes
0	CPU Area	00-FF	256
1	Punch Image	00-7F	128
	PFR Row Image	80-FF	128
2	MPX UCW Area	00-FF	256
3	Reader Translate Table	00-FF	256
4	Punch Check, PFR Read	00-9F	160
	Reader Card Image (Part 1)	A0-FF	96
5	Reader Card Image (Part 2)	00-1F	32
	Console Printer Translate Table	20-5F	64
	Reader Readout Area	60-FF	160
6	Punch Translate Table	00-FF	256
7	Printer Translate Table	00-FF	256

Figure 64. Auxiliary-Storage Byte Allocations for 16K Systems

Aux Stor Mod.	Usage	Rel. Byte Loc.	No. of Bytes
0	CPU Area	00-FF	256
1	Punch Image	00-7F	128
	PFR Row Image	80-FF	128
2	MPX UCW Area	00-FF	256
3	Reader Translate Table	00-FF	256
4	Punch Check, PFR Read	00-9F	160
	Reader Card Image (Part 1)	A0-FF	96
5	Reader Card Image (Part 2)	00-1F	32
	Console Printer Translate Table	20-5F	64
	Reader Readout Area	60-FF	160
6	Not Available	----	---
7	Not Available	----	---
8	Punch Translate Table	00-FF	256
9	Printer Translate Table	00-FF	256
10	Special Features	00-FF	256
11	Special Features	00-FF	256

Figure 65. Auxiliary-Storage Byte Allocations for 24K Systems

Aux Stor Mod.	Usage	Rel. Byte Loc.	No. of Bytes
0	CPU Area	00-FF	256
1	Punch Image	00-7F	128
	PFR Row Image	80-FF	128
2	MPX UCW Area	00-FF	256
3	Reader Translate Table	00-FF	256
4	Punch Check, PFR Read	00-9F	160
	Reader Card Image (Part 1)	A0-FF	96
5	Reader Card Image (Part 2)	00-1F	32
	Console Printer Translate Table	20-5F	64
	Reader Readout Area	60-FF	160
6	Punch Translate Table	00-FF	256
7	Printer Translate Table	00-FF	256
8	Special Features	00-FF	256
9	Special Features	00-FF	256
10	Special Features	00-FF	256
11	Special Features	00-FF	256

Figure 66. Auxiliary-Storage Byte Allocations for 32K Systems

Aux Stor Mod.	Usage	Rel. Byte Loc.	No. of Bytes
0	CPU Area	00-FF	256
1	Punch Image	00-7F	128
	PFR Row Image	80-FF	128
2	MPX UCW Area	00-FF	256
3	Reader Translate Table	00-FF	256
4	Punch Check, PFR Read Reader Card Image (Part 1)	00-9F A0-FF	160 96
5	Reader Card Image (Part 2)	00-1F	32
	Console Printer Translate Table	20-5F	64
	Reader Readout Area	60-FF	160
6	Punch Translate Table	00-FF	256
7	Printer Translate Table	00-FF	256
8	Special Features	00-FF	256
9	Special Features	00-FF	256
10	Special Features	00-FF	256
11	Special Features	00-FF	256
12	Special Features	00-FF	256
13	Special Features	00-FF	256
14	Special Features	00-FF	256
15	Special Features	00-FF	256

Figure 67. Auxiliary-Storage Byte Allocations for 48K Systems

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	General Purpose Register 0								Floating Point Register 0							
1x	General Purpose Register 1															
2x	General Purpose Register 2								Floating Point Register 2							
3x	General Purpose Register 3															
4x	General Purpose Register 4								Floating Point Register 4							
5x	General Purpose Register 5															
6x	General Purpose Register 6								Floating Point Register 6							
7x	General Purpose Register 7															
8x	General Purpose Register 8															
9x	General Purpose Register 9															
Ax	General Purpose Register 10															
Bx	General Purpose Register 11															
Cx	General Purpose Register 12															
Dx	General Purpose Register 13															
Ex	General Purpose Register 14															
Fx	General Purpose Register 15															

Note: Areas left blank are used for microprogram functions.

Figure 68. CPU Area, Auxiliary Storage Module 0

	x0	x2	x4	x6	x8	xA	xC	xE
0x	UCW 0,	Addr	000	or 080*	UCW 16,	Addr	010	
1x	UCW 1,	Addr	001	or 090*	UCW 17,	Addr	011	
2x	UCW 2,	Addr	002	or 0A0*	UCW 18,	Addr	012	
3x	UCW 3,	Addr	003	or 0B0*	UCW 19,	Addr	013	
4x	UCW 4,	Addr	004	or 0C0*	UCW 20,	Addr	014	
5x	UCW 5,	Addr	005	or 0D0*	UCW 21,	Addr	015	
6x	UCW 6,	Addr	006	or 0E0*	UCW 22,	Addr	016	
7x	UCW 7,	Addr	007	or 0F0*	UCW 23,	Addr	017	
8x	UCW 8,	Addr	008		UCW 24,	Addr	018	
9x	UCW 9,	Addr	009		UCW 25,	Addr	019	
Ax	UCW 10,	Addr	00A		UCW 26,	Addr	01A	
Bx	UCW 11,	Addr	00B		UCW 27,	Addr	01B	
Cx	UCW 12,	Addr	00C		UCW 28,	Addr	01C	
Dx	UCW 13,	Addr	00D		UCW 29,	Addr	01D	
Ex	UCW 14,	Addr	00E		UCW 30,	Addr	01E	
Fx	UCW 15,	Addr	00F		UCW 31,	Addr	01F	

Example: Unit control word 27 is located at position B8 in auxiliary-storage module 2. The unit address is 01B.

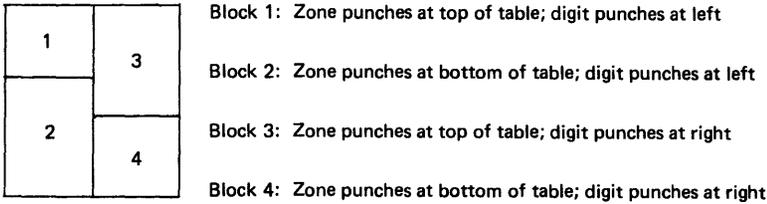
* These eight MPX UCWs may be used for single-address subchannels or shared subchannels. Refer to the Multiplexer Channel Device Addressing section for further information.

Figure 69. Multiplexer UCW Area, Auxiliary Storage Module 2

APPENDIX B: CODES

The 256-position table (Figure 70 , Part 2 of 2) outlined by the heavy black lines, shows the graphic characters and control character representations for EBCDIC. The bit-positions and card hole patterns for these and other possible EBCDIC characters are also shown.

The shaded areas (such as shown for position 1010 1111) designate recommended bit patterns to be used for the 32 graphics of the 120 character set that are in addition to the 88 graphics shown for the EBCD Interchange Code. (Use of a 120 character set requires the use of the Multiple Character Set special feature.)



Fifteen positions in the table are exceptions to the above arrangement. These positions are indicated by small numbers in the upper right corners of their boxes in the table. The card hole patterns for these positions are given at the bottom of the table. Bit-position numbers, bitpatterns, and hexadecimal representations for these positions are found in the usual manner.

Following are some examples of the use of the EBCDIC chart:

Character	Type	Bit Pattern	Hex	Hole Pattern	
				Zone Punches	Digit Punches
PF	Control Character	00 00 0100	04	12 - 9 - 4	
%	Special Graphic	01 10 1100	6C	0 - 8 - 4	
R	Upper Case	11 01 1001	D9	11 - 9	
a	Lower Case	10 00 0001	81	12 - 0 - 1	
	Control Character, function not yet assigned	00 11 0000	30	12 - 11 - 0 - 9 - 8 - 1	-

Bit Positions
01 23 4567

Figure 70. Extended Binary Coded Decimal Interchange Code (EBCDIC), Part 1 of 2

		00				01				10				11				Bit Positions 0,1	
		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11	Bit Positions 2,3	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	First Hexadecimal Digit	
		9	9	9	9	9	9	9	9									Zone Punches	
		12				12	12		12	12	12		12	12				Digit Punches	
			11				11	11	11		11	11	11		11				
				0		0		0	0	0		0	0			0			
Bit Positions 4, 5, 6, 7	Second Hexadecimal Digit																		
Digit Punches																			
0000	0 8-1	1 NUL	2 DS	3	4	5 SP	6 &	7	8					9	10	11	12 0	8-1	
0001	1 1		SOS					13		a	i			A	J	14	1	1	
0010	2 2		FS							b	k	s		B	K	S	2	2	
0011	3 3		TM							c	l	t		C	L	T	3	3	
0100	4 4	PF	RES	BYP	PN					d	m	u		D	M	U	4	4	
0101	5 5	HT	NL	LF	RS					e	n	v		E	N	V	5	5	
0110	6 6	LC	BS	EOB	UC					f	o	w		F	O	W	6	6	
0111	7 7	DEL	IL	PRE	EOT					g	p	x		G	P	X	7	7	
1000	8 8									h	q	y		H	Q	Y	8	8	
1001	9 8-1									i	r	z		I	R	Z	9	9	
1010	A 8-2		CC	SM		¢	!	15	:									8-2	
1011	B 8-3					.	\$,	#									8-3	
1100	C 8-4					16	*	%	@									8-4	
1101	D 8-5					()	_	'									8-5	
1110	E 8-6					+	;	>	=									8-6	
1111	F 8-7						¬	?	"									8-7	
		9	9	9	9									9	9	9	9		
		12				12				12	12		12	12	12	12	12		
			11				11				11	11	11		11	11	11		
				0				0		0		0	0	0		0	0		

Card Hole Patterns

- | | |
|-----------------|--------------|
| 1 12-0-9-8-1 | 5 No Punches |
| 2 12-11-9-8-1 | 6 12 |
| 3 11-0-9-8-1 | 7 11 |
| 4 12-11-0-9-8-1 | 8 12-11-0 |

Control Character Representations

- | | |
|-------------------|---------------------------|
| NUL Null | SOS Start of Significance |
| PF Punch Off | FS Field Separator |
| HT Horizontal Tab | BYP Bypass |
| LC Lower Case | LF Line Feed |
| DEL Delete | EOB End of Block |
| TM Tape Mark | PRE Prefix |
| RES Restore | SM Set Mode |
| NL New Line | PN Punch On |
| BS Backspace | RS Reader Stop |
| IL Idle | UC Upper Case |
| CC Cursor Control | EOT End of Transmission |
| DS Digit Select | SP Space |

Special Graphic Characters

- | | |
|---------------------|----------------------|
| 9 12-0 | 13 0-1 |
| 10 11-0 | 14 11-0-9-1 |
| 11 0-8-2 | 15 12-11 |
| 12 0 | |
| ¢ Cent Sign | - Minus Sign, Hyphen |
| . | / Slash |
| < Less-than Sign | , Comma |
| (Left Parenthesis | % Percent |
| + Plus Sign | _ Underscore |
| Logical OR | > Greater-than Sign |
| & Ampersand | ? Question Mark |
| ! Exclamation Point | : |
| \$ Dollar Sign | # Number Sign |
| * Asterisk | @ At Sign |
|) Right Parenthesis | ' Prime, Apostrophe |
| ; Semicolon | = Equal Sign |
| ¬ Logical NOT | " Quotation Mark |

16 On some chain configurations, the lozenge (■) is printed for this bit pattern, but this is nonstandard.

Figure 70. Extended Binary Coded Decimal Interchange Code (EBCDIC), Part 2 of 2

APPENDIX C: TIMINGS

SYSTEM/360 MODEL 25 INSTRUCTION TIMINGS

The instruction-time tables are provided for instruction execution when instructions are located in processor storage. All times are given in microseconds.

Refer to the Legend for definitions of symbols used in the timing charts.

Complete information for each instruction is included in the IBM System/360 Principles of Operation, Form A22-6821.

Timing Considerations

Unless otherwise noted, the following conditions were used in the development of the instruction timings (both groups):

1. The time required for indexing by a base register is included in the times given. For those instructions that may be double-indexed (indicated by an asterisk), an additional 6.3 microseconds must be added to the times given in the tables.
2. It is equally probable that:
 - a. Arithmetic operands will be either positive or negative.
 - b. Any bit will be either 0 or 1, and each bit location will be independent of other bit locations.
 - c. Decimal data can be 0-9 for each digit position.
 - d. Instructions will start on even or odd halfword boundaries.
3. Except for the Supervisor Call (SVC) instruction, interruption time is not included in these timings.

TIMING ASSUMPTIONS

Unless otherwise noted, the following assumptions were used in the development of the timing tables:

1. For Decimal Add (AP) and Decimal Subtract (SP) instructions, the first operand (i.e., the destination field) is assumed to be equal to or greater than the length of the second operand (i.e., the source field).
2. The instruction times for the floating-point instructions depend on the number of hexadecimal digits that are preshifted and postshifted, as well as the number of times recomplementation of the result occurs. The times given in the tables for floating-point instructions are a weighted average of these variables.

LEGEND FOR INSTRUCTION TIMINGS

- | | |
|----|---|
| E | Time for the subject instruction which is executed by the Execute instruction. |
| MK | Number of times the mark address is stored in the Edit and Mark instruction. |
| N | Total number of bytes in the first operand for those instructions with a single field length. |
| ND | Total number of digit-select and significant-start characters in the edit pattern. |
| N1 | Total number of bytes in the first operand. |
| N2 | Total number of bytes in the second operand. |
| N4 | Total number of field-separator characters in the edit pattern. |
| N5 | Total number of control characters in the edit pattern. |
| R | Number of registers loaded or stored. |
| SG | Number of signs in the field to be edited. |
| U1 | Select-out delay + device delay. |
| U2 | Device delay for Halt I/O instructions. |

Instruction	Format	Mnemonic	Timing (microseconds)
Add	RR	AR	35.1
Add*	RX	A	49.5
Add Decimal	SS	AP	67.5 + 10.8N
Add Halfword*	RX	AH	52.2
Add Logical	RR	ALR	31.5
Add Logical*	RX	AL	45.0
Add Normalized-Long	RR	ADR	233.1
Add Normalized-Long*	RX	AD	256.5
Add Normalized-Short	RR	AER	185.4
Add Normalized-Short*	RX	AE	207.0
Add Unnormalized-Long	RR	AWR	207.9
Add Unnorm-Long*	RX	AW	231.3
Add Unnorm-Short	RR	AUR	158.4
Add Unnorm-Short*	RX	AU	180.0
AND	RR	NR	28.8
AND*	RX	N	44.1
AND	SI	NI	26.1
AND	SS	NC	31.5 + 8.1N
Branch and Link	RR	BALR	32.4 if branch; 24.3 if no branch
Branch and Link*	RX	BAL	41.4
Branch on Condition	RR	BCR	20.7 if branch; 9.9 if no branch
Branch on Condition*	RX	BC	27.9 if branch; 22.5 if no branch
Branch on Count	RR	BCTR	30.6 if branch; 27.0 if no branch
Branch on Count*	RX	BCT	43.2 if branch; 35.1 if no branch
Branch on Index High	RS	BXH	71.1 if branch; 64.8 if no branch
Branch on Index Low or Equal	RS	BXLE	71.1 if branch 64.8 if no branch
Compare	RR	CR	29.7
Compare*	RX	C	45.0
Compare Decimal	SS	CP	67.5 + 10.8N
Compare Halfword*	RX	CH	48.6
Compare Logical	RR	CLR	27.9
Compare Logical*	RX	CL	43.2
Compare Logical	SI	CLI	24.3
Compare Logical	SS	CLC	31.5 + 8.1N
Compare (Long)	RR	CDR	228.6
Compare (Long)*	RX	CD	248.4
Compare (Short)	RR	CER	167.4
Compare (Short)*	RX	CE	187.2
Convert to Binary*	RX	CVB	Positive number: 837.0 + (4.5 for every bit present in decimal field) Negative number: 846.0 + (4.5 for every bit present in decimal field)
Convert to Decimal*	RX	CVD	Positive number: 48.6 + (8.1 times number of left zeros) + (18.0 times number of remaining bits) Negative number: 55.8 + (8.1 times number of left zeros) + (18.0 times number of remaining bits)
Divide	RR	DR	Positive number: 702.0; negative number: 720.0
Divide*	RX	D	Positive number: 716.4; negative number: 734.4
Divide Decimal	SS	DP	107 + (86N2 + 116)(N1-N2)
Divide (Long)	RR	DDR	1706.4
Divide (Long)*	RX	DD	1726.2
Divide (Short)	RR	DER	568.1
Divide (Short)*	RX	DE	567.9

Instruction	Format	Mnemonic	Timing (microseconds)
Edit	SS	ED	39.6 + 21.6ND + 14.4N4 + 8.1N5 + 49.5SG
Edit and Mark	SS	EDMK	39.1 + 21.6ND + 14.4N4 + 8.1N5 + 49.5SG + 10.8MK
Exclusive OR	RR	XR	28.8
Exclusive OR*	RX	X	44.1
Exclusive OR	SI	XI	27.0
Exclusive OR	SS	XC	31.5 + 8.1N
Execute*	RX	EX	36.9 + E
Halt I/O	SI	HIO	See I/O Tables.
Halve (Long)	RR	HDR	97.2
Halve (Short)	RR	HER	70.2
Insert Character*	RX	IC	27.0
Insert Storage Key	RR	ISK	23.4
Load	RR	LR	15.3
Load*	RX	L	32.4
Load Address*	RX	LA	26.1
Load and Test	RR	LTR	23.4
Load and Test (Long)	RR	LTDR	52.2
Load and Test (Short)	RR	LTER	45.9
Load Complement	RR	LCR	32.4
Load Complement-Long	RR	LCDR	54.9
Load Complement-Short	RR	LCER	48.6
Load Halfword*	RX	LH	33.3
Load (Long)	RR	LDR	38.7
Load (Long)*	RX	LD	59.4
Load Multiple	RS	LM	20.7 + 13.5R
Load Negative	RR	LNR	Positive number: 32.4; negative number: 24.3
Load Negative (Long)	RR	LNDR	54.0
Load Negative (Short)	RR	LNER	46.8
Load Positive	RR	LPR	Positive number: 24.3; negative number: 32.4
Load Positive (Short)	RR	LPER	47.7
Load PSW	SI	LPSW	57.6
Load (Short)	RR	LER	31.5
Load (Short)*	RX	LE	52.2
Load Positive (Long)	RR	LPDR	54.0
Move	SI	MVI	21.6
Move	SS	MVC	30.6 + 5.4N
Move Numeric	SS	MVN	30.6 + 8.1N
Move with Offset	SS	MVO	39.6 + 3.6N1 + 5.4N
Move Zones	SS	MVZ	30.6 + 8.1N
Multiply	RR	MR	178.2 + 90.0N1 (avg)
Multiply*	RX	M	192.6 + 90.0N1 (avg)
Multiply Decimal	SS	MP	107 + (44N2 + 20)(N1-N2)
Multiply Halfword*	RX	MH	198.0 + 90.0N1 (avg)
Multiply (Long)	RR	MDR	301.5 + 90.0N1 (avg)
Multiply (Long)*	RX	MD	321.3 + 90.0N1 (avg)
Multiply (Short)	RR	MER	253.8 + 90.0N1 (avg)
Multiply (Short)*	RX	ME	273.6 + 90.0N1 (avg)
OR	RR	OR	28.8
OR*	RX	O	44.1
OR	SI	OI	27.0
OR	SS	OC	31.5 + 8.1N
Pack	SS	PACK	33.3 + 3.6N1 + 4.05N2

Instruction	Format	Mnemonic	Timing (microseconds)
Read Direct	SI	RDD	27.0
Set Program Mask	RR	SPM	14.4
Set Storage Key	RR	SSK	23.4
Set System Mask	SI	SSM	25.2
Shift Left Double	RS	SLDA	See Shift Tables.
Shift Left Double - Logical	RS	SIDL	See Shift Tables.
Shift Left Single	RS	SLA	See Shift Tables.
Shift Left Single - Logical	RS	SLL	See Shift Tables.
Shift Right Double	RS	SRDA	See Shift Tables.
Shift Right Double - Logical	RS	SRDL	See Shift Tables.
Shift Right Single	RS	SRA	See Shift Tables.
Shift Right Single - Logical	RS	SRL	See Shift Tables.
Start I/O	SI	SIO	See I/O Tables.
Store*	RX	ST	31.5
Store Character*	RX	STC	27.0
Store Halfword*	RX	STH	28.8
Store (Long)*	RX	STD	53.1
Store Multiple	RS	STM	18.0 + 13.5R
Store (Short)*	RX	STE	44.1
Subtract	RR	SR	36.0
Subtract*	RX	S	50.4
Subtract Decimal	SS	SP	67.5 + 10.8N
Subtract Halfword*	RX	SH	53.1
Subtract Logical	RR	SLR	32.4
Subtract Logical*	RX	SL	45.9
Subtract Normalized (Long)	RR	SDR	233.1
Sub Norm (Long)*	RX	SD	256.5
Sub Norm (Short)	RR	SER	185.4
Sub Norm (Short)*	RX	SE	207.0
Subtract Unnormalized (Long)	RR	SWR	207.9
Sub Unnorm (Long)*	RX	SW	231.3
Sub Unnorm (Short)	RR	SUR	158.4
Sub Unnorm (Short)*	RX	SU	180.0
Supervisor Call	RR	SVC	54.9
Test and Set	SI	TS	25.2
Test Channel	SI	TCH	10.8
Test I/O	SI	TIO	See I/O Tables.
Test Under Mask	SI	TM	24.3
Translate	SS	TR	31.5 + 12.6N1
Translate and Test	SS	TRT	Condition code 0: 31.5 + 12.6N1 Condition code 1: 44.1 + 12.6(N1/2) Condition code 2: 54.0 + 12.6(N1-1)
Unpack	SS	UNPK	36.0 + 3.6N1 + 455N2
Write Direct	SI	WRD	23.4
Zero and Add	SS	ZAP	60.3 + 7.2N

SHIFT TABLES

No. of Places Shifted	SRL	SLL	SRA	SLA	SRDL	SLDL	SRDA	SLDA
0	53.1	53.1	62.1	63.0	63.0	63.9	77.4	75.6
1	84.6	64.8	93.6	74.7	112.5	79.2	126.9	90.9
2	76.5	73.8	85.5	83.7	92.7	91.8	107.1	103.5
3	70.2	85.5	79.2	95.4	90.9	107.1	105.3	118.8
4	63.0	91.8	72.0	101.7	80.1	117.0	94.5	128.7
5	94.5	103.5	103.5	113.4	129.6	132.3	144.0	144.0
6	86.4	112.5	95.4	122.4	109.8	144.9	124.2	156.6
7	80.1	124.2	89.1	134.1	108.0	160.2	122.4	171.9
8	62.1	65.7	71.1	75.6	76.5	81.0	90.9	92.7
9	93.6	77.4	102.6	87.3	126.0	96.3	140.4	108.0
10	84.6	86.4	94.5	96.3	106.2	108.9	120.6	120.6
11	79.2	98.1	88.2	108.0	104.4	124.2	118.8	135.9
12	72.0	104.4	81.0	114.3	93.6	134.1	108.0	145.8
13	103.5	116.1	112.5	126.0	143.1	149.4	157.5	161.1
14	95.4	125.1	104.4	135.0	123.3	162.0	137.7	173.7
15	89.1	136.8	98.1	146.7	121.5	177.3	135.9	189.0
16	68.4	75.6	77.4	85.5	87.3	95.4	101.7	107.1
17	99.9	87.3	108.9	97.2	136.8	110.7	151.2	127.4
18	91.8	96.3	100.8	106.2	117.0	123.3	131.4	135.0
19	85.5	108.0	94.5	117.9	115.2	138.6	129.6	150.3
20	78.3	114.3	87.3	124.2	104.4	148.5	118.8	160.2
21	109.8	126.0	118.8	135.9	153.9	163.8	168.3	175.5
22	101.7	135.0	110.7	144.9	134.1	176.4	148.5	188.1
23	95.4	146.7	104.4	156.6	132.3	191.7	146.7	203.4
24	77.4	88.2	86.4	98.1	100.8	112.5	115.2	124.2
25	108.9	99.9	117.9	109.8	150.3	127.8	164.7	139.5
26	100.8	108.9	109.8	118.8	130.5	140.4	144.9	152.1
27	94.5	120.6	103.5	130.5	128.7	155.7	143.1	167.4
28	87.3	126.9	96.3	136.8	117.9	165.6	132.3	177.3
29	118.8	138.6	127.8	148.5	167.4	180.9	181.8	192.6
30	110.7	147.6	119.7	157.5	147.6	193.5	162.0	205.2
31	104.4	159.3	113.4	169.2	145.8	208.8	160.2	220.5

(continued)

No. of Places Shifted	SRL	SLL	SRA	SLA	SRDL	SLDL	SRDA	SLDA
32					98.1	124.2	112.5	135.9
33					147.6	139.5	162.0	151.2
34					127.8	144.9	142.2	163.8
35					126.0	167.4	140.4	179.1
36					115.2	177.3	129.6	189.0
37					164.7	192.6	179.1	204.3
38					144.9	205.2	159.3	216.9
39					143.1	220.5	157.5	232.2
40					111.6	141.3	126.0	153.0
41					161.1	156.6	175.5	168.3
42					141.3	169.2	155.7	180.9
43					139.5	184.5	153.9	196.2
44					128.7	194.4	143.1	206.1
45					178.2	209.7	192.6	221.4
46					158.4	219.6	172.8	234.0
47					158.4	237.6	171.0	249.3
48					122.4	155.7	136.8	167.4
49					171.9	171.0	186.3	182.7
50					152.1	183.6	166.5	195.3
51					150.3	198.9	164.7	210.6
52					139.5	208.8	153.9	220.5
53					189.0	224.1	203.4	235.8
54					169.2	236.7	183.6	248.4
55					167.4	252.0	181.8	263.7
56					135.9	172.8	150.3	184.5
57					185.4	188.1	199.8	199.8
58					165.6	200.7	180.0	212.4
59					163.8	216.0	178.2	227.7
60					153.0	225.9	167.4	237.6
61					202.5	241.2	216.9	252.9
62					182.7	253.8	197.1	265.5
63					180.9	269.1	195.3	280.8

I/O TIMING TABLES

CHANNEL TIMINGS

Start I/O (Channel)

Condition Code		MPX Chnl	Sel Chnl
0	I/O operation initiated and channel proceeding with its execution	114.3 + U1	90.9 + 11
1	CSW stored; immediate operation initiated or Command rejected	105.6 + U1	104.4 + U1
2	Channel or subchannel busy	50.4	28.8
3	Device not operational	132.3 + U1	109.8 + U1
3	Channel or subchannel not operational	36.0	18.0

Test I/O (Channel)

Condition Code		MPX Chnl	Sel Chnl
0	Subchannel and device available	68.4 + U1	45.9 + U1
1	CSW stored device-end status only	64.8 + U1	57.6 + U1
1	CSW stored, channel-end interruption in subchnl	48.6	39.6
1	CSW stored, channel-end interruption in device	70.2 + U1	Not appl.
2	Channel or subchannel busy	43.2	19.8
3	Device not operational	85.5 + U1	63.0 + U1
3	Channel or subchannel not operational	30.6	12.6

Halt I/O (Channel)

Condition Code		MPX Chnl	Sel Chnl
0	Interruption pending in subchannel	50.4	29.7
1	CSW stored	51.3 + U1	41.4 + U1
2	Burst operation terminated	Not appl.	32.4 + U2
3	Device not operational	82.8 + U1	61.2 + U1
3	Channel not operational	30.6	12.6

I/O INSTRUCTION TIMES FOR CONSOLE
PRINTER-KEYBOARD

Start I/O (Console Printer-Keyboard)

Timings for the Console Printer-Keyboard do not include time required to handle data.

Condition Code		Time
0	Read	111.6
0	Write	108.0
1	Read or Write	65.7
2	Read or Write	38.7

Test I/O (Console Printer-Keyboard)

Condition Code		Time
0		42.3
1	Active yes, Secondary yes	77.4
1	Active no, Secondary yes	74.7
2	No command chain	37.8
2	Command chain	45.9

Halt I/O (Console Printer-Keyboard)

<u>Condition Code</u>	<u>Time</u>
0	46.8
1 Active yes, Secondary no	54.0
1 Active no, Secondary yes	58.5
3	45.0

I/O INSTRUCTION TIMES FOR INTEGRATED 1403

See channel-0 times for condition code setting of 3. In the following list, cc = condition code.

START I/O (1403 Printer)

- 1403 ready and not busy.
 - Write command (cc = 0)
162.0 + 16.2x + 10.8y microseconds
x = number of bytes in data field
(= count in CCW)
y = number of blanks, provided by 1403, at the end of the record.
x + y must equal 132.
 - Carriage control (cc = 1)
120.6 microseconds
 - Diagnostic PLB read (cc = 0)
147.6 + 14.4x microseconds
x = number of bytes sent to the CPU
(maximum of 132)
 - Diagnostic print-check read (cc = 0)
147.6 + 20.mx microseconds
x = number of bytes sent to the CPU
(maximum of 132)
 - Sense (cc = 0)
129.6 microseconds
 - No op (cc = 1)
116.1 microseconds
 - Gate load (cc = 1)
118.8 microseconds
 - Allow data check (cc = 1)
118.8 microseconds
 - Block data check (cc = 1)
118.8 microseconds
 - Load UCB and fold (cc = 1)
118.8 microseconds
 - Load UCB and no fold (cc = 1)
118.8 microseconds
- 1403 working, waiting for device-end (channel-end has already been accepted):
 - Device-end present (cc = 1)
67.5 microseconds
 - Device-end not present (cc = 1)
63.9 microseconds

- Channel-end not yet accepted
(cc = 2): 43.2 microseconds

TEST I/O (1403 Printer)

- 1403 not busy:
 - 1403 ready (cc = 0)
51.3 microseconds
 - 1403 not ready (cc = 1)
69.3 microseconds
- 1403 working, waiting for device-end (cc = 1):
 - Device-end present
67.5 microseconds
 - Device-end not present
63.0 microseconds
 - Channel-end not yet accepted, waiting for device-end (cc = 1):
72 microseconds

HALT I/O (1403 Printer)

51.3 microseconds

I/O INSTRUCTION TIMES FOR INTEGRATED 2540

The following times are for condition code 0. See the Channel Timings section for other condition codes. These timings do not include time required for the reader or punch traps.

Start I/O (2540 Reader)

Read and Feed, data mode 1, active 0, secondary 0: 3144.6 + (18.0 times number of columns) microseconds.

Test I/O (2540 Reader)

Active 0, Secondary 0: 51.3 microseconds.

Halt I/O (2540 Reader)

52.2 microseconds.

Start I/O (2540 Punch)

Write and Feed, Stacker Select, Data Mode
1: $574.2 + (36.9 \text{ times number of columns})$
microseconds.

Halt I/O (2540 Punch)

44.1 microseconds.

Test I/O (2540 Punch)

Active 0, secondary 0: 45.0 microseconds.

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