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IBM SYSTEM/360 OPERATING SYSTEM PL/I (F) COMPILER PROGRAM LOGIC MANUAL

This Technical Newsletter provides replacement pages for IBM System/360 Operating System, PL/I (F) Compiler, Program Logic Manual, Form Y28-6800-3. Pages to be inserted and removed are listed below.

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A change to the text or a small change to an illustration is indicated by a vertical line to the left of the change; a changed or added illustration is denoted by the symbol • to the left of the caption.

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The specifications contained in this Technical Newsletter correspond to Release 16 of IBM System/360 Operating System. Significant changes or additions will be reported in subsequent revisions or technical newsletters.

Summary of Amendments

This Technical Newsletter documents incremental improvements to the PL/I F Compiler for Release 16 of IBM System/360 Operating System. These improvements include: implementation of the UNALIGNED attribute and the STRING function; array and subscript optimization; and diagnostic message improvements.

Note: Please file this cover letter at the back of the manual to provide a record of changes.

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Module AD

Module AD performs inter-phase dumping.

All specified active storage is dumped at the end of the phases stated or implied in the DUMP option. If the DUMP option includes either I, for the Annotated Dictionary Dump, or E, for the Annotated Text Dump, or both, then phase. AD will load either phase AH, or phases AI and AJ, or all three, to produce the required output.

The DUMP Option

The DUMP option which is specified in the PARM field of the EXEC card indicates where dumping of main storage is to take place. It may be specified in one of the following ways:

- DUMP, means a dynamic dump is required (the dump routine will be called by a running phase)
- DUMP=(AREA, x₁, x₂, x₃,...,x_n) means a dump of the storage after the named phase.
 - AREA is any combination of TDPSCIE:
 - T text blocks
 - D dictionary blocks
 - P phases loaded
 - S scratch storage
 - C control phase
 - I annotated dictionary blocks
 - E annotated text blocks

The general syntax is:

DUMP [= ([AREA], $\{x | (y, z)\}, \dots$]

A single phase name indicates dumping of storage after this single phase. A pair of phase names indicates a continuous group of phases after which dumping of storage is to occur.

The dump will appear on SYSPRINT, inserted into the normal compiler output.

If AREA is omitted the default taken is DTSP. If a program check occurs and DUMP has been specified then AREA will be given the default DTSPC.

Use of the DUMP option may cause the compiler to use about 8K bytes more core than the SIZE option specifies. This is because SIZE specifies the amount of core the compiler can use for normal compilation and does not allow for the internal compiler diagnostic dumps. Example of an EXEC card using the DUMP option:

//STEP1 EXEC PROC=PL1LFC, PARM.PL1L='DUMP=(TE,QJ)'

This statement specifies compilation using the DUMP option to obtain a printout of the text blocks, the annotated text blocks, and of storage after the completion of compiler phase QJ.

Module AE

Module AE is the finalization of the READ-IN Phase control. (See Fig.4, Note¹)

Module AF

Module AF is a control section consisting of a table containing the compiler options which may be used during a compilation. The table is constructed at system generation time. The control section is brought into storage by the initialization Module AB at compilation time. A description of the use of Module AF is given in Appendix G.

Module AG

Module AG closes SYSUT3 for output, and re-opens it for input.

The closing and opening operations are performed in the following order:

CLOSE

alter macro-type in data control block (DCB)

OPEN(INPUT) switch routine ZURD to point at SYSUT3 DCB

Module AH

This module produces a dump of the dictionary. It prints out the communications region in the first block, and the offsets tables for each block if the extended dictionary option is in use. The remainder of each block is printed out entry by entry. The BCD is translated for those entries containing BCD. At the end of the dump, a list of all the dictionary codes used is given, with an explanation for each code.

The module is called by phase AD only if an I is specified in the AREA field of the DUMP option.

Modules AI and AJ

Modules AI and AJ are called, if E is specified in the area field of the dump option, to provide an 'easy-to-read' text print in which the triples and pseudo-code items comprising the text are printed separately. This option is available between phases IA and OE inclusive.

Module AN

This module contains the routines for dictionary and text-block handling for the normal-sized dictionary.

Module JZ

Module JZ builds the second half phase directory. A build list is constructed from the second half list neld in Module AA; a BLDL is performed on this list. The phase directory is then reconstructed in Module AA for the second half of the compiler.

48-CHARACTER SET PREPROCESSCR

Module AK

Module AK is the closing routine of the compiler. Its function is to release core used for dictionary, text blocks, scratch storage, and completed phases. If batch compilation is not specified, module AK closes all the files used by the compiler. If a batch compilation is specified, a check is made to determine whether any source programs are still to be compiled. Where there are none module AK closes all files. Where one or more programs remain to be compiled, the spill file only is closed, the batch delimiter card is scanned for syntax errors, and control is returned to module AA.

Module AL

This module contains the control routines for dictionary and text-block handling for the extended dictionary.

Module AM

Module AM marks phases as either wanted or not wanted, depending upon the compiler invocation options. Phases that are always loaded are marked wanted.

AM is the first compiler phase loaded after compiler initialization. It tests the relevant bits in CCCODE and marks the phases accordingly. Phase BX is the 48-character set preprocessor. It is loaded on programmer option and receives, as input, source text in the 48-character syntax.

The preprocessor scans the input text for occurrences of characters peculiar to the 48-character set, and converts these to the corresponding 60-character symbols. It then puts out the adjusted text onto backing storage ready for Phase CI, the first pass of the Read-In Phase.

The text is real in record by record. It is then scanned for alphatetic characters which may be the initial letters of operator keywords, for periods, and for commas. Items within comments or character strings are ignored.

When a possible initial letter is discovered, tests are made to determine whether or not one of the reserved operator keywords has been found. If one has been found, it is replaced by its 60-character set equivalent. Similarly, appearances of two periods are replaced by a colon, and a comma-period pair is replaced by a semicolon if the comma-period pair is not immediately followed by a numeric character.

Allowance is made for the possibility that a concatenation of characters which is meaningful in the 48-character set may be split between two records.

Before the text is processed a copy of the original input is preserved. The output from the preprocessor is the transformed text, record by record, followed by the original text. The Read-In Phase processes transformed text but prints out the



Note: There is an entry E for each parameter described in D. Figure 6. Dictionary Entries for an Internal Entry Point

Phase ED

Phase ED contains a set of subroutines, for processing certain of the tasking and list processing attributes, and tables of generic and non-generic built-in functions. The phase obtains 1K of scratch core, into which it moves the routines and tables, setting a slot in the communications region to point at them. This address is later picked up and used by phase EL.

Phase EG(EF)

Phase EG has two main functions. The first is to set up a hash table, and to insert the label entries left in the dictionary by the Read-In Phase into hash chains. The second function of the phase is to create dictionary entries for PROCE-DURE, BEGIN, and ENTRY statements, and to construct chains linking entries of particular types.

For <u>PROCEDURE-BEGIN</u> statements, entry type 1 dictionary entries are created (see Appendix C.2), and block header chains are set up to link these entries sequentially. A containing block chain is also set up to link each entry with that of its containing block.

On the appearance of <u>PROCEDURE</u> statements, circular PROCEDURE-ENTRY chains are initialized to link the entry type 1 dictionary entries of the PROCEDURE and ENTRY statements of the same block. The formal parameter list is scanned, and formal parameter type 1 entries are created and inserted into the hash chain. Details of the PROCEDURE-ENTRY chains appear in Appendix C.2.

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The attribute list is scanned and an options code byte is created in the entry type 1 (see Appendix C.2). A check is then made for invalid and inconsistent attributes. CHARACTER and BIT attributes are processed, and second file statements (see Appendix D.8) are created if necessary. Precision data are converted to binary, and dictionary entries are created for pictures (see Appendix C.7).

Statement labels are scanned and their entry type 2 dictionary entries are created. The relevant data bytes in the dictionary are completed by default rules (see Appendix C.3).

For <u>ENTRY</u> statements, entry type 1 dictionary entries are created (see Appendix C.2), and the circular PROCEDURE-ENTRY chain is extended. Formal parameters, attributes, and labels are processed in a similar manner to those for PROCEDURE statements, except that the options code byte is not created.

Phase EI (EH, EJ)

Phase EI scans the chain of DECLARE statements set up by the Read-In Phase, and modifies the statements to assist Phase EK as follows:

Structure Level Numbers: these are converted to binary.

Factored Attributes: parentheses enclosing factored attributes are replaced by special code bytes, so that Phase EK can distinguish them easily. A factored attribute table is set up. It consists of slots corresponding to each factored level. Each slot contains the address of the attribute list associated with that level, and the address of the slot for the containing level.

The following attributes are processed:

DIMENSION: dimension table entries (see Appendix C.8) are created in the dictionary and the source text is replaced by a pointer to the entry. Fixed bounds are converted to binary and inserted in the table. A second file statement (see Appendix D.8) is created at the end of the text, for adjustable bounds, and a pointer to the statement is inserted in the dimension table. Identifiers with identical array bounds share the same dimension table.

<u>PRECISION:</u> precision and scale constants are converted to binary.

<u>INITIAL</u>: dictionary entries are created for INITIAL attributes.

<u>INITIAL CALL:</u> second file statements are created for INITIAL CALL attributes.

CHARACTER and BIT: fixed length constants are converted to binary; a ccde byte marker is left for * lengths (see Appendix C.8). Second file statements (see Appendix D.8) are created for adjustable length constants, and the source text is replaced by pointers to the statements.

<u>DEFINED:</u> second file statements (see Appendix D.8) are created and the source text is replaced by pointers to the statements.

<u>POSITION:</u> the position constant is converted to binary.

<u>PICTURE:</u> a picture table entry (see Appendix C.7) is created and inserted into the picture chain; similar pictures share the same picture table. The source text is replaced by a pointer to each entry.

<u>USES and SETS:</u> USES and SETS attributes are moved into dictionary entries, and pointers to the entries replace the source text.

LIKE: BCD entries are created for identifiers with the LIKE attribute.

LABEL: if the LABEL attribute has a list of statement label constants attached, a single dictionary entry is created. The dictionary entry contains the dictionary references of the statement label constants in the list.

<u>OFFSET</u> and <u>BASED</u>: Second file statements are made and text references are inserted in the DECLARE statements for these attributes.

<u>AREA:</u> Fixed-length specifications are converted to binary; second file statements are made for expressions; a code byte, followed by the length of text reference, is inserted in the DECLARE statement text.

All other attributes, identifiers, or constants are skipped.

Phase EL (EK, EM)

Phase EL, consisting of modules EK, EL, and EM, scans the chain of DECLARE statements constructed by the Read-In Phase.

An area of storage known as the <u>attri-</u> <u>bute collection area</u> is reserved. This is used to store information about the identifiers, and has entries of a similar format to that for dictionary entries.

Complete dictionary entries are constructed for every identifier found in a IECLARE statement. These identifiers can he one of the following types:

- 1. Data Items (see Appendix C.4)
- Structures (in this case, the 'true' level number is calculated) (see Appendix C.4)
- 3. Label Variables (see Appendix C.4)
- 4. Files (see Appendix C.7)
- 5. Entry Points (see Appendix C.2)
- 6. Parameters (see Appendix C.7)
- 7. Event Variables
- 8. Task Variables.

Identifiers appearing as multiple declarations are rejected and a diagnostic message is given.

The attributes to be associated with each identifier are picked up in three ways.

First, the attributes immediately following the identifier are stored in the attribute collection area.

Secondly, any factored attributes and structure level numbers are examined. These are found by using the list of addresses placed in scratch core storage by Phase EI. Each applicable attribute is marked in the attribute collection area, and any other information, e.g. dimension table address, or picture table address, is moved into a standard location in the attribute collection area. All conflicting attributes are rejected and diagnostic messages are given.

Finally, any attributes which are required by the identifier, and which have not been declared, are obtained from the default rules.

After the dictionary, entry has been made, further processing (e.g. linking of chains, etc.) must be done in the follow-ing cases:

- 1. DEFINED data
- 2. Data with the LIKE attribute
- 3. Files
- 4. Strings with adjustable lengths
- 5. Arrays having adjustable bounds
- 6. GENERIC identifiers
- 7. Structure members
- 8. Identifiers with INITIAL CALL
- 9. Identifiers with the INITIAL attribute

After the declaration list has been fully scanned and processed, it is erased.

Phase EP

Phase EP first conditionally marks later phases as 'wanted' or 'not wanted,' according to how certain flags in the dictionary are set on or off. This assists in the load-ahead technique.

The entry type 1 chain in the dictionary is then scanned. For each FROCEDURE entry in the chain, each entry label is examined for a completed declaration of the type of data the entry point will return when invoked as a function. If this has previously been given in a DECLARE statement nothing further is done, ctherwise entry type 2 and 3 dictionary entries are constructed from default rules (see Appendix C.2). If this default data description does not agree with the description derived from the PROCEDURE or ENTRY statement, a warning message is generated.

At each PROCEDURE entry, the chain to the ENTRY statement entry type 1 is followed. Each statement is treated in a similar manner to that for a PROCEDURE entry type 1.

The CALL chain is then scanned and, at each point in the chain, the dictionary is searched for the identifier being called. If the correct one is not found, a dictionary entry for an EXTERNAL procedure is made (see Appendix C.2), using default rules for data description. Before making the entry, the identifier is checked for agreement with any of the built-in function names. If there is agreement a diagnostic message is generated, and a dummy dictionary reference is inserted.

If an identifier is found, it is examined to see if it is an undefined formal parameter. If it is, the formal parameter is made into an entry point, again using default rules for data description. If it is not, or if the declaration of the formal parameter is complete, the type of entry is checked for the legality of the call. A diagnostic message is generated if the item may not be called. In all cases, the item called is marked IRREDUCIBLE if it has not previously been declared REDUCIBLE.

Phase EW (EV)

Phase EW is an optional phase, loaded only if any LIKE attributes appear in the source program.

This phase scans the LIKE chain which has been constructed by Phase EK, and completes the dictionary entry for any structure containing a LIKE reference. When a structure in the LIKE chain is found, its validity is checked, and dimension data and inherited information are saved. The dictionary is scanned for the reference of the "likened" structure and the entry is checked for validity.

This dictionary entry (see Appendix C.4) is copied into the dictionary, with alterations if there is a difference between the original structure and this structure with regard to dimensioned data. If both structures have dimensions a straight copy is made; if the structure with the LIKE attribute has dimensions and the likened structure has not, the dimension information is added to the copy; if the structure with the LIKE attribute is not dimensioned and the likened structure is, then the dimension data is deleted from the copy. Inherited data is added to the copy. If an error is found, the structure with the LIKE attribute is deleted and a base element copy of the master structure is inserted instead. Where copies of entries occur which refer to dimension tables with variable dimensions, the dimension table entry is copied, and new second file dictionary entries and statements are created. Simi-lar entries must be made if the structure item has been declared to be an adjustable length string, or has been declared with the INITIAL attribute.

Finally, the newly completed structure is scanned by the ALIGN routine in phase EV, to provide correct explicit/inherited/ default alignment attributes for its base elements.

<u>Phase EY</u>

Phase EY is an optional phase which processes all ALLOCATE statements.

The second file is scanned first and all pointers to the dictionary are reversed. All ALLOCATE statements using the DECLARE chain are then scanned, and the dictionary references of allocated items are obtained by hashing the respective BCD of each item. The attributes given on the ALLOCATE statement for an item are collected together.

A copy of the dictionary entry of the allocated item is then made (see Appendix C.4), and the ALLOCATE statement is set to point to it. The dictionary entry is completed by including any attributes given on the ALLOCATE statement, and copying any second file statements from the DECLARE chain which are not overriden by the ALLO-CATE statement.

In the case of an ALLOCATE statement in which a based variable is declared, no copy of the original dictionary entry is required. The BCD is replaced by the original dictionary reference.

All pointer qualified references in the text are checked to determine that the qualified variable is based. For every occurrence of a variable with a different pointer a new dictionary entry is made. If the variable is a structure the entire structure is copied. A PEXP second file statement is made for the pointer and the 'defined' slot in the new dictionary entry is set to point to it instead of to the declared pointer.

The BCD of the pointer and the based variable in the text are replaced by the new dictionary reference followed by padding of blanks which will be removed by phase FA.

The based variable can be the qualified name of a structure member. If this is so, the name is checked for validity. Only the first part or lowest level of the qualified name in the text is replaced by the dictionary reference of the member. It is preceded by a special marker to tell phase FA that a partially replaced name follows.

<u>Phase FA</u>

Phase FA scans the text sequentially. If, during the scan, qualified names are found with subscripts attached, they are reordered so that a single subscript list appears after the base element name. The each dimension. It is then added to the AUTOMATIC chain for the appropriate block. Iterative DO loops are constructed, with the temporaries iterating between the upper and lower bounds of that particular dimension. Base elements are assigned, with the temporaries as subscripts, and with scalars remaining unchanged. END statements are created for the DO loops, and SELL statements for the temporaries. The statements which have been created are nested within the original statement.

Phase HK

The purpose of Phase HK is to detect array or scalar assignments, possible array expressions in I/O lists in GET and PUT statements, and nested statements, in particular nested assignment statements.

The leftmost array in an expression, or the leftmost array or scalar in an assignment is used as a basis for comparison, and if similar dimensions or bounds are not found in the array references, diagnostic messages are issued. Any expression containing only scalars is left unchanged.

For unsubscripted arrays which are equally spaced in core only one temporary is bought. For all other arrays a temporary is bought for each dimension, except in the case of certain partially subscripted arrays where the number may be minimized. Each temporary will be added to the AUTO-MATIC chain for the appropriate block. If the ON-condition name SUBSCRIPTRANGE is enabled for any statement, a temporary will be bought for each dimension in all cases. Iterative DO loops are constructed: for an unsubscripted array expression of dimensionality N, the temporary will iterate between the lower bound of the Nth dimension and an evaluated product so that all elements of the array are processed; while for other arrays the temporaries will iterate between the lower and upper bound of the particular dimension of the array. The assignment statement is added to the output string with additional subscripts where necessary. End statements are created for the DO loops, and SELL statements for the temporaries. The statements which have been created are nested within the original statement.

The syntax of pseudo-variables is also checked.

<u>Phase HP</u>

Phase HP scans the source text for references to items defined using iSUBs. For each reference found, the subscripts are computed for the base array corresponding to the subscripts given for the defined array.

The subscripts of the defined array are assigned to temporaries specially created for this purpose, which are then used to replace the iSUBs in the defining subscript list. The base array, with the subscript list so formed, replaces the defined array in the text.

THE TRANSLATOR LOGICAL PHASE

The Translator Phase consists of two physical phases, the stacker phase and the generic phase. The purpose of the Translator is to convert the output from the Pretranslator into a series of "triples" (see Appendix D.4). A "triple" is in the form of an operator followed normally by two operands.

The translation is achieved by using a double stack, with one part for operators, and the other part for operands, and assigning two weights to each operator. One weight (the stack weight) applies to the operator while it is in the stack, and the other weight (the compare weight) applies when the operator is obtained from the input string.

When an operator is obtained from the input string it is compared with the top stack operator. Depending on the result of the comparison, one or other of the two operators is switched on to determine what action is next to be performed. Apart from some special cases, this action is usually either to continue to fill the stack, or to generate a triple. The special cases lead to various manipulations of the stack items, after which the translation process continues.

For the purposes of translation, the input text to the translator is considered to consist of operators and operands only. This means that I/O options, etc., are regarded as operators.

After translation, the text string consists of operands and operators. All statements start with an operator to indicate a statement number or label, followed by the statement type, which may be a single operator, as in the case of RETURN or STOP, or which may be an operator such

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as a function or subscript marker, followed by a list of arguments. This list may also include compiler generated statements, e.g., DO loops for I/O lists. All I/O options are regarded as operators and require no markers before them. The end of the source text will be marked by a special operator, and compiler generated code, which may follow this end-of-program marker, will appear between the marker and the special second-end-of-program marker. The end of a block of text will be marked by an ECB operator. The program is now assumed to be syntactically correct.

Phase IA

Phase IA rearranges the source text into a prefix form, in which parentheses and statement delimiters have been removed, and the operations within a statement have been so arranged that those with the highest priority appear first.

As operators and operands are encountered, they are stored in stacks. Tables give the priority of each operator as it appears in the input text and in its stack.

When an operator is found during the scan of the source text, its compare weight (see Appendix D.4) is tested against the stack weight of the top operator in the stack. If the compare weight is the lesser of the two, then action is taken according to the compare operator. This is referred to as the compare action. Similarly, if the compare weight for the current operator found in the scan is greater than or equal to the stack weight of the top stack operator, action is taken according to the top stack operator. This is referred to as the stack action. Normally, the compare action is to place the compare operator in the stack, and to continue the scan, placing any subsequent operand in the stack until another operator is found. The normal stack action is to generate a triple, consisting of the top operator in the stack and the top two operands, eliminating the items from the stack, and inserting a special flag as the operand of the triple which is now at the top of the stack. The source (compare) item is then compared with the new top stack item.

The output text of the stacking phase is in the form of a series of triples, i.e. statement types with no operands, and operators with one or two operands. If the result of a triple operation is to be used in a later triple, the appropriate result is flagged accordingly. Certain phases are marked wanted or not wanted at this stage. If the source text contains an invocation by CALL or function reference, Phases IL and IM are marked wanted. If it does not, Phases IL, IM, IN, IO, IP, IQ, MG, MH, MI, MJ, MK, MM, MN, and MO are marked not wanted. Phases MB and MC are marked wanted when the source text contains pseudo-variables or multiple assignments; otherwise, they are marked not wanted. The DO loop processing phases (LG and LH) are marked in co-operation with the dynamic initialization phases (LB and LC). If LB and LC are requested, the marking of LG and LH is left until that stage of compilation; otherwise, LG and LH are marked by Phase IA independently.

When ALLOCATE and FREE statements occur, phase NG is marked wanted. When LOCATE statements occur, phase NJ is marked wanted.

<u>Phase IG</u>

Phase IG is an optional phase which is loaded to process array and structure arguments to built-in functions. When aggregate arguments are given for built-in functions they are expanded by the structure and array assignment phases so that the built-in functions appear as base elements, subscripted where necessary.

Phase GP examines these arguments, and ascertains whether it is necessary to create a dummy. If it is necessary, a scalar dummy is created, but the assignment of the argument expression is not inserted in the text, as this would be an invalid aggregate assignment.

Phase IG examines the text for a BUY statement for a dummy for an aggregate argument to a built-in function, and then inserts an assignment triple in the correct place in the text.

<u>Phase IL</u>

This phase immediately precedes the main generic phase. Its function is to obtain a block of scratch storage and place the entire built-in function table in that area. The starting address of this table is then placed in a register, and control is released to the main generic processor.

<u>Phase IM</u>

Phase IM scans the source text for procedure invocations by a CALL statement, procedure or library invocations by a function reference, and assignments to "chameleon" dummy arguments (see Phase GP).

Any procedure which is generic and is invoked by a CALL statement or function reference is replaced by the appropriate family member. If the invoked procedure is non-generic, it is ignored. A generic library routine invoked by a function reference is also replaced by the appropriate family member.

The arguments passed to library routines are checked for number and type, and a conversion inserted where necessary and possible.

The type and location of the result of all function invocations is placed in the text which follows the end of the text which invoked the function. The resulting type of an expression assigned to a "chameleon" dummy is determined and set in the dictionary entry which relates to the dummy.

Phase IT

Phase IT scans the source text for function triples and, in particular, the built-in functions for which code will be generated in-line. Further tests are made to detect the functions which, according to the method used to generate in-line code, are optimizable. This applies only to the SUBSTR, UNSPEC, and INDEX functions. All references to 'chameleon' temporary assignments within the scope of these functions are removed subject to certain restrictions imposed by the function nesting situation.

Phase IX

Phase IX checks that POINTER and AREA references are used as specified by the language. This phase is loaded only if POINTER or AREA references are found, declared either explicitly or contextually. Error messages are produced if errors are found and the statement in error is erased.

Data type triples in the text are scanned and a stack of temporary results is created containing the values: X'40' for POINTER X'02' for AREA X'00' for any other data type

The maximum permitted number of temporaries at any one point in a program is 200. The compilation is terminated if this figure is exceeded.

Phase JD

Phase JD scans the text for concatenation and unary prefixed triples with constant operands. These are evaluated and the results are placed in new dictionary entries. The references are passed through a stack into the corresponding result slots in the text.

THE AGGREGATES LOGICAL PHASE

The Aggregates Phase consists of three physical phases, the preprocessor (phase JI), the structure processor (phase JK) and the DEFINED chain check (phase JP).

The structure processor phase carries out the mapping of structures and arrays in order to align elements on their correct storage boundaries.

The DEFINED chain check ensures that items DEFINED on arrays and structures can be mapped consistently.

<u>Phase JI</u>

The first function of phase JI is to obtain scratch storage in which the text skeletons contained in phase JJ are to be held. Phase JJ is then loaded, and its contents are moved to the scratch storage for subsequent use by phases JI and JK. Phase JJ is then released and control is returned to phase JI.

The main function of phase JI is to expedite data interchange activities. A scan of static, automatic, and controlled chains is performed. The chains are reordered so that all data variables appear before non-data items. Adjustable PL/I structures and arrays are detected. Each entry in the COBOL chain is mapped as far as possible at compile-time, removed from the chain, and placed in the appropriate AUTOMATIC chain.

<u>Phase JK</u>

This phase scans the AUTOMATIC, STATIC, and CONTROLLED chains for arrays, structures (including COBOL structures), adjustable length strings, DEFINED items, AREA, and POINTER arrays and structures, TASK and EVENT arrays, and TASK and EVENT arrays in structures.

For the base elements of structures without adjustable bounds or string lengths, the following calculations are made:

The offset from the start of the major structure

The padding required to align the elements on the correct boundary

All multipliers of arrays of structures.

For all minor structures and major structures the following calculations are made:

Size

The offset from the preceding alignment boundary with the same value as the maximum appearing in the structure

Where a structure contains adjustable bounds or string lengths, code is generated to call the Library at object time.

For arrays, the multipliers are calculated, unless the array contains adjustable items, in which case the Library performs the calculations.

For adjustable structures, arrays, or strings, code is generated to add a symbolic accumulator register into the virtual origin slot of the dope vector, and the accumulator register is incremented by the size of the item.

Calculations are made in a similar fashion for arrays of strings (in structures or otherwise) with the VARYING attrihute. In addition, code is generated to set up an array of string dope vectors which refer to the individual strings in the array using the dope vector. Code is also generated to convert the original dope vector to refer to the array of string dope vectors, instead of to the storage for the array.

The routine which generates code for arrays of VARYING strings is also used to generate code for the initialization of arrays of TASK, EVENT, and AREA variables. DEFINED items are processed in the following way:

Code is generated to set the multipliers and virtual origin address of correspondence defined arrays without iSUBs in the dope vector of the DEFINED items from the defining base dope vector.

Code is generated for cverlay DEFINED items if they do not fall into the class which is to be addressed directly. The code first maps the DEFINED item, if necessary, calculates the address of the start of the storage to be used by the DEFINED item, and finally, relocates the DEFINED item using this address.

Dope vector descriptor dictionary entries and record dope vector dictionary entries are made for items which need to be mapped at object time, or which appear in RECORD-oriented input/output statements.

Phase JP

Phase JP scans the DEFINED chain, and differentiates between the fcllowing:

- 1. Correspondence defining
- 2. Scalar overlay defining
- 3. Undimensioned structure overlay defining
- 4. Mixed scalar-array-structure-string class overlay defining

In correspondence defining, this phase differentiates between arrays of scalars and arrays of structures. It also checks that the elements of the defined item may validly overlay the elements of the base belong to the same defining class, and that the base is contiguous.

In scalar overlay defining, this phase checks that the defined item may validly overlay the base.

For undimensioned structure overlay defining, this phase checks that the elements of the defined item may validly overlay the elements of the base.

For mixed scalar-array-structure-string class overlay defining, this phase checks that all elements of the defined item and all elements of the base belong to the same defining class (bit or character), and that the base is contiguous.

THE PSEUDO-CODE LOGICAL PHASE

The Pseudo-Code Phase accepts the output of the Translator Phase, and converts the triples into a series of machine-like instructions. The transformation into pseudo-code is achieved by a series of passes through the text; each pass removes variables, subscripts, functions, and argument markers.

Phase LR

The purpose of Phase LR is to save space during the expression evaluation phase, LS. It provides the initialization for Phase LS by obtaining 4,096 bytes of scratch storage and setting stack pointers. The scan phase, Phase LA, is initialized and Phase MP is marked.

The translate table for scanning triples, and the constants for expression evaluation are included in this phase and are moved to the first 1K area of scratch storage. Subroutines required by phase LS are also moved into scratch core at this time. Finally, control is passed to Phase LS.

Phase LS

Phase LS scans the source text to convert expression triples to pseudo-code. If a triple produces a result, it is added to the temporary work stack.

For the arithmetic triples +,-,*,/,**, prefix +, and prefix -, the operands are combined to give the base, scale, mode, and precision of the result. If conversion is necessary, an assignment triple, with the target and source types as operands, is inserted in the text. In-line pseudo-code is generated for all operators except ** and some complex type * and / operators. In these cases, Library calling sequences are generated. An intermediate result is always produced and the triple is removed from the text.

The operands of comparison triples GT, GE, equals, NE, LE, and LT are combined and converted as for the arithmetic triples. In-line pseudo-code is generated and the triple is removed from the text, unless both operands are string type, in which case a temporary is created. If the next triple is a conditional branch, a mask for branch-on-false is inserted. Otherwise, the result is a length 1 bit string.

For the string triples CAT, AND, OR, NOT, and string comparisons, if an operand is zero, TMPD triples, containing the intermediate result from the top of the stack, are inserted in the text after the triple. The result is a CHARACTER or BIT string or a COMPARE operator. When subscript triples appear, a symbolic register number is inserted in the triple. The result contains the dictionary reference of the array and the symbolic register.

For function triples, a description of the workspace for the function result is inserted in the TMPD triples which follow the function triples. The function result is added to the intermediate stack.

For add, multiply, and divide functions, the function and argument triples are removed from the text. Arithmetic type in-line pseudo-code is generated, with modifications for the precision and scale factor, and the result is added to the intermediate stack.

With pseudo-variable triples, a special marker is added to the intermediate result stack.

Other triples which may use an intermediate result, are examined. If an operand is zero, two or three TMPD triples, containing the intermediate result from the top of the stack, are inserted in the text after the triple. If both operands are zero, the TMPDs for the second operand precede those for the first operand.

Phase LV

Phase LV provides string handling facilities for the pseudo-code phases.

It converts any type of data item to a CHARACTER or BIT string, and an assignment triple, with the target and source types used as the operands is inserted in the text.

A string dope vector description is produced from a standard string description.

Phase LX (LW, LY)

Phase LX consists of three modules, LW, LX, and LY. Module LW acts as a preprocessor for LX and LY, moving constants into scratch core prior to loading the string-handling modules.

Phase LX scans the source text to convert string triples to pseudo-code. If a result is produced it is added to a stack of intermediate string results. For the comparison triples GT, GE, equals, NE, LE, AND LT, both operands are already string type. If one operand is zero, the operand is obtained from the associated TMPD triples. In-line pseudocode is generated if the operands are aligned and are of known lengths less than or equal to 255 bytes; otherwise, Library calling sequences are generated. The triple and any TMPD triples are removed from the text.

In the case of the string triples CAT, AND, OR, and NOT, the operands are converted to string type by phase LV. Zero operands are obtained from associated TMPD triples. In-line pseudo-code is generated when operands are aligned and are of known lengths less than or equal to 255 bytes. For the CAT operator, the first operand must be a multiple of 8 bits unless the strings involved are less than or equal to 32 bits in length. In-line code is also generated for the following cases involving non-adjustable varying strings:

- Character string concatenation of varying strings with lengths less than 256 bytes.
- 2. Bit string operations for AND, OR, NOT, concatenation, and comparison where the strings are aligned and are less than 33 bits in length.

Otherwise, Library calling sequences are generated. The triple and any TMPD triples are removed from the text, and the string result is added to the intermediate result stack.

For TMPD triples, if the intermediate result described by the TMPD triples is a string, a complete string description is moved from the top of the intermediate stack to the TMPD triples. If the TMPD triples do not describe a string, they are ignored.

In-line code is generated for the BOOL functions AND, OR, and EXCLUSIVE OR, when the third argument is a character or bit string constant and the first and second arguments are aligned and of known lengths less than or equal to 255 bytes. Otherwise Library calling sequences are generated. Subscript and function triples may produce intermediate string results.

<u>Phase MB</u>

Phase MB scans the text for pseudovariable markers and multiple assignment markers. A stack of pseudo-variable descriptions is maintained, together with the left hand side descriptions of multiple assignments when they occur. Pseudo-code and triples are generated for pseudovariables and the left hand side descriptions of multiple assignments are put out in the correct sequence.

Phase MD

Phase MD uses the SCAN routine LA to scan the text for ADDR and STRING built-in functions for which it generates in-line code. It appears before the normal function processor phase and removes all trace of the in-line function. The general SCAN routine passes control when these functions are found.

For all cases of ADDR the generated code establishes the start address of the argument. If structure name arguments are present the structure chain is hashed for the first base-element. For array names the address of the first element is calculated.

If the argument to the SIRING function is contiguous in core, and its length is known at compile-time, an adjustable string assignment is generated. Otherwise the library routines IHESTGA and IHESTGB are called to produce the concatenated length and to concatenate the elements of the array or structure argument.

Phase ME

Phase ME identifies all invocations of the SUBSTR function and pseudo-variable, all UNSPEC, STATUS, and CCMPLETION functions, and those invocations of the INDEX function which can be implemented in-line; and generates pseudo-code tc perform these functions at object time. The scan of the text is conducted by the general SCAN routine, and all trace of the invocations of these functions is removed before the normal function processor phase is loaded. When the end-of-program marker is encountered the terminating routine is entered.

Phase MG

Phase MG identifies functions which are to be coded in-line, and generates, in their place, the pseudo-code to perform the relevant function. This phase appears before the normal function processor phase and removes all trace of the in-line function.

The scan of the text is conducted by the general SCAN routine, and control is handed to the present phase when one of the following functions is found:

ALLOCATION	FLOOR	BINARY
BIT	IMAG	DECIMAL
CEIL	REAL	FIXED
CHAR	TRUNC	FLOAT
COMPLEX		PRECISION
CONJG		

Control is also passed to this phase if ABS is found with real arguments. The arguments are collected, and the appropriate routine is entered to generate the pseudo-code. When the end-of-program marker is encountered the terminating routines are entered.

Phase MI

1

Phase MI identifies functions which are to be coded in-line, and generates , in their place, pseudo-code to perform the relevant function. This phase appears before the normal function processor phase and removes all trace of the in-line function.

The scan of the text is conducted by the general SCAN routine and control is handed to the present phase when one of the following functions is found:

MAX MOD MIN ROUND

If the number of arguments to the MAX or MIN functions is greater than three, a Library call is generated.

Phase MK

Phase MK identifies functions which are to be coded in-line, and generates, in their place, pseudo-code to perform the relevant function. This phase appears before the normal function processor phase and removes all trace of the in-line function.

The scan of the text is conducted by the general SCAN routine, and control is passed to the present phase when one of the following functions is found:

DIM	HBOUND
LBOUND	SIGN
LENGTH	FREE

<u>Phase ML</u>

Phase ML scans the source text for generic entry name arguments to procedure invocations.

Such entry names may be floating arithmetic built-in functions cr programmersupplied procedures with the GENERIC attribute. When one is found, the correct generic family member to be passed is selected by this phase, depending on the entry description of the invoked procedure.

<u>Phase MM</u>

Phase MM scans through the source text for procedure invocations by a CAIL statement, or for procedure or Library routine invocations by a function reference.

Procedure invocations are replaced by an external standard calling sequence, and Library routine invocations are replaced by an external or internal standard calling sequence as appropriate (see Appendix D.10).

If a CALL is accompanied by a TASK, EVENT, or PRIORITY option, library module IHETSA is loaded rather than IHESA, and the parameter list is modified to include the addresses of the TASK and EVENT variables and the relative PRIORITY.

Phase MP

Phase MP reorders the BUY and SELL statements involved in obtaining Variable Data Areas (VDAs) for adjustable length strings or temporaries, which were created by Phase GK. On entering this phase, the BUY triples precede the code compiled to evaluate the length of storage required for the VDA. This evaluation code is included between further BUYS and BUY triples, which themselves are between the BUY triple being considered and its associated SELL triple. Phase MP extracts these sections of code and places them before the EUY triple of the adjustable string temporary. Since such BUY triples may be nested, the phase maintains a count to record the nesting status.

Phase MS

Phase MS scans the source text for references to subscripted array elements.

If references are found, pseudo-code is generated to calculate the offset of the subscripted element in relation to the origin of the array. If necessary, further pseudo-code is generated to check the subscript range.

Optimization of constant subscript evaluation is carried out on arrays having one subscript which is an integer constant, and all following subscripts declared to have fixed upper and lower bounds. This applies to arrays with fixed-length elements.

Phase NA

Phase NA generates pseudo-code for the following triples:

For <u>PROCEDURE'</u> and <u>BEGIN'</u> triples a Library call is generated to the FREEDSA routine.

For <u>RETURN</u> triples a Library call is generated, unless a value is to be returned as the result of a function invocation, in which case code is first generated to assign the result to the target field, and then the Library call is made. If the function may return the result as more than one data type, a switch would have been set at the entry point to the function, and the RETURN statement would test the switch value, so that the data type appropriate to the entry point is returned.

<u>GOTO</u> triples either will be invalid branches detected by Phase FI, in which case they will be deleted, or they will be branches to statement label constants in the same PROCEDURE or BEGIN block. In this case, they will be compiled as oneinstruction branches.

<u>GOLN</u> triples are compiled into oneinstruction branches to the compiler label number in operand 2 of the triple.

A <u>GOOB</u> (Go Out Of Block) triple is a branch to a label variable, possibly subscripted, or to a label in a higher block than the current one (a branch to a lower block is invalid). A call is generated to a Library epilogue routine, pointing at a double-word slot containing the address of the label and the Pseudo-Register Vector (PRV) offset (for a label constant), or the invocation count (for a label variable). STOP and EXIT statements are implemented simply by invocation of the appropriate Library routine.

For <u>IF</u> triples, if the second operand is an identifier, or the result of an expression which is not a comparison, code is generated to convert it to a BIT string, if necessary. This BIT string is compared to zero, either in-line, or by a call to the Library.

The second operand may be a mask which will have been inserted by the expression evaluation phase as a result of the comparison specified in the IF statement. This mask is put into a generated instruction to branch if the condition is not satisfied, i.e. either to the ELSE clause or to the next statement.

For ON triples, code is generated to set flag bits and update the ON-unit address in the double-word ON slot in the DSA.

For <u>SIGNAL</u> arithmetic condition triples, in-line code is generated to simulate the condition. For all other conditions, a Library error routine is called.

<u>REVERT</u> triples generate code to set flag bits in the double-word ON slot in the DSA.

<u>Phase NG</u>

Phase NG generates the calling sequences to the Library for DELAY and DISPLAY and WAIT statements.

It generates code to call the library routines which handle ALLOCATE and FREE statements whose arguments are BASED variables.

For DELAY statements, the argument has to be a fixed binary integer, and, if necessary, code is generated for conversion.

For DISPLAY statements, the message must be a CHARACTER string, or, if necessary, converted to one. A parameter list is built up to pass to the Library.

For WAIT statements, the parameter list is built up in WORKSPACE. It consists of the address of the scalar expression (converted to a fixed binary integer), followed by the addresses of the eventnames that appear in each WAIT statement. If the scalar expression option does not appear, the address of the total number of event-names is used. When all data element descriptors and symbol tables in the compilation have been processed, all STATIC storage has been allocated and the total size of the STATIC control section is placed in a slot in the communications region.

Phase PP

Phase PP extracts all ON condition entries and places them at the head of the AUTOMATIC chain. It then extracts all temporary variable dictionary entries from the AUTOMATIC chain and places them in the zone following the ON conditions in the chain.

All dictionary entries which are totally independent of any other variable are extracted, and also placed in the zone following the ON conditions.

The phase then extracts all dictionary entries which depend upon some other variable in containing blocks or in the zones already extracted, and places them in the next following zone. Dependency includes expressions for string lengths, expressions for array bounds, expressions for INITIAL iteration factors, and defined dependencies. This is repeated recursively until the end of the chain. If some variable depends upon itself, a warning message is issued.

A special zone delimiter dictionary entry is inserted between each zone in the AUTOMATIC chain (see Appendix C.7). A code byte is initialized in the delimiter to indicate to Phases PT and QF whether its following zone contains any variables which require storage (i.e., it does not consist entirely of DEFINED items, which do not require storage), and whether or not the following zone contains any arrays of VARY-ING strings.

<u>Phase PT</u>

Phase PT allocates AUTOMATIC storage, scans the CONTROLLED chain, and determines the size of the largest dope vector. It scans the entry type 1 chain, and for each PROCEDURE block or BEGIN block it allocates storage for a DSA and compiles code to initialize the DSA.

A two-word slot in the DSA is allocated for each ON condition in the block, and code is compiled to initialize the slot. Space for the addressing vector and workspace in the DSA is also allocated. Two words are allowed for tasking information in the DSA if the TASK option is on the external PROCEDURE of the compilation.

The AUTOMATIC chain is scanned and dope vectors are allocated for the items requiring them. Code is compiled to copy the skeleton dope vector, and to relocate the address in the dope vector.

Where there is a block with its DSA in STATIC, dope vector initialization is not performed for the variables in the first region of the AUTOMATIC chain. Address slots in dope vectors for variables in the remainder of the chain are relocated.

Storage is allocated for addressing temporaries type 2 and for addressing controlled variables, and for the parameters chained to the entry type 1

The first region of the AUTOMATIC chain is scanned and storage allocated for double precision variables, single precision variables, CHARACTER strings and BIT strings, in that order.

The first region of the AUTOMATIC chain is scanned and storage allocated for arrays, relocating the virtual origin. For arrays of strings with the VARYING attribute, the secondary dope vector is also allocated and code is compiled to initialize the secondary dope vector. Correctly aligned storage is allocated for structures. If a structure contains any arrays of strings with the VARYING attribute, the storage for the secondary dope vector is allocated at the end of the structure.

A pointer is set up in the AUTOMATIC chain delimiter to the second file statement which has been created.

The remaining regions of the AUTOMATIC chain are scanned and code is compiled to obtain a Variable Data Area (VDA) for each region. Code is compiled to copy the skeletons into the dope vectors and to relocate the addresses in the dope vectors. During this pass, any DEFINED items which are to be addressed directly have the storage offset and the storage class copied from the data item specified as the base identifier.

<u>Phase QF</u>

Phase QF, which constructs prologues, scans that text which is in pseudo-code form at this time with end-of-text block markers inserted. When a statement label pseudo-code item is found, it is analyzed and one of three things happens:

- 1. The item is saved if it relates to a PROCEDURE statement
- 2. The item is omitted if it relates to a BEGIN or ON block
- 3. The item is passed if it relates to neither of the first two conditions

When a BEGIN statement is found, a standard prologue of simple form is generated, and code is inserted from second file statements (if there are any) to get the DSA, either dynamically, or in the case of eligible bottom-level blocks, by using the supplementary LWS made available at initialization time. Code is also inserted to initialize the DSA and to allocate and initialize any VDAS.

When a PROCEDURE statement is found, it is first determined whether it heads an ON block or a PROCEDURE block. If it is an ON block, a standard prologue (similar to that for a BEGIN block) is generated. If it is a PROCEDURE block, a specialized prologue is generated. This takes account of the manner of getting the DSA, the number of entry points, the number of entry labels on a given entry point, the number of parameters on each entry point, and whether the PROCEDURE is a function.

Prologue code is generated for AUTOMATIC scalar TASK, EVENT or AREA variables, in order to perform the initialization required when these variables are allocated.

The code generated by the prologue construction phase is partly in pseudo-code and partly in machine code. The machine code (which is delimited by special pseudocode items) has the same form as the code produced by the Register Allocation Phase (see Appendix D.7).

DSA optimization is performed under certain conditions (see Appendix H).

At the end of the prologue, the statement label item saved earlier is inserted to mark the apparent entry point. Code is produced to effect linkage to BEGIN blocks in such a way that general register 15 contains the address of the entry point, and general register 14 contains the address of the byte beyond the BEGIN epilogue.

At the end of the text, any text blocks that are not needed are freed, and control is passed to the next phase. <u>Phase QJ</u>

Phase QJ scans the text for ALLOCATE, FREE, and BUY statements.

On finding an ALLOCATE statement, a routine is called which does a 'look ahead' for initialization statements associated with the allocated variable, e.g., adjustable array bounds or adjustable string lengths, and places the text references of each statement in the dictionary entry associated with each statement.

If the allocated item has a dope vector, code is generated to move the skeleton dope vector generated by Phase PH into a block of workspace in the DSA of the current block.

Any adjustable bound expressions or string length expressions are then extracted from the text references, and the expressions are placed in-line in the text.

Any information required from previous allocations (specified by * in the ALLOCATE statement) is extracted from the previous allocation, and copied into the workspace.

Code generated by Phase JK to initialize multipliers, etc., is extracted and placed in-line, after first loading the variable storage accumulator with the dope vector size. Phase JK generates code to increment the accumulator register by the size of the item.

If the item has no adjustable parameters, code is generated to increment the accumulator by the size calculated at compilation time. If this size is greater than 4,096, Phase JK generates a constant dictionary entry, which is used in this code.

If the item has any arrays of varying strings, the size of the array string dope vector is added to a second accumulator register. Code is generated to add the two accumulators into the second one, which is a parameter to a Library routine. A routine is then called which extracts the Library call inserted by pseudo-code and places it in-line in the text.

Code is inserted after the Library call to initialize the dope vector in workspace to point to the allocated storage. Code is generated to transfer the dope vector from the workspace to the allocated storage.

The code generated by phase JK to initialize arrays of varying strings, tasks, events, and areas is then inserted in the output stream.

Phase RA

Phase RA scans the text for dictionary references, the beginnings and ends of PROCEDURE and BEGIN blocks, and the starting points of the original PL/I statements.

A dictionary reference, when found, is decoded into a word-aligned dictionary address and a code. These are used to determine what is being referenced. The corresponding object time address as an offset and base is then calculated.

If the address required has an offset less than 4,096 and a base which is either an AUTOMATIC or STATIC data pointer, no extra instructions are generated. If this is not so, extra instructions are inserted in the text stream to calculate the required address. The calculation of this address is broken down into logical steps in a 'step table.' On completion, the table is scanned backwards to determine whether an intermediate result has been previously calculated. The steps which have not been previously calculated are then assembled into the pseudo-code. The compiled code is added either to the output stream or to a separate file. The code in the separate file is terminated by a store instruction to save the calculated address. The extra "insertion file" is placed in the prologue of the relevant block by the next phase. Instructions are stored in-line if the referenced item is CONTROLLED, if it is a parameter, if fewer instructions are required to recalculate the base rather than load the stored address, or if the reference itself is in the prologue.

If no addressing code is generated, a special item is put in text to tell phase RF what base to use.

All relevant information for PROCEDURE and BEGIN blocks is stacked and unstacked at the start and end of the blocks respectively.

At the start of PL/I statements, code is compiled to keep the required PREFIX ON slots in the Dynamic Storage Area updated. On meeting the pseudo-code error marker, the calling sequence to the Library error package is generated, and the error marker removed. If the STMT option has been specified, code is generated at the start of each PL/I statement to keep the statement number slot in the current DSA up to date.

Phase RF

Phase RF scans the text for register occurrences, implicit and explicit, and the start and end of PROCEDURE and BEGIN blocks. At the beginning of PROCEDURE and BEGIN blocks all relevant information is stacked, and is later unstacked at the corresponding end.

Registers are classified as assigned, symbolic, or base.

Assigned registers require the explicitly menticned register to be used. If that register is not free it is stored. Symbolic registers may occupy any register in the range 1 through 8. An even-odd pair may be requested. Base registers may occupy any of registers 1 through 8.

When a register is requested, a table of the contents of registers is scanned, to determine whether the register already has the required value. If it does, that is used. If it does not, and it is not an assigned register, a search is made for a free register and this is allocated if one is found. Should no register be free, a look-ahead is performed to determine which register it is most profitable to free.

If a register contains a base it need not be stored on freeing. If a register contains a symbolic or assigned register, it may require to be stored when freed, depending upon whether it has had its value altered since any storage associated with it was last referenced.

At a BALR (Branch and Link) instruction it is insured that all the necessary parameter registers are in physical registers, and not in storage.

No flow trace is carried out by the compiler. Therefore, the register status is made zero at branch-in and branch-out points. An exception is at a conditional branch. Here the registers are not freed after having been saved.

Any coded addressing instructions are expanded when found in-line. At a specific "insertion point" in a prologue, any addressing instructions in the "insertion file" are brought in and expanded.

THE FINAL ASSEMBLY LOGICAL FHASE

The Final Assembly Phase converts the pseudo-code output of the register allocation phase into machine code, the principal functions being the substitution of machine operation codes for pseudo-code operations, and the replacement of PL/I and compiler inserted symbolic labels by offset values.

Loader text is generated for program instructions, DECLARE control blocks, and OPEN file control blocks, initial values defined in the source program, parameter lists, skeleton dope vectors, symbol tables, etc. ESD and RLD cards are generated for external names and pseudoregisters. An object listing of the code generated by the compiler is produced if the option has been specified by the source programmer.

<u>Phase TF</u>

Phase TF scans the text, assigns offsets to compiler and statement labels, and determines the code required for instructions which reference labels.

The size of each procedure is determined and stored in the PROCEDURE entry type 1. A location counter of machine instructions is also maintained.

<u>Phase TJ</u>

Phase TJ scans the text until no further optimization can be achieved in the final assembly.

A location counter is maintained for assembled code, and offsets are assigned to labels.

The size of each procedure is determined and stored in the PROCEDURE entry type 1. The amount of code required for instructions to reference labels is also determined, while attempting to reduce this from the amount estimated by the first assembly pass.

This phase also attempts to reduce the number of Move (MVC) instructions by searching for consecutive MVC instructions which refer to contiguous locations.







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Table ED. Phase ED, Initialization

Statement or Operation Type	Main Processing Routine	Subroutines Used
Sets up routines in scratch core for phase EL	SETUP	None

• Table ED1. Phase ED Routine/Subroutine Directory

Routine/Subroutine	Function
EVENT TASK CELL BASED POINTER OFFSET	Routines for processing declared attributes. These set up information in the attribute collection area of scratch core, for reference by CDICEN, etc., in phase EL.

Table EG. Phase EG Dictionary Initialization

Statement or Operation Type	Main Processing Routine	Subroutines Üsed
Hashes labels	CAA1	CHASH, CBCDL2
PROCEDURE-BEGIN chain	CA7	None
BEGIN	CA8 A	None
PROCEDURE	CAPROC	CANATP, CFORP
ENTRY	CA10	CANATP, CFORP
Formal parameters	CFORP	CHASH, CBCDL2
Attribute list	CANATP	CAPRE1, CATCHA, CATBIT, CATPIC
Creates entry type 2 entries for labels	CTYPBL	ENT2F, CDEFAT

•	Table	EG1.	Phase	EG	Routine/Subroutine	Directory
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Routine/Subroutine	Function	
CAA1	Scans label table and hashes labels.	
CANATP	Processes attribute list.	
CAPROC	Processes PROCEDURE statements.	
CAPRE1	Processes precision data.	
CATBIT	Processes BIT attribute.	
CATCHA	Processes CHARACTER attribute.	
CATPIC	Processes PICTURE attribute.	
CA6	Scans the PROCEDURE-BEGIN chain for the relevant statements.	
CA8A	Processes BEGIN statements.	
CA10	Processes ENTRY statements.	
CBCDL2	Traverses the hash chain looking for entries with the same BCD as that just found.	
CDEFAT	Completes data byte for entry type 2 entries by default rules.	
CFORP	Processes formal parameter lists.	
CHASH	Obtains an address in the hash table for an identifier.	
CTYPBL	Creates entry type 2 entries for labels.	
ENT 2F	Creates or copies second file statements.	
ТҮРЖ	Scans ENTRY chain.	
OPTN1 (EF)	Checks containing block options, for inheritance.	
CPTN2 (EF)	Processes procedure options.	
OPTN3 (EF)	Performs post processing, makes STATIC DSA decisions.	
ATTRBT (EF)	Processes POINTER, OFFSET, and AREA attributes.	

	Routine/Subroutine	Function
	ATLSCN	Scans the list of attributes following the identifier.
	BCDISB	Checks for multiple declarations, etc.
	BCDPR	Processes BCD of identifier.
	CDATPR (EK)	Attribute controlling routine.
	CDAT40 (EK)	Processes DECIMAL attribute.
	CDAT41 (EK)	Processes BINARY attribute.
	CDAT42 (EK)	Processes FLOAT attribute.
	CDAT43 (EK)	Processes FIXED attribute.
	CDAT44 (EK)	Processes REAL attribute.
	CDAT45 (EK)	Processes COMPLEX attribute.
	CDAT46 (EK)	Processes precision attributes.
	CDAT48 (EK)	Processes VARYING attribute.
ļ	CDAT49 (EK)	Processes PICTURE attribute.
1	CDAT4A (EK)	Processes BIT attribute.
	CDAT4B (EK)	Processes CHARACTER attribute.
	CDAT4C (EK)	Processes FIXED DIMENSIONS attribute.
	CDAT4D (EK)	Processes LABEL attribute.
	CDAT4F (EK)	Processes ADJUSTABLE DIMENSIONS attribute.
1	CDAT56 (EK)	Processes USES attribute.
	CDAT57 (EK)	Processes SETS attribute.
	CDAT58 (EK)	Processes ENTRY attribute.
l	CDAT59 (EK)	Processes GENERIC attribute.
1	CDAT5A (EK)	Processes BUILT-IN attribute.
I	CDAT60 (EK)	Processes EXTERNAL attribute.
ĺ	CDAT61 (EK)	Processes INTERNAL attribute.
	CDAT62 (EK)	Processes AUTOMATIC attribute.
	CDAT63 (EK)	Processes STATIC attribute.
	CDAT64 (EK)	Processes CONTROLLED attribute.
	CDAT69 (EK)	Processes INITIAL attribute.
ł	CDAT6A (EK)	Processes LIKE attribute.

• Table EL1. Phase EL Routine/Subroutine Directory

• Table EL1. Phase EL Routine/Subroutine Directory (cont'd)

Routine/Subroutine	Function
CDAT6B (EK)	Processes DEFINED ATTRIBUTE.
CDAT6C (EK)	Processes ALIGNED attributes.
CDAT6D (EK)	Processes UNALIGNED attribute.
CDAT70 (EK)	Processes AREA attribute.
CDAT88 (EK)	Processes POS attribute.
CDCLSC	Scans each item of DECLARE statement.
CDFATT (EM)	Applies factored attributes.
CDFLT (EM)	Applies default attributes.
CDICEN (EM)	Constructs dictionary entry.
CGENSC (EM)	Performs phase initialization and scans chain of DECLARE statements.
CHASH (EM)	Hashes BCD of identifier.
DCID1	Main scan routine.
DCIDPR	Processes factor brackets and level numbers.
ECHSKP (EK)	Initializes and passes control to Module EM.
IMPATT (EM)	Applies implicit attributes.
INTLZE	Performs initialization for each identifier declared.
POSTPR	Post-processor.
SCAN4 (EM)	Scans chain of DECLARE statements.
SELMSK	Selects correct test mask to be initialized.
STRPR	Processes inheriting of dimensions in structures.
TEMSCN	Scans ahead for next level number.

Table EW. Phase EW Dictionary LIKE

Statement or Operation Type	Main Processing Routine	Subroutines Used
Scans LIKE chain	EWBEGN	EWCOPY, EWELDM, EWINCH, EWONDM
Updates hash chain for new entry	EWHSCN	None
Calculates start of structure data from start of variable information	EWVART	None
Changes error entry to base element	EWCHEN	None
Copies dimension table entry and second file statement	EW2 FNT	EWNWBK

• Table EW1. Phase EW Routine/Subroutine Directory

Routine/Subroutine	Function
ALIGN (EV)	Provides correct alignment of base elements in likened structure.
BASED (EV)	Inserts or deletes defined slot, where only one structure is based.
CESCN	Scans dictionary to find entry corresponding to BCD in text.
EWBEGN	Scans LIKE chain.
EWCHEN	Changes error entry to base element.
EWCOPY	Copies dictionary entry into scratch storage.
EWDCCY (EV)	Copies initial dictionary entries and associated second file state- ments, etc.
EWELDM	Copies entry into scratch storage with dimension data removed.
EWELTS	Tests whether the likened structure is dimensioned.
EWEND	Handles transfer of control to next phase.
EWERNC	Processes erroneously "likened" major structure.
EWHSCN	Updates hash chain for new entry.
EWINCH	Completes entry copy and places it in dictionary.
EWNOLK	Tests whether original structure is dimensioned.
EWNWBK (EV)	Obtains new dictionary block and terminates current one in use.
EWONDM	Copies entry into scratch storage, inserting dimension information.
EWORDM	Processes dimension information in original structure.
EWSTRI	Tests validity of likened structure.
EW2FNT (EV)	Copies second file statement and associated dictionary reference.

• Table EY. Phase EY Dictionary ALLOCATE

Statement or Operation Type	Main Processing Routine	Subroutines Used
Scans text for explicitly pointer- qualified based variables	IEMEX	EY14
Copies dictionary entries for explicitly qualified based varia- bles	EY14	HASH, ATPROC, DICBLD, STRCPY
Second file pointers. Scans ALLO- CATE statements	IEMEY	ATPROC, DICBLD, HASH, STRCPY
Completes copied dictionary entry for an allocated item	ATPROC with second entry point ATPROD	MOVEST
Controls ATPROC and ATPROD routines for each member of a structure	STRCPY	ATPROC, ATPROD

• Table EY1. Phase EY Routine/Subroutine Directory

Routine/Subroutine	Function	
ATPROC/ATPROD (EZ)	Complete copied dictionary entry for allocated item by including attributes from ALLOCATE and second file statements.	
DICBLD	Collects attribute given for an identifier and copies its dictionary entry.	
EY16	Processes ALLOCATE statements.	
EY17	Processes identifier in ALLOCATE statement.	
EY21	Processes major structures.	
HASH	Hashes BCD of identifier to obtain its dictionary reference.	
IEMEX	Scans text for explicitly pointer-qualified variables.	
EY14	Copies dictionary entries for explicitly qualified based variables.	
IEMEY	Scans second file, reverses pointers. Scans ALLOCATE statements.	
MOVEST (EZ)	Copies second file statement and associated dictionary entry.	
STRCPY	Controls ATPROC and ATPROD for each member of structure.	









Table MB1. Phase MB Routine/Subroutine Directory

Routine/Subroutine	Function	
DRFTMP	Makes temporary descriptor from a dictionary reference.	
GETWKS	Obtains workspace to accommodate a variable of given type.	
MB0001	Scans source text.	
МВ0004	Multi-switch for triples of interest.	
MB0010	On reaching end-of-text marker, releases remaining block, and releases control of phase.	
MB0011	PSI operator; starts new entry in stack for pseudo-variable.	
MB0012	PSI' operator; completes stack entry and generates code for data list items.	
MB0013	ASSIGN; completes stack and rescan group of assignments, putting target descriptions out in correct sequence, generates code for pseudo-variable in stack.	
MB0014	Multiple ASSIGN; places any target descriptors in stack.	
MB0020	Constructs pseudo-variable stack entry:	
MB1310	Resets input pointer to start of sequence of ASSIGNS.	
MB1311	Rescans ASSIGNS and associated TMPDS from stack in reverse order.	
MB1316	Tests for end of stack.	
MB1318	Tests for pseudo-varaible TMPD.	
MB1 320	Generates code for pseudo-variable.	
MMV 3A 5	Moves one triple to output.	
MVTMPD	Places temporary descriptor in stack.	
OUTMPD	Places temporary descriptor in output string.	
SWITCH	Changes scanning table.	
TARGET	Obtains temporary workspace for pseudo-variable, if necessary.	

• Table MD. Phase MD Pseudo-Code In-Line Functions

	Statement or Operation Type	Main Processing Routine	Subroutines Used
	Scans text	Phase LA (SCAN)	None
	Builds up function stack	LFARIN	None
	Builds up argument stack	LFC OM	None
	Moves generated code to output block	LFMOVE	MV3(LA)
	Generates in-line code and library calling sequences	LFEOF2	SNAKE, ROPE

• Table MD1. Phase MD Routine/Subroutine Directory

LFARI1	Continues scan for in-line functions.
LFARIN	Builds up function stack.
LFCOM	Builds up argument stack.
LFDR	Unpacks dictionary reference of argument when argument triple found.
LFEOF2	Calls subroutines to generate in-line code.
LFIGN	Removes triple from text if inside an in-line function.
LFSPEC	Branches if IGNORE triple or not an in-line function.
ROPE	Generates code for STRING function.
SNAKE	Generates code for ADDR function.

• Table MS. Phase MS Pseudo-Code Subscripts

	Statement or Operation Type	Main Processing Routine	Subroutines Used
	Scans text	SBSCAN	None
	Calculates element offset	SBSTIH	SBASS, SBCOBI, SBGNOR, SBMVCD, SBNEST, SBSUBP, SBSUDV, SBXOP, UTTEMP, SBOPT
	Checks subscript range	SBSBRN	None

• Table MS1. Phase MS Routine/Subroutine Directory

I

1

Routine/Subroutine	Function	
SBASS	Updates scan pointer over an assignment.	
SBCOBI (MT)	Converts subscript to binary integer.	
SBERR (MT)	Puts error message into dictionary.	
SBGNOR (MT)	Allocates an odd symbolic register.	
SBMVCD (MT)	Generates pseudo-code and moves it into output text block.	
SBNEST (MT)	Handles nested subscript situation.	
SBOPT	Calculates element offset in optimizable cases.	
SBSBRN (MT)	Checks subscript range.	
SBSCAN	Branches to LA for scan.	
SBSTIH	Generates code to calculate element offset.	
SBSUBI	Saves array name.	
SBSUBP (MT)	Handles end of subscript list.	
SBSUDV	Generates code to set up the dope vector of an array of adjustable strings.	
SBS05	Generates code to multiply subscript by multiplier.	
SBS06	Compiles code to convert to fixed binary.	
SBS002	Checks for occurrence of subscript.	
SBS029	Generates code to multiply subscript by 4 or 8.	
SBTRID	Scans for comma, subscript prime, or subscript triple.	
SBXOP (MT)	Handles special index feature.	
SCAN	Controlling scan of text.	
UTTEMP (MT)	Allocates workspace.	

Main Processing Routine	Subroutines Used
NAINIT	SCINIT (LA)
NASC1, NASC2, NASC3	SC1, SC2, SC3 (all in LA)
STOP	NAUT1
EXIT	NAUT1
IF	NAUTD, NAUT16, NAUT21, ZSTUT1
ON	NAUTD, NAUT6, NAUT16, SC5 (LA)
PROCP, BEGINP	NAUT1
RETURN	NAUT1
NA3002	NAUTB, NAUTCA, NAUT1, NAUT12
NA3013	NAUTA, NAUTB, NAUTCA, NAUTD, NAUTF, NAUT1, NAUT7, NAUT8, NAUT9, NAUT11, NAUT12
GOTO	NAUTD
GOLN	NAUTD
GOOB	NAUT5, NAUTD, NAUT16, SC5 (LA)
SIGNAL	NAUTD, NAUT6, NAUT16, NAUT8, NAUT10, NAUT21
REVERT	NAUTD, SC5 (LA)
	Main Processing Routine NAINIT NASC1, NASC2, NASC3 STOP EXIT IF ON PROCP, BEGINP RETURN NA3002 NA3013 GOTO GOLN GOOB SIGNAL REVERT

Table NA. Phase NA Pseudo-Code Branches, ON, Returns



•Chart QJ. Phase QJ Overall Logic Diagram



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Table PA. Phase PA DSAs in STATIC Storage

Statement or Operation Type	Main Processing Routine	Subroutines Used
Scans Entry Type 1 chain for blocks eligible for STATIC DSAs	PADSA	DSASIZ, DVSIZE
Makes a dictionary entry for each STATIC DSA	DICENT	None
Sorts STATIC chain (called from PD)	SCSORT	None
Scans STATIC chain for INTERNAL arrays; calculates number of ele- ments for those arrays needing initialization. Allocates storage for arrays and, if necessary, for secondary dope vectors	ARR SCN	None

Table PA1. Phase PA Routine/Subroutine Directory

Routine/Subroutine	Function		
ARRSCN	Scans STATIC chain for INTERNAL arrays; allocates storage for arrays and secondary dope vectors (called from PH).		
DICENT	Makes a dictionary entry for each STATIC DSA.		
DSASIZ	alculates size of DSA excluding Register Allocator Workspace.		
DVSIZE	Scans AUTOMATIC chain for variables requiring dope vectors, and calculates size of dope vectors.		
PADSA	Determines eligibility of a block for a STATIC DSA.		
 SCSORT 	Sorts STATIC chain (called from PD).		

• Table QU. Phase QU Alignment Processor

Statement or Operation Type	Main Processing Rov ine	Subroutines Used
Tests pseudo-code instructions for misaligned operands and deduces the correct alignment	ALIGNQ	ALREGQ, MVCMAK, REGENT
Generates a move character (MVC) instruction for a misaligned oper- and	MVC MAK	ABEOT, NEXREG, OUTEST, PSMOVE, REMOVE, SNEXT, TRANS
Skips a pseudo-code item	T3	TNEXT
Processes the load address (LA) pseudo-code instruction	TLA	TRR
Processes the library calling sequence in the pseudo-code	TLTB	ABEOT, T 3
Processes the L pseudo-code instruction	TLL	ALIGNQ, ALREGQ, OUTESI, PSMOVE, REMOVE, SNEXT, TRANS, TRR
Processes pseudo-code instructions, other than L and LA, that may have misaligned operands	ТНТ 	ALIGNQ, TRRS
Examines a pseudo-code item and passes control to the appropriate processing routine	TRANS	T3, TABS, TDROP, TEOP, THI, TLA, TLIB, TLL, TRR, TSN

• Table QU1. Phase QU Routine/Subroutine Directory

Routine/Subroutine	Function
ABEOT	Outputs terminal error message.
ALREGQ	Tests whether or not the register is in the register table.
NEXREG	Gets a symbolic register.
OUTEST	Gets a new output text block if required.
PSMOVE	Fills current output text block and gets a new one.
REGENT	Makes an entry in the register table for a register that has been loaded with the address of a misaligned operand.
REMOVE	Copies text into the output text block.
SNEXT	Accesses next pseudo-code item in the source text.
TABS	Scans absolute code and copies it onto the output text if necessary.
TDROP	Removes dropped registers from the register table.
TEOB	At the end of a source text block, moves out the scanned text and gets the next source text block.
TEOP	At the end of the program, outputs the remaining text, and releases control.
TRR	Deletes an assigned register from the register table.
TSN	Updates the statement number slot in the communications region.

• Table QX. Phase QX Print Aggregate Length Table

Statement or Operation Type	Main Processing Routine	Subroutines Used
Scan storage chains in dictionary for aggregate entries	SCANC	ANAGG, PRNTAB
Analyze aggregate dictionary entries and print table entry	ANAGG	ANCOB, EXTENT, FINALA, FIRSTA, FORMAL, GETVO, GETSB, MAKEN, PRHED, SORTEN, VOPLUS

• Table QX1. Phase QX Routine/Subroutine Directory

Routine/Subroutine	Function
ANAGG	Analyzes dictionary entries for a majór strúcture or non-structured array.
ANCOB	Finds original major structure dictionary entry for a COBOL major structure.
EXTENT	Calculates length in bytes of a data variable, label, task, event, or area.
FINALA	Calculates address of final basic element of a major structure.
FIRSTA	Calculates address of first basic element of a major structure.
FORMAL	Calculates length of a non-structured array.
GETVO	Gets virtual origin of a dimensioned variable.
GETSB	Sets pointer to BCD in a dictionary entry.
MAKEN	Makes an entry in text block for each aggregate.
PRHED	Prints main heading and sub-heading of table.
PRNTAB	Prints Aggregate Length Table.
SCANC	Scans STATIC, AUTOMATIC and CONTROLLED chains in dictionary for aggregate entries.
SORTEN	Sorts text block entry for aggregate so that the entries are chained in collating sequence order of the aggregate identifiers.
VOPLUS	Calculates address of first or last element of major structure.





APPENDIX A: GUIDE TO PHASES AND MODULES

This a es, phys within th name is :	appendix rei sical phases he physical IEMAA.	lates the logical phas- s, and modules contained phases. The compiler	BC	BC, BE, BF	Initial scan and tran- slation phase for compile-time processor
PHYSICAL PHASE	MODULES	DESCRIPTION	BG	BG,BI,BJ	Final scan and replace- ment phase for compile- time processor
<u>Compiler</u>	Control AA	Controls running of	BM	BM, BN	Error message printout phase
	АВ	compiler Performs detailed ini-		BO, BV	Contain the diagnostic messages
	AC	Writes records on intermediate file	BW		Cleanup phase for compile-time processor
		SYSUT3	<u>Read-In</u>	Logical Pha	se
	AD	Performs interphase dumping as specified in the DUMP option		CĂ	Read-In phase common routines
	AE	End of read-in phase		CC	Read-In phase common routines
	AF	Controls system genera-		CE	Keyword tables
		tion compiler options	CI	CG,CI	Read-In pass 1
	AG	put, reopens for input		СК	Keyword tables
	АН	Format annotated dic- tionary dumo	CL	CL,CM	Read-In pass 2
	AI,AJ	Format annotated text		CN	Keyword tables
	·	dump	CÒ	CO, CP	Read-In rass 3
	AK	Closing phase of com- piler		CR	Keyword tables
	Δ.Τ.	Controls extended dic-	CS	CS,CT	Read-In pass 4
	AU	tionary compilation	CV	CV,CW	Read-In pass 5
	AM	Phase marking	Dictiona	ry Logical	Phase
	AN	Controls normal dic- tionary compilation	ED	ED	Initialization, subroutine package for Declare Fass 2
	ВХ	48-character set prep- rocessor	EG	EF,EG	Initialization
	JZ	Builds second half phase directory	EI	eh,ei,ej	First pass over DECLARE statements
<u>Compile-t</u>	ime Process	sor Logical Phase	EL	EK,EL,EM	Second pass over DECLARE statements
	AS	Resident phase for compile-time processor	EP	EP	Constructs dictionary
	AV	Initialization phase for compile-time proc- essor			ENTRY and CALL state- ments

EW	EV,EW	Constructs dictionary	IA	IA, IB, IC	Stacks cperators and operands
		entries for LIKE attri- butes	IG	IG	Processes array and structure arguments and
EΥ	EX,EY,EZ	Constructs dictionary			built-in functions
		and for explicitly qualified based varia-	IL	IL	Preprocessor for gener- ic functions
FΔ	FA FB	Dies.	IM	IM, IN, IR IO	Processes generic func-
1.11	(4,10	source text	ፐጥ	11,12	Processes function tri-
FΈ	FE,FF	Changes BCD to dic- tionary references	11		ples
FI	FI	Checks validity of dic-	IX	IX	POINTER and AREA check- ing
		tionary references	JD	JD	Evaluates constant
FK	FK	Rearranges attributes			expressions
FO	FO, FP	Constructs dictionary entries for ON-	<u>Aqqreqat</u>	tes Logical	Phase
		conditions	JI	JI,JJ	Struccure pre-preprocessor
FÇ	FQ	Checks validity of	TT	דד עד דד	St rugt und proprodos jor
ъø			77		Structure preprocessor
L.T	F1,F0	house-keeping	JK 	JK,JL,JM	Structure processor
FV	ev, ew	Merges second file	JP	JP	Checks DEFINED chains
		statements into text	<u>Pseudo-(</u>	Code Logical	Phase
FX	FX,FY,FZ	Processes identifiers for cross reference and	LA	LA	Utility scanning phase
		attribute listing	LB	LB,LC	Generates triples to
Pretrans	slator Logic	cal Phase			and CCNTROILED scalar variables
GA	GA	Constructs DECLARE and OPEN control blocks	LD	LD	Constructs dictionary
GB	GB,GC	Modifies I/O statements			entries for initialized STATIC scalar variables
GK	GK	Checks parameter match-			and arrays
		ing	\mathbf{LG}	LG,LH	Expands CO loops
GO	GO	Preprocessor for second check on parameters	LR	LR	Initialization for Phase LS
GP	GP,GQ,GR	Second check on param- eters	LS	ls,LT,LU	Converts expression triples to pseudo-code
GU	GU,GV	Processes CHECK condi- tion statements	LV	LV	Provides string han- dling facilities
HF	HF, HG	Processes structure assignments	LW	LW	Initialization for phase IX
нк	HK,HL	Processes array assign- ments	LX	LX,LY	Converts string triples to pseudc-code
HP	НР	Processes items defined using iSUBs	MB	MB, MC	Constructs pseudo-code for pseudo-variables
<u>Transl</u> at	or Logical	Phase	MD	MD	Scans for ADDR and
			•		

ł		STRING functions and generates code for each	OP	OP, OQ	Generates pseudo-code for further in-line conversions
ME	ME	Constructs pseudo-code for in-line functions	OS	os, ot, ou	Converts constants to required internal form
MG	MG,MH	Constructs pseudo-code for in-line functions			-
мт	мт.мт	Constructs pseudo-code	Storage	Allocation	Logical Phase
		for in-line functions	PA	PA	Puts eligible DSA's into STATIC
MK	MK	Constructs pseudo-code for in-line functions	PD	PD	First STATIC storage
ML	ML	Processes generic entry names	PH	PH	Second STATIC storage
ММ	MM - MN - MO	Processes CALL and			allocation, phase
		function procedure invocations	PL	PL,PM	Constructs symbol tables and DEDs
MP	MP	Reorders BUY and SELL statements	PP	PP	Sorts AUTOMATIC chain
MS	MS,MT	Constructs pseudo-code	PT	PT,PU,PV	Allocates AUTOMATIC storage
		for subscripts	QF	QF,QG,QH	Constructs prologues
NA	NA	Generates pseudo-code for branches, RETURN triples, etc.	QJ	QJ,QK,QL	Allocates DYNAMIC stor- age
NG	NG	Generates Library call- ing sequences for DELAY	QU ·	QU	Aligns misaligned oper- ands
NJ	nj, nk	Generates Library call-	QX	QX	Lists lengths of aggre- gates
		ing sequences for exe- cutable RECORD-oriented	<u>Register</u>	Allocation	Logical Fhase
NM	NM, NN	Generates Library call-	RA	RA, RB, RC	Processes addressing mechanisms
		ing sequences for exe- cutable STREAM-oriented input/output statements	RF	RF,RG,RH	Allocates physical reg- isters
NT	NT	Pre-processor for NU	<u>Final As</u>	sembly Logi	cal Phase
NU	NU, NV	Generates Library call-	TF	TF	Assembly first pass
		data/format lists	TJ	tj , tk	Optimizacion
OB	OB, OC	Processes compiler	TO	TO, TP, TQ	Produces ESD cards
		variables	TT	TT " TU	Assembly second pass
OD		Pseudo-code assignment	UA	UA,UB,UC	Final assembly initial values, first pass
OE	CD,OE,OF	Constructs Pseudo-code for assignments	UD	UD, UB, UC	Generates RLD and TXT
OG	OG, OH	Generates library calling sequences			vectors for STATIC DSAs
OM	OM, ON, OO	Generates pseudo-code	UE	UE,UB,UC	Final assembly initial values, second pass
		sions in-line	UF	UF, UG, UH	Produces listings

UI	UI,UG,UH	Completes final assem-	XA,XB	Constructs the third phase list
		51/ 11001.90	XA,XC	Controls the printing of messages
Error Ed:	itor		XF	Message address blocks
XA	XA	Determines whether	<u> </u>	nessage duaress stoons
		there are diagnostic messages to be printed	XG,YY	Contain the diagnostic messages

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APPENDIX C: INTERNAL FORMATS OF DICTIONARY ENTRIES

This appendix describes the formats of dictionary entries during the compilation of a source program. The appendix is organized in the following manner:

- 1. Dictionary entry code bytes
- 2. Dictionary entries for ENTRY points
- 3. Code bytes for ENTRY dictionary entries
- 4. Dictionary entries for DATA, LABEL, and STRUCTURE items
- 5. Code bytes for DATA, LABEL, and STRUC-TURE dictionary entries
- Uses of the OFFSET 1 and OFFSET 2 6. slots in DATA, LABEL, and STRUCTURE dictionary entries
- 7. Dictionary entries for:

label constants data constants formal parameters FILE entries TASK and EVENT data internal library functions parameter descriptions CN conditions PICTURES expression evaluation workspace dope vector skeletons symbol table entries AUTOMATIC chain definitions DED dictionary entries FED dictionary entries temporary dope vectors BCD entries second file statements

8. Dimension tables

1. **DICTIONARY ENTRY CODE BYTES**

The dictionary is used to communicate a complete description of every element of the source program, the compiled object program, and the compiler diagnostic messages between phases of the compiler; the text describes the operations to be carried out on the elements.

Each type of element has a characteristic dictionary entry, which is identified by a code occupying the first byte of the entry. In general, each type of element has a different code byte, but in order to permit rapid identification of dictionary entries, the code bytes have been allocated on the following basis:

First Half Byte

Bit Position	Bit <u>Value</u>	Meaning
0	0 1	entry has BCD entry has no BCD
1*	0 1	entry is to be chained entry not to be chained
2	0 1	not a member of structure member of structure
3	0 1	not dimensioned dimensioned

*This bit only applies to Phase FT which constructs the storage class chains by a sequential scan of the dictionary; later in the compiler, items with this bit on are added to the storage class chains.

Second Half Byte

In the second half byte, the following codes have the meanings shown, unless the first half byte is X'C':

x '7' means label variable means task identifier means event variable X'C' X'D' X'E' means structure X'F' means data variable

The second and third bytes of every dictionary entry contain the length, in bytes, of the entry. If the entry has BCD (i.e., the first bit of the entry is zero), this length count does not include the BCD; instead, the BCD, which follows the main body of the entry, is preceded by a single byte containing one less than the number of characters of BCD.

Using this general scheme, the code bytes allocated for dictionary entries appear in the following table. Code bytes in the table which have no corresponding description are not allocated.

- X'00' Statement label constant
 - 01 Procedure or entry label
 - 02 GENERIC entry label
 - External entry label (entry type 4) Built-in function, e.g., DATE 03
 - 04

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- 05 Temporary variable and controlled allocation workspace06 Built-in GENERIC label, e.g., SIN

```
07
   Label variable
80
   File constant
09
A0
0B
0C
   Task identifier
0D
   Event variable
0E
0F
    Data variables (not dimensioned or a
    structure member)
10
11
12
13
14
15
16
    Dimensioned label variable
17
18
19
1A
1B
1C
    Dimensioned task identifier
    Dimensioned event variable
1D
1E
    Dimensioned data variable
1 F
20
21
22
23
24
25
26
27
    Label variable in structure
28
29
2A
2B
2C
    Task identifier in structure
2D
    Event variable in structure
2E
    Structure item
2F
    Data variable in structure
30
31
32
33
34
35
36
    Dimensioned and structured label
37
    variable
38
39
3A
3B
   Dimensioned task identifier in
3C
    structure
3D Dimensioned event variable in
    structure
3E
    Dimensioned structure item
    Dimensioned and structured data
3F
    variable
40
    Formal parameter type 1
41
```

```
42
43
44
45
46
47
48
49
4A
4B
4C
4D
    ON CONDITION entry
4E
4 F
8.0
    ENTRY type 1 -- from a PROCEDURE
    statement
81
    BEGIN statement entries -- entry
    type 1
82
    ENTRY statement -- entry type 1
    Entry type 5
83
84
    Entry type 3
    Entry type 2
Entry type 6
Label variable formal parameter or
85
86
87
    temporary
88
    Constant
89
    File formal parameter cr file
    temporary
8A
8B
8C
    Task identifier formal parameter
    Event variable fcrmal parameter
8D
8E
8F
    Data variable formal parameter or
    temporary
90
    Invocation count dictionary entry
91
92
93
94
95
96
97
    Dimensioned variable formal parameter
    or temporary
98
    File attribute entry
99
9A
9B
9C
    Dimensioned task identifier formal
    parameter
    Dimensioned event variable formal
9D
    parameter
9E
9 F
    Dimensioned data variable formal
    parameter or dimensioned temporary
A0
A1
A2
Α3
Α4
Α5
A6
    Structured label variable temporary
A7
A8
A9
```

5. CODE BYTES FOR DATA, LABEL, AND STRUCTURE DICTIONARY ENTRIES

The First Code Byte - Other 1

Bit No.	Description	Set By
1	Symbol or requires load constant if label constant	Phase EL, FT, or NU
2	Defined on	Phase EL
3	Mentioned in CHECK list	Phase FO
4	Needs DVD	Various
5	Last member in structure	Phases EL or EW
6	Variable dimensions	Phase EL
7	* dimensions	Phases EL and FT
8	* string length for data item	Phases EL and FT
	More labels follow for a label constant	Phase EG
	Major Structure - no member of the structure has a dimension or length attribute which is not *	Phase EY

The Second Code Byte - Other 2

Bit No.	Description	Set by
1	Dynamically defined	Phase EL
2	CONTROLLFD major structure with varying strings	Phase EY
3	NORMAL = O, ABNORMAL = 1	Phases EI and FT
4	Reserved	
5	Formal Parameter	Phase EI
6	INTERNAL = 0, EXTERNAL = 1	Phase EI
7	00 = AUTOMATIC or DEFINED or simple	Phase EL
and	parameter	
	01 = STATIC	Phase EL
8	11 = CONTROLLED	Phase EL

The Third Code Byte - Other 3

Bit No.	Description	Set by
	Needs dope vector	Phases EK and EY if variable dimension entries, variable string length, or in CONTROLLED storage; Phase NU when item appears in an argument list
2	Needs DED	Phase NU
3	Needs no storage for the item itself	Phase GP
4	Correspondence defined	Phase FV
5	Chameleon	Phase GP
6	Sign bit for first offset	Phase PH for STATIC and Phase PT for AUTOMATIC
7	Indication of the state of the value in the first offset 0 = rubbish 1 = good value	Phase PH for STATIC and Phase PT for AUTOMATIC
8	As above but for second address slot	Phase PH

-

The Fourth Code Byte - Other 4

Bit No.	Description	Set by
	Usage (i): An explicit alignment declaration has been made Usage (ii): A constant has been produced for this structure or array	Phase EL (for EW) Phase JK
2 and 3 	00 = Not temporary 01 = Temporary type 2 10 = Temporary not sold 11 = COBOL temporary	Phase GP, HF, HK, IM, or LB
4	Member of defined structure	Phase FV
5	Packed = 0 Aligned = 1	Phase EL
6	Major structure	Phase EL
7	No dope vector initialization	Phase GP
8	A temporary type 2 which has been incorporated in work- space 1 or RDV required. For COBOL temporaries this bit means RDV required	Phase OB

- 7 Data Precision*
- 8 Scale Factor*

*These are the apparent precision and factor derived from the BCD of the constant (see Note 2)

- 9 Type (see note 1)
- 10 DATA byte (2)
- 11 Data Precision (2)**
- 12 Scale Factor (2)**

**These bytes are inserted by the phase requesting conversion. If a picture is required, these bytes are used to contain a picture table reference (see Note 3)

- 13-14 Dictionary reference used when a phase requires a constant to be converted into a specific location in storage
- 15 BCD

Notes:

1. The type byte has the following mean-ing:

First and second bits:

- 00 normal BCD constant. The first offset slot must be relocated by the storage allocation phase, to contain the offset of the converted constant from the start of STATIC storage, rather than from the start of the constants pool
- 11 the BCD is replaced by the internal form of the constant. The first offset slot is treated in the same way as for the code 00
- 10 or 01 the constant is required to be converted into a specific location in storage. The second code implies the converted constant should be made negative before being stored

Sixth bit: 1 indicates that the constant requires a DED.

Seventh bit: 1 indicates that the constant requires a dope vector.

Eighth bit: 1 indicates that no conversion is required.

- 2. After the constants processor the bytes 6 through 8 will contain the offset of the constant from the start of the pool of constants. If a dope vector is requested then the offset of this from the start of the constants pool is eight less than that of the converted constant.
- 3. Should a DED be required, this will be constructed by Phase FL. The two bytes, precision(2) and scale factor(2), will contain a dictionary reference of a DED dictionary entry. If the constant requires a dope vector then Phase OS will make a dictionary entry for it, and the dictionary reference preceding the ECD will be the dictionary reference of this.

Task Identifiers and EVENT Data

The format of the dictionary entries for task identifiers and EVENT data is, apart from the initial code byte, the same as that for a label variable.

Dictionary Entries for Built-in Functions

The format is:

6-8

9-10

- Byte Number Description
 - 1 Code byte X'04'
 - 2-3 Length
 - 4-5 Hash chain later becomes the STATIC chain

Offset - gives the position in STATIC storage of the load constant for Library routine

Code bytes - the first code byte contains a value which identifies the built-in function and also provides information about it. It is used mainly by phases IM and MD-MM inclusive. The second code byte contains further information about the builtin function (See "Second Code Byte.")

11-12 DECLARE statement number

Appendix C: Internal Formats of Dictionary Entries 363

13	Level		further information about the function
14	Count	13	Level
15	BCD length-1 BCD	14	Count

Second Code Byte

The second code byte contains the following information:

Eit Number Description

1	May	be	passed	as	an	argument

2 May have an array as an argument

- 3 Must have an array as an argument
- 4 Is a pseudo-variable
- 5 Indicates to which of the two tables the offset refers
- 6 May have an array (or structure) as an argument, but will return a scalar result

Internal Library Functions

Library routines, other than built-in or GENERIC functions, are known as Internal Library Functions. Their dictionary entry format is as follows:

<u>Byte Number</u>	Description
1	Code Byte X'C2'
2-3	Length
4-5	Hash chain
6-8	Offset
9	Library Code – identifies the particular Library rou- tine required
10	Not used
11-12	Code Bytes - the first code byte contains a value used by phase MG to pick up com- plete information about the Library function. The sec- ond code byte contains

BCD entries

BCD entries are used when the LIKE or DEFINED attributes are used. A short dictionary entry with the format given below is used. This is pointed at by the dictionary entry with the attribute.

<u>Byte Number</u>	Description
1	Code Byte X'40"
2-3	Length
4	BCD length-1
5	BCD

Dictionary Entry for Parameter Descriptions

Dictionary entries for parameter descriptions are identical with the normal entry for data variable, label variable, structure, file, or entry points, except for the following details:

Hash chain contains pointer to formal parameter type 1. After Phase FT this pointer is moved to the tytes containing level and count

No BCD is present

No block identification is present for ENTRY or FILE

The code byte for an entry point - referred to as entry type 6 - is X'86'

ON Statements

Entries for ON statements are made by Phase FO, and contain the following:

<u>Byte Number</u>	Description
1	Code Byte X'CD'
2-3	Length
4-5	AUTOMATIC chain

6-8	Offset	PICTURE Entry	
9	Code byte as supplied by the Read-In Phase	The format table in the d	of an entry in the picture ictionary.
10	Diosk lovel	Byte Number	Description
10	BLOCK LEVEL	1	Code Byte X'C8'
11	Block count	2-3	Length = $L+13$
12	n	4-5	Contains address of next entry in picture chain
13 onwards	n dictionary references of variables or ON condition entries	6-8	Usage (1) (Before Phase FQ) Dictionary reference of associated declare or format statement, right adjusted
ON Condition			Usage (11) Offset in STATIC storage
This entry :	is made by Phase FO:	9	Code Byte (after Phase FQ) (See Code Byte description)
<u>Byte Number</u>	Description	10	P - the number of digit
1	Code Byte X'4D'		ic picture.
2-3	Length	11	Q - the number of digit
4-5	Hash chain later used as AUTOMATIC chain		in numeric picture. Code X'80' represents 0, X'7F'
6-8	Offset		represents +1.
9	Code byte as supplied by the read in phase	12	W - apparent length of pic- ture length of picture
10	Block level		numeric picture the length is obtained in bytes 12-13.)
11	Block count	14 onwards	Picture.
12	BCD length-1	T4 Ollwards	- TOOMTO.
13 onwards	BCD	Byte 9 - Code H	Byte

		<u>Bit Number</u>	Description
CHECK LIST ENT	£Υ	1	0 string 1 numeric
This entry	is made by Phase FO:	2	0 correct
Byce Mulliber	Description		1 61101
1	Code Byte X'C8'	3	0 not sterling 1 sterling
2-3	Length		0 h t
4	n where n is the number of dictionary references fol-	4	1 long
	lowing	5	Not used
5 onwards	Dictionary references (2n bytes)	6	0 decimal 1 binary

I	7	0 fixed 1 floating
	8	Not used

Dictionary Entry for Workspace Requirement

The format for a dictionary entry for workspace requirement is:

Byte Number	Description
1	Code Byte X'C8' or X'CA'
2-3	Length = 8
4-5	Total workspace required

Offset 6-8

If the code byte is C8 this is the temporary workspace used by pseudo-code (temporary type 1).

Dictionary Entry for Parameter Lists

Dictionary entries for parameter lists have the following format:

Byte Number	Description
1	Code Byte X'C5'
2-3	Length
4-5	STATIC chain
6-8	STATIC offset
9-10	Assembled length

11 onwards Contains DCA's

Dictionary Entries for Dope Vector Skeletons

<u>Byte Number</u>	Description
1	Code Byte X'C6'
2-3	Length
4-5	STATIC chain
6-8	Offset in STATIC
9-10	Dictionary reference DECLARE number

11 onwards Bit pattern of skeleton dope vector

This entry is constructed by Phase PD

Byte Number	Description
1	Code Byte X'C7'
2-3	Length
4-5	STATIC chain
6-8	Offset in STATIC of DED
9-11	Actual DED if not pictured. If a picture is involved, the last two bytes are the dictionary reference of the picture table entry

12-13 Offset in STATIC storage of symbol table entry

Symbol table entries are made by Phase

- 15-16 Dictionary reference of next item in the symbol table for this block
- 17-18 Dictionary reference of item requiring entry in symbol table

Dictionary Entry for AUTOMATIC Chain Delimiter

An entry for AUTOMATIC chain delimiter is made by Phase PP.

Byte Number	Description
1	Code Byte X'CC'
2-3	Length
4-5	AUTOMATIC chain
6-7	Pointer to first second file entry
8-9	Pointer to second second file entry

DED Dictionary Entry

or

An entry for a DED is created by Phase PL.

Byte Number	Description
1	Code Byte X'C7'

Symbol Table Entry

PL.

• First Level Table (80 to FF)

	8	9	A	В	С	D	E	F
0	ТО	LINE	A	HYBRID QUAL		SN		FL DEC IMAG
1	ALLOCATE		CALL	ENTRY		<u>ASSIGN BY</u> <u>NAME</u>		FL DEC REAL
2	BY		В			SL		FL BIN IMAG
3	FREE		RETURN	PROC		SL	ON PROC	FL EIN REAL
4	WHILE		Р	CHECK	t [1	CN		FIX DEC IMAG
5		DISPLAY	GOOB+	BEGIN		GET	+	FIX DEC REAL
6	SNAP	COL	R			CL		FIX BIN IMAG
7		SIGNAL	<u>GO TO</u>	ITDO	WRITE	PUT	END DO	FIX BIN REAL
8	SYSTEM	E		NO CHECK	2nd LEVEL MARKER		END ITDO	INTEGER
9	WAIT	REVERT		<u>DO</u>	<u>READ</u>	UNLOCK	END	STG DEC REAL
A	THEN	F		DATA LIST DO				
в	DELAY		INIT LABEL	IF	LOCATE	REWRITE	END PROG	ON
C	CONTROL VARIABLE			SN2		`		ARRAY CROSS SECTION
D	EXIT	NULL	DECLARE	ELSE	DELETE	OPEN	END BLOCK	CHAR CONSTANT
E		с	X	NO SNAP				ISUB
F	<u>STOP</u>	ASSIGN		FORMAT		<u>CLOSE</u>		BIT CONSTANT

+ Go Out Of Block

	Second Level	Table	(00)	to	7F)	(preceded	bv	second	level	marker	byte	C8)
•	2000110 20102			~~		(prococca	~ 7	000010	TCACT	THOTICT		

	0	1	2	3	4	5	6	7
0		FILE	r		DECIMAL	OPTIONS	EXTERNAL	AREA
1					BINARY	IRREDUCIBLE	INTERNAL	POINTER
2		LIST			FLOAT	REDUCIBLE	AUTOMATIC	EVENT
3		EDIT	EVENT ¹		FIXED	RECURSIVE	STATIC	TASK
4	TITLE	DATA	PRIORITY		REAL	ABNORMAL	CONTRCLLED	CELL
5	ATTRIBUTES	STRING	REPLY		COMPLEX	NORMAL	SECONDARY	BASED
6	PAGESIZE	SKI			PRECISION 1	USES		OFFSET
7	IDENT	LINE			PRECISION 2	SETS		•
8	LINESIZE	PAGE			VARYING	ENTRY	INITVAR 1	
9		COPY			PICTURE (NUM)	GENERIC	INITIAL	INITVAR 2
A	INTO	KEYTO			BIT ATTRIBUTE	BUILTIN	LIKE	
в	FROM	TASKOP			CHAR ATTRIBUTE		DEFINED	
с	SET		IN		DIMS (INTEGERS)		ALIGNED	
D	KEY				LABEL		UNALIGNED	
E	NOLOCK	KEYFROM		,			UNALIGNED	
F	IGNORE	FORMAT LIS		BY NAME	DIMS (NON-INTEGER)	RETURNS	POS	PICTURE (CHAR)

¹The EVENT built-in function and pseudo-variable are known externally by the equivalent name COMPLETION.

BYTE NAME	OFFSET	BIT (HEX)	BIT NAME	DESCRIPTION Bits are set on, on encountering:-
ZFLAG1	ZCOMM+16	80 40 20 10 08 04 02 01	ZDEFFL ZAWAFL ZSECFL ZDIMFL ZCHKFL ZONFL ZSTRFL ZDECFL	DEFINED attribute ALLOCATE statement Second File statement Dimension attribute CHECK/NOCHECK prefix ON, SIGNAL or REVERT statement Structure DECLARE statement
ZFLAG2	+17	80 40 20 10 08 04 02 01	ZLIKFL ZINTST ZOPCFL ZGTPFL ZGOTFL ZTEPFL ZPICFL ZISBFL	LIKE attribute STATIC INITIAL OPEN/CLOSE statement GET/PUT statement GO TO statement TASK/EVENT/PRIORITY options, REPLY statement PICTURE attribute/format item iSUB defining
ZFLAG3	+18	80 40 20 10 08 04 02 01	ZCONTG ZSETFL ZOSSFL ZARGFL ZINLFL ZDIOFL ZRECIO ZINTAC	UNALIGNED(NONSTRING) attribute SETS attribute DELAY, DISPLAY, WAIT statement Argument list INITIAL Label DATA directed I/O RECORD I/O AUTO/CTL initialization
ZFLAG4	+19	80 40 20 10 08 04 02 01	ZFREE STM256 FILEFL ZPUTFL ZGETFL ZPTRFL ZRODFL	FREE statement More than 256 statements Files present SPARE PUT DATA GET DATA Pointer Qualifier STATIC DSA Entry
ZFLAG5	+20	80 20 10 to 01	ZFTASK ZDENFL ALCSLM	TASK/EVENT/PRIORITY option on a CALL statement Set by FT ALLOCATE, with second level marker Spare

• Table 3. Communications Region. Bit Usage in ZFLAGS

APPENDIX G: SYSTEM GENERATION

For full details of the system generation process, see <u>IBM System/360 Operating</u> System: System Generation, Form C28-6554.

During the system generation process, a control section named IEMAF is assembled (see Figure 13) containing a table consisting of five fixed-point values aligned on full-word boundaries, immediately followed by a bit string field that is twelve bytes in length. The five fixed-point values are related to the compiler options LINECNT, SIZE, SORMGIN (start), SORMGIN (end), and CONTROL COLUMN (PAGECTL), respectively. Bits 1 to 39, and 43 to 46 in the string are used to specify the default status of the options. Bits 47 to 91 in the string are used to specify if an option keyword is to be deleted or not. A "1" in the bit string means "yes" and a "0" means "no". The remaining bits in the string are spare bits not currently in use. Figure 14 shows the bit identification table associated with the control section.

IEMAF	START
	DC F'60'
1	DC F'99999'
	DC F'2'
	DC F'72'
	DC F'0'
	DC B' 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	DC B 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 SWITCHES
	DC B' 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	DC B' 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	DC B' 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	DC B' 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Figure 13. The IEMAF Control Section

ST	4,84(13)
\mathbf{ST}	2,80(13)
ST	2,8(13)
MVI	76(13),X'00'
ST	2,96(13)
BR	14
L	15,32(11)
BR	15

- * END SUBROUTINE
- * EPILOGUE SUBROUTINE

TM	1(13),X'80'
BC	8,60(15)
L	2,80(13)
LTR	2,2
BC	7,60(15)
С	13, PR IHEQSLA(12)
BC	7,60(15)
L	13,4(13)
ST	13, PR IHEQSLA(12)
TM	0(13),X'80'
BC	1,50(15)
L	13,4(13)
в	34(15)
ST	2,8(13)
LM	14,11,12(13)
BR	14

L	15,AIHESAFA
BR	15

END SUBROUTINE

*

*

*

STATIC PROLOGUE SUBROUTINE

L LTR BC L MVC LA ST ST LR ST ST ST ST ST	4, PR IHEQINV(12) 4, 4 11,86(15) 7, PR IHEQLWO(12) 80(4,3),80(7) 4,1(4) 4, PR IHEQINV(12) 4,84(3) 76(3),X'00' 3,8(13) 13,3 3, PR IHEQSLA(12) 3,4(13) 13,PR IHEQSLA(12) 2,2 2,80(13) 2,8(13) 2,96(13)
ST	$Z_{\mathbf{w}} \otimes (\bot 3)$
ST	2,96(13)
BR	14

END SUBROUTINE

APPENDIX I: DIAGNOSTIC MESSAGES

The messages produced by the PL/I (F) Compiler are explained in the publication IBM System/360 Operating System, PL/I (F) Programmer's Guide, Form C28-6594. The following table associates a message number with the particular phase and module in which the corresponding message is generated.

	ed.				IEMOO64I	Read	In	CC
					IEM0066I	Read	In	CG
	Message				IEM0067I	Read	In	CL
	Number	Logic	cal_Phase	Module	IEM0069I	Read	In	CG
					IEM0070I	Read	In	CG
	IEM0001I	Read	In	CA	IEM0071I	Read	In	CG
	IEM0002I	Read	In	CA	IEM0072I	Read	In	CG
	IEM0003I	Read	In	CA, CP	IEM0074I	Read	In	CG
	IEM0004I	Read	In	CA	IEM00751	Read	In	CG
	IEM0005I	Read	In	CA, CL	IEM0076I	Read	In	CG
	IEM0006I	Read,	In	CA	IEM0077I	Read	In	CG
	IEM0007I	Read	In	CA	IEM0078I	Read	In	CG
	IEM00081	Read	In	CA	IEM0080I	Read	In	CG
	TEM0009T	Read	In	CA	IEM00811	Read	In	CG
	TEM0010T	Read	Tn	CA	IEM00821	Read	In	CG
	TEM00111	Read	Tn	CA	TEM0083T	Read	Tn	CG
	TEM0012T	Read	In	CA	TEMOORUT	Read	Tn	ĊĠ
	TEM00121	Read	In	CA	TEMO085T	Read	Tn	CT
		Doad	In	CA	TEMOOGOT	Doad	Tn	CT
	TEMOO141	Poad	111 Tn	CA	TEMOODUT	Poad	In	CT
	TEMO0151	Read		Ch	TEMOODST	Doad	In Tn	CI
		Dead		CA	TEMOODET	Dood	111 Tp	
	IEMOUI/I	Read			1EM00901	Dood	111 Tm	CG,CI
	IEM00181	Read	In	CA	IEM009/I	Read		
	IEM00191	Read	In	CA	1EM00991	Read		
	1EM00201	Read	In	CA	TEMOTOOT	Read	In	CI
	IEM0021I	Read	In	CA	1EM01011	Read	In	CM
	IEM0022I	Read	In	CA	IEM01021	Read	In	CI
	IEM0023I	Read	In	CA	IEM0103I	Read	In	CI
	IEM0024I	Read	In	CA	IEM0104I	Read	In	CC
	IEM0025I	Read	In	CA	IEM0105I	Read	In	CC,CG
	1EM00261	Read	In	CA	IEM0106I	Read	In	CI,CV
	1EM00271	Read	In	CA	IEM0107I	Read	In	CI
	ÍEM0028I	Read	In	CG	IEM0108I	Read	In	CI
	IEM0029I	Read	In	CA	IEM0109I	Read	In	CG,CI
	IEM0031I	Read	In	CA, CL, CT	IEM0110I	Read	In	CI
	IEM0032I	Read	In	CC	IEM01111	Reađ	In	CI
	IEM0033I	Read	In	CC	IEM0112I	Read	In	CI
	1EM00351	Read	In	CC	IEM0113I	Read	In	CG,CM
	IEM00371	Read	In	CC	IEM0114I	Read	In	CI
	IEM0038I	Read	In	CC	IEM0115I	Reađ	In	CL
	IEM0039I	Read	In	CC	IEM0116I	Read	In	CI
	IEM0040I	Read	In	CC	IEM0118I	Read	In	CL
	IEM0043I	Read	In	cc	IEM0128I	Read	In	со
	IEM0044I	Read	In	CC	IEM0129I	Read	In	CL
	TEM0045T	Read	In	CC	IEM01301	Read	In	CL
	TEM0046T	Read	In	CC	IEM01311	Read	In	co
	TEMOQUET	Read	Tn	CG	TEM0132T	Read	Tn	CO
ı.	TEMOOU9T	Read	In In	CT	TEM0133T	Read	Tn	co
•	TEMO050T	Read	In	CL. CP	TEM0134T	Read	Tn	CP
	TEMOOSIT	Read	 Tn	CLCP	TEM0135T	Read	 Tn	CP
	TEMOOSIT	Road	1.1. Tn	CO	TEM0136T	Read	Tn	co
	TEMOOSZI	Read	111 Tn	co	TEMO138T	Read	Tn	CP
	TEMOUSUT	Post	111 Tn	C0	TEM01301	Read	 Tn	CP
	TEMODEET	Read	T 22	CD		Doad	Tn	CP
	TEMOODOT	Read		Cr Cm		Read	111 To	CP
1	1 EM 00561	кead	TU	CT		Read	T11	CO

IEM00571

IEM0058I

IEM0059I

IEM0060I

IEM0061I

IEM0063I

[IEM00621

Read In

Read In Read In

Read In

Read In

Read In

Read In

сс

CC

CP

CP

CP

CP

co

IEM0143I	Read	In	со
IEM01441	Read	In	CO
IEM0145I	Read	In	co

Appendix I: Diagnostic Messages 422.1

TEM0709T	Prot ranglator	GP GO GP	ТЕМ1051 Т	Translator	тм
107901			TEMIOSET	Translator	TM
1EM0/991	Pretranslator	GP, GQ, GR	TEMIOSOT		
IEM0800I	Pretranslator	GP,GQ,GR	1EM105/1	Translator	ΤW
IEM08011	Pretranslator	GP,GQ,GR	IEM1058I	Translator	IM
TEM08021	Pretranslator	GP.GO.GR	IEM1059I	Translator	IM
TEMOROST	Pretranslator	GP, GO, GP	TEM1060T	Translator	тм
TEMODOUT	Drotranglator		TEM1061T	Translator	тм
1EM08041	Pretranslator	GP, GQ, GR	TEMICOLL		TM
IEM08051	Pretranslator	GP,GQ,GR	1EM10621	Translator	TW
IEM0806I	Pretranslator	GP,GQ,GR	IEM1063I	Translator	IM
IEM0807I	Pretranslator	GP, GQ, GR	IEM1064I	Translator	IM
TEM0816T	Pretranslator	GUL GV	TEM1065T	Translator	ТМ
TEM00101	Drotranolator		TEM1066T	Translator	тм
IEMU81/I	Pretranslator	GU, GV	TEMICOUL	Translator	T 14
IEM0818I	Pretranslator	GU, GV	TEMI06/I	Translator	TW
IEM0819I	Pretranslator	gu,gv	IEM1068I	Translator	.IM
IEM0820I	Pretranslator	GU, GV	IEM1071I	Translator	IM
TEM 08 21 T	Pretranslator	GU GV	TEM1072T	Translator	IM
TEM00211	Ducturelator		TEM1073T	Translator	тм
1EM08231	Pretranslator	GU, GV			TM
IEM08241	Pretranslator	GU	IEMI0741	Translator	T M
IEM0825I	Pretranslator	gu, gv	IEM1076I	Translator	JD
IEM0826I	Pretranslator	GU, GV	IEM10821	Translator	IX
TEMOS32T	Pretranglator	HF. HG	TEM1088T	Aggregates	JK
1000021	Destronglator		TEM10001	Aggregates	JK
TEM08331	Pretranslator	nr,ng	TEM10091	Aggregates	
IEM0834I	Pretranslator	HF, HG	1EM10901	Aggregates	JK
IEM0835I	Pretranslator	HF, HG	IEM1091I	Aggregate Preprocessor	JI
IEM08361	Pretranslator	HF,HG	IEM1092I	Aggregates	JK
TEM0837T	Pretranslator	HEHG	TEM1104I	Aggregates	JP
TEMOQUOT	Drotranglator		TEM1105T	Aggregates	TP
IEMO0401	Pretraiislator		IDMIIOJI	Aggregates	
IEM08491	Pretranslator	HF, HG	TEMITOPT	Aggregates	JP
IEM0850I	Pretranslator	HF,HG	IEM1107I	Aggregates	JP
IEM0851I	Pretranslator	HF, HG	IEM1108I	Aggregates	JP
TEM0852T	Pretranslator	HF.HG	TEM1110I	Aggregates	JP
TTM00521	Drotranglator	UP UC	Т БМ1111Т	Nagregates	ŢΡ
IEM00001			TEMILITI	Aggregates	<u>т</u> р
IEM08641	Pretranslator	нк, нь	LEMITIZI	Aggregates	JP
IEM0865I	Pretranslator	HK,HL	IEM1113I	Aggregates	JP
IEM0866I	Pretranslator	HK, HL	IEM1114I	Aggregates	JP
TEM 0867T	Pretranslator	HK.HL	IEM1115I	Aggregates	JP
TEMORERT	Protranglator	нк нт.	TEM1120T	Aggregates	JP
TEMOOCOT	Ducture alater		TEM1101T	Aggregates	J.T.D.
TEM0803T	Pretranslator			Aygregates	J P
IEM0870I	Pretranslator	HK, HL	1EM11221	Aggregates	JP
IEM0871I	Pretranslator	HK, HL	IEM1123I	Pseudo-code	LD
TEM08721	Pretranslator	HK, HL	IEM1125I	Pseudo-code	LD
TEMO873T	Protranslator	HK HT.	TEM1200T	Pseudo-code	LA
100731	Destronglator		TEM1560T	Pseudo-code	LG-ON
1EM08741	Pretranslator		1 50 1 50 91		
IEM0875I	Pretranslator	HK, HL	1EM15/01	Pseudo-code	LG
IEM0876I	Pretranslator	HK, HL	IEM1571I	Pseudo-code	LG
IEM0877I	Pretranslator	HK, HL	IEM1572I	Pseudo-code	\mathbf{LG}
TEM0878T	Pretranslator	HK HI.	IEM1574I	Pseudo-code	\mathbf{LG}
TEMOQ7OT	Protranglator	нк нг.	TEM1575T	Pseudo-code	T.G
TEMOORD	Pretranslator		TEMISTOL	Psoudo-code	ונד ייד פיד
TEM08801	Pretranslator	пк, пь	TEMICOUL	Pseudo-code	
IEM0881I	Pretranslator	HK, HL	TEWIOOII	Pseudo-code	<u>ь</u> з
IEM0882I	Pretranslator	HK	IEM1602I	Pseudo-code	LS, LT, LU
IEM0896I	Pretranslator	HP	IEM1603I	Pseudo-code	LS,LT,LU
TEMOS97T	Pretranslator	HP	TEM16041	Pseudo-code	LS, LT, LU
100001	Drot ranglator	uр	TEM1605T	Pseudo-code	LS LT LI
TEM08981	Pretraistator	nr IID	TEMICOST	Decudo codo	
TEM08991	Pretranslator	HP	LEMICOUL	Pseudo-coue	
IEM0900I	Pretranslator	HP	1EM160/1	Pseudo-coae	LS, LT, LU
IEM0901I	Pretranslator	HP	IEM1608I	Pseudo-code	LS,LT,LU
TEM09021	Pretranslator	HP	IEM1609I	Pseudo-code	LS, LT, LU
TEMOGORT	Pretranslator	HP	IEM1610T	Pseudo-code	LW
TEMODOCT	Drotranclator	uD	TEM1611 T	Pseudo-code	T.W
TEM02001		11F	TEMICIT	Decudo-codo	TW
LEM0907I	Pretranslator	п г .	TEMIOICI		10 TT
IEM1024I	Translator	IA	1EM1613I	rseudo-code	ьз,ьт,ьU
IEM10251	Translator	IA	IEM1614I	Pseudo-code	LW
TEM1 026T	Translator	IA	IEM16151	Pseudo-code	ME
TEM1027T	Tranglator	ТА	TEM1616T	Pseudo-code	ME
	Tanotacor	 T N	TEM1617T		MB
TEMIOSSI	Translator	TH	IEMICI/I		MD
IEM1029I	Translator	IA	TEWT0181	Faendo-code	MB
IEM1040I	Translator	IM	IEM1619I	Pseudo-code	MВ

IEM1620I	Pseudo-code	MB	IEM1812I	Pseudo-code	os
IEM1621I	Pseudo-code	MB	IEM1813I	Pseudo-code	OS
IEM1622I	Pseudo-code	MB, ME	IEM1814I	Pseudo-code	OS
IEM1623I	Pseudo-code	MB	IEM1815I	Pseudo-code	OS
IEM1624I	Pseudo-code	MB	IEM1816I	Pseudo-code .	NJ
IEM1625I	Pseudo-code	MB	IEM1817I	Pseudo-code	NJ
IEM1626I	Pseudo-code	ME	IEM1818I	Pseudo-code	NJ
IEM1627I	Pseudo-code	ME	IEM1819I	Pseudo-code	NJ
IEM1628I	Pseudo-code	ME	IEM1820I	Pseudo-code	NJ
IEM1629I	Pseudo-code	ME	IEM1821I	Pseudo-code	NJ
IEM1630I	Pseudo-code	MG, MH	IEM1822I	Pseudo-code	NJ
IEM1631I	Pseudo-code	MI,MJ	IEM1823I	Pseudo-code	NJ
IEM1632I	Pseudo-code	MI,MJ	IEM1824I	Pseudo-code	NM
IEM1633I	Pseudo-code	ME	IEM1825I	Pseudo-code	NG
IEM1634I	Pseudo-code	ME	IEM1826I	Pseudo-code	NG
IEM1635I	Pseudo-code	ME	IEM1827I	Pseudo-code	NG
IEM1636I	Pseudo-code	ME	IEM1828I	Pseudo-code	NG
IEM1637I	Pseudo-code	ME	IEM1829I	Pseudo-code	NG
IEM1638I	Pseudo-code	ME	IEM1830I	Pseudo-code	NG
IEM1639I	Pseudo-code	MF	IEM1832I	Pseudo-code	NM
IEM1640I	Pseudo-code	MM, MN	IEM1833I	Pseudo-code	NM
IEM1641I	Pseudo-code	MM, MN	IEM1834I	Pseudo-code	NM
IEM1642I	Pseudo-code	MM, MN	IEM1835I	Pseudo-code	NM
IEM1643I	Pseudo-code	MM, MN	IEM1836I	Pseudo-code	NM
IEM1644I	Pseudo-code	MM, MN	IEM1837I	Pseudo-code	NM
IEM1645I	Pseudo-code	MM, MN	IEM1838I	Pseudo-code	NM
IEM1648I	Pseudo-code	MM, MN	IEM1839I	Pseudo-code	NM
IEM1649I	Pseudo-code	MM, MN	IEM1840I	Pseudo-code	NM
IEM1650I	Pseudo-code	MM, MN	IEM1841I	Pseudo-code	NM
IEM1651I	Pseudo-code	MM, MN	IEM1843I	Pseudo-code	NM
IEM1652I	Pseudo-code	MM, MN	IEM1844I	Pseudo-code	NM
IEM1653,I	Pseudo-code	MM, MN	IEM1845I	Pseudo-code	NM
IEM1654I	Pseudo-code	MM, MN	IEM1846I	Pseudo-code	NM
IEM1655I	Pseudo-code	MN	IEM1847I	Pseudo-code	NM
IEM1656I	Pseudo-code	ME	IEM1848I	Pseudo-code	NM
IEM1657I	Pseudo-code	MM	IEM1849I	Constant Conversions	os
IEM1670I	Pseudo-code	MP	IEM1850I	Constant Conversions	os
IEM1671I	Pseudo-code	MP	IEM1860I	Pseudo-code	NU
IEM1680I	Pseudo-code	MS	IEM1861I	Pseudo-code	NU
IEM1687I	Pseudo-code	MS	IEM1862I	Pseudo-code	NU
IEM1688I	Pseudo-code	MS	IEM1870I	Pseudo-code	NU
IEM1689I	Pseudo-code	MS	IEM1871I	Pseudo-code	NU
IEM1691I	Pseudo-code	MS	IEM1872I	Pseudo-code	NU
IEM1692I	Pseudo-code	MS	IEM1873I	Pseudo-code	NU
IEM1693I	Pseudo-code	MS	IEM1874I	Pseudo-code	NU
IEM1750I	Pseudo-code	MS	IEM1875I	Pseudo-code	NV
IEM1751I	Pseudo-code	MS	IEM2304I	Storage Allocation	PD
IEM1752I	Pseudo-code	NA	1EM23051	Storage Allocation	PD
IEM1753I	Pseudo-code	NA	IEM23521	Storage Allocation	PD
IEM17541	Pseudo-code	NA	1EM25601	Storage Allocation	QU
IEM1790I	Pseudo-code	OG, OM	1EM27001	Register Allocation	RF, RG, RH
IEM1793I	Pseudo-code	OE	1EM2/011	Register Allocation	RF, RG, RH
IEM1794I	Pseudo-code	OE	1EM2/021	Register Allocation	RF, RG, RH
IEM17951	Pseudo-code	OE	1EM27031	Register Allocation	RF, RG, RH
IEM1796I	Pseudo-code	OE	1EM2/041	Register Allocation	RF,RG,RH
IEM17971	Pseudo-code	OE	1EM27051	Register Allocation	RF, RG, RH
IEM1800I	Pseudo-code	os	1EM2/061	Register Allocation	RF, RG, RH
IEM18011	Pseudo-code	os	1EM27071	Register Allocation	RF, RG, RH
1EM1802I	rseudo-code	05	TEM2/081	Register Allocation	KF, KG, KH
IEM1803I	Pseudo-code	0S	1EM2/091	Register Allocation	KF, KG, RH
1EM18041	Pseudo-code	05	LEM2/101	Register Allocation	KF, KG, KH
LEMI805I	Pseudo-code	05		Register Allocation	KF, KG, KH
IEM1806I	rseudo-code	05	1 EMZ/121	Register Allocation	Kr, KG, KH
LEM1807I	Pseudo-code	05		DCB Generation	GA
1EM18081	Pseudo-code	05	TEM28181	DCB Generation	GA
TEMI8091	rseudo-code	05	TEMJOJOT TEMJOJOT	DCB Generation	GA
	Pseudo-code	05	1 BM20201 TGM2021T	DCB Generation	GA
TUMIOTIT	rseudo-code	03	TULICOLL	PCD GENETACIÓN	JA

IEM28221	DCB Generation	GA	IEM3851I	Compiler Control	AA
IEM2823I	DCB Generation	GA	IEM3852I	Compiler Control	AA
IEM2824I	DCB Generation	GA	IEM3853I	Compiler Control	AA
IEM2825I	DCB Generation	GA	IEM3855I	Compiler Control	AA
IEM2826I	DCB Generation	GA	IEM3856I	Compiler Control	AA
IEM2827I	DCB Generation	GA	IEM3857I	Compiler Control	AA
IEM2828I	DCB Generation	GA	IEM3858I	Compiler Control	AA
IEM28291	DCB Generation	GA	IEM3859I	Compiler Control	AA
IEM2833I	Final Assembly	TF	IEM3860I	Compiler Control	AA
IEM28341	Final Assembly	TF	IEM3861I	Compiler Control	AA
IEM28351	Final Assembly	TF	IEM3862I	Compiler Control	AA
IEM28361	Final Assembly	TF	IEM3863I	Compiler Control	AA
IEM2837I	Final Assembly	TF	IEM3864I	Compiler Control	AA
IEM 2849I	Final Assembly	TJ	IEM3865I	Compiler Control	AA
IEM28521	Final Assembly	ТJ	IEM3872I	Compiler Control	AA
IEM2853I	Final Assembly	TJ	IEM3873I	Compiler Control	AA
IEM28541	Final Assembly	ТJ	IEM3874I	Compiler Control	AA
IEM28551	Final Assembly	TJ	IEM3875I	Compiler Control	AA
IEM2865I	Final Assembly	TO	IEM3876I	Compiler Control	AA
IEM2866I	Final Assembly	TO	IEM3877I	Compiler Control	AA
IEM28671	Final Assembly	то	IEM3878I	Compiler Control	AA
IEM28681	Final Assembly	TO	IEM3880I	Compiler Control	AA
IEM2881I	Final Assembly	\mathbf{TT}	IEM3887I	Compiler Control	AA
IEM2882I	Final Assembly	TT	IEM3888I	Compiler Control	AA
IEM 2883I	Final Assembly	TT	IEM38891	Compiler Control	AA
IEM28841	Final Assembly	TT	IEM3890I	Compiler Control	AA
IEM28851	Final Assembly	TT	IEM3891I	Compiler Control	AA
IEM28861	Final Assembly	TT	IEM3892I	Compiler Control	AA
IEM2887I	Final Assembly	$\mathbf{T}\mathbf{T}$	IEM3893I	Compiler Control	AA
IEM2888I	Final Assembly	TT	IEM 3894I	Compiler Control	AA
IEM2897I	Final Assembly	UA	IEM3895I	Compiler Control	AA
IEM2898I	Final Assembly	UA	IEM3896I	Compiler Control	AA
IEM2899I	Final Assembly	UC	IEM3897I	Compiler Control	AA
IEM2900I	Final Assembly	UC	IEM3898I	Compiler Control	AA
IEM2913I	Final Assembly	UF	IEM3899I	Compiler Control	AL
IEM3088I	Dictionary, Declare	EL	IEM3900I	Compiler Control	AB
	Pass 2		IEM3901I	Compiler Control	AB
IEM3136I-	Dictionary, Declare	EL	IEM3902I	Compiler Control	AB
3149I	Pass 2		IEM3902I	Compiler Control	AB
IEM3151I	Dictionary, Declare	EL	IEM3903I	Compiler Control	AB
	Pass 2		IEM3904I	Compiler Control	AA
IEM3153I	Dictionary, Declare	EL	IEM3905I	Compiler Control	AA
	Pass 2		IEM39061	Compiler Control	AA
IEM3154I	Dictionary, Declare	EL	IEM39071	Compiler Control	AA
	Pass 2		1EM39081	compiler Control	AA
IEM3156I	Dictionary, Declare	EL	1EM 39091	Compiler Control	AL
	Pass 2	T T	1EM39101	Compiler Control	
1EM31621	Dictionary, Declare	БГ	LEM39111	Compiler Control	
	Pass Z	T . T		Compiler Concror	AD AC
1EM310/1-	Dictionary, Declare	51	TEMULOOT	Compile-time Processor	70
	Pistionary Doglaro	চা		Compile time Processor	AS
1EM31701-	Diccionary, Decrare		TEM#115T	Compile-time Processor	AS
TEM 3100 T	Dictionary Declare	FT.	TEM4118T	Compile-time Processor	AS
30131	Dags 2	L	TEM4121T	Compile-time Processor	AS.BC.BG
TEM 3584T	48 Character	BX	TEM4124T	Compile-time Processor	BC.BG
THIJJOHT	Preprocessor	211	IEM4130I	Compile-time Processor	BG
TEM 3840T	Compiler Control	АА	IEM4133I	Compile-time Processor	BC
TEM 38 41 T	Compiler Control	AA	IEM4134I	Compile-time Processor	BC
IEM 3842I	Compiler Control	AA	IEM4136I	Compile-time Processor	BC
IEM 3843I	Compiler Control	AA	IEM4139I	Compile-time Processor	BC
IEM38441	Compiler Control	AA	IEM4142I	Compile-time Processor	BC
IEM3845I	Compiler Control	AA	IEM4143I	Compile-time Processor	BC
IEM3846I	Compiler Control	AA	IEM4148I	Compile-time Processor	BC
IEM 3847I	Compiler Control	AA	IEM4150I	Compile-time Processor	BC
IEM3848I	Compiler Control	AA	IEM4151I	Compile-time Processor	BC
IEM 38491	Compiler Control	AA	IEM4152I	Compile-time Processor	BC
		~ ~	TEM 0 1 5 3 T	Compile-time Processor	BC

IEM4154I	Compile-time	Processor	BC
TEM/1157T	Compile-time	Drocessor	BC
TTN414 COT	Complie cime	Discossor	DC
TEM41001	compile-time	Processor	BC
IEM4163I	Compile-time	Processor	BC
TEM4166T	Compile-time	Processor	BC
TEM/1160T	Compile-time	Drococce	DO
15441091	compile-lime	Processor	DC
IEM4172I	Compile-time	Processor	BC
IEM4175I	Compile-time	Processor	BC
TEM/176T	Compiletime	Processor	PC
10441/01	compile-cime	FIOCESSOL	DC
IEM4178I	Compile-time	Processor	BC
IEM4184I	Compile-time	Processor	BC
T EM4187T	Compile-time	Processor	BC
10041071	compile cime	7100000001	DC
15241881	Compile-time	Processor	BC
IEM4190I	Compile-time	Processor	BC
TEM4193T	Compile-time	Processor	BC
TEMULOGT	Compilo-time	Drogoccor	DC
T EM141 901	compile-cime	PIOCessor	DC
IEM4199I	Compile-time	Processor	BC
IEM 4202T	Compile-time	Processor	BC
TEMU 205T	Compile-time	Brogossor	PC
I EM4 2001	compile-cime	PIOCESSOL	DC
IEM4208I	Compile-time	Processor	BC
IEM4211I	Compile-time	Processor	BC
TEM # 212T	Compile-time	Drocessor	BC
112192121	compile cime	110065501	50
1EM42141	Compile-time	Processor	BC
IEM4217I	Compile-time	Processor	BC
T FM4 220 T	Compile-time	Processor	BC
TEMUSOST	Compile time	Duesessor	DC
1EM42231	Compile-time	Processor	BC
IEM4226I	Compile-time	Processor	BC
T EM4 2 29 T	Compile-time	Processor	BC
TEMUDDOT	Compilo_time	Drogoscor	PC
10442321	compile-cime	PIOCESSOI	DC
1EM4235I	Compile-time	Processor	BC
IEM4238I	Compile-time	Processor	BC
Т 〒МШ 2 Ш1 Т	Compile-time	Processor	BC
10442411	compile cime	Due an an an	100
1EM42441	Compile-time	processor	BC
IEM4247I	Compile-time	Processor	BC
TFM4248T	Compile-time	Processor	BC
TEMU250T	Compile-time	Brococcor	PC
11442301	compile-cime	FIOCESSOL	DC DC
IEM4253I	Compile-time	Processor	BC
IEM4254I	Compile-time	Processor	BC
TEM4 256 T	Compile-time	Processor	BC
10442501		2100003001	DC
1EM42591	Compile-time	Processor	BC
IEM4262I	Compile-time	Processor	BC
TEM4265T	Compile-time	Processor	BC
TEMU 071 T	Compile-time	Drogogor	DC
16042/11	compile-cime	Processor	BC
IEM4277I	Compile-time	Processor	BC
IEM4280I	Compile-time	Processor	BC
TEM/1283T	Compile-time	Processor	BC
10442001	compile cime	7100003001	DC
1EM42861	Compile-time	Processor	BC
IEM4289I	Compile-time	Processor	BC
IEM42921	Compile-time	Processor	BC
TEM/1205T	Compile-time	Drocessor	BC
IEM42931	compile cime	FICCESSOL	DC
1EM42961	Compile-time	processor	BC
IEM4298I	Compile-time	Processor	BC
TEM 4 2 9 9 T	Compile-time	Processor	BC
TEM 0 201 T	Compile time	Dreessor	na
IEM4 SULI	Comprise_true	PIOCessor	BC
IEM4304I			
IEM4307I	Compile-time	Processor	BC
	Compile-time Compile-time	Processor Processor	BC BC
TEMUSIOT	Compile-time Compile-time	Processor Processor Processor	BC BC BC
IEM4310I	Compile-time Compile-time Compile-time	Processor Processor Processor	BC BC BC
IEM4310I IEM4313I	Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor	BC BC BC BC
IEM4310I IEM4313I IEM4319I	Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor	BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322T	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325T	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4322I	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I IEM4331I	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I IEM4331I IEM43321	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I IEM43311 IEM43321	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I IEM4331I IEM43321 IEM4334I	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC
I EM4 310I IEM4 313I I EM4 319I IEM4 322I IEM4 325I IEM4 328I I EM4 331 I IEM4 3321 IEM4 334I IEM4 337I	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC BC BC BC
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I IEM43311 IEM43321 IEM4337I IEM4340T	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC BC BC BC B
IEM4310I IEM4313I IEM4319I IEM4322I IEM4325I IEM4328I IEM4331I IEM43321 IEM4337I IEM437I IEM4340I IEM4340I	Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time Compile-time	Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor Processor	BC BC BC BC BC BC BC BC BC BC BC BC BC B

1	IEM4346I	Compile-time	Processor	BC	
-	TEM4349T	Compile-time	Processor	BC	
-	TEM#352T	Compile-time	Processor	BC	
	10M/2551	Compile time	Drocessor	DC	
-	150433331	comprise-crime	Processor	DC	
-	LEM43581	Compile-time	Processor	BC	
-	IEM4361I	Compile-time	Prccessor	BC	
]	IEM4364I	Compile-time	Processor	BC	
1	IEM4367I	Compile-time	Prccessor	BC	
-	IEM4370I	Compile-time	Processor	BC	
-	TEM4373T	Compile-time	Drecessor	BC	
	TEMU376T	Compile time	Brocessor	DC	
-	LEM43701	Compile-time	Processor	DC	
-	LEM43/91	compile-time	Processor	BC	
-	IEM43821	Compile-time	Prccessor	BC	
]	IEM4283I	Compile-time	Processor	вс	
]	IEM4391I	Compile-time	Processor	BC	
]	IEM4394I	Compile-time	Processor	BC	
1	IEM4397I	Compile-time	Processor	BC	
	TEMULOOT	Comrile-time	Processor	BC	
		Compile-time	Brocossor	DC	
-		Compile-time	Processor	DC	
4	LEM44061	Compile-time	Processor	BC	
1	IEM4407I	Compile-time	Prccessor	BC	
]	IEM4409I	Compile-time	Processor	BC	
]	IEM4412I	Compile-time	Processor	BC	
1	IEM4415I	Compile-time	Processor	BC	
-	TEM4421 T	Compile-time	Processor	BC	
-	TFM/1/133T	Compile-time	Processor	BC	
-	TEMPHOLI	Compile-time	Drecessor	DG	
-	LEM44301	compile-time	Processor	BG	
-	LEM44391	Compile-time	processor	BG	
-	IEM4448I	Compile-time	Processor	BG	
1	IEM4451I	Compile-time	Prccessor	BG	
3	IEM4452I	Compile-time	Processor	BG	
1	IEM4454I	Compile-time	Processor	ВG	
-	ТЕМЦЦ57Т	Compile-time	Processor	BG	
-		Compile-time	Processor	PC	
	LEM44001	Compile time	Dreason	DG	
-	LEM440JL	Compile-cime	PICCessor	BG	
	1EM44691	Compile-time	Processor	BG	
]	IEM4472I	Compile-time	Processor	BG	
]	IEM4473I	Compile-time	Prccessor	BG	
2	IEM4475I	Compile-time	Processor	BG	
]	IEM4478I	Compile-time	Prccessor	BG	
	IEM4481I	Compile-time	Prccessor	BG	
-	TEMUU8UT	Compile-time	Processor	BG	
-	TEMUNGGT	Compile-time	Processor	BC	
-	TEMUSOOT	Compile time	Processor	DC	
-		Compile-time	Processor	DG	
	LEM45041	Compile-time	Processor	BG	
-	IEM4505I	Compile-time	Prccessor	BG	
3	IEM45061	Compile-time	Prccessor	ВG	
]	IEM4508I	Compile-time	Processor	BG	
1	IEM4511I	Compile-time	Processor	BC	
3	IEM4514I	Compile-time	Processor	BG	
]	IEM451 7 I	Compile-time	Processor	BG	
	TEM4520T	Compile-time	Processor	BG	
-	TEM/1523T	Compile_time	Brocessor	PC	
-		Compile time	Processor	DG	
_	LEM45261	compile-time	Processor	AS	_
]	IEM4529I	Compile-time	Prccessor	BC	BG
]	IEM4532I	Compile-time	Prccessor	AS	
]	IEM4535I	Compile-time	Processor	AS	
]	IEM4538I	Compile-time	Processor	BC	
1	IEM4547I	Compile-time	Processor	AV	
-	TEM4550T	Compile-time	Processor	BG	
1	TEM4552T	Compile-time	Droceecor	BC	
-		Compile-time	Droccasor	50	
-	L 15174 3 3 7 1 T 1514 5 4 3 7 1	Comprise-time	Processor	DG DC	
1	15142021	compile-time	riocessor	BG	
]	LEM45/0I	compile-time	Processor	BG	
3	IEM4572I	Compile-time	Processor	BG	
]	IEM4574I	Compile-time	Processor	BG	
]	IEM4576I	Compile-time	Processor	BG	
-		-			

IEM4578I	Compile-time	Processor	BG
IEM4580I	Compile-time	Processor	BG

Any initial value statements associated with the ALLOCATE statement are extracted and placed in-line. The initialization statements are then skipped, and the scan continues.

The last two steps are also performed for LOCATE (based variable) and ALLOCATE (based variable) statements.

The action on encountering a BUY statement is similar to that for the ALLOCATE statement, with the following exceptions:

- Bound and string length code is inline, bracketed between BUYS and BUY statements - there is therefore no lcok ahead
- 2. There is no initial value code associated with temporaries
- 3. A slot in the DSA is updated with the pointer to the allocated storage for a temporary

The action on encountering a FREE statement is to generate code to load a parameter register with the pointer to the allocated storage for the FREE VDA Library call inserted by the pseudo-code.

Phase QU

Phase QU scans the pseudo-code text in search of instructions which have misaligned operands. (A misaligned operand has the UNALIGNED attribute and is not aligned on the boundary appropriate to its data When such an instruction is found, type). QU inserts a move character (MVC) instruction in the pseudo-code text to move the operand to or from an aligned workspace area, and substitutes the address of this workspace for the operand address in the original instruction. If the address of a misaligned operand is loaded into a register, a note is made of that register. QU thereafter treats the instructions which refer to it as if they referred to the operand itself, by inserting a move character instruction, and substituting the workspace address for the reference in the instruction.

Phase QU uses storage beginning at offset 32 from register 9 for its workspace.

Whenever a load address (LA) instruction is found which lies within the calling sequence of a library routine and which loads the address of a misaligned argument of that routine, an aligned workspace address is substituted in the instruction, and the requisite move character instruction is stacked. It is not inserted in the output text until the instruction is encountered that loads register 15 prior to the exit to the library routine, or in the case of EDIT-directed I/O routines, until the appropriate branch-and-link (BALR) instruction is encountered. The stacked move character instruction is inserted into the output before the exit to the routine if the argument in question is an input argument to the routine, and after the return from the routine if it is an output argument.

Phase QX

Phase QX is the 'AGGREGATE LENGTH TABLE' printing phase. It is entered only if the ATR (attribute list) option is specified. It scans the STATIC, AUTOMATIC, CONTROLLED and COBOL chains, and, for each major structure or non-structured array that is found, an entry is printed in the AGGREGATE length table.

An AGGREGATE LENGTH TABLE entry consists of the source program DECLARE statement number, the identifier and the length (in bytes) of the aggregate. In the case of an aggregate with the CONTROLLED attribute, no entry is printed for the DECLARE statement, but an entry is printed for each ALLOCATE for the aggregate, the source program ALLO-CATE statement number being printed in the 'statement number' column.

Where the aggregate length is not known at compilation the word "adjustable" is printed in the 'length in bytes' column. In the case of a DEFINED aggregate, the word 'DEFINED', and not the aggregate length, appears in the 'length in bytes' column.

Before printing begins the aggregate length table entries are sorted so that the identifiers appear in collating sequence order.

THE REGISTER ALLOCATION LOGICAL PHASE

The purpose of the Register Allocation Phase is to insert into the text the appropriate addressing mechanisms for all types of storage, and to allocate physical general registers where symbolic registers are specified or required as base registers.

This phase comprises two physical phases, each with a specific function. The first, Phase RA, processes the addressing mechanisms, while the second phase, Phase RF, allocates the physical registers.