IBM System/360 Reference Data

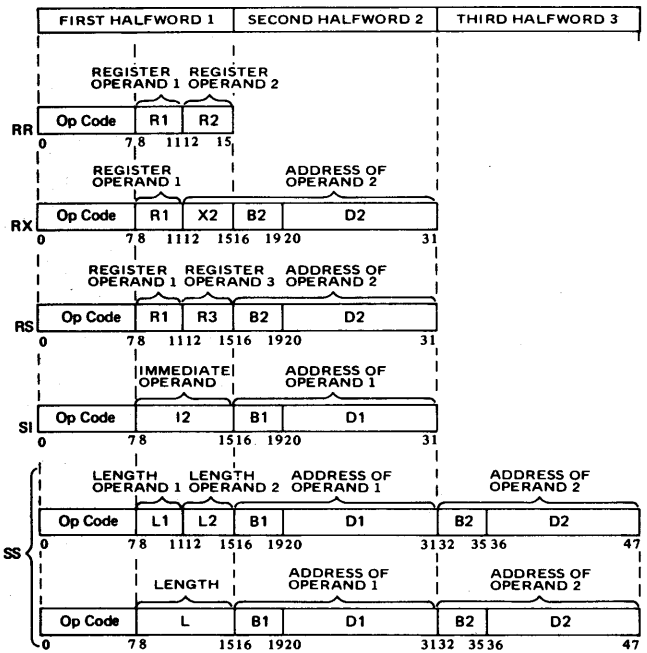
MACHINE INSTRUCTIONS

NAME	MNEMONIC	OP CODE	FOR-MAT	OPERANDS
Add (c)	AR	1A	RR	R1,R2
Add (c)	A	5A	RX	R1,D2(X2,B2)
Add Decimal (c,d)	AP	FA	SS	D1(L1,B1),D2(L2,B2)
Add Halfword (c)	AH	4A	RX	R1,D2(X2,B2)
Add Logical (c)	ALR	1E	RR	R1,R2
Add Logical (c)	AL	5E	RX	R1,D2(X2,B2)
AND (c)	NR	14	RR	R1,R2
AND (c)	N	54	RX	R1,D2(X2,B2)
AND (c)	NI	94	SI	D1(B1),I2
AND (c)	NC	D4	SS	D1(L,B1),D2(B2)
Branch and Link	BALR	05	RR	R1,R2
Branch and Link	BAL	45	RX	R1,D2(X2,B2)
Branch and Store (e)	BASR	0D	RR	R1,R2
Branch and Store (e)	BAS	4D	RX	R1,D2(X2,B2)
Branch on Condition	BCR	07	RR	M1,R2
Branch on Condition	BC	47	RX	M1,D2(X2,B2)
Branch on Count	BCTR	06	RR	R1,R2
Branch on Count	BCT	46	RX	R1,D2(X2,B2)
Branch on Index High	BXH	86	RS	R1,R3,D2(B2)
Branch on Index Low or Equal	BXLE	87	RS	R1,R3,D2(B2)
Compare (c)	CR	19	RR	R1,R2
Compare (c)	C	59	RX	R1,D2(X2,B2)
Compare Decimal (c,d)	CP	F9	SS	D1(L1,B1),D2(L2,B2)
Compare Halfword (c)	CH	49	RX	R1,D2(X2,B2)
Compare Logical (c)	CLR	15	RR	R1,R2
Compare Logical (c)	CL	55	RX	R1,D2(X2,B2)
Compare Logical (c)	CLC	D5	SS	D1(L,B1),D2(B2)
Compare Logical (c)	CLI	95	SI	D1(B1),I2
Convert to Binary	CVB	4F	RX	R1,D2(X2,B2)
Convert to Decimal	CVD	4E	RX	R1,D2(X2,B2)
Diagnose (p)		83	SI	
Divide	DR	1D	RR	R1,R2
Divide	D	5D	RX	R1,D2(X2,B2)
Divide Decimal (d)	DP	FD	SS	D1(L1,B1),D2(L2,B2)
Edit (c,d)	ED	DE	SS	D1(L,B1),D2(B2)
Edit and Mark (c,d)	EDMK	DF	SS	D1(L,B1),D2(B2)
Exclusive OR (c)	XR	17	RR	R1,R2
Exclusive OR (c)	X	57	RX	R1,D2(X2,B2)
Exclusive OR (c)	XI	97	SI	D1(B1),I2
Exclusive OR (c)	XC	D7	SS	D1(L,B1),D2(B2)
Execute	EX	44	RX	R1,D2(X2,B2)
Halt I/O (c,p)	HIO	9E	SI	D1(B1)
Insert Character	IC	43	RX	R1,D2(X2,B2)
Insert Storage Key (a,p)	ISK	09	RR	R1,R2
Load	LR	18	RR	R1,R2
Load	L	58	RX	R1,D2(X2,B2)
Load Address	LA	41	RX	R1,D2(X2,B2)
Load and Test (c)	LTR	12	RR	R1,R2
Load Complement (c)	LCR	13	RR	R1,R2
Load Halfword	LH	48	RX	R1,D2(X2,B2)
Load Multiple	LM	98	RS	R1,R3,D2(B2)
Load Multiple Control (e,p)	LMC	B8	RS	R1,R3,D2(B2)
Load Negative (c)	LNR	11	RR	R1,R2
Load Positive (c)	LPR	10	RR	R1,R2
Load PSW (n,p)	LPSW	82	SI	D1(B1)
Load Real Address (c,e,p)	LRA	B1	RX	R1,D2(X2,B2)
Move	MVI	92	SI	D1(B1),I2
Move	MVC	D2	SS	D1(L,B1),D2(B2)
Move Numerics	MVN	D1	SS	D1(L,B1),D2(B2)
Move with Offset	MVO	F1	SS	D1(L1,B1),D2(L2,B2)
Move Zones	MVZ	D3	SS	D1(L,B1),D2(B2)
Multiply	MR	1C	RR	R1,R2
Multiply	M	5C	RX	R1,D2(X2,B2)
Multiply Decimal (d)	MP	FC	SS	D1(L1,B1),D2(L2,B2)
Multiply Halfword	MH	4C	RX	R1,D2(X2,B2)
OR (c)	OR	16	RR	R1,R2
OR (c)	O	56	RX	R1,D2(X2,B2)
OR (c)	OI	96	SI	D1(B1),I2
OR (c)	OC	D6	SS	D1(L,B1),D2(B2)
Pack	PACK	F2	SS	D1(L1,B1),D2(L2,B2)
Read Direct (b,p)	RDD	85	SI	D1(B1),I2
Set Program Mask (n)	SPM	04	RR	R1
Set Storage Key (a,p)	SSK	08	RR	R1,R2
Set System Mask (p)	SSM	80	SI	D1(B1)
Shift Left Double (c)	SLDA	8F	RS	R1,D2(B2)
Shift Left Double Logical	SLDL	8D	RS	R1,D2(B2)
Shift Left Single (c)	SLA	8B	RS	R1,D2(B2)
Shift Left Single Logical	SLL	89	RS	R1,D2(B2)
Shift Right Double (c)	SRDA	8E	RS	R1,D2(B2)
Shift Right Double Logical	SRDL	8C	RS	R1,D2(B2)
Shift Right Single (c)	SRA	8A	RS	R1,D2(B2)
Shift Right Single Logical	SRL	88	RS	R1,D2(B2)
Start I/O (c,p)	SIO	9C	SI	D1(B1)
Store	ST	50	RX	R1,D2(X2,B2)
Store Character	STC	42	RX	R1,D2(X2,B2)
Store Halfword	STH	40	RX	R1,D2(X2,B2)
Store Multiple	STM	90	RS	R1,R3,D2(B2)
Store Multiple Control (e,p)	STMC	B0	RS	R1,R3,D2(B2)
Subtract (c)	SR	1B	RR	R1,R2
Subtract (c)	S	5B	RX	R1,D2(X2,B2)
Subtract Decimal (c,d)	SP	FB	SS	D1(L1,B1),D2(L2,B2)
Subtract Halfword (c)	SH	4B	RX	R1,D2(X2,B2)
Subtract Logical (c)	SLR	1F	RR	R1,R2
Subtract Logical (c)	SL	5F	RX	R1,D2(X2,B2)
Supervisor Call	SVC	0A	RR	I
Test and Set (c)	TS	93	SI	D1(B1)
Test Channel (c,p)	TCH	9F	SI	D1(B1)
Test I/O (c,p)	TIO	9D	SI	D1(B1)
Test under Mask (c)	TM	91	SI	D1(B1),I2
Translate	TR	DC	SS	D1(L,B1),D2(B2)
Translate and Test (c)	TRT	DD	SS	D1(L,B1),D2(B2)
Unpack	UNPK	F3	SS	D1(L1,B1),D2(L2,B2)
Write Direct (b,p)	WRD	84	SI	D1(B1),I2
Zero and Add (c,d)	ZAP	F8	SS	D1(L1,B1),D2(L2,B2)

NOTES FOR PANELS 1-3

a. Protection feature
b. Direct control feature
c. Condition code is set
d. Decimal feature
e. Model 67
n. New condition
p. Privileged instruction
x. Extended precision floating point feature

MACHINE FORMATS



FLOATING-POINT FEATURE INSTRUCTIONS

Add Normalized, Extended (c,x)	AXR	36	RR	R1,R2
Add Normalized, Long (c)	ADR	2A	RR	R1,R2
Add Normalized, Long (c)	AD	6A	RX	R1,D2(X2,B2)
Add Normalized, Short (c)	AER	3A	RR	R1,R2
Add Normalized, Short (c)	AE	7A	RX	R1,D2(X2,B2)
Add Unnormalized, Long (c)	AWR	2E	RR	R1,R2
Add Unnormalized, Long (c)	AW	6E	RX	R1,D2(X2,B2)
Add Unnormalized, Short (c)	AUR	3E	RR	R1,R2
Add Unnormalized, Short (c)	AU	7E	RX	R1,D2(X2,B2)
Compare, Long (c)	CDR	29	RR	R1,R2
Compare, Long (c)	CD	69	RX	R1,D2(X2,B2)
Compare, Short (c)	CER	39	RR	R1,R2
Compare, Short (c)	CE	79	RX	R1,D2(X2,B2)
Divide, Long	DDR	2D	RR	R1,R2
Divide, Long	DD	6D	RX	R1,D2(X2,B2)
Divide, Short	DER	3D	RR	R1,R2
Divide, Short	DE	7D	RX	R1,D2(X2,B2)
Halve, Long	HDR	24	RR	R1,R2
Halve, Short	HER	34	RR	R1,R2
Load and Test, Long (c)	LTDR	22	RR	R1,R2
Load and Test, Short (c)	LTER	32	RR	R1,R2
Load Complement, Long (c)	LCDR	23	RR	R1,R2
Load Complement, Short (c)	LCER	33	RR	R1,R2
Load, Long	LDR	28	RR	R1,R2
Load, Long	LD	68	RX	R1,D2(X2,B2)
Load Negative, Long (c)	LNDR	21	RR	R1,R2
Load Negative, Short (c)	LNER	31	RR	R1,R2
Load Positive, Long (c)	LPDR	20	RR	R1,R2
Load Positive, Short (c)	LPER	30	RR	R1,R2
Load Rounded, Extended to Long (x)	LRDR	25	RR	R1,R2
Load Rounded, Long to Short (x)	LRER	35	RR	R1,R2
Load, Short	LER	38	RR	R1,R2
Load, Short	LE	78	RX	R1,D2(X2,B2)
Multiply, Extended (x)	MXR	26	RR	R1,R2
Multiply, Long	MDR	2C	RR	R1,R2
Multiply, Long	MD	6C	RX	R1,D2(X2,B2)
Multiply, Long/Extended (x)	MXDR	27	RR	R1,R2
Multiply, Long/Extended (x)	MXD	67	RX	R1,D2(X2,B2)
Multiply, Short	MER	3C	RR	R1,R2
Multiply, Short	ME	7C	RX	R1,D2(X2,B2)
Store, Long	STD	60	RX	R1,D2(X2,B2)
Store, Short	STE	70	RX	R1,D2(X2,B2)
Subtract Normalized, Extended (c,x)	SXR	37	RR	R1,R2
Subtract Normalized, Long (c)	SDR	2B	RR	R1,R2
Subtract Normalized, Long (c)	SD	6B	RX	R1,D2(X2,B2)
Subtract Normalized, Short (c)	SER	3B	RR	R1,R2
Subtract Normalized, Short (c)	SE	7B	RX	R1,D2(X2,B2)
Subtract Unnormalized, Long (c)	SWR	2F	RR	R1,R2
Subtract Unnormalized, Long (c)	SW	6F	RX	R1,D2(X2,B2)
Subtract Unnormalized, Short (c)	SUR	3F	RR	R1,R2
Subtract Unnormalized, Short (c)	SU	7F	RX	R1,D2(X2,B2)

NOTES

EXTENDED MNEMONIC INSTRUCTION CODES

GENERAL

Extended Code		Machine Instruction		Meaning
B	D2(X2,B2)	BC 15,	D2(X2,B2)	Branch Unconditionally
BR	R2	BCR 15,	R2	Branch Unconditionally
NOP	D2(X2,B2)	BC 0,	D2(X2,B2)	No Operation
NOPR	R2	BCR 0,	R2	No Operation (RR)

AFTER COMPARE INSTRUCTIONS (A:B)

BH	D2(X2,B2)	BC 2,	D2(X2,B2)	Branch on A High
BL	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch on A Low
BE	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch on A Equal B
BNH	D2(X2,B2)	BC 13,	D2(X2,B2)	Branch on A Not High
BNL	D2(X2,B2)	BC 11,	D2(X2,B2)	Branch on A Not Low
BNE	D2(X2,B2)	BC 7,	D2(X2,B2)	Branch on A Not Equal B

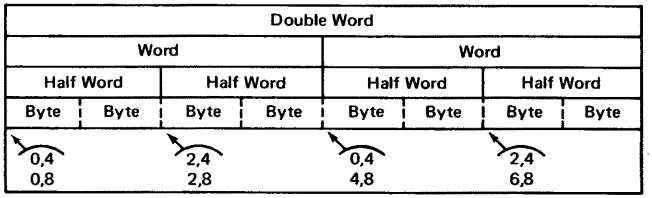
AFTER ARITHMETIC INSTRUCTIONS

BO	D2(X2,B2)	BC 1,	D2(X2,B2)	Branch on Overflow
BP	D2(X2,B2)	BC 2,	D2(X2,B2)	Branch on Plus
BM	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch on Minus
BZ	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch on Zero
BNP	D2(X2,B2)	BC 13,	D2(X2,B2)	Branch on Not Plus
BNM	D2(X2,B2)	BC 11,	D2(X2,B2)	Branch on Not Minus
BNZ	D2(X2,B2)	BC 7,	D2(X2,B2)	Branch on Not Zero

AFTER TEST UNDER MASK INSTRUCTIONS

BO	D2(X2,B2)	BC 1,	D2(X2,B2)	Branch if Ones
BM	D2(X2,B2)	BC 4,	D2(X2,B2)	Branch if Mixed
BZ	D2(X2,B2)	BC 8,	D2(X2,B2)	Branch if Zeros
BNO	D2(X2,B2)	BC 14,	D2(X2,B2)	Branch if Not Ones

CNOP ALIGNMENT



EDIT AND EDMK PATTERN CHARACTERS (in hex)

20–digit selector	40–blank	5C--asterisk
21–start of significance	4B--period	6B--comma
22–field separator	5B--dollar sign	C3D9--CR

SUMMARY OF CONSTANTS (OS and DOS Assemblers)

TYPE	IMPLIED LENGTH, BYTES	ALIGNMENT	FORMAT	TRUNCATION/ PADDING
C	–	byte	characters	right
X	–	byte	hexadecimal digits	left
B	–	byte	binary digits	left
F	4	word	fixed-point binary	left
H	2	halfword	fixed-point binary	left
E	4	word	short floating-point	right
D	8	doubleword	long floating-point	right
L	16	doubleword	extended floating-point	right
P	–	byte	packed decimal	left
Z	–	byte	zoned decimal	left
A	4	word	value of address	left
Y	2	halfword	value of address	left
S	2	halfword	address in base-displacement form	–
V	4	word	externally defined address value	left
Q*	4	word	symbol naming a DXD or DSECT	left

*OS only

ASSEMBLER INSTRUCTIONS

Source: GC24-3414 for DOS
GC28-6514 for OS

Function	Mnemonic	Meaning
Data definition	DC	Define constant
	DS	Define storage
	CCW	Define channel command word
Program sectioning and linking	START	Start assembly
	CSECT	Identify control section
	DSECT	Identify dummy section
	DXD*	Define external dummy section
	CXD*	Cumulative length of external dummy section
	COM	Identify blank common control section
	ENTRY	Identify entry-point symbol
	EXTRN	Identify external symbol
	WXTRN	Identify weak external symbol
Base register assignment	USING	Use base address register
	DROP	Drop base address register
Control of listings	TITLE	Identify assembly output
	EJECT	Start new page
	SPACE	Space listing
	PRINT	Print optional data
Program control	ICTL	Input format control
	ISEQ	Input sequence checking
	PUNCH	Punch a card
	REPRO	Reproduce following card
	ORG	Set location counter
	EQU	Equate symbol
	OPSYN*	Equate operation code
	LTORG	Begin literal pool
	CNOP	Conditional no operation
	COPY	Copy predefined source coding
	END	End assembly
Macro definition	MACRO	Macro definition header
	MNOTE	Request for error message
	MEXIT	Macro definition exit
	MEND	Macro definition trailer
Conditional assembly	ACTR	Conditional assembly loop counter
	AGO	Unconditional branch
	AIF	Conditional branch
	ANOP	Assembly no operation
	GBLA	Define global SETA symbol
	GBLB	Define global SETB symbol
	GBLC	Define global SETC symbol
	LCLA	Define local SETA symbol
	LCLB	Define local SETB symbol
	LCLC	Define local SETC symbol
	SETA	Set arithmetic variable symbol
	SETB	Set binary variable symbol
	SETC	Set character variable symbol

*OS only

CONDITION CODES

Condition Code Setting	0	1	2	3
Mask Bit Position	8	4	2	1
Floating-Point Arithmetic				
Add Normalized S/L/E	zero	<zero	>zero	–
Add Unnormalized S/L	zero	<zero	>zero	–
Compare S/L (A:B)	equal	A low	A high	–
Load and Test S/L	zero	<zero	>zero	–
Load Complement S/L	zero	<zero	>zero	–
Load Negative S/L	zero	<zero	–	–
Load Positive S/L	zero	–	>zero	–
Subtract Normalized S/L/E	zero	<zero	>zero	–
Subtract Unnormalized S/L	zero	<zero	>zero	–
Fixed-Point and Decimal Arithmetic				
Add H/F/Dec.	zero	<zero	>zero	overflow
Add Logical	zero, no carry	not zero, no carry	zero, carry	not zero, carry
Compare H/F/Dec. (A:B)	equal	A low	A high	–
Load and Test	zero	<zero	>zero	–
Load Complement	zero	<zero	>zero	overflow
Load Negative	zero	<zero	–	–
Load Positive	zero	–	>zero	overflow
Shift Left Single/Double	zero	<zero	>zero	overflow
Shift Right Single/Double	zero	<zero	>zero	–
Subtract H/F/Dec.	zero	<zero	>zero	overflow
Subtract Logical	–	not zero, no carry	zero, carry	not zero, carry
Zero and Add	zero	<zero	>zero	overflow
Logical Operations				
AND	zero	not zero	–	–
Compare Logical (A:B)	equal	A low	A high	–
Edit	zero	<zero	>zero	–
Edit and Mark	zero	<zero	>zero	–
Exclusive OR	zero	not zero	–	–
OR	zero	not zero	–	–
Test under Mask	zero	mixed	–	one
Translate and Test	zero	incomplete	complete	–
Input/Output Operations				
Halt I/O	interruption pending	CSW stored	halted	not oper
Start I/O	started	CSW stored	busy	not oper
Test I/O	available	CSW stored	busy	not oper
Test Channel	available	interruption pending	burst mode	not oper
Miscellaneous Operations				
Test and Set	zero	one	–	–
Load Real Address (Mod. 67)	successful	segment unavailable	page unavailable	–

NOTES

CODES FOR PROGRAM INTERRUPTION

Interruption Code		Program Interruption Cause	Interruption Code		Program Interruption Cause
Dec	Hex		Dec	Hex	
1	0001	Operation	10	000A	Decimal overflow
2	0002	Privileged operation	11	000B	Decimal divide
3	0003	Execute	12	000C	Exponent overflow
4	0004	Protection	13	000D	Exponent underflow
5	0005	Addressing	14	000E	Significance
6	0006	Specification	15	000F	Floating-point divide
7	0007	Data	16*	0010	Segment translation
8	0008	Fixed-point overflow	17*	0011	Page translation
9	0009	Fixed-point divide			

*Model 67

HEXADECIMAL AND DECIMAL CONVERSION

From hex: locate each hex digit in its corresponding column position and note the decimal equivalents. Add these to obtain the decimal value.

From decimal: (1) locate the largest decimal value in the table that will fit into the decimal number to be converted, and (2) note its hex equivalent and hex column position. (3) Find the decimal remainder. Repeat the process on this and subsequent remainders.

Note: Decimal, hexadecimal, (and binary) equivalents of all numbers from 0 to 255 are listed on panels 11-14.

HEXADECIMAL COLUMNS											
6		5		4		3		2		1	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
0123		4567		0123		4567		0123		4567	
BYTE				BYTE				BYTE			

POWERS OF 2

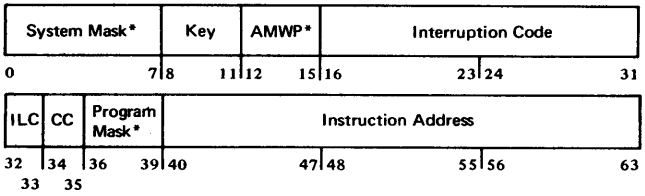
2^n	n
256	8
512	9
1 024	10
2 048	11
4 096	12
8 192	13
16 384	14
32 768	15
65 536	16
131 072	17
262 144	18
524 288	19
1 048 576	20
2 097 152	21
4 194 304	22
8 388 608	23
16 777 216	24

$2^0 = 16^0$
$2^4 = 16^1$
$2^8 = 16^2$
$2^{12} = 16^3$
$2^{16} = 16^4$
$2^{20} = 16^5$
$2^{24} = 16^6$
$2^{28} = 16^7$
$2^{32} = 16^8$
$2^{36} = 16^9$
$2^{40} = 16^{10}$
$2^{44} = 16^{11}$
$2^{48} = 16^{12}$
$2^{52} = 16^{13}$
$2^{56} = 16^{14}$
$2^{60} = 16^{15}$

POWERS OF 16

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

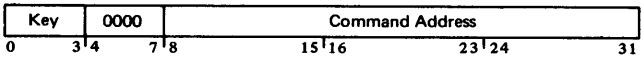
PROGRAM STATUS WORD



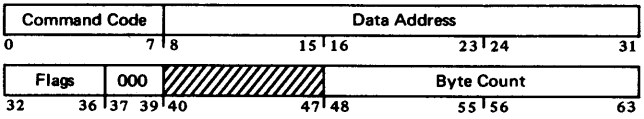
0 Channel 0 mask
1 Channel 1 mask
2 Channel 2 mask
3 Channel 3 mask
4 Channel 4 mask
5 Channel 5 mask
6 Mask for channel 6 and up
7 External mask
12 ASCII-8 mode (A)
13 Machine check mask (M)
14 Wait state (W)
15 Problem state (P)
32-33 Instruction length code (ILC)
34-35 Condition code (CC)
36 Fixed-point overflow mask
37 Decimal overflow mask
38 Exponent underflow mask
39 Significance mask

*A one-bit equals on, and permits an interrupt.

CHANNEL ADDRESS WORD

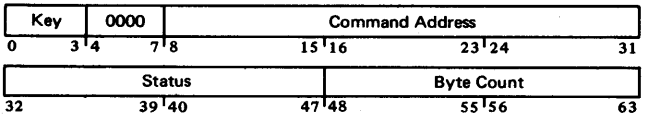


CHANNEL COMMAND WORD



CD—bit 32 (80) causes use of address portion of next CCW.
CC—bit 33 (40) causes use of command code and data address of next CCW.
SLI—bit 34 (20) causes suppression of possible incorrect length indication.
Skip—bit 35 (10) suppresses transfer of information to main storage.
PCI—bit 36 (08) causes a channel Program Controlled Interruption.

CHANNEL STATUS WORD



32 (8000) Attention
33 (4000) Status modifier
34 (2000) Control unit end
35 (1000) Busy
36 (0800) Channel end
37 (0400) Device end
38 (0200) Unit check
39 (0100) Unit exception
40 (0080) Program-controlled interruption
41 (0040) Incorrect length
42 (0020) Program check
43 (0010) Protection check
44 (0008) Channel data check
45 (0004) Channel control check
46 (0002) Interface control check
47 (0001) Chaining check

Byte Count: bits 48-63 form the residual count for the last CCW used.

Comments about this card may be sent to the Technical Publications Department at the White Plains address below. All comments and suggestions become the property of IBM.

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International Business Machines Corporation
Data Processing Division
1133 Westchester Ave., White Plains, N.Y. 10604
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IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
(International)

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PERMANENT STORAGE ASSIGNMENTS

Dec	Hex	Length	Purpose
0	0	double word	Initial program loading PSW
8	8	double word	Initial program loading CCW1
16	10	double word	Initial program loading CCW2
24	18	double word	External old PSW
32	20	double word	Supervisor Call old PSW
40	28	double word	Program old PSW
48	30	double word	Machine-check old PSW
56	38	double word	Input/output old PSW
64	40	double word	Channel status word
72	48	word	Channel address word
76	4C	word	Unused
80	50	word	Timer (uses bytes 50, 51 & 52)
84	54	word	Unused
88	58	double word	External new PSW
96	60	double word	Supervisor Call new PSW
104	68	double word	Program new PSW
112	70	double word	Machine-check new PSW
120	78	double word	Input/output new PSW
128	80	(1)	Diagnostic scan-out area

(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

CHANNEL COMMANDS

2314, 2311/2321 DASD

Source: GA26-3599, GA26-5988

Command for CCW‡		Count	MT Off	MT On†
Control	Seek	6	07	
	Seek Cylinder	6	0B	
	Seek Head	6	1B	
	Set File Mask	1	1F	
	Space Count	3	0F	
	Recalibrate (Note 1)	Not zero	13	
	Restore (2321 only)	Not zero	17	
Sense	Sense I/O	6	04	
	Release Device (Note 2)	6	94	
	Reserve Device (Note 2)	6	B4	
Search	Home Address EQ	4 (usually)	39	B9
	Identifier EQ	5 (usually)	31	B1
	Identifier HI	5 (usually)	51	D1
	Identifier EQ or HI	5 (usually)	71	F1
	Key EQ	1 to 255	29	A9
	Key HI	1 to 255	49	C9
	Key EQ or HI	1 to 255	69	E9
	Key & Data EQ	Number of bytes in search argument, including mask bytes. (Special feature.)	2D	AD
	Key & Data HI		4D	CD
	Key & Data EQ or HI		6D	ED
Continue Scan	Search EQ		25	A5
	Search HI		45	C5
	Search HI or EQ		65	E5
	Set Status Modifier*		35	B5
	Set Status Modifier*		75	F5
	No Status Modifier		55	D5
Read	Home Address	5	1A	9A
	Count	8	12	92
	Record 0		16	96
	Data	Number of bytes transferred	06	86
	Key & Data		0E	8E
	Count, Key & Data		1E	9E
	IPL		02	
Write	Home Address	5 (usually)	19	
	Record 0	8+KL+DL of R0	15	
	Count, Key & Data	8+KL+DL	1D	
	Special Count, Key & Data	8+KL+DL	01	
	Data	DL	05	
	Key & Data	KL+DL	0D	
	Erase	8+KL+DL	11	

1. For 2311 or 2314 only.
2. Two-channel switch required except for a 2314/2844 combination.

*Sense byte determines command used.
†Code same as MT Off except as listed.
‡See also standard commands, panel 10.

CHANNEL COMMANDS (Contd)

Standard Command Code Assignments (CCW bits 0-7) for I/O Operations

xxxx 0000	Invalid	†††† ††01	Write
†††† 0100	Sense	†††† ††10	Read
xxxx 1000	Transfer in Channel	†††† ††11	Control
†††† 1100	Read Backward	0000 0011	Control No Operation

x—Bit ignored. †Modifier bit for specific type of I/O device

1052 CONSOLE

Source: GA22-6877

Read Inquiry BCD	0A	Sense	04
Write BCD, Auto Carrier Return	09	Alarm	0B
Write BCD, No Carrier Return	01		

2540 CARD READ PUNCH

Source: GA24-3312

Command	Type	Code
Read, Feed, Select Stacker	AA	SSD0 0010
Read	AB	11D0 0010
Read, Feed (1400 Compatibility*)	–	11D1 0010
Feed, Select Stacker	BA	SS10 0011
PFR* Write, Feed, Select Stacker	BA	SSD0 1001
Write, Feed, Select Stacker	BB	SSD0 0001
Sense	–	0000 0100

Bit	Meanings
SS	Stacker
00	R1 or P1
01	R2 or P2
10	RP3
D	Data Mode
0	1-EBCDIC
1	2-Col. binary*

1442-N1 CARD READ PUNCH

Source: GA21-9025

Write	01	Read	02
Write, Select Stacker 2	41	Read, Select Stacker 2	42
Write, Feed	81	Read Card Image	22
Write, Feed, Select Stacker 2	C1	Read Card Image, Sel Stkr 2	62
Write Card Image*	21	Read 1442 Compatibility*	12
Write Card Image, Sel Stkr 2	61	Read 1442 Compat, Sel Stkr 2	52
Write Card Image, Feed	A1	Control Feed	83
Write Card Image, Feed, Sel Stkr 2	E1	Control Feed, Select Stkr 2	C3
Sense	04	Control Select Stacker 2	43

1403, 1443 PRINTERS

Source: GA24-3312, GA24-3120

	After Write	Immed
Skip to Channel 1	89	8B
Skip to Channel 2	91	93
Skip to Channel 3	99	9B
Skip to Channel 4	A1	A3
Skip to Channel 5	A9	AB
Skip to Channel 6	B1	B3
Skip to Channel 7	B9	BB
Skip to Channel 8	C1	C3
Skip to Channel 9	C9	CB
Skip to Channel 10	D1	D3
Skip to Channel 11	D9	DB
Skip to Channel 12	E1	E3

1403 only	Diagnostic Data Read	02
	Diagnostic Check Read	06
	UCS Gate*	EB
	UCS Load (No Folding)*	FB
	UCS Load (Folding)*	F3
	Block Data Check*	73
	Reset Block Data Check*	7B
Write without Spacing		01
Sense		04

	After Write	Immed
Space 1 Line	09	0B
Space 2 Lines	11	13
Space 3 Lines	19	1B

2400-SERIES MAGNETIC TAPE

Note: Refer to GA22-6866 for operation of specific models, special features required, mode resets, and precedence of commands.

		Density	Parity	DC	Trans	Cmd
Sense	04	Set Mode 1 (7-track)				
Read Backward	0C					
Write	01	200	odd	on	off	13
Read	02			off	off	33
Rewind (REW)	07				on	3B
Rewind-Unload (RUN)	0F		even	off	off	23
Erase Gap (ERG)	17				on	2B
Write Tape Mark (WTM)	1F	556	odd	on	off	53
Backspace Block (BSB)	27			off	off	73
Backspace File (BSF)	2F				on	7B
Forward Space Block (FSB)	37		even	off	off	63
Forward Space File (FSF)	3F				on	6B
Request Track in Error (TIE)	1B	800	odd	on	off	93
Diagnostic Mode Set	0B			off	off	B3
Set Mode 2 (9-track), 1600 bpi	C3				on	BB
Set Mode 2 (9-track), 800 bpi	CB		even	off	off	A3
					on	AB

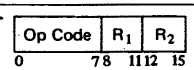
*Special feature required.

Decimal	Hexadecimal	Instruction Mnemonic (RR Format)	Graphic & Control Symbols (5) BCDIC	Graphic & Control Symbols (5) EBCDIC	7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code
0	00			NUL		12-0-1-8-9	0000 0000
1	01			SOH		12-1-9	0000 0001
2	02			STX		12-2-9	0000 0010
3	03			ETX		12-3-9	0000 0011
4	04	SPM		PF		12-4-9	0000 0100
5	05	BALR		HT		12-5-9	0000 0101
6	06	BCTR		LC		12-6-9	0000 0110
7	07	BCR		DEL		12-7-9	0000 0111
8	08	SSK				12-8-9	0000 1000
9	09	ISK				12-1-8-9	0000 1001
10	0A	SVC		SMM		12-2-8-9	0000 1010
11	0B			VT		12-3-8-9	0000 1011
12	0C			FF		12-4-8-9	0000 1100
13	0D	BASR (4)		CR		12-5-8-9	0000 1101
14	0E			SO		12-6-8-9	0000 1110
15	0F			SI		12-7-8-9	0000 1111
16	10	LPR		DLE		12-11-1-8-9	0001 0000
17	11	LNR		DC1		11-1-9	0001 0001
18	12	LTR		DC2		11-2-9	0001 0010
19	13	LCR		TM		11-3-9	0001 0011
20	14	NR		RES		11-4-9	0001 0100
21	15	CLR		NL		11-5-9	0001 0101
22	16	OR		BS		11-6-9	0001 0110
23	17	XR		IL		11-7-9	0001 0111
24	18	LR		CAN		11-8-9	0001 1000
25	19	CR		EM		11-1-8-9	0001 1001
26	1A	AR		CC		11-2-8-9	0001 1010
27	1B	SR		CU1		11-3-8-9	0001 1011
28	1C	MR		IFS		11-4-8-9	0001 1100
29	1D	DR		IGS		11-5-8-9	0001 1101
30	1E	ALR		IRS		11-6-8-9	0001 1110
31	1F	SLR		IUS		11-7-8-9	0001 1111
32	20	LPDR		DS		11-0-1-8-9	0010 0000
33	21	LNDR		SOS		0-1-9	0010 0001
34	22	LTDR		FS		0-2-9	0010 0010
35	23	LCDR				0-3-9	0010 0011
36	24	HDR		BYP		0-4-9	0010 0100
37	25	LRDR		LF		0-5-9	0010 0101
38	26	MXR		ETB		0-6-9	0010 0110
39	27	MXDR		ESC		0-7-9	0010 0111
40	28	LDR				0-8-9	0010 1000
41	29	CDR				0-1-8-9	0010 1001
42	2A	ADR		SM		0-2-8-9	0010 1010
43	2B	SDR		CU2		0-3-8-9	0010 1011
44	2C	MDR				0-4-8-9	0010 1100
45	2D	DDR		ENQ		0-5-8-9	0010 1101
46	2E	AWR		ACK		0-6-8-9	0010 1110
47	2F	SWR		BEL		0-7-8-9	0010 1111
48	30	LPER				12-11-0-1-8-9	0011 0000
49	31	LNER				1-9	0011 0001
50	32	LTER		SYN		2-9	0011 0010
51	33	LCER				3-9	0011 0011
52	34	HER		PN		4-9	0011 0100
53	35	LRER		RS		5-9	0011 0101
54	36	AXR		UC		6-9	0011 0110
55	37	SXR		EOT		7-9	0011 0111
56	38	LER				8-9	0011 1000
57	39	CER				1-8-9	0011 1001
58	3A	AER				2-8-9	0011 1010
59	3B	SER		CU3		3-8-9	0011 1011
60	3C	MER		DC4		4-8-9	0011 1100
61	3D	DER		NAK		5-8-9	0011 1101
62	3E	AUR				6-8-9	0011 1110
63	3F	SUR		SUB		7-8-9	0011 1111

NOTES FOR PANELS 11-14

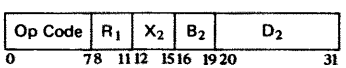
1. Add C (check bit) for odd or even parity as needed, except as noted
2. For even parity use CA
3. Decimal feature
4. Model 67
5. EBCDIC graphics shown are standard bit pattern assignments. For specific print train/chain see printer manual.

RR FORMAT



Decimal	Hexadecimal	Instruction Mnemonic (RX Format)	Graphic & Control Symbols (5) BCDIC	Graphic & Control Symbols (5) EBCDIC	7-Track Tape BCDIC (1)	Punched Card Code	System/360 8-bit Code
64	40	STH		SP	(2)	no punches	0100 0000
65	41	LA				12-0-1-9	0100 0001
66	42	STC				12-0-2-9	0100 0010
67	43	IC				12-0-3-9	0100 0011
68	44	EX				12-0-4-9	0100 0100
69	45	BAL				12-0-5-9	0100 0101
70	46	BCT				12-0-6-9	0100 0110
71	47	BC				12-0-7-9	0100 0111
72	48	LH				12-0-8-9	0100 1000
73	49	CH				12-1-8	0100 1001
74	4A	AH		¢		12-2-8	0100 1010
75	4B	SH	.	.	B A 8 2 1	12-3-8	0100 1011
76	4C	MH	¤)	<	B A 8 4	12-4-8	0100 1100
77	4D	BAS (4)	[	(	B A 8 4 1	12-5-8	0100 1101
78	4E	CVD	<	+	B A 8 4 2	12-6-8	0100 1110
79	4F	CVB	≠	¦	B A 8 4 2 1	12-7-8	0100 1111
80	50	ST	& +	&	B A	12	0101 0000
81	51					12-11-1-9	0101 0001
82	52					12-11-2-9	0101 0010
83	53					12-11-3-9	0101 0011
84	54	N				12-11-4-9	0101 0100
85	55	CL				12-11-5-9	0101 0101
86	56	O				12-11-6-9	0101 0110
87	57	X				12-11-7-9	0101 0111
88	58	L				12-11-8-9	0101 1000
89	59	C				11-1-8	0101 1001
90	5A	A		!		11-2-8	0101 1010
91	5B	S	$	$	B 8 2 1	11-3-8	0101 1011
92	5C	M	*	*	B 8 4	11-4-8	0101 1100
93	5D	D	]	)	B 8 4 1	11-5-8	0101 1101
94	5E	AL	:	;	B 8 4 2	11-6-8	0101 1110
95	5F	SL	Δ	¬	B 8 4 2 1	11-7-8	0101 1111
96	60	STD	-	-	B	11	0110 0000
97	61		/	/	A 1	0-1	0110 0001
98	62					11-0-2-9	0110 0010
99	63					11-0-3-9	0110 0011
100	64					11-0-4-9	0110 0100
101	65					11-0-5-9	0110 0101
102	66					11-0-6-9	0110 0110
103	67	MXD				11-0-7-9	0110 0111
104	68	LD				11-0-8-9	0110 1000
105	69	CD				0-1-8	0110 1001
106	6A	AD		¦		12-11	0110 1010
107	6B	SD	,	,	A 8 2 1	0-3-8	0110 1011
108	6C	MD	% (	%	A 8 4	0-4-8	0110 1100
109	6D	DD	∨	—	A 8 4 1	0-5-8	0110 1101
110	6E	AW	\	>	A 8 4 2	0-6-8	0110 1110
111	6F	SW	⫴	?	A 8 4 2 1	0-7-8	0110 1111
112	70	STE				12-11-0	0111 0000
113	71					12-11-0-1-9	0111 0001
114	72					12-11-0-2-9	0111 0010
115	73					12-11-0-3-9	0111 0011
116	74					12-11-0-4-9	0111 0100
117	75					12-11-0-5-9	0111 0101
118	76					12-11-0-6-9	0111 0110
119	77					12-11-0-7-9	0111 0111
120	78	LE				12-11-0-8-9	0111 1000
121	79	CE		`		1-8	0111 1001
122	7A	AE	ϐ	:	A	2-8	0111 1010
123	7B	SE	# =	#	8 2 1	3-8	0111 1011
124	7C	ME	@ '	@	8 4	4-8	0111 1100
125	7D	DE	:	'	8 4 1	5-8	0111 1101
126	7E	AU	>	=	8 4 2	6-8	0111 1110
127	7F	SU	√	"	8 4 2 1	7-8	0111 1111

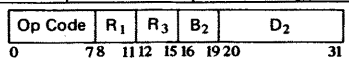
RX FORMAT



R1, D2 (X2, B2) or R1, S2 (X2)
R1, D2 (0, B2) or R1, S2

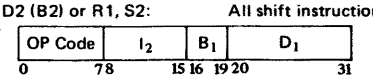
Decimal	Hexadecimal	Instruction Mnemonic (Var.Formats)	Graphic & Control Symbols (5) BCDIC	EBCDIC	7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code
128	80	SSM				12-0-1-8	1000 0000
129	81			a		12-0-1	1000 0001
130	82	LPSW		b		12-0-2	1000 0010
131	83	(Diagnose)		c		12-0-3	1000 0011
132	84	WRD		d		12-0-4	1000 0100
133	85	RDD		e		12-0-5	1000 0101
134	86	BXH		f		12-0-6	1000 0110
135	87	BXLE		g		12-0-7	1000 0111
136	88	SRL		h		12-0-8	1000 1000
137	89	SLL		i		12-0-9	1000 1001
138	8A	SRA				12-0-2-8	1000 1010
139	8B	SLA				12-0-3-8	1000 1011
140	8C	SRDL				12-0-4-8	1000 1100
141	8D	SLDL				12-0-5-8	1000 1101
142	8E	SRDA				12-0-6-8	1000 1110
143	8F	SLDA				12-0-7-8	1000 1111
144	90	STM				12-11-1-8	1001 0000
145	91	TM		j		12-11-1	1001 0001
146	92	MVI		k		12-11-2	1001 0010
147	93	TS		l		12-11-3	1001 0011
148	94	NI		m		12-11-4	1001 0100
149	95	CLI		n		12-11-5	1001 0101
150	96	OI		o		12-11-6	1001 0110
151	97	XI		p		12-11-7	1001 0111
152	98	LM		q		12-11-8	1001 1000
153	99			r		12-11-9	1001 1001
154	9A					12-11-2-8-9	1001 1010
155	9B					12-11-3-8-9	1001 1011
156	9C	SIO				12-11-4-8-9	1001 1100
157	9D	TIO				12-11-5-8-9	1001 1101
158	9E	HIO				12-11-6-8-9	1001 1110
159	9F	TCH				12-11-7-8-9	1001 1111
160	A0					11-0-1-8	1010 0000
161	A1			~		11-0-1	1010 0001
162	A2			s		11-0-2	1010 0010
163	A3			t		11-0-3	1010 0011
164	A4			u		11-0-4	1010 0100
165	A5			v		11-0-5	1010 0101
166	A6			w		11-0-6	1010 0110
167	A7			x		11-0-7	1010 0111
168	A8			y		11-0-8	1010 1000
169	A9			z		11-0-9	1010 1001
170	AA					11-0-2-8	1010 1010
171	AB					11-0-3-8	1010 1011
172	AC					11-0-4-8	1010 1100
173	AD					11-0-5-8	1010 1101
174	AE					11-0-6-8	1010 1110
175	AF					11-0-7-8	1010 1111
176	B0	STMC (4)				12-11-0-1-8	1011 0000
177	B1	LRA (4)				12-11-0-1	1011 0001
178	B2					12-11-0-2	1011 0010
179	B3					12-11-0-3	1011 0011
180	B4					12-11-0-4	1011 0100
181	B5					12-11-0-5	1011 0101
182	B6					12-11-0-6	1011 0110
183	B7					12-11-0-7	1011 0111
184	B8	LMC (4)				12-11-0-8	1011 1000
185	B9					12-11-0-9	1011 1001
186	BA					12-11-0-2-8	1011 1010
187	BB					12-11-0-3-8	1011 1011
188	BC					12-11-0-4-8	1011 1100
189	BD					12-11-0-5-8	1011 1101
190	BE					12-11-0-6-8	1011 1110
191	BF					12-11-0-7-8	1011 1111

RS FORMAT



R1, R3, D2 (B2) or R1, R3, S2: BXH, BXLE, LM, LMC, STM, STMC
R1, D2 (B2) or R1, S2: All shift instructions

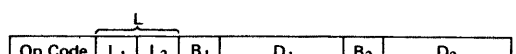
SI FORMAT



D1 (B1) or S1: LPSW, SSM, HIO, SIO, TIO, TCH; TS
D1 (B1), I2 or S1, I2: MVI, CLI, NI, OI, XI, TM, WRD, RDD

Decimal	Hexadecimal	Instruction Mnemonic (SS Format)	Graphic & Control Symbols (5) BCDIC	EBCDIC	7-Track Tape BCDIC (1)	Punched Card Code	System/360 8-bit Code
192	C0		?	¢	B A 8 2	12-0	1100 0000
193	C1		A	A	B A 1	12-1	1100 0001
194	C2		B	B	B A 2	12-2	1100 0010
195	C3		C	C	B A 2 1	12-3	1100 0011
196	C4		D	D	B A 4	12-4	1100 0100
197	C5		E	E	B A 4 1	12-5	1100 0101
198	C6		F	F	B A 4 2	12-6	1100 0110
199	C7		G	G	B A 4 2 1	12-7	1100 0111
200	C8		H	H	B A 8	12-8	1100 1000
201	C9		I	I	B A 8 1	12-9	1100 1001
202	CA					12-0-2-8-9	1100 1010
203	CB					12-0-3-8-9	1100 1011
204	CC			.		12-0-4-8-9	1100 1100
205	CD					12-0-5-8-9	1100 1101
206	CE			+		12-0-6-8-9	1100 1110
207	CF					12-0-7-8-9	1100 1111
208	D0		!	-	B 8 2	11-0	1101 0000
209	D1	MVN	J	J	B 1	11-1	1101 0001
210	D2	MVC	K	K	B 2	11-2	1101 0010
211	D3	MVZ	L	L	B 2 1	11-3	1101 0011
212	D4	NC	M	M	B 4	11-4	1101 0100
213	D5	CLC	N	N	B 4 1	11-5	1101 0101
214	D6	OC	O	O	B 4 2	11-6	1101 0110
215	D7	XC	P	P	B 4 2 1	11-7	1101 0111
216	D8		Q	Q	B 8	11-8	1101 1000
217	D9		R	R	B 8 1	11-9	1101 1001
218	DA					12-11-2-8-9	1101 1010
219	DB					12-11-3-8-9	1101 1011
220	DC	TR				12-11-4-8-9	1101 1100
221	DD	TRT				12-11-5-8-9	1101 1101
222	DE	ED (3)				12-11-6-8-9	1101 1110
223	DF	EDMK (3)				12-11-7-8-9	1101 1111
224	E0		+	\	A 8 2	0-2-8	1110 0000
225	E1					11-0-1-9	1110 0001
226	E2		S	S	A 2	0-2	1110 0010
227	E3		T	T	A 2 1	0-3	1110 0011
228	E4		U	U	A 4	0-4	1110 0100
229	E5		V	V	A 4 1	0-5	1110 0101
230	E6		W	W	A 4 2	0-6	1110 0110
231	E7		X	X	A 4 2 1	0-7	1110 0111
232	E8		Y	Y	A 8	0-8	1110 1000
233	E9		Z	Z	A 8 1	0-9	1110 1001
234	EA					11-0-2-8-9	1110 1010
235	EB					11-0-3-8-9	1110 1011
236	EC			<		11-0-4-8-9	1110 1100
237	ED					11-0-5-8-9	1110 1101
238	EE					11-0-6-8-9	1110 1110
239	EF					11-0-7-8-9	1110 1111
240	F0		0	0	8 2	0	1111 0000
241	F1	MVO	1	1	1	1	1111 0001
242	F2	PACK	2	2	2	2	1111 0010
243	F3	UNPK	3	3	2 1	3	1111 0011
244	F4		4	4	4	4	1111 0100
245	F5		5	5	4 1	5	1111 0101
246	F6		6	6	4 2	6	1111 0110
247	F7		7	7	4 2 1	7	1111 0111
248	F8	ZAP (3)	8	8	8	8	1111 1000
249	F9	CP (3)	9	9	8 1	9	1111 1001
250	FA	AP (3)				12-11-0-2-8-9	1111 1010
251	FB	SP (3)				12-11-0-3-8-9	1111 1011
252	FC	MP (3)				12-11-0-4-8-9	1111 1100
253	FD	DP (3)				12-11-0-5-8-9	1111 1101
254	FE					12-11-0-6-8-9	1111 1110
255	FF					12-11-0-7-8-9	1111 1111

SS FORMAT



D1 (L, B1), D2 (B2) or S1 (L), S2 — NC, OC, XC, CLC, MVC, MVN, MVZ, TR, TRT, ED, EDMK
D1 (L1, B1), D2 (L2, B2) or S1 (L1), S2 (L2) — PACK, UNPK, MVO, AP, CP, DP, MP, SP, ZAP