Systems

IBM System/370 Model 145 Functional Characteristics

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This publication describes the relationship of the Model 145 to other System/370 models and to System/360. Included is information concerning the system features and capabilities; console file; input/output channels; integrated file adapter; OS/DOS compatibility; IBM 1401, 1440, 1460, 1410, and 7010 emulation features; console printer-keyboard; additional instructions; and instruction timings.

The following IBM manuals offer information to assist the reader.

A Guide to the IBM System/370 Model 145, GC20-1734.

System/370 Model 145 Operating Procedures, GA24-3554.

System/370 Principles of Operation, GA22-7000.

System/370 System Summary, GA22-7001.

System/370 Input/Output Configurator, GA22-7002.

System/360 and System/370 Bibliography, GA22-6822,

System/360 Principles of Operation, GA22-6821.

System/360 Component Descriptions, IBM 2314 Direct Access Storage Facility and IBM 2844 Auxiliary Storage Control, GA26-3599.

System/360 I/O Interface -- Channel to Control Unit Original Equipment Manufacturers' Information, GA22-6843.

System/360 Direct Control and External Interrupt Feature, Original Equipment Manufacturers' Information, GA22-6845.

System/360 OS Program Planning Guide for the DOS Emulator on the System/370, GC24-5076.

System/360 DOS Program Planning Guide for MCAR/CCH Function for the IBM System/370 Model 145, GC24-5076

3210 Console Printer-Keyboard Model 2 Component Description, GA24-3552.

3215 Console Printer-Keyboard Model 1 Component Description, GA24-3550.

Form-Design Consideration--System Printers, GA24-3488.

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Preface

This reference publication is intended for system analysts and programmers who require information about system features, CPU and input/output characteristics, timings, machine instructions, and the functions of integrated and attachable I/O devices.

The reader is assumed to have a working knowledge of the *IBM System/370 Principles of Operation*, GA22-7000, and to have had programming experience with other System/360 or System/370 models.

System operating information is contained in the *IBM System/370 Operating Procedures*, GA24-3554.

The manual is divided into sections to assist you in locating a particular topic.

Introduction - General overview of System/370 Model 145, including discussions of CPU components, and a brief description of integrated attachments and I/O channels.

Console File - Functions of this microprogram-loading device.

Console Printer-Keyboard - Programming and configuration information for the printer-keyboard units.

Features Descriptions - A description of major system features such as OS/DOS Compatibility, the Interval Timer, and the Time-of-Day Clock.

Integrated File Adapter - Description and characteristics of the disk-storage facility that is recommended for primary program and data residence.

Input/Output Channel Characteristics - Information about the byte-multiplexer, selector, and block-multiplexer channels.

1401/1460, 1440 Emulation Feature and *1401/1460, 1440, and 1410/7010 Emulation Feature* - Descriptions of these features, including the relationship to the required Emulator Programs.

Timings - Detailed timings for internal CPU functions (instruction execution), the printer-keyboard, the byte-multiplexer channel, the selector channels, the block-multiplexer channels, and the integrated file adapter.

CPU Configurator and System Features - A list of standard and available features, feature dependencies, etc.

Second Edition (October 1970)

This edition replaces GA24-3577-0, which was presented in preliminary form for the announcement of the IBM System/370 Model 145. Changes were made primarily in composition and format to improve the readability and function of this publication; minor corrections were made throughout in style, grammer, and punctuation to further enhance its usability. Before using this manual as a reference for system operation or programming, check the latest SRL Newsletter or contact the local IBM Branch Office to ensure that you have the current information.

Requests for copies of IBM publications should be made to your IBM representative or the IBM branch office serving your locality.

This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. 171, P.O. Box 6, Endicott, N. Y. 13760. A form for readers' comments is provided at the back of this publication. If the form has been removed, send your comments to the above address.

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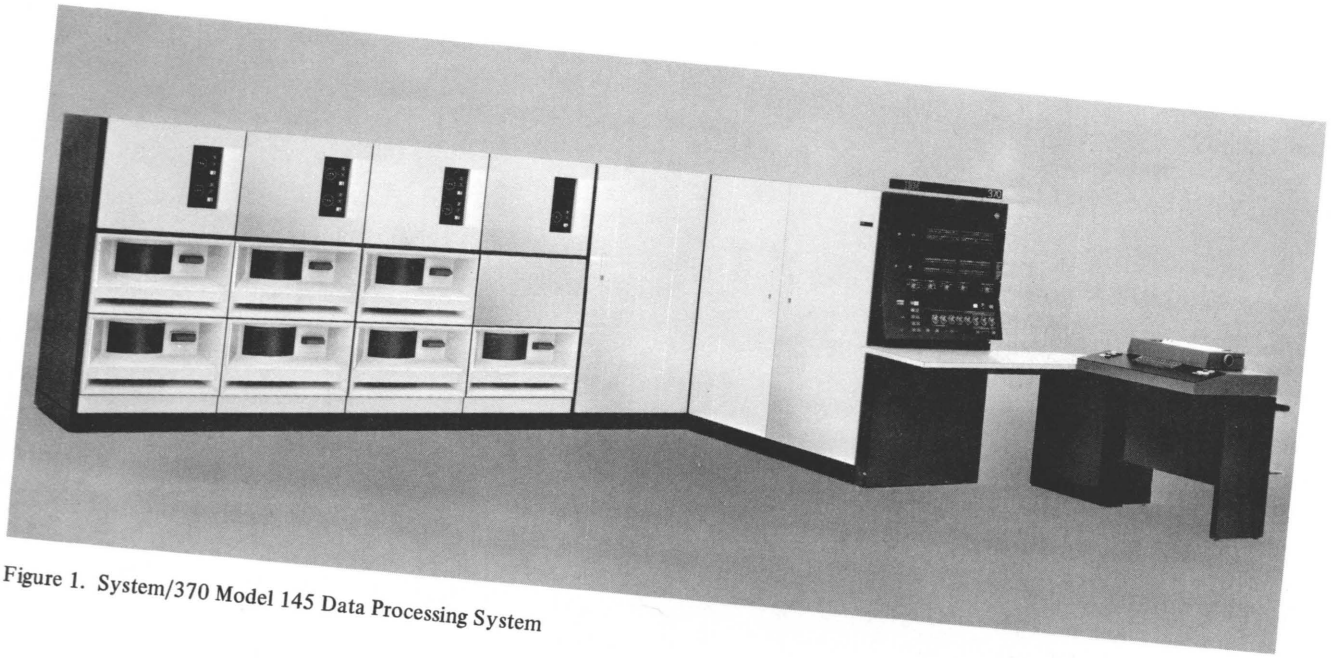


Figure 1. System/370 Model 145 Data Processing System

The System/370 Model 145 is a high-availability general-purpose data processing system that offers significant price/performance improvement and additional functions. It provides the reliability, availability, performance, and convenience demanded by both business and scientific users. The various CPU and I/O configurations allow tailoring computing facilities to match your company's growth.

Each CPU cycle requires from 202.5 to 315.0 nanoseconds, depending upon the operation. The times required for instruction execution are given in the *Timings* section.

The selector and block-multiplexer channels are capable of handling an aggregate data rate of about 5.0 million bytes per second when the Word Buffer feature is installed. Without the word buffer, the maximum aggregate data rate for these channels is about 1.5 million bytes per second.

The maximum byte-multiplexer channel data rates are 50,000 bytes per second in byte mode and 180,000 bytes per second in burst mode. Most input/output devices that can be attached to System/360 can be attached to this system.

The program-storage capacities (114, 688 to 524, 288 bytes), channel configuration, and other system specifications are given in the *System/370 Model 145 CPU Configurator* section. This system incorporates the following features as *standard*. These facilities are described in the *Features Descriptions* section or in the *IBM System/370 Principles of Operation,* GA22-7000.

Audible Alarm
Byte-Oriented Operand Feature
Byte-Multiplexer Channel
Channel Retry Information
Command Retry
Console File
Control Registers
Error Checking and Correction (ECC)
Extended Channel Logout
Extended External Masking
Extended I/O Masking
Interval Timer
Limited Channel Logout
Machine-Check Handling
Microprogram Instruction Retry
OS/DOS Compatibility
Selector Channel (channel 1 without IFA; channel 2 with IFA)
Storage Protection (Store and Fetch)
Time-of-Day Clock
System/370 Commercial Instruction Set, which includes the System/360 Commercial Instruction set, modified instruction formats for Start I/O and Halt I/O, and these enhancement instructions:
  Compare Logical Characters Under Mask
  Compare Logical Long
  Insert Characters Under Mask
  Load Control
  Move Long
  Set Clock
  Shift and Round Decimal
  Start I/O Fast Release (executed as start I/O on the Model 145)
  Store Channel ID
  Store Characters Under Mask
  Store Clock
  Store CPU ID
  Store Control

The following features are *optional* on the System/370 Model 145. Refer to the *System/370 Model 145 CPU Configurator* section for more information.

Additional Byte-Multiplexer Channel Subchannels
Block-Multiplexer Channels (up to 4)
Channel-to-Channel Adapter
Direct Control
Extended Precision Floating-Point Feature
Integrated File Adapter (IFA)
Selector Channels (channels 2, 3, & 4 without IFA; channel 3 with IFA)
Word Buffer (Selector and Block-Multiplexer Channels)
1401/1460, 1440 Emulator
1401/1460, 1440, and 1410/7010 Emulator
3046 Power Unit (required for 3345 or 3346)
3210 Console Printer-Keyboard Models 1 and 2
3215 Console Printer-Keyboard Model 1
3345 Main Storage Frame Model 1 (for 384K systems)
3346 Main Storage Frame Model 1 (for 512K systems)

This publication is intended as a reference for users of the System/370 Model 145: only items that are unique to the Model 145 are discussed in detail. For this reason, a comprehensive understanding of the information in the *IBM System/370 Principles of Operation*, GA22-7000, and the *IBM System/360 Principles of Operation*, GA22-6821, is necessary for effective use of this publication.

Several programming support systems are available for use with the Model 145. These include System/360 Operating System (OS), MFT and MVT, as well as System/360 Disk Operating System (DOS). Refer to the *IBM System/360 and System/370 Bibliography,* GA22-6822, for abstracts of IBM programming publications that apply to this system.

Data Representation

This system is both character- and word-oriented: the basic addressable unit is an 8-bit byte (a character, two decimal digits, or eight binary bits). This provides for more efficient use of storage, and for high effective input/output rates for decimal data, variable field lengths, broad and flexible code conversion, decimal arithmetic, 32-bit words and 16-bit halfwords for fixed-point arithmetic, 32-bit words and 64-bit doublewords for floating-point arithmetic, and powerful instructions for such functions as translate and edit.

Compatibility Between This System, Other System/370 Models, and System/360

Within the storage capacity, internal and input/output channel processing rates, and type of input/output devices that can be attached, compatibility is maintained with other System/370 and System/360 models, with the following *exceptions.*

1. Programs using machine-dependent data (for example, machine logouts).
2. Programs using the ASCII bit (PSW bit 12).
3. Programs that depend upon features or I/O devices that are not implemented on this system (such as special instructions for the System/360 Model 44).
4. Programs that depend upon validity of data after the system power has been turned off and restored.

Programs written for other System/370 or System/360 models that contain the following conditions or requirements should be evaluated on an individual basis to ensure proper operation.

1. Time-dependent programs.
2. Programs written to cause deliberate program checks.
3. Programs that depend upon model-dependent features of other System/370 and System/360 models.
4. Programs that use storage locations between address 128 (decimal) and 704 after a diagnostic logout into program storage. *However*, such programs may be executed:
   a. if the check-control switch is set to Stop After Log position. In this case, processing stops after the diagnostic logout into program storage takes place.
   b. if program-storage locations that are overlaid by the diagnostic logout are restored with the program requirements before an IPL and program restart.

Any attempt to continue processing after a diagnostic logout to program storage *without* restoring your program information to the logout area will have unpredictable results.

The 705-byte extent (the permanently assigned program-storage locations) can be reduced to 512 bytes by moving the 192 bytes (between locations 512 and 704) into another program-storage area. The technique used to accomplish this relocation depends upon your application.

SYSTEM RESIDENCE AND MAINTENANCE-STORAGE REQUIREMENTS

Optimum performance and maximum system availability are maintained when a disk-storage facility is provided for residence of the operating system and the application-program files, storage of diagnostic tests, and storage for error-logout information. In the remainder of this manual, these storage requirements are assumed to be contained in an IBM 2319 Disk Storage Facility (DSF) attached through the Integrated File Adapter (IFA) feature, or a similar disk-storage device attached through a selector channel. For this reason, either the IFA feature with 2319 or selector-channel 1 with DSF is listed as a *Selective Feature Required for Minimum System Configuration. However,* the user has the option of:

1. Using the IFA with a 2319 DSF,
2. Using a selector or block-multiplexer channel with a disk-storage device (selector or block-multiplexer channel 1 with a 2314-type DSF is assumed hereafter), or
3. Electing not to use the Recovery Management Support (RMS) package as described in the *IBM System/360 DOS Program Planning Guide for MCAR/CCH Function for IBM System/370 Model 145,* GC24-5078 and *A Guide to the IBM System/370 Model 145,* GC20-1734. When this option is chosen, the user loses the ability to perform many of the diagnostic tests that provide information to assist in the location and correction of system failures.

CENTRAL PROCESSING UNIT (CPU)

The IBM 3145 Central Processing Unit contains from 114,688 (112K) to 262,114 (256K) bytes of program storage (depending upon the model). The CPU includes control storage, the system control panel, and other facilities necessary to perform arithmetic functions and logical processing of data. The CPU also contains the input/output channel circuitry for control of data transfers between the CPU and I/O devices. The manner in which the various system data-flow elements interact depends upon the microprogram loaded into control storage for that application (such as System/370 operation and 1401 emulation).

See the *Program and Control Storage* section.

Program and Control Storage

At least 32K bytes of control storage, and up to 256K bytes of program storage, are housed in the CPU. For systems with 384K bytes of program storage, the IBM 3345 is required. Systems with 512K bytes of program storage require the IBM 3346. (The IBM 3046 Power Unit is required with either the 3345 or the 3346.)

The system is equipped with a movable control-storage boundary that allows for up to 64K bytes of control storage, depending upon the mix of features installed for the system configuration. This additional control-storage requirement is at the expense of program storage. The storage boundary is determined when the microprogram is compiled by IBM. Refer to the *Control-Storage Requirements* section for an understanding of how this boundary is established.

Control storage contains the microprogram upon which all system operations depend. Control storage is not available to the user and should not be modified. To do so could make application results unpredictable.

Application-program data is read out of (or into) storage four bytes (a fullword) at a time. To increase system performance, however, program instructions are read out eight bytes (a doubleword) at a time.

Error Checking and Correction (ECC) on processor storage provides automatic single-bit error detection and correction. It also detects all double-bit errors and most multiple-bit storage errors but does not correct them. Parity checking is used to verify other data in the system that is not contained in program or control storage.

Program-storage addressing begins at location 0 and continues up through the highest installed program-storage byte location. Fixed program-storage allocations for all configurations to ensure compatibility between System/370 and System/360 models are:

Decimal Word Addr	*Length*	*Purpose*
0	2 wds	Initial program-loading PSW (also Restart New PSW)
8	2 wds	Initial program-loading CCW1 (also Restart Old PSW)
16	2 wds	Initial program-loading CCW2
24	2 wds	External old PSW
32	2 wds	Supervisor-call old PSW
40	2 wds	Program old PSW
48	2 wds	Machine-check old PSW
56	2 wds	Input/output old PSW
64	2 wds	Channel status word
72	1 wd	Channel address word
76	1 wd	---
80	1 wd	Timer
84	1 wd	---
88	2 wds	External new PSW
96	2 wds	Supervisor-call new PSW
104	2 wds	Program new PSW
112	2 wds	Machine-check new PSW
120	2 wds	Input/output new PSW
128	8 wds	Reserved
160	8 wds	I/O communications area
192	10 wds	Reserved
232	2 wds	Machine-check interruption code
240	2 wds	Reserved
248-704	110 wds	Diagnostic logout area.

The remaining byte locations of program storage are available for programming functions.

Note: When the IBM 3345 or 3346 is included, the low-order storage addresses are in that unit.

Control-Storage Requirements

At least 32K bytes of storage are reserved for control storage; it may be as much as 64K bytes (in 2K-byte increments). However, the amount of program storage is varied by the control-storage requirements of the features mix specified for a given microprogram load. Thus, depending upon the features actually needed for a particular application, the decrease in available program storage is from 0 bytes to 32K bytes in 2K increments.

The address boundary between control and program storage is assigned when the microprogram is compiled (before writing the console file disk). The boundary is established at the upper limit of program storage. If any program instruction or I/O operation attempts to access a storage location at or above this boundary, an address check results and no storage access is made. Similarly, if a control-storage access is attempted below the boundary, a machine check occurs.

Most System/360 Programming Systems, such as Disk Operating System (DOS), Tape Operating System (TOS), and Operating System (OS), support program-storage sizes in 2,048-byte increments. Other System/360 Programming Systems run on this model, but the amount of program storage available after control-storage requirements have been met must be equal to (or larger than) the program-storage size supported by that programming system.

The reloadable control storage is housed in the central processing unit. It is loaded from the Console File. Control-storage requirements for this system are the *sum* of the following.

	Bytes	*Bytes*
Basic System Microcode (does not include 16 standard subchannels on byte-multiplexer channels):		= 24,600
• Byte-multiplexer channel UCW's --		
16 MPX channel units:	256	
32 MPX channel units:	512	
64 MPX channel units:	1,024	
128 MPX channel units:	2,048	
256 MPX channel units:	4,096	= __ , ___
Optional System Features:		
• Console Printer-Keyboards --		
3210 Model 1:	3,040	
3210 Model 1 with 3210 Model 2:	3,160	
3215 Model 1:	3,620	
3215 Model 1 with 3210 Model 2:	4,180	= __ , ___
• Block-Multiplexer channel (microcode that supports any or all block-multiplexer channels, excluding UCW requirements):	2,100	= __ , ___
• Block-multiplexer channel UCW's (UCW's for the block-multiplexer channels come in groups of 8, and are shared between all installed block-multiplexer channels) - 64 bytes times groups of 8 UCW's:		= __ , ___
• Integrated File Adapter:	8,800	= __ , ___
• Compatibility Support --		
1401/1440/1460 compatibility:	4,800	
1401/1440/1460 and 1401/7010 compatibility:	6,000	= __ , ___
• Floating point with extended precision:	2,240	= __ , ___
• Direct Control:	120	= __ , ___
Total Control-Storage Locations for your System:		__ , ___

Example:

Basic system:	24,600 bytes
16 UCW's on byte-multiplexer channel:	256 bytes
3210 Model 1:	3,040 bytes
Integrated file adapter:	8,800 bytes
1401/1440/1460 compatibility:	4,800 bytes
Total:	41,496 bytes

Control-storage requirements in *excess* of 32,768 bytes are at the expense of program storage. Additional control-storage space is allocated in 2,048-byte increments. In the example, although the total control-storage requirement is 41,496 bytes, 43,008 bytes must be allocated for control storage because this is the next-higher level in 2,048-byte increments [that is, 32,768 + (5 times 2,048) = 43,008]. This reduces the available program storage by 10,240 bytes.

The user may load another console-file disk for a different feature mix (and automatically reset the control-storage/program-storage boundary). Because applications for a system installation would normally require only one microprogram load, additional disks that contain other feature mixes for that installation are available by special order from IBM.

Local Storage

Local storage is a facility that is used to contain working areas for high-speed access by the arithmetic/logic unit and other data-flow components. Certain areas of local storage are reserved for:

General registers 0 through 15.
Floating-point registers 0, 2, 4, and 6.
Instruction counter.

Refer to the *IBM System/370 Model 145 Operating Procedures*, GA24-3554, for reasons and techniques for displaying or altering local-storage areas.

Microprogram Loading

The microprogram control words are loaded from read-only magnetically encoded disks that are read by the console file. These disks are prepared for each configuration and shipped with the system. Additional disks contain a comprehensive set of system diagnostics that are used to assist in locating a failing component. The actual initial microprogram load (IMPL) procedures, as well as other operator instructions, are included in the *IBM System/370 Model 145 Operating Procedures*.

After the microprogram is loaded into control storage, system operation can be initiated by the operator from the system control panel. Depending upon the job requirements and the operating system being used, the microprogram sequences control further system operations.

Refer to the sections titled *Console File* and *Control Storage Requirements* for additional information.

ERROR HANDLING

If application-program errors occur (such as illogical action requests), the operating system attempts to handle the exception and provide any necessary operator messages. Refer to

the applicable programming publications for the IBM operating system you use. These are listed in the *IBM System/360 and System/370 Bibliography*, GA22-6822.

If a failure occurs within the CPU or an I/O unit, provisions are made to retry the failing operation. Error-logout facilities are incorporated into the system to record any such failures. (This is in addition to any provisions made by the operating system for error retry and error logging.)

Microprogram instruction retry, limited and extended channel logout, storage validation (Error Checking and Correction -- ECC) for program and control storage, and other error-detection and error-handling provisions are standard.

Microprogram Instruction Retry

The ability to recover from most intermittent failures is provided by retry techniques. CPU retry is done by microprogram routines that save the source data before it is altered by the operation. When an error is detected, a microprogram routine returns the CPU to the beginning of the operation (or to a point during the operation that was executed correctly), and the operation is repeated.

Error Checking and Correction (ECC)

Error checking and correction circuitry for program and control storage automatically corrects single-bit errors. Automatic detection of double-bit errors is also provided.

Channel Retry Information

Channel retry information is provided in the Extended Channel Status Word (ECSW). This information may be used with Channel Check Handler (CCH) routines in the retry of failing I/O operations. Where possible, channel microprogram instructions are retried using the existing CPU-retry machine logic. When an uncorrectable channel-CPU error occurs, the channel affected by the error provides a Channel Status Word (CSW), and ECSW, and a logout via an interruption or a condition code 1 store operation.

Command Retry

Command retry is a control-unit initiated procedure between the channel and the control unit. (Not all control units have this capability.) No I/O interruption is required. The number of retries is device-dependent.

INTEGRATED INPUT/OUTPUT ADAPTERS

The following three I/O devices are attached directly to the central processing unit through integrated adapters. These are described in detail in other sections of this manual. In addition, a wide variety of input/output devices can be attached through the input/output channels.

Console File: This device is used to load control storage with either the normal microprogram or with diagnostic microprograms.

Console Printer-Keyboard: This unit serves as the on-line input/output device for operator/system communication. It is used to enter or display programming-systems control parameters, responses to system messages, and display or alterations of application data, general and floating-point registers, etc.

Integrated File Adapter (with DSF): The IBM 2319 Disk Storage Facility (DSF) is attached through the Integrated File Adapter (IFA) feature. The 2319 includes three access mechanisms. Refer to the *IFA Characteristics* section for information about additional access mechanisms (up to eight).

The IFA (with 2319 DSF) is used to contain portions of the programming operating system. It also contains system tests and the error-logout storage areas for minimum system-maintenance support that require one cylinder. The remaining capacity of the device is available for problem-program use.

If the IFA is *not* installed, selector channel 1 with a direct-access storage device is required to satisfy this minimum system-configuration support.

INPUT/OUTPUT CHANNELS

This section is an introduction to the input/output channels. Refer to the *Input/Output Channel Characteristics* section for detailed information.

The byte-multiplexer, block-multiplexer, and selector channels operate with the same I/O instructions and command formats used for other System/370 models and for System/360 models 25 and up. In addition, the Halt I/O instruction has been redefined: a variation of Halt I/O (Halt Device) has been implemented.

Selector channels operate with attached I/O control units by using signal sequences defined in *IBM System/360 I/O Interface - Channel to Control Unit Original Equipment Manufacturers' Information,* GA22-6843. Block multiplex mode, and additional control lines (data-in, data-out, and disconnect-in) are described in the *Input/Output Channel Characteristics* section. Refer also to the *Integrated File Adapter* section.

With the *byte-multiplexer* channel, a maximum of 256 subchannels are available to address up to 256 devices. Sixteen subchannels are provided in the basic machine with the option of 32, 64, 128 and 256. If subchannels are shared, the number of unshared subchannels is reduced accordingly. The definition and addressing of shared and unshared

subchannels is discussed in the *Input/Output Channel Characteristics* section.

With each selector channel, up to 256 I/O devices can be addressed. When the block-multiplexer channel feature is installed on a selector channel, that channel becomes a *block-multiplexer* channel with a *pool* of Unit Control Words (UCW's) available for that channel. The size of this pool is optional (in increments of 8) and the number allocated per channel is flexible and may be varied from job to job through the dynamic assignment capability. The maximum size of the pool is 512 unshared UCW's. Refer to the *Block-Multiplexer Channel UCW Assignments* section for a discussion of the factors to be considered in selecting the optimum number of UCW's for a particular installation.

Channel Interface

A standard input/output interface is provided for attachment of a wide range of I/O devices. This interface is a set of standard electrical connections through which data and control signals are exchanged between the CPU and attached I/O devices.

For selector channel and block-multiplexer channel operation, the standard interface is *extended* to include the data-in, data-out, and disconnect-in lines.

Data-In/Data-Out, used with Service-In/Service-Out, permits data transfers to take place faster than when using only the Service-In/Service-Out tags. Or, these facilities can be utilized to permit the placement of a control unit at a greater distance from the channel.

Disconnect-In provides control units with the ability to alert the system of a malfunction that prevents the control unit from signaling properly over the I/O interface.

Byte-Multiplexer Channel

One byte-multiplexer channel is included as part of the basic system. The channel data rate is 50,000 bytes per second. This data rate allows for typical interface delays but does not include selector-channel interference. The byte-multiplexer channel normally operates in byte mode. In this mode, the single data path of the channel can be time-shared by a number of low-speed I/O devices operating simultaneously. The channel, on demand, handles data to or from these devices (one device at a time) in groups of bytes as determined and specified by the device being serviced. Such interleaved segments of information can consist of a single byte, several bytes, or status or control information used to initiate a new sequence.

Certain I/O devices may force the byte-multiplexer channel to operate in burst mode. The burst can consist of a few bytes, a whole block of data, or a sequence of data blocks with associated control and status information. The data rate in burst mode is 180,000 bytes per second. This data rate allows for typical interface delays but does not include selector-channel interference.

Selector Channel

Up to four selector channels are available. Average data rates are dependent upon whether the word-buffer feature is installed, the number of channels in use, the interface cable lengths, and the number of I/O units attached. The maximum data rate possible for a selector channel with the buffer installed is 1,850,000 bytes per second. The maximum data rate without the word-buffer feature is 820,000 bytes per second.

Block-Multiplexer Channel

Block-multiplexing channels (defined in the *IBM System/360 Principles of Operation*) are available instead of any of the installed selector channels 1, 2, 3, and/or 4 (only channels 2 and 3 when the IFA is installed). This channel is optimized for relatively high-speed burst operations and is designed to multiplex complete blocks of data, permitting the device to disconnect *only* after channel end or upon execution of a halt I/O instruction.

The multiplexing facility of the block-multiplexer channel allows the interleaved execution of several channel programs by the same channel.

Block-Multiplexing Control (defined in the *IBM System/370 Principles of Operation*) allows operation of the block-multiplexer channel as a selector channel.

Attachable Input/Output Devices

The I/O devices that can be attached to Model 145 are listed in the *IBM System/370 Input/Output Configurator*, GA22-7002.

The Console File is the Initial Microprogram Loading (IMPL) device for the system. It provides, on removable disks, all microprograms for the system. Each disk contains a full control-storage load of system microcode. The several disks supplied with the system supply the microprograms required for System/370 operation, emulators, diagnostics, etc, to be loaded into control storage.

Power to the file is normally off. An IMPL (automatic with power on) or diagnostic operation initiated from the system console turns console-file power on, and loading of data from the file occurs. Power to the console file is turned off automatically when loading is complete.

The console file is located at the back of the operator's console table. Room to store a number of disks is provided inside the cover (adjacent to the file mechanism).

Instructions for using the console file are included in the *IBM System/370 Model 145 Operating Procedures,* GA24-3554.

Initial Microprogram Loading (IMPL)

An IMPL occurs automatically when system power is applied or when the console file start key is pressed. In either case, the IMPL indicator is turned on and power is applied to the console file. When the console file attains operating speed, reading is started (CPU console switches must be set to PROCESS or their normal positions).

The microprogram is loaded from the console file into control storage. The amount of control storage depends upon the configuration of features installed in the system, as outlined in the *Control Storage Requirements* section). When loading is complete, console-file power is turned off, and a system reset is executed.

After the system reset routine is executed, the IMPL indicator is turned off, and the CPU enters the stopped state until some external action is taken (such as IPL).

Console Printer-Keyboard

The console printer-keyboard (PR-KB) is an input/output device that provides for manual entry into storage, alter/display functions, and printing of program-generated messages messages. The device consists of a printer and keyboard, which are linked to attachment circuitry in the CPU.

Configurations

System/370 Model 145 offers three console printer-keyboard options.

Option 1 - An IBM 3210 Console Printer-Keyboard Model 1 (Figure 2).

Option 2 - An IBM 3215 Console Printer-Keyboard Model 1 (Figure 3).

Option 3 - In combination with either option 1 or 2, a pedestal-mounted, remotely attached auxiliary IBM 3210 Console Printer-Keyboard Model 2 may be specified (Figure 4).

This section assumes the presence of the 3210 Model 1. Differences between the 3210 Model 1, the 3210 Model 2, and the 3215 Model 1 are given where applicable.

The 3210 Model 2 is functionally identical to the 3210 Model 1, except that it has no alter/display capability and has its own ac power cord and on/off switches (for the printer drive motor). Refer to the *IBM 3210 Console Printer-Keyboard Model 2 Component Description,* GA24-3552, for additional information.

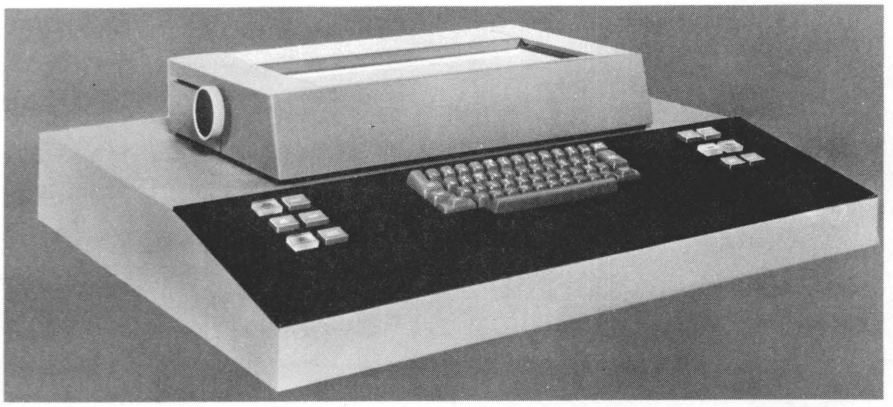


Figure 2. IBM 3210 Console Printer-Keyboard Model 1

Figure 3. IBM 3215 Console Printer-Keyboard Model 1

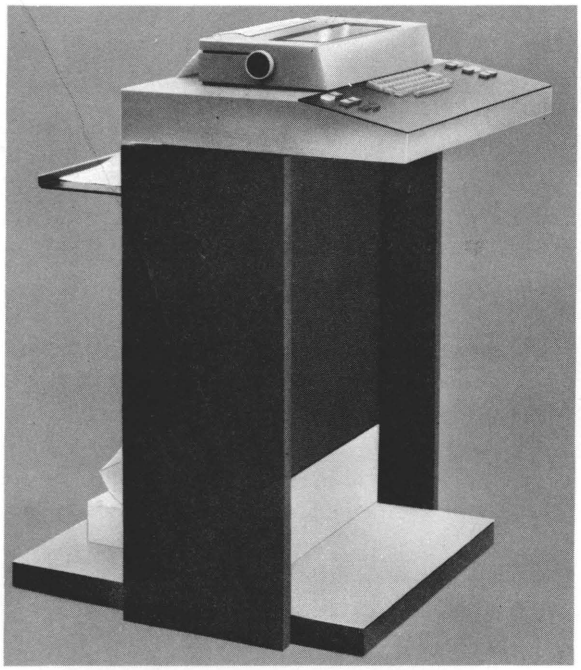


Figure 4. IBM 3210 Console Printer-Keyboard Model 2

Both the 3210 and the 3215 accept the same I/O commands, perform the same functions, and (except for the 3210 Model 2) have the same keys and indicators. The 3210 Model 2 has no alter/display capabilities, or alter/display lights or switches. Instead it has an ac power-on and power-off switch. Both units print serially (one character at a time). The 3210 units print about 15.5 characters per second. The 3215 prints about 85 characters per second. When the 3210 Model 2 is included, it can be located up to 50 feet from the CPU, such as near an I/O device that requires supervision by the operator.

Options 1 and 3 -- IBM 3210 PR-KB: The printer uses a spherical print element having 88 graphic characters, any of which may be printed either from the system or manually from the keyboard. The characters have an optimized arrangement on the print element that provides a faster response. Carrier return speed is about 15 inches per second.

Option 2 -- IBM 3215 PR-KB: The characters are formed in a dot matrix as the print element (containing seven print wires in a vertical row) drives the wires against the ribbon, paper, and platen. For additional information on this printer, refer to *IBM 3215 Console Printer-Keyboard Model 1 Component Description,* GA24-3550.

Printer Functions

Both printers have fixed margins and, in addition to printing, both perform the following functions.

Space: Advance the print element one space to the right.

New Line: Provide a powered return of the print element to the left margin accompanied by a vertical line-feed operation.

Forms Carriage

Each printer uses a pin-feed platen for positive feeding of continuous forms having a hole-to-hole width of 13-1/8 inches. For additional information on forms specifications, refer to *Form-Design Considerations--System Printers,* GA24-3488.

Vertical line spacing is six lines per inch. The horizontal print line is 12.5 inches long, or a maximum of 125 character spaces (ten character spaces to the inch).

Keyboard

The keyboard with either PR-KB option contains 44 character keys along with shift, shift lock, and return keys, as well as the space bar. The tab and backspace keys are not used.

Each of the graphic character keys represents two characters. The character to be entered is selected by using the shift key. Figure 5 shows the arrangement of the character and function keys as well as the control keys and indicator lights.

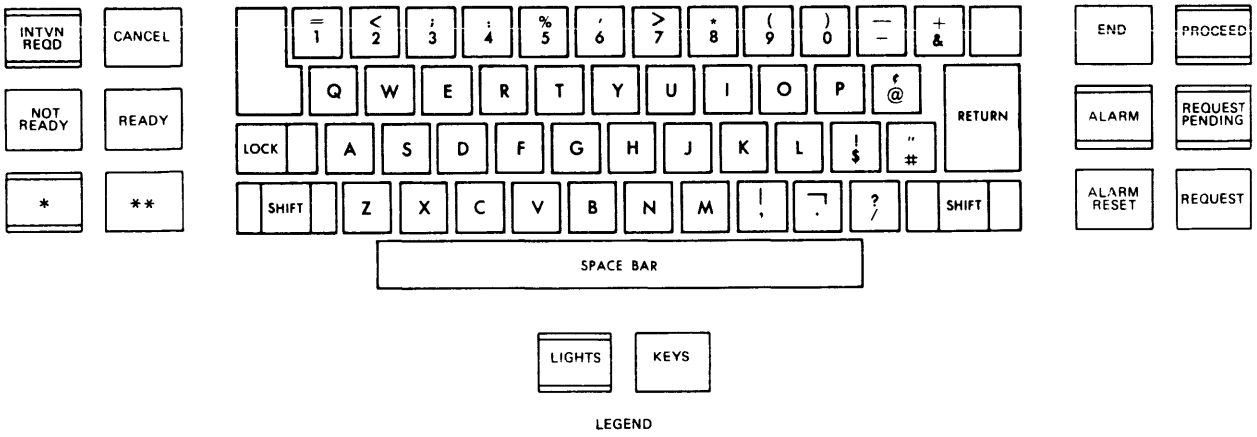
Detailed information on the function of each of the non-graphic (control) keys is found in the *IBM System/370 Model 145 Operating Procedures,* GA24-3554.

EBCDIC Graphic Code Set

Representations of the EBCDIC graphic set and associated code bits are shown in Figure 6.

Manual Operations

Manual operations, including alter/display operations, are described in the *System/370 Model 145 Operating Procedures.*



* ALT/DISP MODE (indicator), 3210 Model 1 and 3215 Model 1 only.
POWER ON (Back-Lighted Switch), 3210 Model 2 only.

** ALTER/DISPLAY (Switch), 3210 Model 1 and 3215 Model 1 only.
POWER OFF (Switch), 3210 Model 2 only.

Figure 5. Printer-Keyboard Keys and Lights Arrangement

Bits 0-1	00				01				10				11			
Bits 2-3	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
Bits 4,5,6,7																
0000					SP	&	-									0
0001							/		a	j			A	J		1
0010									b	k	s		B	K	S	2
0011									c	l	t		C	L	T	3
0100									d	m	u		D	M	U	4
0101		NL							e	n	v		E	N	V	5
0110									f	o	w		F	O	W	6
0111									g	p	x		G	P	X	7
1000									h	q	y		H	Q	Y	8
1001									i	r	z		I	R	Z	9
1010					¢	!		:								
1011					.	$	,	#								
1100					<	*	%	@								
1101					(	)	_	'								
1110					+	;	>	=								
1111					|	¬	?	"								

Figure 6. EBCDIC Graphic Code Set

PROGRAMMING INFORMATION FOR PRINTER-KEYBOARD

Except for transfer-in-channel, printer-keyboard operation written for these units are compatible with programs written for the IBM 1052 Model 7 Printer-Keyboard. (Transfer-in-channel is not defined for the 1052 Model 7.)

Except as specifically noted, system operation with either PR-KB configuration is as follows.

To the programmer, the printer-keyboard appears to be attached to the multiplexer channel with a device address of 01F; a multiplexer channel UCW is used for printer-keyboard program-controlled operations. The printer-keyboard does *not* use one of the eight control-unit positions on the multiplexer channel.

Besides program-controlled operations, microprogram-controlled alter/display functions are provided by the 3210 Model 1 or the 3215 Model 1 PR-KB (not by the 3210 Model 2 remote unit). The alter/display function can be requested by pressing the Alter/Display key (3210 Model 1 and 3215 Model 1 only). The primary function of this operation is to provide a means of altering or displaying local storage, main storage, and certain other facilities. These facilities are described in the section on Alter/Display Operations in the *IBM System/370 Model 145 Operating Procedures.*

Status or sense information is not applicable to alter/display functions. However, the alter/display function is not executed until any current program-controlled operation is completed to the point at which status for the operation is presented to the CPU.

If an alter/display operation is started, any CPU instruction execution is delayed until after the alter/display operation is completed. Therefore, initial-selection status for an I/O instruction cannot be obtained while the alter/display operation is in progress because the I/O instruction cannot be executed.

Channel Command Words For Printer-Keyboard

Valid commands are:

Command Bits 0123 4567	*Command Name*
0000 0001	Write without Automatic Carrier Return (ACR)
0000 0011	No-Op
0000 0100	Sense
xxxx 1000	Transfer in Channel (TIC)
0000 1001	Write with Automatic Carrier Return (ACR)
0000 1010	Read
0000 1011	Audible Alarm

Any command code issued to the PR-KB with a bit structure other than those listed results in unit check (status bit 6) and command reject (sense bit 0) indications.

Write (without Automatic Carrier Return)

The write command is accepted by the PR-KB attachment only if:

1. The PR-KB is operational (ready).
2. The write command has a valid format (data count is not 0, data address valid, etc), and
3. The PR-KB is not performing some other operation.

If the PR-KB is not ready, condition-code 1 is set, and unit check status in the Channel Status Word (CSW) is:

1. Stored for the Start I/O initiating the write command, or
2. Stored on a subsequent I/O interruption (or a Test I/O) if chaining to the write command was performed.

If the write command is accepted, a console service request occurs and the character is printed or the function performed.

If the end-of-line switch is activated, a new-line function is automatically initiated.

The keyboard is interlocked during a write operation.

Operation of the End key terminates any write command operation that is in progress. When the write command is terminated, an asterisk is printed, and a new-line operation takes place.

No-Op (No Operation)

No-Op is an immediate command. This command is processed whether or not the PR-KB is operational. The unit-check and intervention-required bits are *not* set on when a No-Op is executed.

Channel end and device end are set in a CSW stored for a Start I/O that indicates a No-Op (if command chaining is not indicated).

Sense

The sense command is processed whether or not the PR-KB is operational. The sense byte is read from control storage and placed in the main storage location specified by the address in the sense command. If not operational, unit check and intervention required are *not* set on when a sense command is executed. The data count in the sense command should equal one. If the count is greater than one, an Incorrect Length (IL) indication results if the Suppress Length Indication (SLI) flag is off in the sense command.

Channel-end and device-end status are presented in the CSW stored by a subsequent I/O interruption (or cleared by a Test I/O) for the sense operation.

Transfer in Channel (TIC)

The transfer-in-channel command functions in the normal manner, as described in the *IBM System/360 Principles of Operation.*

Write with ACR

The write with Automatic Carrier Return (ACR) command functions in the same basic manner as a write command. However, a new-line function (carrier return and line feed) is performed after the data count reaches zero. The new-line function is performed as follows.

1. In the service request that occurs after the last character has been sent to the printer, a new-line operation is forced and channel end is set on in the PR-KB status byte.
2. The new-line function is performed by the printer.
3. On completion of the ACR, another service request is called for to set device end in the unit status.

Read

The read command is accepted by the attachment only if:

1. The PR-KB is ready, and
2. The PR-KB is not performing some other operation.

If the PR-KB is not ready, unit-check status set in the CSW is:

1. Stored for the Start I/O initiating the command, or
2. Stored on a subsequent I/O interruption (or a Test I/O) if chaining to the read command was performed (condition-code 1 is set).

If the read command is accepted, the proceed indicator lights.

If the end-of-line switch is operated after a character is printed, a new-line function occurs but the new line-character bit-pattern is not sent to main storage. The Proceed light is off until the new-line function is completed.

If the end key is pressed, the read operation is ended. (If the count is not 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation.) The end character bit pattern is not sent to main storage and nothing is printed as a result of an end-key operation.

If the cancel key is pressed, unit exception status is set on. (If the data count is not 0 and the SLI flag is off, IL is indicated in the CSW stored for the operation.) A bit pattern is not sent to program storage, but an asterisk is printed and the carrier returns. If the data count equals zero, the operation is ended the next time any key is operated. The character bit pattern is not sent to main storage and nothing is printed. If any key other than the end or cancel key is operated, IL is indicated in the CSW stored when the SLI flag is *off*.

At the end of each read operation (count zero or end of data), the printer-ready condition is tested. If the printer is not ready, chaining is not allowed. Unit check, channel end, and device end are set on as ending status in the PR-KB sense byte.

Audible Alarm

This control command is an immediate command and functions in the same manner as a No-Op, except that an alarm sounds in the CPU when the control command is executed.

Under program control, the Audible Alarm signals the operator when the system requires manual attention. When the program issues the alarm command, the feature emits an audio tone and turns on the Alarm indicator on the printer-keyboard. The tone sounds for about 1.5 seconds, but the indicator remains on until the operator presses the Alarm Reset key on the printer-keyboard. The alarm intensity is adjustable.

An audible-alarm command is executed even if the PR-KB is in the not-ready state.

Status Byte For Printer-Keyboard

The status byte for the printer-keyboard is kept in control storage. Status is presented in the CSW, only for not-ready-to-ready, device-end, channel-initiated, and attention-status operations (that is, *not* for alter/display functions).

Attention (Status Bit 0): This bit is set when the Request key is pressed if no other operation is in progress. If another operation is in progress, pressing the request key causes the attention status bit to be turned on after status for the other operation has been cleared (that is, accepted by the CPU program). If the other operation is an alter/display operation (for which operations status is not presented), attention is not set on until the alter/display is completed.

When the attention bit (status bit 0) is on, bit 32 of the CSW is set on for the following.

1. If an I/O interruption for the PR-KB is processed.
2. If a Start I/O is executed before the I/O interruption can be processed. Busy (bit 35) is also set on.
3. If a Test I/O is executed before the I/O interruption can be processed.
4. If a Halt I/O is executed before the I/O interruption can be processed, the CSW is not stored and the condition code is 0 (interruption pending).

The preceding Items 1, 2, and 3 clear the status at the PR-KB. Item 4 does not clear the status.

Status Modifier (Status Bit 1) and Control Unit End (Status Bit 2): Unit status bits 1 and 2 are not used for PR-KB operations.

Busy (Status Bit 3): Busy is set in the CSW (bit 35) stored as a result of execution of a Start I/O for the following conditions only.

1. A program operation (other than a No-Op or alarm command) has been completed to the point at which channel end has been accepted by the CPU (and I/O interruption or Test I/O instruction has been processed to store the channel end in a CSW), but device end is now outstanding. Device end (CSW bit 37) accompanies busy in the CSW for the Start I/O, and the status at the PR-KB is cleared.
2. Attention status (resulting from a request-key operation) is outstanding for the PR-KB (that is, the attention has not yet been cleared by an I/O interruption or Test I/O operation). Attention (CSW bit 32) accompanies the busy bit in the CSW stored for the Start I/O.
3. A device end for a not-ready-to-ready sequence (the ready switch has been operated) is outstanding at the PR-KB. Device end (CSW bit 37) accompanies busy in the CSW stored for the Start I/O.
4. A program operation has been completed to the point at which channel end has been accepted by the CPU (an I/O interruption or Test I/O instruction has been processed to store the channel end in the CSW), but device end is not yet available. The busy bit alone is presented in the CSW for the Start I/O, and the PR-KB status is not affected.

Busy is stored as a result of a Test I/O instruction, only if it is executed after channel end for a command is accepted, but before device end for that same command occurs.

Channel End (Status Bit 4): Channel end is set on in the PR-KB attachment for any of the following conditions.

1. A zero data count has occurred for a write, write-with-ACR, read, or sense command.
2. At initial selection during execution of a No-Op or alarm command when that command is accepted by the PR-KB attachment.
3. The end key or the cancel key has been operated during a read command.
4. The end key is operated during a write command.
5. If a count of greater than 1 is specified in a sense command; the operation is terminated after 1 byte is transferred.

If channel end alone is in the byte-multiplexer channel Interruption Buffer (IB) or has been stacked at the PR-KB, it is cleared by an I/O interruption (or by a Test I/O) and stored in the CSW.

Device End (Status Bit 5): Device end is set on for any of the following.

1. When carrier-return motion has begun for a read or write-with-ACR command.
2. On the service request following the one in which a zero-count condition occurs for a write (with no ACR) command.
3. When the PR-KB attachment accepts a No-Op or alarm command.
4. When the ready key is pressed while the PR-KB is in the not-ready condition. (The key must produce a ready condition to set device end.)
5. During the service request in which a sense byte is sent to the CPU.

If a device end has been generated or stacked at the PR-KB, it is cleared by initial selection for a Start I/O, only if channel end (as a result of the operation) has already been stored in the CSW by an I/O interruption or Test I/O. Busy accompanies device end in the CSW stored for the Start I/O.

Test I/O clears any outstanding device end at the PR-KB.

A Halt I/O does not clear a device end at the PR-KB.

Unit Check (Status Bit 6): Unit check is set for any of the following reasons.

1. When a character with even parity is sent from the keyboard to the CPU during a read command operation. Equipment check, sense bit 3, is also set on for this condition.
2. If a parity error is detected on data on a write operation, a check condition is indicated in the same manner as for other multiplexer channel operations.
3. When the forms switch indicates that the PR-KB is out of paper or in the not-ready condition, but then only:
   a. At initial selection for a read or write (with or without ACR) command, or
   b. During execution of a Test I/O instruction to the PR-KB.

   (Intervention required, sense bit 1, is also set on for this condition.)
4. If a command byte not defined for the PR-KB is sent to the PR-KB. (Command reject, sense bit 0, is also set for this condition.)
5. If the printer fails to print within approximately two seconds, equipment check (sense bit 3) is also set.
6. If the 3215 printer has a print-sync check.
7. If the 3215 printer is in the not-ready condition because the cover is not closed, or because it is in test mode.

Unit Exception (Status Bit 7): This bit is set on if the cancel key is operated *during* a read command operation. The read operation is terminated (channel-end status is set on).

If the count is not zero and the SLI flag is off for the read command, the incorrect-length indication (CSW bit 41) is also given during a subsequent I/O interruption or Test I/O operation.

Channel Status Byte For Printer-Keyboard

The channel status byte for PR-KB operations is set up in the UCW used for the PR-KB. The channel status byte portion of the CSW is stored as a result of processing a Test I/O instruction, only if an interruption condition is outstanding for the PR-KB, or as a result of an I/O interruption executed for the PR-KB.

Program Controlled Interruption [PCI] (CSW Bit 40): The following are characteristics of the PCI.

1. The PCI does not affect the progress of the current operation.
2. PCI's are not stacked. If one or more PCI's in a chain have not been processed (prevented by the system mask), only the latest PCI will be processed.
3. A PCI bit in a CCW causes the PCI to remain pending (until processed) throughout the chain if the PCI cannot be taken when first detected.

Incorrect Length [IL] (CSW Bit 41):

1. IL is set in the CSW (stored by a Test I/O or I/O interruption) as a result of a *read* command during which the end or cancel key is operated, or a result of a *write* command during which the end key (not cancel) is operated, when the count does not equal zero and the SLI flag is *off*. Any chain is terminated.
2. IL is set in the CSW (stored by a Test I/O or I/O interruption) as a result of a *read* command during which the count equals zero and any key other than the end or cancel is operated *and* the SLI flag is *off*. Any chain is terminated.
3. An intervention-required condition occurs (out-of-forms or not-ready switch is operated), and the count does not equal zero when either:
   a. The SLI flag is off, or
   b. The SLI flag is on *and* data chaining is also specified. Any chaining is terminated.
4. IL is set for any *write* command if the SLI flag is off for that operation. This results from the fact that the PR-KB attachment requests one more data cycle after the CCW data count has decremented to zero. Any chaining is terminated if the IL indication occurs. If, however, the chain-data flag is on in the current write command, the IL indication will not occur for that write command. But, the last write command in the data chain should have its SLI flag on in order to avoid the IL indication.
5. IL is set for a sense command if the data count specified is greater than 1 and the SLI flag is *off*.

Program Check (CSW Bit 42) and Protection Check (CSW Bit 43): Program check and protection check are set as defined for the multiplexer channel.

Channel Data Check (CSW Bit 44): This bit does not apply to PR-KB operations.

Channel Control Check (CSW Bit 45): This bit is set as defined for the multiplexer channel.

Interface Control Check (CSW Bit 46): A share request is received and *none* of the following conditions exist.

1. A not-ready-to-ready sequence has not been performed, or
2. The request key has not been operated, or
3. No program-controlled operation is in progress, or
4. No status is outstanding for the PR-KB.

Chaining Check (CSW Bit 47): This bit does not apply to PR-KB operations.

Sense Byte For Printer-Keyboard

The PR-KB sense byte is kept in control storage. Unit check status is set whenever any one or more of the following bits are set.

Command Reject (Sense Bit 0): This bit is set on if a command not defined for the PR-KB is issued.

Intervention Required (Sense Bit 1): This bit is set on only for a read or write command in which:

1. The not-ready switch has been operated to place the PR-KB in a not-ready condition, or
2. The forms switch indicates that the PR-KB requires forms.
3. The 3215 cover is not closed.
4. AC power is off in the 3210 Model 2.

Bus Out Check (Sense Bit 2): This bit is not set for PR-KB read operations.

Equipment Check (Sense Bit 3): This bit is set on:

1. When *even* parity is detected on a character code sent from the PR-KB to the CPU during a read operation.
2. If the printer fails to print.
3. If the 3215 printer had a print-sync check or incorrect data from the keyboard.

Sense Bits 4-7: These bits are not set for PR-KB operations.

SUGGESTED RESTART PROCEDURES FOR PRINTER-KEYBOARD

An I/O error causes an interruption condition, which is indicated in the CSW. The CSW is located in main-storage locations 40 through 47 (hexadecimal). Bit 38 of the CSW, when on, indicates a unit-check condition. This is bit 6 of the byte at main-storage address 44 (hexadecimal).

When a PR-KB unit check is detected by the program, a sense command should be executed for the PR-KB. Sense information sent from the attachment provides more detailed information concerning the cause of the unit check. As a result of program analysis of the sense information, an error message should be made available to the operator to indicate the condition.

The following information describes the actions that should be performed when the program detects unit-check status in the CSW. The actions are related to particular sense indications that can occur. These bits are analyzed by the program.

Command Reject (Sense Bit 0): Provide an operator message and exit from this error-recovery procedure. Command reject indicates that an invalid command was received at the PR-KB attachment.

Intervention Required (Sense Bit 1): The PR-KB enters a not-ready condition (intervention-required light on) because one of the following has occurred.

1. The not-ready key was operated to place the PR-KB in a not-ready condition.
2. The PR-KB has run out of forms.
3. The PR-KB cover is open.
4. The ac power switch in the 3210 Model 2 is off.

Programs should include an operator message to remedy the problem.

Equipment Check (Sense Bit 3): Provide an operator message to indicate failure to read the input message and do one of the following:

1. If there is no additional error-recovery procedure, continue operation but consider the PR-KB inoperative.
2. If there is an additional error-recovery procedure defined, exit to it. If the additional error recovery procedure fails, continue the operation but consider the PR-KB inoperative.

If equipment check is set because of bad parity from the keyboard, the operation is not terminated until its normal ending point.

If equipment check is set because the printer fails to print (during a read or write operation), the operation is terminated.

Refer to the *IBM System/360 Principles of Operation,* GA22-6821, the *IBM System/370 Principles of Operation,* GA22-7000, or other sections of this manual, for system features not described here. For example, the 1401/1440/1460 Emulator feature is described in a separate section and new instructions are included in the *IBM System/370 Principles of Operation.*

BYTE-ORIENTED OPERAND FEATURE

The byte-oriented operand feature allows the main-storage operands of non-privileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. When operands for word operations are not on word boundaries, or operands for halfword operations are not on halfword boundaries, performance degradation can be expected. This feature does *not* apply to the alignment of instructions or channel command words (CCW's).

CHANNEL-TO-CHANNEL ADAPTER

The channel-to-channel adapter feature provides a path for data transfers between two channels and synchronizes such transfers. This provides systems with interchannel communications.

The channels may be either within the same system or on separate systems. Within one system, an adapter can permit moving blocks of data from one area of main storage to another. Connecting a channel of one system to a channel of another has the effect of interconnecting two CPU's. Only one channel need have the adapter.

The adapter uses one control-unit position on each of the two connected channels.

EXTENDED EXTERNAL MASKING

The extended external masking feature provides for selective masking of interruptions that are caused by timer, interrupt key, and external signals 2 through 7.

Masking is controlled by three subclass mask bits in control register 0, defined as follows.

Timer Mask (T): Bit 24 of control register 0 controls whether the CPU is enabled for a timer interruption. An external interruption caused by the timer value's becoming negative can occur only when both the external mask bit in the PSW *and* the timer mask bit in control register 0 are one. (The T-bit is set to one by system reset.)

Key Mask (K): Bit 25 of control register 0 controls whether the CPU is enabled for interruptions due to a signal from the interrupt key.

An interruption from this source can occur only when both the external mask bit in the PSW and the key mask bit in control register 0 are one. (The K-bit is set to one by system reset.)

Signal Mask (S): Bit 26 of control register 0 controls whether the CPU is enabled for interruption by external signals 2-7. An external interruption resulting from the presence of external signals 2-7 can occur only when the external mask bit in the PSW and the signal mask bit in control register 0 are one. (The S-bit is set to one by system reset.)

DIRECT CONTROL

The direct control feature includes two instructions (read direct and write direct) and six external interruption lines. The read and write instructions transfer a single byte of information between an external device and main storage. Each of the six external signal lines, when active, sets up the conditions for an external interruption. Additional information can be found in the *IBM System/360 Direct Control and External Interrupt Feature, Original Equipment Manufacturers' Information,* GA22-6845.

EXTENDED-PRECISION FLOATING-POINT FEATURE

Both the System/360 Floating Point feature instructions and the Extended-Precision Floating-Point feature instructions are included in this feature. The extended precision instructions can handle extended precision (28-hexadecimal-digit) floating-point operands. Extended-precision operands can also be rounded to long-precision format, and long-precision operands can be rounded to short-precision format. See the *IBM System/360 Principles of Operation,* GA22-6821, for further information.

STORAGE PROTECTION (STORE AND FETCH)

Storage protection (during both storage and retrieval of data and instructions) is standard on the Model 145. The storage-protection feature makes it possible to protect the contents of storage from misuse or inadvertent destruction.

OS/DOS COMPATIBILITY

The OS/DOS Compatibility feature allows execution of DOS programs by emulation while the OS supervisor is controlling the system operation. Refer to the *IBM System/360 OS Program Planning Guide for the DOS Emulator on the System/370,* GC24-5076.

The emulated environment must be a single contiguous block in main storage.

Special instructions are provided to assist the emulation process. The basic operation of the instructions is performed through a microprogram in conjunction with a group of address-assocative hardware registers. These instructions are unique to the OS/DOS compatibility feature, and are intended and supported only for use by the integrated emulator program.

INTERVAL TIMER

The Interval Timer provides program interruption on a program-controlled time basis. Uses of the interval timer include:

- Job accounting
- Monitoring for perpetual program loops
- Time stamping
- Polling at timed intervals.

The storage word at program-storage locations 80-83 (decimal) is reserved for the interval timer feature. Any value stored at this location is automatically reduced by decrementing bit 23 every 3.3 milliseconds, provided the interval-timer switch is in the NORM (normal) position.

The program in process can be automatically interrupted by an external interruption (if PSW system-mask bit 7 is on) when the interval-timer word goes from a *positive* value to a *negative* value. The interruption is identified by setting PSW bit 24 on.

The high-order 24 bits of the interval-timer word are used to provide a full cycle of about 15.5 hours. The interval-timer bit values are:

Timer Bit	*Hex Address*	*Hours*	*Min.*	*Seconds*
0	50	7	45	17.287424
1		3	52	38.643712
2		1	56	19.321856
3			58	9.660928
4			29	4.840464
5			14	32.415232
6			7	16.207616
7			3	38.103808
8	51		1	49.051904
9				54.525952
10				27.262976
11				13.631488
12				6.815744
13				3.407872
14				1.703936
15				.861968
16	52			.425984
17				.212992
18				.106496
19				.053248
20				.026624
21				.013312
22				.006656
23				.003328

Note: Actual values may vary slightly according to the resolution of the timing method but will never be off more than 3.3 milliseconds of the stated value. However, the timer interruption could be later than expected, depending upon the system operation in progress.

Interval Timer Switch

When the interval-timer switch is set to the NORM position, the value stored in the interval-timer word is automatically decremented immediately after being stored.

When the switch is in the DSBL position, no decrementing of the interval-timer word takes place. The four bytes may be used for normal program applications.

TIME-OF-DAY CLOCK FEATURE

The Time-of-Day Clock provides an accurate measure of time, independent of system events or activities (except power-off), and makes measurement available for programming applications. When system power is turned off, the clock value is lost. Once the time-of-day clock has been made operational through the Set Clock instruction and the TOD CLK switch, it maintains a constant rate of increase. The full cycle of the clock is about 143 years. This timing operation is *not* affected by:

- Any normal activity or event in the system
- Wait state
- Stopped state
- Instruction-step mode
- Single-cycle mode
- Test mode*
- System reset
- Initial program load procedure.

*The clock value is lost when the time-of-day clock micro-diagnostic tests are being performed, or when system power is turned off.

The time-of-day clock is an internal doubleword binary counter. Time is measured by incrementing bit position 51 by one every microsecond, following the rules for fixed-point arithmetic. When the clock is being set, bits 52 through 63 of the designated doubleword value are ignored and are not used as part of the clock value. When the clock value is stored, bits 52 through 63 of the clock value are automatically zeroed.

TIME-OF-DAY CLOCK INSTRUCTIONS

The clock value can be accessed by the Store Clock instruction. It causes the current clock value to be stored in a program-storage location specified by the instruction.

The clock can be set to a specific value by the privileged Set Clock instruction. It causes the current clock value to be replaced by the value specified in the instruction. The Set Clock instruction changes the clock value only when the TOD CLK switch is in the enable position.

WORD BUFFER

The channel word-buffer feature increases the efficiency of the system because it permits the assembly of up to four bytes of data before requiring a share cycle to transfer the data. Thus the channel speeds and the CPU throughput are greatly improved.

Note: Data transfers on the interface are still one byte at a time, but the number of data accesses to main storage are fewer.

The word-buffer feature, if ordered, is effective on all attached selector and block-multiplexer channels.

When operating with the recommended IBM operating system programs, the system requires disk-file storage for handling its programming sequences. Because of the data-handling speed of the system, the disk files should have the capability of the IBM 2314 A-Series Direct Access Storage Facility (DASF). As an alternative to placing a 2314 A-Series on the selector channel, the Integrated File Adapter (IFA) feature with the IBM 2319 Disk Storage Facility is available for the system. Three access mechanisms are included. Up to five additional access mechanisms (combinations of IBM 2312, 2313, and 2318 units) may be attached (for a total of eight).

For simplicity, the term *IFA* has been used in this manual to mean both the IFA control and the attached access mechanisms.

The IFA feature is assigned exclusive use of selector channels 1 and 4. Only selector channels 2 and 3 are available when the IFA feature is installed.

This manual covers only the highlights of the IFA and the attached DSF units. Details of the disk-storage record formatting, the commands, and the general operation for the IFA are the same as for the 2314 A-Series. These are given in the *IBM System/360 Component Descriptions, IBM 2314 Direct Access Storage Facility and IBM 2844 Auxiliary Storage Control,* GA26-3599.

IFA CHARACTERISTICS

Capacity

The IFA control can accommodate from one to five disk-storage access mechanisms in addition to the first three (which are included as part of the IBM 2319). No provision is made for the ninth or spare access mechanism provided by the 2314 Model A1. When fewer than eight access mechanisms are required for operation, one access mechanism may be made a spare by setting the address plug for on-line servicing. On-line service provisions are the same as for the 2314 Model A1. The IFA DSF's (after the first three) may be any combination of the following:

2312 Disk Storage Model A1 – 1 access mechanism
2313 Disk Storage Model A1 – 4 access mechanisms
2318 Disk Storage Model A1 – 2 access mechanisms

Data Rates

The IFA data-transfer rate is 312,000 bytes per second. See the integrated file adapter information in the *Timings* section.

IFA Compared to 2314 A-Series

The IFA offers a more compact system than the use of the 2314 connected to a channel. This should offer great advantage when the application-program requirements for selector-channel connection of other I/O equipment do not exceed the capability of channels 2 and 3. The same restrictions that apply to the 2314 Model A1 apply to the IFA operation. Only one of the disk-storage modules can be operated at a time.

IFA Limitations

The disk-storage units connected to the IFA are limited to the single control unit and single channel operation. The IBM 2844 Auxiliary Storage Control, the Word Buffer feature, the Channel-to-Channel Adapter, the Block Multiplexer Channel feature, and the Two Channel Switch feature do not apply to the IFA.

The Scan feature and the Record Overflow feature are standard with the IFA feature. In disk-storage-oriented application programs where other features are required, a 2314 A-Series should be connected to a selector channel.

The IFA control unit makes use of the CPU controls on a high-priority basis for sequencing the disk-storage operations. The time required for this control is in part offset by the fact that the IFA does not require time for the channel interface sequence.

DISK-STORAGE CHARACTERISTICS

Disk Pack Storage

Disk-storage devices allow either sequential or random access to records that are stored either sequentially or randomly. The records may be of any length, the only requirements being that the tracks are formatted for the length of records to be stored (and the track and cylinder byte-capacity limits are not exceeded). The length information is stored with the location identifier at the start

of each record for use in subsequent operations. The disk packs may be interchanged between the access mechanisms connected through the IFA and any other 2314 for either reading or writing.

The stored data can be protected during an operation by setting a mask byte with the file-mask command. One portion of the mask defines to what extent seek commands to select different areas of the file may be executed. The second portion of the mask defines to what extent write commands may be performed.

The disk pack used with the IFA has 20 recording surfaces each with 200 tracks for record storage, plus three alternate tracks per recording surface. Each track has a capacity of 7,294 bytes. To locate a specific track, a seek command is executed to place the access arm on one of the 200 tracks and to select one of the 20 heads on the access arm. In one position of the access arm, a cylinder of 20 tracks can be processed by changing only the head selection. Each cylinder (20 tracks) has a capacity of 145,880 bytes. In multi-track operations the sequence can advance from track to track without an additional seek command.

Track Format

All reference to position on the track is from a common index point (Figure 7). A home-address identification of the track is written first. Following the home address, record zero (R0) is written with operating system information in IBM-recommended programs. In other programming systems this area can also contain an application record. The remainder of the track contains application records numbered R1 through Rn. The start of each record is identified with an address marker.

Each record consists of at least a count field and a data field. It may also contain a key field between the count and data fields. The count field contains the track flags, the location identifier, and the formatted length of the key and data fields. The key field (when used) normally contains record-oriented identification information that may serve to identify the record. The data field contains the actual application record information. Each of the fields is followed by computed data-check information that is used to prove the accuracy of the data in subsequent operations.

IFA OPERATION

The response to disk-storage instructions and commands is identical to that expected from the same condition with the 2314 A-Series. The following comments abstract the operating conditions of the 2314 A-Series as they apply to the IFA.

Addressing

The IFA is assigned the channel-1 address and is operated through channel instructions and commands. The control unit and device address normally transmitted to the channel to select the channel-connected disk-storage unit is now sent to the IFA. The control-unit address is compared to a stored address to determine that the selection is correct. The device address is used to select the specified module after determining that the module is part of the connected configuration.

Operation Initiation

The channel Start I/O instruction defines the channel, control-unit, and unit addresses for all control and data transfer operations. The Channel Address Word (CAW) provides the address of the first channel command. The IFA determines whether the unit is available and free of pending status conditions before allowing the command to be entered. If the command is invalid or is presented in an improper sequence, the operation is ended immediately with appropriate status indication.

The Test I/O, Halt I/O, and Halt Device instructions can be used with the IFA. These operations are performed and reported in the same manner as for a device on channel.

Data Transfer

Data transfer for the IFA makes use of the share-cycle principle used by the selector channels. A storage cycle is taken between cycles of the current CPU operation for each transfer. The IFA control transfers one byte of data at a time the same as an unbuffered channel.

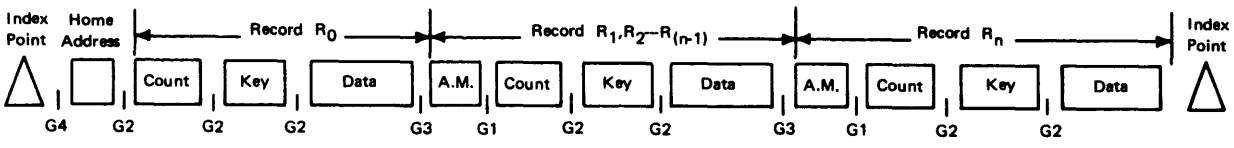


Figure 7. Track Format

Command Chaining

Most disk-storage operations are performed as a sequence of steps defined by a chain of commands in Channel Command Words (CCW's). New commands are obtained from their chained sequences through interruption of the CPU operation the same as for selector channel. A request from the IFA has higher priority than a similar request from either selector or multiplexer channels. In its function as the control unit for the disk-storage modules, the IFA may request more than one interruption for each command.

Ending Status

The final status conditions for an IFA operation are reported through the Channel Status Word (CSW) and the condition code of the Program Status Word (PSW). If a unit-check status is reported, the control unit remains busy until a sense command is executed to obtain the error information. The sense information provides a means of defining the error condition and determining the method of correction. The operating program transmits a message to the operator if the trouble cannot be remedied by its retry sequences. Operations that cannot be initiated because of busy or not-ready conditions are reported through the condition code.

IFA FEATURES

The IFA is capable of the following 2314 A-Series operating features, thus making it compatible in normal operation. The nature of the channel control and the disk-storage interface prohibits the use of dual channel or dual control-unit arrangements.

Scan Feature

The scan feature of the 2314 is a standard feature on the IFA. This feature allows selectively searching the key and data fields of the stored records. The search argument in main storage is compared with the next record for a possible equal or high condition. Chained commands and the multi-track control allow searching all of the records in a cylinder.

Record Overflow Feature

The record overflow feature of the 2314 is a standard feature on the IFA. This feature allows writing a record that extends beyond the end of a track by continuing it on the next track within the cylinder. It can be used for writing records that are longer than the track length or for filling in the areas at the end of the tracks to obtain more storage.

The I/O channels for this System/370 model are, with a few variations, identical to those of System/360 models. For a description of some channel operations, refer to the *IBM System/370 Principles of Operation,* GA22-7000. For details of the standard channel interface, refer to the *IBM System/360 I/O Interface--Channel to Control Unit Original Equipment Manufacturers' Information,* GA22-6843.

For information about I/O devices attaching to the Model 145 interface, refer to *IBM System/370 I/O Configurator,* GA22-7002.

This section covers the basic characteristics and defines the limitations and additional capabilities of the I/O channels. The additional capabilities include new and redefined instructions, new interface lines, the block-multiplexer channel, and other extensions to System/360 provided by System/370.

This system offers the following channel configurations.

1. A single byte-multiplexer channel.
2. Selector channel 1 or Integrated File Adapter (IFA) with 2319 Disk Storage Facility (DSF) addressed as selector channel 1. The IFA, and selector channels 1 and 4, are mutually exclusive.
3. Selector channels 2, 3, and 4 for non-IFA configurations; selector channels 2 and 3 for IFA configurations; a block-multiplexer channel in place of any installed selector channel; and the word buffer feature on all (non-IFA) selector or block-multiplexer channels. (Also refer to the *Channel-to-Channel Adapter* section.)

The byte-multiplexer channel can operate in either byte or burst mode. The mode is determined by the characteristics of the device operating on the channel. When a device on the byte-multiplexer channel forces burst mode, no other device can operate with the byte-multiplexer channel until the burst-mode operation is completed.

In the byte mode, the single data path of the byte-multiplexer channel can be shared by a number of low-speed I/O devices operating simultaneously. The channel multiplexes data to or from these devices (one device at a time) in groups of bytes as required by the I/O device being serviced.

Selector channels are designed to be used primarily for devices with higher data rates. Operations between a selector channel and an operating I/O unit can be overlapped with CPU processing cycles. The selector channel operates in burst mode only. Only one I/O unit per selector channel can be engaged in the transfer of data at one time. Selector channel accesses to main storage during a data transfer cycle are on a byte basis or, if the word buffer feature is present, on a word basis.

Block multiplexer channels are available instead of selector channels 1, 2, 3, or 4 (only channels 2 and 3 when the IFA feature is installed). The block-multiplexer channel is optimized for relatively high-speed burst operations and can multiplex complete blocks of data. It is particularly suited to buffered or cyclic devices with high data rates (such as disk-storage devices). The multiplexing facility of the block-multiplexer channel allows the interleaved execution of several channel programs by the same channel.

The byte-multiplexer, selector, and block-multiplexer channels operate from the same I/O instruction and command formats used for other System/370 models.

STANDARD I/O INTERFACE

The standard System/360 I/O interface is used to connect the CPU channel to I/O devices or control units. In addition to the standard System/360 I/O interface, extensions to the I/O interface operations are provided.

High-Speed Transfer: This extension to the I/O interface enables data transfer to take place (on selector and block-multiplexer channels) faster than the data rates that would be obtained with service-in and service-out alone. It may also be used by some control units to permit the placement of a control unit at a greater distance from the channel than would otherwise be possible. This extension includes two additional tag lines: data-in and data-out.

Data-in may be alternated with service-in tag line to enable transfer of data at a higher rate than is possible if service-in alone is used. In this case, data-out is alternated with service-out as the response to data-in. Data-out is the response to data-in as service-out is the response to service-in.

I/O Error Alert: A new tag line, disconnect-in, provides (on selector and block-multiplexer channels) control units with the ability to alert the system of a malfunction that prevents the control unit from signaling correctly over the I/O interface.

Disconnect-in can be activated by a control unit only when it is connected to the channel (has operational-in up). The channel performs a selective reset in response to disconnect-in and indicates to the program the occurrence of disconnect-in by causing an I/O interruption.

Command Retry: Command retry is a channel-control unit procedure that can cause a command to be retried without requiring an I/O interruption.

It is a function of the control unit to determine whether the last command can be retried, based on factors such as whether operator intervention or program re-orientation is required before retry.

Command retry applies only to selector and block-multiplexer channels.

INPUT/OUTPUT INTERRUPTIONS

The input/output interruption definition is extended by the addition of a new interruption condition.

Channel-Available Interruption Condition: A channel-available interruption condition is generated by a channel to signify that a previously indicated channel-busy condition no longer exists. Its purpose is to inform the CPU program that the instruction that received a channel-busy indication (condition code 2) can now be expected to be successful.

The channel-available interruption condition is meaningful only for the block-multiplexer channel because a selector channel always terminates a channel-busy condition with an interruption or an interruption-pending condition.

BYTE-MULTIPLEXER CHANNEL

The maximum byte-multiplexer-channel byte-mode data rate is 50,000 bytes per second. The maximum burst-mode data rate is 180,000 bytes per second. Any IFA, selector-channel, or block-multiplexer channel activity reduces the data rate for the byte-multiplexer channel.

The byte-multiplexer channel operations with attached I/O units are implemented under microprogram control. A particular status, data, or control communication with a device is coordinated by the standard-interface signal sequences between the device and the byte-multiplexer channel. Data transfer to or from main storage is on a byte basis only.

The byte-multiplexer microprograms control data flow to and from the CPU, and the functions performed by specific registers that are used for byte-multiplexer channel operations only.

The byte-multiplexer channel contains a number of subchannels, each of which is capable of controlling one I/O device. Each subchannel has its functional control information stored in a four-word Unit Control Word (UCW) that is contained in control storage.

When a byte-multiplexer-channel operation requires use of the information in a UCW, that UCW (identified by the address of the I/O unit involved in the operation) is read from control storage. The operation specified by the UCW is then performed under microprogram control. The UCW is used, updated, and returned to control storage when the operation is completed. Hence the UCW carries a dynamic record of the operation for the I/O device assigned.

There is *one* assigned byte-multiplexer channel area in local storage for use in processing a *single* UCW. Therefore, when the UCW is being set up in that area during execution of an I/O instruction (or I/O interruption operation), service requests from other units on the byte-multiplexer channel are blocked.

Byte-Multiplexer Subchannel Capacity

A maximum of 256 UCW's are available for the byte-multiplexer channel. Sixteen UCW's are provided in the basic machine. At system order time, the number of units on the byte-multiplexer channel is specified for the control-storage (microprogram) load so that an adequate amount of control-storage is reserved. The number of available byte-multiplexer channel UCW's is 16, 32, 64, 128, or 256.

An *unshared* subchannel has a UCW that is reserved for one specified device only. For example, some devices require a UCW for exclusive use; each unit attached to a 2821 Control Unit requires a single UCW for its use. If a 2821 services two 1403 Printers and a 2540 Reader-Punch, four UCW's are required: two for the printers; one for the reader; and one for the punch. Each of these units has its own unique unit address.

A *shared* subchannel has a UCW that can contain operating information for any one of a number of devices, all of which are serviced by the same control unit. The 2821 previously described is in reality four separate control units and is not a shared control unit. An example of a shared control unit is a tape control unit, which can service the requirements of several tape drive mechanisms.

The UCW address in control storage is derived from the unit address.

For most effective use of control storage, and in recognition of the average needs of most applications, UCW's are available in the following configurations:

Standard	-	16 UCW	-	MUA Folding and full SUA Folding*
Options	-	32 UCW	-	MUA Folding and full SUA Folding
	-	64 UCW	-	MUA Folding and full SUA Folding
	-	128 UCW	-	MUA Folding
	-	256 UCW	-	No Folding

MUA: Multi-unit address.
SUA: Single-unit address.
* Folding is discussed under *Device Addressing.*

Device Addressing

Before a command for operation of an I/O device can be sent to its control unit, the device must be addressed. The address is derived from the I/O instruction and consists of the three low-order bytes of the developed address. The interface address (if applicable) is in the high-order byte, the channel address is next, and the device address is in the low-order byte.

MUA (Multi-Unit Addressing) refers to shared subchannels. SUA (Single-Unit Addressing) refers to unshared subchannels. Address folding is done to allow maximum addressing flexibility, while using a minimum amount of control storage. *Folding* means that certain bits in the address byte are ignored; thus several address values are assumed by the system to be identical. Because of this, *full* folding requires discretion in assigning addresses to avoid mutually exclusive addresses. For example, if I/O device 1F (0001 1111) is assigned, another device with address 0F (0000 1111) could not be used because both would address the same UCW.

For a unit-address byte of $A^0A^1A^2A^3A^4A^5A^6A^7$, the addressing scheme is:

Number of UCW's	*Address Bits*	*UCW Addressing Scheme*			
		Unshared Unit Addresses		*Shared Unit Addresses*	
16	A^0	Must be 0	0	Must be 1	1
	A^1-A^3	Not significant ; folding permitted	x	Provides 8 unique control-unit/	
			x	UCW addresses (0-7)	A^1
			x		
	A^4-A^7	Provides 16 unique addresses (00-0F)	A^4		x
			A^5		x
			A^6		x
			A^7		x
32	A^0	Must be 0	0	Same as for 16 UCW's	
	A^1-A^2	Not significant; folding permitted	x		
			x		
	A^3-A^7	Provides 32 unique addresses (00-1F)	A^3		
			A^4		
			A^5		
			A^7		
64	A^0	Must be 0	0	Same as for 16 UCW's	
	A^1	Not significant; folding permitted	x		
	A^2-A^7	Provides 64 unique addresses (00-3F)	A^2		
			A^3		
			A^4		
			A^5		
			A^6		
			A^7		
128	A^0	Must be 0	0	Same as for 16 UCW's	
	A^1-A^7	Provides 128 unique addresses (00-7F), no folding	A^1		
			A^2		
			A^3		
			A^4		
			A^5		
			A^6		
			A^7		
256	A^0-A^7	Provides 256 unique addresses (00-FF), no folding, no shared unit address	A^0	None	
			A^1		
			A^2		
			A^3		
			A^4		
			A^5		
			A^6		
			A^7		

If any *shared* subchannel is assigned, no unit using an *unshared* subchannel can have its high-order address bit set to a 1. The byte-multiplexer channel microprogram routines recognize the high-order 1 as specifying a unit on a shared subchannel. In this case, any unit address of the form 1xxxxxxx is recognized as a shared subchannel.

When a unit address specifying a shared subchannel is recognized by the byte-multiplexer-channel microprogram routines, these routines reset the high-order bit to access one of UCW's 0 through 7.

Therefore, as far as UCW usage for shared subchannels is concerned, only bits 0-3 of the unit address are used to specify the UCW. For example, the shared control unit address 1000xxxx pertains only to UCW zero. (The x's specify the particular unit being controlled by the shared control unit.) A maximum of eight shared subchannels (UCW's 0 through 7) can be assigned.

In Summary:

1. If shared subchannels *are* used, unshared subchannels are restricted to:
   a. UCW's 0 through 7 that are *not* used as shared subchannels, and
   b. UCW's that are specified by unit addresses in which the high-order bit is at a value of 0.
2. If shared subchannels *are not* used, the number of unshared subchannels can be a maximum of 256 (0 through 255), but the actual number and types used must be established during ordering so that the microprogram load can be set up properly.

The number of subchannels used is also dependent upon the characteristics of the devices on the channel, as pointed out in the following description.

The electrical characteristics of the channel allow for up to eight I/O control-unit positions, connected serially. Positions for units on the I/O interface can be thought of in three ways, depending upon the units involved:

1. A single control unit that controls one I/O unit can be connected to the channel. An example of this type of unit is the IBM 1443 Printer Model N1. One control-unit position is needed.
2. A single unit that contains several control units can be connected to the channel. An example is the 2821 control unit, which has separate control units for each attached 1403 printer, one for the 2540 reader section, and one for the 2540 punch section. One control unit position is needed.
3. A single control unit that services the requirements of several I/O units (one at a time) can be connected to the channel. An example is a tape control unit that controls several tape drives. One control-unit position is needed.

Assume, for example, that eight 1443 Model N1 printers are attached to the byte-multiplexer channel. All eight positions are then used, and no other unit can be attached to the channel. Any eight of the subchannels could then be used for the printers, according to the device address.

As a second example, assume that eight shared control units, each controlling eight I/O units, are connected to the byte-multiplexer channel:

1. Eight positions are required for the eight control units.
2. Eight UCW's (0-7) are required, one for each shared control unit.
3. No other positions are then available.

SELECTOR CHANNELS

The selector channels are designed primarily for use with devices that have high data rates, such as magnetic tape, drum storage, and disk-storage units. From one to four selector channels are available.

Average data rates are dependent upon whether or not the word buffer feature is installed, and upon the number of channels in use. The maximum data rate possible with the word buffer installed is 1.85 million bytes per second. The maximum data rate without the word buffer feature is 820,000 bytes per second.

Selector channels 1, 2, 3, and 4 are available for non-IFA configurations, and selector channels 2 and 3 are available for IFA configurations.

Selector channels are capable of controlling one operation at a time. Each operation is performed in burst mode; the other devices on a selector channel cannot be operated during this period. (See the *Block Multiplexer Channels* section for expansions of selector-channel capability.)

Circuitry registers, and special microprogram routines in control storage, are used to perform selector-channel operations. The selector channels do not require a group of UCW's to retain channel-operating data because only one operation can be performed at a time. The operating data remains in the operating registers in local storage. This results in a faster data access for data on selector channels than on the byte-multiplexer channel.

When a selector channel is operating, the data is transferred byte by byte as requested by the device. When a selector channel is operating within its maximum speed, there is time between byte transfers to allow for CPU processing and operating the integrated I/O devices.

Selector-channel service requests are used for data-transfer and skip operations but are not used for status transfer. A service-request operation is initiated by a request from the channel that required service.

The four selector-channel service-request operations provide for the following functions (non-IFA option).

1. *Skip (Read)*: The current CCW count is decremented by 1 for each Skip service request. The address portion of the CCW is not changed, and no data is transferred into or from main storage.

2. *Input Backward (Read Backward):* The current CCW count is decremented by 1, and the address portion of the current CCW is decremented by 1 for each input-backward service request. A data byte is placed into storage at the location specified by the current CCW address before the address update is performed.
3. *Input Forward (Read):* The current CCW count is decremented by 1, and the address portion of the current CCW is incremented by 1, for each input-forward service request. A data byte is placed into storage at the location specified by the current CCW address before the address update is performed.
4. *Output (Write):* The current CCW count is decremented by 1, and the address portion of the current CCW is incremented by one for each output service request. A data byte is taken from the main-storage location specified by the current CCW address before the address update is performed.

Only one service request can be in progress at a time. The channel obtaining service determines which area will be accessed for protect key, count, and data-address information.

No selector channel can obtain action for a service request in the machine cycle immediately following a service request for that same channel. Also, each channel is guaranteed that no other channel may have more than one request serviced when a service request is outstanding for another channel. For example, suppose channels 2, 3, and 4 simultaneously request service. Channel 2 is serviced first because it has the highest priority. Channel 3 is serviced next, but during the channel 3 activity, channel 2 initiates another service request. The channel 4 request will be serviced next because its request has been pending the longest time. Channel 2's second request is now serviced.

Device Addressing

The selector-channel addresses are 01-04. Device addressing on the selector channel may be any of the 256 possible bit combinations of a byte and may be assigned as required by the program for the selector-channel devices.

BLOCK-MULTIPLEXER CHANNELS

A block-multiplexer channel is available instead of an installed selector channel. The block-multiplex mode allows concurrent operation of many I/O devices on a channel by multiplexing blocks of data on the channel's single data path.

Although only one device may actually be transmitting data at any given instant, multiple channel programs may be concurrently active.

Block multiplexing involves temporarily disconnecting an operation in a sequence of chained channel commands. This frees the channel during non-data transfer activity of the device, thereby allowing other devices access to the channel during this time. The block-multiplexer channels would normally attach I/O equipment that has high data rates.

Block-Multiplexer Channel UCW Assignments

The 256 possible device addresses on a block-multiplexer channel are divided into 32 device address groups of 8. Each block-multiplexer channel has a UCW address table with a halfword entry for each device address group. The halfword entry in the table translates the actual UCW addresses from the device addresses as needed.

Each device address group is one of three types according to the UCW requirements of the devices that are to be attached. All devices in a group *must* have the same UCW requirements. The three types are as follows.

Type 1: *Each* device of the group requires an *unshared* UCW,
Type 2: *All* the devices of the group use the same *shared* UCW, or
Type 3: A UCW is *not* to be assigned for *any* device address of the group, and the devices are not allowed to operate in block-multiplexer mode.

All the devices on a shared control unit *must* use the same UCW and *may* require several Type 2 device address groups. Because each shared UCW requires a UCW plus one byte, a group of 8 UCW's provides 7 shared UCW's. The eighth UCW in a group provides the extra bytes required for the 7 shared UCW's. Thus, in theory, one channel could operate with up to 256 devices on one shared UCW, or 256 unshared UCW's could be used to operate 256 devices. These are not intended as typical examples but are given merely to illustrate the flexibility of UCW assignment.

The type of each device address group and the listing of the Type 2 address groups that are to use the same UCW must be specified at order time so that the UCW address tables can be formed for the IMPL disk. In addition, an estimate of the number of UCW's required for unshared (Type 1) operation is necessary so that the size of the UCW pool can be set realistically. Unshared UCW's are assigned dynamically during the first successful Start I/O operation to any device of the group, if there are UCW's available to be assigned. This assignment remains until the next IMPL or other action that results in a system reset.

If a Start I/O with a Type 1 device address that has not had a UCW assigned is attempted on an available channel and no UCW's are available, the result is a condition code 3 setting.

The method used for dynamic UCW allocation of Type 1 devices allows flexibility in reassignment of a device from

one channel to another. A Type 2 device may also be moved to another channel *if* a shared UCW is provided for the other channel(s) at order time.

Address Tables

For a device of $d^0d^1d^2d^3d^4d^5d^6d^7$, the 5 high-order bits are manipulated by the microprogram to access a particular table entry address. Because only the 5 high-order bits are significant, 32 unique table entries result from a possible 256 device addresses. This gives 32 groups of 8 device addresses per group. Each channel has an address table.

To execute programs written for the IBM 1401, 1440, and 1460 systems, or the 1410 and 7010 systems, this system uses both the emulator programming support (in OS or DOS) and the applicable emulator feature. Programs for the emulated system normally can be executed without modification, provided the original program was written in accordance with established IBM procedures and practices.

In the following text the term *1400* refers to the 1401/1460, 1440 systems, and the term *1410* refers to the 1410/7010 systems.

EMULATOR PROGRAMMING SUPPORT

The emulator programming support for 1400/1410 emulation depends upon:

- The user's operating system (OS or DOS).
- The system being emulated (1401/1460, 1440, or 1410/7010).

The emulator programming support has the following characteristics.

- It requires the host (emulating) system to have the applicable version of the emulator feature installed.
- It uses the standard System/370 instruction set, plus the special instructions of the emulator feature (which are defined in the Emulator Program publications).

All phases of 1400/1410 emulation are controlled by the emulator programming support, including:

- All 1400/1410 CPU operations.
- All 1400/1410 input/output operations.
- 1400/1410 operator console operations.
- Error handling.
- System operator messages.

This System/370 model has two emulator features available:

- IBM 1401/1460, 1440 Emulator Feature–for use with the OS or DOS emulator program in the emulation of a 1401, 1460, or 1440 system.
- IBM 1401/1460, 1440, and IBM 1410/7010 Emulator Feature–for use with the OS or DOS emulator program in the emulation of a 1401, 1440 1460, 1410, or 7010 system.

The corresponding emulator feature is required for the execution of the emulator programming support. It consists of a set of special instructions that perform some of the most frequent and more complex functions of the system being emulated. These instructions are supported only for use with these programs. The instructions do not require that the CPU be in a special emulation mode.

Emulator Feature Instructions

Each of the emulator features consist of the following instructions. The difference is in the instruction's ability to perform the functions described for the 1401/1460, and 1440 systems only or for both the 1401/1460, 1440 and the 1410/7010 systems.

- Do Interpretive Loop (DIL): fetches the 1400/1410 instruction, updates the simulated A- and B-storage address registers, index addresses if needed, verifies addresses, updates the simulated I-storage address register, and returns control to the emulator program at a routine to execute the 1400/1410 instruction.
- Branch and Do Interpretive Loop (BDIL): places the address from the simulated A-storage address register into the simulated I-storage address register and then enters into the DIL routine.
- Add Numeric (ANUM): performs the 1400/1410 decimal add or subtract. All arithmetic functions are performed except multiply and divide.
- Compare (COMP): executes the 1400/1410 compare function and sets simulated high, low, and equal indicators.
- Move Data in CPU (MCPU): moves data in simulated 1400/1410 storage.
- Move Data for Input/Output (MIO): moves data from simulated 1400/1410 storage to the buffer area and vice versa for input/output operations. Data is translated to EBCDIC for output or to internal code on input.
- Branch If Address Flaged (BIFLAG): tests whether the simulated B- and A-storage address registers contain valid addresses. An invalid address returns control to the emulator program at an error routine. Valid addresses cause processing to continue at the next sequential System/370 instruction.

Note: Abbreviations within parentheses (such as MIO) are *not mnemonics* for coding the instructions but are used as easy reference to the instructions in emulation publications.

INSTRUCTION TIMINGS

The accompanying tables give average instruction timings in microseconds for CPU and input/output operations. All timings for instructions that include reference to main storage include the time required for base-register addition in the address formation.

Note that the instruction timings are dependent upon a number of factors: storage-unit timing capabilities; circuit timings; and logic optimization. Changes to any of these areas can result in a change in the instruction timings listed in this section.

Interference attributable to operations of channels or the integrated file adapter is not included in these timings.

If timings for index-register addition are desired (for RX formats), 0.248 microsecond must be added to the compute time.

These instruction times have been obtained by assuming that on the average the instruction buffer must be filled half the time for the Next Sequential Instruction (NSI). The timings, in effect, assume that the average NSI is 4 bytes in length. The actual times for the instruction buffer loading are as follows:

	Actual Time	*Time Included in Average*
1. Branches		
A. Branch Unsuccessful		
(All of NSI in buffer):	None	.422
(part of NSI in buffer):	.743	.422
(none of NSI in buffer):	.945	.422
B. Branch Successful		
(Double Fetch Required):	.743	.183
2. Other Operations		
A. All RR Format:	.540	.270
B. RX (No operand fetch):	.293	.147
RX (operand fetch):	.090	.045
C. All RS or SI format:	.293	.147
D. SS (Not followed by another SS on a word boundary internal to doubleword):	.293	.147
SS (*Does* end on a word boundary internal to doubleword; followed by another SS):	.743	None

For the decimal instructions, the first-operand field length (N^1) is assumed to be greater than, or equal to, the length of the second operand field (N^2).

Instruction Timing Formula Legend

Symbol	*Definition*
D	Number of digits shifted.
CR	Number of control registers loaded or stored.
E	Time for the subject instruction that is executed by the Execute instruction.
F^1	1 if the branch operation is successful; 0 otherwise.
F^2	0 if the R^2 field specified in the RR formatted branch instruction is zero (that is, the branch is suppressed); 1 otherwise.
GI	Number of interruptions that occur during instruction execution.
GR	Number of general-purpose registers loaded or stored.
H^5	Number of high-order leading zero bytes in the decimal field (that is, source or resulting destination)
H^6	Number of high-order leading zero bytes in the binary field.
K	Constant depending upon mask M3:

M3	*Constant*
0000	0.5
xxx1	4
xx10	3
x100	2
1000	1

In compare logical, the value of these constants in the maximum value. When a unequal comparison occurs before all bits are examined, the constant is equal to the number of bits that had been examined when the unequal comparison occurred.

MK	Number of times the mark address is stored in the Edit and Mark instruction.
N	Total number of bytes in the first operand for those instructions with a single length field.
N^1	Total number of bytes in the first operand (destination).
N^2	Total number of bytes in the second operand (source).
N^4	Total number of field-separator characters in the edit pattern.
N^7	Total number of significance starter characters in the edit pattern.
N^8	Total number of digit-select characters in the edit pattern.
N^9	Total number of bytes of the first operand that lie outside that part of the field bounded by words.
NB	Absolute value of (NM+NP)/256, which is the total number of bytes moved or compared, divided by 256. Any remainder is ignored.
NM	Number of bytes (not pad characters) moved or compared.
NP	Number of pad characters moved or compared.
$NWBL^1$	Number of word-boundary crossovers for the first operand.
$NWBL^2$	Number of word-boundary crossovers for the second operand.
SG	Number of signs in the field to be edited.
T^1	1 if the result field is recomplemented (that is, changes sign); 0 otherwise.
TI	Time taken by interruptions.
V^5-V^8	Legends V^5 through V^8 are for use in the timing formula of the Move instruction, depending upon the locations of the operand fields.

- V^5 Use if the first and second operand fields start and end on word boundaries.
- V^6 Use if the first and second operand fields start at corresponding byte addresses within words but do not lie on word boundaries.
- V^7 Use if the first and second operand fields do not start at corresponding byte addresses within words.
- V^8 Use if the first and second operand fields start on word boundaries but do not end on word boundaries. N must be greater than 4 to use this case.

Note: A byte address of a word can have a value of 0, 1, 2, or 3.

* Indicates that the instruction has a double indexing capability.
\# Indicates that timings have been weighted to provide realistic estimates for actual values that could be expected in typical applications.

Instruction	*Format*	*Op Code*	*Mnemonic*	*Time in Microseconds*
add	RR	1A	AR	1.373
add*	RX	5A	A	2.138
add decimal	SS	FA	AP	$8.757 + 0.744\ N^1 + 1.375\ NWBL^1 + 0.540\ NWBL^2 + T^1$ $(3.044 + 0.451\ N^1 + 1.127\ NWBL^1)$
add halfword*	RX	4A	AH	2.949
add logical	RR	1E	ALR	1.373
add logical*	RX	5E	AL	2.138
add normalized (extended)	RR	36	AXR	12.134#
add normalized (long)	RR	2A	ADR	6.655#
add normalized* (long)	RX	6A	AD	7.523#
add normalized (short)	RR	3A	AER	5.663#
add normalized* (short)	RX	7A	AE	5.847#
add unnormalized (long)	RR	2E	AWR	6.199#
add unnormalized* (long)	RX	6E	AW	6.473#
add unnormalized (short)	RR	3E	AUR	5.204#
add unnormalized* (short)	RX	7E	AU	5.342#
and	RR	14	NR	1.935
and*	RX	54	N	2.700
and	SI	94	NI	2.397
and	SS	D4	NC	$N \leqslant 4 = 6.437 + 1.148 NWBL^1 + 0.540\ NWBL^2 + 0.405N$ $N > 4 = 6.740 + 1.148 NWBL^1 + 0.540\ NWBL^2 + 0.203N$
branch and link	RR	05	BALR	$1.682 + 0.874F^1$
branch and link*	RX	45	BAL	2.399
branch on condition	RR	07	BCR	$0.872 + 0.875F^1$
branch on condition*	RX	47	BC	$0.917 + 0.875F^1$
branch on count	RR	06	BCTR	$1.074 + 1.078F^1$
branch on count	RX	46	BCT	$1.369 + 0.873F^1$
branch on index high	RS	86	BXH	$2.469 + 0.875F^1$
branch on index low or equal	RX	87	BXLE	$2.469 + 0.875F^1$
compare	RR	19	CR	1.676
compare*	RX	59	C	2.441
compare decimal	SS	F9	CP	$8.577 + 0.451N^1 + 0.789NWBL^1 + 0.540NWBL^2$
compare halfword*	RX	49	CH	2.949
compare logical	RR	15	CLR	1.373
compare logical*	RX	55	CL	2.138
compare logical	SI	95	CLI	1.784
compare logical	SS	D5	CLC	$N \leqslant 4 = 3.494 + 0.540\ (NWBL^1 + NWBL^2) + 0.405N$ $N > 4 = 3.994 + 0.540\ (NWBL^1 + NWBL^2) + 0.203N$
compare logical characters under mask	RS	BD	CLM	$2.194 + 0.405K + 0.540NWBL^2$
compare logical (long)	RR	0F	CLCL	7.503 +1.900 (NM/4) +1.350 (NP/4) +4.850NB +7.850GI+TI
compare (long)	RR	29	CDR	7.000#
compare (long)*	RX	69	CD	7.869#
compare (short)	RR	39	CER	5.803#
compare (short)*	RX	79	CE	5.992#
convert to binary*	RX	4F	CVB	$37.542\text{-}3.85H^5$
convert to decimal*	RX	4E	CVD	$55.914\text{-}11.925H^6$
diagnose	SI	83	—	Varies depending upon function

Instruction	*Format*	*Op Code*	*Mnemonic*	*Time in Microseconds*
divide	RR	1D	DR	34.183
divide*	RX	5D	D	34.771
divide decimal	SS	FD	DP	$11.044 + 1.110N^1 - 2.550N^2 + (N^1 - N^2)\ [28.500 + 6.378\ (N^2 + 1)]$
divide (long)	RR	2D	DDR	88.190
divide (long)*	RX	6D	DD	89.565
divide (short)	RR	3D	DER	27.862
divide (short)*	RX	7D	DE	28.702
edit	SS	DE	ED	$4.376 + 1.984N + 0.203N^4 + 1.162\ (N^7 + N^8) + 0.950SG$
edit and mark	SS	DF	EDMK	$4.376 + 1.984N + 0.203N^4 + 1.162\ (N^7 + N^8) + 0.950SG + 0.203MK$
exclusive or	RR	17	XR	1.373
exclusive or*	RX	57	X	2.138
exclusive or	SI	97	XI	2.397
exclusive or	SS	D7	XC	$N \leq 4 = 6.437 + 1.148NWBL^1 + 0.540NWBL^2 + 0.405N$ $N > 4 = 6.740 + 1.148NWBL^1 + 0.540NWBL^2 + 0.203N$
execute*	RX	44	EX	2.979+E
halt device	SI	9E	HDV	See Channels, IFA, and PR-KB timings at the end of this section.
halt I/O	SI	9E	HIO	See Channels, IFA, and PR-KB timings at the end of this section.
halve (long)	RR	24	HDR	5.080
halve (short)	RR	34	HER	4.208
insert character*	RX	43	IC	1.384
insert characters under mask	RS	BF	ICM	$2.800 + 0.405K + 0.540NWBL^2$
insert storage key	RR	09	ISK	2.183
load	RR	18	LR	0.923
load*	RX	58	L	1.688
load address	RX	41	LA	1.452
load and test	RR	12	LTR	1.373
load and test (long)	RR	22	LTDR	2.210
load and test (short)	RR	32	LTER	1.980
load complement	RR	13	LCR	1.575
load complement (long)	RR	23	LCDR	2.210
load complement (short)	RR	33	LCER	1.980
load control	RS	B7	LCTL	4.071 +2.205CR +factor from load control register table.
load halfword*	RX	48	LH	2.295
load (long)	RR	28	LDR	1.779
load (long)*	RX	68	LD	2.633
load multiple	RS	98	LM	3.621 +0.945GR
load negative	RR	11	LNR	1.676
load negative (long)	RR	21	LNDR	2.210
load negative (short)	RR	31	LNER	1.980
load positive	RR	10	LPR	1.676
load positive (long)	RR	20	LPDR	2.210
load positive (short)	RR	30	LPER	1.980
load PSW	SI	82	LPSW	8.145
load rounded (extended operands, long result)	RR	25	LRDR	4.140
load rounded (long operands, short result)	RR	35	LRER	3.488
load (short)	RR	38	LER	0.923
load (short)*	RX	78	LE	1.688

Instruction	*Format*	*Op Code*	*Mnemonic*	*Time in Microseconds*
move	SI	92	MVI	1.249
move	SS	D2	MVC	$N \leq 4 = 5.728+0.608NWBL^1 + 0.540\ NWBL^2 +0.681N$ $N>4, V^5 = 6.500 +0.287N$ $N>4,V^6 = 6.028 +0.608\ NWBL^1 + 0.540NWBL^2 +0.203N^9$ $N>4,V^7 = 6.028 +0.608NWBL^1 +0.540NWBL^2 +0.203N$ $N>4,V^8 = 6.838 +0.608\ NWBL^1 +0.540NWBL^2 +0.203N^9$
move long	RR	0E	MVCL	7.153 +1.750 (NM/4) +1.400 (NP/4) +4.850NB +7.850GI+TI
move numerics	SS	D1	MVN	$N \leq 4 = 6.032 +1.103NWBL^1 +0.540NWBL^2 +0.405N$ $N>4 = 6.335 +1.102NWBL^1 +0.540NWBL^2 +0.203N$
move with offset	SS	F1	MVO	$2.609 +1.000N^1 +0.750N^2$
move zones	SS	D3	MVZ	$N \leq 4 = 6.032 +1.148NWBL^1 +0.540\ NWBL^2 +0.405N$ $N>4 = 6.335 + 1.148NWBL^1 +0.540\ NWBL^2 +0.203N$
multiply	RR	1C	MR	19.929
multiply*	RX	5C	M	20.077
multiply decimal	SS	FC	MP	$18.955 + (N^1-N^2)\ [16.000 +4.444\ (N^2+1)]$
multiply halfword*	RX	4C	MH	10.508
multiply (extended operands, extended result)	RR	26	MXR	181.645
multiply (long)	RR	2C	MDR	44.864
multiply (long)*	RX	6C	MD	45.673
multiply (long operands, extended result)	RR	27	MXDR	51.795
multiply (long operands, extended result)*	RX	67	MXD	52.769
multiply (short)	RR	3C	MER	16.071
multiply (short)*	RX	7C	ME	16.795
or	RR	16	OR	1.373
or	RX	56	O	2.138
or	SI	96	OI	2.397
or	SS	D6	OC	$N \leq 4 = 6.437 +1.148NWBL^1 +0.540NWBL^2 +0.405N$ $N>4 = 6.740 +1.148NWBL^1 +0.540NWBL^2 +0.203N$
pack	SS	F2	PACK	$2.609 +0.99N^1 +0.619N^2$
read direct	SI	85	RDD	2.361 + time for hold-in to drop
set clock	SI	B204	SCK	6.165
set program mask	RR	04	SPM	1.125
set storage key	RR	08	SSK	2.588
set system mask	SI	80	SSM	5.805
shift and round decimal	SS	F0	SRP	Left shift: 11.946 +0.40N +0.56D Right shift: 12.546 +0.55N +0.35D
shift left double	RS	8F	SLDA	See shift tables
shift left double logical	RS	8D	SLDL	See shift tables
shift left single	RS	8B	SLA	See shift tables
shift left single logical	RS	89	SLL	See shift tables
shift right double	RS	8E	SRDA	See shift tables
shift right double logical	RS	8C	SRDL	See shift tables
shift right single	RS	8A	SRA	See shift tables
shift right single logical	RS	88	SRL	See shift tables
start I/O	SI	9C	SIO	See Channel, IFA, and PR-KB timings at the end of this section.
start I/O fast release	SI	9C	SIOF	Executed as start I/O.
store*	RX	50	ST	1.497
store channel ID	SI	B203	STIDC	5.200

Instruction	*Format*	*Op Code*	*Mnemonic*	*Time in Microseconds*
store character*	RX	42	STC	1.452
store characters under mask	RS	BE	STCM	3.274 +0.603K +0.608NWBL^2
store clock	SI	B205	STCK	5.670
store control	RS	B6	STCTL	4.071 +1.957CR
store CPU ID	SI	B202	STIDP	5.750
store halfword*	RX	40	STH	1.498
store (long)*	RX	60	STD	2.869
store multiple	RS	90	STM	3.566 +1.013GR
store (short)*	RX	70	STE	1.497
subtract	RR	1B	SR	1.575
subtract	RX	5B	S	2.340
subtract decimal	SS	FB	SP	8.757 +0.744N^1+1.375NWBL^1 +0.540NWBL^2+T^1 (3.044+0.451N^1+1.127NWBL^2)
subtract halfword*	RX	4B	SH	2.949
subtract logical	RR	1F	SLR	1.373
subtract logical*	RX	5F	SL	2.138
subtract normalized (extended)	RR	37	SXR	12.134#
subtract normalized (long)	RR	2B	SDR	6.655#
subtract normalized (long)*	RX	6B	SD	7.523#
subtract normalized (short)	RR	3B	SER	5.664#
subtract normalized (short)*	RX	7B	SE	5.841#
subtract unnormalized (long)	RR	2F	SWR	6.199#
subtract unnormalized (long)*	RX	6F	SW	6.473#
subtract unnormalized (short)	RR	3F	SUR	5.204#
subtract unnormalized (short)*	RX	7F	SU	5.342#
supervisor call	RR	0A	SVC	9.553#
test and set	SI	93	TS	2.442
test channel	SI	9F	TCH	See Channel, IFA, and PR-KB timings at the end of this section.
test I/O	SI	9D	TIO	See Channel, IFA, and PR-KB timings at the end of this section.
test under mask	SI	91	TM	1.992
translate	SS	DC	TR	3.472+2.318N
translate and test	SS	DD	TRT	3.872+2.971N
unpack	SS	F3	UNPK	3.591+0.788N^1 +0.923N^2
write direct	SI	84	WRD	1.991
zero and add	SS	F8	ZAP	8.374+0.451N^1+1.285NWBL^1+0.540NWBL^2

Byte-Oriented-Operand Timing Considerations

The foregoing timings assume that operands are on word boundaries for fullword operations (or halfword boundaries for halfword operations). When the operands are *not* on these boundaries, add the following factors to the times given.

Operand Length	*Read Operation*	*Store Operation*
Halfword	0.990	1.553
Fullword	1.350	2.363
Doubleword	2.565	3.523

For Load and Store Multiple functions, the adjustment factors must be added once for each general register involved.

For Store and Store Halfword operations, an additional factor of 0.765 microsecond must be added if the operand address is not on a word or halfword boundary, respectively.

CONSOLE PRINTER-KEYBOARD INSTRUCTION TIMINGS

Operation	*Function*	*Condition Code*	*Time (Microseconds)*
Start I/O	Write	0	19.654
	Read	0	19.248
	Read/Write	1	17.581
	Read/Write	2	6.762
Test I/O	Available	0	11.644
	Channel end has occurred but has not been accepted by the CPU input buffer	1	16.910
	Channel end has been stacked in the device	1	21.638
	Channel end has been accepted by the CPU	1	15.672
	Working	2	6.627
Halt I/O	Interruption pending	0	6.829
	Channel end has not yet occurred	1	18.484
	Not operational	3	12.657

Load Control Register Table

The following timings (in microseconds), required for the complete load operation, must be added to the Load Control op-code timing for the specified control register.

Control Register	*Complete Load Operation*
0	0.608
1-14	0
15	0.810

BYTE-MULTIPLEXER CHANNEL TIMINGS

Maximum byte-multiplexer channel service-request timings (in microseconds) are as follows. These timings do not include the effect of delays due to other system operations.

Byte Mode	14.30*
Burst Mode	5.30*
Command Chain, Burst	19.20*
Command Chain, Byte	31.00*
Data Chain	6.25
Transfer in Channel	2.00

*To these timings, add the appropriate time required for interface delays (refer to the *IBM System/360 I/O Interface--Channel to Control Unit Original Equipment Manufacturers' Information,* GA22-6843). Data-transfer modes are described in the *IBM System/360 Principles of Operation*.

The following chart gives maximum byte-multiplexer channel timings (in microseconds) for error-free channel operations for given condition-code settings.

	Condition Code			
	0	*1*	*2*	*3*
Start I/O	26.88*	25.28*	9.53	19.08*
Test I/O	17.23*	25.83*	11.98	12.53*
Halt I/O	9.38	19.73*	----	12.53*
Halt Device	10.38	19.73*	10.58	12.53*
Test Channel	2.88	2.88	----	----

*To these timings, add the appropriate time required for interface delays.

Shift Tables (Timings in Microseconds)

Bits	*SLDA*	*SLA*	*SLDL*	*SLL*
0	5.300	5.000	2.950	2.900
1	6.050	5.500	3.700	3.400
2	6.800	6.000	4.450	3.900
3	7.550	7.500	5.200	4.400
4	8.750	7.450	6.400	5.350
5	9.500	7.950	7.150	5.850
6	10.250	8.450	7.900	6.350
7	11.000	8.950	8.650	6.850
8	7.100	6.000	4.750	2.900
9	7.850	6.500	5.500	4.400
10	8.600	7.000	6.250	4.900
11	9.350	7.500	7.000	5.400
12	10.550	8.450	8.200	6.350
13	11.300	8.950	8.950	6.850
14	12.050	9.450	9.700	7.350
15	12.800	9.950	10.450	7.850
16	7.100	6.000	4.750	3.900
17	7.850	6.500	5.500	4.400
18	8.600	7.000	6.250	4.900
19	9.350	7.500	7.000	5.400
20	10.500	8.450	8.200	6.350
21	11.300	8.950	8.950	6.850
22	12.050	9.450	9.700	7.350
23	12.800	9.950	10.450	7.850
24	7.100	6.000	4.750	3.900
25	7.850	6.500	5.500	4.400
26	8.600	7.000	6.250	4.900
27	9.350	7.500	7.000	5.400
28	10.550	8.450	8.200	6.350
29	11.300	8.950	8.950	6.850
30	12.050	9.450	9.700	7.350
31	12.800	9.950	10.450	7.450
32	6.200	5.650	3.850	3.550
33	6.950	6.150	4.600	4.050
34	7.700	6.850	5.350	4.550
35	8.450	7.150	6.100	5.050
36	9.650	8.100	7.300	6.000
37	10.400	8.600	8.050	6.500
38	11.150	9.100	8.800	7.000
39	11.900	9.800	9.550	7.500
40	8.000	6.650	5.650	4.550
41	8.750	7.150	6.400	5.050
42	9.500	7.650	7.150	5.550
43	10.250	8.150	7.900	6.050
44	11.450	9.100	9.100	7.000
45	12.200	9.600	9.850	7.500
46	12.950	10.100	10.600	8.000
47	13.700	10.600	11.350	8.500
48	8.000	6.650	5.650	4.550
49	8.750	7.150	6.400	5.000
50	9.500	7.650	7.150	5.550
51	10.250	8.150	7.900	6.050
52	11.450	9.100	9.100	7.000
53	12.200	9.600	9.850	7.500
54	12.950	10.100	10.600	8.000
55	13.700	10.600	11.350	8.500
56	8.000	6.650	5.650	4.550
57	8.750	7.150	6.400	5.050
58	9.500	7.650	7.150	5.550
59	10.250	8.150	7.900	6.050
60	11.450	9.100	9.100	7.000
61	12.200	9.600	9.850	7.500
62	12.950	10.100	10.600	8.000
63	13.700	10.600	11.350	8.500

Bits	*SLDA*	*SLA*	*SLDA*	*SLL*
0	4.800	4.500	3.200	3.150
1	7.400	6.100	5.800	4.750
2	6.700	5.650	5.100	4.300
3	6.000	5.200	4.400	3.850
4	5.300	4.750	3.700	3.400
5	7.900	6.350	6.300	5.000
6	7.200	5.900	5.600	4.550
7	6.500	5.450	4.900	4.100
8	5.800	5.000	4.200	3.650
9	8.900	6.600	6.800	5.150
10	7.700	6.150	6.100	4.800
11	7.000	5.700	5.400	4.350
12	6.300	5.250	4.700	3.900
13	8.900	6.850	7.300	5.500
14	8.200	6.400	6.600	5.050
15	7.500	5.950	5.900	5.600
16	6.800	5.500	5.200	4.150
17	9.400	7.100	7.800	5.750
18	8.700	6.650	7.100	5.300
19	8.000	6.200	6.400	4.850
20	7.300	5.750	5.700	4.400
21	9.900	7.350	8.300	6.000
22	9.200	6.900	7.600	5.550
23	8.500	6.450	6.900	5.100
24	7.800	6.000	6.200	4.650
25	10.400	7.600	8.800	6.250
26	9.700	7.150	8.100	5.800
27	9.000	6.700	7.400	5.350
28	8.300	6.250	6.700	4.900
29	10.900	7.850	9.300	6.500
30	10.200	7.400	8.600	6.050
31	9.500	6.900	7.900	5.600
32	5.300	4.500	3.700	3.150
33	7.900	6.100	6.300	4.750
34	7.200	5.650	5.600	4.300
35	6.500	5.200	4.900	3.850
36	5.800	4.750	4.200	3.400
37	8.400	6.350	6.800	5.000
38	7.700	5.900	6.100	4.550
39	7.000	5.450	5.400	4.100
40	6.300	5.000	4.700	3.650
41	8.900	6.600	7.300	5.250
42	8.200	6.150	6.600	4.800
43	7.500	5.700	5.900	4.350
44	6.800	5.250	5.200	3.900
45	9.400	6.850	7.800	5.500
46	8.700	6.400	7.100	5.050
47	8.000	5.950	6.400	4.600
48	7.300	5.500	5.700	4.150
49	9.900	7.100	8.300	5.750
50	9.200	6.650	7.600	5.300
51	8.500	6.200	6.900	4.850
52	7.800	5.750	6.200	4.400
53	10.400	7.350	8.800	6.000
54	9.700	6.900	8.100	5.550
55	9.000	6.450	7.400	5.100
56	8.300	6.000	6.700	4.650
57	10.900	7.600	9.300	6.250
58	10.200	7.150	8.600	5.800
59	9.500	6.700	7.900	5.350
60	8.800	6.350	7.200	4.900
61	11.400	7.850	9.800	6.500
62	10.700	7.400	9.100	6.050
63	10.000	6.950	8.400	5.600

SELECTOR-CHANNEL TIMINGS

Selector-Channel Data Rates

Average selector-channel data rates are dependent upon whether or not the word buffer is installed, the number of channels in use, the interface cable lengths, and the number of attached I/O units. These timings ignore any delays due to other system operations. The maximum data rate with the word buffer is 1.85 million bytes per second. The maximum rate without the word buffer is 820,000 bytes per second.

Representative selector-channel data-transfer rates are given below. (*KB* stands for thousands of bytes per second; *MB* stands for millions of bytes per second.)

Selector Channels without Word Buffer			
IFA	*Chnl 2*	*Chnl 3*	
312KB	----	----	
312KB	820KB	----	
312KB	540KB	410KB	
Chnl 1	*Chnl 2*	*Chnl 3*	*Chnl 4*
820KB	----	----	----
820KB	540KB	----	----
540KB	540KB	410KB	----
410KB	410KB	410KB	320KB

Selector Channels with Word Buffer		
IFA	*Chnl 2*	*Chnl 3*
312KB	----	----
312KB	1.85MB	----
321KB	1.85MB	1.2MB

Chnl 1	*Chnl 2*	*Chnl 3*	*Chnl 4*
1.85MB	----	----	----
1.85MB	1.45MB	----	----
1.85MB	1.45MB	1.2MB	----
1.64MB	1.45MB	1.2MB	1.0MB

The preceding rates are dependent upon interface delays.

Maximum selector-channel service-request timings (in microseconds) are as follows.

Command Chain	8.178
Data Chain	7.228
Load UCW	7.600
Store UCW	6.000
Interrupt Condition	7.000

Selector-Channel Timings

The following chart gives maximum selector-channel timings (in microseconds) for condition codes 0 through 3.

	Condition Code			
	0	*1*	*2*	*3*
Start I/O	14.91*	16.61*	5.68	14.40*
Test I/O	9.18*	11.93*	5.93	8.93*
Halt I/O	7.63*	12.68*	8.83*	37.88*
Halt Device	2.90	8.45*	8.30*	4.65*
Test Channel	4.13	3.93*	4.13	2.18

*To these timings, add the appropriate time required for interface delays.

BLOCK-MULTIPLEXER CHANNEL TIMINGS

The following chart gives maximum block-multiplexer channel timings (in microseconds) for condition codes 0 through 3. These timings do not include the effect of delays due to other system operations.

	Condition Code			
	0	*1*	*2*	*3*
Start I/O	18.46*	23.96*	6.08	16.46*
Test I/O	13.43*	17.63*	6.18	12.63*
Halt I/O	7.63*	13.93*	12.23*	40.03*
Halt Device	11.45	20.70*	8.90*	10.60*
Test Channel	4.13	3.93	4.13	2.08

*To these timings, add the appropriate time required for interface delays.

INTEGRATED FILE ADAPTER (IFA) TIMINGS

The following chart gives maximum IFA timings (in microseconds) for given condition-code settings.

	Condition Code			
	0	*1*	*2*	*3*
Start I/O	26.0	25.0	7.4	6.4
Test I/O	13.0	11.4	7.4	6.4
Halt I/O	8.8	10.4	8.6	6.4
Halt Device	6.2	13.0	8.6	6.4
Test Channel	6.0	7.2	7.4	----

Model	*Program-Storage*	*Control-Storage*
3145FED	114,688 bytes (112K)	
3145GE	163,840 bytes (160K)	
3145GFD	212,992 bytes (208K)	See Note 1
3145H	262,114 bytes (256K)	
Note 2	393,216 bytes (384K)	
Note 2	524,288 bytes (512K)	

STANDARD FEATURES

3145 Processing Unit (with Main Power Frame)
112K to 512K Bytes of Program Storage (with ECC)
32K Bytes of Control Storage (with ECC)
Audible Alarm
Byte-Multiplexer Channel
Byte-Oriented Operand
Channel Retry Information
Command Retry
Console File
Error Checking and Correction (ECC)
Extended Channel Logout
Extended External Masking
Extended I/O Masking
Interval Timer
Limited Channel Logout
Machine-Check Handling
Microprogram Instruction Retry
OS/DOS Compatibility
Selector Channel 1 (without IFA) or Selector Channel 2 (with IFA)
Storage Protection (Store and Fetch)
System/370 Commercial Instruction Set
Time of Day Clock

OPTIONAL FEATURES

Additional Byte-Multiplexer-Channel Subchannels (Note 3)
Block-Multiplexer Channels (up to four) (Note 4)
Channel-to-Channel Adapter
Direct Control (with External Interrupt)
Extended Precision Floating-Point Feature
Integrated File Adapter (IFA) (Note 6)
Selector Channels 2, 3, and 4 (without IFA) or Selector Channel 3 (with IFA) (Note 6)
Word Buffer (Note 7)
1401/1460, 1440 Emulation
1401/1460, 1440 and 1410/7010 Emulation
3210 Console Printer-Keyboard Model 1 (Note 5)
3210 Console Printer-Keyboard Model 2 (Note 5)
3215 Console Printer-Keyboard Model 1 (Note 5)
3345 Main Storage Frame Model 1 (Note 2)
3346 Main Storage Frame Model 1 (Note 2)

SELECTIVE FEATURES REQUIRED FOR MINIMUM SYSTEM CONFIGURATION

Selector Channel 1 with a Direct Access Storage Facility (DASF) *or* Integrated File Adapter with IBM 2319 DSF, a Card Reader (or Card Reader/Punch), a 3210 Console Printer-Keyboard Model 1 *or* 3215 Console Printer-Keyboard Model 1, and a line printer.

Note 1: The standard control-storage is 32,768 bytes (32K). The system is equipped with a movable control-storage boundary that allows up to 64K bytes of control storage, depending upon the mix of features installed. These additional control-storage requirements are at the expense of program storage. The storage boundary is set automatically as a function of the Initial Microprogram Load (IMPL) function. Refer to *Control Storage Requirements* for additional information.

Both program and control-storage are equipped with error checking and correction (ECC).

Note 2: Program storage above 256K bytes is contained in the 3345 Main Storage Frame Model 1 (128K additional bytes for 384K bytes total) or the 3346 Main Storage Frame Model 1 (256K additional bytes for 512K total). When either of these units is included, it contains the low-order storage addresses. The 3046 Power Unit is required for either.

Note 3: The byte-multiplexer channel has 16 subchannels that address up to 136 I/O devices (eight shared UCW's can address up to 16 devices each; eight unshared UCW's can address one device each). Up to eight control units can be attached. Configurations with 32, 64, 128, or 256 subchannels are available.

Note 4: A block-multiplexer channel can be ordered in place of any selector channel. Block-multiplexer channels cannot replace selector channels 1 and 4 when integrated file adapter is installed.

Note 5: The 3210 Model 1 and the 3215 Model 1 are mutually exclusive: one is required. The 3210 Model 2 can be used as an auxiliary printer-keyboard (except for alter/display functions).

Note 6: The integrated file adapter, and selector channels 1 and 4, are mutually exclusive. Each selector channel addresses up to 256 I/O devices. Up to eight control units can be attached.

Note 7: The word buffer feature is installed on all selector or block-multiplexer channels or none. The word buffer feature is not available for the integrated file adapter feature.

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