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Systems

**IBM System/370 Model 135
Functional Characteristics**

IBM

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IBM System/370 Model 135 Functional Characteristics

This publication describes the capabilities, features, input/output channels, integrated adapters, and operations of the IBM System/370 Model 135. The information includes the relationship of System/370 Model 135 to the IBM System/360.

The publication is intended for users and potential users (such as systems analysts and programmers) of the System/370 Model 135. The reader is assumed to have a working knowledge of *IBM System/360 Principles of Operation*, GA22-6821, *IBM System/370 Principles of Operation*, GA22-7000, and *IBM System/370 System Summary*, GA22-7001.

IBM

First Edition (March, 1971)

Changes are periodically made to the information herein; before using this publication in connection with the operation of IBM systems, refer to the latest System Library Newsletter, *Accumulative Index of Publications and Programs*, GN20-0360, for the editions that are applicable and current.

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This publication is intended for users and potential users, such as systems analysts and programmers, of the IBM System/370 Model 135 who require information about the capabilities, features, input/output channels, integrated adapters, and operations of this system. The reader is assumed to have a working knowledge of *IBM System/360 Principles of Operation*, GA22-6821, *IBM System/370 Principles of Operation*, GA22-7000, and *IBM System/370 System Summary*, GA22-7001.

In "Introduction", the relationship between System/370 Model 135 and the IBM System/360 is shown, with emphasis on the Model 135 as providing extensions of the System/360 facilities. In "System Structure and Operation", the Model 135 is described in terms of its basic concept, the principal functions, and its units. "CPU Characteristics" and "Input/Output Characteristics" give detailed information on the standard features and optional features of the processing unit, input/output channels, and integrated adapters. These feature descriptions, although principally defining the Model 135, also directly relate the system to System/360 in terms of extended and/or compatible facilities.

Appendix A defines the abbreviations and special terms used in this publication. Appendix B details the Model 135 instruction timings.

Associated Publications

The following publications are referred to in this manual:

1. *IBM System/360 Principles of Operation*, GA22-6821 (see Note).
2. *IBM System/360 DOS – Program Planning Guide for MCAR/CCH Function for IBM System/370 Model 135*, GC24-5089.

3. *IBM System/360 OS – Program Planning Guide for the DOS Emulator on IBM System/370, Models 135, 145, and 155*, GC24-5076.
4. *IBM System/360 Component Descriptions – 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control*, GA26-3599.
5. *IBM System/370 Principles of Operation*, GA22-7000 (see Note).
6. *IBM System/370 System Summary*, GA22-7001.
7. *IBM System/370 Input/Output Configurator*, GA22-7002.
8. *IBM System/370 Model 135 Configurator (U.S.A. only)*, GA33-3006.
9. *IBM System/370 Model 135 Configurator (Countries other than U.S.A.)*, GA19-0044.
10. *IBM 2701 Data Adapter Unit Principles of Operation*, GA22-6864.
11. *IBM 2701 Data Adapter Unit Original Equipment Manufacturers' Information*, GA22-6844.
12. *IBM 2703 Transmission Control Component Description*, GA27-2703.
13. *Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Models 135 using DOS/360*, GC33-2004.
14. *Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Models 135, 145, and 155 using OS/360*, GC27-6945.
15. *General Information – Binary Synchronous Communications*, GA27-3004.

Note: Manuals GA22-6821 and GA22-7000 are referred to jointly in the text as "the Principles of Operation manuals".

The titles of other publications that may help the reader are given in *IBM System/360 and System/370 Bibliography*, GA22-6822 and its associated newsletter *Accumulative Index of Publications and Programs*, GN20-0360.

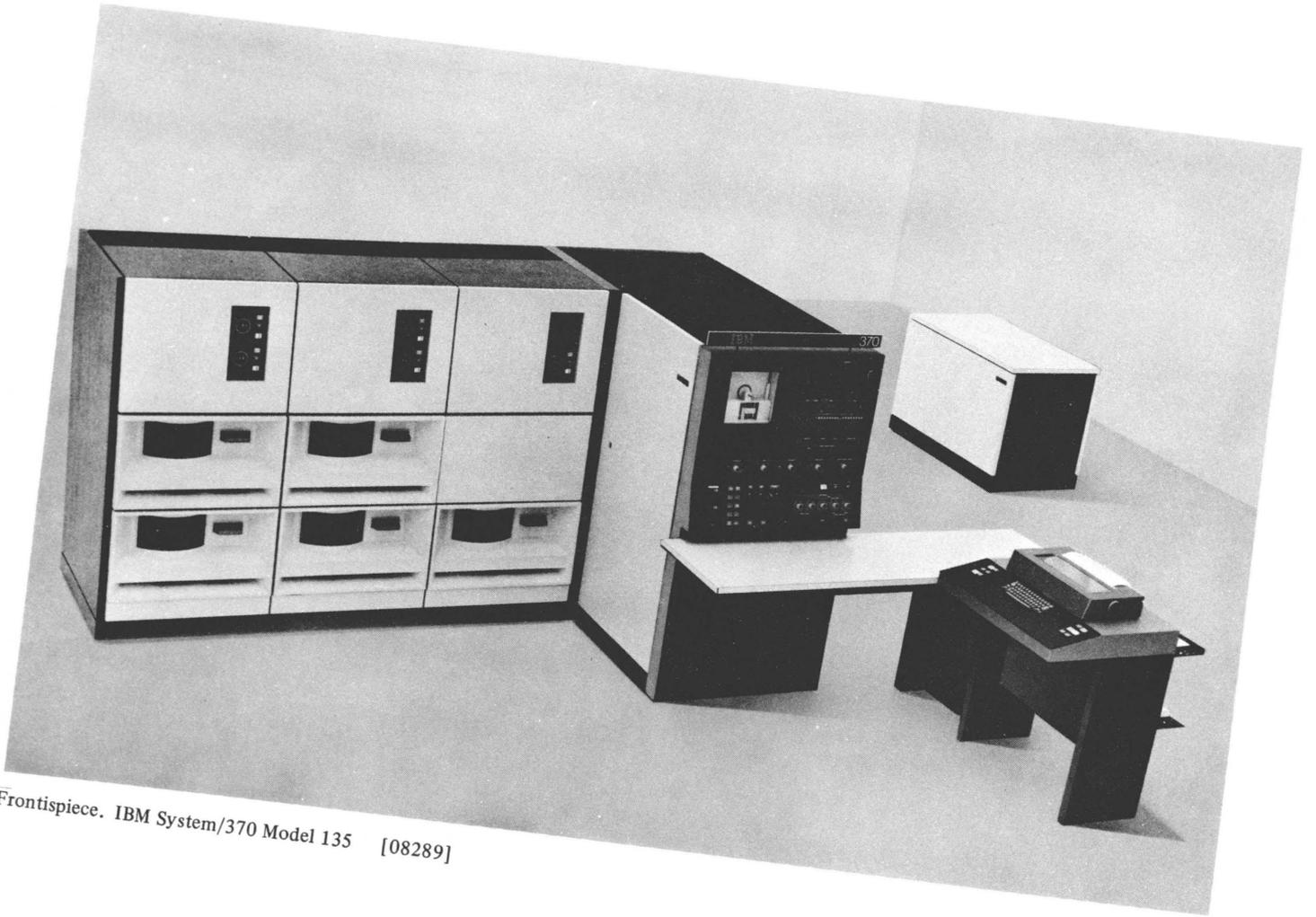
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Frontispiece. IBM System/370 Model 135 [08289]

The IBM System/370 comprises a series of compatible, general purpose data processing systems that are designed for teleprocessing as well as for commercial and scientific applications. The System/370 provides a successor range of models to the IBM System/360 that, in addition to incorporating the basic System/360 capabilities, provides many extensions and improvements.

The System/370 Model 135 (see Frontispiece) presents to users of intermediate systems, such as the System/360 Models 25 and 30, a varied and comprehensive potential for expansion without the need for reprogramming. Most System/360-supported programs can be run on the Model 135.

PERFORMANCE CHARACTERISTICS

Typical performance characteristics of the System/370 Model 135 are as follows:

Storage access width: Two bytes or four bytes. The control storage access width is two bytes; the main storage access width is two or four bytes, depending on the operation.

Basic machine cycle time: A minimum of 275 nanoseconds (ns), the actual time depending on the type of control instruction.

Storage cycle time: 660 ns for a cycle steal operation, 770 ns for a read operation, and 935 ns for a write operation. The cycle times for the read and write operations include the fetch time of the next microinstruction.

CPU MAIN STORAGE CAPACITY

Various models of the IBM 3135 Processing Unit are available for the System/370 Model 135. These central processing units (CPU's) differ only in the size of main storage:

<i>Model of 3135</i>	<i>Main Storage Size</i>
FE	98,304 (96K) bytes
GD	147,456 (144K) bytes
GF	196,608 (192K) bytes
DH	245,760 (240K) bytes

SYSTEM FEATURES

The features of the System/370 Model 135 are classified as selective, standard, and optional.

Selective Features

Either of the following console printer-keyboards can be chosen:

- IBM 3210 Console Printer-Keyboard Model 1
- IBM 3215 Console Printer-Keyboard Model 1.

Standard Features

The standard features of the system represent the basic capability of any System/370 Model 135. They include:

1. System/360 standard features, including some improved functions.
2. Changes to System/360 standard features.
3. Various System/370 features.

System/360 Features

The following features of the System/360 are incorporated in the standard features of the System/370 Model 135:

1. The System/360 Instruction Set, including decimal arithmetic.
2. All other definitions that are contained in the Principles of Operation manual* (except those items shown under "Changes to System/360 Features"), including:
 - Byte-multiplexer channel
 - Byte-oriented operands
 - Interval timer
 - Storage protection (store and fetch).
3. Specific definition of the following functions (which, in the System/360, are permitted unpredictable operations), without affecting the operation of programs written for the System/360 when these are run on the System/370 Model 135:
 - Handling of invalid decimal sign
 - Protection exception in edit and edit-and-mark operations
 - Imprecise interruptions.

Changes to System/360 Features

One standard feature of the System/360 is redefined for use in the System/370 Model 135 and two standard features are omitted:

1. The 'halt I/O' instruction is modified so that the same operation code is also used by the 'halt device' instruction.
2. American National Standard Code for Information Interchange (ASCII) is omitted.
3. The multisystem operation mode is omitted.

* *IBM System/360 Principles of Operation*, GA22-6821, and *IBM System/370 Principles of Operation*, GA22-7000.

System/370 Features

The following features of the System/370 are included in the Model 135 standard features:

- Control registers
- Error recovery (machine-check handling)
- Extended external masking
- Limited channel logout (extended channel status word)
- OS/DOS compatibility
- System/370 Commercial Instruction Set
- Time-of-day clock.

Optional Features

The optional features of the Model 135 are as follows:

- Block multiplexing
- Direct control
- Expanded control storage (36,864 bytes or 49,152 bytes, depending on other features required)
- Extended-precision floating point
- First selector channel
- First and second selector channels
- Floating point
- Integrated communications adapter (ICA)
- Integrated file adapter (IFA)
- 1401/1440/1460 compatibility.

Compatibility Features

OS/DOS Compatibility

The OS/DOS compatibility feature allows a Disk Operating System (DOS) emulator program to run under Operating System (OS) with MFT*. The DOS emulator program in turn allows System/360 programs that were written for a DOS system to be run in the OS job stream on the System/370 Model 135. For further details, refer to *IBM System/360 OS – Program Planning Guide for the DOS Emulator on IBM System/370, Models 135, 145, and 155, GC24-5076*.

1401/1440/1460 Compatibility

The 1401/1440/1460 compatibility feature enables certain operations associated with the IBM 1401, 1440, and 1460 Data Processing Systems to be executed. This compatibility feature allows an emulator program to emulate one of the three systems. For further details, refer to *Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Models 135, 145, and 155 using DOS/360, GC33-2004, and Emulating the IBM 1401, 1440, and 1460 on the IBM System/370 Models 135, 145, and 155 using OS/360, GC27-6945*.

* MFT: Multiprogramming with a fixed number of tasks

SYSTEM/360 PROGRAM COMPATIBILITY

All programs that are written for a System/360 (Model 25 and above) operate on a System/370 Model 135 that has a comparable hardware configuration, except for the following programs:

1. Time-dependent programs.
2. Programs written deliberately to cause program checks.
3. Programs using machine-dependent data, such as machine logs.
4. Programs using the ASCII mode (program status word [PSW] bit 12).
5. Programs that depend upon the reserved lower storage area being smaller than 512 bytes.
6. Programs that depend upon devices or architecture not available in System/370 (such as the single disk storage file of the System/360 Model 44).
7. Programs that depend upon the validity of storage data after the system power supply has been turned off and restored.

The System/370 Model 135 is not necessarily compatible with any model of System/360 for those functions that are specified as model-dependent in *IBM System/360 Principles of Operation, GA22-6821*.

Note: Programs written for System/360 can be run initially in the stop-after-log mode in order to facilitate error recording.

SYSTEM RESIDENCE AND MAINTENANCE STORAGE REQUIREMENTS

The optimum performance and maximum availability of the System/370 Model 135 are maintained when a disk-storage facility is provided for residence of the operating system and the application-program files, for the storage of diagnostic tests, and for the storage of error-logout information. In this manual, these residence and storage requirements are assumed to be contained either in an IBM 2319 Disk Storage Model A1 (attached through the integrated file adapter feature) or in a similar disk-storage device (attached through a selector channel). The user has the following options:

1. Using the IFA with a 2319 Disk Storage.
2. Using a selector channel or block-multiplexer channel with a disk-storage device. (In this manual, a selector channel or block-multiplexer channel with a 2314-type direct access storage facility is assumed.)
3. Electing not to use the associated Recovery Management Support package described in the *IBM System/360 DOS – Program Planning Guide for MCAR/CCH Function for IBM System/370 Model 135, GC24-5089*.

The operation of the System/370 Model 135 depends on the microprogram-controlled 3135 Processing Unit, which has the following functions:

1. To execute the instructions of the system.
2. To provide channel and control unit functions for various input/output (I/O) devices that are integrated adapters.
3. To control the operation of System/370 channels.

The CPU performs these operations by means of the following principal units and functions which, together, constitute the basic structure of the system:

- Console file
- Main storage
- Control storage
- Work storage
- Auxiliary storage
- Arithmetic and logic unit (ALU)
- Input/output facilities.

The principal power supply for the CPU is obtained from a motor-generator frequency-converter set, the IBM 3046 Power Unit Model 1. This power unit converts the mainline

power supply frequency (50 hertz or 60 hertz, depending on the country of installation) to a frequency of about 400 hertz. The power unit also protects the CPU power supplies from mainline power supply disturbances.

DATA FLOW

A concept of the System/370 Model 135 operation is provided by the simplified data flow of the CPU (Figure 1). Microinstructions from the console file are loaded into control storage during the initial microprogram load (IMPL) procedure. Control word data from control storage is entered directly into a control data register, and one control word is fetched for each machine cycle. For sequential microinstruction fetching, the contents of a backup address register are transferred to a storage address register through an incrementer; the information is then returned to the backup address register, ready for the next machine cycle.

Data transfer operations to or from both main storage and control storage are controlled by the microprogram,

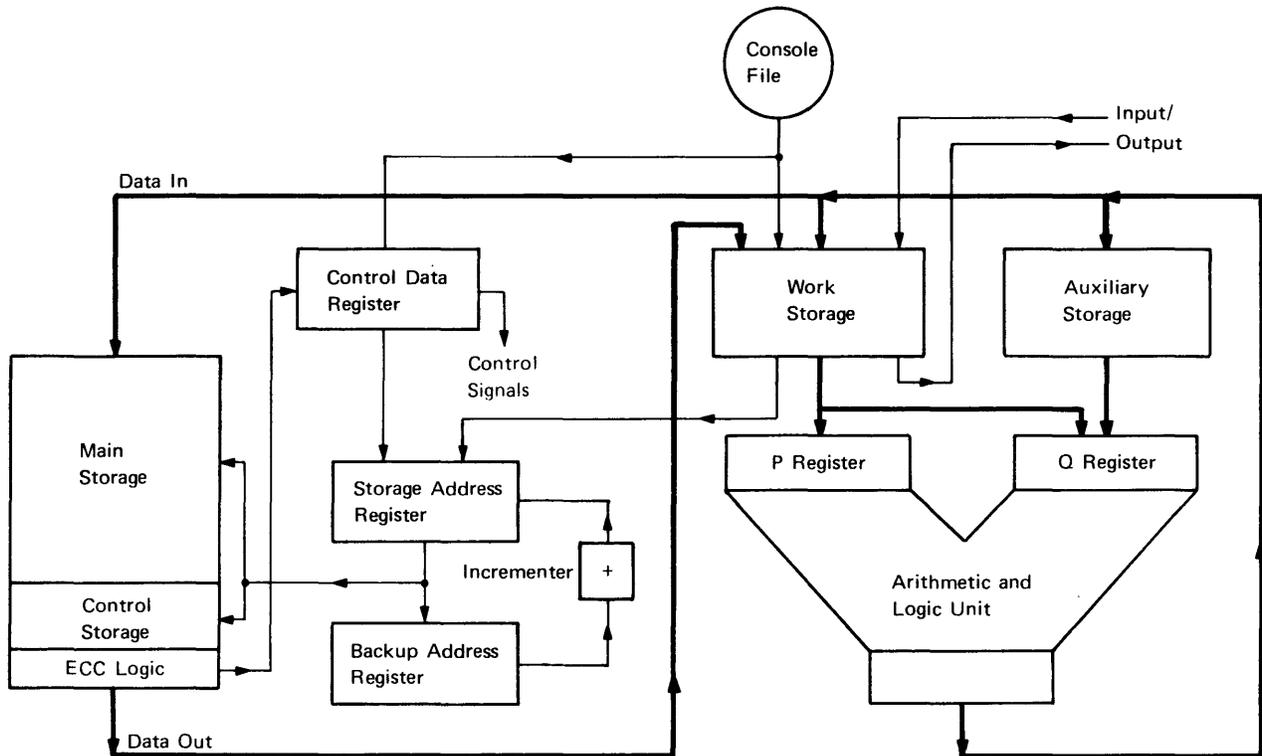


Figure 1. CPU – Simplified Data Flow [08290]

with the work storage being used as a source or destination for the data. For access to main storage data, a 24-bit address is transferred from work storage into the storage address register.

Note: Control storage is not available to the programmer.

Data is transferred between main storage and the I/O interface or between control storage and the I/O interface along a work storage bus.

CONSOLE FILE

The console file is a read-only, single-drive disk storage unit that provides all the microcode which is loaded into control storage during the IMPL procedure. Four disks are supplied with the console file:

1. An initial microprogram disk, which carries a bootstrap loader routine, initial microdiagnostic routines, and the microprogram (particular to the system features installed) that is required for System/370 operation.
2. A device diagnostic program disk, which carries the microprogram for checking the CPU and the timing of mechanical actions within the integrated I/O attachments; this disk is for use by maintenance engineers only.
3. Two automatic system checkout program (ASCP) disks, which provide a stand-alone program that tests and reports on the reliability of the CPU, I/O channels, and integrated adapters. This program does not overwrite control storage; a second IMPL procedure is therefore not necessary after using this program.

Initial Microprogram Loading

Initial microprogram loading occurs automatically when system power is applied or when the START CONSOLE FILE pushbutton (on the system control panel of the 3135) is pressed. In either case, the IMPL indicator comes on and power is applied to the console file. When the console file attains operating speed, disk reading starts and microcode is loaded from the console file into control storage under control of the bootstrap loader routine.

During the initial stages of the IMPL procedure, microprogram checkout routines are performed before the microprogram is loaded into control storage. When the checkout routines have been successfully executed, the error checking and correction (ECC) mode is changed by microprogram to a mode in which all correctable storage errors on data-fetch cycles cause an error condition. This new mode permits a storage-mapping microdiagnostic program to be executed, which determines the location of single-bit errors in storage.

The functional microprogram is then loaded into control storage. When loading is completed, power to the console file is turned off and the system reset microprogram is executed. After system reset, the IMPL indicator goes off and the CPU stops until an external action, such as initial program load, is taken.

MAIN STORAGE

The main storage consists of monolithic storage cells. Its size depends on the model of 3135 in the system (see "CPU Main Storage Capacity"). The storage cycle time is the same for each size of main storage.

A storage data word of 72 bits is used, of which 64 bits (one doubleword) are data bits and eight bits are check bits. The check-bit code enables any single-bit error to be detected and corrected automatically. This error checking and correction code also allows double errors and some multiple errors to be detected.

The ECC logic, located separately from the storage logic, handles both main storage errors and control storage errors.

Permanently Assigned Areas

In the System/370 Model 135, program-storage addressing begins at location 0 and continues upward through the highest installed program-storage byte location. To ensure compatibility between System/370 models and System/360 models, however, fixed program-storage allocations (that is, permanently-assigned main storage areas) for all configurations of the System/370 Model 135 are as follows:

<i>Word Address</i>		<i>Length</i>	<i>Purpose/Function</i>
<i>Decimal</i>	<i>Hex</i>		
0	00	2 words	Initial program-loading PSW and Restart New PSW
8	08	2 words	Initial program-loading CCW1 and Restart Old PSW
16	10	2 words	Initial program-loading CCW2
24	18	2 words	External old PSW
32	20	2 words	Supervisor-call old PSW
40	28	2 words	Program old PSW
48	30	2 words	Machine-check old PSW
56	38	2 words	Input/output old PSW
64	40	2 words	Channel status word
72	48	1 word	Channel address word
76	4C	1 word	—
80	50	1 word	Timer
84	54	1 word	—
88	58	2 words	External new PSW
96	60	2 words	Supervisor-call new PSW
104	68	2 words	Program new PSW
112	70	2 words	Machine-check new PSW
120	78	2 words	Input/output new PSW
128	80	8 words	(Reserved)
160	A0	8 words	I/O communications area
192	C0	10 words	(Reserved)
232	E8	2 words	Machine-check interruption code
240	F0	2 words	(Reserved)
248-512	F8-200	66 words	Diagnostic logout area

All remaining byte locations of main storage are available for programming functions.

CONTROL STORAGE

The basic control storage consists of 24,576 bytes of monolithic storage. The unit functions as a read/write control storage and accommodates the microcode for controlling all standard features of the system as well as the following features:

- Direct control
- First selector channel
- First and second selector channel
- Floating-point arithmetic
- Integrated file adapter
- 3210-1 adapter.

The basic control storage can be expanded by two increments of 12,288 bytes to a capacity of 49,152 bytes, according to the feature-configuration of the system.

In general, the microprogram for any feature is assigned to a specific area of control storage. If a feature is not included in the system, its allocated space in control storage is normally left vacant. *In specific cases*, however, where the user can be saved the purchase of an increment of control storage, unused control storage space is sometimes allocated to another feature; for example, in the basic control storage, if the floating-point feature is not installed, microcode for the 3215-1 adapter can replace the microcode for the 3210-1 adapter. This flexibility of control storage allocations is further illustrated by the various expansion-block requirements.

The first increment (up to 36,864 bytes) is needed if any one of the following features is included in the system:

- 3215-1 adapter *and* the floating-point arithmetic feature
- 1401/1440/1460 compatibility
- Extended-precision floating point arithmetic
- Integrated communications adapter
- Block multiplexing
- Additional 48 subchannels for byte-multiplexer channel.

The second increment of control storage (up to 49,152 bytes) is required when either:

1. The 1401/1440/1460 compatibility feature is installed and the ICA is equipped with the Synchronous Data Adapter Type II (Equivalent) feature, *or*
2. Any three (or more) of the following features are installed:
 - a. 1401/1440/1460 compatibility.
 - b. Block multiplexing.
 - c. Terminal Adapter Type I Model II (Equivalent), in the ICA.
 - d. Terminal Adapter Type III (Equivalent), in the ICA.
 - e. Synchronous Data Adapter Type II (Equivalent), in the ICA.

The control storage is loaded with microcode from the console file during the initial microprogram load procedure. Data is lost whenever power is removed, and the control storage must be reloaded by the IMPL procedure when power is restored following a power-off condition.

Access

Control-storage data is written in words of 72 bits, consisting of 64 data bits (one doubleword) and eight check bits; the check bits provide error checking and correction facilities as for main storage. When access is made to the control storage, eight bytes of microcode data are transferred to a storage data register in the control storage unit. The data is then fetched from this register in halfwords (two bytes), each halfword representing the microprogram control word.

The rate of access depends on the execution time that is required for the particular microinstruction being implemented. The minimum time between successive accesses to control storage is 275 nanoseconds; this time is based on a machine clock period of 55 nanoseconds and a minimum cycle of 5 clock beats (see Figure 2).

Addressing

All control storage locations can be read and written by microprogram, using indirect addressing from a work storage address. Some locations can also be addressed directly, by an address contained in the microinstruction.

WORK STORAGE

Work storage is used as a source or destination of data/information by both main storage and control storage. Work storage is divided functionally into eight zones, each zone consisting of eight halfwords.

Zone Allocation

A specific zone of work storage is allocated as a work area to the CPU and each input/output feature of the system, as follows:

Zone	Feature
0	CPU
1	Console (logout and system reset)
2	Byte-multiplexer channel and console printer-keyboard
4	Integrated communications adapter
5	Integrated file adapter
6	First selector channel
7	Second selector channel

A zone may be capable of handling more than one I/O feature, as shown for zone 2, for example.

Priority Allocation

The central data flow can handle only one task at a time and only one zone of work storage is active at any one time in a microprogram task. A microprogram interruption system permits microprogram service, on a priority basis, to the CPU or the various I/O features (channel and integrated adapters) using the central data flow.

The CPU and I/O features are each assigned a level, or number of levels, of priority according to their relative importance. Several adapters may be allocated to one priority and, in this case, a sublevel order is applied. If numerous requests of the same priority level are received simultaneously, they are serviced in a specific order before any further requests are accepted at that level. This action prevents one adapter from excluding others of the same priority.

When a microprogram interruption request is accepted by the central data flow hardware, the status of the interrupted microprogram, in particular the next microprogram address from which a restart will be made, is preserved in the allocated zone of work storage. The status for up to seven individual microprograms can be preserved.

AUXILIARY STORAGE

An additional high-speed store – called auxiliary storage – provides general registers, floating-point registers, and sixteen halfwords of working area that are used mainly for multiply and divide functions. Auxiliary storage is used only by the CPU.

ARITHMETIC AND LOGIC UNIT

The ALU has an access width of two bytes and provides the following functions:

Add
 Subtract
 OR
 Exclusive OR
 AND
 AND Not
 Pass
 Complement.

Data is processed by the ALU according to the function that is required by the microinstruction and the results are written into work storage. Data that is transferred between work storage and auxiliary storage is passed through the ALU.

An ALU operation cycle on two bytes (halfword) requires a minimum of five beats of the basic 55-nanosecond system clock (Figure 2). Each extra halfword that is operated upon in a cycle requires a further three beats.

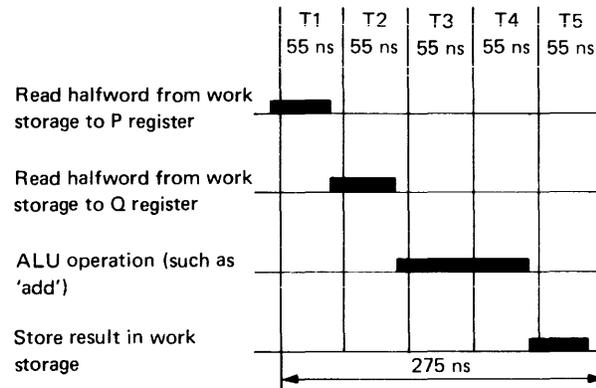


Figure 2. Example of Microinstruction Timing [08291]

INPUT/OUTPUT FACILITIES

Internal I/O Interface

The internal input/output interface provides data transfer facilities between the CPU hardware and the hardware of the various integrated adapters and channel adapters. The interface is used by microinstructions that transfer data between work storage and I/O attachments or send control fields to the I/O attachments. It is also used during cycle steal transfers between main or control storage and the attachments.

Integrated I/O Adapters

Certain input/output devices are attachable to the System/370 Model 135 through adapter circuits that are connected directly to the CPU circuitry. These integrated adapters eliminate the need for the standard interface associated with channel and control-unit combinations. The program, however, is not affected by the method of attachment used.

Integrated adapter features (shown in *italics*) are available for the following devices:

- 2319 Disk Storage. (*Integrated file adapter.*) This device contains three disk storage modules. When the device is attached, either one, but not both, of the following additional disk storage devices can be connected to the 2319:
 IBM 2312 Disk Storage Model A1 (containing one disk storage module).
 IBM 2318 Disk Storage Model A1 (containing two disk storage modules).
- Up to eight start/stop or binary synchronous data communication lines. (*Integrated communications adapter.*)

Further details about the attachment of these devices are given under "Integrated Adapters" in the section "Input/Output Characteristics".

Channels

The range of I/O devices that may be attached to the system is expanded by the use of the byte-multiplexer channel and two selector channels. The byte-multiplexer channel (channel 0) is capable of providing up to 64 subchannels, eight of which can be shared subchannels. Each of the two selector channels can be enhanced by the block-multiplexer feature, which provides 17 subchannels for the interleaved (multiplexed) execution of two or more channel programs.

This section describes the functional characteristics of the CPU and the central data flow area in greater detail than that outlined under "System Structure and Operation". Channel and integrated I/O facilities are described in the section "Input/Output Characteristics".

INSTRUCTION SETS

All instructions of the System/370 Model 135 are implemented by microprogram. The instruction set that is

available to the system can be considered in three groups:

1. A basic instruction set that includes the System/370 standard and commercial instruction sets.
2. A floating-point arithmetic instruction set that can include extended-precision floating-point arithmetic instructions.
3. Instructions for compatibility features.

Instruction word formats and definitions are dealt with in detail in the Principles of Operation manual. The general organization of System/370 instructions is shown in Figure 3.

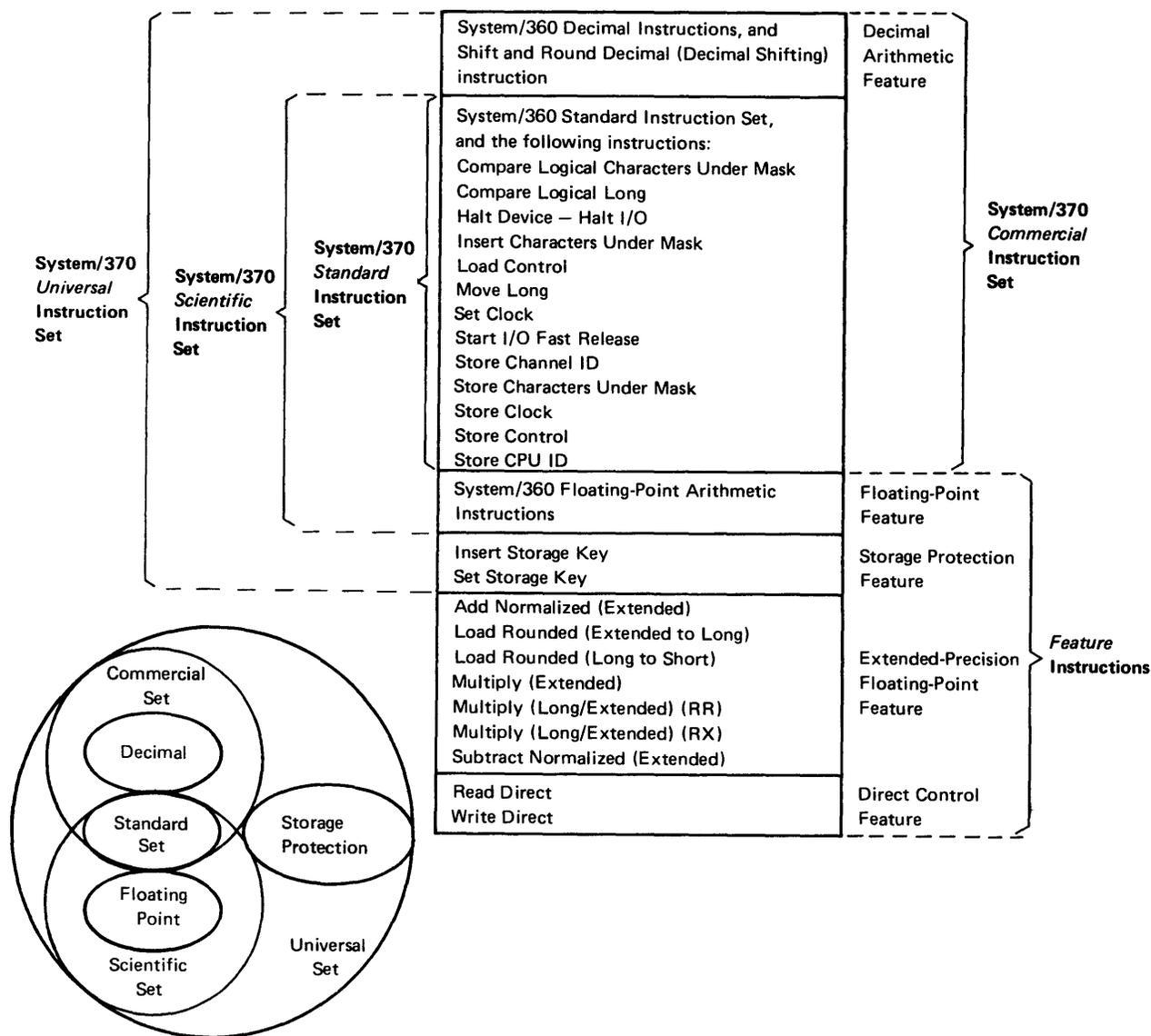


Figure 3. System/370 Instruction Sets [08292]

Basic Instruction Set

The basic instruction set of the Model 135 consists of the System/370 commercial instruction set (System/370 standard instruction set plus decimal arithmetic with decimal shifting), and the following instructions:

‘Halt I/O’ – ‘halt device’

Storage protection instructions; see “CPU Facilities”.

System/360 Instructions

The instructions of the System/360 standard set are implemented by an instruction-fetch (I-fetch) micro-instruction that obtains the instruction from control storage, partially decodes the instruction, then branches to a microprogram routine to complete the instruction or group of instructions.

Start I/O Fast Release

The Model 135 executes the ‘start I/O fast release’ instruction as a ‘start I/O’ instruction.

Halt I/O – Halt Device

The ‘halt I/O’ and ‘halt device’ instructions are available for terminating input/output operations. Either instruction may be used, depending on the program requirement for the channel.

The ‘halt I/O’ instruction operates in the same manner as the correspondingly named System/360 instruction (described in the Principles of Operation manual). Its definition, however, requires that bit 15 of the instruction word must be specified as 0. This bit is part of the high-order address byte, which is ignored in the System/360 instruction.

If bit 15 of the instruction word is set to 1, the instruction becomes ‘halt device’. This instruction offers the program greater flexibility than does ‘halt I/O’ for controlling the termination of I/O operations. For example, it permits the CPU to:

1. Stop data transfer with a given device.
2. Terminate action at a given device.
3. Terminate a current burst operation on a channel only if the channel is working with the addressed device.

Floating-Point Arithmetic

The floating-point arithmetic facilities consist of two groups of instructions: floating-point and extended-precision floating-point. The basic floating-point instruction set is a prerequisite for the extended-precision floating-point set.

Basic Floating-Point Arithmetic Instructions

The basic floating-point arithmetic group of instructions is the same as the System/360 floating-point instruction set (described in the Principles of Operation manual).

Extended-Precision Floating-Point Arithmetic Instructions

The extended-precision floating-point arithmetic instruction set consists of the following instructions:

Add normalized (extended)

Load rounded (extended to long)

Load rounded (long to short)

Multiply (extended)

Multiply (long/extended), RR format

Multiply (long/extended), RX format

Subtract normalized (extended).

The extended-precision format uses two long-precision number formats (two doublewords) to provide a fraction of 28 hexadecimal digits (112 bits), which is approximately equivalent to 34 decimal digits. One long-precision number is designated as the high-order part of the extended-precision number, and the other as the low-order part. The sign and characteristic of the high-order part are also the sign and characteristic of the whole extended-precision number.

CPU FACILITIES

The following general facilities are available to the CPU to enhance the flexibility and control of the System/370 Model 135:

Byte-oriented operands

Channel identification

CPU identification

Direct control and external interruption

Interval timer

Storage protection (store and fetch)

Time-of-day clock.

Byte-Oriented Operands

The byte-oriented operand feature allows the main-storage operands of unprivileged instructions to appear on any byte boundary without causing a specification exception and a program interruption. When this facility is used, the operation which is termed “boundary alignment” affects storage references made by the CPU with RX-format and RS-format instructions.

The feature applies to fixed-point operands, floating-point operands, and logical operands. It does not apply to instruction addresses, privileged instructions and channel command words (CCWs). The definition of the feature and the limitations of boundary alignment operations are given in the Principles of Operation manual.

Note: Optimum performance is achieved only when operands are aligned in accordance with System/360 procedure.

Storage Protection

The storage protection feature, which includes both storage protection and fetch protection, allows the contents of

main storage to be protected from destruction or improper handling during the execution of a program. The protection is achieved by the matching of storage keys (associated with blocks of main storage) and protection keys (associated with the PSW or an I/O operation) to identify the right of access to a storage location. A special 64-word, eight-bit store is used to hold the storage keys. The feature includes the instructions 'insert storage key' and 'set storage key' and is defined in the Principles of Operation manual.

Time-of-Day Clock

The time-of-day clock feature provides a consistent measurement of elapsed time that can be used for indicating the time of day. The feature consists of a 64-bit binary counter with bit positions that correspond to those of a fixed-point number in double-precision format. Time is measured by the clock increasing its value incrementally, in accordance with the rules of fixed-point arithmetic. The resolution of the clock is at least one microsecond.

The feature includes the instructions 'store clock' and 'set clock'. The 'store clock' instruction allows the clock to be inspected, thereby causing the current clock value to be placed in main storage. The 'set clock' instruction allows the clock to be set to a specific value, and causes the current clock value to be replaced by an operand that is designated by the instruction.

The clock does not run and the clock value is lost when the system power is off; the clock value is lost also when the IMPL procedure is carried out.

Interval Timer

The interval timer provides program interruption on a program controlled basis. The storage word at main-storage locations 80-83 (decimal) is reserved for the interval timer feature. Any value stored at this location is automatically reduced by decrementing bit 23 every 3.333 milliseconds, provided the interval-timer switch is in the NORM (normal) position. The high-order 24 bits provide a full cycle of about 15.5 hours.

The program in process can be automatically interrupted by an external interruption, provided PSW system-mask bit 7 is on, when the interval timer word goes from a positive value to a negative value. The interruption is identified by setting PSW bit 24 on.

CPU Identification

Information identifying the CPU is stored in an eight-byte field of main storage that is designated by the operand address of the 'store CPU ID' instruction. The format of the stored information is as follows:

Bits 0-7	(Reserved)
Bits 8-31	CPU serial number
Bits 32-47	CPU model number
Bits 48-63	Contain all zeros

Channel Identification

Information that identifies a designated channel is stored in a four-byte field of main storage at location 168 of the I/O communications area (location 160 through 191). Bits 16 through 23 of the sum that is formed by adding the contents of the register B1 and the contents of the D1 field of the 'store channel ID' instruction identify the channel to which the instruction applies. The format of the stored information is as follows:

Bits 0-3	Contain a code to identify the type of channel:
	0000 indicates selector channel
	0001 indicates byte-multiplexer channel
	0010 indicates block multiplexer channel
Bits 4-32	Contain all zeros

Direct Control and External Interruption

The direct control feature provides two instructions, 'read direct' and 'write direct', for transferring a single byte of information between an external device and main storage. The feature also provides six external interruption lines, each of which, when active, sets up the conditions for an external interruption. Detailed definitions of the instructions and the external interruptions are given in the Principles of Operation manual.

SYSTEM CONTROL

The System/370 Model 135 operates under the control of the current PSW and control registers. The current PSW is loaded from main storage by means of the 'load PSW' instruction, and is stored in various permanently assigned areas of main storage when an interruption is accepted; see the Principles of Operation manual. The control registers are part of control storage.

System and CPU recovery from hardware errors is controlled by an automatic machine-check handling procedure.

Control Registers

The control registers consist of up to sixteen 32-bit registers that are located in fullword areas 0 through 15 of control storage. Registers and/or specific bit positions within a register are allocated to each system feature that requires control register facilities. The usage of the registers and the bit positions available depends on the number of features installed.

Two instructions, 'load control' and 'store control', are associated with the control registers. 'Load control' allows control information to be loaded from main storage into the control registers; 'store control' allows information to be transferred to main storage from the control registers.

Instructions

'Load Control': The main storage area *from* which the contents of the control registers are obtained starts at the

location designated by the second-operand address and continues through as many storage words as the number of control registers specified. The control registers are loaded in ascending order of their addresses, starting with the control register specified by the R1 field and continuing up to and including the control register specified by the R3 field, with control register 0 following control register 15.

'Store Control': The main storage area *into* which the contents of the control registers are placed starts at the location designated by the second-operand address and continues through as many storage words as the number of control registers specified. The contents of the control registers are stored in ascending order of register addresses, starting with the control register specified by the R1 field and continuing up to and including the control register specified by the R3 field, with control register 0 following control register 15. The contents of the control registers remain unchanged.

External Masking

The external masking arrangements of the System/370 Model 135 provide the means for selective masking of interruptions due to timer, interruption key, and external signals (bits 24, 25, 26 respectively). The extended external masking feature is implemented by three subclass mask bits in control register 0, in conjunction with the external mask bit of the PSW, as defined in the Principles of Operation manual.

Machine-Check Handling

The error-recovery facilities and machine-check interruption procedures of System/370 Model 135 comply with the general definitions that are contained in the Principles of Operation manual. Specific definitions for Model 135 can be considered in the following phases:

- Error checking, with automatic correction whenever possible
- Internal logout
- Error analysis and actions
- Instruction retry, with error recovery whenever possible
- Machine-check logout
- Check stop.

Error Checking and Correction

Both main storage and control storage are provided with an error checking and correction code that automatically corrects any single-bit error and detects any double-bit error. In addition, if more than 255 single-bit error corrections are made in any one 416-microsecond period, the CPU sets bits 2 and 17 in the machine-check interruption code. (If a storage error is not corrected, the CPU sets bits 1, 14, and 16 in the machine-check interruption code.)

A single-bit correction adds 165 nanoseconds to the execution time of the microinstruction within which it is

performed. During this period, the data is corrected and passed to the CPU. The data in storage is not corrected. Each correction increments an eight-bit hardware counter that is reset every 416 microseconds.

The error checking and correction code is derived from eight bits that are associated with each doubleword in main storage and control storage.

Internal Logout

For any hardware error other than normal-rate, corrected single-bit errors, the CPU generates an internal logout as a preliminary action to error analysis. Error analysis is followed either by a recovery or, if a machine-check interruption proves necessary, by a synchronous machine-check logout. This internal logout records the hardware-indicated error conditions in two special buffers that are maintained in a private control storage area: the machine-check interruption code (MCIC) buffer and the logout buffer. The buffer area consists of ten halfwords that are allocated as follows:

1. One fullword is allocated to the MCIC buffer to provide an image of the machine check interruption code, which is stored at location 232 of main storage.
2. Eight halfwords are allocated to the logout buffer to provide:
 - a. An immediate storage for hardware error signals.
 - b. The address of the "failed" microinstruction.
 - c. The identity of the adapter that is in error.
 - d. The current storage address.
 - e. Information relating to the interruption status of the CPU and the state of the 'instruction retry' latches.

Error Analysis

An internal logout invokes a microprogram that analyzes the error status and decides the next action. If the error status is such that the extent of the damage cannot be determined, the system-damage bit is set and all validity bits are reset in the MCIC buffer. A *machine-check interruption* is requested, and the subsequent action depends on the value of bit 13 in the program status word and of the hardstop bit in control register 14.

If the error status is such that the current CPU instruction sequence has not been affected, a specific interruption is requested and normal instruction execution is resumed. No validity bits are reset in the MCIC buffer. Typical causes and the subsequent actions are as follows:

1. *Channel program affected.* The subchannel is set up to request an I/O interruption with channel-control check.
2. *Damage to time-of-day clock or interval timer.* A machine-check interruption is requested.
3. *Single-bit storage errors have been corrected at a rate of more than 255 in 416 microseconds.* The storage error corrected bit is set in the MCIC buffer and a machine-check interruption is requested.

If the error status indicates that the current CPU instruction sequence cannot be immediately resumed, the microprogram analyzes the recovery possibilities by an instruction-retry routine.

Instruction Retry

The system can attempt to recover from intermittent failures automatically by restarting the instruction, from the beginning, when an error is detected – but only if the source data was not changed before the point of error. The instruction is retried up to eight times. The success of the retry depends on the cause of the error.

Validity Bits

The validity bits of the machine-check interruption code have the following significance:

1. *If zero:* At a point of error preceding the interruption, the contents of the indicated storage registers were modified in error.
2. *If one:* At all preceding points of error, the contents of the indicated storage registers remained valid.

Machine-Check Logout

Each internal logout normally leads to an error inter-

ruption. The contents of the logout buffer are copied to main storage during the interruption. Because the data flow area and microprograms of the System/370 Model 135 are used for the control of channels and integrated adapters as well as for CPU control, the logout buffer contents can relate to either a machine-check condition or a channel control check. Thus the interruption may relate to either a CPU error or a channel error.

Check Stop

The system enters the check-stop condition if any one of the following situations arises:

1. Any hardware error is detected when the system is in the manual-stopped state.
2. Repeated errors occur during the error analysis microprogram.
3. PSW bit 13 and the hardstop bit in control register 14 are both ones, and an error occurs during a machine-check interruption which is already attempting to report system damage or instruction processing damage.
4. PSW bit 13 is zero and the hardstop bit is one, and an error occurs which causes the system damage bit or the instruction-processing-damage bit to be set in the MCIC buffer.

The input/output devices that can be connected to the System/370 Model 135 are listed in *IBM System/370 Input/Output Configurator*, GA22-7002. Most of these devices are attached to the CPU through either a *byte-multiplexer channel* or a *selector channel* operating across a standard I/O interface. Some I/O devices, however, are attached directly to the CPU through special adapters that replace the standard channel/control-unit combination and I/O interface; devices that can be attached in this manner are dealt with in this section under "Integrated Adapters".

Channel Facilities

The channel facilities of the System/370 Model 135 consist of one byte-multiplexer channel and two selector channels, with a block-multiplexer feature available for the selector channels.

BYTE-MULTIPLEXER CHANNEL

The byte-multiplexer channel conforms to the definitions given in the Principles of Operation manual. Communication with the input/output devices attached to the channel is through a standard I/O interface that is extended to include a disconnect-in line and a mark-out line.

The byte-multiplexer channel is intended for the attachment of low-speed input/output devices. Functionally, it interprets I/O instructions, translates them into commands and controls at the interface to operate the devices, transfers data between the devices and main storage, and controls interruptions that are raised either by device requests to the program or by error conditions. The channel is addressed as channel 0.

Mode of Operation

The channel multiplexes (interleaves) data to or from the I/O devices, on request and for one device at a time, in groups of sequential bytes as required by the particular device being serviced. An unbuffered burst-mode device can be attached to the channel, but this is not recommended if there is any possibility of the burst-mode device operating concurrently with the integrated file adapter, the integrated communications adapter, or a selector channel.

Data Rates

Data times and rates for the byte-multiplexer channel are

given in Figure 4; these assume that there is no activity on the selector channels, the IFA, or the ICA. *Data-chaining* data rates which, if exceeded, cause an overrun condition are also given in Figure 4.

Delays within the control unit are assumed to be greater than delays within the channel. As control unit delays increase, so the time for each additional byte in burst mode increases, by 2.2-microsecond increments, up to 13.3 microseconds. One larger increment to 19.2 microseconds per additional byte then occurs, after which the time per byte increases linearly with the increase in control unit delay.

Control

Byte-multiplexer channel operations are implemented mainly by microprogram. To facilitate this control, I/O operations utilize the CPU data flow area, the arithmetic and logic unit, general registers, and zone 2 of CPU work storage. Work storage zone 2 is also shared with the integrated 3210-1 or 3215-1 adapter.

In addition to these areas, an area of 16 bytes is reserved in control storage for each I/O device that is attached to the channel. This area holds the unit control word (UCW), which contains information for controlling the current operation of the device. Also, one halfword of directly addressable control storage is used as an interruption buffer to present the CPU with information when it makes an interruption. The hardware of the byte-multiplexer channel includes seven bytes of external registers that contain interface tags, data, and various controls.

Input/output operations are initiated by a common microprogram at CPU level, and control is transferred to the channel when it becomes necessary to select a device at the I/O interface. This need occurs when the channel detects a condition that requires the channel microprogram; a hardware-generated request is then sent to the CPU to transfer control. This request can be caused either by the 'operational in' signal falling, by a CPU interruption to request initiation of an I/O operation or timeout, or by any of the following signals received at the interface:

- Address in
- Disconnect in
- Select in
- Service in
- Status in.

When the byte-multiplexer channel has completed the initial selection routine, it sets a condition code in an I/O operation buffer that consists of three halfwords of CPU

DATA TIMES AND RATES

Channel Operation	Time (microseconds)	Maximum Data Rate (bytes per second)
One byte-multiplexed transfer	24	41,000
One byte-multiplexed transfer with PCI	26	38,000
Each additional byte in burst mode	6.7	149,000
Command chaining with TIC and PCI (if no other activity on channels)	56	—

DATA CHAINING TIMES AND RATES (See Note)

Channel Operation	Time (microseconds)	Data Rate (bytes per second)
Data chaining within channel	22	45,000
Data chaining with TIC	28	35,000
Data chaining with PCI	34	30,000
Data chaining with TIC and PCI	40	25,000

Note: If these chaining rates are exceeded, an overrun condition is caused.

PCI: Program-controlled interruption

TIC: Transfer in channel

Figure 4. Byte-Multiplexer Channel – Data Rates and Times [08293]

work storage. This buffer information also contains the UCW address, the CCW command code, the device address, and a byte of flags. When control is returned to the CPU, this condition code is examined and a channel status word (CSW) is stored, if required, by using information already placed in the UCW by the channel.

When an I/O device initiates a multiplexer interface sequence for data or status transfer and raises the 'address in' signal, the channel requests a microprogram interruption. The channel then generates the UCW address and loads the UCW from control storage into work storage; the UCW contains the information that is needed to continue the operation at the unit. When the interface sequence is finished and the 'operational in' signal falls, the updated UCW is stored back in control storage and control is restored to the CPU. Control is also restored to the CPU during a multiplexer interface sequence if the delay between in-tag signals exceeds 10 microseconds.

Error Handling

Channel programming errors are mostly detected by the common I/O microprogram. The following errors are

detected by either channel hardware or microprogram:

1. *Channel-data check*. This is caused by bad parity on the I/O interface bus-in lines, with the 'service in' signal raised.
2. *Channel-control check*. This is caused by bad parity in the data or address on the bus from the CPU.
3. *Interface-control check*. This is caused by one of the following:
 - a. Bad parity on the I/O interface bus-in lines, with 'address in' or 'status in' raised.
 - b. More than one in-tag signal is raised.
 - c. The 'service out' and 'command out' signals are raised.
 - d. The 'select in' and 'operational in' signals are raised.
 - e. Interface stops during selection or re-selection that last for more than 64 microseconds.
 - f. Interface stops during data transfers that last for more than 30 seconds; during the timeout period, the channel behaves as if it is in burst mode to new I/O instructions.
 - g. A wrong address is received with 'address in' response to 'address out'.
 - h. The 'disconnect in' signal is raised.

4. *Channel-protection check.* This is caused when a protected address is encountered during data servicing or chaining.
5. *Channel-program check.* This is caused by one of the following:
 - a. When an invalid address is encountered during data servicing or chaining.
 - b. When an invalid CCW format is encountered during a start I/O operation or chaining.

CPU errors that are detected when the byte-multiplexer channel is in control are handled by the CPU check system. If the errors are successfully retried, the channel is not informed. If retries are unsuccessful and channel checks are not disabled, the control passes to the multiplexer channel error microprogram, which then sets channel-control check.

Channel-control check or interface-control check raises an error line to the CPU. The higher-priority error handler obtains control and takes action depending on 'stop on error' and console disable mode. An 'inhibit error' latch in the channel is set to prevent interface-control check from raising a trap request; this enables the error handler to set up a channel microprogram start address and to restore control to the channel. The channel then enters an error analysis microprogram, which performs interface-disconnect, selective-reset, or channel-reset operations as necessary, and stores status and logout information in the UCW. The channel raises an I/O program interruption request, unless the error occurred during an I/O instruction, in which case a condition code of 1 is set and a CSW is stored with an I/O logout.

Interruption Handling

To handle interruptions at user program level, an 'interruption request' latch is provided in the CPU for the byte-multiplexer channel. A halfword interruption buffer is

provided in control storage for the channel, but the buffer is also shared by the adapters. A further halfword interruption buffer is associated with the channel for use in error conditions.

When the channel detects a condition that requires an interruption to the user program, it tests its 'interruption request' latch. If the latch is off, it is set on, and the address of the I/O device associated with the interruption is placed in the interruption buffer. In the case of a channel-end type interruption, the status that is needed for the subsequent storing of a CSW is accepted from the device and is placed in the UCW. In all other cases, device status remains in the device and is fetched, when the interruption is accepted, by a pseudo 'test I/O' instruction; the channel mask is examined and, if enabled, the 'program interruption' latch is set. The device address in the interruption buffer can be used to retrieve, from the UCW, the information that is required for storing a CSW.

Note: Program-controlled interruptions (PCIs) are given priority over all other channel interruptions except those requested by error conditions.

Subchannels

The byte-multiplexer channel contains either 16 or 64 subchannels. Each I/O unit attached to the channel requires a subchannel to hold information for controlling the current operation at the unit. A subchannel may be shared by more than one device or it may be nonshared. A *shared* subchannel is used for an I/O unit that can have several devices attached, only one of which requires the subchannel at any one time; a *nonshared* subchannel is used for an I/O unit having only one device.

The allocation of subchannels for the System/370 Model 135 is summarized in Figure 5. The integrated communications adapter is addressed as if it were on channel 0

	With Total Number of Subchannels	
	=16	=64
Maximum Number of Nonshared Subchannels	16	64
Maximum Number of Shared Subchannels	8*	8*
Shared Device Addresses	80 (hex) through FF (hex)	80 (hex) through FF (hex)
Console Printer-Keyboards	09 (hex) or 1F (hex)	09 (hex) or 1F (hex)
ICA Lines*	01 (hex) through 08 (hex)	01 (hex) through 08 (hex)

*When the integrated communications adapter feature is provided, the maximum number of shared subchannels is reduced according to the number of lines installed in the ICA. If 1, 2, 3, 4, 5, or 6 lines are installed, the maximum number of shared subchannels available is 7, 6, 5, 4, 3, or 2 respectively; if 7 or 8 lines are installed, the number of shared subchannels is one.

Figure 5. Byte-Multiplexer Subchannels – Availability and Allocation [08294]

SELECTOR CHANNELS

One or two selector channels are available to the System/370 Model 135. Each selector channel includes the following features, which are described in the Principles of Operation manual:

- Command retry
- High-speed transfer (data in, data out)
- I/O error alert (disconnect in)
- Extended channel status word, that is, limited channel logout.

In addition, block-multiplexing is available on each selector channel. See "Block Multiplexing" in this section.

Each selector channel allows up to eight control units to be attached, through the extended I/O interface. Any control units designed for attachment to the standard I/O interface can be used, within the limits of data rates and response times outlined in this section.

The selector channels are addressed respectively as channel 1 and channel 2 when the integrated file adapter is not provided; they are addressed as channel 2 and channel 3 when the integrated file adapter is provided. (When the IFA is provided, it is always addressed as selector channel 1.)

Mode of Operation

The selector channels are intended for high-speed devices. Only one I/O unit on a channel can be engaged in data-transfer operations at any one time but operations between the unit and the channel can be overlapped with CPU processing cycles.

The operation of a selector channel is implemented by a combination of microprogram and hardware. Each channel is allocated a work storage zone of eight halfwords; when the channel is in control of the central data flow, it uses the work storage zone and external registers in the channel data flow area. Input/output operations, status handling, command chaining, and data chaining are implemented under microprogram control, hardware aids being used to accelerate the chaining.

Data transfer takes place during CPU cycle-steal operations, the data being transferred to storage one or two bytes at a time. The data is buffered in the selector channel, between storage and the I/O interface, by a four-byte buffer.

Device addressing on a given selector channel can use any one of the 256 bit-combinations of a byte and can be assigned by the program, as required for the channel devices. The standard I/O instructions are interpreted by the CPU and are implemented as far as possible at CPU level. Control is transferred to the selector channel microprogram for the selection of a device or to load a channel command word at start I/O time. A buffer in the CPU working registers (auxiliary storage) is used for the transfer of control information from CPU to channel or from channel to CPU.

Selector channel data transfers cause interference of approximately 0.033% per kilobyte per second to all channels and integrated adapters. Selector channel command chaining also causes interference to all channels and integrated adapters, the amount of interference depending on the control unit and the frequency of chaining; for example, the long term interference due to the IBM 3330 Disk Storage data transfer is 28% but this can increase to a worst-case interference of 45% due to command chaining.

Data Transfer

Data is transferred between main storage and a selector channel during cycle-steal operations. During the transfer of a block of data as defined by a CCW, two bytes are transferred during each cycle-steal operation except, possibly, for the first or last cycle-steal operation concerned with that block of data. If the block starts on an odd-byte boundary, a one-byte cycle-steal operation is taken to begin the transfer. Similarly, if the block ends on an odd-byte boundary, a one-byte cycle-steal operation is taken to end the transfer.

During the transfer operation, the current count and the data address are held in the selector channel zone of work storage and are automatically updated by the cycle-steal operation. The four-byte buffer, provided between main storage and the I/O interface, allows for any delay in obtaining response to cycle-steal requests and for the delay that is introduced by data chaining.

In input operations, data is transferred from the I/O interface into the buffer one byte at a time, and a cycle-steal request is set when two bytes have been loaded. Further bytes of data are accepted into the buffer while the buffer is waiting for the cycle-steal response. A count is kept in hardware of the number of bytes in the buffer. The residual count of bytes required is also kept in hardware and an indication is given, during the cycle-steal operation, when this count is six or less. The two counts are compared, and a stop command is issued to the I/O device when the counts are equal. This action ensures that no more bytes will be accepted over the I/O interface than are specified by the count in the CCW.

In output operations, data is transferred during cycle-steal operations from main storage to the buffer, and another cycle-steal operation is requested if the buffer is not now full. When the I/O device requests data, provided that a byte is available in the buffer, the data is gated to the I/O interface register. A byte count is again kept in hardware; when the count reaches zero, cycle-steal requests are inhibited. A count is also kept of the number of bytes in the buffer and is reduced by 1 whenever a byte is sent over the I/O interface; this count is used to determine incorrect length. Because data is fetched from main storage ahead of its transfer to the I/O device, invalid or protected storage

indications are given before they need be recognized. When such an indication occurs, the conditions are latched in the selector channel and further cycle-steal requests are inhibited. Data transfer continues over the I/O interface for as long as bytes remain in the buffer. If the I/O device requests more data when the buffer has become empty, the incorrect length bit in the channel status byte becomes set (=1), unless the suppress length indication (SLI) flag, bit 34 of the CCW, is set.

Data Chaining

To ensure high performance, data transfer is buffered during data chaining. In input operations, the chaining involves accepting bytes into the buffer while a new CCW is being fetched; in output operations, it involves fetching the next CCW while bytes are still in the buffer awaiting transfer to the I/O device. The selector channel hardware detects when the count reaches zero and the data chaining flag is on, and requests microprogram control at the highest priority for the selector channel. The microprogram then fetches a new CCW.

In input operations, because data is accepted into the buffer during the CCW-fetch routine, no check can be kept that the number of bytes accepted will not exceed the count specified in the CCW. If the count is found to be less than the number of bytes in the buffer at the end of data chaining when cycle-stealing occurs, and if no further data chaining is indicated, chaining check is set.

In output operations, cycle-stealing for the new channel command word is inhibited until the buffer has been emptied; then any errors that are caused by the CCW-fetch routine are recognized. A copy of the old CCW address is kept so that, if the I/O device signals end before the buffer is emptied, a microprogram routine can return to that CCW. The minimum block length that can be data chained without overrun depends on both the data rate of the I/O device and the presence or absence of concurrent processing on other channels.

Command Chaining

The selector channel hardware recognizes the conditions for command chaining (channel end, device end, and no-error indications, either from the I/O device or from the channel) and it then requests microprogram control at the highest priority. The microprogram routine fetches a new CCW and reselects the device to present the new command. Control is relinquished after the command has been sent, in order to minimize the time spent at top priority. The hardware then checks for a zero-status reply from the device and generates a response that allows data transfer to begin immediately.

Data Rates

Maximum selector channel data rates are shown in Figure 9. These rates and times allow for the data requirements of control units but do *not* allow for:

1. The requirements of the byte-multiplexer channel or the integrated communications adapter.
2. The response time requirements of control units.
3. Degradation that may result because of the distance between the channel and the control unit.
4. The response time requirements of the integrated file adapter.

Selector Channel	Data Rate (bytes per second)	
	Maximum Permissible	Maximum Permissible while Data Chaining
First	1,300,000	400,000 (see Notes)
Second	1,200,000	400,000 (see Notes)
Combined (see Notes)	2,400,000	200,000

Notes:

1. Data chaining can only be maintained at this rate if a minimum count of 16 is in successive data-chaining channel command words.
2. Chaining requirements must be considered as well as data rates when assessing the feasibility of any configuration.
3. When the system includes the IFA feature and the IBM 3330 Disk Storage on a selector channel, the instantaneous data rates of devices on the other selector channel should not exceed 90,000 bytes per second.

Figure 9. Selector Channels -- Data Rates and Response Times [08298]

Error Handling

Errors detected by the selector channels are divided into three groups:

1. *Channel-data checks.* These are caused by bad parity on the bus-in line, together with the 'service in' or 'data in' signal raised.
2. *Channel-control checks.* These are raised by internal checks within the hardware or by CPU checks when the channel is in control of the data flow.
3. *Interface-control checks.* These may be caused by any one of the following:
 - a. Multiple tag check.
 - b. Parity check on bus-in, together with a raised 'status in' or 'address in' signal.
 - c. Timeouts on interface sequences.
 - d. Address mismatch on selection sequence.
 - e. 'Disconnect in' signal received from the control unit.

If a channel-control check or an interface-control check is detected, an adapter-error signal is sent to the CPU and a trap occurs if the process control switch is in the PROCESS position. Hardware cycles preserve the central data flow for logout, and control is passed to the error-handling routine in the channel. This routine generates limited logout

information and clears the channel for the next operation. The routine also reports the error by generating an I/O interruption and storing the channel status and limited channel logout when the interruption is serviced. If an I/O instruction is currently in progress, the error-handling routine stores the channel status and the limited channel logout, then sets a condition code of 1 for the I/O instruction.

Command Retry

Command retry is a control-unit-initiated procedure between the selector channel and the control unit; not all control units have this capability. No I/O interruption is required. The number of retries depends on the particular control unit.

Interruption Handling

Status is presented to the CPU by means of I/O interruptions. The selector channels set up I/O interruptions by loading interrupt buffers that are held in directly addressable control storage. These buffers hold both the address of the interrupting device and the flags for indicating the type of interruption.

Program-controlled interruptions are set when a channel command word containing a PCI flag is fetched. The CCW-fetch routine places the flag bit in a hardware register and a lower-priority routine then examines the bit to see if a PCI should be set. A copy of the current CCW address and channel status is put in directly addressable storage in the UCW to enable the CPU to service the PCI without interfering with the operation of the channel. The UCW is kept updated by the low-priority routine which follows the CCW-fetch routine.

Channel Status

Channel status is held in hardware in the selector channel. The individual bits in the channel status are hardware-controlled, except for the incorrect-length, program-check, and protection-check bits which may be set by microprogram. A channel-control check or interface-control check also causes a request for microprogram control and thus generates a program interruption condition.

Direct Access Storage Devices on Selector Channels

Direct access storage devices can be attached to two selector channels, including the IFA (channel 1, when fitted). That is, a direct access storage device which is additional to the IFA devices can be attached to only one selector channel.

Two Selector Channels With IFA

When the system includes two selector channels and the IFA feature, the additional direct access storage device

must be attached to the higher-priority selector channel. Normally, channel 2 (the "first" selector channel) has the higher priority in such a system but a Channel Priority feature is available, in association with the selector channels, to allow transfer of priority to channel 3.

The channel priority feature provides a higher command-chaining priority and allows the additional direct access storage device to be attached to channel 3 (the "second" selector channel) instead of to channel 2.

If the IBM 3330 Disk Storage is attached to either channel, the other channel should not be connected to devices with instantaneous data rates that exceed 90,000 bytes per second.

Two Selector Channels Without IFA

When the system includes two selector channels but no IFA feature (selector channels 1 and 2, in this case), a direct access storage device can be attached to both channels. Normally, only one of these attachments may be of the 3330 Disk Storage type but, in certain circumstances, arrangements may be made to allow attachment of this type of device to both channels.

BLOCK MULTIPLEXING

When one or two selector channels are fitted to the system and the block-multiplexer feature is provided, each selector channel is converted into a block-multiplexer channel. With the feature fitted, the selection of the channel mode of operation, for either block-multiplexer mode or ordinary selector-channel mode, becomes the responsibility of the programmer. The mode is implemented by the block-multiplexer control bit (bit 0, control register 0), as described in the Principles of Operation manual.

A block-multiplexer channel is usually used with control units that handle a number of I/O devices. It is most effective when the devices perform their internal mechanical and electronic operations independently of the control unit and the control unit is required only for the data transfer.

The channel is designed for relatively high-speed burst operations and is able to multiplex complete blocks of data, thereby permitting a device to disconnect only after channel end or the execution of a halt instruction. This facility allows the interleaved execution of several channel programs by one channel.

Seventeen subchannels are available on each block-multiplexer channel. Each channel can be assigned, therefore, either to two control units with up to eight I/O devices attached to each unit or to one control unit with up

to 16 I/O devices attached. The seventeenth subchannel is used for all other devices that, because of device addressing, do not use any of the first 16 subchannels. Devices assigned to the seventeenth subchannel do not block-multiplex; that is, the channel does not allow disconnection at channel-end time if chaining is indicated. The common channel microprogram is informed of the channel configuration by a plug-in byte of data in the channel hardware.

Note: If the seventeenth subchannel is employed, the block-multiplexing capability of the other 16 subchannels may be degraded by activity on the seventeenth subchannel.

Device Addressing

The device address byte, generated by the I/O instruction for a block-multiplexer channel, is regarded as two half-bytes; the more significant half-byte provides the control-unit address and the less-significant half-byte provides the address of a particular I/O device that is attached to the control unit. A reference byte of plug-in data is held in the channel hardware, and also represents two half-bytes.

The more-significant half-byte of the device address is compared with both half-bytes of reference data to determine the subchannel allocation. If a match is obtained against both reference characters, 16 subchannels are allocated for block-multiplexer operation, one to each of the 16 device addresses that contains the same more-significant half-byte.

If a match is obtained against only one character, the device address is examined again for the condition of its bit 4. If this bit is a zero, eight subchannels are allocated for block-multiplexer operation, one to each of the device addresses that contains the same more-significant half-byte; if bit 4 is a one, only one subchannel (the seventeenth) is allocated.

If no match results from the comparison, the seventeenth subchannel is again allocated to the device address.

Channel-Available Interruption Condition

A channel-available interruption condition is generated by a channel to signify that a previously indicated channel-busy condition no longer exists. The channel-available interruption condition informs the CPU program that the instruction that received a channel-busy indication (condition code 2) can now be expected to be successfully executed.

The channel-available interruption condition is meaningful only for the block-multiplexer channel, because a selector channel always terminates a channel-busy condition with an interruption or an interruption-pending condition.

STANDARD I/O INTERFACE

The System/370 standard I/O interface connects a CPU channel (byte-multiplexer or selector) to any I/O device or device control unit that is equipped with a similar interface. The interface is a set of standard electrical connections through which data and control signals are exchanged between the CPU and the attached input/output devices. (It is termed the *standard* I/O interface because its specification complies with the System/360 standard interface and because the devices made available to System/370 also comply with this specification.)

The 'data in' and 'data out' tag lines are associated with the high-speed transfer facility. 'Data in' can be alternated with the 'service in' line, and 'data out' is alternated with the 'service out' line in response to 'data in'. This arrangement provides an increase of data transfer rate to almost twice the rate that is obtained with 'service in'/'service out'.

The 'disconnect in' tag line is associated with the I/O error alert facility. The line allows a control unit to alert the system when a malfunction prevents the control unit from signaling normally or correctly across the interface, and results in a selective reset sequence being initiated to that control unit.

CONSOLE PRINTER-KEYBOARD

The console printer-keyboard provides a manual entry into storage, alter/display facilities, and a printout of program-generated messages. The printer and keyboard are physically one unit but are electrically and functionally independent; that is, the input (read) function of the keyboard is independent of the output (write) function of the printer.

The System/370 Model 135 offers a choice of two console printer-keyboards — the 3210 Model 1 (Figure 10) or the 3215 Model 1 (Figure 11). Both machines accept the same I/O commands, perform the same functions, and have the same keys, indicators, and controls (Figure 12). Both units print serially (that is, one character at a time).

The main difference between the 3210 and 3215 is in the speed and manner of printing. The 3210 prints at about 15.5 characters per second, using a spherical print element. The 3215 prints at about 85 characters per second, the characters being formed in a dot matrix by a print element that contains seven print wires in a vertical row; the ends of the wires drive against the ribbon, the paper, and the platen to form the printed character.

The adapter circuits connect the console printer-keyboard to the CPU through an interface that is controlled by microprogram. The microprogram also provides all translations from keyboard code to EBCDIC* code, and from

* EBCDIC: Extended binary-coded-decimal interchange code

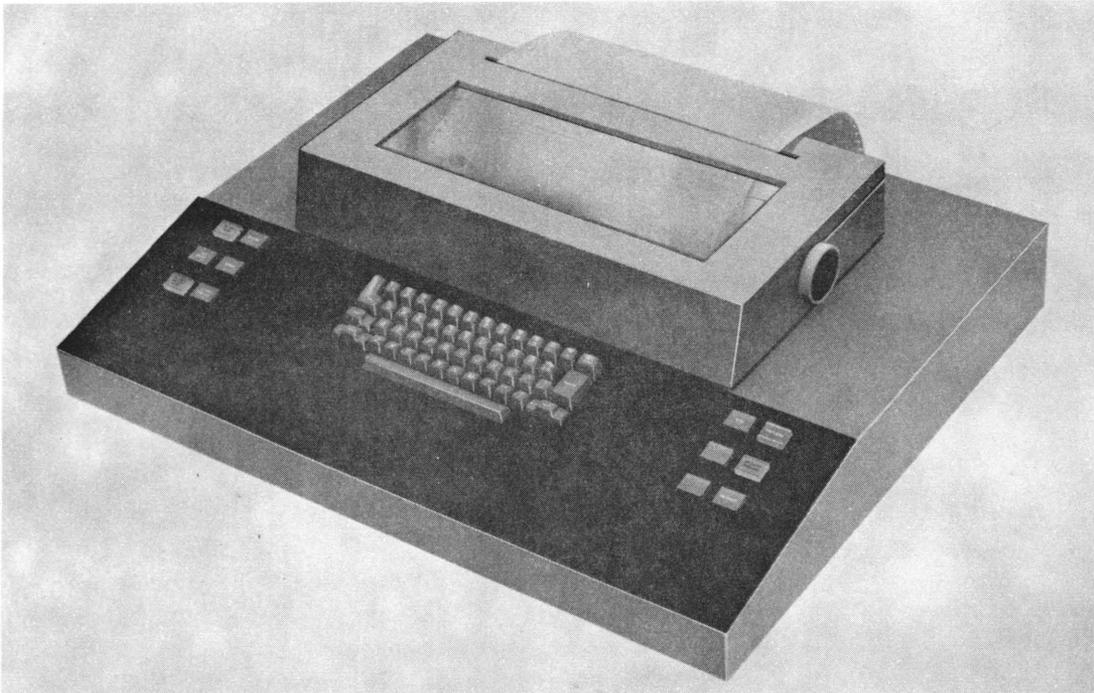


Figure 10. IBM 3210 Console Printer-Keyboard Model 1 [08299]

EBCDIC code to printer code; Figure 13 shows the EBCDIC graphic codes. The circuits provide all timing and functional controls for both keyboard and printer operations.

Through the adapter, the console printer-keyboard appears to the program as if connected to the byte-multiplexer channel (channel 0), although no standard I/O interface is involved. A byte-multiplexer channel UCW is used for program-controlled printer-keyboard operations.

The device address of the console printer-keyboard may be either 009 (hex), which is the preferred address for OS,

or 01F (hex), which is the preferred address for DOS. The choice is made by the user at the time of ordering so that the chosen address can be recorded on the initial micro-program disk of the console file. (Although the console printer-keyboard uses a byte-multiplexer device address, it does not occupy one of the eight available control unit positions.)

The alter/display function is requested by depression of the ALTER/DISPLAY pushbutton, and does not involve status or sense information. The function is not effective, however, until the CPU is in the manual stop state. See "Alter/Display Facility" later in this section.

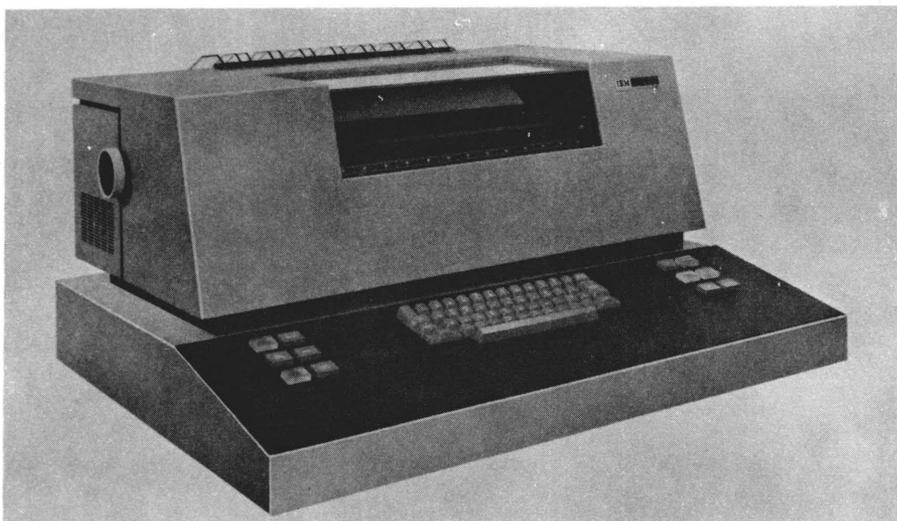
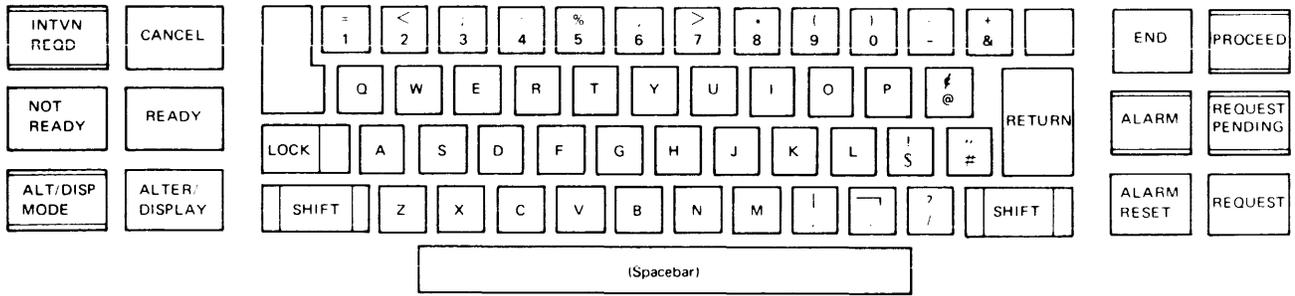
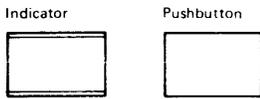


Figure 11. IBM 3215 Console Printer-Keyboard Model 1 [08300]



Legend:



INDICATORS AND CONTROL PUSHBUTTONS

Indicator	Condition
INTVN REQD	The printer is out of forms or the printer-keyboard is not ready
ALT/DISP MODE	A request for an alter/display operation was accepted
ALARM	An alarm command was issued, and manual intervention by the operator is needed
PROCEED	The printer-keyboard is unlocked and is ready to accept characters. PROCEED is lit by operation of the ALTER/DISPLAY pushbutton or by a read command
REQUEST PENDING	A request operation was initiated. The indicator goes out when the attention status is accepted by the CPU

Control Pushbutton	Function
NOT READY	Places the printer in the not-ready state
CANCEL	Is used to terminate a read command when the operator has made an error in data entry. Normally, the program will re-issue the same read command
READY	Places the printer-keyboard in the ready state when forms are in the printer
ALTER/DISPLAY	Requests or ends an alter/display operation. When used to end an alter/display operation, the printer-keyboard remains in the alter/display mode
END	Terminates a read, write, or alter/display operation
ALARM RESET	Resets the ALARM indicator
REQUEST	Requests the supervisor program to initiate a read command to the printer-keyboard, to allow the operator to enter data

CHARACTER AND FUNCTION KEYS

Character Keys: Forty-four character keys are provided. Uppercase or lowercase characters are determined by the position of the SHIFT key

Function Key	Function
SHIFT	Provides uppercase and lowercase characters
LOCK	Locks the SHIFT key in the uppercase position
RETURN	Returns the print carrier to the left margin and indexes the forms
Spacebar	Moves the print carrier one space

Figure 12. 3210 and 3215 – Keys, Indicators, and Controls [08301]

Bits 0-3	→	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
Bits 4-7	Hex →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0					SP	&	-									0
0001	1							/		a	j			A	J		1
0010	2									b	k	s		B	K	S	2
0011	3									c	l	t		C	L	T	3
0100	4									d	m	u		D	M	U	4
0101	5		NL							e	n	v		E	N	V	5
0110	6									f	o	w		F	O	W	6
0111	7									g	p	x		G	P	X	7
1000	8									h	q	y		H	Q	Y	8
1001	9									i	r	z		I	R	Z	9
1010	A					¢	!		:								
1011	B					.	\$,	#								
1100	C					<	*	%	@								
1101	D					()	-	'								
1110	E					+	;	>	=								
1111	F						¬	?	"								

SP: Space
 NL: New Line

Figure 13. EBCDIC Graphic Codes [08302]

Printer-Keyboard Command Words

The CCW command codes for the console printer-keyboard are summarized in Figure 14.

Read Inquiry (X'0A')

When the 'read inquiry' command is issued, and is accepted

by the adapter, the PROCEED indicator on the keyboard is lit, indicating that keyboard entries may be made. The adapter accepts the command only if the console printer-keyboard is in a ready state and in a not-busy condition, that is, if it is not currently performing another operation or does not have any outstanding status conditions. When

Command	Command Code Byte								Hex
	0	1	2	3	4	5	6	7	
Read inquiry	0	0	0	0	1	0	1	0	0A
Write	0	0	0	0	0	0	0	1	01
Write with automatic carrier return	0	0	0	0	1	0	0	1	09
Sense	0	0	0	0	0	1	0	0	04
Control no-op	0	0	0	0	0	0	1	1	03
Control (alarm)	0	0	0	0	1	0	1	1	0B
Transfer in channel (TIC)*	0	0	0	0	1	0	0	0	08

*This command functions in the manner described in the Principles of Operation manual.

Figure 14. Console Printer-Keyboard – CCW Command Codes [08303]

the PROCEED indicator is lit, entries made on the keyboard are processed in the following way:

1. Shift codes, uppercase or lowercase, are detected by hardware and no further action takes place.
2. All nonshift codes are gated into the keyboard data register, together with the keyboard mode bit, and a microprogram interruption is initiated.

The microprogram interruption causes the microprogram to take a data byte from the keyboard data register. The microprogram translates this data byte into EBCDIC code and stores it in main storage under control of the CCW. The microprogram also translates the data byte into printer code, sets the data into the printer data register, and causes the keyed character to be printed.

The operation is terminated by any one of the following conditions:

1. The CCW count reaches zero. When this condition occurs, the next microprogram interruption, if for a data service, causes channel end and device end to be generated.
2. The operator presses the END pushbutton. This action causes channel end and device end to be generated.
3. The operator presses the CANCEL pushbutton. This action has the same effect as in item 2, but the unit-exception status bit (bit 7) is included in the status; an asterisk character is printed to signify that the operation was canceled.

At channel-end time, an automatic carrier-return and line-feed operation is initiated.

Write (X'01')

The 'write' command is implemented by the adapter circuits, provided the console printer-keyboard is not busy and is in the ready state. Data is fetched from main storage, under control of the CCW, by printer-generated microprogram interruptions that are related to the mechanical timings of the device. The fetched data byte is translated into printer code and is placed in the printer data register. The specified operation is then performed.

The write operation is terminated by any one of the following conditions:

1. The CCW count reaches zero. This causes channel end and device end to be generated in response to the next data service microprogram interruption.
2. The operator presses the END pushbutton. This action causes the operation to be ended at the next microprogram interruption, by generating channel end, device end, and unit exception status. An asterisk character is printed.

During the write operation, the keyboard is locked.

Write With Automatic Carrier Return (X'09')

The 'write with automatic carrier return' command is of the same type as 'write', except that an automatic carrier-return

and line-feed operation is initiated when channel end and device end are presented.

Sense (X'04')

The 'sense' command is performed by the adapter microprogram. No mechanical movement takes place in the console printer-keyboard. The microprogram puts the sense byte into the area designated by the CCW and terminates the operation by setting channel end and device end status into the adapter.

Control No-Op (X'03')

The 'control no-op' command is treated as an immediate operation. A CSW is stored, with the channel-end and device-end bits (bits 4 and 5) set in the unit status portion. A condition code of 1 is set up. No action is initiated in the adapter hardware or in the console printer-keyboard.

Control (Alarm) (X'0B')

The 'control (alarm)' command is treated as an immediate operation in the same way as the 'control no-op' command, except that the audible alarm in the CPU is operated and the ALARM indicator on the console printer-keyboard is lit; the ALARM indicator goes out when the ALARM RESET pushbutton is pressed. The audible alarm switches off automatically after one and one-half seconds.

Unit Status Byte

The unit status byte is kept in the adapter hardware and has the following format:

<i>Bit</i>	<i>Designation</i>
0	Attention
1	(Not used)
2	(Not used)
3	Busy
4	Channel end
5	Device end
6	Unit check
7	Unit exception

Status Bit 0 (Attention)

The attention bit is set when the operator presses the REQUEST pushbutton on the keyboard, provided that the state of the adapter complies with the following conditions:

1. It is not busy executing a command.
2. It is not between device end and reselection, in command chaining.
3. It has no other outstanding status.
4. It is in a ready state.

The attention bit, when set, causes a microprogram interruption (status). The microprogram, when interrupted, attempts to set up an I/O interruption, through the channel 0 'interrupt request' latch. The attention bit is reset when the I/O interruption that it initiated is cleared.

Status Bit 3 (Busy)

The busy bit is set by the microprogram if any outstanding status condition exists at command initiation.

Status Bit 4 (Channel End)

The channel-end bit is set for the following conditions:

1. In 'start I/O immediate' commands, the bit, with device end (bit 5), is set by the microprogram.
2. In other start I/O commands, the bit is generated by the microprogram from the hardware 'terminal status' latch when a program interruption is being set up at the completion of data transfer.
3. In test I/O commands, the bit is generated by the microprogram from the hardware 'terminal status' latch when the subchannel is busy and the console printer-keyboard has an interruption pending.

Status Bit 5 (Device End)

The device-end bit is set by the microprogram for all immediate commands. The condition of the 'terminal status' latch in the hardware sets the device-end bit in other commands.

Status Bit 6 (Unit Check)

The unit-check bit is set whenever error conditions, which are represented by sense bit 0 or 3, arise; it is also set, alone, at command initiation time if sense bit 1 is set. See "Restart Procedure". The unit-check bit is presented, with either the channel-end bit or the device-end bit, if any error conditions arise during an operation. When set, unit check inhibits command chaining.

Status Bit 7 (Unit Exception)

The unit-exception bit is set if the CANCEL key on the keyboard is pressed during a read operation or when the END key is pressed during a write operation. The bit is presented with the channel-end bit, which is generated at the same time. When set, unit exception inhibits command chaining.

Channel Status Byte

The channel status byte is kept in the UCW of the adapter and has the following format:

Bit	Designation
0	Program-controlled interruption
1	Incorrect length
2	Program check
3	Protection check
4	Channel data check = 0
5	Channel control check
6	Interface control check = 0
7	Chaining check = 0

Bits 4, 6, and 7 cannot be set. Bits 0 through 3 and 5 are defined in the Principles of Operation manual.

Sense Byte

The sense byte has the following format:

Bit	Designation
0	Command reject
1	Intervention required
2	(Not used)
3	Equipment check
4	(Not used)
5	(Not used)
6	(Not used)
7	(Not used)

Sense Bit 0 (Command Reject)

The command-reject bit is set by the microprogram during command initiation time if an invalid command is sent to the adapter. No attempt is made to perform the command, and a unit-check status is presented.

Sense Bit 1 (Intervention Required)

The intervention-required bit is set by the adapter hardware if either the adapter is in a not-ready state or the end-of-forms switch in the console printer-keyboard is operated. These conditions do not affect an operation that is in progress when they arise. If they exist at command initiation time, however, the operation is immediately terminated either by status storing and the setting of a condition code of 1 (in the case of a start I/O instruction) or by "breaking" of the chain (if command chaining is being used).

Sense Bit 3 (Equipment Check)

The equipment-check bit is set by the hardware if a keyboard output has bad parity. The parity is corrected before being sent to the CPU, but the presence of the equipment-check bit causes the unit-check status bit to be presented with the channel-end bit.

Alter/Display Facility

The alter/display facility provides access to various CPU storage areas and the means of either altering or displaying the contents of these areas. Through the console printer-keyboard, a printout record of alter/display operations is obtained.

The alter/display function is initiated as follows:

1. The STOP pushbutton on the system control panel of the CPU is depressed.
2. The MANUAL indicator on the system control panel is lit, indicating that the system has entered the manual stop state.
3. The ALTER/DISPLAY pushbutton on the console printer-keyboard is depressed.
4. The ALT/DISP MODE indicator on the console printer-keyboard is lit and a carrier-return and line-feed operation occurs.

5. The PROCEED indicator on the console printer-keyboard is lit, indicating that the alter/display operation may begin.

The type of function that is required and the storage area to which access is required are specified by a two-character mnemonic. The first character must be either "A" (to specify alter) or "D" (to specify display), and the second character must be one of the designations shown in Figure 15, to specify the storage area required.

Mnemonic Characters		Definition	Associated Address Length
First	Second		
A		Alter	
D		Display	
	M	Main storage	6
	S	Control storage (see Note)	4
	G	General register	1
	F	Floating-point register	1
	P	PSW	0
	C	Control register	1
	K	Storage protection key	6

Note: The 'alter' operation cannot be performed on control storage

Figure 15. Alter/Display Function Mnemonics [08304]

When the second character (except "P") of the mnemonic is entered, a space is printed automatically and the required address within the storage area specified must then be entered in hexadecimal notation (see Figure 15). If the second character of the mnemonic is "P" (meaning PSW), no address or register number is necessary and a new line is taken automatically.

If the alter function has been specified, the microprogram accepts further hexadecimal data from the keyboard and places it in the specified storage location. If display has been specified, the console printer-keyboard prints out the data that is contained in the specified storage location. The microprogram accepts uppercase or lowercase characters from the keyboard, but the printer output is in uppercase characters.

If any of the following conditions occurs, the character that has been keyed in is not printed:

1. The first character entered for the mnemonic is neither "A" nor "D".
2. The second character entered is not one of those specified for storage locations.
3. The feature referred to is not fitted.
4. Any data character is not a valid hexadecimal code.

No action is taken for these conditions, but the adapter waits for the correct key entry to be made and normal operation is then continued.

Storage Address

The address or register number of the location specified for

the alter/display function must be of the correct length for the mnemonic and must consist of valid hexadecimal characters. If not, or if the storage address is invalid (that is, outside the range of storage) or if a floating-point register number is not 0, 2, 4, or 6, the message ?ADR is printed. A new line is then taken and the keyboard is set up for a new operation.

Storage protection does not apply to alter/display operations because the protection key of 0 is used. The address for the storage-protection key function does not have to be on any special boundary.

Data Format

All alter/display functions are formatted in words of eight digits and the words are separated by double spaces, with up to eight words per line. The spacing and carrier controls are provided automatically.

If the storage address is not on a fullword boundary, spaces are provided automatically in the first word so that subsequent groups of eight digits represent fullwords on boundaries. The operation continues indefinitely, unless terminated. New lines are taken as necessary until the end of the storage area is reached. A new line is then taken, and the message ?ADR is printed if an attempt is made to alter or display an invalid address.

The format of the PSW consists of one line of two words.

The register operations for floating-point registers are formatted in one line and for general registers and control registers in two lines, with eight words per line. Each operation starts from the register number that is specified and continues, wrapping around to 0 as necessary, until all registers are altered or displayed.

Storage keys are also formatted as words of eight digits. Each word consists of 4 two-digit keys for successive 2048-byte blocks of storage. When the end of storage is reached, a new line is taken and the message ?ADR is printed if an attempt is made to alter or display the invalid address.

Termination

An alter/display operation is terminated by any of the following conditions:

1. An invalid address was specified initially.
2. The end of the storage area is reached or all registers have been dealt with.
3. The ALTER/DISPLAY pushbutton is pressed again during an alter/display operation.
4. The END pushbutton is pressed during the operation.

For items 1 and 2, an error message is printed, a new line is taken, the carrier returns, and the console printer-keyboard is set up for a new operation. Similar actions result for item 3, except that no error message occurs. For item 4, a new line is taken, the carrier returns, the ALT/DISP MODE indicator goes out, and the system returns to the CPU manual stop state.

Sense Byte Information	Suggested Action for Programmer	Recommended Action for Operator
Command reject (sense bit 0)	Issue a message to the operator to say that the last program command failed. The program could then try to repeat the command that failed	None
Intervention required (sense bit 1)	Issue the 'control (alarm)' command	Insert a fresh supply of paper. Press the READY pushbutton
Equipment check (sense bit 3)	Issue a message to the operator to say that the program has been notified of an error. Optionally, the program could then either: <ol style="list-style-type: none"> 1. Branch to an error recovery routine (for example) to repeat the last operation 2. Regard the console printer-keyboard as inoperative 	None

Figure 16. Summary of Recommended Actions after Unit Check from Console Printer-Keyboar [08305]

Restart Procedure

When unit check is detected in the CSW, the program should issue the sense command to the console printer-keyboard and proceed according to the information received in the sense byte (Figure 16).

Integrated Adapters

The integrated adapter features of the System/370 Model 135 serve important input/output devices in the system, permitting these devices to be connected directly to the CPU without the need for the usual interface/control unit combination. The following features are available:

- Integrated communications adapter (ICA)
- Integrated file adapter (IFA).

INTEGRATED COMMUNICATIONS ADAPTER

The integrated communications adapter provides for line communication between the system and communication terminals and/or other computers at remote locations.

Up to eight communication lines of various types can be attached through the ICA. Each line appears to the system to be a subchannel of the byte-multiplexer channel. A modem, outside the System/370 Model 135, is required for each line.

Note: The user is cautioned that unrecoverable overrun may occur if the total CPU interference by all ICA lines exceeds the available percentage time that remains when selector channel or IFA operations have been provided for. Approximate percentage interference per line for each type of adapter is given in this section.

Types of Communication Line

Adapters

The integrated communications adapter provides up to eight adapters that are equivalent to the following features of the IBM 2701 Data Adapter Unit:

- IBM Terminal Adapter Type I Model II
- IBM Terminal Adapter Type III
- Synchronous Data Adapter Type II.

The equivalent of the Terminal Adapter Type I Model II allows one of the following systems or devices to be connected at the remote end of the line:

- IBM 1050 Data Communication System
- IBM 2740 Communication Terminal Models 1 and 2
- IBM 2741 Communication Terminal Model 1
- IBM System/7.

The equivalent of the Terminal Adapter Type III allows the following devices to be connected at the remote end of each line:

- IBM 2845 Display Control Model 1 (for the IBM 2265 Display Station Model 1)
- IBM 2848 Display Control Model 3 (for the IBM 2260 Display Station Model 1)
- IBM 2848 Display Control Model 1 or 2 (for the IBM 2260 Display Station Model 2).

The equivalent of the Synchronous Data Adapter Type II allows any synchronous device that conforms to the IBM specification for binary synchronous communication (as defined in the IBM publication *General Information – Binary Synchronous Communications*, GA27-3004) to be connected at the remote end of the line. The following list shows some of the devices in this category:

- IBM System/3 Model 6 and Model 10
- IBM System/360 or System/370 with either an IBM 2701 Data Adapter Unit or an IBM 2703 Transmission Control
- IBM System/360 Model 20 with a Binary Synchronous Communications Adapter
- IBM System/360 Model 25 with ICA having a Synchronous Data Adapter
- Another IBM System/370 Model 135 with a Synchronous Data Adapter Type II (equivalent) feature
- IBM 1130 Computing System
- IBM 1800 Data Acquisition and Control System
- IBM 2770 Data Communication System
- IBM 2780 Data Transmission Terminal
- IBM 2790 Data Transmission System.

The hardware of the basic ICA is common to all attached communication lines. The adapters can be used in any combination and are incorporated in the system according to the type of device to be attached. Adapter control is by microprogram.

Modems

In addition to the appropriate adapter, each communication line that is attached to the system requires an external modem. Details of communication facilities that are suitable for ICA operation are given in *IBM System/370 Model 135 Configurator (U.S.A. only)*, GA33-3006, and *IBM System/370 Model 135 Configurator (Countries other than U.S.A.)*, GA19-0044.

Data Rates

For a communication line that uses clocking signals derived from the System/370 Model 135, the integrated communications adapter can provide any data rate up to 600 bits per second (nominal). It can also provide a rate of 1,200 bits per second (nominal).

Data rates on a line using a self-clocking modem are limited only by the particular modem used, up to a maximum of 4,800 bits per second.

Internal I/O Interface

The integrated communications adapter uses the internal I/O interface of the CPU. On this interface, the ICA has priority 8 for data service and priority 10 for status handling. The ICA does not provide metering signals, but

the 'metering in' signal is raised by the CPU logic when zone 4 of work storage is selected and a main-storage access operation is taking place.

Modem Interface

The interface to the modem, provided by each modem adapter, is capable of handling data rates up to 4,800 bits per second and conforms to the following specifications:

- CCITT* V24 (International)
- EIA* RS232C (U.S.A.)
- NTTPC* Gazette Number 2147 (Japan).

The adapter for CPU-clocked modems provides the following interface lines:

<i>In</i>	<i>Out</i>
Received data	Transmitted data
Ready for sending (Clear to send)	Request to send
Data set ready	Data terminal ready
Calling indicator (Ring indicator)	-
Received line signal detected (Data carrier detected)	-

The adapter for self-clocking modems provides the foregoing interface lines and the following lines.

<i>In</i>	<i>Out</i>
Transmitted signal element timing	New sync
Received signal element timing	-

Operation

The operation of the integrated communications adapter is similar to that of the 2701 Data Adapter Unit and of the associated terminal transmission adapters corresponding to the ICA adapter features. Detailed information on the 2701 and on terminal adapters is given in *IBM 2701 Data Adapter Unit Principles of Operation*, GA22-6864, and in *IBM 2701 Data Adapter Unit Original Equipment Manufacturers' Information*, GA22-6844.

Operations within the ICA are implemented and controlled by microprogram. The microprogram is compiled according to the line configuration specified by the user.

Unit Addresses

Each communication line that is attached to the integrated communications adapter has a byte-multiplexer channel

* CCITT: International Telephone and Telegraph Consultative Committee
 EIA: Electronic Industries Association
 NTTPC: Nippon Telephone and Telegraph Public Corporation

unit address. If one line is installed, it must have address 001 (hex); if two lines are installed, they must have addresses 001 and 002 (hex); similarly, for any number of lines installed, the addresses must be consecutive — starting at 001 (hex) and not exceeding 008 (hex).

System and Channel Reset

Any event that causes a System/370 Model 135 system reset or a byte-multiplexer channel reset also causes an ICA reset. In this state, all Terminal Adapter Type I Model II (equivalent) lines are disabled, all Terminal Adapter Type III (equivalent) lines are placed in a partially disabled condition, and all Synchronous Adapter Type II (equivalent) lines receive a mode reset.

Status Byte

The status byte definition for the integrated communications adapter is the same as that of the 2701. Channel-end and device-end status always occur together.

Sense Byte

Each attached communication line has a specific sense field of one byte in control storage. Three bits of the sense byte have a common definition, independent of the type of line, as follows:

1. Bit 0 (command reject) is set if a command is invalid for the type of line.
2. Bit 2 is always at 0.
3. Bit 5 (overrun) may be set during read or write operations if the instantaneous data rate of *all* channels and *all* integrated devices is excessive. The bit may also be set if the Model 135 has been in hardstop during the I/O operation.

Other bits of the sense byte are defined as for the 2701.

Common I/O Instructions

The 'test I/O' and 'halt I/O' instructions for the integrated communications adapter are the same as those defined for the 2701. The 'halt device' instruction is executed as a halt I/O operation.

Errors

A hardware error in the integrated communications adapter causes a channel check, with channel logout information placed in main storage locations 368 through 371. Any data transfer operations that are in progress when the error occurs are terminated with channel end, device end, unit check, and overrun.

Terminal Adapter Type I Model II (Equivalent) Feature

A communication line that is operating as if a Terminal Adapter Type I Model II is attached accepts the same

control characters as does a Terminal Adapter Type I and uses the following command codes:

Code	Command
X'01'	Write
X'02'	Read
X'03'	No op
X'04'	Sense
X'05'	Diagnostic write
X'06'	Prepare
X'0A'	Inhibit
X'0D'	Break. This command is accepted only if the addressed line is equipped with the read-interruption feature
X'12'	Diagnostic read
X'27'	Enable
X'2F'	Disable

Data Rates

The data rate can be either 134.5 bits per second or 600 bits per second.

Write Interruption Feature

The write interruption feature within the Terminal Adapter Type I Model II (equivalent) feature is compatible with the receive-interrupt feature on the 2741 Communication Terminal and allows the terminal operator to interrupt a transmission from the System/370 Model 135.

During a write operation, the 'received data' line is monitored. If this line remains at space for the whole of one character time, the 'write' command is ended with channel end, device end, and unit check in the status byte and intervention required in the sense byte.

Read Interruption Feature

The read interruption feature within the Terminal Adapter Type I Model II (equivalent) feature allows the program to interrupt a transmission from the terminal. The 'break' command OD (hex) causes the transmitted data line to be held at space for the number of character times specified in the byte count field of the CCW. (A 'character time' is 15 milliseconds at 600 bits per second, and 66.7 milliseconds at 134.5 bits per second.)

Unit Exception Feature

If a line is equipped with the unit-exception feature, unit exception will not be set in response to a © signal. This feature is compatible with the 2741-break feature on the 2703 Transmission Control (see *IBM 2703 Transmission Control, Component Description, GA27-2703*).

Interference

When the integrated communications adapter is in the Terminal Adapter Type I Model II (equivalent) mode, interference with CPU operations is less than 200 micro-

seconds per byte per line. With all eight lines operating at 134.5 bits per second and transferring data simultaneously, CPU interference is approximately 2.2%. With all eight lines operating at 600 bits per second and transferring data simultaneously, CPU interference is about 11% (see Footnote).

Terminal Adapter Type III (Equivalent) Feature

A communication line that is operating as if a Terminal Adapter Type III is attached (with a remote 2845/2848 Display Control) accepts the same control characters as does the Terminal Adapter Type III and uses the following command codes:

Code	Command
X'01'	Write
X'02'	Read
X'03'	No op
X'04'	Sense
X'05'	Diagnostic write
X'06'	Diagnostic read
X'41'	Write break
X'42'	Read clear

Data Rates

The data rate that is available depends on the type of modem used by the line. If clocking is provided by the CPU, the data rate is 1,200 bits per second (nominal). If a self-clocking modem is used, the data rate is 2,400 bits per second.

Interference

When the ICA is in the Terminal Adapter Type III (equivalent) mode, interference with CPU operations is less than 100 microseconds per byte per line. If all eight lines use this feature and transfer data simultaneously, CPU interference is less than 24% (see Footnote).

Synchronous Data Adapter Type II (Equivalent) Feature

When the ICA is equipped with the Synchronous Data Adapter Type II (Equivalent) feature, the CPU can communicate with any IBM computer, multiplexer device, or terminal that conforms to the IBM specifications for binary synchronous communication.

For leased line operation, the network can be of either the centralized-multipoint type or point-to-point type. In a centralized-multipoint network, each ICA communication line can operate either as a control station or as a tributary station. For switched public network operation, the communications facility must be point-to-point, half-duplex.

Programs that cause the ICA to operate as a tributary

Note: These percentages are average values, valid for a period of about 1 second. Peak values may be significantly higher, and need careful evaluation when the total load on a system is assessed.

station normally use the 'address prepare' command. This command is provided as part of the ICA tributary station feature. (The ICA tributary station feature is equivalent to the Station Selection feature on the 2701.)

An ICA line that is used neither as a control station nor as a tributary station operates only in point-to-point mode in the same way as a (2701) Synchronous Data Adapter Type II.

No provision is made in the Synchronous Data Adapter Type II (equivalent) feature for noncentralized-multipoint operation. 'Search' commands are always rejected.

Each binary synchronous communication line of the ICA accepts the same control character as the (2701) Synchronous Data Adapter Type II and uses the following command codes:

Code	Command
X'01'	Write
X'02'	Read
X'03'	No op
X'04'	Sense
X'06'	Prepare
X'09'	Poll
X'23'	Set mode
X'27'	Enable
X'2F'	Disable
X'0E'	Search. This command is always rejected. No provision is made for noncentralized-multipoint operation
X'1E'	Address prepare. This command is accepted only if the line that is addressed is equipped with tributary station feature
X'29'	Dial. This command is always rejected. No autocal feature is provided

Data Code Features

The following data code options are available for the binary synchronous communication line:

1. EBCDIC data code feature.
2. ASCII data code feature.
3. Six-bit transcode feature. This feature is used only if a 2780 Data Transmission Terminal is connected.

A transparency mode feature provides for the transmission of all possible bit patterns within the selected code level. A dual-code feature permits a second code, selected from the three options, to be used as an alternate code. The alternate code is brought into use by the 'set mode' command.

Set Mode Command

The 'set mode' command transfers a byte of data from main storage to the line control word. The definition of the byte is as follows:

Bit	Function
0, 6, 7	(Ignored)
1	When on, bit 1 sets the Intermediate Block Check mode as in the 2701
2	(Ignored. No dual communications interface feature is provided on the ICA)
3	When on, bit 3 causes test mode to be simulated
4	When on, bit 4 selects the alternate code if the line is equipped with the dual-code feature
5	(Ignored. Attention interruptions cannot occur on the ICA)

Data Rates

When clocking is provided by the CPU, a binary synchronous communication line can have a data rate of either 600 bits per second or 1,200 bits per second, whereas with a self-clocking modem, the line can have any data rate up to 4,800 bits per second. Also, when clocking is provided by the CPU, an oscillator having a frequency tolerance of 0.01% is used.

Interference

Interference with CPU operations for the various data-rate modes is as follows:

1. With clocking provided by the CPU: Less than 200 microseconds per byte per line, and less than 24% when all eight lines are used simultaneously (see Footnote).
2. With a self-clocking modem: Less than 70 microseconds per byte per line, and less than 4.2% for one line at 4,800 bits per second (see Footnote).

When no data is being transferred but the line is enabled, the CPU interference rate is slightly less than if data were being transferred. When the line is disabled, CPU interference is less than 0.01% per line (see Footnote).

Timeouts

Timeouts are imposed in the same way as for the (2701) Synchronous Data Adapter Type II. The 1-second, 3-second, and 6-second timeouts have the same nominal values and a tolerance of ± 60 milliseconds.

Error Checking

The method of checking the binary synchronous communication line for line errors is the same as for the (2701) Synchronous Data Adapter Type II.

INTEGRATED FILE ADAPTER

The integrated file adapter provides for the attachment of the 2319 Disk Storage Model A1 (containing three disk

Note: These percentages are average values, valid for a period of about 1 second. Peak values may be significantly higher, and need careful evaluation when the total load on a system is assessed.

storage modules), plus either one of the following devices in the IBM 2314 Direct Access Storage Facility – A Series:

2312 Disk Storage Model A1 (containing one disk storage module)

2318 Disk Storage Model A1 (containing two disk storage modules).

The 2319 constitutes the minimum configuration for the integrated file adapters. When this device is connected to the IFA, the additional access mechanisms can be attached, up to a maximum of five disk storage modules.

Each disk storage module requires an IBM 2316 Disk Pack as the storage medium. The disk storage equipment provides the following processing facilities:

1. A storage capacity of 29,176,000 bytes on each 2316 Disk Pack.
2. An average access time of 60 milliseconds.
3. Up to 145,000 bytes of data are available in each disk pack in a single access operation.
4. Data is transferred to the CPU at a rate of 312,000 bytes per second.
5. Up to five disk storage modules can be attached.
6. The 2316 is compatible with any device in the 2314 Direct Access Storage Facility – A Series that is used in System/360.
7. Each disk pack takes about two minutes to change.

The integrated file adapter provides the following direct-access storage capabilities for the System/370 Model 135:

1. The interpretation and execution of channel commands for the operation of the disk storage modules.
2. The translation of data as it is moved between the serial-by-bit disk storage modules and the parallel-by-byte system data flow.
3. The checking of the validity of the information that is transferred to or from the disk packs.
4. The furnishing of operating status information to the system.

The integrated file adapter also provides file-scan and record-overflow facilities. The file-scan feature gives an automatic and rapid search of the disk pack for specifically stated argument conditions. The record-overflow feature enables the processing of logical files that extend beyond the end of a disk track and continue on the next track.

Mode of Operation and Usage

Detailed information on the disk-file data format, track format, record capabilities, basic commands, access mechanisms, and module operating controls is contained in *IBM System/360 Component Descriptions – 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control, GA26-3599*.

The integrated file adapter simulates, functionally, a system selector channel with I/O control unit and provides the necessary data transfer rate. Data is transferred by cycle-steal operations. The IFA circuits are connected

internally and, therefore, the channel interface controls are not required. The IFA is addressed as selector channel 1 and operations are programmed on the same principles as for I/O devices that are connected to this channel through control units.

Data is transferred one byte at a time between the CPU and the IFA over nine bit lines; the nine bits, including the parity bit, are transferred in parallel-by-byte mode. Data is transferred between the IFA and a disk storage module in serial-by-bit mode; the parity bit is not transferred to the disk pack but, instead, cyclic-check bytes are written with the data and are checked when the data is read (cyclic checking).

The conversion of information from parallel-by-byte to serial-by-bit or from serial-by-bit to parallel-by-byte is provided by the integrated file adapter.

Data transfers from the IFA cause interference of approximately 20% to all channels and integrated adapters. Command chaining from the IFA can increase interference to a maximum of 36%, except to the high priority selector channel.

Cyclic Checking

The disk pack data is stored in and retrieved from areas that contain one or more fields. Capacity is more effectively used by associating 32 check bits with each storage area, rather than one bit with each byte.

When data is transferred from the CPU to a disk pack, the integrated file adapter removes the parity bit from each byte. The IFA then computes the 32 check bits in the form of two cyclic-code bytes and two bit-count-appendage bytes (in this text, called *bit-count* bytes); the cyclic-code and bit-count bytes are written at the end of each storage area. The four bytes are arithmetically coded from the information that is being written into the associated area. Subsequently, when the area is read from the disk pack, the IFA recomputes the check information and compares it with the check bytes read from the associated area. Because the check bytes are located at the end of each area, the IFA cannot complete the check until the entire area is read.

The integrated file adapter can also read and check data that has been written without the bit-count bytes. This format writes a byte CC (hex) following the two cyclic-code bytes. When an area is rewritten, the bit-count bytes are added, and are used in subsequent reading operations. The record length requirements remain the same because the bit-count bytes are written in byte positions that were previously used for the gap.

Command Requirements

The disk storage facilities of the System/370 Model 135 use the standard channel instructions and commands of the System/360, but the channel-interface control sequence is

not required. Data and control information is transferred directly between the disk-storage areas and CPU main-storage areas.

The complex format of the disk-storage area needs several commands, in a command-chaining sequence, to search for a record and process it. Disk-storage operations, whether for initialization or for application runs, include the following sequences:

1. A 'set file mask' command is issued. This command sets up a file-protection mask to prevent the execution of commands that should not operate on the disk-pack area that is being selected. For example, the mask can be set up to prevent any write commands being executed.
2. A seek operation is performed for the read/write heads to access the desired disk-pack area. A specific track and cylinder can be reached through use of the 'seek' or 'seek cylinder' commands. (In the IFA, these two commands perform the same function.) A specific track within the currently-selected cylinder can be reached by the 'seek head' command.
3. An operation that does not require a search (such as the 'write home address' command) can then be executed, provided it is permitted by the file-protection mask. If, however, a specific record must be found, a search must be performed first.

If an equal comparison is not obtained for any identity on the disk track, the search can be programmed to continue to the next track. This operation can be performed through a new 'seek' command or through use of the multiple-track mode. A no-record-found sense indication is available in the integrated file adapter if the identity cannot be found on the track (non multiple-track mode operation). The unit check status bit is set in the CSW when a no-record-found condition occurs.

Input/Output Instructions

Five input/output channel instructions are used to initiate operations or to test the disk attachment control:

- Start I/O
- Test I/O
- Halt I/O
- Halt device
- Test channel

Operational Commands

The commands that are recognized by the integrated file adapter for operation of the disk-storage attachments are classified as control, sense, read, write, and search commands; the individual commands within these classes are shown in Figure 17. These commands are presented to the integrated file adapter in the first byte of each CCW from the CPU. Any other command configuration, except that of the 'transfer in channel' command, is considered invalid by the IFA.

The commands are chained to execute the desired sequence of events, the 'transfer in channel' command being used to repeat search commands until the desired area is located. A read or write command is then given for the desired data. Each of the channel commands is acted upon in the same manner as for a control unit connected to a System/360 channel. The status is returned after initialization and at the completion of the operation. Sense information is developed for unusual conditions and is available through the sense command. If a parity error occurs during transfer of the CCW, a machine-check occurs.

The 'no operation' command is the only command that is processed as an immediate command. Certain conditions of operation arise when the integrated file adapter is performing automatic functions, however, that prevent the 'no operation' command from returning device-end status with the initial status. Commands such as 'restore' are not processed as immediate commands, even though they perform no operation.

The SLI flag must be set with the 'restore' and 'recalibrate' commands because the condition of no data being transferred causes an incorrect-length indication. The 'no operation' and 'space count' commands may also cause this interruption under some conditions.

In normal operation, a repeated search or read command continues to operate in the same track of the disk until the index point is passed twice. If bit 0 of the command code in the CCW is set to one, the integrated file adapter advances the head selection each time the index point is passed until the end of the cylinder is reached. This procedure (multiple-track operation) allows a more rapid search or read sequence to be performed.

Control Commands

Control operations (see Figure 17) do not involve a transfer of data records between the disk storage modules and the CPU. In certain operations, however, control bytes are transferred between the CPU and the integrated file adapter to enable the operation to take place. These bytes are parity-checked during transfer.

No Operation (X'03')

The 'no operation' command does not cause any action at the integrated file adapter, but it is the only one that the IFA process as an immediate command. Channel-end and device-end status are presented by the IFA at initial selection in response to the command, unless the disk storage module is completing a formatting-write operation and the 'no operation' command is chained to it; in this case, zero initial status is given, and channel-end and device-end status are presented to the channel after the remainder of the track has been erased.

The 'no operation' command should not be used

Command Type	Command Name	Hexadecimal Code	
		Single Track	Multitrack
CONTROL	No operation	03	—
	Recalibrate	13	—
	Restore	17	—
	Set file mask	1F	—
	Seek	07	—
	Seek cylinder	0B	—
	Seek head	1B	—
	Space count	0F	—
SENSE	Sense I/O	04	—
READ	Read data	06	86
	Read key and data	0E	8E
	Read count, key and data	1E	9E
	Read home address	1A	9A
	Read record R0	16	96
	Read count	12	92
	Read IPL	02	—
WRITE	Write data	05	—
	Write key and data	0D	—
	Write count, key and data	1D	—
	Write home address	19	—
	Write record R0	15	—
	Write (special) count, key and data*	01	—
	Erase	11	—
SEARCH	Search equal ID	31	B1
	Search high ID	51	D1
	Search equal or high ID	71	F1
	Search equal key	29	A9
	Search high key	49	C9
	Search equal or high key	69	E9
	Search equal HA	39	B9
	Search equal key and data**	2D	AD
	Search high key and data**	4D	CD
	Search high or equal key and data**	6D	ED
	Continue scan equal†	25	A5
	Continue scan high†	45	C5
	Continue scan high or equal†	65	E5
	Continue scan, no compare†	55	D5
Continue scan, set compare†	75, 35	F5, B5	

* Used with record overflow

** Used with file scan

† Used with file scan with record overflow

Figure 17. Integrated File Adapter – Operational Commands [08306]

indiscriminately because it resets orientation information in the integrated file adapter. For example, if the command is inserted between a 'read count' command and a 'read data' command, it changes the operation so that the data field area is in the next record (that is, the record *after* that in which the count field is read). Also, if 'no operation' commands are inserted after search commands in command chains, any no-record-found indications (sense byte 1, bit 4) and missing-address-mark indications (sense byte 1, bit 6) are suppressed. Because a no-operation CCW does not cause data transfer, the SLI flag should be set to avoid an incorrect length check.

Recalibrate (X'13')

The 'recalibrate' command causes the access mechanism for the designated disk pack to seek to head 0 and cylinder 0. Channel end is generated about 15 milliseconds after the integrated file adapter has accepted the 'recalibrate' command. Device-end status is presented to the channel when the operation is completed. The setting of the file-protection mask affects the 'recalibrate' command in the same way as it affects the seek commands.

'Recalibrate' is not processed as an immediate command at initial selection. The integrated file adapter returns a zero-status byte if the recalibrate CCW is accepted. The SLI flag should be set in any recalibrate CCW, therefore, because no data is transferred.

Restore (X'17')

The 'restore' command does not directly affect the disk storage modules. When the command is given, the integrated file adapter presents zero initial status, followed immediately by the final status of channel end and device end.

The 'restore' command is not processed as an immediate command. Because no data transfer occurs, the SLI flag should be set in the restore CCW. The command is performed regardless of the state of the file-protection mask.

Set File Mask (X'1F')

Execution of the 'set file mask' command causes one byte of data to be transferred from CPU main storage to the integrated file adapter; this byte specifies the write and seek commands that the access mechanism is allowed to execute. If a write or seek command that violates the file-protection mask is subsequently issued (following the set-file-mask CCW in the same chain), that command is not executed, and unit-check status is presented to the channel by the integrated file adapter. If a write command was not executed, a subsequent 'sense I/O' command obtains sense information and the file-protection and command-reject bits are set; if a seek command was not executed, only the file-protection bit is set. The file-protection indication takes precedence over the end-of-cylinder indication. Hence,

when the file-protection bit is detected, the end-of-cylinder sense bit is not set.

The 'set file mask' command can be issued once at any point in a command chain. At the completion of the chain, the file-protection mask is reset to all zeros. A system reset or a selective reset causes any file mask in the integrated file adapter also to be reset to all zeros. If a 'start I/O' instruction is subsequently issued, and a set-file-mask CCW is not in the chain being used, the following conditions apply:

1. All seek commands are permitted.
2. 'Write count, key and data', 'write key and data', and 'write data' commands are permitted.
3. 'Write home address' and 'write record RO' commands are not permitted (bits 0 and 1 of the file-protection mask are set to zeros).
4. Any command not controlled by the file-protection mask is permitted.

If an attempt is made to issue a 'set file mask' command more than once in any CCW chain, unit-check status is signaled by the integrated file adapter. A subsequent sense operation indicates command-reject and invalid sequence.

Seek Commands

Three seek commands are used in the control group of commands: 'seek', 'seek cylinder', and 'seek head'. After a 'start I/O' instruction has selected the disk storage module, a seek CCW is used to locate the desired area on the disk pack. When necessary, and depending on the seek command used, the access mechanism in the module moves the read/write head array to the specified cylinder and the designated head is selected.

The execution of a seek CCW causes a seek address to be transferred from CPU main storage to the integrated file adapter. The seek address is composed of six bytes:

Byte 0 = 0	}	Bin number (BB)
Byte 1 = 0		
Byte 2 = 0	}	Cylinder number (CC)
Byte 3 = 0 through 202*		
Byte 4 = 0		
Byte 5 = 0 through 19	}	Head number (HH)

Any seek address other than those outlined is considered invalid by the integrated file adapter. Every valid seek address defines and locates only one track. When only the head-number bytes (HH) of the seek address differ, the selected track can be found without any mechanical motion of the access mechanism. Tracks with different cylinder and head numbers can be found by movement of the read/write head array.

* A cylinder byte of 255 is used for detecting an incomplete seek condition. Although any seek address with this cylinder number causes an incomplete seek condition, it is not considered an invalid address by the IFA when a 'seek cylinder' operation is being executed.

Any seek-CCW count field (bit positions 48 through 63) should specify a six-byte field. If the count is greater than six, the integrated file adapter operates on the first six bytes that are transferred and, if the seek-CCW SLI flag is zero, a wrong-length record is then signaled to the CPU (bit 41 in the CSW is set). If the count is less than six, the seek command is not executed, and the seek-check and command-reject sense bits are set; in this case, unit-check, channel-end, and device-end conditions are set in the CSW.

The six bytes sent from CPU main storage must indicate a valid cylinder and head address. If the seek address is valid, channel-end status is presented to the channel after the address is transferred. If the seek address is not valid, the seek-check and command-reject sense bits are set, and unit-check, channel-end, and device-end status are presented. If mechanical motion is required, device-end status is made available after the mechanical movement is completed. If no mechanical motion is required, device-end status is presented, together with channel-end status.

If a parity error occurs during transfer of the seek address, the command is not executed and an I/O interruption is caused. If the access mechanism is unable to complete the seek operation for any other reason, the integrated file adapter presents unit-check, channel-end, and device-end status, and the seek-check sense bit is set.

A seek command does not have to be preceded by any other command in order to be executed. However, the three seek commands allow the file-protection mask to provide restriction and also compatibility with other direct access devices. The mask affects the use of the seek commands as follows:

1. 'Seek' and 'seek cylinder' both have the same effect on the access mechanism.
2. 'Seek head' is used when the mask permits only seek operations on the cylinder at which the access mechanism is already positioned.

Seek (X'07'): All six seek-address bytes, referenced by the CCW, are used to determine the cylinder and track for the access operation. For the integrated file adapter, bytes 0, 1, 2, and 4 must be zero.

Seek Cylinder (X'0B'): Only bytes 2 through 5, referenced by the CCW, are used to determine the seek address. All six bytes, however, must constitute a valid seek address. Bytes 0, 1, 2, and 4 must be zero.

Seek Head (X'1B'): Only bytes 4 and 5, referenced by the CCW, are used to determine the seek address. All six bytes, however, must constitute a valid seek address. If the file-protection mask is set to allow only 'seek head' commands, byte 3 must correspond to the cylinder at which the access mechanism is positioned. Otherwise, the command is rejected with unit-check and command reject status.

Space Count (X'0F')

The 'space count' command provides a means of bypassing a defective area on a track in order to recover data immediately following on that track. The command can be used for the following conditions:

1. A defective home-address or record-R0 area.
2. A defective count area, other than record R0.

Condition 1 sets the unit-check and data-check bits in the count field to interrupt the program. Record R1 is then read by the chained commands: 'space count' (SLI flag set) and 'read count, key and data'.

If two successive 'space count' commands are followed by a 'read count, key and data' command, record R2 is read. If 'space count' is the first command in a chain, it searches for the index point, then counts over the home-address and record-R0 areas. The function is the same if 'no operation' is the first command and 'space count' is the second command in a chain.

A defective count area (record N) situation sets the 'data check in count field' sense bit. In this case, key and data for record N are read by the following command chain:

'Read home address' command

One of the search-ID commands (record N-1)

'Transfer in channel' command (to repeat search if unsuccessful)

'Read data' command (record N-1; skip and SLI flag bits on)

'Space count' command (over record N count area)

'Read key and data' command (record N).

The space-count CCW must contain both a count of three bytes and the address in CPU main storage where the record-N key length and data length are located.

If the index point occurs before an address mark is found, the no-record-found bit is set. If the index point occurs while spacing over the eleven bytes, the track-overrun bit is set. The three bytes of data are used by the integrated file adapter for key length (the first byte) and data length (remaining two bytes) if the 'space count' command is followed by a 'read key and data' or 'read data' command.

When the 'space count' command is chained from a read or search command or from another 'space count' command, it searches for the next address mark. It then spaces over the count area of that record, reading the values of key length and data length from CPU main storage. If the last command in the previous chain is 'read count, key and data' (instead of 'read key and data'), record N+1 is read normally and record N is ignored. The key length and data length in the space-count CCW are ignored when the next command in the chain reads the count area.

The 'space count' command is rejected, with invalid-sequence and command-reject bits set, if it is chained from a write command. The 'space count' command also sets the file-protection mask so that a following write command in the same chain is rejected.

Sense I/O Command (X'04')

The 'sense I/O' command should be sent to the integrated file adapter whenever unit-check status is detected, even if the sense information is not to be used. The integrated file adapter sends from one to six sense bytes as specified by the count (bits 48 through 63) in the command. The sense bytes are placed in CPU main storage, starting at a data address specified in the command; that is, sense byte 0 is placed in the first address byte specified, sense byte 1 in the next-highest sequential byte, and so on.

Sense Bytes

Unit-check status (bit 6 of the status byte) indicates that the I/O device has detected either a programming error (such as an invalid command sequence), an equipment malfunction, or a condition that requires operator or program intervention. The conditions that cause the unit check are indicated as sense information – six sense bytes, numbered 0 through 5, being provided. The data-address portion of the 'sense I/O' command specifies the address in CPU main storage into which the sense bytes are to be placed. When a sense command is sent to the integrated file adapter, the sense bytes that are returned apply to the module for which the unit check occurred.

Only sense bytes 0, 1, and 5 have significance to the programmer. Byte 4 is used to allow the system program to identify which module is assigned a given address. Byte 5 is always zero, except when an overflow-incomplete condition occurs (sense byte 1, bit 7). Any information in sense bytes 0, 1, 2, and 5 is reset to all zeros whenever an initial status byte of zero is given in response to a 'test I/O' instruction or to a command other than 'sense I/O' or 'no operation'. Also, whenever another unit check is generated, any outstanding sense information is reset and replaced by the new sense information.

It is important to issue a 'sense I/O' command after every unit-check indication, even if the sense information is of no interest. With the exception of three bits that are never set (bit 2 of sense byte 0 and bits 2 and 4 of sense byte 2), the conditions that set the sense bits are stated in *IBM System/360 Component Descriptions – 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control*, GA26-3599.

Read Commands

The execution of a read command (see Figure 17) causes information to be transferred from the disk storage module to CPU main storage. In all read operations, the integrated file adapter checks (with check bytes) the validity of each area of a record as the record is read from a track. A parity bit is added to each byte as it is sent to the CPU.

If a data check is detected, the command is terminated at the end of the field in which the error occurs, the appropriate sense bits ('data check in count field' and/or

'data check') are set, and unit check, channel end, and device end are set in the CSW. A data check is not set for the key field in a 'read data' command or for the HA field in a 'read record RO' command. If an overrun is detected, the operation is terminated, and unit check, channel end, and device end are set in the CSW.

A read command does not need to be preceded by any other CCW in order to be executed, although read commands are normally chained from search commands. The 'read IPL' command, however, cannot be preceded by a 'set file mask' command in the same chain.

Write Commands

A write command (see Figure 17) is used to transfer information from CPU main storage to a specified access mechanism. The command is normally command-chained from a successful search to ensure that the area to be written is the correct one. If a write command is not chained from a successful search command, an invalid-sequence condition is set in the CSW, and the write operation is not initiated.

The write CCW specifies both the CPU main-storage location of the information to be transferred and the number of bytes to be transferred. This command transfers the specified number of bytes and writes them into the addressed disk storage. When the transfer is complete, the integrated file adapter generates two cyclic-check bytes and two bit-count-appendage bytes, appends them to the information that has just been transferred, and signals channel end and device end.

If a new data area is shorter than the data area that was written when the track was formatted, the integrated file adapter writes valid zeros in the remainder of the data area. A data check, in record areas that must be passed over but not written, terminates *any* write command before the data is written.

To verify that data was written correctly and can be retrieved correctly, a read operation is recommended after each write operation while the original data is still available in CPU main storage. The programmer should provide a satisfactory means for recovering from a data error if the read operation is not used after writing.

Formatting-Write Commands

A formatting-write command is used to initialize tracks and records and to establish the lengths of the areas within each record. If a command other than formatting-write is command-chained from a formatting-write command, the integrated file adapter retains the command and executes it after the track has been erased and the index mark has been detected. Detection of a parity check or an overrun condition during a formatting-write operation causes a unit check to be signaled to the CPU at the end of the operation. The integrated file adapter writes valid zeros from the time the overrun condition is detected until the end of the record.

Search Commands

The search commands (see Figure 17) locate and identify information or areas that have been previously written on a disk. During a search operation, the CPU operates in a write mode, sending information from CPU main storage to the integrated file adapter, while the integrated file adapter operates in a read mode, accepting information from the addressed disk storage; the IFA compares the information coming from the module with the information coming from CPU storage. The IFA remains busy during the execution of any search command.

If the search condition is satisfied, a status-modifier indication is sent, and the next CCW in the command chain is read from a position that is 16 positions higher than the current (search) CCW. This action allows a command chain to be modified as a function of the data that is recorded in disk storage.

On all search commands, command code bit 0 determines whether the operation is to be a multiple track operation; that is, whether switching to the next read/write head in the cylinder is to occur when the index mark is detected. If bit 0 is not set (0), head switching does not take place; if bit 0 is set (1), head switching does take place. If head switching has occurred, the next track is used if the search command is repeated. This action allows for sequential searching of an entire cylinder by repeating the search command once for each record to be searched.

The following command chain illustrates the procedures for reading a record that is identified by a key stored at location "A" in the CPU:

Command Chain	Function
Search key "A"	Compare key "A" (from the CPU) with the search key area that is read from the disk (search argument)
TIC* -8 Read data	Transfer back to search Read the data area of the record if status modifier was returned from the search (indicating that the search was satisfied)

The following search commands have the same functions and definitions as the corresponding commands for the 2314 Direct Access Storage Facility - A Series, described in *IBM System/360 Component Description - 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control*, GA26-3599:

- Search equal ID
- Search high ID
- Search equal or high ID
- Search equal key
- Search high key
- Search equal or high key
- Search equal HA

- Search equal key and data
- Search high key and data
- Search high or equal key and data.

File Scan With Record Overflow

In addition to the search commands listed previously, the integrated file adapter facilities provide six search commands that are associated with the file-scan and record-overflow functions when these functions are used together. The functions are available as features of the IFA.

The six search commands (effectively 12 commands because a multitrack bit may be used in the commands) assist in continuing a search-key-data command that has been interrupted during an overflow record. The commands are of the search-data type operating as 'read data' commands, except that data is searched rather than read (the masking function of the search-key-data command is included); they continue an interrupted search-key-data operation through the use of sense byte 5. The commands (see Figure 17) are as follows, file-scan functions associated with them being in parentheses:

Code	Command
X'25'	Search equal (continue scan equal)
X'45'	Search high (continue scan high)
X'65'	Search high or equal (continue scan high or equal)
X'35'	Set status modifier, regardless of compare (continue scan, set compare)
X'55'	Do not set status modifier, regardless of compare (continue scan, no compare)
X'75'	Set status modifier, regardless of compare (continue scan, set compare)

Addressing

The integrated file adapter can control up to five disk storage modules. The 16 address bits that are developed from the I/O instruction identify the IFA and the module for the operation. The program treats the IFA as if it were on selector channel 1 with an attached control unit and disk drives. The 16 bits of the I/O address are assigned as follows:

For IFA: Channel number (bits 16 through 23), 01 (hex) = selector channel 1.

For disk storage unit: Control unit number (bits 24 through 27), 0-3 (hex). Bit 28 is set to 0 for system compatibility.

For module: Device number (bits 29 through 32), 0-4 (hex); depends on number of module being addressed.

Hence the IFA has an address, for I/O instructions, of 013X where X can have a value of 0 through 4 (hex).

One module identifier plug is furnished for each disk storage module attached. By plugging where desired, the

user can assign any existing module number address to any disk storage module. Use of a nonexistent address in programming causes intervention-required status to be presented.

Address Associated with Pending Status

All status conditions (except control unit end) in the integrated file adapter are associated with the address of a specific disk storage module. When the module is in the contingent-connection state, however, control unit end is associated with a specific address, and that address is the last address presented by the IFA.

Status Information

The status conditions of the integrated file adapter and the definition of the status byte (CSW) are generally the same as those described for the 2314-A Series units in *IBM System/360 Component Descriptions – 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control*, GA26-3599.

Initial Status Conditions

Condition code 1 is set for any of the following conditions on a 'start I/O' or 'test I/O' instruction. If more than one condition exists, the first-stated condition determines the initial status byte that is to be stored in the CSW.

1. The integrated file adapter is busy. In this case, a status byte indicating control-unit-busy is stored in the CSW. The IFA is busy if:
 - a. Chaining is terminated and writing or erasing is still in progress in the disk.
 - b. A halt I/O operation is still in progress.
2. A status condition is pending in the integrated file adapter and is not specifically associated with the device. In this case, the pending status is presented and the busy bit is included in the status byte if the instruction was other than 'test I/O'.
3. The device is busy (unavailable). In this case, the busy bit alone is set in the status byte. The busy bit is not set,

however, when busy, pending status, appears with other status bits. When busy occurs with bits other than status modifier, the device is considered to be busy because of the included outstanding status. The status is cleared and the device must be re-addressed to determine if it is available.

4. Status is pending in the device. In this case, the pending status is presented and the busy bit is included if the instruction was other than 'test I/O'.
5. A unit-check condition exists at the device (for example, seek-check or intervention required). In this case, unit check is indicated except for the following conditions:
 - a. A valid sense command (0100) is accepted so that the command may be executed to permit sensing of the sense indicators.
 - b. A module seek check. A 'recalibrate' command is accepted so that the command may be executed.
6. The command is rejected. In this case, unit check occurs.

Pending Status Conditions

A pending-status condition may exist in either the integrated file adapter or the disk storage module.

Status Pending in IFA: Status is pending if control unit busy was presented and a control unit end has not been accepted.

Status Pending in Disk Storage Module: The only status that can be pending is device end. When unit check occurs with device end (and not channel end), it is not generated until the device-end status is presented. The device-end and unit-check conditions then become pending in the integrated file adapter if they are not accepted. Status is pending if the following conditions exist:

1. Channel-end alone is set for the operation. Device-end status is pending.
2. The device has changed from the not-operational state to the ready state. Device-end status is pending.

ABBREVIATIONS

ALU	Arithmetic and logic unit
ASCII	American National Standard Code for Information Interchange
ASCP	Automatic system checkout program
CAW	Channel address word
CCITT	International Telephone and Telegraph Consultative Committee
CCW	Channel command word
CPU	Central processing unit
CSW	Channel status word
Dec	Decimal
DOS	Disk operating system
EBCDIC	Extended binary-coded-decimal interchange code
ECC	Error checking and correction
EIA	Electronic Industries Association
HA	Home address
Hex	Hexadecimal
ICA	Integrated communications adapter
ID	Identifier, identity
IFA	Integrated file adapter

I-Fetch	Instruction fetch
IMPL	Initial microprogram load
I/O	Input/output
IPL	Initial program load
MCIC	Machine-check interruption code
MFT	Multiprogramming with a fixed number of tasks
MST	Monolithic system technology
ns	Nanosecond
NTTTC	Nippon Telephone and Telegraph Public Corporation
Op	Operation
OS	Operating system
PCI	Program-controlled interruption
PSW	Program status word
SLI	Suppress length indication
TIC	Transfer in channel
UCW	Unit control word
X' . . '	Hexadecimal representation; for example X'02' means 02 (hexadecimal)
μs	Microsecond

GLOSSARY

Address Folding: A method of interpreting device addresses so that, with a limited number of subchannels, a maximum number of actual device addresses is available.

Control Station: The station (usually a CPU) in a multipoint data communications system that controls network traffic by means of polling and selection. On a centralized multipoint network, tributary stations can communicate *only* with the control station, when polled or selected by the control station.

Cycle-Steal Operation: A means of transferring data from a channel to main storage without microprogram intervention. The operation is totally hardware-controlled, "stealing" time from whatever (lower priority) microprogram operation is in progress (in CPU or other channel), without the microprogram being aware of this stealing.

Data Set: 1. In data processing, the major unit of data storage and retrieval in the operating system. It consists of a collection of data in one of several prescribed arrangements, and is described by control information to which the system has access.

2. In data communication (teleprocessing), a device that performs the modulation/demodulation and control functions necessary to provide compatibility between business machines and communications facilities.

Disk Module: A disk-storage device that includes the specified

number of storage-media disks for the particular model, the read/write access mechanism for each surface of the disks, and the power drive for each mechanism.

Hexadecimal: A number system that uses the equivalent of decimal number 16 as a base.

Microinstruction: An element of *machine* control data (16 bits in the System/370 Model 135) that is provided within the design as a definition of the operation to be performed by the machine in one machine cycle. Each System/370 instruction, each channel routine, and so on, is built from appropriate sequences of microinstructions.

Microprogram: A program of microinstructions. Also termed a *microroutine*.

Modem: Contraction of *modulator/demodulator*. A device that converts digital dc signals into frequency encoded signals to allow transmission over telephone lines. It also reconverts frequency encoded signals received from a remote station into digital dc signals. In some countries, the term is applied to devices that have the functions of a data set and is considered synonymous with *data set*.

Monolithic Storage: Storage that is comprised of monolithic transistor circuits. A monolithic circuit is an electronic circuit, all of whose components (transistors, resistors, and so on) are formed by chemical processes in a single piece of silicon, termed a *chip*. The circuit density can be high; in the Model 135, for example, 128

storage bits are provided on a single chip measuring about 1/8 in. x 1/8 in. (3 mm x 3 mm).

Multipoint Network: A line or circuit that interconnects several stations in a data communications system.

Plug-In Byte: A byte of address data that is incorporated in the hardware of a block multiplexer channel. The byte contains 2 four-bit addresses corresponding to the two control units to be multiplexed; when only one control unit is used, both half-bytes contain the same address. The address byte is incorporated in the channel circuits at installation by means of a plug-in MST card. The card contains an eight-bit external register and eight lines (jumpers), which tie the individual bits, up or down, as required by the two address codes.

Storage Cycle: The time interval that is needed for access, either input or output, of a word in main storage.

Tributary Station: In a centralized multipoint data communications system, a station, other than the control station, that can communicate only with the control station when polled or selected by the control station.

Appendix B. Instruction Timings

The following tables contain the average timings, or formulas for calculating these timings, for instructions associated with CPU and input/output operations. All timings for instructions that include reference to main storage include also the time required for base-register addition in the address formation.

The instruction timings are dependent on the following factors: storage-unit timing capabilities, circuit timings, and optimum use of logic. Changes to any of these factors can result in a change to the timings listed in the tables.

Interference that is attributable to operations of channels or the integrated file adapter is not included in the timings.

Indexing Time

In the tables, it is assumed that the RX-format instructions specify register zero as the index register. With non-zero indexing, 0.715 microseconds should be added for halfword operations and for branching operations other than branch-on-condition (BC), and 0.440 microseconds should be added for all other RX instructions. When the branch-on-condition (BC) operation is indexed, its execution time is 3.630 microseconds.

Data Alignment

In the tables, it is assumed that the halfword, fullword, and doubleword operands of RX-format instructions are located in storage on integral halfword or fullword boundaries. If the operands are not on boundaries, the quoted times should be increased as follows:

Fetch a halfword that is on an odd-byte boundary (for example, AH): 2.915 μ s

Store a halfword on an odd-byte boundary (for example, STH): 3.685 μ s

Fetch a fullword that is not on a fullword boundary: 4.565 μ s

Store a fullword on a halfword boundary but not a fullword boundary: 5.555 μ s

Store a fullword on an odd-byte boundary: 6.105 μ s

Fetch a doubleword that is not on a fullword boundary: 12.375 μ s

Store a doubleword on a halfword boundary but not on a fullword boundary: 11.660 μ s

Store a doubleword on an odd-byte boundary: 12.760 μ s

The off-boundaries timing (in microseconds) for the following load and store operations is:

Load multiple (LM): 3.506 + 6.490GR

Store multiple (STM): 3.506 + 7.755GR

Load control (LCTL): 23.606 + 7.865CR

Store control (STCTL): 6.902 + 10.890CR

Instruction Alignment

The exact time of an instruction with a format longer than one halfword (that is, not RR) varies slightly according to its alignment in storage. If the first two halfwords of the instruction lie completely within an ECC word, the execution time is 0.041 microseconds faster than the time quoted in the tables; if they lie in different ECC words, the execution time is 0.124 microseconds slower. Thus the times quoted are averages which assume that each possible alignment of an instruction within an ECC word is equally likely and that the ECC word is eight bytes.

For the decimal instructions, the length of the first operand field (N^1) is assumed to be greater than, or equal to, the length of the second operand field (N^2).

Parameters for Instruction Timing Formulas

Symbol	Definition
B	Total number of bytes of the first operand that are processed.
CR	Number of control registers loaded or stored.
D	Number of digits shifted.
DODD	1 if D is odd; 0 otherwise.
DSC	Number of digit select characters in the pattern field.
E	Time for the subject instruction that is executed by the 'execute' instruction.
ERS	1 if the subject instruction has RS format; 0 otherwise.
ERX	1 if the subject instruction has RX format; 0 otherwise.
ESS	1 if the subject instruction has SS format; 0 otherwise.
F ¹	1 if the branch operation is successful; 0 otherwise.
GR	Number of general registers loaded or stored.
G ⁴	1 if the condition code is zero, that is, all of the selected bits are zero or the mask is all zero; 0 otherwise.
HWB	1 if one operand address is even and the other is odd; 0 if the addresses are both even or both odd.
HWO	1 if the fields overlap in such a way that the first operand address is equal to the second operand address + 1; 0 otherwise.
I/F	Channel interface response time.
MK	Number of times the mark address is stored in the 'edit and mark' instruction.
N	Total number of bytes in the first operand.
NBC	Absolute value of $(NM + NP)/128$, which is the total number of bytes compared, divided by 128. Any remainder is ignored.
NBM	Absolute value of $(NM + NP)/256$, which is the total number of bytes moved, divided by 256. Any remainder is ignored.
NM	Number of bytes (not pad characters) moved or compared.
NODD	1 if N is odd; 0 otherwise.
NP	Number of pad characters moved or compared.
N ¹	Total number of bytes in the first operand (destination).
N ²	Total number of bytes in the second operand (source).
SB ³² , SB ¹⁶ , SB ⁸ , SB ⁴ , SB ² , SB ¹	These are the bits in binary value of the amount to be shifted. For example, if the number of positions to be shifted is five, then SB ⁴ and SB ¹ are one and the other parameters are zero.
SSC	Number of significant start characters in the pattern field.
TPX	1 if NM, NP are both non-zero; 0 otherwise.
T ¹	1 if the result field is recomplemented (that is, it changes sign); 0 otherwise.
T ³	1 if N ² is less than $(N^1 + 1)/2$; 0 otherwise.
T ⁶	1 if N ² is less than or equal to 4; 0 otherwise.
T ⁹	0 if any non-zero function byte is found; 1 otherwise.
T ¹¹	1 if N ¹ is greater than $(N^2 + 1)/2$; 0 otherwise.
T ¹³	0 if N ² is equal to or greater than N ¹ ; 1 otherwise.

Instruction	Format	Op Code	Mnemonic	Time (Microseconds)
Add	RR	1A	AR	2.558
Add*	RX	5A	A	4.208
Add decimal	SS	F5	AP	$17.079 + 4.070N^1 + 3.878N^2 + T^1(2.200 + 4.235N^1)$
Add halfword*	RX	4A	AH	5.006
Add logical	RR	1E	ALR	2.558
Add logical*	RX	5E	AL	4.208
Add normalized (extended)	RR	36	AXR	28.354#
Add normalized (long)	RR	2A	ADR	16.132#
Add normalized (long)*	RX	6A	AD	17.727#
Add normalized (short)	RR	3A	AER	13.614#
Add normalized (short)*	RX	7A	AE	13.725#
Add unnormalized (long)	RR	2A	AWR	15.103#
Add unnormalized (long)*	RX	6E	AW	16.698#
Add unnormalized (short)	RR	3E	AUR	12.984#
Add unnormalized (short)*	RX	7E	AU	13.095#
AND	RR	14	NR	2.145
AND*	RX	54	N	3.795
AND	SI	94	NI	4.648
AND	SS	D4	NC	$10.368 + 2.531N$
Branch and link	RR	05	BALR	4.950
Branch and link*	RX	45	BAL	4.620
Branch on condition	RR	07	BCR	2.365
Branch on condition*	RX	47	BC	1.375
Branch on count	RR	06	BCTR	$3.410 + 0.275F^1$
Branch on count*	RX	46	BCT	$3.080 + 0.275F^1$
Branch on index high	RS	86	BXH	$5.390 - 0.440F^1$
Branch on index low or equal	RS	87	BXLE	$5.390 - 0.440F^1$
Compare	RR	19	CR	2.255
Compare*	RX	59	C	3.905
Compare decimal	SS	F9	CP	$16.940 + 4.070N^1 + 2.805N^2$
Compare halfword*	RX	49	CH	4.703
Compare logical	RR	15	CLR	1.980
Compare logical*	RX	55	CL	3.630
Compare logical	SI	95	CLI	3.300
Compare logical	SS	D5	CLC	$6.505 + 1.596B$
Compare logical character under mask	RS	BD	CLCM	$4.510 + 1.288N$
Compare logical (long)	RR	0F	CLCL	$33.655 + 2.475NM + 1.650NP + 10.600(NBC + TPX)$
Compare (long)	RR	29	CDR	14.883#
Compare (long)*	RX	69	CD	16.478#
Compare (short)	RR	39	CER	13.094#
Compare (short)*	RX	79	CE	13.205#
Convert to binary*	RX	4F	CVB	25.369 (minimum); 70.304 (maximum)
Convert to decimal*	RX	4E	CVD	12.554 (minimum); 171.009 (maximum)

* Indicates that the instruction has a double indexing capability

Indicates that the timing has been weighted to provide realistic estimates for actual values that could be expected in typical applications

Instruction	Format	Op Code	Mnemonic	Time (Microseconds)
Diagnose	SI	83	—	Varies, depending upon function
Divide	RR	1D	DR	40.267
Divide*	RX	5D	D	41.917
Divide decimal	SS	FD	DP	$43.024 + 3.658N^1 + 2.008T^6 + (64.213 + 36.052T^6)(N^1 - N^2)$
Divide (long)	RR	20	DDR	77.990#
Divide (long)*	RX	6D	DD	79.214#
Divide (short)	RR	3D	DER	49.285#
Divide (short)*	RX	7D	DE	49.391#
Edit	SS	DE	ED	$6.710 + 5.473N + 2.971DSC + 3.796SSC$
Edit and mark	SS	DF	EDMK	$6.710 + 5.473N + 2.971DSC + 3.796SSC + 2.090MK$
Exclusive OR	RR	17	XR	2.420
Exclusive OR*	RX	57	X	4.070
Exclusive OR	SI	97	XI	4.923
Exclusive OR	SS	D7	XC	$10.505 + 2.668N$
Execute*	RX	44	EX	$5.789 + 3.369ERX + 1.746ERS + 3.919ESS + E$
Halt I/O	SI	9E	HIO	$55.839 + I/F$
Halve (long)	RR	24	HDR	14.108
Halve (short)	RR	34	HER	14.163
Insert character*	RX	43	IC	3.025
Insert characters under mask	RS	BF	ICM	$4.510 + 1.075N$
Insert storage key	RR	09	ISK	6.077
Load	RR	18	LR	1.430
Load*	RX	58	L	3.080
Load address*	RX	41	LA	2.090
Load and test	RR	12	LTR	1.843
Load and test (long)	RR	22	LTDR	5.555
Load and test (short)	RR	32	LTER	4.620
Load complement	RR	13	LCR	2.553
Load complement (long)	RR	23	LCDR	5.830
Load complement (short)	RR	33	LCER	4.895
Load control	RS	87	LCTL	$23.675 + 4.332CR$
Load halfword*	RX	48	LH	3.603
Load (long)	RR	28	LDR	5.005
Load (long)*	RX	68	LD	6.600
Load multiple	RS	98	LM	$3.575 + 1.980GR$
Load negative	RR	11	LNR	2.200

* Indicates that the instruction has a double indexing capability

Indicates that the timing has been weighted to provide realistic estimates for actual values that could be expected in typical applications

Instruction	Format	Op Code	Mnemonic	Time (Microseconds)
Load negative (long)	RR	21	LNDR	5.555
Load negative (short)	RR	31	LNER	4.620
Load positive	RR	10	LPR	2.475
Load positive (long)	RR	20	LPDR	5.555
Load positive (short)	RR	30	LPER	4.620
Load PSW	SI	82	LPSW	22.279
Load rounded (extended operand, long result)	RR	25	LRDR	8.993
Load rounded (long operand, short result)	RR	35	LRER	7.480
Load (short)	RR	38	LER	4.070
Load (short)*	RX	78	LE	4.180
Move	SI	92	MVI	2.998
Move	SS	D2	MVC	$5.665 + (1.018 + 0.418HWB + 0.880HWO)N + 0.770NODD$
Move (long)	RR	0E	MVCL	$34.355 + (1.018 + 0.418HWB)NM + 0.605NP + 9.010(NBM + TPX)$
Move numerics	SS	D1	MVN	$10.093 + 2.531N$
Move with offset	SS	F1	MVO	$9.515 + 4.510N^1 - 1.870T^{13} (N^1 - N^2)$
Move zones	SS	D3	MVZ	$10.093 + 2.618N$
Multiply	RR	1C	MR	23.870
Multiply*	RX	5C	M	25.520
Multiply decimal	SS	FC	MP	$38.424 + 3.795N^1 + 0.825N^2 + 6.215T^6 + (30.558 + 11.550T^6) (N^1 - N^2)$
Multiply (extended)	RR	26	MXR	168.300#
Multiply halfword*	RX	4C	MH	17.188
Multiply (long)	RR	2C	MDR	49.452#
Multiply (long)*	RX	6C	MD	51.322#
Multiply (long operand, extended result)	RR	27	MXDR	70.524#
Multiply (long operand, extended result)*	RX	67	MXD	72.064#
Multiply (short)	RR	3C	MER	32.127#
Multiply (short)*	RX	7C	ME	32.237#
OR	RR	16	OR	2.420
OR*	RX	56	O	4.070
OR	SI	96	OI	4.648
OR	SS	D6	OC	$10.368 + 2.531N$
Pack	SS	F2	PACK	$7.013 + 5.748N^1 - 1.595T^{11} (2N^1 - N^2 - 1)$
Read direct	SI	85	RDD	5.802 + time for hold-in to drop

* Indicates that the instruction has a double indexing capability

Indicates that the timing has been weighted to provide realistic estimates for actual values that could be expected in typical applications

Instruction	Format	Op Code	Mnemonic	Time (Microseconds)
Set clock	RS	B204	SCK	13.035
Set program mask	RR	04	SPM	4.730
Set storage key	RR	08	SSK	5.583
Set system mask	SI	80	SSM	11.424
Shift and round decimal	SS	F0	SRP	<i>Left shift:</i> 24.063 + 4.098N + 0.206D + (0.798 + 1.595N - 0.798D)DODD <i>Right shift:</i> 24.063 + 6.436N - 0.963D + (0.660 + 1.320N - 0.660D)DODD
Shift left double	RS	8F	SLDA	7.343 + 7.480SB ³² + 3.740SB ¹⁶ + 11.440SB ⁸ + 5.720SB ⁴ + 2.860SB ² + 2.585SB ¹
Shift left double logical	RS	8D	SLDL	6.655 + 4.730SB ³² + 2.365SB ¹⁶ + 8.140SB ⁸ + 4.070SB ⁴ + 2.035SB ² + 2.723SB ¹
Shift left single	RS	8B	SLA	6.408 + 6.380SB ³² + 3.190SB ¹⁶ + 10.120SB ⁸ + 5.060SB ⁴ + 2.530SB ² + 2.255SB ¹
Shift left single logical	RS	89	SLL	5.720 + 3.630SB ³² + 1.815SB ¹⁶ + 6.820SB ⁸ + 3.410SB ⁴ + 1.705SB ² + 2.393SB ¹
Shift right double	RS	8E	SRDA	7.343 + 5.005SB ³² + 2.503SB ¹⁶ + 4.070SB ⁸ + 2.035SB ⁴ + 4.895SB ² + 7.205SB ¹ - 7.755(SB ²)(SB ¹)
Shift right double logical	RS	8C	SRDL	6.665 + 5.005SB ³² + 2.503SB ¹⁶ + 4.896SB ⁸ + 2.448SB ⁴ + 4.758SB ² + 6.931SB ¹ - 6.793(SB ²)(SB ¹)
Shift right single	RS	8A	SRA	6.408 + 3.905SB ³² + 1.953SB ¹⁶ + 3.410SB ⁸ + 1.705SB ⁴ + 4.510SB ² + 6.215SB ¹ - 7.040(SB ²)(SB ¹)
Shift right single logical	RS	88	SRL	5.720 + 3.905SB ³² + 1.953SB ¹⁶ + 4.236SB ⁸ + 2.118SB ⁴ + 4.098SB ² + 5.941SB ¹ - 5.803(SB ²)(SB ¹)
Start I/O	SI	9C	SIO	91.789 + I/F
Start I/O fast release	SI	9C	SIOF	Executed as start I/O
Store*	RX	50	ST	3.300
Store channel ID	SI	B203	STIDC	8.470 (minimum); 11.275 (maximum)
Store character*	RX	42	STC	3.135
Store character under mask	RS	BE	STCM	3.465 + 1.732N
Store clock	SI	B205	STCK	15.159
Store control	RS	B6	STCTL	6.971 + 5.230CR
Store CPU ID	SI	B202	STIDP	11.000
Store halfword*	RX	40	STH	2.585
Store (long)*	RX	60	STD	5.500
Store multiple	RS	90	STM	3.575 + 1.925GR
Store (short)*	RX	70	STE	3.575
Subtract	RR	1B	SR	3.713
Subtract*	RX	5B	S	5.363
Subtract decimal	SS	FB	SP	17.079 + 4.070N ¹ + 3.878N ² + T ¹ (2.200 + 4.235N ¹)
Subtract halfword*	RX	4B	SH	6.161
Subtract logical	RR	1F	SLR	3.713
Subtract logical*	RX	5F	SL	5.363
Subtract normalized (extended)	RR	37	SXR	29.179#
Subtract normalized (long)	RR	2B	SDR	16.682#
Subtract normalized (long)*	RX	6B	SD	18.277#
Subtract normalized (short)	RR	3B	SER	14.164#

* Indicates that the instruction has a double indexing capability

Indicates that the timing has been weighted to provide realistic estimates for actual values that could be expected in typical applications

Instruction	Format	Op Code	Mnemonic	Time (Microseconds)
Subtract normalized (short)*	RX	7B	SE	14.275#
Subtract unnormalized (long)	RR	2F	SWR	15.653#
Subtract unnormalized (long)*	RX	6F	SW	17.248#
Subtract unnormalized (short)	RR	3F	SUR	13.534#
Subtract unnormalized (short)*	RX	7F	SU	13.645#
Supervisor call	RR	0A	SVC	34.765
Test and set	SI	93	TS	4.373
Test channel	SI	9F	TCH	11.179
Test I/O	SI	9D	TIO	55.169 + I/F
Test under mask	SI	91	TM	3.850 – 0.550G ⁴
Translate	SS	DC	TR	4.730 + 4.428N
Translate and test	SS	DD	TRT	7.095 + 4.180B – 2.365T ⁹
Unpack	SS	F3	UNPK	9.818 + 3.136N ¹ – 0.152T ³ (N ¹ – 2N ² + 1)
Write direct	SI	84	WRD	4.730
Zero and add	SS	F8	ZAP	13.723 + 2.310N ¹ + 2.063N ²

* Indicates that the instruction has a double indexing capability

Indicates that the timing has been weighted to provide realistic estimates for actual values that could be expected in typical applications

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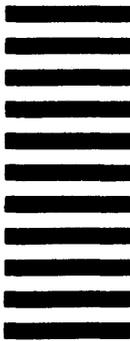
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