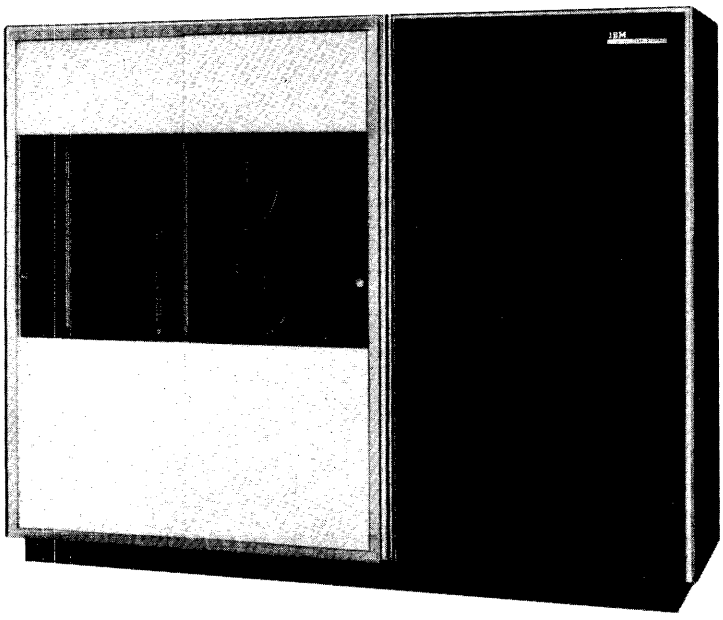
7090 DATA PROCESSING SYSTEM BULLETIN

IBM 1301 DISK STORAGE

THE IBM 1301 Disk Storage, IBM 7631 File Control (Figure 1), and IBM 7909 I Data Channel are available as an optional feature on all IBM 7090 Data Processing Systems. Capacity is more than 56 million characters of storage for each disk storage unit attached to the 7090 system. Up to five storage units may be attached to one or two file control units.

Some of the operating characteristics of the IBM 1301 Disk Storage are:

Function	Result
Positioning of Access Mechanism	50-180 Milliseconds
Average Rotational Delay	17 Milliseconds
Characters for One Access Positioning	111,600 Maximum
Instantaneous Character Rate	90,000 per Second
Characters per Track	2,790 Maximum
Characters per Storage Unit	55,800,000 Maximum



IBM 1301 Disk Storage

As many as five disk storage units may be attached to a 7090 system as shown in Figure 2. Other arrangements may be made by using two file control units and two 7909 I data channels. For example, three disk storage units may be attached to one file control (and one 7909 data channel), while one or two disk storage units are attached to another file control and its 7909 data channel. The 7909 channel attaches in the same manner as the 7607 channel. Normal data channel addresses are used and, therefore, no more than eight data channels (7607 and 7909) may be used with any one 7090 system.

ADVANTAGES OF DISK STORAGE

The large amount of storage capacity available with this feature increases system operational efficiency in many areas. One of these areas is program storage. A disk storage unit may be used as the "program tape" in a 7090 installation to give:

1. Access to all programs: With such capacity, all of the programs for a total installation could be placed on the disk and be available to the computer in milliseconds instead of minutes.
2. Simplified scheduling: Schedules do not have to rely upon the operator to have the proper program tape on the proper tape unit.
3. Improved program test: Programs in test status can be stored on the disk. This eliminates the need for manipulation of large numbers of cards before each test run. If only certain sections of the programs need to be used, they are readily available.
4. Program compiling aid: Compilers may work without the need to search tape for appropriate routines as requested by each program parameter. Compilers may remain on-line for use by the "compile and go" methods of operation.

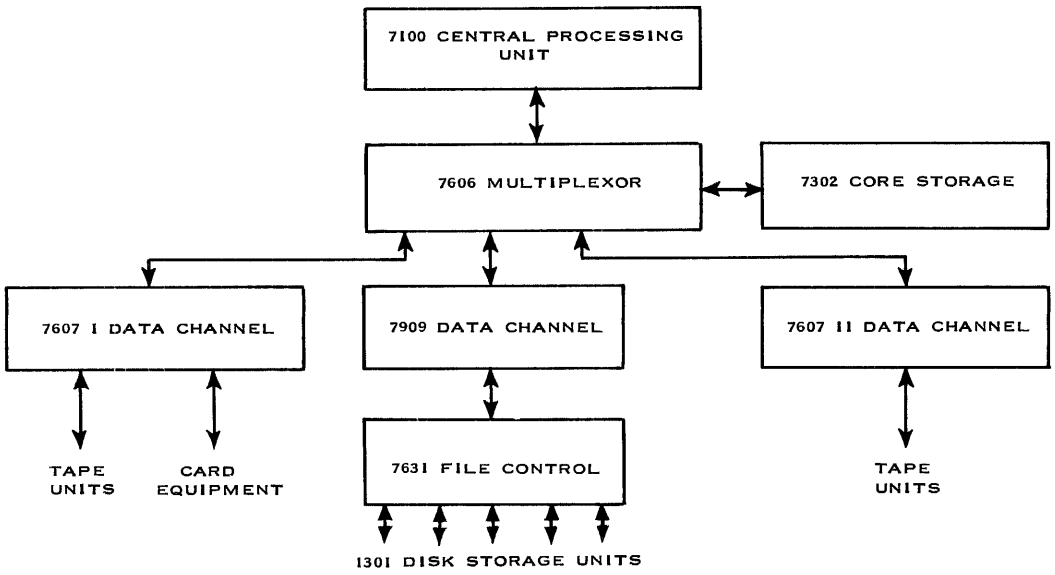


Figure 2. IBM 7090 System with IBM 1301 Disk Storage

It is recommended that storage "back up" (such as magnetic tape or other media) be used when necessary to insure system operation when the disk storage is off-line for preventive maintenance.

IBM 7631 FILE CONTROL OPERATIONS

Operations performed by the IBM 7631 File Control, IBM 1301 Disk Storage, and IBM 7909 Data Channel result from execution of instructions, commands, and orders. These terms are defined as:

Instruction:	Data decoded and executed by the central processing unit (add, subtract, etc.).
Command:	Data decoded and executed by the data channel.
Order:	Data decoded and executed in the file control.
Status Data:	Indicator data reflecting various conditions in the disk system.

Transmission of data to and from disk storage is accomplished by data channel commands. Data are transmitted in a manner similar to that used by the 7607 channels, except that read and write operations are decoded in the 7909 channel rather than in the central processing unit. Disk control operations which do not require data transmission are accomplished by sending an order to the file control itself where it is decoded and executed. A complete description of these orders and their operation is contained in IBM 1301 Disk Storage with IBM 7631 File Control, General Information Manual, Form D22-6576.

Seek

Execution of this order causes the specified access mechanism of the addressed disk storage to locate itself in a position specified by the track address and to select the specified head. The order is sent to the file control, and, when received, signals the data channel to proceed with its own routine while disk storage executes the seek operation. An attention signal informs the computer when the operation is completed. This signal also sets a bit of status data in the file control. The status data may then be sent to the computer by execution of a sense command.

Prepare to Verify (Single Record Operation)

Execution of this order conditions the file control for single-record operation. The desired disk and access mechanism are selected, the address is specified and verified, and a subsequent read or write command sequence transmits data to or from the addressed record sector of the disk.

Prepare to Verify (Cylinder Operation) (Optional Feature)

Execution of this order permits reading or writing of data starting at the first record sector after the home address of the addressed track, and continuing through successive record locations and tracks until either the end of cylinder is reached or a stop condition occurs in the computer. (The prime function of the home address is to define the track address.)

Prepare to Verify (Track Operation)

Execution of this order, followed by a read or write command, permits reading or writing of a full track of information. It also makes use of the home address. The order instructs the file control to select the desired disk and access mechanism, supply the home address to be verified, and condition the file control to operate on a full-track basis.

Select and Condition

This order is used to select an access mechanism and disk preparatory to writing format tracks, or reading or writing the home address on data tracks. The head and track will have been selected by a previous seek order and switch setting. This order is valid only when a three-position lockable switch is set to the FT (format) or HA (home address) position.

Prepare to Write Check

Execution of this order checks either a written format or written data. In format checking, the key-lock switch must be in the FT position. In data checking, the key-lock switch must be in the normal position. This order performs a bit-for-bit comparison and signals the results of that comparison.

Set Access Inoperative

Execution of this order causes the file control to disconnect the addressed access unit circuits from the disk. (This permits disconnection of a malfunctioning access unit from the system.) Any subsequent command to this access mechanism results in an unusual-end signal.

Six Bit Mode

Execution of this order places the file control in a six-bit operational mode.

Eight Bit Mode

Execution of this order places the file control in an eight-bit operational mode, but only the six normal data bits of each eight-bit byte are used; the other two bits are discarded.

No Operation

Execution of this order results in normal no-operation status in the file control.

SYSTEM INSTRUCTIONS AND COMMANDS

INFORMATION FLOW

Data being transmitted between core storage and disk storage pass through the IBM 7631 File Control, IBM 7909 Data Channel, and the IBM 7606 Multiplexor. Operation of the data channel is initiated in the CPU. Once started, the channel operates independently of the main program being executed by the CPU. The data channel has the responsibility for controlling quantity and destination of all data transmitted between core and disk storages.

Programs for a channel operation are stored in core storage just as are instructions executed by the central processing unit. To distinguish between a main (CPU) program and a channel program, data executed by a data channel are termed commands, data executed by the CPU are termed instructions and data executed by the file control are termed orders.

DATA FLOW

A simplified flow chart, containing 7909 data channel registers and data switches concerned with data flow, is shown in Figure 3.

1. Storage Bus In and Storage Bus Out: These 36-position data switches direct data between the multiplexor and the data register of the 7909 data channel.

2. Data Register: This 36-position register serves as a buffer register for data flowing between core storage and the assembly register.

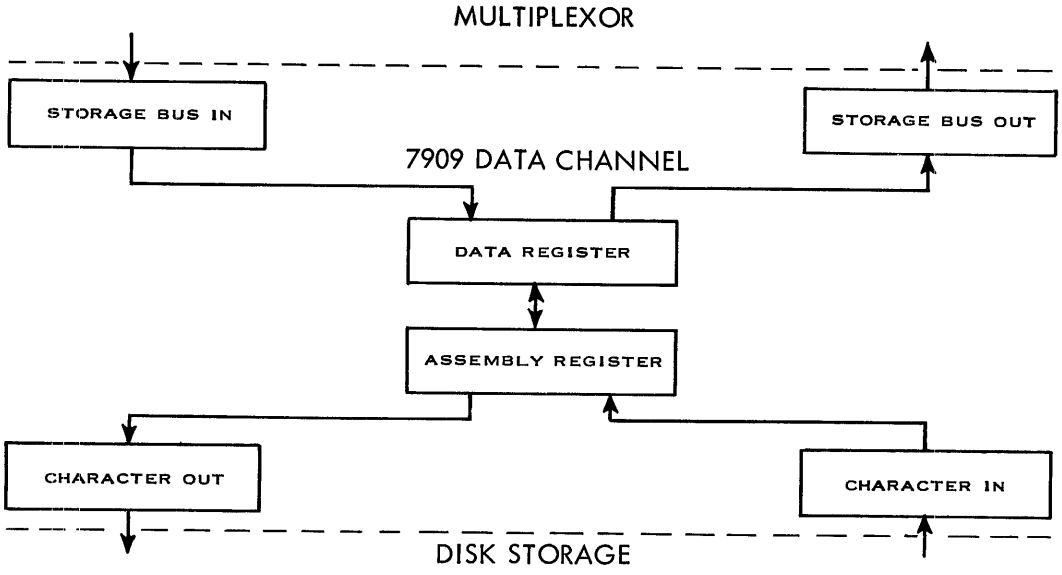


Figure 3. Data Flow within the IBM 7909 Data Channel

3. Assembly Register: The 36-position assembly register assembles characters from the character-in switch and, when six characters have been assembled, sends them (as a word) to the data register. A word from the data register is placed in the assembly register and then sent, one character at a time, to the character-out switch. Characters placed in or taken from the assembly register are automatically shifted (in the register) to take their proper sequence in the word.

4. Character Out and Character In: These six-position data switches direct data (by character) to or from disk storage.

OPERATION AND CONTROL INFORMATION FLOW

Four additional 7909 data channel registers are used to decode and control channel operations (Figure 4). These registers are:

Operation Register and Decoder: This five-position register (positions S, 1, 2, 3, and 19) hold the operation code of the command being executed by the data channel. Decoding circuitry receives operation bits of word locations and sets up switching circuits for the execution of the command.

Address Counter: The address counter (15 positions) is used to locate data addresses in core storage. On operations under word count control, the address counter is increased by one for each word transmitted. Storage words are thus taken from or placed into sequential word locations. The counter is normally set from the address portion of the command effecting the data transfer.

Word Counter: The 15-position word counter is used to control the number of words to be transmitted. As each word is transmitted, the word counter is reduced by one. A signal is given when the contents of the word counter are reduced to zero. The word counter is normally set from the count portion of the command effecting the data transfer.

Command Counter: This 15-position counter locates and controls the sequence of commands taken from core storage.

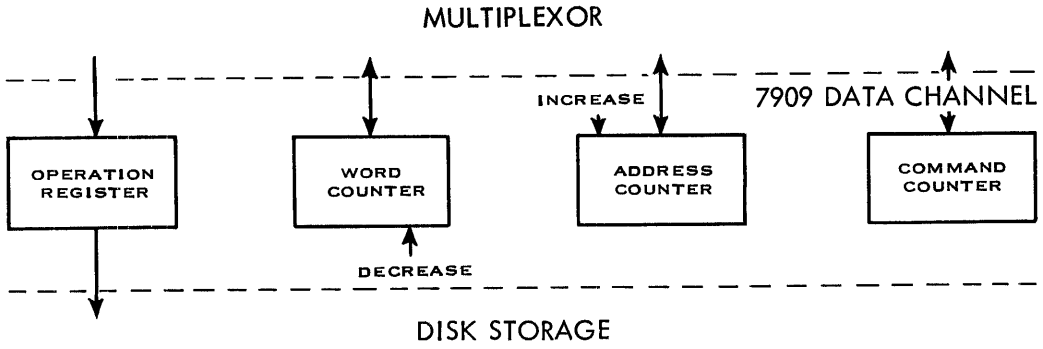


Figure 4. Operation and Control Registers of IBM 7909 Data Channel

CENTRAL PROCESSING UNIT INSTRUCTIONS

The format used in the following descriptions of instructions and commands uses the established formats contained in the IBM 7090 Data Processing System Reference Manual, Form A22-6528. Execution timing is not included since execution is dependent on organization of commands in storage and the status of the data channel when it is addressed. Symbols used are:

C = Count Field
F = Indirect Address Flag
T = Index Register Action
Y = Address Field

RSCA--Reset and Start Channel A

The channel is selected and reset, and takes its next command from address Y. The instruction is interlocked against channel activity; if the instruction is executed while the channel is busy, its execution is delayed until the channel is in wait status.

Instruction	Code	Name
RSCB	-0540	Reset and Start Channel B
RSCC	+0541	Reset and Start Channel C
RSCD	-0541	Reset and Start Channel D
RSCE	+0542	Reset and Start Channel E
RSCF	-0542	Reset and Start Channel F
RSCG	+0543	Reset and Start Channel G
RSCH	-0543	Reset and Start Channel H

STCA--Start Channel A

If the channel is not in wait status, execution of this instruction is delayed. If in wait status, the channel is started and takes its next command from the address part of the wait command.

Instruction	Code	Name
STCB	-0544	Start Channel B
STCC	+0545	Start Channel C
STCD	-0545	Start Channel D
STCE	+0546	Start Channel E
STCF	-0546	Start Channel F
STCG	+0547	Start Channel G
STCH	-0547	Start Channel H

SCHA--Store Channel

Execution of this instruction causes the specified channel to be selected and that channel's command counter contents to be placed in positions 21-35 of location Y. The channel's address counter contents are placed in positions 3-17 of location Y. Positions S, 1, 18, and 19 are reserved for diagnostics and their contents cannot be predicted.

Instruction	Code	Name
SCHB	-0640	Store Channel B
SCHC	+0641	Store Channel C
SCHD	-0641	Store Channel D
SCHE	+0642	Store Channel E
SCHF	-0642	Store Channel F
SCHG	+0643	Store Channel G
SCHH	-0643	Store Channel H

ENB--Enable from Y

When this instruction is executed, the contents of location Y determine which signals may cause a trapping operation. Execution of each enable instruction cancels the effect of previous enable instructions. The channel may be disabled (traps will not occur) by executing an enable instruction whose operand contains a zero in the proper position. Trapping signals are controlled as follows:

Signal Due to	Channel	Effective if a "1" in
Control word	A	0035
Control word	B	0034
Control word	C	0033
Control word	D	0032
Control word	E	0031
Control word	F	0030
Control word	G	0029
Control word	H	0028

Execution of a trap inhibits all further traps until a new enable instruction is executed or a restore-channel-traps instruction is executed. Depression of the reset or clear key, or execution of an RIC instruction, also disables all channels.

RICA--Reset Channel A

This instruction, when executed by the central processing unit, causes all conditions in the channel to be reset. This instruction is not interlocked against channel activity. If data transmission is taking place when a RIC occurs, validity of the data already transmitted cannot be guaranteed.

Instruction	Code	Name
RICB	0760-- 2350	Reset Channel B
RICC	0760-- 3350	Reset Channel C
RICD	0760-- 4350	Reset Channel D
RICE	0760-- 5350	Reset Channel E
RICF	0760-- 6350	Reset Channel F
RICG	0760-- 7350	Reset Channel G
RICH	0760--10350	Reset Channel H

INPUT-OUTPUT COMMANDS

CTL--Control

The control command is decoded in the channel itself. Information contained in address Y is sent to the file control, starting with the high-order character, and continues until an end signal is received from the file control. If more than one word location is necessary to transmit all of the data required by the channel, the next word is taken from location Y + 1, etc. This process continues until an end signal is received; the next command is then taken from the storage location following the control command.

CTLR--Control and Read

This command causes the channel to transmit control information in the same manner as for a control command, and prepares the channel to read. When an end signal is received from the file control (signaling the end of the order), the channel proceeds to the next command in sequence. When a copy command is encountered, the channel is placed in read status and data are transmitted to storage under control of the copy.

CTLW--Control and Write

This command causes the channel to transmit control information in the same manner as for a control command, and prepares the channel to write. When an end signal is received from the file control (signaling end of order) the channel proceeds to the next

sequential command. When a copy command is encountered, the channel is placed in write status and data are transmitted from storage to the file control under control of the copy command.

SNS--Sense

This command prepares the channel for a sense operation and then proceeds to the next sequential command. When a copy command is encountered, the channel places the file control in sense status and information is sent to storage under control of the copy command.

CPYD--Copy and Disconnect

This command, when decoded by a channel not in read or write status, causes a sequence check and thus a channel interrupt. If the channel is in read or write status, this command causes C words to be transmitted between the channel and core storage, starting with location Y. Data transmission continues until C is reduced to zero or an end signal is received by the channel. In either event, the channel read or write select is reset. If, while a CPYD is being executed, an end signal is received before the count is reduced to zero, the channel read or write select is reset and the channel obtains a new command from the next sequential location.

If the next command is other than a copy, the channel executes that command. If the next command is a copy, the channel interrupts on a program sequence check. The last word transmitted under CPYD control remains in the channel assembly register.

If the count for a CPYD goes to zero before the end signal is received, the channel does not get the next sequential command until an end or unusual-end signal is obtained.

In general, when operating under CPYD control, the channel does not obtain the next sequential command until either an end (or unusual end signaling an error) occurs. In the event of an unusual end, an interrupt occurs.

CPYP--Copy and Proceed

This command, when decoded by a channel not in read or write status, causes a sequence check and channel interrupt. If the channel is in read or write status, this command causes C words to be transmitted between the channel and storage starting with location Y. End signals from the file control are ignored and data transmission continues until C is reduced to zero.

When C is reduced to zero, the channel does not disconnect but obtains the next sequential command. If this command is either a CPYD, CPYP, or TCH, operation is normal and data transmission resumes. If the new command is other than CPYD, CPYP, or TCH, the channel disconnects and interrupts on a sequence error.

CHANNEL INTERRUPT AND CONTROL COMMANDS

The channel interrupts command sequence if either the attention or unusual-end conditions occur. The attention interrupt will, in general, be delayed until after the end signal is generated. If attention is generated while the channel is in wait status, the interrupt starts the channel. This interrupt stores the location counter contents in a fixed storage location and transfers channel control to another fixed location. Return to the original channel sequence by means of a leave interrupt program (LIP) command again causes the channel to be in wait status. Interrupt locations are:

Channel	Store Command Counter	Obtain Next Command
A	0042	0043
B	0044	0045
C	0046	0047
D	0050	0051
E	0052	0053
F	0054	0055
G	0056	0057
H	0060	0061

Conditions which yield a channel interrupt may be readily handled by a special channel program sequence. Thus, in the case of either unusual-end or attention signals, the channel is capable of diagnosing the more elementary problems and responding accordingly. As the last input-output unit selected remains selected, the problem of determining which unit on a channel is being dealt with is eliminated. Conditional transfer commands (TCM) can then be used to diagnose the problem, corrective action can be taken, and either a LIP or indirect TCH command can be executed to return to the original channel command sequence.

Once an interrupt occurs on a given channel, subsequent attempts to interrupt on the channel are inhibited until a LIP command is executed by the channel. This command, when executed by a given channel, causes that channel to take its next command from the fixed address contained in the fixed location into which that channel's location counter contents were stored when the interrupt occurred. If a trap command occurs in the interrupt program, it is processed in the normal fashion. Interrupts are also inhibited if a trap is being executed by the channel. This inhibiting persists until either a reset and start or start channel instruction (depending on whether the channel was enabled or not) is executed by the central processing unit. See "TWT."

TCH--Transfer in Channel

This command is the transfer command for all channels. When a TCH command is executed, command sequence control is transferred to location Y.

WTR--Wait and Transfer

When this command is decoded, the channel stops operation and may be thought of as waiting. The channel location counter contains the location of the WTR command. When the channel is told to start, it takes its next command from the location specified by the address part of the WTR command. If an interrupt occurs while the channel is in wait status, return from the interrupt program (by means of the LIP command) puts the channel back in wait status.

TWT--Trap and Wait

Upon decoding a TWT command, the channel suspends operation until either a reset and start or start channel instruction is given by the CPU, depending upon conditions described below. If the channel is enabled for control word or end-of-file traps, the channel causes the CPU to trap to a fixed location. Particulars concerning this trap are described in the "Data Channel Trap" section of the IBM 7090 Data Processing System Reference Manual, Form A22-6528.

If the channel is enabled, start channel instructions are ignored until the trap is executed or a reset and start channel is given, resetting the trap condition. If the channel is not enabled, either a reset and start or a start channel resets the trap and causes the channel to resume operation.

Channel interrupt signals are remembered but not executed until the channel brings in a command other than the TWT. (An RSC resets these stored interrupt signals.)

After the channel has stopped operation as a result of a TWT, the channel command counter contains the location of that command.

Assume that B is the location where the instruction counter contents are stored when a trap occurs on this particular channel and that CPU control is transferred to B+1. SUB is the entry point for the subroutine that the channel requests the CPU to execute.

Command	Address
XMT	B+1, 1
TRA	SUB
TWT	Y

LIP--Leave Interrupt Program

This command causes the channel to transfer control to the location contained in the address part of that channel's fixed "interrupt-to" location. The channel command counter is set to the value in the address portion of this fixed location. Execution of the LIP command also cancels the inhibiting effect of a previous interrupt.

LAR--Load Assembly Register

Execution of this command causes the contents of the assembly register in the channel to be replaced by the C(Y). The C(Y) remain unchanged. After execution, the channel proceeds to the next sequential command.

SAR--Store Assembly Register

Execution of the SAR causes the contents of location Y to be replaced by the contents of the assembly register. Contents of the assembly register remain unchanged. After executing this command, the channel proceeds to the next sequential command.

TCM--Transfer on Condition Met

When the count (C) field is not zero, this command causes C to specify one of the six characters in the assembly register for comparison against the mask field (M). If a bit-for-bit comparison is achieved, the channel executes a transfer to location Y. If the comparison is not achieved, the channel proceeds to the next sequential command.

If C is zero, the channel check condition register is compared against M. Transfer conditions for the comparison are the same as above. When indirect addressing is used, control is transferred to the indirectly addressed location when the condition is met.

Unless interrupts are inhibited, the channel interrupts whenever a bit appears in one or more positions of the channel's condition register. The register indications are:

Position	Function
1	I-O Check: This condition occurs when the channel fails to obtain a storage cycle in time to satisfy demands of the attached I-O device. The condition is monitored in the CPU and indicated by the I-O check light.
2	Sequence Error: This condition occurs as a result of an improper sequence of commands.
3	Unusual End: This condition occurs when transmission is terminated by an unusual-end rather than an end signal.

4	Attention: This is a signal indicating a change in the status of the attached I-O device.
5	Reserve
6	Read-Write Check: This condition occurs when the file control is not operational and a command is encountered by the channel, or when the character rate of the I-O device exceeds the capability of the channel.

All interrupts are executed immediately following the logical termination of the command during which they occur. Attention interrupts occurring during a read or write operation are executed following termination of that operation. There is no provision for enabling only certain interrupts. All interrupts may be disabled by forcing an interrupt and not executing a LIP command.

TDC--Transfer and Decrement Counter

Upon execution of this command, the contents of the six-bit channel control counter are examined. If the contents are not zero, the counter is decremented by one (one is subtracted from it) and control is transferred to location Y. If the contents of the counter are zero, the channel proceeds to the next sequential command without disturbing the counter.

LCC--Load Control Counter

This command causes the contents of the channel control counter to be replaced by the six low-order positions of the count field of the LCC command. The channel then proceeds to the next sequential command. If the LCC is indirectly addressed (bit in position 18), the contents of the control counter are replaced by the six low-order bits contained in the location specified by positions 20-35 of the LCC.

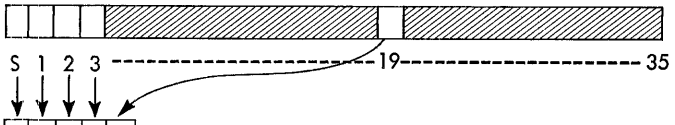
XMT--Transmit

The transmit command causes the C words immediately following the location of the XMT command to be transmitted to C locations starting at location Y.

When the count (C) field is reduced to zero and the Cth word has been transmitted, the channel obtains its next command from the location of the XMT command plus one. If the initial count field is zero, the XMT command is skipped and the channel proceeds to the next sequential command.

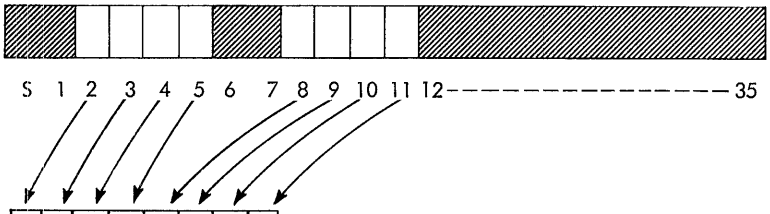
The transmission rate is dependent upon a variety of factors, including the number of channels attached to the system.

Input-Output Command Bit Configurations



S	1	2	3	19	
0	1	0	0	0	Control
0	1	0	0	1	Control and Read
0	1	0	1	0	Control and Write
0	1	0	1	1	Sense
0	1	1	0	0	Load Assembly Register
0	1	1	0	1	Store Assembly Register
0	1	1	1	0	Trap and Wait
1	1	0	0	1	Leave Interrupt Program
1	1	0	1	0	Transfer and Decrement Counter
1	1	0	1	1	Load Control Counter
0	0	0		0	Wait and Transfer
0	0	0		1	Transmit
0	0	1		0	Transfer in Channel
1	0	0		0	Copy and Proceed
1	0	1		0	Copy and Disconnect
1	0	1		1	Transfer on Condition Met

Order Configurations



2	3	4	5	8	9	10	11	
0	0	0	0	0	0	0	0	No Operation
0	0	0	0	1	0	0	0	Eight Bit Mode
0	0	0	0	1	0	0	1	Six Bit Mode
1	0	0	0	0	0	0	0	Seek
1	0	0	0	0	0	1	0	Prepare to Verify (Single Record)
1	0	0	0	0	0	1	1	Select and Condition
1	0	0	0	0	1	0	0	Prepare to Verify (Cylinder--Optional Feature)
1	0	0	0	0	1	1	0	Prepare to Write Check
1	0	0	0	0	1	1	1	Set Access Inoperative
1	0	0	0	1	0	0	0	Prepare to Verify (Track)

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