# Hard disk drive specifications

# Deskstar 40GV & 75GXP

## 3.5 inch ATA/IDE hard disk drive

Models:

| | |
|---|---|
| DTLA-305010 | DTLA-307015 |
| DTLA-305020 | DTLA-307020 |
| DTLA-305030 | DTLA-307030 |
| DTLA-305040 | DTLA-307045 |
| | DTLA-307060 |
| | DTLA-307075 |

Revision 1.0

S07-4778-01

**2nd Edition (Revision 1.0) S07N-4778-01 (10 May, 2000)**
**1st Edition (Revision 0.1) S07N-4778-00 (15 March, 2000) Preliminary**



Technical information about this product is available by contacting your local IBM representative or on the |Internet at **http://www.ibm.com/harddrive**

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# Figures

# 1.0 General

This document describes the specifications of the following IBM 3.5-inch ATA interface hard disk drives:

- DTLA-305010 (10.2GB) (5400 RPM)
- DTLA-305020 (20.5GB) (5400 RPM)
- DTLA-305030 (30.7GB) (5400 RPM)
- DTLA-305040 (41.1GB) (5400 RPM)

- DTLA-307015 (15.3GB) (7200 RPM)
- DTLA-307020 (20.5GB) (7200 RPM)
- DTLA-307030 (30.7GB) (7200 RPM)
- DTLA-307045 (46.1GB) (7200 RPM)
- DTLA-307060 (61.4GB) (7200 RPM)
- DTLA-307075 (76.8GB) (7200 RPM)

*Note:The specifications in this document are subject to change without notice.*

## 1.1 Glossary

| | |
|---|---|
| ESD | Electrostatic Discharge |
| Kbpi | 1,000 bits per inch |
| Ktpi | 1,000 tracks per inch |
| Mbps | 1,000,000 bits per second |
| GB | 1,000,000,000 bytes |
| MB | 1,000,000 bytes |
| KB | 1,000 bytes unless otherwise specified |
| 32KB | 32 x 1024 bytes |
| 64KB | 64 x 1024 bytes |
| S.M.A.R.T. | Self-Monitoring Analysis and Reporting Technology |
| DFT | Drive Fitness Test |
| ADM | Automatic Drive Maintenance |

## 1.2 General caution

The drive can be damaged by shock or ESD (Electrostatic Discharge). Any damage sustained by the drive after removal from the shipping package and opening the ESD protective bag are the responsibility of the user.

## 1.3 References

- ATA/ATAPI-5 (T13/1321D Revision 2)

# 2.0 General features

- Data capacities of 10.2GB - 76.8GB
- Spindle speeds of 5400 RPM (DTLA-305xxx) and 7200 RPM (DTLA-307xxx)
- Enhanced IDE (ATA-5) interface
- Sector format of 512 bytes/sector
- Closed-loop actuator servo
- Automatic Actuator lock
- Interleave factor 1:1
- Seek time of 8.5ms in Read Operation including Command Overhead (DTLA-307xxx)
- Seek time of 9.5ms in Read Operation including Command Overhead (DTLA-305xxx)
- Sector Buffer 512KB (DTLA-305xxx) or 2048KB (DTLA-307xxx)
  Upper 132KB is used for firmware
- Ring buffer implementation
- Write Cache
- Queued feature support
- Advanced ECC On The Fly (EOF)
- Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- PIO Data Transfer Mode 4 (16.6MB/sec)
- DMA Data Transfer
  - Multiword mode Mode 2 (16.6MB/sec)
  - Ultra DMA Mode 4 (66.6MB/sec)
- CHS and LBA mode
- Transparent Defect Management with ADR (Automatic Defect Reallocation)
- Power Saving modes
- S.M.A.R.T. (Self Monitoring and Analysis Reporting Technology)
- Security function support
- Default Logical Head Number (16 or 15) selectable with jumper
- Address Offset Feature for DFT implementation

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# Part 1. Functional specification

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# 3.0 Fixed disk subsystem description

## 3.1 Control Electronics

The drive is electronically controlled by a microprocessor, several logic modules, digital/analog modules, and various drivers and receivers. The control electronics performs the following major functions:

- Controls and interprets all interface signals between the host controller and the drive.
- Controls read write accessing of the disk media, including defect management and error recovery.
- Controls starting, stopping, and monitoring of the spindle.
- Conducts a power-up sequence and calibrates the servo.
- Analyzes servo signals to provide closed loop control. These include position error signal and estimated velocity.
- Monitors the actuator position and determines the target track for a seek operation.
- Controls the voice coil motor driver to align the actuator in a desired position.
- Constantly monitors error conditions of the servo and takes corresponding action if an error occurs.
- Monitors various timers such as head settle and servo failure.
- Performs self-checkout (diagnostics).

## 3.2 Head disk assembly

The head disk assembly (HDA) is assembled in a clean room environment and contains the disks and actuator assembly. Air is constantly circulated and filtered when the drive is operational. Venting of the HDA is accomplished via a breather filter.

The spindle is driven directly by an in-hub, brushless, sensorless DC drive motor. Dynamic braking is used to quickly stop the spindle.

## 3.3 Actuator

The read/write heads are mounted in the actuator. The actuator is a swing-arm assembly driven by a voice coil motor. A closed-loop positioning servo controls the movement of the actuator. An embedded servo pattern supplies feedback to the positioning servo to keep the read/write heads centered over the desired track.

The actuator assembly is balanced to allow vertical or horizontal mounting without adjustment.

When the drive is powered off, the actuator automatically moves the head to the actuator ramp outside of the disk where it is parked.

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# 4.0 Drive characteristics

This chapter describes the characteristics of the drive.

## 4.1 Default logical drive parameters

The default of the logical drive parameters in Identify Device data are as shown below.

| Model | Capacity (GB) | Word 1 (Cyl) | Word 3 (Head) | Word 6 Sect/Trk) | Word 60-61 (LBA) | Customer Usable Data Bytes |
|---|---|---|---|---|---|---|
| DTLA-305010 | 10.2 | 16,383 | 16/15 | 63 | 20,074,320 | 10,278,051,840 |
| DTLA-305020 | 20.5 | 16,383 | 16/15 | 63 | 40,188,960 | 20,576,747,520 |
| DTLA-305030 | 30.7 | 16,383 | 16/15 | 63 | 60,036,480 | 30,738,677,760 |
| DTLA-305040 | 41.1 | 16,383 | 16/15 | 63 | 80,418,240 | 41,174,136,880 |
| DTLA-307015 | 15.6 | 16,383 | 16/15 | 63 | 30,003,120 | 15,361,597,440 |
| DTLA-307020 | 20.5 | 16,383 | 16/15 | 63 | 40,188,960 | 20,576,747,520 |
| DTLA-307030 | 30.7 | 16,383 | 16/15 | 63 | 60,036,480 | 30,738,677,760 |
| DTLA-307045 | 46.1 | 16,383 | 16/15 | 63 | 90,069,840 | 46,115,758,080 |
| DTLA-307060 | 61.4 | 16,383 | 16/15 | 63 | 120,103,200 | 61,492,838,400 |
| DTLA-307075 | 76.8 | 16,383 | 16/15 | 63 | 150,136,560 | 76,869,918,720 |

Figure 1. Default logical drive parameters

*Note: 16 is the ship default value of Word 3 (Head) in Figure 1. This value can be changed by jumper. Refer to 7.3, "Jumper Settings," on page 41 for further information.*

## 4.2 Data sheet

| | DTLA-307xxx | DTLA-305xxx |
|---|---|---|
| Media transfer rate (Mb/sec) | 444 max | 372 max |
| Interface transfer rate (MB/sec) | 16.6 (PIO Mode-4)<br>66.6 (Ultra DMA/66) | 16.6 (PIO Mode-4)<br>66.6 (Ultra DMA/66) |
| Data buffer size (KB[1)] | 2,048 | 512 |
| Rotational speed (RPM) | 7,200 | 5,400 |
| Average latency (msec) | 4.17 | 5.56 |
| Recording density (Kbpi) | 391 max | 415 max |
| Track density (Ktpi) | 28.35 | 35 |
| Areal density (Gbits/in$^2$) | 11 max | 14.5 max |
| Number of zones | 12 | 12 |
| Number of data disks | 5/4/3/2/1 | 2/1 |
| Number of data heads | 10/8/6/4/3/2 | 4/3/2 |
| Servo method | Embedded sector servo | Embedded sector servo |

[1]Upper 132KB is used for firmware

Figure 2. Mechanical positioning performance

## 4.3 Drive organization

### 4.3.1 Drive format

Upon shipment from IBM manufacturing the drive satisfies the sector continuity in the physical format by means of the defect flagging strategy described in section 5.0 in order to provide the maximum performance to users.

### 4.3.2 Cylinder allocation

| | DTLA-305XXX | | DTLA-307XXX | |
|---|---|---|---|---|
| | **Physical Cylinders** | **Sectors/Track** | **Physical Cylinders** | **Sectors/Track** |
| Data Zone 0 | 0–623 | 792 | 0–1375 | 702 |
| Data Zone 1 | 624–2047 | 780 | 1376–2831 | 684 |
| Data Zone 2 | 2048–3727 | 760 | 2832–4239 | 666 |
| Data Zone 3 | 3728–5343 | 740 | 4240–6975 | 648 |
| Data Zone 4 | 5344–8095 | 720 | 6976–9759 | 612 |
| Data Zone 5 | 8096–10975 | 680 | 9760–11551 | 594 |
| Data Zone 6 | 10976–12879 | 660 | 11552–13631 | 567 |
| Data Zone 7 | 12880–15263 | 630 | 13632–16239 | 540 |
| Data Zone 8 | 15264–18591 | 600 | 16240–18319 | 504 |
| Data Zone 9 | 18592–23023 | 540 | 18320–19567 | 486 |
| Data Zone 10 | 23024–27551 | 480 | 19568–21199 | 459 |
| Data Zone 11 | 27552–29743 | 440 | 21200–23519 | 432 |
| Data Zone 12 | 29744–31343 | 420 | 23520–25215 | 396 |
| Data Zone 13 | 31344–32511 | 400 | 25216–26319 | 378 |
| Data Zone 14 | 32512–34326 | 370 | 26320–27724 | 351 |

Figure 3. Cylinder allocation

Physical cylinder is calculated from the starting data track of 0. It is not relevant to logical CHS. Depending on the capacity some of the inner zone cylinders are not allocated.

**Data cylinder**
This cylinder contains the user data which can be sent and retrieved via read/write commands and a spare area for reassigned data.

## 4.4 Performance characteristics

Drive performance is characterized by the following parameters:

- Command overhead
- Mechanical positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (Look ahead/Write cache)

All the above parameters contribute to drive performance. There are also other parameters that contribute to the performance of the actual system. This specification defines the characteristics of the drive, not the characteristics of the system throughput which depends on the system and the application.

## 4.4.1 Command overhead

Command overhead is defined as the time required

- from the time the command is written into the command register by a host
- to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer
- excluding
  - Physical seek time
  - Latency

The table below gives average command overhead.

| **Command type (Drive is in quiescent state)** | **Time (Typical)** (ms) | **Time (Typical) for queued command** (ms) |
|---|---|---|
| Read (Cache not hit) (from Command Write to Seek Start) | 0.3 | 0.3 |
| Read (Cache hit) (from Command Write to DRQ) | 0.1 | 0.1 |
| Write (from Command Write to DRQ) | 0.015 | 0.05 |
| Seek (from Command Write to Seek Start) | 0.3 | not applicable |

Figure 4. Command overhead

## 4.4.2 Mechanical positioning

### 4.4.2.1 Average seek time (without command overhead, including settling)

| **Command Type** | **Typical** (ms) | | **Max** (ms) | |
|---|---|---|---|---|
| | DTLA-305XXX | DTLA-307XXX | DTLA-305XXX | DTLA-307XXX |
| Read | 9.2 | 8.2 | 10.2 | 9.2 |
| Write | 10.2 | 9.2 | 11.2 | 10.2 |

Figure 5. Mechanical positioning performance

The terms “Typical” and “Max” are used throughout this specification with the following meanings:

**Typical.** The average of the drive population tested at nominal environmental and voltage conditions.

**Max.** The maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See 7.4 “Environment” on page 46 and 7.5 “DC Power Requirements” on page 48.

Seek time is measured from the start of the motion of the actuator to the start of **a reliable read or write operation**. “Reliable read or write” implies that error correction/recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted average} = \frac{\sum_{n=1}^{max} (max+1-n)\,(Tn.in+Tn.out)}{(max+1)\,(max)}$$

where

max = Maximum seek length
n = seek length (1 to max)
Tn.in = Inward measured seek time for an n track seek
Tn.out = Outward measured seek time for an n track seek

### 4.4.2.2 Full stroke seek (without command overhead, including settling)

| **Function** | **Typical** (ms) | | **Max** (ms) | |
|---|---|---|---|---|
| | DTLA-305XXX | DTLA-307XXX | DTLA-305XXX | DTLA-307XXX |
| Read | 16.7 | 14.7 | 19.7 | 17.7 |
| Write | 18.3 | 15.7 | 21.3 | 18.7 |

Figure 6. Full stroke seek time

Full stroke seek is measured as the average of 1000 full stroke seeks with a **random head switch** from both directions (inward and outward).

### 4.4.2.3 Head switch time (Head skew)

| **Head switch time** | **Typical** (ms) |
|---|---|
| DTLA-305XXX | 1.5 |
| DTLA-307XXX | 1.2 |

Figure 7. Head switch time

Head switch time is defined as the amount of time required by the fixed disk to complete a seek of the next sequential track after reading the last sector in the current track

The measuring method is given in 4.4.6 “Throughput” on page 16.

### 4.4.2.4 Cylinder switch time (Cylinder skew)

| **Cylinder switch time** | **Typical** (ms) |
|---|---|
| DTLA-305XXX | 2.0 |
| DTLA-307XXX | 1.7 |

Figure 8. Cylinder Skew

A cylinder switch time is defined as the amount of time required by the fixed disk to access the next sequential block after reading the last sector in the current cylinder.

The measuring method is given in 4.4.6, “Throughput” on page 16.

### 4.4.2.5 Single track seek time (without command overhead, including settling)

| **Function** | **Typical** (ms) | | **Max** (ms) | |
|---|---|---|---|---|
| | DTLA-305XXX | DTLA-307XXX | DTLA-305XXX | DTLA-307XXX |
| Read | 1.3 | 0.9 | 2.0 | 1.6 |
| Write | 1.8 | 1.4 | 2.5 | 2.1 |

Figure 9. Single Track Seek Time

Single track seek is measured as the average of one (1) single track seek from every track with a random head switch in both directions (inward and outward).

### 4.4.2.6 Average latency

| **Average latency** | **Time for a revolution** (ms) | **Average latency** (ms) |
|---|---|---|
| DTLA-305XXX | 11.1 | 5.56 |
| DTLA-307XXX | 8.3 | 4.17 |

Figure 10. Latency Time

## 4.4.3 Drive ready time

| **Power on to ready** | **Typical** (sec) | **Maximum** (sec) |
|---|---|---|
| DTLA-305XXX | 13 | 31 |
| DTLA-307XXX | 18 | 31 |

Figure 11. Drive ready time

**Ready** The condition in which the drive is able to perform a media access command (e.g. read,write) immediately.

**Power on** This includes the time required for the internal self diagnostics.

*Note: Max Power On to ready time is the maximum time period that Device 0 waits for Device 1 to assert PDIAG–.*

## 4.4.4 Data transfer speed

| **Data transfer speed** | **DTLA-305XXX** (Mbyte/sec) | **DTLA-307XXX** (Mbyte/sec) |
|---|---|---|
| Disk-Buffer transfer (Zone 0) | | |
| Instantaneous - typical | 36.5 | 43.4 |
| Sustained - typical | 31.8 | 37.7 |
| Disk-Buffer transfer (Zone 14) | | |
| Instantaneous - typical | 17.0 | 21.7 |
| Sustained - read typical | 14.8 | 18.8 |
| Sustained - write typical | 14.8 | 18.8 |
| Buffer-Host (max) | 100 | 100 |

Figure 12. Data transfer speed

- Instantaneous disk-buffer transfer rate (Mbyte/sec) is derived by the formula

  (Number of sectors on a track) * 512 * (revolution/sec)

  *Note:The number of sectors per track will vary because of the linear density recording.*

- Sustained disk-buffer transfer rate (Mbyte/sec) is defined by considering head/cylinder change time for read operation. This gives a local average data transfer rate. It is derived by the formula

  (Sustained Transfer Rate) = A / (B +C +D ) where

  A = (Number of data sectors per cylinder) * 512
  B = ((# of Surface per cylinder) - 1) * (Head switch time)
  C = (Cylinder change time)
  D = (# of Surface) * (One revolution time)

- Instantaneous buffer-host transfer rate (Mbyte/sec) defines the maximum data transfer rate on the AT Bus. It also depends on the speed of the host.

The method of measurement is given in 4.4.6, “Throughput” on page 16.

## 4.4.5 Buffering Operation (Look ahead/Write cache)

To improve the total performance, the drive utilizes a ring buffer for look ahead and write cache. The total 380KB (DTLA-305XXX) and 1916KB (DTLA-307XXX) of the buffer is divided into multiple segmented blocks for write buffer or read buffer use.

Write data will be cached in the buffer for the random block request.

## 4.4.6 Throughput

### 4.4.6.1 Simple sequential access

| **Sequential read** | **Typical** (sec) | | **Max** (sec) | |
|---|---|---|---|---|
| | DTLA-305XXX | DTLA-307XXX | DTLA-305XXX | DTLA-307XXX |
| Zone 0 | 0.57 | 0.48 | 0.60 | 0.50 |
| Zone 14 | 1.20 | 0.95 | 1.26 | 1.00 |

Figure 13. Simple Sequential Access performance

The above table gives the time required to read/write for a total of 8000x consecutive blocks (16,777,216 bytes) accessed by 128 read commands. Typical and Max values are given by 105% and 110% of T respectively throughout following performance description.

*Note: It is assumed that a host system responds instantaneously and host data transfer is faster than sustained data rate.*

T = A + B + C + 16,777,216/D + 512/E (READ)

where

T = Calculated time (sec)

A = Command process time (Command overhead) (sec)

B = Average seek time (sec)

C = Average latency (sec)

D = Sustained disk-buffer transfer rate (byte/sec)

E = Buffer-host transfer rate (byte/sec)

### 4.4.6.2 Random access

| **Random read** | **Typical** (sec) | **Maximum** (sec) |
|---|---|---|
| DTLA-305XXX | 65 | 68 |
| DTLA-307XXX | 55 | 57 |

Figure 14. Random Access Performance

The above table gives the time required to execute a total of 1000h read/write commands which access a random LBA.

T = (A + B + C + 512/D + 512/E) * 4096 (READ)

where

T = Calculated time (sec)

A = Command process time (Command overhead) (sec)

B = Average seek time (sec)

C = Latency

D = Average sustained disk-buffer transfer rate (byte/sec)

E = Buffer-host transfer rate (byte/sec)

## 4.4.7 Operating modes

### 4.4.7.1 Operating mode descriptions

| Operating mode | Description |
|---|---|
| **Spin-up** | Start up time period from spindle stop or power down |
| **Seek** | Seek operation mode |
| **Write** | Write operation mode |
| **Read** | Read operation mode |
| **Idle** | Spindle motor and servo system are working normally**.** Commands can be received and processed immediately**.** |
| **Standby** | Actuator is unloaded and spindle motor is stopped. Commands can be received immediately. |
| **Sleep** | Actuator is unloaded and spindle motor is stopped. Only soft reset or hard reset can change the mode to standby. |

*Note: Upon power down or spindle stop a head locking mechanism will secure the heads in the OD parking position.*

### 4.4.7.2 Mode transition times

Mode transition times are shown below.

| From | To | RPM | Transition time (typical ) (sec) | Transition time (max) (sec) |
|---|---|---|---|---|
| Standby | Idle | 5400 (2 disks)<br>7200 (3 disks)<br>7200 (5 disks) | 11<br>16<br>18 | 31<br>31<br>31 |
| Idle | Standby | | Immediately | Immediately |
| Standby | Sleep | | Immediately | Immediately |
| Sleep | Standby | | Immediately | Immediately |

*Note: The command is processed immediately but there will be an actual spin down time reflecting the seconds passed until the spindle motor stops.*

Figure 15. Mode transition times

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# 5.0 Defect flagging strategy

Media defects are remapped to the next available sector during the Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internally maintained table.

**Shipped format**

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by spare tracks of inner zone.

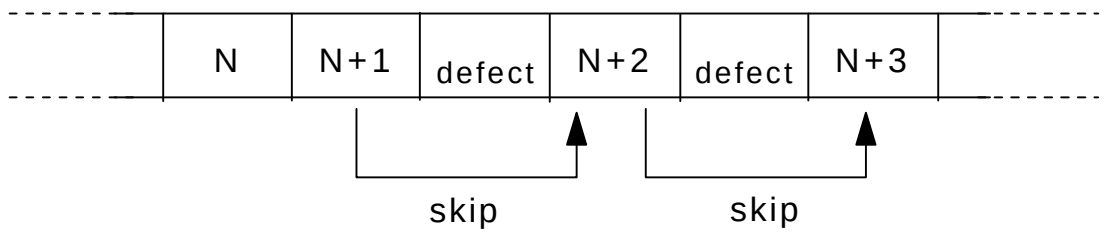


Figure 16. PList physical format

Defects are skipped without any constraint, such as track or cylinder boundary. The calculation from LBA to physical is done automatically by internal table.

*Note: It is possible to reallocate sectors during drive usage including sectors damaged during the early period of usage. Reallocation of sectors is primarily caused by handling problems and is a normal maintenance function performed by the hard disk drive.*

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# 6.0 Data integrity

## 6.1 Data loss at Power off

- The drive retains recorded information under all non-write operations.
- No more than one sector can be lost by power down during write operation while write cache is disabled.
- Power off during write operations may make an incomplete sector which will report hard data error when read. The sector can be recovered by a rewrite operation.
- Hard reset does not cause any data loss.
- If the write cache option is active, the data in the write cache will be lost. To prevent the loss of customer data, it is recommended that the last write access before power off be issued after setting write cache to off.

## 6.2 Write cache

- Power off while write cache is enabled may cause the loss of data remaining in the cache that has not been flushed onto the disk media. Therefore, it is possible for data to be lost due to a power off after write command completion.
- There are two ways to check if all data in the write cache has been flushed onto the disk. Checking just before power off is recommended to prevent data loss.
  - Confirm successful completion of Software Reset
  - Confirm successful completion of Flush Cache command

## 6.3 Equipment status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- Access recalibration/tuning is complete
- Spindle speed meets requirements for reliable operation
- Self-check of drive is complete

Appropriate error status is made available to the host system if any of the following conditions occur after the drive has become ready:

- Spindle speed outside requirements for reliable operation
- Occurrence of a WRITE FAULT condition

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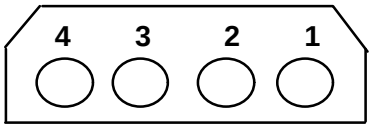
# 7.0 Specification

## 7.1 Electrical interface

### 7.1.1 Connectors

#### 7.1.1.1 DC power connector

The DC power connector is designed to mate with AMP (part 1-480424-0) using AMP pins part 350078-4 (strip) or part 61173-4 (loose piece) or their equivalents. Pin assignments are shown in the figure below.




| Pin | Voltage |
|---|---|
| 1 | +12 V |
| 2 | GND |
| 3 | GND |
| 4 | +5V |

Figure 17. Power connector pin assignments

#### 7.1.1.2 AT signal connector

The AT signal connector is a 40-pin connector.

## 7.1.2 Signal definition

The pin assignments of interface signals are listed in the figure below:

| PIN | SIGNAL | I/O | Type | PIN | SIGNAL | I/O | Type |
|---|---|---|---|---|---|---|---|
| 01 | RESET- | I | TTL | 02 | GND | | |
| 03 | DD7 | I/O | 3-state | 04 | DD8 | I/O | 3-state |
| 05 | DD6 | I/O | 3-state | 06 | DD9 | I/O | 3-state |
| 07 | DD5 | I/O | 3-state | 08 | DD10 | I/O | 3-state |
| 09 | DD4 | I/O | 3-state | 10 | DD11 | I/O | 3-state |
| 11 | DD3 | I/O | 3-state | 12 | DD12 | I/O | 3-state |
| 13 | DD2 | I/O | 3-state | 14 | DD13 | I/O | 3-state |
| 15 | DD1 | I/O | 3-state | 16 | DD14 | I/O | 3-state |
| 17 | DD0 | I/O | 3-state | 18 | DD15 | I/O | 3-state |
| 19 | GND | | | (20) | key | | |
| 21 | DMARQ | O | 3-state | 22 | GND | | |
| 23 | DIOW-(*) | I | TTL | 24 | GND | | |
| 25 | DIOR-(*) | I | TTL | 26 | GND | | |
| 27 | IORDY(*) | O | 3-state | 28 | CSEL | I | TTL |
| 29 | DMACK- | I | TTL | 30 | GND | | |
| 31 | INTRQ | O | 3-state | 32 | IOCS16-(**) | O | OC |
| 33 | DA1 | I | TTL | 34 | PDIAG- | I/O | OC |
| 35 | DA0 | I | TTL | 36 | DA2 | I | TTL |
| 37 | CSO- | I | TTL | 38 | CS1- | I | TTL |
| 39 | DASP- | I/O | OC | 40 | GND | | |

Figure 18. Table of signals

***Notes:***

1. "O" designates an output from the drive.
2. "I" designates an input to the drive.
3. "I/O" designates an input/output common.
4. "OC" designates open-collector or open-drain output.
5. The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the Host decides to allow a DMA burst if the Ultra DMA transfer mode was previously chosen via SetFeatures. The Drive becomes aware of this change upon assertion of the DMACK- line. These lines revert back to their original definitions upon the deassertion of DMACK- at the termination of the DMA burst.
6. (**) complies with ATA-2.

| | Special Definition (for Ultra DMA) | Conventional Definition |
|---|---|---|
| Write Operation | DDMARDY-<br>HSTROBE<br>STOP | IORDY<br>DIOR-<br>DIOW- |
| Read Operation | HDMARDY-<br>DSTROBE<br>STOP | DIOR-<br>IORDY<br>DIOW- |

Figure 19. Signal special definitions for Ultra DMA

**DD0-DD15** 16-bit bi-directional data bus between the host and the drive. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00-15, are used for data transfer. These are 3-State lines with 24 mA current sink capability.

**DA0-DA2** Address used to select the individual register in the drive.

**CS0-** Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error {Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status {Command when written} register) can be selected. (See Figure 42 on page 40.)

**CS1-** Chip select signal generated from the Host address bus. When active one of the Control Block Registers (Alternate Status {Device Control when written} and Drive Address register) can be selected. (See Figure 42 on page 40.)

**RESET-** This line is used to reset the drive. It shall be kept in Low logic state during power up and in High thereafter.

**DIOW-** The strobe signal asserted by the host to write device registers or the data port.

**DIOR-** The strobe signal asserted by the host to read device registers or the data port.

**INTRQ** Interrupt is enabled only when the drive is selected and the host activates the nIEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.

**IOCS16-** Indication to the host that a 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

**DASP-** This is a time-multiplexed signal which indicates that a drive is active, or that device 1 is present. This signal is driven by Open-Drain driver and internally pulled-up to 5 volts through a 10kΩ resistor.

During Power-on initialization or after RESET- is negated, DASP- shall be asserted by Device 1 within 400 ms to indicate that device 1 is present. Device 0 shall allow up to 450 ms for device 1 to assert DASP-. If device 1 is not present, device 0 may assert DASP- to drive an LED indicator.

DASP- shall be negated following acceptance of the first valid command by device 1. Anytime after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

**PDIAG-** PDIAG- shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics. This line is pulled-up to 5 volts in the drive through a 10kΩ resistor.

Following a Power On Reset, software reset, or RESET-, drive 1 shall negate PDIAG- within 1 ms (to indicate to device 0 that it is busy). Drive 1 shall then assert PDIAG- within 30 seconds to indicate that it is no longer busy and is able to provide status.

Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate PDIAG- within 1 ms to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert PDIAG-. Device 1 should clear BSY before asserting PDIAG-, as PDIAG- is used to indicate that device 1 has passed its diagnostics and is ready to post status.

If DASP- was not asserted by device 1 during reset initialization, device 0 shall post its own status immediately after it completes diagnostics and clear the device 1 Status register to 00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

Device 1 shall release PDIAG-/CBLID- no later than after the first command following a power on or hardware reset sequence so that the host may sample PDIAG-/CBLID- in order to detect the presence or absence of an 80-conductor cable assembly.

**CSEL (Cable Select) (Optional)**

The drive is configured as either Device 0 or 1 depending upon the value of CSEL.

- If CSEL is grounded, the device address is 0.
- If CSEL is open, the device address is 1.

**KEY** Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion by mistake.

**IORDY** This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request, and may be negated when the host transfer cycle is less than 240 ns for PIO data transfer. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

**DMACK-** This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

This signal is internally pulled up to 5 Volt through a 15 KΩ resistor and the tolerance of the resistor value is –50% to +100%.

**DMARQ** This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used on a handshake manner with DMACK-. This signal is a 3-state line with 24mA sink capability and internally pulled down to GND through 10 KΩ resistor.

**HDMARDY- (Ultra DMA)**

This signal is used only for Ultra DMA data transfers between the host and the device.

HDMARDY- is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate HDMARDY- to pause an Ultra DMA data in transfer.

**HSTROBE (Ultra DMA)**

This signal is used only for Ultra DMA data transfers between the host and the device.

HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

**STOP (Ultra DMA)**

This signal is used only for Ultra DMA data transfers between the host and the device.

STOP shall be asserted by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

**DDMARDY- (Ultra DMA)**

This signal is used only for Ultra DMA data transfers between the host and the device.

DDMARDY- is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate DDMARDY- to pause an Ultra DMA data out transfer.

**DSTROBE (Ultra DMA)**

This signal is used only for Ultra DMA data transfers between the host and the device.

DSTROBE is the data in strobe signal from the device for an Ultra DMA data in transfer. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

The termination resistors at the device side are implemented as follows:

Device Termination (implemented on the drive side)

- 33 Ω for DD0 thru DD15, DMARQ, INTRQ
- 82 Ω for CS0-, CS1-, DA0, DA1, DA2, DIOR-, DIOW-, DMACK-
- 22 Ω for IORDY

## 7.1.3 Interface logic signal levels

The interface logic signal has the following electrical specifications:

| | | |
|---|---|---|
| Inputs | Input High Voltage | 2.0 V min. |
| | Input Low Voltage | 0.8 V max. |
| Outputs | Output High Voltage | 2.4 V min. |
| | Output Low Voltage | 0.5 V max. |

# 7.2 Signal timings

## 7.2.1 Reset timings

Drive reset timing.

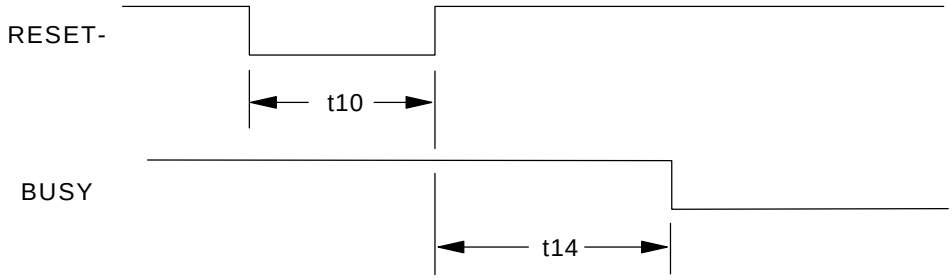



Figure 20. System reset timing chart

| | PARAMETER DESCRIPTION | Min (sec) | Max (sec) |
|---|---|---|---|
| t10 | RESET low width | 25 | |
| t14 | RESET high to not BUSY | – | 31 |

Figure 21. System reset timing

## 7.2.2 PIO timings

The PIO cycle timings meet Mode 4 of the ATA/ATAPI-4 description.

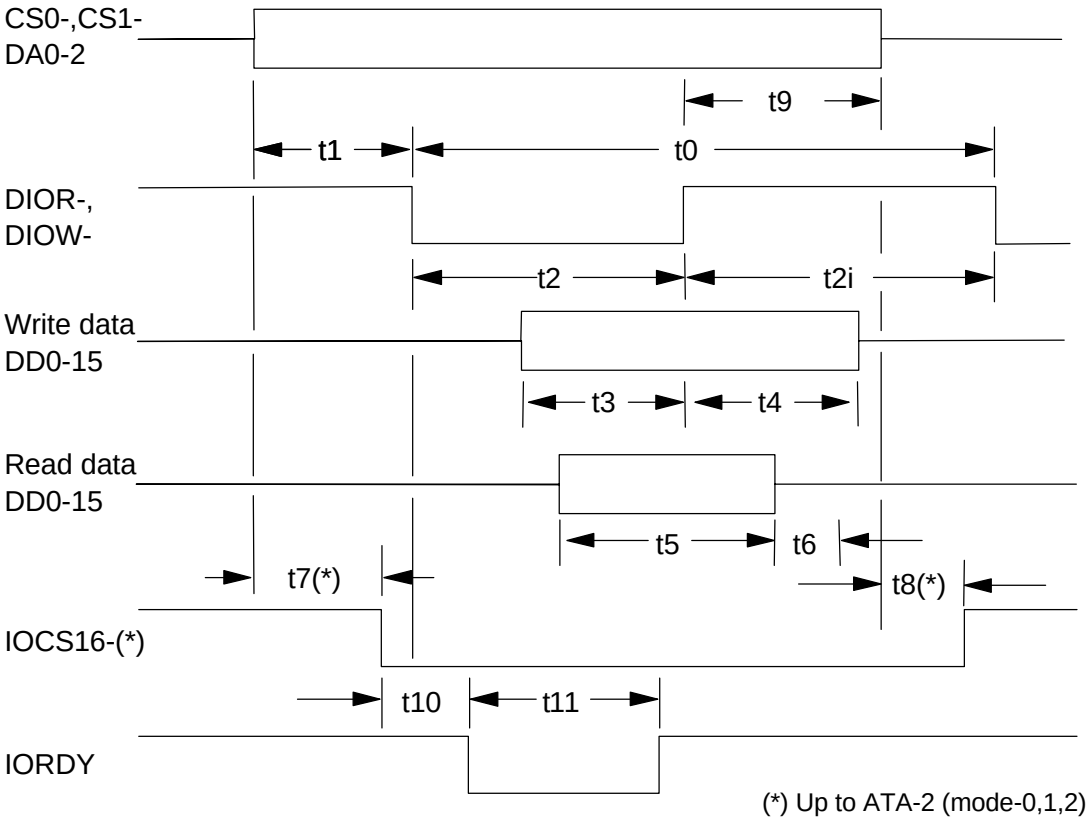



Figure 22. PIO cycle time chart

| | PARAMETER DESCRIPTION | MIN (ns) | MAX (ns) |
|---|---|---|---|
| t0 | Cycle time | 120 | – |
| t1 | CS0- CS1-, DA00–02 valid to DIOR-, DIOW- active | 25 | – |
| t2 | DIOR-, DIOW- pulse width | 70 | – |
| t2i | DIOR-, DIOW- recovery | 25 | – |
| t3 | DD00–15 setup to DIOW- high | 20 | – |
| t4 | DIOW- high to DD00–15 hold | 10 | – |
| t5 | DD0–15 setup to DIOR- high | 20 | – |
| t6 | DIOR- high to DD0–15 hold | 5 | – |
| t7(*) | CS0-, CS1-, DA0–02 valid to IOCS16- assertion | – | 40 |
| t8(*) | CS0-, CS1-, DA0–02 invalid to IOCS16- negation | – | 30 |
| t9 | DIOR-, DIOW- high to CS0-, CS1-, DA0-2 hold | 10 | - |
| t10 | DIOR-, DIOW- low to IORDY low | – | 35 |
| t11 | IORDY pulse width | – | 1250 |

Figure 23. PIO cycle timings

#### 7.2.2.1 Write DRQ interval time

For write sectors and write multiple operations 3.8 us is inserted from the end of negation of the DRQ bit until setting of the next DRQ bit.

#### 7.2.2.2 Read DRQ interval time

For read sectors and read multiple operations the interval from the end of negation of the DRQ bit until setting of the next DRQ bit is as follows:

- In the event that a host reads the status register only before the sector or block transfer DRQ interval

  DRQ interval ..... 4.2 us

- In the event that a host reads the status register after or both before and after the sector or block transfer

  DRQ interval ..... 11.5 us

## 7.2.3 Multiword DMA timings

The Multiword DMA timing meets Mode 2 of the ATA/ATAPI-4 description.

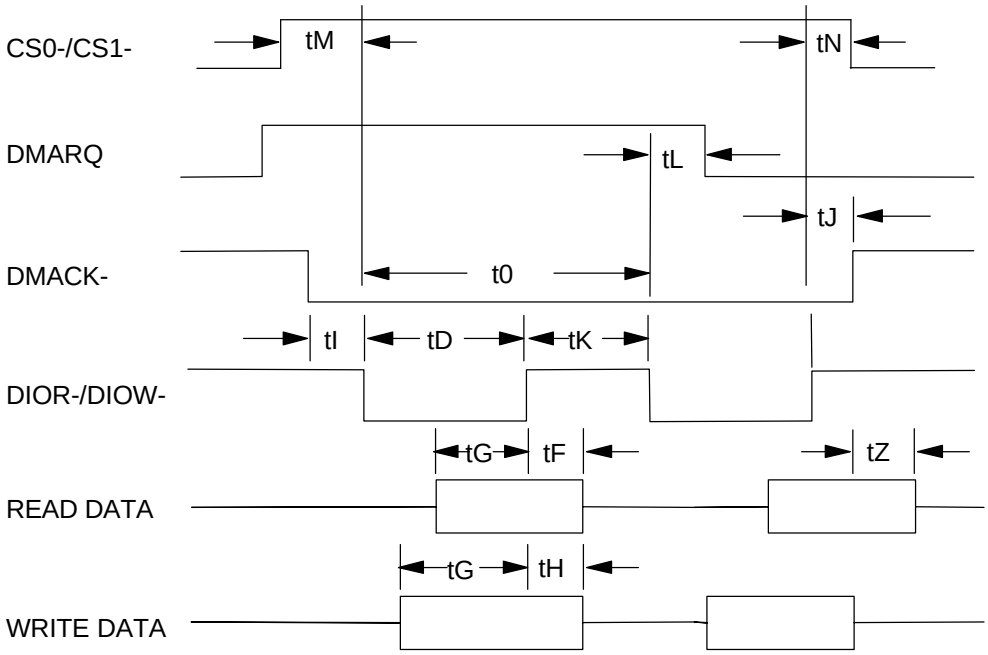



Figure 24. Multiword DMA cycle timing chart

| | PARAMETER DESCRIPTION | MIN (ns) | MAX (ns) |
|---|---|---|---|
| t0 | Cycle time | 120 | – |
| tD | DIOR–, DIOW– pulse width | 70 | – |
| tE | DIOR– data access | 50 | – |
| tF | DIOR– data hold | 5 | – |
| tG | DIOR–/DIOW– data setup | 20 | – |
| tH | DIOW– data hold | 10 | – |
| tI | DMACK– to –DIOR/–DIOW setup | 0 | – |
| tJ | DIOR–/DIOW– to DMACK- delay | 5 | – |
| tK | DIOR–/DIOW– negated pulse width | 25 | – |
| tL | DIOR–/DIOW– to DMARQ– delay | – | 35 |
| tM | CS (1:0) valid to DIOR–/DIOW– | 25 | – |
| tN | CS (1:0) hold | 10 | – |
| tZ | –DMACK to tristate | – | 25 |

Figure 25. Multiword DMA cycle timings

## 7.2.4 Ultra DMA timings

The Ultra DMA timing meets Mode 0,1,2,3 and 4 of the Ultra DMA Protocol.

### 7.2.4.1 Initiating Read DMA

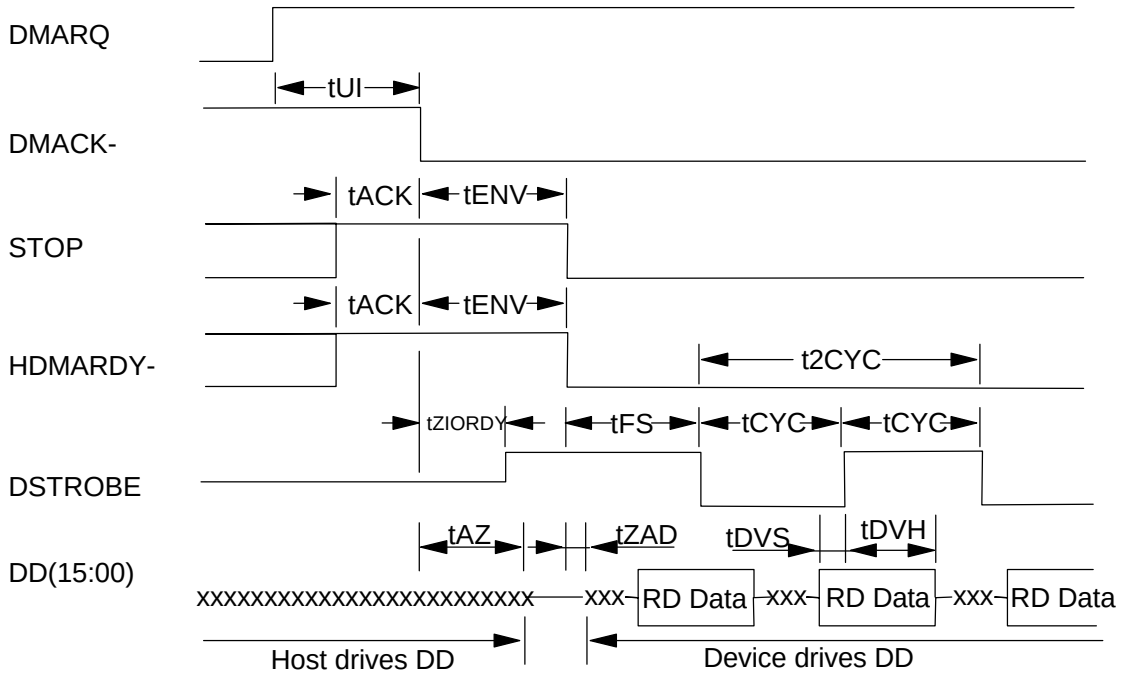



Figure 26. Ultra DMA cycle timing chart (Initiating Read)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tUI | Unlimited interlock time | 0 | – | 0 | – | 0 | 0 | 0 | – | 20 | – |
| tACK | Setup time before –DMACK | 20 | – | 20 | – | 20 | – | 20 | – | | – |
| tENV | Envelope time | 20 | 70 | 20 | 70 | 20 | 70 | 20 | 55 | 20 | 55 |
| tZIORDY | Wait time before driving DSTROBE | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – |
| tFS | First strobe time | 0 | 230 | 0 | 200 | 0 | 170 | 0 | 130 | 0 | 120 |
| tCYC | Cycle time | 112 | – | 73 | – | 54 | – | 39 | – | 25 | – |
| t2CYC | 2 cycle time | 230 | – | 154 | – | 115 | – | 86 | – | 57 | – |
| tAZ | Output release time | – | 10 | – | 10 | – | 10 | – | 10 | – | 10 |
| tZAD | Output enable time | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – |
| tDVS | Data setup time (at device side) | 70 | – | 48 | – | 30 | – | 20 | – | 6 | – |
| tDVH | Data hold time (at device side) | 6 | – | 6 | – | 6 | – | 6 | – | 6 | – |

all values in ns

Figure 27. Ultra DMA cycle timings (Initiating Read)

### 7.2.4.2 Host Pausing Read DMA

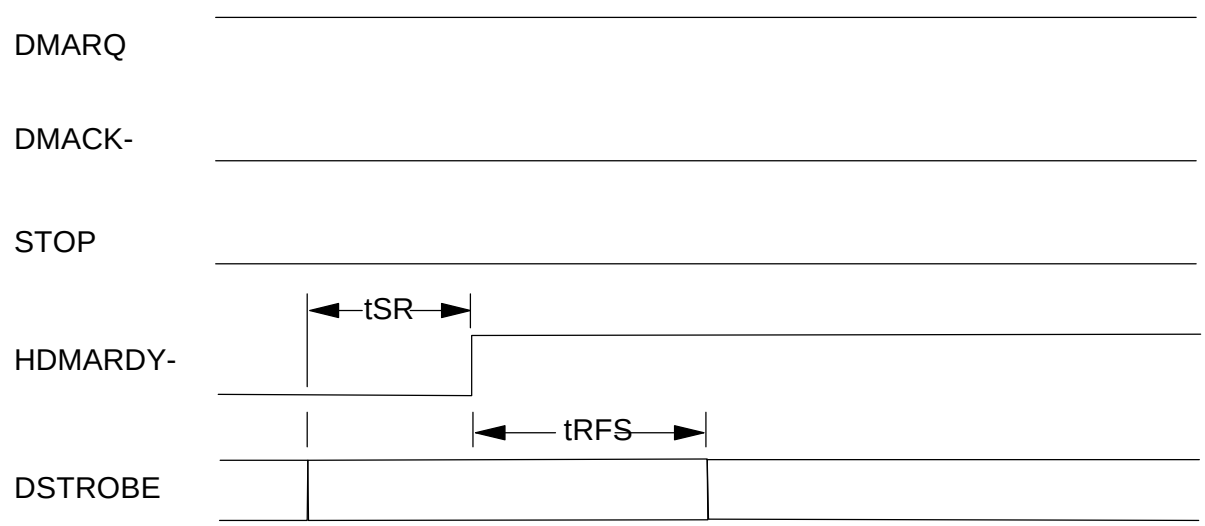



Figure 28. Ultra DMA cycle timing chart (Host pausing Read)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tSR | Strobe to ready response time | – | 50 | – | 30 | – | 20 | – | – | – | – |
| tRFS | Ready to final strobe time | – | 75 | – | 70 | – | 60 | – | 60 | – | 60 |
| all values in ns | | | | | | | | | | | |

*Note: When a host does not meet tSR, it should be ready to receive 2 (mode 0, 1 and 2) or 3 (mode 3 and 4) more strobes after HDMARDY– is negated.*

Figure 29. Ultra DMA cycle timings (Host pausing Read)

### 7.2.4.3 Host Terminating Read DMA

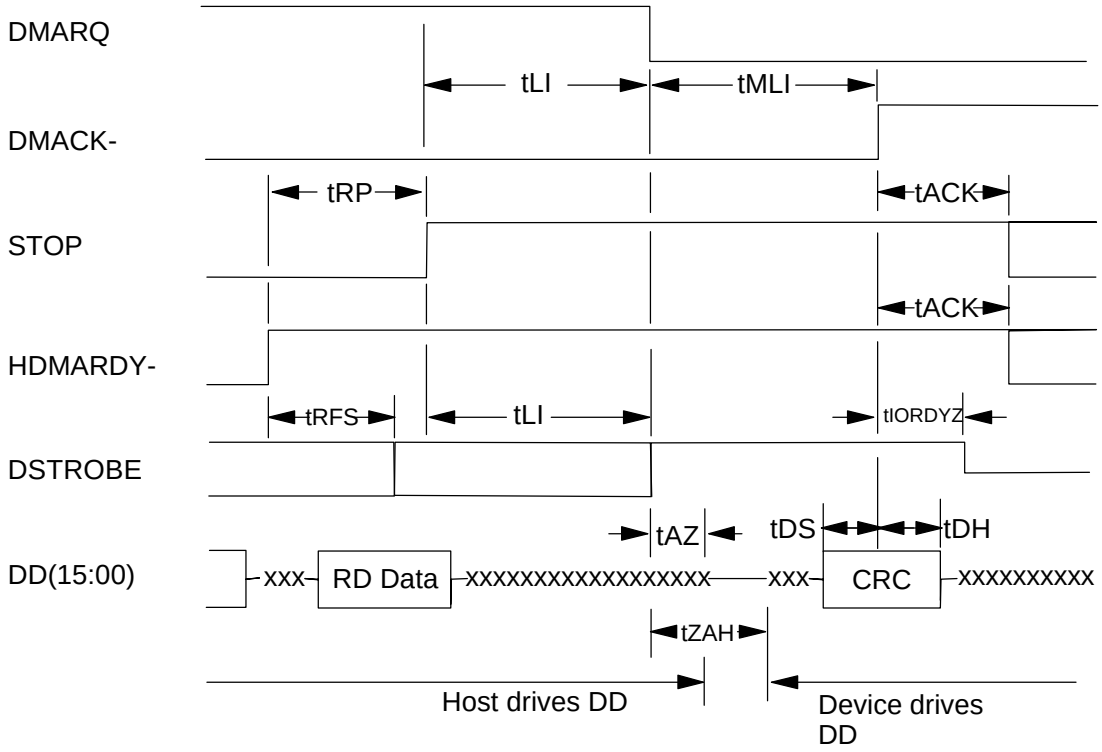



Figure 30. Ultra DMA cycle timing chart (Host terminating Read)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tRFS | Ready to final strobe time | – | 75 | – | 70 | – | 60 | – | 60 | – | 60 |
| tRP | Ready to pause time | 160 | – | 125 | – | 100 | – | 100 | – | 100 | – |
| tLI | Limited interlock time | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 |
| tAZ | Output release time | – | 10 | – | 10 | – | 10 | – | 10 | – | 10 |
| tZAH | Output enable time | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tMLI | Interlocking time | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tDS | Data setup time (at device side) | 15 | – | 10 | – | 7 | – | 7 | – | 5 | – |
| tDH | Data hold time (at device side) | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – |
| tACK | Hold time after –DMACK negation | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tIORDYZ | Pull-up time before DSTROBE release | – | 20 | – | 20 | – | 20 | – | 20 | – | 20 |

all values in ns

Figure 31. Ultra DMA cycle timings (Host terminating Read)

### 7.2.4.4 Device Terminating Read DMA

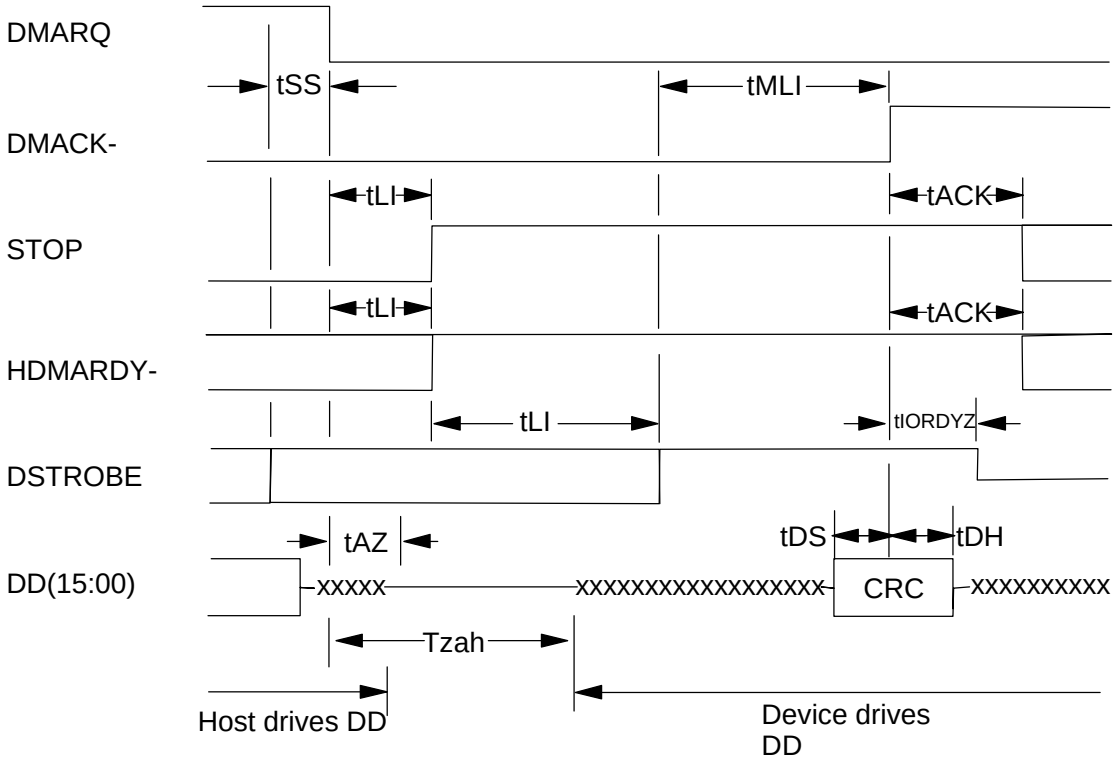



Figure 32. Ultra DMA cycle timing chart (Device terminating Read)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tSS | Time from strobe to stop assertion | 50 | – | 50 | – | 50 | – | 50 | – | 50 | – |
| tLI | Limited interlock time | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 |
| tAZ | Output release time | – | 10 | – | 10 | – | 10 | – | 10 | – | 10 |
| tZAH | Output enable time | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tMLI | Interlocking time | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tDS | Data setup time (at device side) | 15 | – | 10 | – | 7 | – | 7 | – | 5 | – |
| tDH | Data hold time (at device side) | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – |
| tACK | Hold time after –DMACK negation | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tIORDYZ | Pull-up time before DSTROBE release | – | 20 | – | 20 | – | 20 | – | 20 | – | 20 |
| all values in ns | | | | | | | | | | | |

Figure 33. Ultra DMA cycle timings (Device Terminating Read)

### 7.2.4.5 Initiating Write DMA

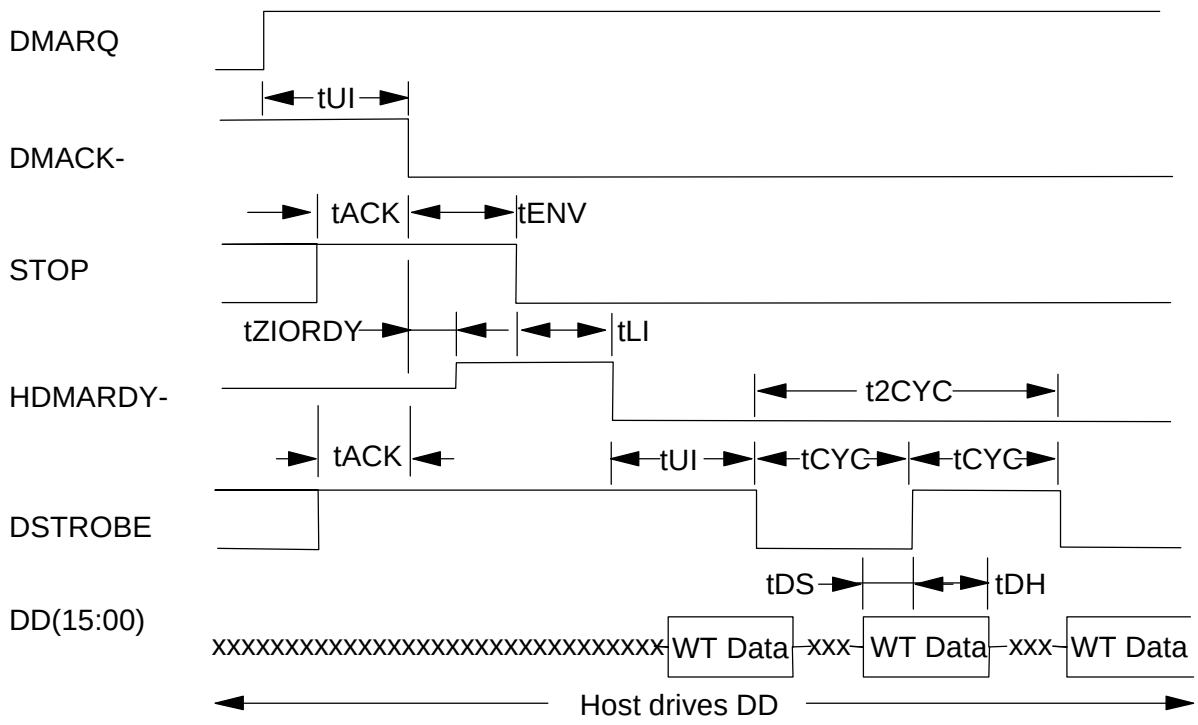



Figure 34. Ultra DMA cycle timing chart (Initiating Write)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tUI | Unlimited interlock time | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – |
| tACK | Setup time before –DMACK assertion | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tENV | Envelope time | 20 | 70 | 20 | 70 | 20 | 70 | 20 | 55 | 20 | 55 |
| tZIORDY | Wait time before driving DSTROBE | 0 | – | 0 | – | 0 | – | 0 | – | 0 | – |
| tLI | Limited interlock time | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 |
| tCYC | Cycle time | 112 | – | 73 | – | 54 | – | 39 | – | 25 | – |
| t2CYC | 2 Cycle time | 230 | – | 154 | – | 115 | – | 86 | – | 57 | – |
| tDS | Data setup time (at device side) | 15 | – | 10 | – | 7 | – | 7 | – | 5 | – |
| tDH | Data hold time (at device side) | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – |
| all values in ns | | | | | | | | | | | |

Figure 35. Ultra DMA cycle timings (Initiating Write)

### 7.2.4.6 Device Pausing Write DMA

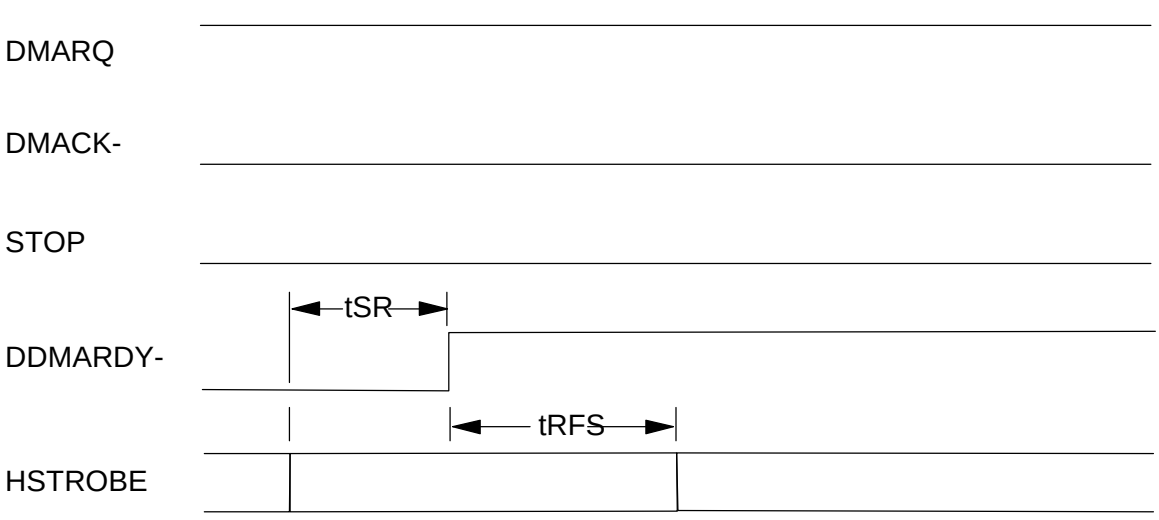



Figure 36. Ultra DMA cycle timing chart (Device Pausing Write)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tSR | Strobe to ready response time | – | 50 | – | 30 | – | 20 | – | – | – | - |
| tRFS | Ready to final strobe time | – | 75 | – | 70 | – | 60 | – | 60 | – | 60 |
| all values in ns | | | | | | | | | | | |

*Note*: *When a device does not meet tSR, it shall be ready to receive 3 more strobes after DDMARDY– is negated.*

Figure 37. Ultra DMA cycle timings (Device Pausing Write)

### 7.2.4.7 Device Terminating Write DMA

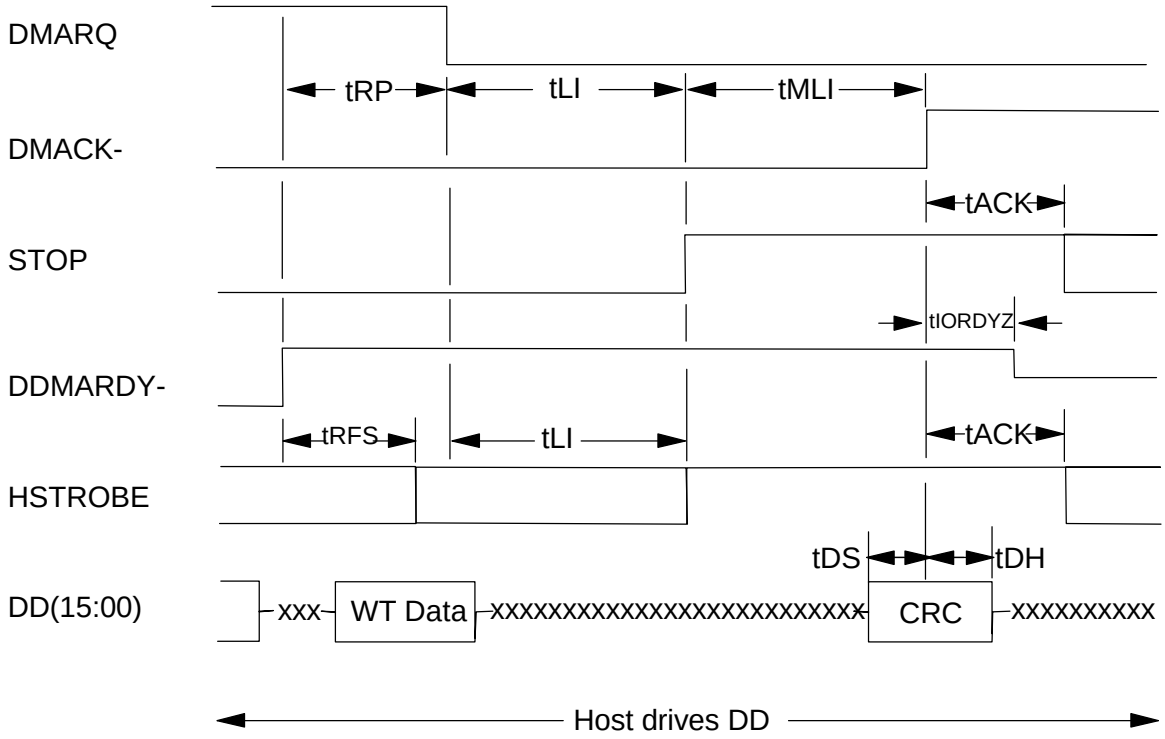



Figure 38. Ultra DMA cycle timing chart (Device Terminating Write)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tRFS | Ready to final strobe time | – | 75 | – | 70 | – | 60 | – | 60 | – | 60 |
| tRP | Ready to pause time | 160 | – | 125 | – | 100 | – | 100 | – | 100 | – |
| tLI | Limited interlock time | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 |
| tMLI | Interlocking time | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tDS | Data setup time (at device side) | 15 | – | 10 | – | 7 | – | 7 | – | 5 | – |
| tDH | Data hold time (at device side) | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – |
| tACK | Hold time after –DMACK negation | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tIORDYZ | Pull-up time before DSTROBE release | – | 20 | – | 20 | – | 20 | – | 20 | – | 20 |
| all values in ns | | | | | | | | | | | |

Figure 39. Ultra DMA cycle timings (Device terminating Write)

### 7.2.4.8 Host Terminating Write DMA

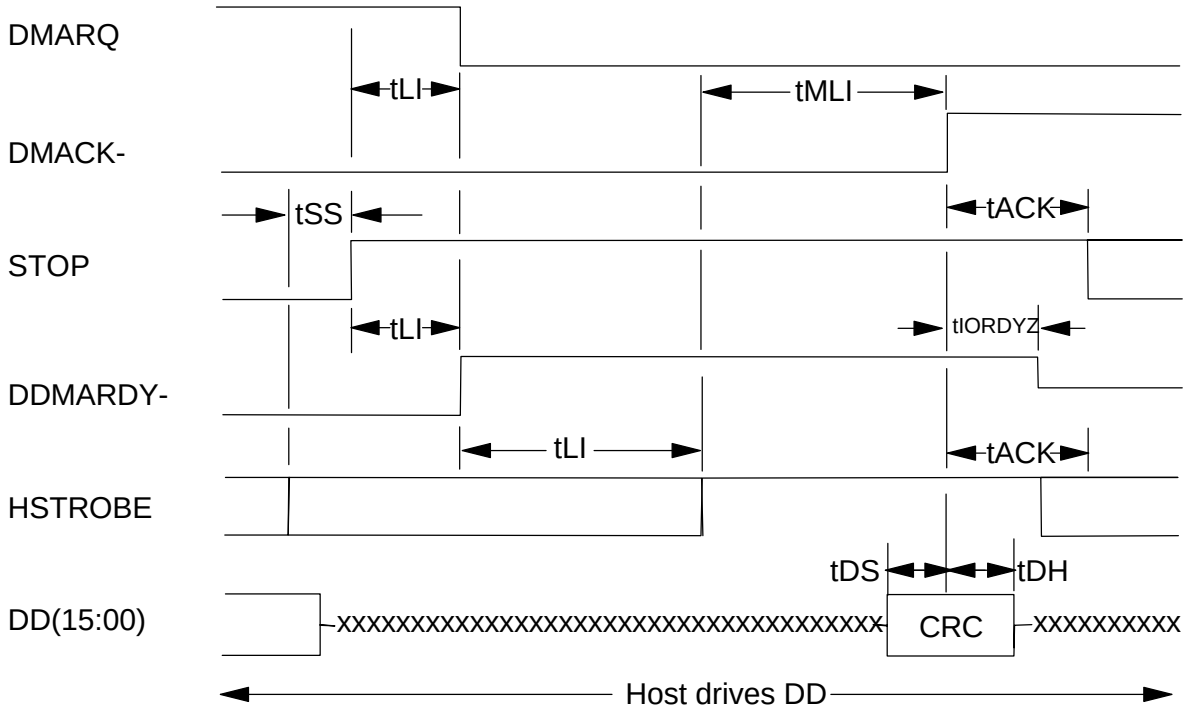



Figure 40. Ultra DMA cycle timing chart (Host Terminating Write)

| | PARAMETER DESCRIPTION | MODE0 | | MODE1 | | MODE2 | | MODE3 | | MODE4 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| tSS | Time from strobe to stop assertion | 50 | – | 50 | – | 50 | – | 50 | – | 50 | – |
| tLI | Limited interlock time | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 |
| tMLI | Interlock time | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tDS | Data setup time (at device side) | 15 | – | 10 | – | 7 | – | 7 | – | 5 | – |
| tDH | Data hold time (at device side) | 5 | – | 5 | – | 5 | – | 5 | – | 5 | – |
| tACK | Hold time after –DMACK negation | 20 | – | 20 | – | 20 | – | 20 | – | 20 | – |
| tIORDYZ | Pull-up time before DSTROBE release | – | 20 | – | 20 | – | 20 | – | 20 | – | 20 |
| all values in ns | | | | | | | | | | | |

Figure 41. Ultra DMA cycle timings (Host Terminating Write)

## 7.2.5 Addressing of registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the I/ O space of the host. Two chip select lines (CS0– and CS1–) and three address lines (DA0-02) are used to select one of these registers, while a DIOR– or DIOW– is provided at the specified time.

The CS0– is used to address Command Block registers. while the CS1– is used to address Control Block registers. The following table shows the I/ O address map.

| CS0– | CS1– | DA2 | DA1 | DA0 | DIOR– = 0 (Read) | DIOW– = 0 (Write) |
|---|---|---|---|---|---|---|
| | | | | | Command Block Registers | |
| 0 | 1 | 0 | 0 | 0 | Data Reg. | Data Reg. |
| 0 | 1 | 0 | 0 | 1 | Error Reg. | Features Reg. |
| 0 | 1 | 0 | 1 | 0 | Sector count Reg. | Sector count Reg. |
| 0 | 1 | 0 | 1 | 1 | Sector number Reg. | Sector number Reg. |
| 0 | 1 | 1 | 0 | 0 | Cylinder low Reg. | Cylinder low Reg. |
| 0 | 1 | 1 | 0 | 1 | Cylinder high Reg. | Cylinder high Reg. |
| 0 | 1 | 1 | 1 | 0 | Drive/Head Reg. | Drive/Head Reg. |
| 0 | 1 | 1 | 1 | 1 | Status Reg. | Command Reg. |
| | | | | | Control Block Registers | |
| 1 | 0 | 1 | 1 | 0 | Alt. Status Reg. | Device control Reg. |
| 1 | 0 | 1 | 1 | 1 | Drive address Reg. | – |

Figure 42. I/O address map

During DMA operation (from writing to the command register until an interrupt) all registers are not accessible.

For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

## 7.2.6 Cabling

The maximum cable length from the host system to the drive plus circuit pattern length in the host system shall not exceed 18 inches.

For higher data transfer application (>8.3MB/sec) a modification in the system design is recommended to reduce cable noise and/or cross-talk, such as a shorter cable, bus termination, or a shielded cable.

For systems operating with Ultra DMA mode 3 or 4, 80-conductor ATA cable assembly (SFF-8049) shall be used.

# 7.3 Jumper settings

## 7.3.1 Jumper pin assignment

There are four jumper settings as shown in the following sections: 16 logical heads (normal use), 15 logical heads, 2GB clip, and auto spin disable. Each category is exclusive. The pin assignment of the 9-pin jumper used to select "Device 0" or "Device 1", "Cable Selection" and "Device 0 Forcing Device 1 Present" is shown below.

The Device 0 setting automatically recognizes device 1 if present.

The Device 0 Forcing Device 1 present setting is for a slave device that does not comply with the ATA specification.

*Note: In conventional terminology 'Device0' means 'Master' and 'Device1' means 'Slave.'*

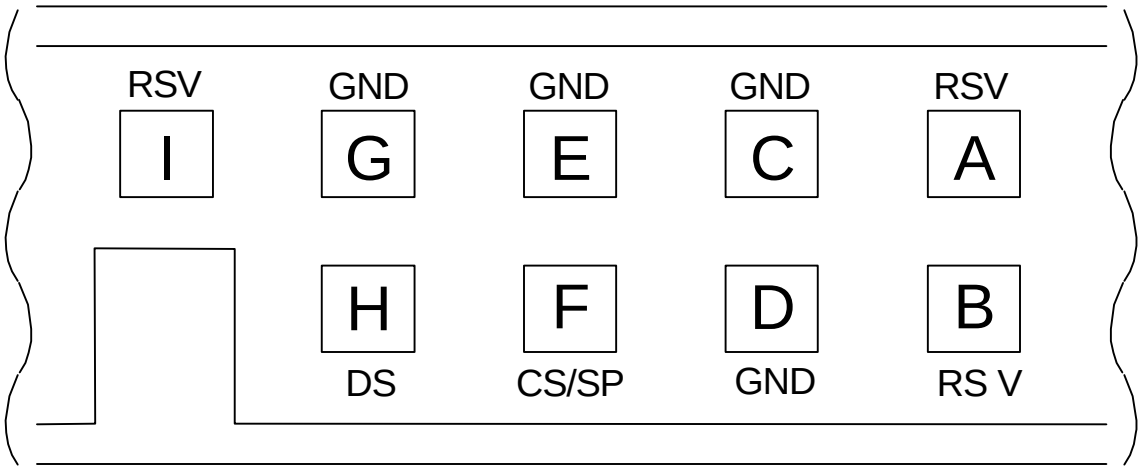



Figure 43. Jumper pin assignment

## 7.3.2 Jumper positions

### 7.3.2.1 16 logical head default (normal use)

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device 0 Forcing Device 1 Present.

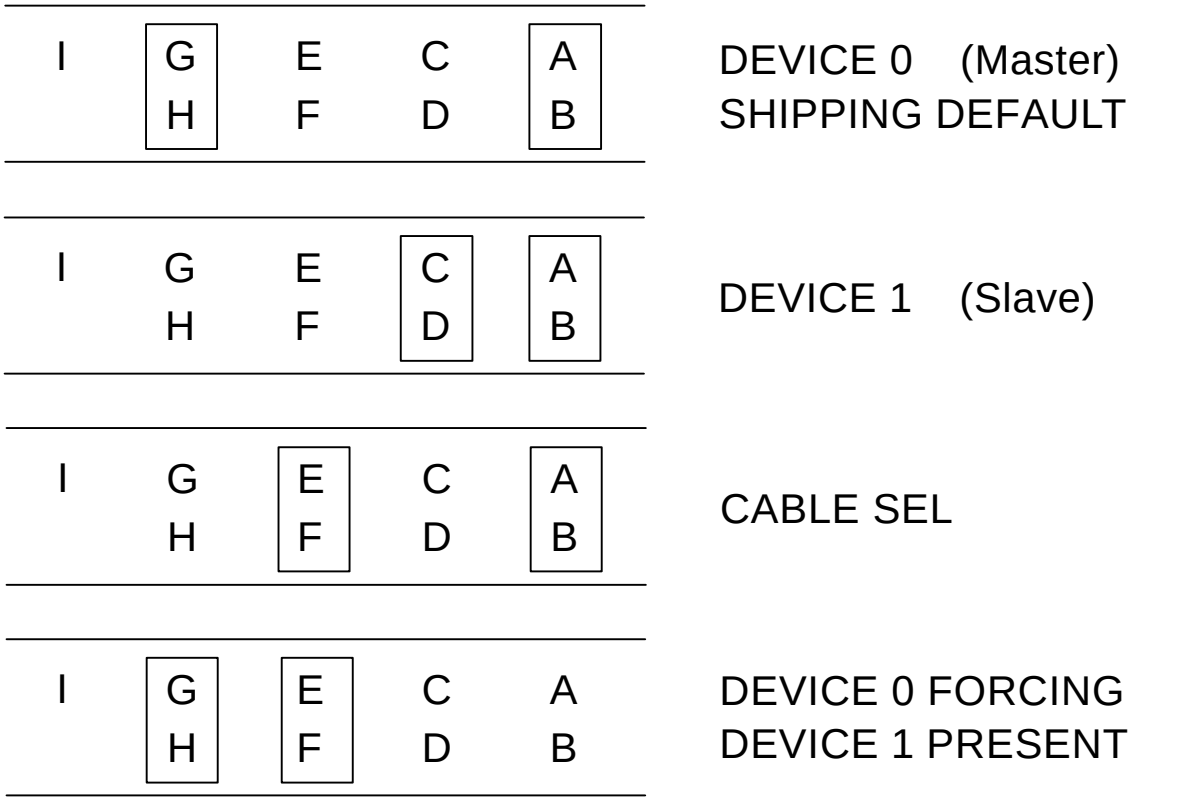



Figure 44. Jumperpositions for normal use

***Notes:***

1. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode, the drive address is determined by AT interface signal #28 CSEL as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device1).*
2. *In CSEL mode, installing or removing the jumper blocks at A-B or C-D position does not affect any selection of Device or Cable Selection mode.*
3. *Shipping default positions of the jumpers are at A-B and G-H which is the condition of Device 0.*

### 7.3.2.2 15 logical head default

The positions of jumper blocks shown below is used to select Device 0, Device 1, Cable Selection, or Device 0 Forcing Device 1 Present, setting 15 logical heads instead of default 16 logical head models.

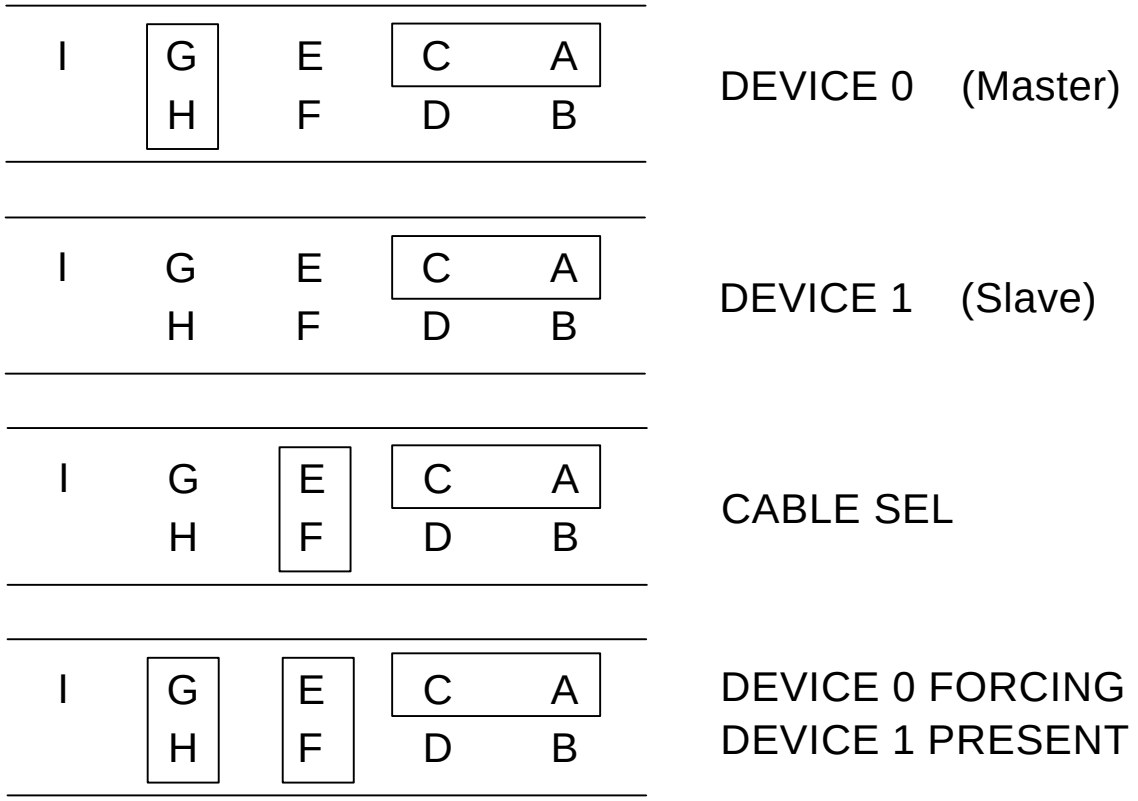



Figure 45. Jumper positions for 15 logical head default

***Notes:***

1. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode, the drive address is determined by AT interface signal #28 CSEL as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device1).*
2. *In CSEL mode, installing or removing the jumper blocks at A-C or B-D position does not affect any selection of Device or Cable Selection mode.*

### 7.3.2.3 Capacity clip to 2GB/32GB with 16 default logical heads

The positions of the jumper blocks shown below are used to select Device 0, Device 1, Cable Selection, or Device 0 Forcing Device 1 Present, setting the drive capacity down either to 2GB or 32GB for the purpose of compatibility.

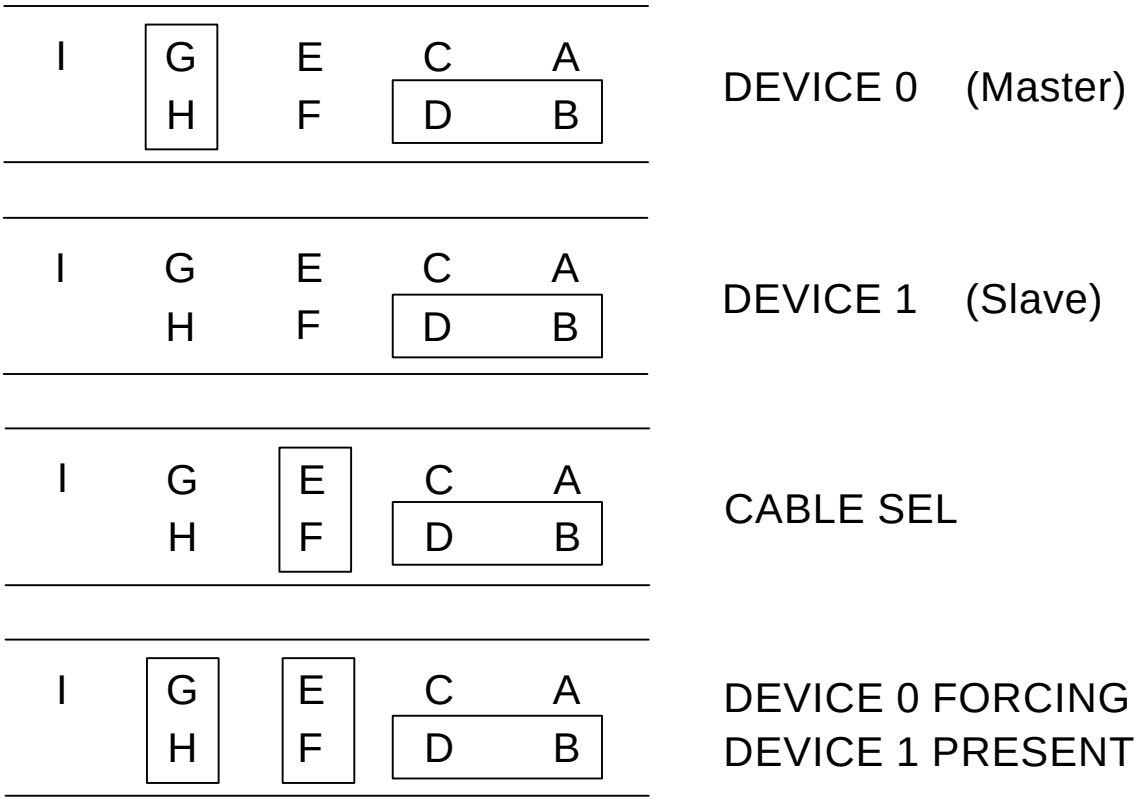



Figure 46. Jumper positions for capacity clip to 2GB/32GB with 16 default logical heads

The above jumper setting forces the values of Word 1,3,6 and 60-61 in Identify Device data as follows:

DTLA-305040/307045/307060/307075

- Word 1/3/6 (C/H/S): Remain ship default value
- Word 60-61 (LBA): 66055248

DTLA-305010/305020/305030/307015/307020/307030

- Word 1/3/6 (C/H/S): 4096/16/63
- Word 60-61 (LBA): Remain ship default value

***Notes:***

1. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode, the drive address is determined by AT interface signal #28 CSEL as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device1).*

### 7.3.2.4 Power up in standby

The jumpers are installed as shown below for enabling power up in standby.

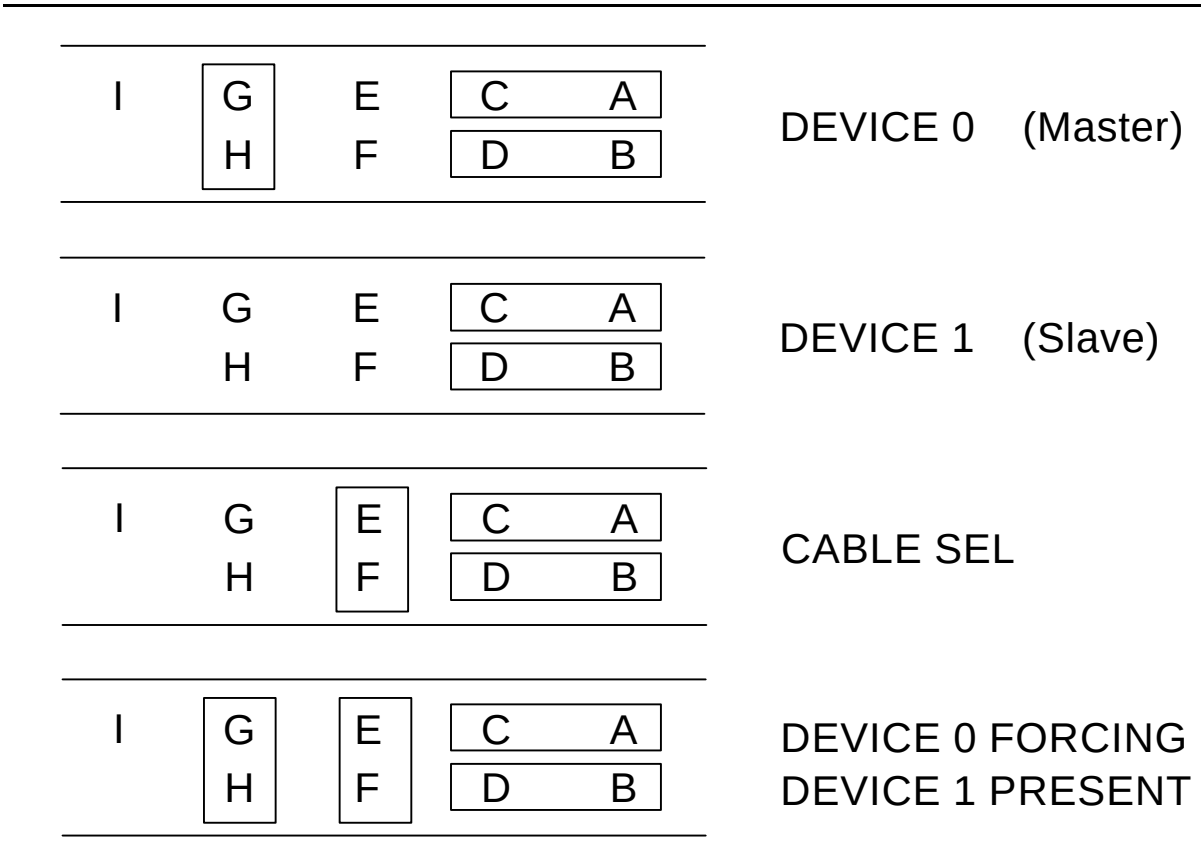



Figure 47. Jumper settings for Disabling Auto Spin

***Notes:***

1. *These jumper settings are used for limiting power supply current when multiple drives are used.*
2. *Command to spin up is SET FEATURES (subcommand 07h). Refer to 12.28 Set Features.*
3. *To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In CSEL mode, the drive address is determined by AT interface signal #28 as follows:*
   - *When CSEL is grounded or at a low level, the drive address is 0 (Device0).*
   - *When CSEL is open or at a high level, the drive address is 1 (Device1).*

# 7.4 Environment

## 7.4.1 Temperature and humidity

| **Operating conditions** | |
|---|---|
| Temperature | 5 to 55°C |
| Relative humidity | 8 to 90% non-condensing |
| Maximum wet bulb temperature | 29.4°C non-condensing |
| Maximum temperature gradient | 15°C/Hour |
| Altitude | -300 to 3,048 m |
| **Nonoperating conditions** | |
| Temperature | -40 to 65°C |
| Relative humidity | 5 to 95% non-condensing |
| Maximum wet bulb temperature | 35°C non-condensing |
| Maximum temperature gradient | 35°C/Hour |
| Altitude | -300 to 12,000 m |

Figure 48. Operating and nonoperating conditions

***Notes:***

1. *The system has to provide sufficient ventilation to maintain a surface temperature below 60°C at the center of the drive top cover.*
2. *Noncondensing conditions should be maintained at any time.*
3. *Maximum storage period with shipping package is one year.*

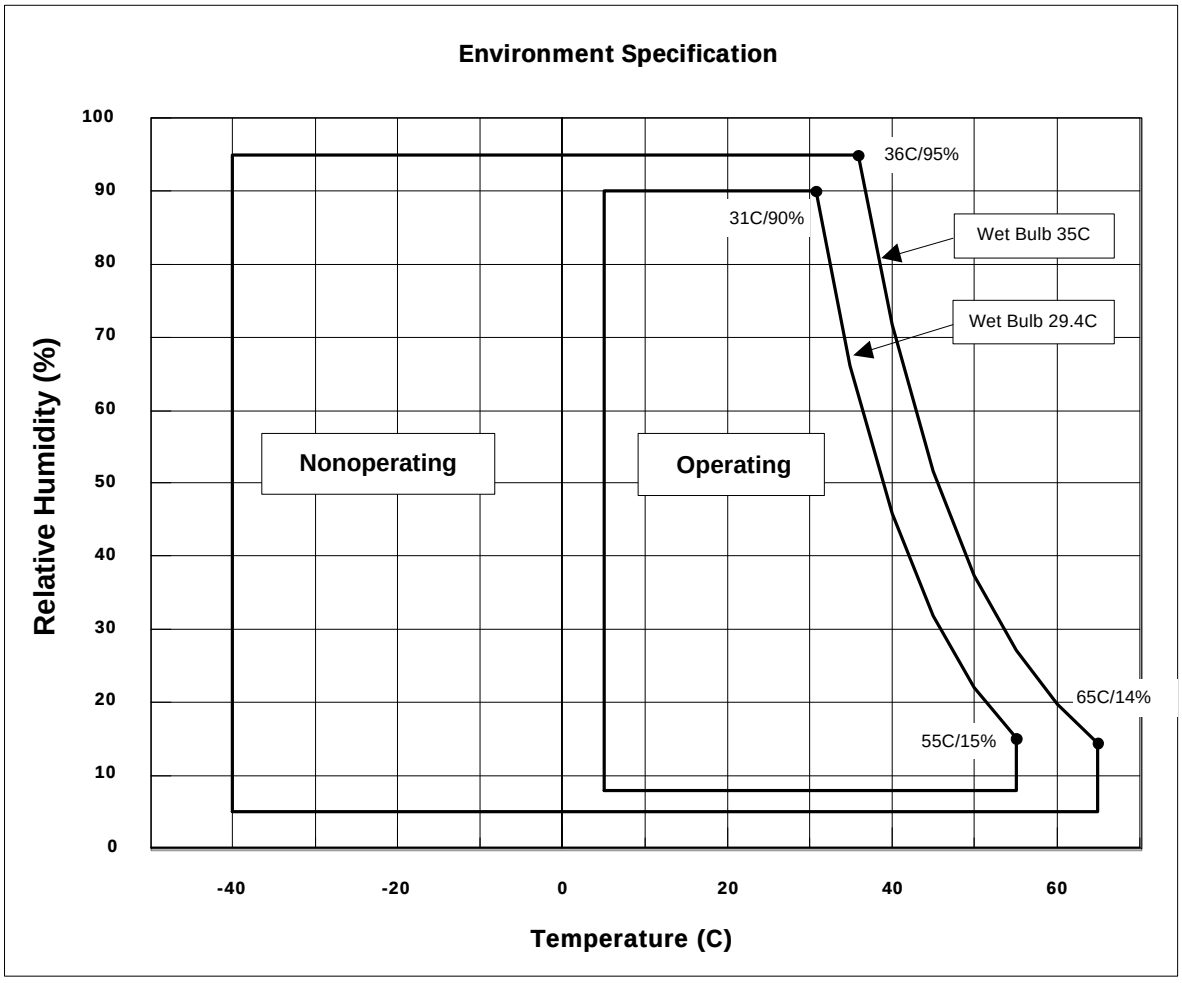



Figure 49. Limits of temperature and humidity

# 7.5 DC power requirements

The following voltage specifications apply at the drive power connector. Damage to the drive electronics may result if the power supply cable is connected or disconnected while power is being applied to the drive (no hot plug/unplug is allowed). Connections to the drive should be made in a low voltage, isolated secondary circuit(SELV). There is no special power on/off sequencing required.

## 7.5.1 Input voltage

| Input voltage | During run and spin up | Absolute max spike voltage[1] |
|---|---|---|
| +5 Volts Supply | 5V ± 5% | 7V |
| +12 Volts Supply | 12V +10% –8% | 15V |

Figure 50. Input voltage

*Note: To avoid damage to the drive electronics power supply voltage spikes must not exceed specifications.*

## 7.5.2 Power supply current (typical)

**DTLA-305020, -305030, -305040**

| | **+5 Volts** (amps RMS) | **+12 Volts** (amps RMS) | **Total** (watts) |
|---|---|---|---|
| Idle Average | 0.26 | 0.30 | 4.9 |
| Idle ripple (peak-to-peak) | 0.29 | 0.43 | -- |
| Seek peak | 0.44 | 1.91 | -- |
| Seek average[1] | 0.27 | 0.54 | 7.9 |
| Start up (max) | 0.98 | 1.86 | -- |
| Random R/W peak | 0.94 | 1.91 | -- |
| Random R/W average[2] | 0.41 | 0.54 | 8.6 |
| Standby average | 0.27 | 0.017 | 1.6 |
| Sleep average | 0.18 | 0.017 | 1.1 |

Except for a peak of less than 100usc duration

[1] Randon seeks at 40% duty cycle

[2] Seek duty = 30%, W/R duty = 45%, Idle Duty = 25%

Figure 51. Power supply current (1 0f 2)

**DTLA-307015, -307020, -307030, -307045**

| | **+5 Volts** (amps RMS) | **+12 Volts** (amps RMS) | **Total** (watts) |
|---|---|---|---|
| Idle Average | 0.24 | 0.46 | 6.7 |
| Idle ripple (peak-to-peak) | 0.33 | 0.41 | --- |
| Seek peak | 0.46 | 2.04 | --- |
| Seek average[1] | 0.26 | 0.73 | 10.1 |
| Start up (max) | 0.81 | 1.90 | --- |
| Random R/W peak | 1.01 | 2.04 | --- |
| Random R/W average[2] | 0.41 | 0.70 | 10.5 |
| Standby average | 0.26 | 0.015 | 1.5 |
| Sleep average | 0.17 | 0.015 | 1.0 |

**DTLA-307060, -307075**

| | **+5 Volts** (amps RMS) | **+12 Volts** (amps RMS) | **Total** (watts) |
|---|---|---|---|
| Idle Average | 0.24 | 0.57 | 8.1 |
| Idle ripple (peak-to-peak) | 0.32 | 0.63 | --- |
| Seek peak | 0.47 | 2.23 | --- |
| Seek average[1] | 0.27 | 0.84 | 11.4 |
| Start up (max) | 0.81 | 1.81 | --- |
| Random R/W peak | 1.02 | 2.23 | --- |
| Random R/W average[2] | 0.41 | 0.78 | 11.5 |
| Standby average | 0.26 | 0.015 | 1.5 |
| Sleep average | 0.17 | 0.015 | 1.0 |

Except for a peak of less than 100us duration

[1] Randon seeks at 40% duty cycle

[2] Seek duty = 30%, W/R duty = 45%, Idle Duty = 25%

Figure 51. Power supply current (2 of 2)

The Total (watts) values in figures above are specifications of power requirements and other values are actual measurements.

## 7.5.3 Power supply generated ripple at drive power connector

| | **Maximum** (mV pp) | **MHz** |
|---|---|---|
| +5V DC | 250 | 0-10 |
| +12V DC | 250 | 0-10 |

Figure 52. Power supply generated ripple at drive power connector

During drive start up and seeking 12-volt ripple is generated by the drive (referred to as dynamic loading). If the power of several drives is daisy chained together, the power supply ripple plus the dynamic loading of the other drives must remain within the above regulation tolerance. A common supply with separate power leads to each drive is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the performance of the drive, the drive must be held by four screws in a user system frame which has no electrical level difference at the four screws position and has less than ±300 millivolts peak to peak level difference to the ground of the drive power connector.

## 7.5.4 Start Up Current

### 7.5.4.1 DTLA-305010/305020/305030/305040

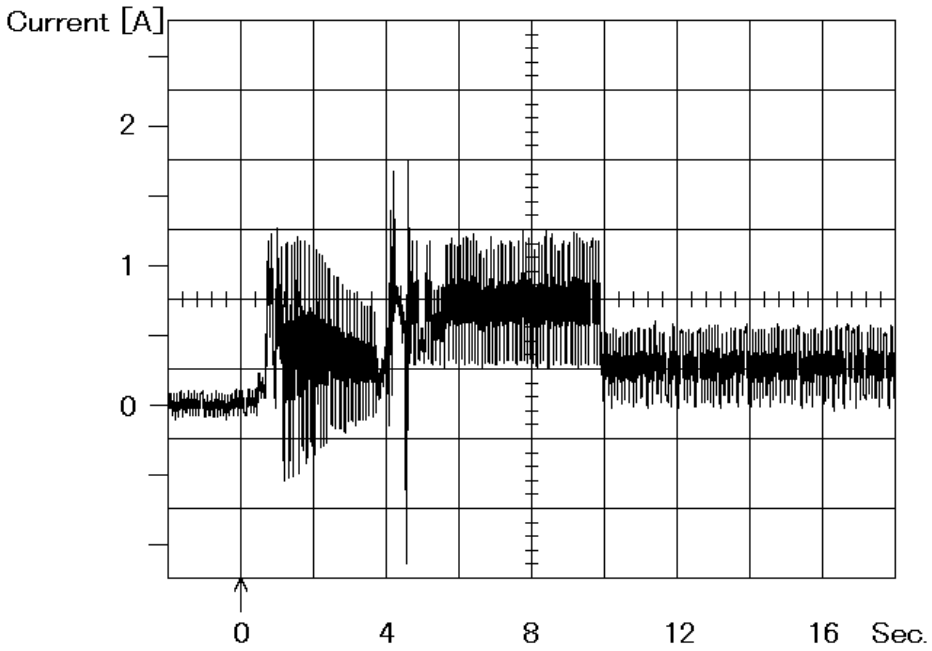



Figure 53. Typical Current Form of 12V at Start Up of DTLA-305010/305020/305030/305040

### 7.5.4.2 DTLA-307015/307020/307030/307045

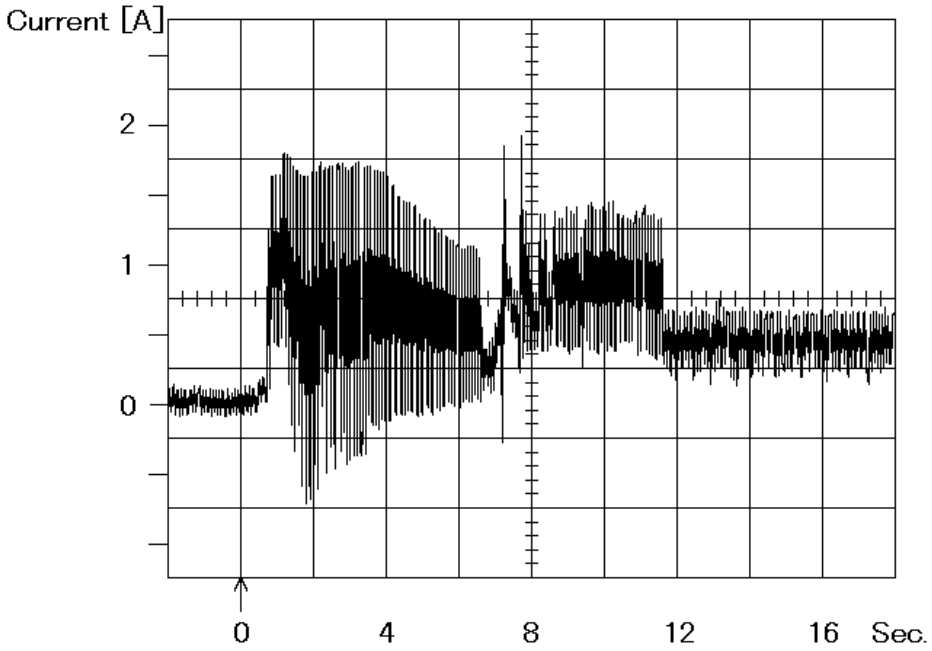



Figure 54. Typical Current Form of 12V at Start Up of DTLA-307015/307020/307030/307045

### 7.5.4.3 DTLA-307060/307075

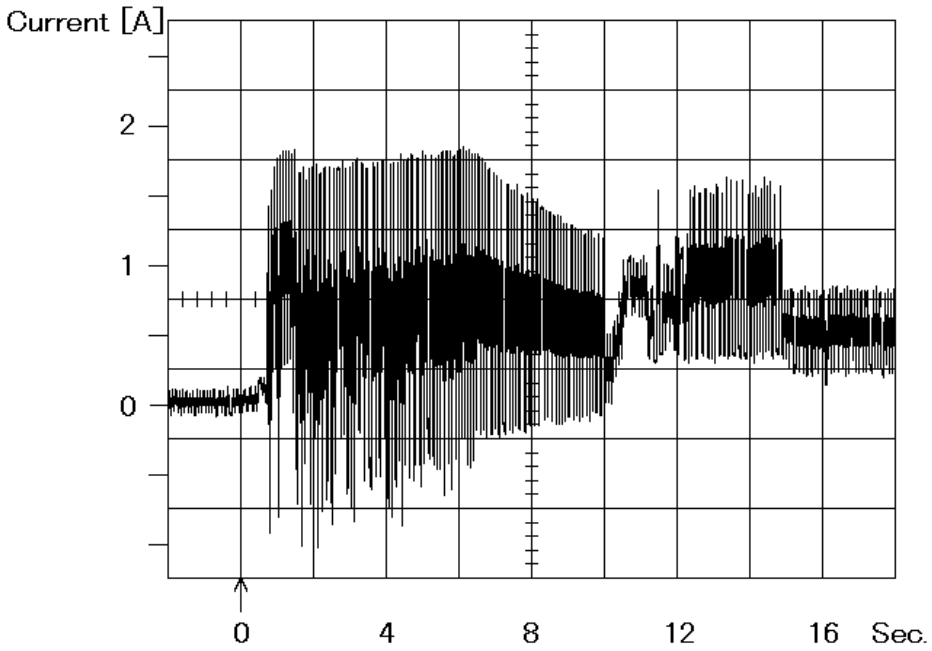



Figure 55. Typical Current Form of 12V at Start Up of DTLA-307060/307075

## 7.5.5 Energy consumption efficiency

| DTLA- | Energy consumption efficiency (W/GB) |
|---|---|
| 305020 | 0.24 |
| 305030 | 0.16 |
| 305040 | 0.12 |
| 307015 | 0.43 |
| 307020 | 0.33 |
| 307030 | 0.22 |
| 307045 | 0.15 |
| 307060 | 0.13 |
| 307075 | 0.11 |

Figure 56. Energy consumption efficiency

Energy consumption efficiency is calculated as

Power consumption of Idle Average (Watt)/Capacity(GB)

# 7.6 Reliability

## 7.6.1 Cable noise interference

To avoid any degradation of performance throughput or error rate when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

## 7.6.2 Start/stop cycles

The drive withstands a minimum of 40,000 start/stop cycles in a 40° C environment and a minimum of 10,000 start/stop cycles in extreme temperature or humidity or complete stop disk rotation. See Figure 48 on page 46 and Figure 49 on page 47.

## 7.6.3 Preventive maintenance

None

## 7.6.4 Data reliability

- Probability of not recovering data: 1 in $10^{13}$ bits read
- ECC On The Fly correction
  - 1 Symbol : 8 bits
  - 3 Interleave
  - 12 ECCs are embedded into each interleave
  - 15 Symbols, 5 Symbols per each interleave, for On The Fly correction
  - This implementation always recovers 5 random burst errors and a 113 bit continuous burst error

.

## 7.7 Mechanical specifications

### 7.7.1 Outline

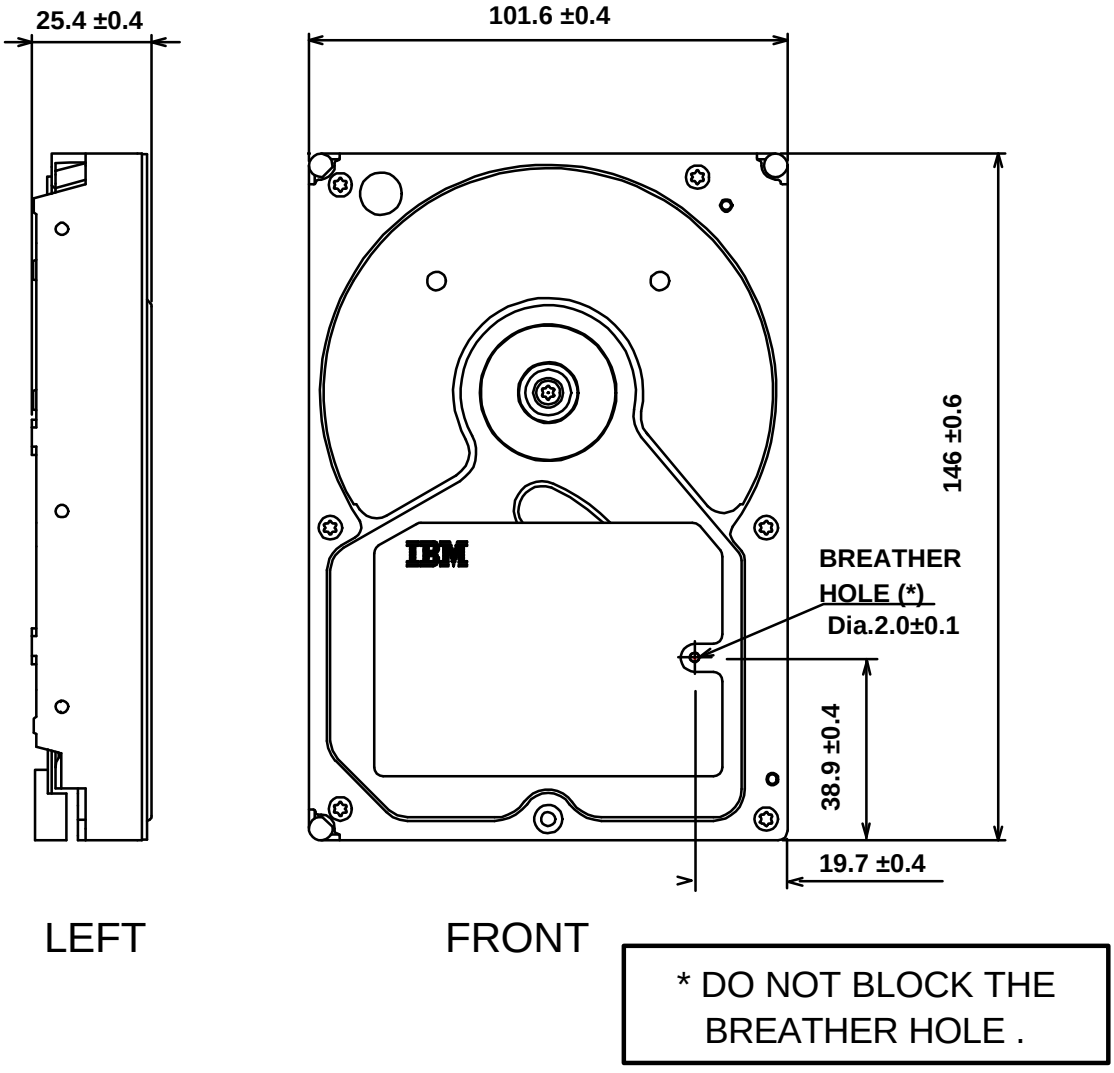



Figure 57. Outline of the DTLA-3xxxxx

## 7.7.2 Physical dimensions

The following chart describes the dimensions for IBM DTLA-307xxx hard disk drive form factor.

| DTLA- | Height (mm) | Width (mm) | Length (mm) | Weight (grams) |
|---|---|---|---|---|
| 305010<br>305020<br>305030<br>305040 | 25.4 ± 0.4 | 101.6 ± 0.4 | 146.0 ± 0.8 | 550 |
| 307015<br>307020<br>307030<br>307045 | | | | 590 |
| 307060<br>307075 | | | | 670 |

Figure 58. Physical Dimensions

## 7.7.3 Hole locations

The figure below shows the outline of the drive including the hole locations.

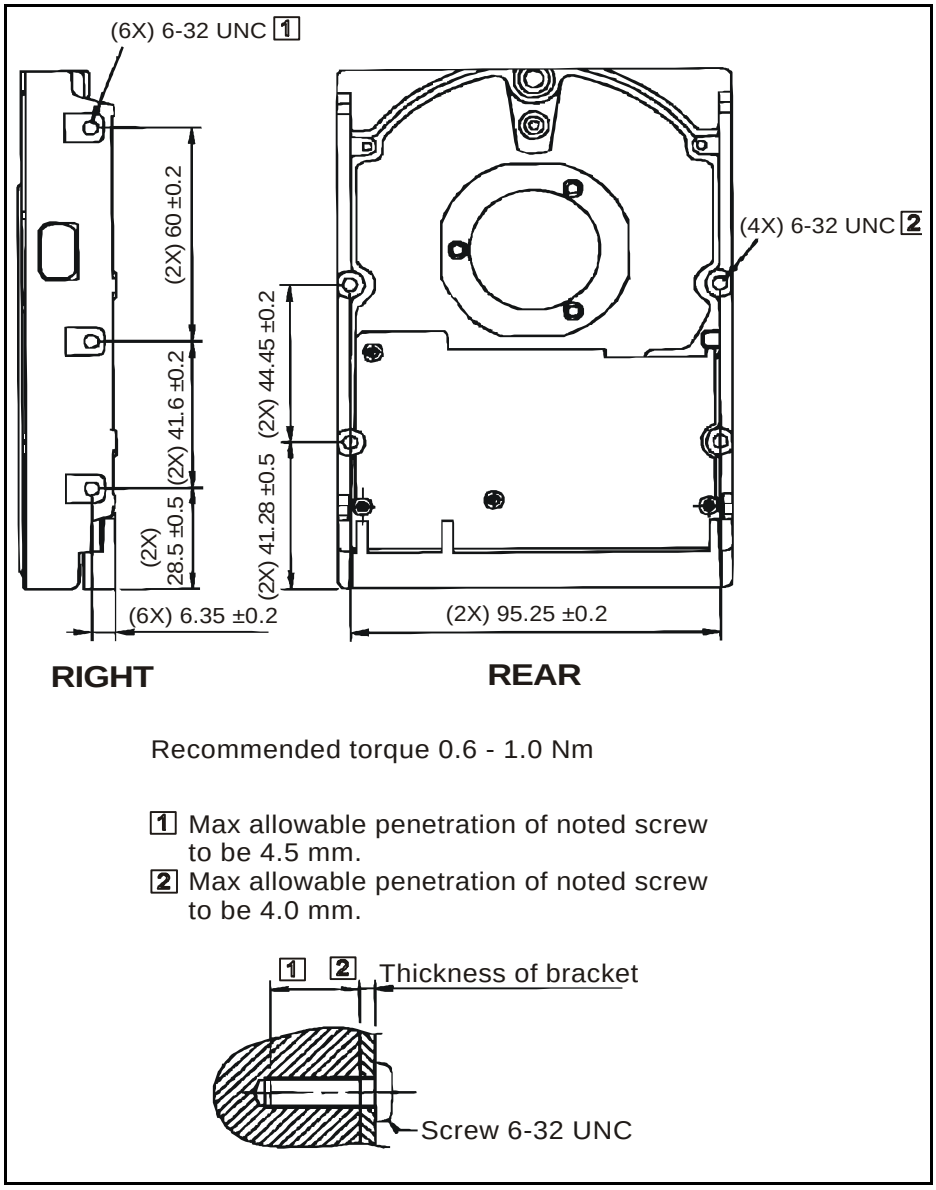



Figure 59. Mounting hole locations

## 7.7.4 Connector locations

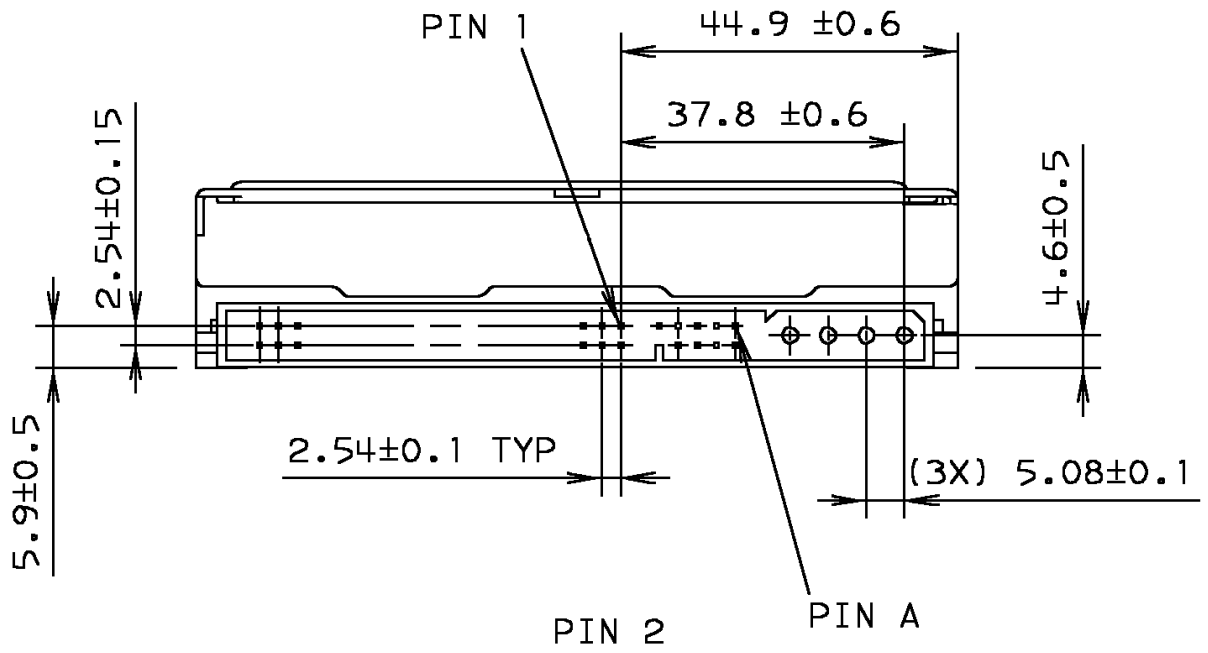



Figure 60. Connector locations

## 7.7.5 Drive mounting

The drive will operate in all axes (6 directions). Performance and error rate will stay within specification limits if the drive is operated in the other orientations from which it was formatted.

For reliable operation, the drive must be mounted in the system securely enough to prevent excessive motion or vibration of the drive during seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

The recommended mounting screw torque is 0.6 - 1.0 [Nm] (6-10 [Kgf.cm]).

The recommended mounting screw depth is 4 [mm] maximum for bottom and 4.5 [mm] maximum for horizontal mounting.

If an electrical screw driver is used for moutning screws, a current control model should be used.

Drive level vibration test and shock test are to be conducted with the drive mounted to the table using the bottom four screws.

## 7.7.6 Heads unload and actuator lock

Heads are moved out from disks (unload) to protect the disk data during shipping, moving or storage. Upon power down, the heads are automatically unloaded from disk area and head actuator locking mechanism will secure the heads in unload position..

# 7.8 Vibration and shock

All vibration and shock measurements recorded in this section are made with a drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

## 7.8.1 Operating vibration

### 7.8.1.1 Random vibration

The drive is designed to operate without unrecoverable errors while being subjected to the following vibration levels. The test consists of 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes.

| Direction | 5 Hz | 17 Hz | 45 Hz | 48 Hz | 62 Hz | 65 Hz | 150 Hz | 200 Hz | 500 Hz | RMS (G) |
|---|---|---|---|---|---|---|---|---|---|---|
| Horizontal $x10^{-3}$ $[G^2/Hz]$ | 0.02 | 1.1 | 1.1 | 8.0 | 8.0 | 1.0 | 1.0 | 0.5 | 0.5 | 0.67 |
| Vertical $x10^{-3}$ $[G^2/Hz]$ | 0.02 | 1.1 | 1.1 | 8.0 | 8.0 | 1.0 | 1.0 | 0.08 | 0.08 | 0.56 |

Figure 61. Random vibration PSD profile break points (operating)

The overall RMS (root mean square) level is 0.67G for horizontal vibration and 0.56G for vertical.

### 7.8.1.2 Swept sine vibration

The hard disk drive will meet the criteria shown below while operating in the specified conditions:

- No errors occur with 0.5 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3 minute dwells at 2 major resonances
- No data loss occurs with 1 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3 minute dwells at 2 major resonances

## 7.8.2 Nonoperating vibration

The drive does not sustain permanent damage or loss of previously recorded data after being subjected to the environment described below.

#### 7.8.2.1 Random vibration

The test consists of a random vibration applied for each of three mutually perpendicular axes with the time duration of 10 minutes per axis. The PSD levels for the test simulate the shipping and relocation environment shown below.

The overall RMS (Root Mean Square) level of vibration is 1.04G.

| Frequency | 2 Hz | 4 Hz | 8 Hz | 40 Hz | 55 Hz | 70 Hz | 200 Hz |
|---|---|---|---|---|---|---|---|
| G2/Hz | 0.001 | 0.03 | 0.03 | 0.003 | 0.01 | 0.01 | 0.001 |

Figure 62. Random vibration PSD profile break points (nonoperating)

#### 7.8.2.2 Swept sine vibration

- 2 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

### 7.8.3 Operating shock

The drive meets the following criteria.

- No error loss occurs with 10G/11 ms half-sine shock pulse
- No data loss occurs with 30G/4 ms half-sine shock pulse
- No data loss occurs with 55G/2 ms half-sine shock pulse

The shock test consists of ten shock inputs in each axis and direction for a total of 60. There must be a minimum of 30 seconds delay between shock pulses. The input level is applied to a base plate where the drive is attached with four screws.

### 7.8.4 Nonoperating shock

The drive will operate with no degradation of performance after being subjected to shock pulses with the following characteristics.

#### 7.8.4.1 Trapezoidal shock wave

- Approximate square (trapezoidal) pulse shape
- Approximate rise and fall time of pulse = 1 ms
- Average acceleration level = 50G. (Average response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 ms")
- Minimum velocity change = 4.23 meters/second

#### 7.8.4.2 Sinusoidal shock wave

- Approximate half-sine pulse shape
- Maximum acceleration level and duration:

| | |
|---|---|
| 400G, 2 ms | DTLA-305XXX |
| 350G, 2 ms | DTLA-307015, -307020, -307030, -307045 |
| 225G, 2 ms | DTLA-307060, -307075 |

### 7.8.5 Rotational shock

All shock inputs shall be applied around the actuator pivot axis.

| | |
|---|---|
| 1 ms duration | 30,000 rad/sec$^2$ |
| 2 ms duration | 20,000 rad/sec$^2$ |

## 7.9 Acoustics

The upper limit criteria of the octave sound power levels are given in Bels relative to one pico watt and are shown in the following table. The sound power emission levels are measured in accordance with ISO 7779.

| Mode | DTLA-305010/305020 /305030/305040 | | DTLA-307015/307020 /307030/307045 | | DTLA-307060/307075 | |
|---|---|---|---|---|---|---|
| | Typical | Max | Typical | Max | Typical | Max |
| Idle | 3.0 | 3.4 | 3.1 | 3.4 | 3.6 | 3.9 |
| Operating | 3.7 | 4.0 | 3.4 | 3.7 | 4.5 | 4.8 |

Figure 63. Sound power levels

**Mode definition:**

**Idle mode.** The drive is powered on, disks spinning, track following, unit ready to receive and respond to interface commands.

**Operating mode.** Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. The seek rate for the drive is to be calculated as listed below:

Ns = 0.4/(Tt + TI)

Ns = average seek rate in seeks/sec

Tt = published random seek rate

TI = time for the drive to rotate by half a revolution

## 7.10 Identification labels

The following labels are affixed to every drive shipped from the drive manufacturing location in accordance with the appropriate hard disk drive assembly drawing:

- A label containing the IBM logo, the IBM part number, and the statement “Made by IBM Japan Ltd.”, or IBM approved equivalent.
- A label containing the drive model number, the manufacturing date code, the formatted capacity, the place of manufacture, UL/CSA/TUV/CE/C-Tick mark logos.
- A bar code label containing the drive serial number.
- A label containing the Jumper pin description.
- A user designed label, per agreement.

The above labels may be integrated with other labels.

# 7.11 Safety

## 7.11.1 UL and CSA standard conformity

The product is qualified per UL 1950 Third Edition and CAN/CSA C22.2 No. 950-M95, Third Edition, for use in Information Technology Equipment including Electric Business Equipment.

The UL recognition or the CSA certification is maintained for the product life.

The UL and C-UL recognition mark or the CSA monogram for CSA certification appear on the drive.

## 7.11.2 IEC compliance

The product is certified for compliance to IEC 950. The product complies with these IEC requirements for the life of the product.

## 7.11.3 German Safety Mark

The product is approved by TUV on Test requirement: EN 60 950:1992/A1-4.

## 7.11.4 Flammability

The printed circuit boards used in this product are made of material with the UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with the UL recognized flammability rating of V-1 or better. However, small mechanical parts such as cable ties, washers, screws, and PC board mounts may be made of material with a UL recognized flammability rating of V-2.

## 7.11.5 Secondary Circuit Protection

Spindle/VCM driver module includes 12V over current protection circuit.

# 7.12 Electromagnetic compatibility

When installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, the hard disk drive meets the following worldwide EMC requirements:

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).
- Electrostatic Discharge Susceptibility limits for a Class 2 ESD environment
- Radiated Electromagnetic Susceptibility (RES)
- Spectrum Management Agency (SMA) EMC requirements of Australia. The SMA has approved two forms of C-Tick Marking for IBM.

## 7.13 CE Mark

The product is declared to be in conformity with requirements of the following EC directives under the sole responsibility of IBM United Kingdom Ltd. or Yamato Lab, IBM Japan Ltd.

Council Directive 89/336/EEC on the approximation of laws of the Member States relating to electro-magnetic compatibility.

## 7.14 C-Tick Mark

The product complies with the following Australian EMC standard:

Limits and methods of measurement of radio disturbance characteristics of information technology, AS/NZS 3548 : 1995 Class B.

# Part 2. Interface specification

This page intentionally left blank.

# 8.0 General

This specification describes the host interface of the DTLA-30XXXX.

The interface conforms to the Working Document of Information Technology - AT Attachment with Packet Interface Extension (ATA/ATAPI-5) Revision 2 dated 13 December 1999 with certain limitations described in 8.2, "**Deviations from standard**."

## 8.1 Terminology

| | |
|---|---|
| **Device** | The DTLA-30XXXX hard disk drive |
| **Host** | The system to which the device is attached |

## 8.2 Deviations from standard

The device conforms to the referenced specifications with the following deviations:

**Check Power Mode**. Check Power Mode command returns FFh to Sector Count Register when the device is in Idle mode. This command does not support 80h as the return value.

**Hard Reset**. Hard reset response is not the same as that of power on reset. Refer to section 10.1, "**Reset response**," on page 73 for details.

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# 9.0 Registers

| Addresses | | | | | Functions | |
|---|---|---|---|---|---|---|
| CS0– | CS1– | DA2 | DA1 | DA0 | READ (DIOR–) | WRITE (DIOW–) |
| N | N | x | x | x | Data bus high impedance | Not used |
| | | | | | Control block registers | |
| N | A | 0 | x | x | Data bus high impedance | Not used |
| N | A | 1 | 0 | x | Data bus high impedance | Not used |
| N | A | 1 | 1 | 0 | Alternate Status | Device Control |
| N | A | 1 | 1 | 1 | Device Address | Not used |
| | | | | | Command block registers | |
| A | N | 0 | 0 | 0 | Data | Data |
| A | N | 0 | 0 | 1 | Error Register | Features |
| A | N | 0 | 1 | 0 | Sector Count | Sector Count |
| A | N | 0 | 1 | 1 | Sector Number | Sector Number |
| A | N | 0 | 1 | 1 | LBA bits 0–7[1] | 2 LBA bits 0–7[1] |
| A | N | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| A | N | 1 | 0 | 0 | LBA bits 8–15[1] | 2 LBA bits 8–15[1] |
| A | N | 1 | 0 | 1 | Cylinder High | Cylinder High |
| A | N | 1 | 0 | 1 | LBA bits 16–23[1] | 2 LBA bits 16–23[1] |
| A | N | 1 | 1 | 0 | Device/Head. | Device/Head |
| A | N | 1 | 1 | 0 | LBA bits 24–27[1] | 2 LBA bits 24–27[1] |
| A | N | 1 | 1 | 1 | Status | Command |
| A | A | x | x | x | Invalid address | |

[1] Mapping of registers in LBA mode

Logic conventions: A = signal asserted
N = signal negated
X = may be A or N

Figure 64. Register Set

Communication to or from the device is through an I/ O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0–, CS1–, DA2, DA1, DA0, DIOR– and DIOW–).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

## 9.1 Alternate Status Register

| Alternate Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC/ SERV | DBQ | COR | IDX | ERR |

Figure 65. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 9.13, “Status Register” on page 72 for the definition of the bits in this register.

## 9.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Figure 82 on page 103.

All other registers required for the command must be set up before writing the Command Register.

## 9.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may range from zero to the number of cylinders minus one.

## 9.4 Cylinder Low Register

This register contains the low order bits of the starting cylinder address for any disk access. At the end of the command this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

## 9.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command and configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

## 9.6 Device Control Register

| Device Control Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | 1 | SRST | –IEN | 0 |

Figure 66. Device Control Register

**Bit Definitions**

**SRST (RST)** Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device.

The host must set RST=1 and wait for at least 5us before setting RST=0 to ensure that the device recognizes the reset.

**-IEN** Interrupt Enable. When -IEN=0 and the device is selected, device interrupts to the host will be enabled. When -IEN=1 or the device is not selected, device interrupts to the host will be disabled.

## 9.7 Drive Address Register

| Drive Address Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| HIZ | –WTG | –H3 | –H2 | –H1 | –H0 | –DS1 | –DS0 |

Figure 67. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

**Bit Definitions**

**HIZ** High Impedance. This bit is not driven and will always be in a high impedance state.

**-WTG** -Write Gate. This bit is 0 when writing to the disk device is in progress.

**-H3,-H2,-H1,-H0** -

-Head Select. These four bits are the 1's complement of the binary coded address of the currently selected head. -H0 is the least significant.

**-DS1** -Drive Select 1. Drive select bit for device 1, active low. DS1=0 when device 1 (slave) is selected and active.

**-DS0** -Drive Select 0. Drive select bit for device 0, active low. DS0=0 when device 0 (master) is selected and active.

## 9.8 Device/Head Register

| Device/Head Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1 | L | 1 | DRV | HS3 | HS2 | HS1 | HS0 |

Figure 68. Device/Head Register

This register contains the device and head numbers.

**Bit Definitions**

**L** Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.

**DRV** Device. When DRV=0, device 0 (master) is selected. When DRV=1, device 1 (slave) is selected.

**HS3,HS2,HS1,HS0**

Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion these bits are updated to reflect the currently selected head.

The head number may be from zero to the number of heads minus one.

In LBA mode HS3 through HS0 contain bits 24-27 of the LBA. At command completion these bits are updated to reflect the current LBA bits 24-27.

## 9.9 Error Register

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ICRCE | UNC | 0 | IDNF | 0 | ABRT | TK0NF | AMNF |

Figure 69. Error Register

This register contains status from the last command executed by the device or a diagnostic code.

At the completion of any command except Execute Device Diagnostic the contents of this register are always valid even if ERR=0 is in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Figure 73 on page 74 for the definition.

**Bit Definitions**

| | |
|---|---|
| **ICRCE (CRC)** | Interface CRC Error. CRC=1 indicates a CRC error has occurred on the data bus during Ultra-DMA transfer. |
| **UNC** | Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered. |
| **IDNF (IDN)** | ID Not Found. IDN=1 indicates the ID field of the requested sector could not be found. |
| **ABRT (ABT)** | Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register. |
| **TK0NF (T0N)** | Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command. |
| **AMNF (AMN)** | Address Mark Not Found. AMN=1 indicates that data address mark has not been found after finding the correct ID field for the requested sector. |

## 9.10 Features Register

This register is command specific. This is used with the Set Features command and S.M.A.R.T. Function Set command.

## 9.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

## 9.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode this register contains Bits 0-7. At the end of the command this register is updated to reflect the current LBA Bits 0-7.

## 9.13 Status Register

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | DRDY | DF | DSC/ SERV | DRQ | CORR | IDX | ERR |

Figure 70. Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

The use of bit 4 is command dependent. After the DMA Queued commands it is used as SERV. After any other commands are reset, it is used as DSC.

**Bit Definitions**

**BSY** Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

**DRDY (RDY)** Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to zero during power on until the device is ready to accept a command. If the device detects an error while processing a command, RDY is set to zero until the Status Register is read by the host, at which time RDY is set back to one.

**DF** Device Fault. DF = 1 indicates that the device has detected a write fault condition. DF is set to zero after the Status Register is read by the host.

**DSC** Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to zero by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host at which time the bit again indicates the current seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.

**SERV (SRV)** Service. SRV is set to one when the device is ready to transfer data after it releases the bus for execution of a DMA Queued command.

**DRQ** Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.

**CORR (COR)** Corrected Data. Always zero.

**IDX** Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to one even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.

**ERR** Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

# 10.0 General operation

## 10.1 Reset response

There are three types of resets in ATA:

**Power On Reset (POR)**

The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed, and other mechanical parametrics, and sets default values.

**Hard Reset (Hardware Reset)**

RESET- signal is negated in ATA Bus. The device resets the interface circuitry as well as Soft Reset.

**Soft Reset (Software Reset)**

SRST bit in the Device Control Register is set, then is reset. The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset is shown in the following figure.

| | POR | hard reset | soft reset |
|---|---|---|---|
| Aborting Host interface | – | O | O |
| Aborting Device interface | – | (1) | (1) |
| Initialization of hardware | O | X | X |
| Internal diagnostic | O | X | X |
| Spinning spindle | O | X | X |
| Initialization of registers (2) | O | O | O |
| DASP handshake | O | O | X |
| PDIAG handshake | O | O | O |
| Reverting programmed parameters to default<br>• Number of CHS (set by Initialize Device Parameters)<br>• Multiple mode<br>• Write Cache<br>• Read look-ahead<br>• ECC bytes | O | (3) | (3) |
| Disable Standby timer | O | X | X |
| Power mode | (5) | (4) | (4) |

O - execute X - not execute

*Notes:*

(1) Execute after the data in write cache has been written.
(2) Default value on POR is shown in Figure 72 on page 74
(3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.
(4) In the case of Sleep mode the device goes to Standby mode. In other cases the device does not change current mode.
(5) Idle when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

Figure 71. Reset Response Table

## 10.1.1 Register initialization

| Register | Default Value |
|---|---|
| Error | Diagnostic Code |
| Sector Count | 01h |
| Sector Number | 01h |
| Cylinder Low | 00h |
| Cylinder High | 00h |
| Device/Head | A0h |
| Status | 50h |
| Alternate Status | 50h |

Figure 72. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in the figure below.

| Code | Description |
|---|---|
| 01h | No error detected |
| 02h | Formatter device error |
| 03h | Sector buffer error |
| 04h | ECC circuitry error |
| 05h | Controller microprocessor error |
| 8xh | Device 1 failed |

Figure 73. Diagnostic Codes

## 10.2 Diagnostic and reset considerations

For each Reset and Execute Device Diagnostic the diagnostic is done as follows:

**Power On Reset**

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error. Otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity.

**Hard Reset, Soft Reset**

If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors. Otherwise Device 0 shall simply reset and clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

**Execute Device Diagnostic**

If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command. Otherwise Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

In all the above cases Power on, RESET-, Soft reset, and the EXECUTE DEVICE DIAGNOSTIC command the Device 0 Error register as shown in the figure below.

| Device 1 present? | PDIAG– Asserted? | Device 0 Passed | | Error Register |
|---|---|---|---|---|
| Yes | Yes | Yes | | 01h |
| Yes | Yes | No | | 0xh |
| Yes | No | Yes | | 81h |
| Yes | No | No | | 8xh |
| No | (not read) | Yes | | 01h |
| No | (not read) | No | | 0xh |

'x' indicates the appropriate Diagnostic Code for the Power on, RESET–, Soft Reset, or Device Diagnostic error.

Figure 74. Reset error register values

## 10.3 Sector Addressing Mode

All addressing of data sectors recorded on the drive media is by a logical sector address. The logical CHS address for the drive is different from the actual physical CHS location of the data sector on the disk media.

The drive supports both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. So a host system must set the L bit to 1 if the host uses LBA Addressing mode.

### 10.3.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: cylinder number, head number and sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but cannot exceed 255(0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 15(0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535(0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode is also described in the Identify Device Information.

### 10.3.2 LBA Addressing Mode

Logical sectors on the device shall be mapped linearly with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector ( cylinder 0, head 0, sector 1). Regardless of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following formula is always true:

LBA = ((cylinder * heads per cylinder + heads) * sectors per track) + sector – 1

where *heads per cylinder* and *sectors per track* are the current translation mode values.

On LBA addressing mode the LBA value is set to the following register:

| | |
|---|---|
| Device/Head | <--- LBA bits 27-24 |
| Cylinder High | <--- LBA bits 23-16 |
| Cylinder Low | <--- LBA bits 15-8 |
| Sector Number | <--- LBA bits 7-0 |

## 10.4 Overlapped and queued feature

Overlap allows devices to perform a bus release so that the other device on the bus may be used. To perform a bus release the device clears both DRQ and BSY to zero. When selecting the other device during overlapped operations, the host shall disable interrupts via the nIEN bit on the currently selected device before writing the Device/Head register to select the other device.

The only commands that may be overlapped are

| | |
|---|---|
| **NOP (with 01h subcommand code)** | ('00'h) |
| **Read DMA Queued** | ('C7'h) |
| **Service** | ('A2'h) |
| **Write DMA Queued** | ('CC'h) |

For the READ DMA QUEUED and WRITE DMA QUEUED commands, the device may or may not perform a bus release. If the device is ready to complete the execution of the command, it may complete the command immediately. If the device is not ready to complete the execution of the command, the device may perform a bus release and complete the command via a service request.

Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the overlapped feature set may be queued. If a queue exists when a non-queued command is received, the nonqueued command shall be aborted and the commands in the queue shall be discarded. The ending status shall be ABORT command and the results are indeterminate.

The maximum queue depth supported by a device is indicated in word 73 of Identify Device information.

A queued command shall have a Tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this Tag shall be restored so that the host may identify the command for which status is being presented. If a queued command is issued with a Tag value that is identical to the Tag value for a command already in the queue, the entire queue is aborted including the new command. The ending status is ABORT command and the results are indeterminate. If any error occurs, the command queue is aborted.

When the device is ready to continue processing a bus released command and BSY and DRQ are both cleared to zero, the device requests service by setting SERV to one, setting a pending interrupt, and asserting INTRQ if selected and if nIEN is cleared to zero. SERV shall remain set until all commands ready for service have been serviced. The pending interrupt shall be cleared and INTRQ negated by a Status register read or a write to the Command register.

When the device is ready to continue processing a bus released command and BSY or DRQ is set to one (i.e., the device is processing another command on the bus), the device requests service by setting SERV to one. SERV shall remain set until all commands ready for service have been serviced. At command completion of the current command processing (i.e., when both BSY and DRQ are cleared to zero), the device shall process interrupt pending and INTRQ per the protocol for the command being completed. No additional interrupt shall occur due to other commands ready for service until after the SERV bit of the device has been cleared to zero.

When the device receives a new command while queued commands are ready for service, the device shall execute the new command and process interrupt pending and INTRQ per the protocol for the new command. If the queued commands ready for service still exist at command completion of this command, SERV remains set to one but no additional interrupt shall occur due to commands ready for service.

When queuing commands, the host shall disable interrupts via the nIEN bit before writing a new command to the Command register and may re-enable interrupts after writing the command. When reading status at command completion of a command, the host shall check the SERV bit since the SERV bit may be set because the device is ready for service associated with another queued command. The host receives no additional interrupt to indicate that a queued command is ready for service.

## 10.5 Power management feature

The power management feature functions permit a host to reduce the power required to operate the drive. It provides a set of commands and a timer that enables a device to implement low power consumption modes.

The drive implements the following set of functions:

- Standby timer
- Idle command
- Idle Immediate command
- Sleep command
- Standby command
- Standby Immediate command

### 10.5.1 Power modes

The lowest power consumption when the device is powered on occurs in Sleep Mode. When in sleep mode, the device requires a reset to be activated.

In Standby Mode the device interface is capable of accepting commands, but as the media may not be immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

In Idle Mode the device is capable of responding immediately to media access requests.

In Active Mode the device is executing a command or accessing the disk media with the read look- ahead function or the write cache function.

### 10.5.2 Power management commands

The Check Power Mode command enables a host to determine if a device is currently in, going into, or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode directly from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The Standby and Standby Immediate commands move a device to standby mode directly from the active or idle modes. The standby command also sets the standby timer count.

The Sleep command moves a device to sleep mode. The interface of the device becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode, it enters Standby mode.

### 10.5.3 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and, if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT register on Idle command or Standby command is set to 00h, the standby timer is disabled.

### 10.5.4 Interface capability for power modes

Each power mode affects the physical interface as defined in the following table.

| Mode | | BSY | RDY | Interface active | Media |
|---|---|---|---|---|---|
| Active | | X | X | Yes | Active |
| Idle | | O | 1 | Yes | Active |
| Standby | | O | 1 | Yes | Inactive |
| Sleep | | O | 1 | No | Inactive |

Figure 75. Power conditions

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

## 10.6 S.M.A.R.T. function

The intent of Self-Monitoring Analysis and Reporting Technology (S.M.A.R.T) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

### 10.6.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on the ability of that attribute to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

### 10.6.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition.

### 10.6.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical values of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimals.

## 10.6.4 Threshold Exceeded Condition

If one or more attribute values, whose Pre-failure bit of their status flag is set, are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

## 10.6.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds, and other logging and reporting information.

## 10.6.6 Off-line read scanning

The device provides the off-line read scanning feature with reallocation. This is the extension of the off-line data collection capability. The device performs the entire read scan with reallocation of the marginal sectors to prevent user data lost.

If interrupted by the host during the read scanning, the device services the host command.

## 10.6.7 Error log

Logging of reported errors is supported. The device provides information on the last five errors that the device reported as described in the SMART error log sector. The device may also provide additional vendor specific information on these reported errors. The error log is not disabled when SMART is disabled. Disabling SMART shall disable the delivering of error log information via the SMART READ LOG SECTOR command.

If a device receives a firmware modification, all error log data is discarded and the device error count for the life of the device is reset to zero.

## 10.6.8 Self-test

The device provides the self-test features which are initiated by SMART Execute Off-line Immediate command. The self-test checks the fault of the device, reports the test status in Device Attributes Data, and stores the test result in the SMART self-test log sector as described in the SMART self-test log data structure. All SMART attributes are updated accordingly during the execution of self-test.

If interrupted by the host during the self-tests, the device services the host command.

If the device receives a firmware modification, all self-test log data is discarded.

## 10.7 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to a hard disk drive even if the device is removed from the computer.

The following commands are supported for this feature:

| | |
|---|---|
| Security Set Password | ('F1'h) |
| Security Unlock | ('F2'h) |
| Security Erase Prepare | ('F3'h) |
| Security Erase Unit | ('F4'h) |
| Security Freeze Lock | ('F5'h) |
| Security Disable Password | ('F6'h) |

### 10.7.1 Security mode

The following security modes are provided:

**Device Locked mode** The device disables media access commands after power on. Media access commands are enabled by either a security unlock command or a security erase unit command.

**Device Unlocked mode** The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a security unlock or a security erase unit command.

**Device Frozen mode** The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

### 10.7.2 Security level

The following security levels are provided:

**High level security** When the device lock function is enabled and the User Password is forgotten, the device can be unlocked via a Master Password.

**Maximum level security** When the device lock function is enabled and the User Password is forgotten, only the Master Password with a Security Erase Unit command can unlock the device. User data is then erased.

### 10.7.3 Passwords

This function can have two kinds of passwords as described below:

**Master Password** When the Master Password is set, the device does NOT enable the Device Lock Function and the device canNOT be locked with the Master Password, but the Master Password can be used for unlocking the device locked.

Identify Device Information word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh.

**User Password** The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function and the device is then locked on next power on reset or hard reset.

The system manufacturer or dealer who intends to enable the device lock function for end-users must set the master password even if only single level password protection is required.

## 10.7.4 Operation example

### 10.7.4.1 Master Password setting

The system manufacturer or dealer can set a new Master Password from default Master Password using the Security Set Password command without enabling the Device Lock Function.

The Master Password Revision Code is set to FFFEh as shipping default by the drive manufacturer.

### 10.7.4.2 User Password setting

When a User Password is set, the device will automatically enter lock mode when the device is powered on the next time.

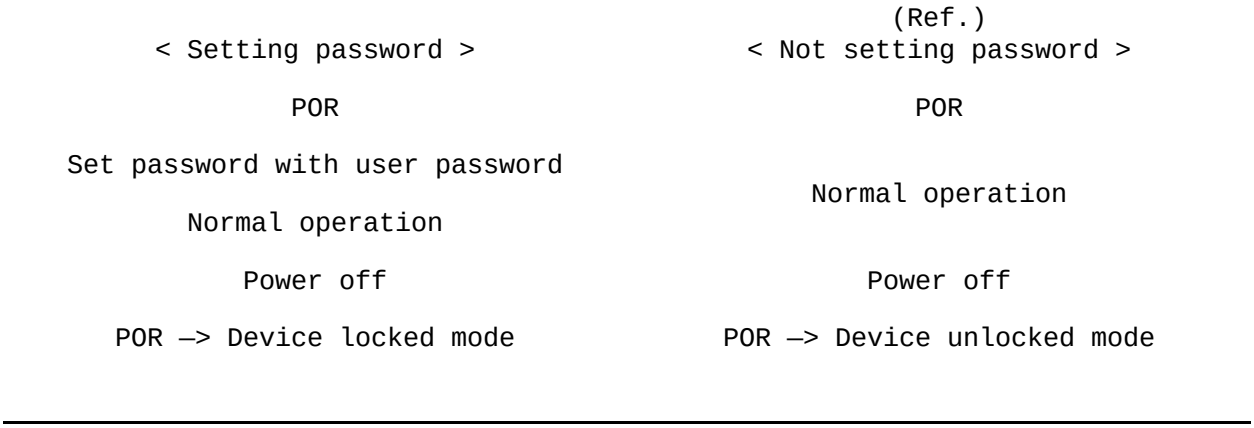



Figure 76. Initial Setting

### 10.7.4.3 Operation from POR after User Password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.

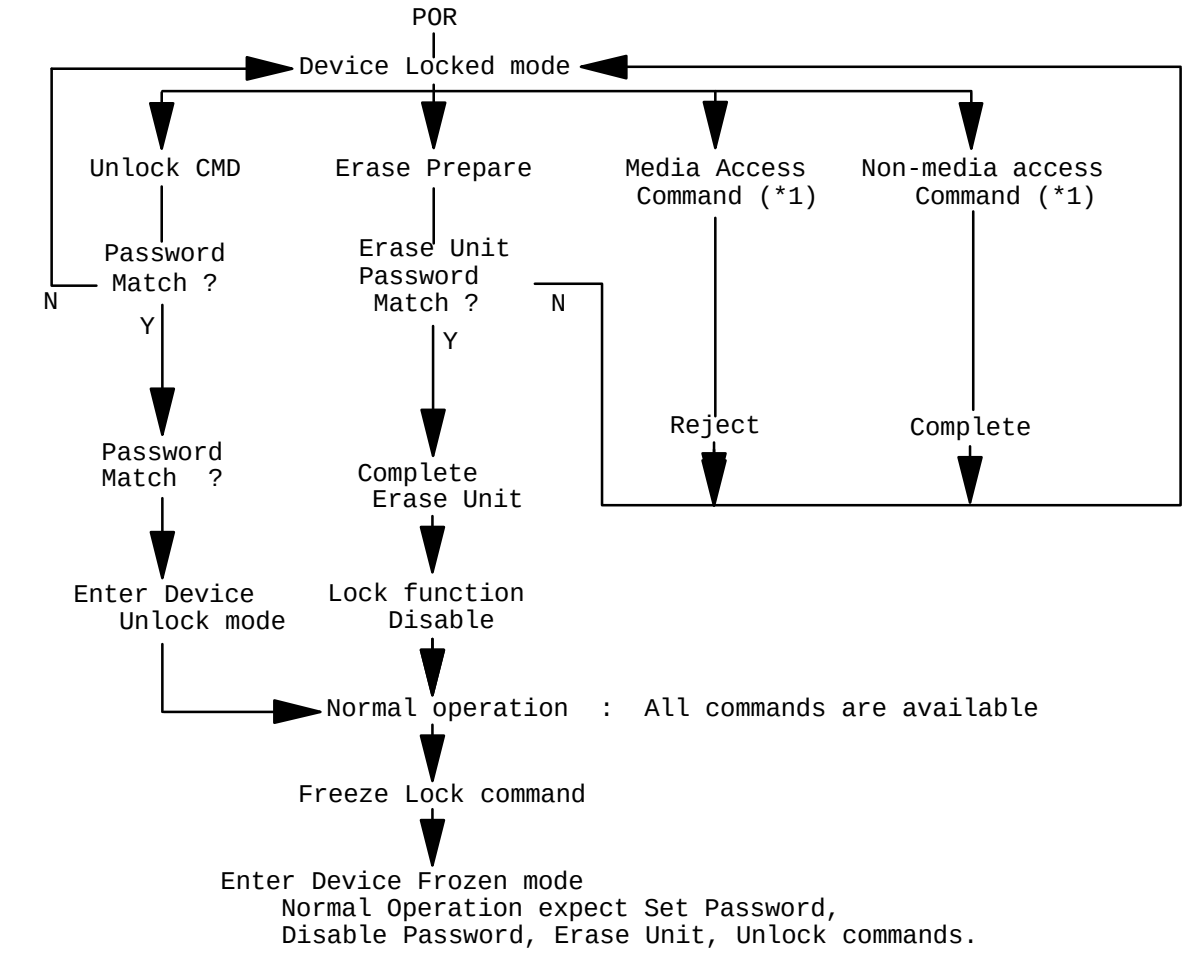



Figure 77. Usual Operation

### 10.7.4.4 User Password Lost

If the User Password is forgotten and High level security is set, the system user cannot access any data. However the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

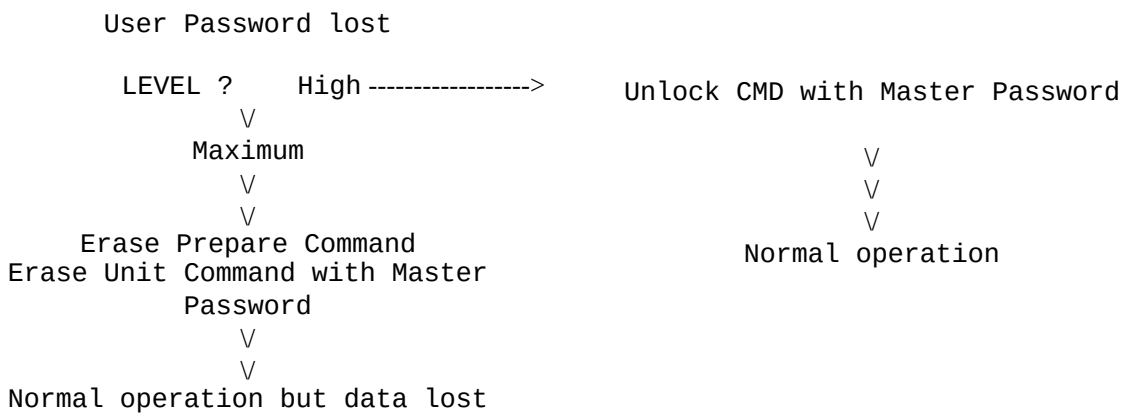



Figure 78. Password Lost

### 10.7.4.5 Attempt limit for SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit. The purpose of this attempt limit is to prevent someone from attempting to unlock the drive by using various passwords multiple times.

The device counts the password mismatch. If the password does not match, the device counts it without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit (bit 4) of Word 128 in Identify Device information is set and the SECURITY ERASE UNIT command and the SECURITY UNLOCK command are then aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power-on reset or a hard reset.

## 10.7.5 Command table

This table shows the response of the device to commands when the Security Mode Feature Set (Device lock function) is enabled.

| Command | Locked Mode | Unlocked Mode | Frozen Mode |
|---|---|---|---|
| Check Power Mode | Executable | Executable | Executable |
| Execute Device Diagnostic | Executable | Executable | Executable |
| Flush Cache | Executable | Executable | Executable |
| Format Track | Command aborted | Executable | Executable |
| Identify Device | Executable | Executable | Executable |
| Idle | Executable | Executable | Executable |
| Idle Immediate | Executable | Executable | Executable |
| Initialize Device Parameters | Executable | Executable | Executable |
| NOP | Executable | Executable | Executable |
| Read Buffer | Executable | Executable | Executable |
| Read DMA (w/o retry) | Command aborted | Executable | Executable |
| Read DMA (w/retry) | Command aborted | Executable | Executable |
| Read DMA Queued | Command aborted | Executable | Executable |
| Read Long (w/o retry) | Command aborted | Executable | Executable |
| Read Long (w/retry) | Command aborted | Executable | Executable |
| Read Multiple | Command aborted | Executable | Executable |
| Read Native Max Address | Executable | Executable | Executable |
| Read Sector(s) (w/o retry) | Command aborted | Executable | Executable |
| Read Sector(s) (w/retry | Command aborted | Executable | Executable |
| Read Verify Sector(s) (w/o retry) | Command aborted | Executable | Executable |
| Read Verify Sector(s) (w/retry) | Command aborted | Executable | Executable |
| Recalibrate | Executable | Executable | Executable |
| Security Disable Password | Command aborted | Executable | Command aborted |
| Security Erase Prepare | Executable | Executable | Executable |
| Security Erase Unit | Executable | Executable | Command aborted |
| Security Freeze Lock | Command aborted | Executable | Executable |
| Security Set Password | Command aborted | Executable | Command aborted |
| Security Unlock | Executable | Executable | Command aborted |
| Seek | Executable | Executable | Executable |
| Service | Command aborted | Executable | Executable |
| Set Features | Executable | Executable | Executable |
| Set Max Address | Executable | Executable | Executable |
| Set Multiple Mode | Executable | Executable | Executable |
| Sleep | Executable | Executable | Executable |
| SMART Disable Operations | Executable | Executable | Executable |
| SMART Enable/Disable Attribute Autosave | Executable | Executable | Executable |
| SMART Enable Operations | Executable | Executable | Executable |
| SMART Execute Off-line Immediate | Executable | Executable | Executable |
| SMART Read Attribute Values | Executable | Executable | Executable |
| SMART Read Attribute Thresholds | Executable | Executable | Executable |
| SMART Return Status | Executable | Executable | Executable |
| SMART Save Attribute Values | Executable | Executable | Executable |
| SMART Enable/Disable Automatic Off-line Data Collection | Executable | Executable | Executable |
| Standby | Executable | Executable | Executable |

Figure 79. Command table for device lock operation (part 1 of 2)

| Command | Locked Mode | Unlocked Mode | Frozen Mode |
|---|---|---|---|
| Standby Immediate | Executable | Executable | Executable |
| Write Buffer | Executable | Executable | Executable |
| Write DMA (w/o retry) | Command aborted | Executable | Executable |
| Write DMA (w/retry) | Command aborted | Executable | Executable |
| Write DMA Queued | Command aborted | Executable | Executable |
| Write Long (w/o retry) | Command aborted | Executable | Executable |
| Write Long (w/retry) | Command aborted | Executable | Executable |
| Write Multiple | Command aborted | Executable | Executable |
| Write Sector(s) (w/o retry) | Command aborted | Executable | Executable |
| Write Sector(s) (w/retry) | Command aborted | Executable | Executable |
| Write Verify | Command aborted | Executable | Executable |

Figure 79. Command table for device lock operation (part 2 of 2)

## 10.8 Host Protected Area Function

The Host Protected Area Function provides a protected area which cannot be accessed via conventional methods. This protected area is used to contain critical system data such as BIOS or system management information. The contents of the main memory of the entire system may also be dumped into the protected area to resume after system power off.

The following set of commands change the LBA/CYL, which affects the Identify Device Information:

**Read Native Max Address** ('F8'h)

**Set Max Address** ('F9'h)

### 10.8.1 Example for operation (in LBA mode)

The following is an example of possible values for LBA, size, and other device characteristics:

| | |
|---|---|
| Capacity (native) | 6,498,680,832 byte (6.4GB) |
| Maximum LBA (native) | 12,692,735 (C1ACFFh) |
| Required size for protected area | 206,438,400 byte |
| Required blocks for protected area | 403,200 (062700h) |
| Customer usable device size | 6,292,242,432 byte (6.2GB) |
| Customer usable sector count | 12,289,536 (BB8600h) |
| LBA range for protected area | BB8600h to C1ACFFh |

*1. Shipping of drives from the manufacturer*

Prior to being shipped from the manufacturer each drive has been tested to have a usable capacity of 6.4GB besides flagged media defects not visible by system.

*2. Preparation of drives by the system manufacturer*

Special utility software is required to define the size of the protected area and to store the data in it. The sequence is as follows:

i. Issue a Read Native Max Address command to get the real device maximum LBA. Returned value shows that the native device maximum LBA is 12,692,735 (C1ACFFh) regardless of the current setting.

ii. Make the entire device accessible including the protected area by setting device maximum LBA to 12,692,735 (C1ACFFh) via Set Max Address command. The option may be either nonvolatile or volatile.

iii. Test the sectors for protected area (LBA > = 12,289,536 (BB8600h)) if required.

iv. Write information data such as BIOS code within the protected area.

v. Change maximum LBA using Set Max Address command to 12,289,535 (BB85FFh) with nonvolatile option.

vi. From this point the protected area cannot be accessed until the next Set Max Address command is issued. Any BIOS, device drivers, or application software access the drive as if it were a 6.2GB device since the device functions in the same manner as real 6.2GB device.

*3. Conventional usage without system software support*

Since the drive works as a 6.2GB device, this device requires no special care for normal use.

*4. Advanced usage using protected area*

The data in the protected area is accessed by the following method:

i. Issue Read Native Max Address command to get the real device maximum LBA. Returned value shows that native device maximum LBA is 12,692,735 (C1ACFFh) regardless of the current setting.

ii. Make the entire device including the protected area accessible by setting device maximum LBA as 12,692,735 (C1ACFFh) via Set Max Address command with the volatile option. By using this option an unexpected power removal or reset will not make the protected area remain accessible.

iii. Read information data from protected area.

iv. Issue hard reset or POR to inhibit any access to the protected area.

## 10.8.2 Security extensions

1. Set Max Set Password
2. Set Max Lock
3. Set Max Freeze Lock
4. Set Max Unlock

The Set Max Set Password command allows the host to define the password to be used during the current power on cycle. The password does not persist over a power cycle but does persist over a hardware or software reset. This password is not related to the password used for the Security Mode Feature set. When the password is set the device is in the Set_Max_Unlocked mode. The Set Max Lock command allows the host to disable the Set Max commands (except set Max Unlock) until the next power cycle or the issuance and acceptance of the Set Max Unlock command. When this command is accepted, the device is in the Set_Max_Locked mode. The Set Max Unlock command changes the device from the Set_Max_Locked mode to the Set_Max_Unlocked mode. The Set Max Freeze Lock command allows the host to disable the Set Max commands (including Set Max UNLOCK) until the next power cycle. When this command is accepted, the device is in the Set_Max_Frozen mode.

The IDENTIFY DEVICE response word 83, bit 8 indicates that this extension is supported if set, and word 86, bit 8 indicates the Set Max security extension is enabled if set.

## 10.9 Seek Overlap

The DTLA-3xxxxx provides an accurate seek time measurement method. The seek command is usually used to measure the device seek time by accumulating the execution time for a number of seek commands. With typical implementation of seek command this measurement must include the device and host command overhead. To eliminate this overhead the DTLA-3xxxxx overlaps the seek command as described below.

The first seek command is completed before the actual seek operation is ended. Then the device can receive the next seek command from the host; however, the actual seek operation for the next seek command starts immediately after the actual seek operation for the first seek command is completed. In other words, the execution of two seek commands overlaps excluding the time required for the actual seek operation.

With this overlap the total elapsed time for a number of seek commands results in the total accumulated time for actual seek operation plus one pre- and post-overhead. When the number of seeks is large, only one overhead may be ignored.

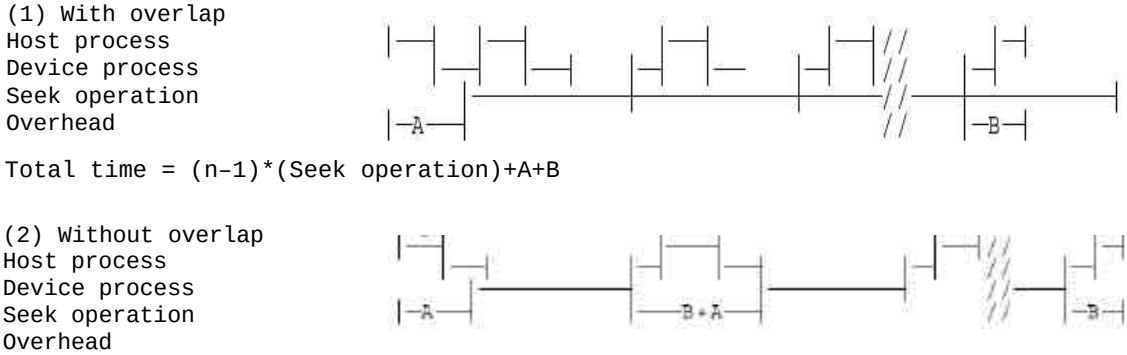



Figure 80. Seek overlap

## 10.10 Write cache function

Write cache is a performance enhancement whereby the device reports the completion of the write command (Write Sectors, Write Multiple, and Write DMA) to the host as soon as the device has received all of the data into its buffer. The device assumes the responsibility of subsequently writing the data onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. However power off terminates the writing operation immediately and unwritten data is lost.
- The Soft reset, Standby (Immediate) command, and Flush Cache commands during the writing of the cached data are executed after the completion of writing to media. So the host system can confirm the completion of write cache operation by issuing a Soft reset, Standby (Immediate) command, or Flush Cache command and then confirming its completion. It is recommended that the host system verify the completion of the write cache operation by issuing Soft reset, the Standby (Immediate) command, or the Flush Cache command to the device before power off.
- The retry bit of Write Sectors is ignored when write cache is enabled.

# 10.11 Reassign Function

Reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector.

This reassignment information is registered internally and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the reassign function will be disabled automatically.

The spare sectors for reassignment are located at the end of device. As a result of reassignment the physical location of logically sequenced sectors will be dispersed.

## 10.11.1 Auto Reassign Function

The sectors which show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located at the end of drive. The conditions for auto-reallocation are described below.

### 10.11.1.1 Nonrecovered write errors

When a write operation cannot be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation has failed.

If the write cache function is ENABLED, and when the number of available spare sectors reaches 0 sector, both auto reassign function and write cache function are disabled automatically.

### 10.11.1.2 Nonrecovered read errors

When a read operation is failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

### 10.11.1.3 Recovered read errors

When a read operation for a sector has failed once and then has recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the predefined conditions.

# 10.12 Power-Up In Standby feature set

The Power-Up In Standby feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.

This feature set will be enabled/disabled via the SET FEATURES command or use of jumper. When enabled by a jumper, the feature set shall not be disabled via the SET FEATURES command. The enabling of this feature set shall be persistent after power cycle.

A device needs a SET FEATURES subcommand to spin-up to active state when the device has powered up into Standby. The device remains in Standby until the SET FEATURES subcommand is received.

If power-up into Standby is enabled, when an IDENTIFY DEVICE is received while the device is in Standby as a result of powering up into Standby, the device shall set word 0 bit 2 to one to indicate that the response is incomplete, then only words 0 and 2 are correctly reported.

The IDENTIFY DEVICE information indicates the states as follows:

- identify device information is complete or incomplete
- this feature set is implemented
- this feature set is enabled or disabled
- the device needs the Set Features command to spin-up into active state

## 10.13 Advanced Power Management feature set (APM)

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands described in the section of Set Feature command in detail. This feature set uses the following functions:

1. A SET FEATURES subcommand to enable Advanced Power Management
2. A SET FEATURES subcommand to disable Advanced Power Management

Advanced Power Management, Automatic Acoustic Management, and the Standby timer setting are independent functions. The device shall enter Standby mode if any of the following are true:

1. The Standby timer has been set and times out
2. Automatic Power Management is enabled, and the associated algorithm indicates that the Standby mode should be entered to save power
3. Automatic Acoustic Management is enabled, and the associated algorithm indicates that the Standby mode should be entered to reduce acoustical emanations

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 91, bits 7-0 contains the current Advanced Power Management level if it is enabled.

## 10.14 Automatic Acoustic Management feature set (AAM)

This feature set allows the host to select an acoustic management level. The acoustic management level may range from the lowest acoustic emanation setting of 01h to the maximum performance level of FEh. Device performance and acoustic emanation may increase with increasing acoustic management levels. The acoustic management levels may contain discrete bands. Automatic Acoustic Management levels 80h and higher do not permit the device to enter Standby mode as a result of the Automatic Acoustic Management algorithm. The Automatic Acoustic Management feature set uses the following functions:

1. A SET FEATURES subcommand to enable Automatic Acoustic Management
2. A SET FEATURES subcommand to disable Automatic Acoustic Management

Advanced Power Management, Automatic Acoustic Management, and the Standby timer setting are independent functions. The device shall enter Standby mode if any of the following are true:

1. The Standby timer has been set and times out.
2. Automatic Power Management is enabled and the associated algorithm indicates that the Standby mode should be entered to save power.

3. Automatic Acoustic Management is enabled and the associated algorithm indicates that the Standby mode should be entered to reduce acoustical emanations.

The IDENTIFY DEVICE response word 83, bit 9 indicates that Automatic Acoustic Management feature is supported if set. Word 86, bit 9 indicates that Automatic Acoustic Management is enabled if set. Word 94, bits 7-0 contain the current Automatic Acoustic Management level if Automatic Acoustic Management is enabled, and bits 8-15 contain the Vendor's recommended AAM level.

---

# 10.15 Address Offset Feature

Computer systems perform initial code loading (booting) by reading from a predefined address on a drive. To allow an alternate bootable operating system to exist in a system reserved area on a drive, this feature provides a Set Features function to temporarily offset the drive address space. The offset address space wraps around so that the entire drive address space remains addressable in offset mode. Max LBA in offset mode is set to the end of the system reserved area to protect the data in the user area when operating in offset mode. The Max LBA can be changed by an Set Max Address command to access the user area. If the native MAX LBA is set, the whole user area can be accessed. But any commands which access sectors across the original native maximum LBA are rejected with error, even if this protection is removed by an Set Max Address command.

## 10.15.1 Enable/Disable Address Offset Mode

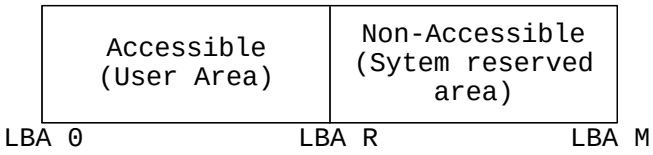
The Set Features subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, LBA 0, to the start of the nonvolatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset, or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a nonvolatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command, the command fails with Abort error status.

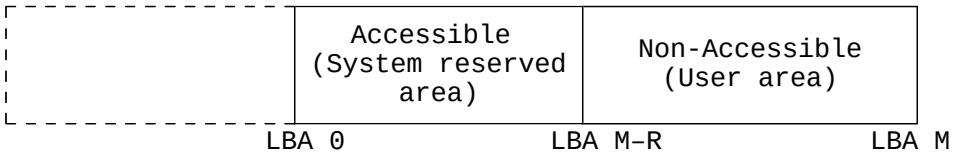
Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last nonvolatile Set Max Address command.

*Before Enable Address Offset Mode*

A reserved area has been created using a non-volatile Set Max command.




*After Enable Address Offset Mode*




*After Set Max Address Command using the Value Returned by Read Max Address*

Any commands which access sectors across the LBA M–R are aborted with error.

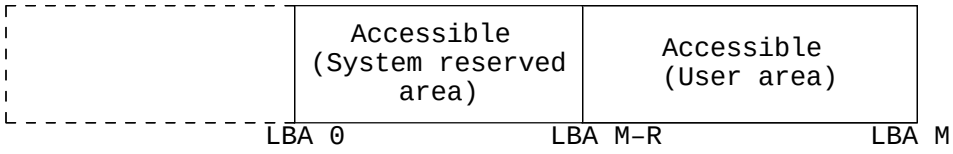



Figure 81. Device address map before and after Set Feature

## 10.15.2 Identify Device Data

Identify Device data word 83 bit 7 indicates the device supports the Address Offset Feature.

Identify Device data word 86 bit 7 indicates the device is in Address Offset mode.

## 10.15.3 Exceptions in Address Offset Mode

Any commands which access sectors across the original native maximum LBA are rejected with error even if the access protection is removed by an Set Max Address command.

The Read Look Ahead operation is not carried out even when enabled by Set Feature command.

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# 11.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from one to zero during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 145 on page 191 shows the device time-out values.

## 11.1 PIO Data In commands

These commands are

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors
- SMART Read Attribute Values
- SMART Read Attribute Thresholds

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector of data to be transferred
   a. The device sets BSY=1 and prepares for data transfer.
   b. When a sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
   c. In response to the interrupt the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads one sector of data via the Data Register.

f. The device sets DRQ=0 after the sector has been transferred to the host.

4. For the Read Long command
   a. The device sets BSY=1 and prepares for data transfer.
   b. When the sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
   c. In response to the interrupt the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads the sector of data including ECC bytes via the Data Register.
   f. The device sets DRQ=0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the device will set BSY=0, ERR=1, and DRQ=1. The device will then store the error status in the Error Register and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode; the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer and will be available to be transferred to the host at the option of the host. In case of a Read Multiple command the host should complete transfer of the block which includes error from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

## 11.2 PIO Data Out commands

These commands are:

- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Set Max Set Password command
- Set Max Unlock command
- SMART Write Log Sector
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. For each sector (or block) of data to be transferred:

   a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).

   b. The host writes one sector (or block) of data via the Data Register.

   c. The device sets BSY=1 after it has received the sector (or block).

   d. When the device has finished processing the sector (or block), it sets BSY=0 and interrupts the host.

   e. In response to the interrupt, the host reads the Status Register.

   f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:

   a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector.

   b. The host writes one sector of data including ECC bytes via the Data Register.

   c. The device sets BSY=1 after it has received the sector.

   d. After processing the sector of data the device sets BSY=0 and interrupts the host.

   e. In response to the interrupt, the host reads the Status Register.

   f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode; the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

All data transfers to the device through the Data Register are 16 bits, except for the ECC bytes which are 8 bits.

## 11.3 Non-data commands

Non-data commands are

- Check Power Mode
- Execute Device Diagnostic
- Flush Cache
- Idle
- Idle Immediate
- Initialize Device Parameters
- NOP
- Read Native Max Address
- Read Verify Sectors
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max Address
- Set MaX LocK command
- Set MaX Freeze Lock command
- Set Multiple Mode
- Sleep
- SMART Disable Operations
- SMART Enable/Disable Attribute Autosave
- SMART Enable Operations
- SMART Execute Off-line Data Collection
- SMART Return Status
- SMART Save Attribute Values
- SMART Enable/Disable Automatic Off Line Data Collection
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. When the device has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The device clears the interrupt in response to the Status Register being read.

## 11.4 DMA commands

DMA commands are

- Read DMA
- Write DMA

Data transfers using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave DMA channel
- no intermediate sector interrupts are issued on multisector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different for the following reasons:

- no intermediate sector interrupts are issued on multisector commands
- the host resets the DMA channel prior to reading status from the device

The DMA protocol allows high performance multitasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave DMA channel
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
3. Host writes command code to the Command Register
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. Host resets the slave DMA channel.
8. Host reads the Status Register and, optionally, the Error Register.

## 11.5 DMA queued commands

These commands are

- Read DMA Queued
- Service
- Write DMA Queued

1. Command Issue
   a. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head registers.
   b. The host writes command code to the Command Register.
   c. The device sets BSY.
   d. The device clears or sets REL.
   e. The device clears BSY.
2. Data Transfer and Command Completion
   If the device is ready for data transfer (REL is cleared)
   a. the host transfers the data for the command identified by the Tag number using the DMA transfer protocol currently in effect.
   b. the device generates an interrupt to the host, when all of the data has been transferred.
   c. the host may issue another command or wait for service request from the device.
3. Bus Release
   If the device is not ready for data transfer (REL is set)
   a. the device generates an interrupt if release interrupt is enabled.
   b. the host may issue another command or wait for service request from the device.

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# 12.0 Command descriptions

| Pro-tocol | Command | Code (Hex) | Binary Code Bit 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| 3 | Check Power Mode | E5 | 1 1 1 0 0 1 0 1 |
| 3 | Check Power Mode* | 98 | 1 0 0 1 1 0 0 0 |
| 3 | Execute Device Diagnostic | 90 | 1 0 0 1 0 0 0 0 |
| 3 | Flush Cache | E7 | 1 1 1 0 0 1 1 1 |
| 2 | Format Track | 50 | 0 1 0 1 0 0 0 0 |
| 1 | Identify Device | EC | 1 1 1 0 1 1 0 0 |
| 3 | Idle | E3 | 1 1 1 0 0 0 1 1 |
| 3 | Idle* | 97 | 1 0 0 1 0 1 1 1 |
| 3 | Idle Immediate | E1 | 1 1 1 0 0 0 0 1 |
| 3 | Idle Immediate* | 95 | 1 0 0 1 0 1 0 1 |
| 3 | Initialize Device Parameters | 91 | 1 0 0 1 0 0 0 1 |
| 3 | NOP | 00 | 0 0 0 0 0 0 0 0 |
| 1 | Read Buffer | E4 | 1 1 1 0 0 1 0 0 |
| 4 | Read DMA (retry) | C8 | 1 1 0 0 1 0 0 0 |
| 4 | Read DMA (no retry) | C9 | 1 1 0 0 1 0 0 1 |
| 5 | Read DMA Queued | C7 | 1 1 0 0 0 1 1 1 |
| 1 | Read Long (retry) | 22 | 0 0 1 0 0 0 1 0 |
| 1 | Read Long (no retry) | 23 | 0 0 1 0 0 0 1 1 |
| 1 | Read Multiple | C4 | 1 1 0 0 0 1 0 0 |
| 3 | Read Native Max Address | F8 | 1 1 1 1 1 0 0 0 |
| 1 | Read Sectors (retry) | 20 | 0 0 1 0 0 0 0 0 |
| 1 | Read Sectors (no retry) | 21 | 0 0 1 0 0 0 0 1 |
| 3 | Read Verify Sectors (retry) | 40 | 0 1 0 0 0 0 0 0 |
| 3 | Read Verify Sectors (no retry) | 41 | 0 1 0 0 0 0 0 1 |
| 3 | Recalibrate | 1x | 0 0 0 1 - - - - |
| 2 | Security Disable Password | F6 | 1 1 1 1 1 0 1 0 |
| 3 | Security Erase Prepare | F3 | 1 1 1 1 0 0 1 1 |
| 2 | Security Erase Unit | F4 | 1 1 1 1 0 1 0 0 |
| 3 | Security Freeze Lock | F5 | 1 1 1 1 0 1 0 1 |
| 2 | Security Set Password | F1 | 1 1 1 1 0 0 0 1 |
| 2 | Security Unlock | F2 | 1 1 1 1 0 0 1 0 |
| 3 | Seek | 7x | 0 1 1 1 - - - - |
| 5 | Service | A2 | 1 0 1 0 0 0 1 0 |
| 3 | Set Features | EF | 1 1 1 0 1 1 1 1 |
| 3 | Set Max Address | F9 | 1 1 1 1 1 0 0 1 |
| 3 | Set Multiple Mode | C6 | 1 1 0 0 0 1 1 0 |
| 3 | Sleep | E6 | 1 1 1 0 0 1 1 0 |
| 3 | Sleep* | 99 | 1 0 0 1 1 0 0 1 |
| 3 | SMART Disable Operations | B0 | 1 0 1 1 0 0 0 0 |
| 3 | SMART Enable/Disable Attribute Autosave | B0 | 1 0 1 1 0 0 0 0 |
| 3 | SMART Enable Operations | B0 | 1 0 1 1 0 0 0 0 |
| 3 | SMART Execute Off-line Data Collection | B0 | 1 0 1 1 0 0 0 0 |

Commands marked * are alternate command codes for previously defined commands.

Figure 82. Command set (1 of 2)

| Pro-tocol | Command | Code (Hex) | Binary Code Bit 7 6 5 4 3 2 1 0 |
|---|---|---|---|
| 3 | SMART Read Attribute Values | B0 | 1 0 1 1 0 0 0 0 |
| 1 | SMART Read Attribute Thresholds | B0 | 1 0 1 1 0 0 0 0 |
| 3 | SMART Return Status | B0 | 1 0 1 1 0 0 0 0 |
| 3 | SMART Save Attribute Values | B0 | 1 0 1 1 0 0 0 0 |
| 1 | SMART Read Log Sector | B0 | 1 0 1 1 0 0 0 0 |
| 2 | SMART Write Log Sector | B0 | 1 0 1 1 0 0 0 0 |
| 3 | SMART Enable/Disable Automatic Off-line Data Collection | B0 | 1 0 1 1 0 0 0 0 |
| 3 | Standby | E2 | 1 1 1 0 0 0 1 0 |
| 3 | Standby* | 96 | 1 0 0 1 0 1 1 0 |
| 3 | Standby Immediate | E0 | 1 1 1 0 0 0 0 0 |
| 3 | Standby Immediate* | 94 | 1 0 0 1 0 1 0 0 |
| 2 | Write Buffer | E8 | 1 1 1 0 1 0 0 0 |
| 4 | Write DMA (retry) | CA | 1 1 0 0 1 0 1 0 |
| 4 | Write DMA (no retry) | CB | 1 1 0 0 1 0 1 1 |
| 5 | Write DMA Queued | CC | 1 1 0 0 1 1 0 0 |
| 2 | Write Long (retry) | 32 | 0 0 1 1 0 0 1 0 |
| 2 | Write Long (no retry) | 33 | 0 0 1 1 0 0 1 1 |
| 2 | Write Multiple | C5 | 1 1 0 0 0 1 0 1 |
| 2 | Write Sectors (retry) | 30 | 0 0 1 1 0 0 0 0 |
| 2 | Write Sectors (no retry) | 31 | 0 0 1 1 0 0 0 1 |

Protocol :
1 : PIO data IN command
2 : PIO data OUT command
3 : Non data command
4 : DMA command
5 : DMA queued command
\+ : Vendor specific command

Commands marked * are alternate command codes for previously defined commands.

Figure 82. Command set (2 of 2)

| Command (Subcommand) | Command Code (Hex) | Feature Register (Hex) |
|---|---|---|
| S.M.A.R.T. Function | | |
| SMART Read Attribute Values | B0 | D0 |
| SMART Read Attribute Thresholds | B0 | D1 |
| SMART Enable/Disable Attribute Autosave | B0 | D2 |
| SMART Save Attribute Values | B0 | D3 |
| SMART Execute Off-line Data Collection | B0 | D4 |
| SMART Read Log | B0 | D5 |
| SMART Write Log | B0 | D6 |
| SMART Enable Operations | B0 | D8 |
| SMART Disable Operations | B0 | D9 |
| SMART Return Status | B0 | DA |
| SMART Enable/Disable Automatic Off-line | B0 | DB |
| Set Features | | |
| Enable Write Cache | EF | 02 |
| Set Transfer Mode | EF | 03 |
| 40 bytes of ECC apply on Read/Write Long | EF | 44 |
| Disable read look-ahead feature | EF | 55 |
| Enable release interrupt | EF | 5D |
| Disable reverting to power on defaults | EF | 66 |
| Disable write cache | EF | 82 |
| Enable read look-ahead feature | EF | AA |
| 4 bytes of ECC apply on Read/Write Long | EF | BB |
| Enable reverting to power on defaults | EF | CC |
| Disable release interrupt | EF | DD |

Figure 83. Command set (Subcommand)

Figure 82 on pages 103 and 104 shows the commands that are supported by the device. Figure 83 shows the subcommands that are supported by each command or feature.

The following symbols are used in the command descriptions:

**Output Registers**

**0** Indicates that the bit must be set to zero.

**1** Indicates that the bit must be set to one.

**D** The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.

**H** Head number. Indicates that the head number part of the Device/Head Register is an output parameter and should be specified.

**L** LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.

**R** Retry. Indicates that the Retry bit of the Command Register should be specified.

| | |
|---|---|
| **B** | Option Bit. Indicates that the Option Bit of the Sector Count Register should be specified. (This bit is used by Set Max Address command) |
| **V** | Valid. Indicates that the bit is part of an output parameter and should be specified. |
| **x** | Indicates that the hex character is not used. |
| **-** | Indicates that the bit is not used. |

**Input Registers**

| | |
|---|---|
| **0** | Indicates that the bit is always set to zero. |
| **1** | Indicates that the bit is always set to one. |
| **H** | Head number. Indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device. |
| **V** | Valid. Indicates that the bit is part of an input parameter and will be set to zero or one by the device. |
| **-** | Indicates that the bit is not part of an input parameter. |

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

## 12.1 Check Power Mode (E5h/98h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | V V V V V V V V |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 1 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 84. Check Power Mode Command (E5h/98h)

The Check Power Mode command reports whether the device is spun up and the media is available for immediate access.

**Input parameters from the device**

**Sector** The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the drive is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to zero.

## 12.2 Execute Device Diagnostic (90h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 - - - - - | | Device/Head | - - - - - - - - |
| Command | 1 0 0 1 0 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| V | V | V | V | V | V | V | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | 0 |

Figure 85. Execute Device Diagnostic Command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 69 on page 70 for the definition.

## 12.3 Flush Cache (E7h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | V V V V V V V V |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 1 1 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 86. Flush Cache Command (E7h)

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

## 12.4 Format Track (50h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 0 1 0 1 0 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | V | V | – | 0 | – | V |

Figure 87. Format Track Command (50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time the sector of data is not verified with read operation whether the sector of data is initialized correctly. Any data previously stored on the track will be lost.

The host may transfer a sector of data containing a format table to the device. But the device ignores the format table and writes zero to all sectors on the track regardless of the descriptors.

Since device performance is optimal at 1:1 interleave and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

**Output parameters to the device**

**Sector Number** In LBA mode this register specifies LBA address bits 0-7 to be formatted. (L=1)

**Cylinder High/Low** The cylinder number of the track to be formatted. (L=0)

In LBA mode this register specifies LBA address bits 8-15 (Low), 16-23 (High) to be formatted. (L=1)

**H** The head number of the track to be formatted. (L=0)

In LBA mode this register specifies LBA address bits 24-27 to be formatted. (L=1)

**Input parameters from the device**

| | |
|---|---|
| **Sector Number** | In LBA mode this register specifies current LBA address bits 0-7. (L=1) |
| **Cylinder High/Low** | In LBA mode this register specifies current LBA address bits 8-15 (Low), 16-23 (High) |
| **H** | In LBA mode this register specifies current LBA address bits 24-27. (L=1) |
| **Error** | The Error Register. An Abort error (ABT=1) will be returned when LBA is out of range. |

In LBA mode this command formats a single logical track including the specified LBA.

## 12.5 Format Unit (F7h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | 0 0 0 1 0 0 0 1 | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 L 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 1 1 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | 1 | 0 | 1 | 0 | 0 | – | 0 |

Figure 88. Format Unit Command (F7h)

The Format Unit command initializes all user data sectors after merging reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available immediately after command completion of this command and are used at next power-on reset or hard reset. Previous information of reassign and defect are erased from the device by executing this command.

Note that the Format Unit command initializes from LBA 0 to Native MAX LBA regardless of the setting by the Initialize Device Parameter (91h) command or the Set Max Address (F9h) command, so that the protected area defined by these commands is also initialized.

Security Erase Prepare (F3h) command should be completed just prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command the device aborts the Format Unit command.

All values in Feature register are reserved and any values other than 11h should not be put into Feature register.

This command does not request a data transfer.

Command execution time depends on drive capacity.

To determine the command time-out value refer to Word 89 of Identify Device data.

## 12.6 Identify Device (ECh)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 1 1 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 89. Identify Device Command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information described in the figure below.

- in the Content field indicates vendor specific use of those parameters.

| Word | Content | | Description |
|---|---|---|---|
| 00 | 045AH<br>or<br>045EH | | Drive classification, bit assignments:<br>15(=0): 1=ATAPI device, 0=ATA device<br>14– 8 : retired<br>7(=0): 1=removable cartridge drive<br>6(=1): 1=fixed drive<br>5– 3 : retired<br>2(=0): 1=soft sectored<br>1 : retired<br>0(=0): Reserved |
| 01 | xxxxH | | Number of cylinders in default translate mode |
| 02 | 37C8H | | Specific Configuration<br>37C8H: Need Set Feature for spin-up after power-up<br>Identify Device is incomplete |
| 03 | 00xxH | | Number of heads in default translate mode |
| 04 | 0 | • | Reserved |
| 05 | 0 | • | Reserved |
| 06 | 003FH | | Number of sectors per track in default translate mode |
| 07 | 0000H | • | Number of bytes of sector gap |
| 08 | 0000H | • | Number of bytes in sync field |
| 09 | 0000H | • | Reserved |
| 10-19 | XXXX | | Serial number in ASCII (0 = not specified) |
| 20 | 0003H | • | Controller type:<br>0003: dual ported, multiple sector buffer with look-ahead read |
| 21 | XXXXH | • | Buffer size in 512-byte increments |
| 22 | 0028H | • | Number of ECC bytes<br>(Vendor unique length selected via set feature cmd) |
| 23-26 | XXXX | | Microcode version in ASCII |
| 27-46 | XXXX | | Model number in ASCII |
| 47 | 8010H | | 15–8 80h<br>7–0 Maximum number of sectors that can be trans ferred per interrupt on Read and Write Multiple commands |
| 48 | 0000H | | Reserved |
| 49 | xF00H | | Capabilities, bit assignments:<br>15-14 (=0) Reserved<br>13 Standby timer<br>(=1) values as specified in ATA standard are supported<br>(=0) values are vendor specific<br>12 (=0) Reserved<br>11 (=1) IORDY supported<br>10 (=1) IORDY can be disabled<br>9 (=1) Reserved<br>8 (=0) Reserved |
| | | • | 7–0 (=0) Reserved |

Figure 90. Identify Device Information (1 of 6)

| Word | Content | Description |
|---|---|---|
| 50 | 400xH | Capabilities, bit assignments:<br>15-14(=01) Word 50 is valid<br>13– 1(=0) Reserved<br>0 Minimum value of Standby timer<br>(=0) less than 5 minutes<br>(=1) equal to or greater than 5 minutes |
| 51 | 0200H | PIO data transfer cycle timing mode |
| 52 | 0200H • | DMA data transfer cycle timing mode<br>Refer Word 62 and 63 |
| 53 | 0007H | Validity flag of the word<br>15–3(=0) Reserved<br>2(=1) 1=Word 88 are Valid<br>1(=1) 1=Word 64-70 are Valid<br>0(=1) 1=Word 54=58 are Valid |
| 54 | xxxxH | Number of current cylinders |
| 55 | xxxxH | Number of current heads |
| 56 | xxxxH | Number of current sectors per track |
| 57-58 | xxxxH | Current capacity in sectors<br>Word 57 specifies the low word of the capacity |
| 59 | 0xxxH | Current Multiple setting. Bit assignments:<br>15–9 (=0) Reserved<br>8 1= Multiple Sector Setting is Valid<br>7–0 xxh = Current setting for number of sectors |
| 60-61 | xxxxH | Total Number of User Addressable Sectors<br>Word 60 specifies the low word of the number |
| 62 | 0000H | |
| 63 | xx07H | Multiword DMA Transfer Capability<br>15-8 Multiword DMA transfer mode active<br>7-0 (=7) Multiword DMA transfer modes supported<br>(support mode 0.1 and 2) |
| 64 | 0003H | Flow Control PIO Transfer Modes Supported<br>15-8 (=0) Reserved<br>7-0 (=3) Advanced PIO Transfer Modes Supported<br>‘11’ = PIO Mode 3 and 4 Supported |
| 65 | 0078H | Minimum Multiword DMA Transfer Cycle Time Per Word<br>15-0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s) |
| 66 | 0078H | Manufacturer’s Recommended Multiword DMA Transfer Cycle Time<br>15-0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s) |
| 67 | 00F0H | Minimum PIO Transfer Cycle Time Without Flow Control<br>15–0 (=F0) Cycle time in nanoseconds (240ns,8.3MB/s) |
| 68 | 0078H | Minimum PIO Transfer Cycle Time Without Flow Control<br>15–0 (=78) Cycle time in nanoseconds (120ns, 16.6MB/s) |
| 69-74 | 0000H | Reserved |

Figure 90. Identify Device Information (2 of 6)

| Word | Content | Description |
|---|---|---|
| 75 | 00xxH | Queue depth<br>15- 5 Reserved<br>4- 0 Maximum queue depth |
| 76-79 | 0000H | Reserved |
| 80 | 003CH | Major version number<br>15- 0 (=3C)ATA-2, ATA-3, ATA/ATAPI-4 and ATA/ATAPI-5 |
| 81 | 0015H | Minor version number<br>15- 0 (=15)ATA/ATAPI-5 X3T13 1321D |
| 82 | 74EBH | Command set supported<br>15(=0) Reserved<br>14(=1) NOP command<br>13(=1) READ BUFFER command<br>12(=1) WRITE BUFFER command<br>11(=0) Reserved<br>10(=1) Host Protected Area feature set<br>9(=0) DEVICE RESET command<br>8(=0) SERVICE interrupt<br>7(=1) RELEASE interrupt<br>6(=1) LOOK AHEAD<br>5(=1) WRITE CACHE<br>4(=0) PACKET Command feature set<br>3(=1) Power management feature set<br>2(=0) Removable feature set<br>1(=1) Security feature set<br>0(=1) SMART feature set |
| 83 | 43EAH | Command set supported<br>15-14(=01) Word 83 is valid<br>13-10 (=0) Reserved<br>9 (=1) Automatic Acoustic mode<br>8 (=1) Set Max Security extension<br>7 (=1) Set Features Address Offset mode<br>6 (=1) SET FEATURES subcommand required to spin-up after power-up<br>5 (=1) Power-Up In Standby feature set supported<br>4 (=0) Removable Media Status Notification feature<br>3 (=1) Advanced Power management feature set<br>2 (=0) CFA feature set<br>1 (=1) READ/WRITE DMA QUEUED<br>0 (=0) DOWNLOAD MICROCODE command |
| 84 | 4000H | Command set/feature supported extension<br>15-14(=01) Word 83 is valid<br>13- 8 (=0) Reserved |

Figure 90. Identify Device Information (3 of 6)

| Word | Content | Description |
|---|---|---|
| 85 | xxxxH | Command set/feature enabled<br>15 Reserved<br>14 NOP command<br>13 READ BUFFER command<br>12 WRITE BUFFER command<br>11 Reserved<br>10 Host Protected Area feature set<br>9 DEVICE RESET command<br>8 SERVICE interrupt<br>7 RELEASE interrupt<br>6 LOOK AHEAD<br>5 WRITE CACHE<br>4 PACKET Command feature set<br>3 Power management feature set<br>2 Removable feature set<br>1 Security feature set<br>0 SMART feature set |
| 86 | xxxxH | Command set/feature enabled<br>15-10 Reserved<br>9 Automatic Acoustic Management enabled<br>8 Set Max Security extensions enabled<br>7 Set Features Address Offset mode<br>6 Set Features subcommand required to spin-up after power-up<br>5 Power-Up In Standby feature set enabled<br>4 Removable Media Status Notification feature<br>3 Advanced Power management feature set<br>2 CFA feature set<br>1 READ/WRITE DMA QUEUED<br>0 DOWNLOAD MICROCODE command |
| 87 | 4000H | Command set/feature default<br>15-14 (=01) Word 87 is valid<br>13- 0 ( =0) Reserved |
| 88 | xx3FH | Ultra DMA transfer modes<br>15- 8 (=xx) Current active Ultra DMA transfer mode<br>15-14 Reserved (=0)<br>13 Mode 5 1= Active 0= Not Active<br>12 Mode 4 1= Active 0= Not Active<br>11 Mode 3 1= Active 0= Not Active<br>10 Mode 2 1= Active 0= Not Active<br>9 Mode 1 1= Active 0= Not Active<br>8 Mode 0 1= Active 0= Not Active<br>7- 0 (=1F) Ultra DMA transfer mode supported<br>7-6 Reserved (=0)<br>5 Mode 5 1= Support<br>4 Mode 4 1= Support<br>3 Mode 3 1= Support<br>2 Mode 2 1= Support<br>1 Mode 1 1= Support<br>0 Mode 0 1= Support |

Figure 90. Identify Device Information (4 of 6)

| Word | Content | Description |
|---|---|---|
| 89 | xxxxH | Time required for Security Erase Unit completion<br>Time = value * 2 (minutes) |
| 90 | 0000H | Time required for Enhanced Security Erase completion |
| 91 | 0000H | Current advanced power management value |
| 92 | FFFEH | Master Password Revision Code |
| 93 | xxxxH | Hardware reset result. Bit assignments<br>15-14 (=01) Word 93 is valid<br>13 CBLID- status 1= Above Vih 0= Below Vil<br>12- 8 Dev 1 H/W reset result<br>12 Reserved<br>11 PDIAG- assertion 1= assert 0= not assert<br>10- 9 How to determine the device number<br>00=Reserved<br>01=Jumper<br>10=CSEL signal<br>11=Some other method<br>8 Shall be set to one if Dev 1<br>7- 0 Dev 0 H/W reset result<br>7 Reserved<br>6 Respond for Dev 1. 1= resp. 0= not resp.<br>5 DASP- detection. 1= detect 0= not detect<br>4 PDIAG- detection. 1= detect 0= not detect<br>3 Device 0 diag. 1=pass 0= fail<br>2- 1 How to determine the device number<br>00=Reserved 01=Jumper<br>10=CSEL signal 11=Some other method<br>0 Shall be set to one if Dev 0 |
| 94 | xxxxH | Current Advanced power management value<br>15- 8 Recommended Acoustic Management level<br>7- 0 Current Acoustic Management level |
| 95-126 | 0000H | Reserved |
| 127 | 0000H | Removable Media Status Notification feature set<br>0000H = Not supported |
| 128 | xxxxH | Device Lock Function. Bit assignments<br>15- 9 Reserved<br>8 Security Level 1= Maximum, 0= High<br>7- 6 Reserved<br>5 Enhanced erase 1= Support<br>4 Expire 1= Expired<br>3 Freeze 1= Frozen<br>2 Lock 1= Locked<br>1 Enable/Disable 1= Enable<br>0 Capability 1= Support |

Figure 90. Identify Device Information (5 of 6)

| Word | Content | Description |
|---|---|---|
| 129 | xxxxH • | Current Set Feature Option. Bit assignments<br>15- 4 Reserve<br>3 Auto reassign 1= Enable<br>2 Reverting 1= Enable<br>1 Read Look-ahead 1= Enable<br>0 Write Cache 1= Enable |
| 130-159 | xxxxH • | Reserved |
| 160-254 | 0000H | Reserved |
| 255 | xxA5H | 15- 8 Checksum. This value is the two's complement of the sum of all bytes in byte 0 through 510<br>7- 0 (A5) Signature |

Figure 90. Identify Device Information (6 of 6)

## 12.7 Idle (E3h/97h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 0 1 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 91. Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately and to set the auto power down time-out parameter (standby timer). And the timer then starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

**Output parameters to the device**

**Sector Count** Time-out Parameter. If it is zero, the automatic power down sequence is disabled. If it is non-zero, the automatic power down sequence is enabled. The time-out interval is shown below:

| Value | Time-out |
|---|---|
| 0 | Timer disabled |
| 1-240 | Value * 5 seconds |
| 241-251 | (Value-240) * 30 minutes |
| 252 | 21 minutes |
| 253 | 8 hours |
| 254 | 21 minutes 10 seconds |
| 255 | 21 minutes 15 seconds |

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the time-out interval expires with no drive access from the host. The time-out interval will be reinitialized if there is a drive access before the time-out interval expires.

## 12.8 Idle Immediate (E1h/95h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 92. Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect the auto power down time-out parameter.

## 12.9 Initialize Device Parameters (91h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | - - - - - - - - |
| Sector Count | V V V V V V V V | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D H H H H | | Device/Head | - - - - - - - - |
| Command | 1 0 0 1 0 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 93. Initialize Device Parameters Command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1 per cylinder. Words 54-58 in Identify Device Information reflect these parameters.

The parameters remain in effect until following events:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- Soft reset/Hard reset has occurred and the Set Feature option of CCh is set instead of 66h.

**Output parameters to the device**

**Sector Count**
The number of sectors per track. Zero does not mean there are 256 sectors per track, but that there are no sectors per track.

**H** The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

*Note: The following conditions need to be satisfied to avoid invalid number of cylinders beyond FFFFh.*

- (Total number of user addressable sectors)/((Sector Count)*(H+1)) = < FFFFh
- The total number of user addressable sectors is described in Identify Device command.

## 12.10 NOP (00h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | V V V V V V V V | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | Initial Value |
| Sector Number | - - - - - - - - | | Sector Number | Initial Value |
| Cylinder Low | - - - - - - - - | | Cylinder Low | Initial Value |
| Cylinder High | - - - - - - - - | | Cylinder High | Initial Value |
| Device/Head | 1 - 1 D - - - - | | Device/Head | Initial Value |
| Command | 0 0 0 0 0 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 94. NOP Command (00h)

This command always fails with an error. The device responds with command aborted.

**Output parameters to the device**

**Feature** Subcommand code

**00H** Abort any outstanding queue

**01H - FFH** Not abort any outstanding queue

The value of Sector Count, Sector Number, Cylinder High/Low, Device/Head set by host is not changed.

## 12.11 Read Buffer (E4h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 1 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 95. Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

## 12.12 Read DMA (C8h/C9h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 0 0 1 0 0 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| V | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 96. Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred. (L=1)

| | |
|---|---|
| **Cylinder High/Low** | The cylinder number of the first sector to be transferred. (L=0) |
| | In LBA mode this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1) |
| **H** | The head number of the first sector to be transferred. (L=0) |
| | In LBA mode this register specifies LBA bits 24-27 to be transferred. (L=1) |
| **R** | The retry bit. If it is set to one, then retries are disabled. |

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0) |
| | In LBA mode, this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0) |
| | In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the sector to be transferred. (L=0) |
| | In LBA mode, this register contains current LBA bits 24 - 27. (L=1) |

## 12.13 Read DMA Queued (C7h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | V V V V V V V V | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 0 0 0 1 1 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| V | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 97. Read DMA Queued Command (C7h)

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

Once the data transfer is begun, the device does not perform a bus release until the entire data transfer has been completed.

**Output parameters to the device**

| | |
|---|---|
| **Feature** | number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred. |
| **Sector Count** | bits 7 - 3 (Tag) contain the Tag for the command being delivered. |
| **Sector Number** | starting sector number or LBA address bits 7 - 0. |
| **Cylinder High/Low** | starting cylinder number or LBA address bits 23 - 8. |
| **H** | starting head number or LBA address bits 27 - 24. |

**Input parameters from the device on bus release**

**Sector Count** bits 7 - 3 (Tag) contain the Tag of the command being bus released.

bit 2 (REL) is set to one.

bit 1 (I/O) is cleared to zero.

bit 0 (C/D) is cleared to zero.

**Sector Number, Cylinder High/low, H** n/a.

**SRV** cleared to zero when the device performs a bus release. This bit is set to one when the device is ready to transfer data.

**Input parameters from the device on command complete**

**Sector Count** bits 7 - 3 (Tag) contain the Tag of the completed command.

bit 2 (REL) is cleared to zero.

bit 1 (I/O) is set to one.

bit 0 (C/D) is set to one.

**Sector Number, Cylinder High/Low, H**

sector address of unrecoverable error (applicable only when an unrecoverable error has occurred.)

**SRV** cleared to zero.

## 12.14 Read Long (22h/23h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | 0 0 0 0 0 0 0 1 | | Sector Count | - - - - - - - V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 0 0 1 0 0 0 1 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 98. Read Long Command (22h/23h)

The Read Long command read the designated one sector of data and the ECC bytes from disk media, then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time; the ECC bytes are transferred 8 bits at a time. The number of ECC bytes is 4 or 40 according to setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC, whatever is read is returned to the host.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. The Sector Count must be set to one.

**Sector Number** The sector number of the sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

| | |
|---|---|
| **H** | The head number of the sector to be transferred. (L=0) |
| | In LBA mode this register contains LBA bits 24-27. (L=1) |
| **R** | The retry bit. If set to one, then retries are disabled. |

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. |
| **Sector Number** | The sector number of the transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 24-27. (L=1) |

It should be noted that the device internally uses 40 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. Use of the 40 byte ECC mode is recommended for testing the effectiveness and integrity of the ECC functions of the device.

## 12.15 Read Multiple (C4h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 0 0 0 1 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 99. Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

**H** The head number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 24 - 27. (L=1)

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. This will be zero unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

## 12.16 Read Native Max Address (F8h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | V V V V V V V V |
| Cylinder Low | - - - - - - - - | | Cylinder Low | V V V V V V V V |
| Cylinder High | - - - - - - - - | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D - - - - | | Device/Head | - - - - H H H H |
| Command | 1 1 1 1 1 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 100. Read Native Max LBA/CYL (F8h)

This command returns the native max LBA/CYL of the drive which is not effected by Set Max Address command.

**Input parameters from the device**

**Sector Number** In LBA mode this register contains native max LBA bits 0 - 7. (L=1)

In CHS mode this register contains native max sector number. (L=0)

**Cylinder High/Low** In LBA mode this register contains native max LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

In CHS mode this register contains native max cylinder number. (L=0)

**H** In LBA mode this register contains native max LBA bits 24 - 27. (L=1)

In CHS mode this register contains native max head number. (L=0)

## 12.17 Read Sectors (20h/21h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 0 0 1 0 0 0 0 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 101. Read Sectors Command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

**H** The head number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 24 - 27. (L=1)

**R** The retry bit. If set to one, then retries are disabled.

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

## 12.18 Read Verify Sectors (40h/41h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 0 0 1 0 0 0 0 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 102. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the device. No data is transferred to the host.

The difference of Read Sectors command and Read Verify Sectors command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

**Output parameters to the device**

| | |
|---|---|
| **Sector Count** | The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified. |
| **Sector Number** | The sector number of the first sector to be transferred. (L=0) |
| | In LBA mode this register contains LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the first sector to be transferred. (L=0) |
| | In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the first sector to be transferred. (L=0) |
| | In LBA mode this register contains LBA bits 24 - 27. (L=1) |
| **R** | The retry bit. If set to one, then retries are disabled. |

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

## 12.19 Recalibrate (1xh)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 0 0 0 1 - - - - | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | V | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 103. Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0. If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

## 12.20 Security Disable Password (F6h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 1 1 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 104. Security Disable Password Command (F6h)

The Security Disable Password command disables the security mode feature ( device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in the figure below. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be reactivated later by setting User Password. This command should be executed in device unlock mode.

| Word | Description |
|---|---|
| 00 | Control Word<br>bit 0 : Identifier (1- Master, 0- User)<br>bit 1-15 : Reserved |
| 01-16 | Password (32 bytes ) |
| 17-255 | Reserved |

Figure 105. Password Information for Security Disable Password command

The device will compare the password sent from this host with that specified in the control word.

| | |
|---|---|
| **Identifier** | Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally. |

## 12.21 Security Erase Prepare (F3h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 0 1 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 106. Security Erase Prepare Command (F3h)

The Security Erase Prepare Command must be issued immediately before the Security Erase Unit Command to enable device erasing and unlocking.

The Security Erase Prepare Command must be issued immediately before the Format Unit Command. This command is to prevent accidental erasure of the device.

This command does not request to transfer data.

## 12.22 Security Erase Unit (F4h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 1 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 107. Security Erase Unit Command (F4h)

The Security Erase Unit command initializes all user data sectors and then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. The Host MAX LBA set by the Initialize Drive Parameter or the Set MAX Address command is ignored. So the protected area by the Set MAX Address command is also initialized.

This command requests to transfer a single sector data from the host including information specified in the figure below.

If the password does not match, the device rejects the command with an Aborted error.

| Word | Description |
|---|---|
| 00 | Control Word<br>bit 0 : Identifier (1- Master, 0- User)<br>bit 1 : Erase mode (1- Enhanced, 0- Normal)<br>Enhanced mode is not supported<br>bit 2-15: Reserved |
| 01-16 | Password ( 32 bytes ) |
| 17-255 | Reserved |

Figure 108. Erase Unit Information

**Identifier** Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). So after completing this command, all user data will be initialized to zero with write operation. At this time it is not verified with read operation whether the sector of data is initialized correctly. Also, the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command, the device aborts the security erase unit command.

This command disables the security mode feature (device lock function); however the master password is still stored internally within the device and may be reactivated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the password stored in the device for either the Master Password or the User Password. The device then erases all user data.

The execution time of this command is set in word 89 of Identify device information.

## 12.23 Security Freeze Lock (F5h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 1 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 109. Security Freeze Lock Command (F5h)

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by Power off.

The following commands are rejected when the device is in frozen mode:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

For details refer to Figure 79 on page 85.

## 12.24 Security Set Password (F1h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 110. Security Set Password Command (F1h)

The Security Set Password command enables security mode feature (device lock function) and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command and the device is not locked immediately. The device is locked after next power on reset or hard reset. When the MASTER password is set by this command, the master password is registered internally, but the device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in the figure below.

The data transferred controls the function of this command.

| Word | Description |
|---|---|
| 00 | Control Word<br>bit 0 : Identifier (1- Master, 0- User)<br>bit 1-7 : Reserved<br>bit 8 : Security level (1- Maximum, 0- High)<br>bit 9-15 : Reserved |
| 01-16 | Password ( 32 bytes ) |
| 17 | Master Password Revision Code<br>Valid if Word 0 bit 0 = 1 |
| 18-255 | Reserved |

Figure 111. Security Set Password Information

**Identifier** Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

**Security Level** Zero indicates High level, one indicates Maximum level. If the host sets High level and the password is forgotten, then the Master Password can be used to unlock the device. If the host sets Maximum level and the user password is forgotten, only a Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

**Password** The text of the password - all 32 bytes are always significant.

**Master Password Revision Code**
The revision code field is returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. The devi ce accepts the command with a value of 0000h or FFFFh in this field but does not change the Master Password Revision code.

The setting of the Identifier and Security level bits interact as follows:

**Identifier=User / Security level = High**
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The drive may then be unlocked by either the user password or the previously set master password.

**Identifier=Master / Security level = High**
This combination will set a master password but will NOT enable the security mode feature (lock function).

**Identifier=User / Security level = Maximum**
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The drive may then be unlocked by only the user password. The master password previously set is still stored in the drive but may NOT be used to unlock the device.

**Identifier=Master / Security level = Maximum**
This combination will set a master password but will NOT enable the security mode feature (lock function).

## 12.25 Security Unlock (F2h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 1 0 0 1 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | V | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 112. Security Unlock Command (F2h)

This command unlocks the password and causes the device to enter device unlock mode. If power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in the figure below.

If the Identifier bit is set to master and the drive is in high security mode, the password supplied will be compared with the stored master password. If the drive is in maximum security mode, the security unlock will be rejected.

If the Identifier bit is set to user, then the drive compares the supplied password with the stored user password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero, all password protected commands are rejected until a hard reset or a power off.

| Word | Description |
|---|---|
| 00 | Control Word<br>bit 0 : Identifier (1- Master, 0- User)<br>bit 1-15 : Reserved |
| 01-16 | Password ( 32 bytes ) |
| 17-255 | Reserved |

Figure 113. Security Unlock Information

**Identifier** Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password as this is the only reason that an abort error will be returned by the drive AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the drive, then another problem exists.

## 12.26 Seek (7xh)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - - - - - |
| Command | 0 1 1 1 - - - - | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 114. Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

**Output parameters to the device**

**Sector Number** In LBA mode this register specifies LBA address bits 0 - 7 for seek. (L=1)

**Cylinder High/Low** The cylinder number of the seek

In LBA mode this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) for seek. (L=1)

**H** The head number of the seek

In LBA mode this register specifies LBA address bits 24 - 27 for seek. (L=1)

**Input parameters from the device**

**Sector Number** In LBA mode this register contains current LBA bits 0 - 7. (L=1)

**Cylinder High/Low** In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

**H** In LBA mode this register contains current LBA bits 24 - 27. (L=1)

## 12.27 Service (A2h)

| Command Block Output Registers | |
|---|---|
| Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - |
| Feature | - - - - - - - - |
| Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - |
| Device/Head | - - - D - - - - |
| Command | 1 0 1 0 0 0 1 0 |

Figure 115. Service Command (A2h)

The Service command is used to provide data transfer and/or status of a command that was previously bus released.

**Output parameters to the device**

**D** Selected device

**Input parameters from the device**

Input from the device as a result of a Service command are described in the command description for the command for which Service is being requested.

## 12.28 Set Features (EFh)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | V V V V V V V V | | Error | see below |
| Sector Count | Note 1 | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 1 1 1 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 116. Set Features Command (EFh)

The Set Feature command is to establish the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

**Output parameters to the device**

**Feature** Destination code for this command.

**02H** Enable write cache

**03H** Set transfer mode based on value in sector count register

**05H** Enable Advanced Power Management

**06H** Enable Power-up in Standby feature set

**07H** Power-up in Standby feature set device spin-up

**09H** Enable Address Offset mode

**42H** Enable Automatic Acoustic Management

**44H** 40 bytes of ECC apply on Read Long/Write Long commands

**55H** Disable read look-ahead feature

**5DH** Enable release interrupt

**66H** Disable reverting to power on defaults

**82H** Disable write cache

**85H** Disable Advanced Power Management

**86H** Disable Power-up in Standby mode

**89H** Disable Address Offset mode

**AAH** Enable read look-ahead feature

**BBH** 4 bytes of ECC apply on Read Long/Write Long commands

**C2H** Disable Automatic Acoustic Management

**CCH** Enable reverting to power on defaults

**DDH** Disable release interrupt

*Note: After a power on reset of hard reset the device is set to the following features as default:*

| | |
|---|---|
| *Write cache* | *: Enable* |
| *ECC bytes* | *: 4 bytes* |
| *Read look-ahead* | *: Enable* |
| *Reverting to power on defaults* | *: Disable* |
| *Release interrupt* | *: Disable* |

## 12.28.1 Set Transfer mode

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

| | |
|---|---|
| PIO Default Transfer Mode | 00000 000 |
| PIO Default Transfer Mode, Disable IORDY | 00000 001 |
| PIO Flow Control Transfer Mode x | 00001 nnn (nnn=000,001,010,011,100) |
| Multiword DMA mode x | 00100 nnn (nnn=000,001,010) |
| Ultra DMA mode x | 01000 nnn (nnn=000,001,010,011,100,101) |

## 12.28.2 Write Cache

If the number of auto reassigned sector reaches reassignment capacity of the device, the write cache function will automatically be disabled. Although the device still accepts the Set Features command with Feature register = 02h without error, the write cache function remains disabled. For current write cache function status, please refer to Identify Device Information (word 85 or 129) by Identify Device command.

## 12.28.3 Advanced Power Management

When Feature register is 05h (=Enable Advanced Power Management), the Sector Count Register specifies the Advanced Power Management level.

C0 - FFh --- Aborted
80 - BFh --- The lowest power consumption mode is Low power Idle mode
40 - 7Fh --- The lowest power consumption mode is Low RPM standby mode
00 - 3Fh --- Aborted

### 12.28.3.1 Low Power Idle mode

Additional electronics are powered off and the heads are unloaded on the ramp. However the spindle is still rotated at the full speed.

### 12.28.3.2 Low RPM standby mode

The heads are unloaded on the ramp and the spindle is rotated at the 60-65% of the full speed.

When Feature register is 85h (=Disable Advanced Power Management), the deepest Power Saving becomes normal Idle.

## 12.28.4 Automatic Acoustic Management

When Feature register is 42h (=Enable Automatic Acoustic Management), the Sector Count Register specifies the Automatic Acoustic Management level.

| | |
|---|---|
| FF | --- Aborted |
| C0 - FEh | --- Set to Normal Seek mode |
| 80 - BFh | --- Set to Quiet Seek mode |
| 00 - 7Fh | --- Aborted |

The device preserves enabling or disabling of Automatic Acoustic Management and the current Automatic Acoustic Management level setting across all forms of reset, that is, Power on, Hardware, and Software Resets.

## 12.29 Set Max Address (F9h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - B | | Sector Count | - - - - - - - - |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 1 1 1 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 117. Set Max Address (F9h)

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command. the device receives this command without a prior Read Native Max Address command, the device regards as Set Max security extensions command according to feature register value. Valid features values are as shown below:

1. 01h indicates Set Max Set Password command
2. 02h indicates Set Max Lock command
3. 03h indicates Set Max Unlock command
4. 04h indicates Set Max Freeze LOCK command

This command overwrites the maximum number of Address of the drive in a range of actual device capacity. Once device receives this command, all accesses beyond that Address are rejected with setting ABORT bit in status register. Identify device command returns the Address which is set via this command as a default value.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

The device returns command aborted for a second non-volatile Set Max Address command until next power on or hardware reset.

The device returns command aborted during Set Max Locked mode or Set Max Frozen mode.

**Output parameters to the device**

| | |
|---|---|
| **B** | Option bit for selection whether nonvolatile or volatile. B = 0 is volatile condition. When B=1, MAX LBA/CYL which is set by Set Max LBA/CYL command is preserved by POR. When B=0, MAX LBA/CYL which is set by Set Max LBA/CYL command will be lost by POR. B = 1 is not valid when the device is in Address Offset mode. |
| **Sector Number** | In LBA mode this register contains LBA bits 0 - 7 which is to be set.(L=1) |
| | In CHS mode this register is ignored. (L=0) |
| **Cylinder High/Low** | In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High) which is to be set. (L=1) |
| | In CHS mode this register contains cylinder number which is to be set. (L=0) |
| **H** | In LBA mode this register contains LBA bits 24 - 27 which is to be set. (L=1) |
| | In CHS mode this register is ignored. (L=0) |

**Input parameters from the device**

| | |
|---|---|
| **Sector Number** | In LBA mode this register contains max LBA bits 0 - 7 which is set. (L=1) |
| | In CHS mode this register contains max sector number. (L=0) |
| **Cylinder High/Low** | In LBA mode this register contains max LBA bits 8 - 15 (Low), 16 - 23 (High) which is set. (L=1) |
| | In CHS mode this register contains max cylinder number which is set. (L=0) |
| **H** | In LBA mode this register contains max LBA bits 24 - 27 which is set. (L=1) |
| | In CHS mode this register contains max head number. (L=0) |

## 12.29.1 Set Max Set Password (Feature = 01h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | 0 0 0 0 0 0 0 1 | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | 1 - 1 D - - - - |
| Command | 1 1 1 1 1 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 118. Set Max Set Password

The device regards as Set Max Address command if this command is immediately preceded by a Read Native Max Address command.

This command requests a transfer of a single sector of data from the host including the information specified in Figure 119 on page 157.

The password is retained by the device until the next power cycle. When the device accepts this command, the device is in Set_Max_Unlocked state.

| Word | Description |
|---|---|
| 00 | Reserved |
| 01-16 | Password (32 byte) |
| 17-255 | Reserved |

Figure 119. Set Max Set Password data contents

## 12.29.2 Set Max Lock (Feature = 02h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | 0 0 0 0 0 0 1 0 | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | 1 - 1 D - - - - |
| Command | 1 1 1 1 1 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 120. Set Max Lock

The device regards as Set Max Address command if this command is immediately preceded by a Read Native Max Address command.

This command sets the device into Set_Max_Locked state. After this command is completed, any other Set Max commands except Set Max Unlock and Set Max Freeze Lock are rejected. The device remains in this state until a power cycle or the acceptance of a Set Max Unlock or Set Max Freeze Lock command.

## 12.29.3 Set Max Unlock (Feature = 03h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | 0 0 0 0 0 0 1 1 | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | 1 - 1 D - - - - |
| Command | 1 1 1 1 1 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 121. Set Max Unlock (F9h)

The device regards as Set Max Address command, if this command is immediately preceded by a Read Native Max Address command.

This command requests a transfer of a single sector of data from the host including the information specified in Figure 119 on page 157 with the stored SET MAX password.

If the password compare fails, the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero, all Set Max Unlock commands are rejected until a hard reset or a power off occurs.

If the password compare matches, then the device sets the Set_Max_Unlocked state and all Set Max commands are accepted.

## 12.29.4 Set Max Freeze Lock (Feature = 04h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | 0 0 0 0 0 1 0 0 | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | 1 - 1 D - - - - |
| Command | 1 1 1 1 1 0 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 122. Set Max Freeze Lock (F9h)

If the Set Max Freeze Lock command is immediately preceded by a Read Native Max Address command, this command is regarded as a Set Max Address command.

The Set Max Freeze Lock command sets the device to Set_Max_Frozen state. After command completion any subsequent Set Max commands are rejected. Commands disabled by Set Max Freeze Lock are the following:

1. Set Max Address
2. Set Max Set PASSWORD
3. Set Max Lock
4. Set Max Unlock

## 12.30 Set Multiple (C6h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 0 0 0 1 1 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 123. Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

If an invalid block size is specified, an Abort error will be returned to the host and Read Multiple and Write Multiple commands will be disabled.

**Output parameters to the device**

**Sector Count** The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

## 12.31 Sleep (E6h/99h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 1 1 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 124. Sleep Command (E6h/99h)

This command causes the device to enter Sleep Mode.

The device is spun down and the interface becomes inactive. If the device is already spun down, the spin down sequence is not executed.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

## 12.32 S.M.A.R.T. Function Set (B0h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | V V V V V V V V | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | 0 1 0 0 1 1 1 1 | | Cylinder Low | - - - - - - - - |
| Cylinder High | 1 1 0 0 0 0 1 0 | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 0 1 1 0 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | V | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 125. S.M.A.R.T. Function Set Command (B0h)

The S.M.A.R.T. Function Set command provides access to Attribute Values, Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which are selectable via the Features Register of the device when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the Features Register of the device before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

| Code | Subcommand |
|---|---|
| **D0h** | SMART Read Attribute Values |
| **D1h** | SMART Read Attribute Thresholds |
| **D2h** | SMART Enable/disable Attribute Autosave |
| **D3h** | SMART Save Attribute Values |
| **D4h** | SMART Execute Off-line Immediate |
| **D5h** | SMART Read Log Sector |
| **D6h** | SMART Write Log Sector |
| **D8h** | SMART Enable Operations |
| **D9h** | SMART Disable Operations |
| **DAh** | SMART Return Status |
| **DBh** | SMART Enable/Disable Automatic Off Line |

## 12.32.1 SMART Read Attribute Values (Subcommand D0h)

This subcommand returns the Attribute Values of the device to the host. Upon receipt of the SMART Read Attribute Values subcommand from the host the device saves any updated Attribute Values to the Attribute Data sectors and then transfers the 512 bytes of Attribute Value information to the host.

## 12.32.2 SMART Read Attribute Thresholds (Subcommand D1h)

This subcommand returns the Attribute Thresholds of the device to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host the device reads the Attribute Thresholds from the Attribute Threshold sectors and then transfers the 512 bytes of Attribute Thresholds information to the host.

## 12.32.3 SMART Enable/Disable Attribute Autosave (Subcommand D2h)

This subcommand enables and disables the Attribute Autosave feature of the device. The SMART Enable/Disable Attribute Autosave subcommand either allows the device to automatically save its updated Attribute Values to the Attribute Data Sector periodically or causes the Autosave feature to be disabled. The state of the Attribute Autosave feature (either enabled or disabled) will be preserved by the device across power cycle.

A value of 00h written by the host into the Sector Count Register of the device before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or power-down.

A value of F1h written by the host into the Sector Count Register of the device before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing the SMART Enable/Disable Attribute Autosave subcommand will not change the current Autosave status but the device will respond with the error code specified in Figure 136 on page 176.

The SMART Disable Operations subcommand disables the Autosave feature along with the SMART operations of the device.

Upon receipt of the subcommand from the host the device asserts BSY, enables or disables the Autosave feature, clears BSY, and asserts INTRQ.

## 12.32.4 SMART Save Attribute Values (Subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the Attribute Data sector of the device regardless of the state of the Attribute Autosave feature. Upon receipt of the SMART Save Attribute Values subcommand from the host the device writes any updated Attribute Values to the Attribute Data sector.

## 12.32.5 SMART Execute Off-line Immediate (Subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode.

The Sector Number register shall be set to specify the operation to be executed.

| Sector Number | Operation to be executed |
|---|---|
| **0** | Execute SMART off-line data collection routine immediately |
| **1** | Execute SMART Short self-test routine immediately in off-line mode |
| **2** | Execute SMART Extended self-test routine immediately in off-line mode |
| **127** | Abort off-line mode self-test routine |
| **129** | Execute SMART Short self-test routine immediately in captive mode |
| **130** | Execute SMART Extended self-test routine immediately in captive mode |

**Off-line mode**: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

**Captive mode:** When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine the device sets the execution result in the Self-test execution status byte (Figure 127 on page 167) and ATA registers as below and executes command completion.

| | |
|---|---|
| **Status** | Set ERR to one when self-test has failed |
| **Error** | Set ABRT to one when self-test has failed |
| **Cyl Low** | Set to F4h when self-test has failed |
| **Cyl High** | Set to 2Ch when self-test has failed |

## 12.32.6 SMART Read Log Sector (Subcommand D5h)

This command returns the specified log sector contents to the host.

The 512 bytes data are returned at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address.

| Log sector address | Content | Type |
|---|---|---|
| 01h | SMART Error Log | Read Only |
| 06h | SMART Self-test log | Read Only |
| 80h-9Fh | Host vendor specific | Read/Write |

Figure 126. Log sector addresses

## 12.32.7 SMART Write Log Sector (Subcommand D6h)

This command writes 512 bytes data to the specified log sector.

The 512 bytes data are transferred at a command and the Sector Count value shall be set to 1. The Sector Number shall be set to specify the log sector address as shown in the above figure. If Read Only log sector is specified, the device returns ABRT error.

## 12.32.8 SMART Enable Operations (Subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host the device enables S.M.A.R.T. capabilities and functions and then saves any updated Attribute Values to the Attribute Data sector.

## 12.32.9 SMART Disable Operations (Subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the attribute Autosave feature of the device. After receipt of this subcommand the device disables all S.M.A.R.T. operations.

Non-self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T. (either enabled or disabled) is preserved by the device across power cycles.

Upon receipt of the SMART Disable Operations subcommand from the host the device disables S.M.A.R.T. capabilities and functions and then saves any updated Attribute Values to the Attribute Data sector.

After receipt of the device of the SMART Disable Operations subcommand from the host all other S.M.A.R.T. subcommands – with the exception of SMART Enable Operations – are disabled and invalid and will be aborted by the device (including the SMART Disable Operations subcommand), returning the error code as specified in Figure 136 on page 176.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the Attribute Data Sectors of the device. If the device is re-enabled, these Attribute Values will be updated as needed upon receipt of a SMART Read Attribute Values or SMART Save Attribute Values command.

## 12.32.10 SMART Return Status (Subcommand DAh)

This command is used to communicate the reliability status of the device upon the request of the host. Upon receipt of the SMART Return Status subcommand the device saves any updated Pre-failure type Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, the device loads 4Fh into the Cylinder Low register and C2h into the Cylinder High register.

If the device detects a Threshold Exceeded Condition, the device loads F4h into the Cylinder Low register and 2Ch into the Cylinder High register.

## 12.32.11 SMART Enable/Disable Automatic Off-line (Subcommand DBh)

This subcommand enables and disables the optional feature that causes the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then saves this data to the nonvolatile memory of the device. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the Automatic Off-line Data Collection feature to be disabled.

A value of zero written by the host into the Sector Count register of the device before issuing this subcommand causes the feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F8h written by the host into the Sector Count register of the device before issuing this subcommand causes this feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vender specific and does not change the current Automatic Off-line Data Collection status, but the device may respond with the error code specified in Figure 136 on page 176.

## 12.32.12 Device Attributes Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Values subcommand. All multibyte fields shown in these data structures are in byte ordering, that is, the least significant byte occupies the lowest numbered byte address location in the field.

| Description | Byte | Offset | Value |
|---|---|---|---|
| Data Structure Revision Number | 2 | 00h | 0010h |
| 1st Device Attribute | 12 | 02h | |
| ... | .. | | |
| ... | .. | | |
| 30th Device Attribute | 12 | 15Eh | |
| Off–line data collection status | 1 | 16Ah | |
| Self–test execution status | 1 | 16Bh | |
| Total time in seconds to complete off–line data collection activity | 2 | 16Ch | |
| Vendor specific | 1 | 16Eh | |
| Off–line data collection capability | 1 | 16Fh | 1Bh |
| SMART capability | 2 | 170h | 0003h |
| SMART device error logging capability | 1 | 172h | 01h |
| Self–test failure check point | 1 | 173h | |
| Short self–test completion time in minutes | 1 | 174h | |
| Extended self–test completion time in minutes | 1 | 175h | |
| Reserved | 12 | 176h | |
| Vendor specific | 125 | 182h | |
| Data structure checksum | 1 | 1FFh | |
| | 512 | | |

Figure 127. Device Attributes Data Structure

### 12.32.12.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

### 12.32.12.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

| Description | Byte | Offset |
|---|---|---|
| Attribute ID Number (01h to FFh) | 1 | 00h |
| Status flags | 2 | 01h |
| Attribute Value (valid values from 01h to FDh) | 1 | 03h |
| Vendor Specific | 8 | 04h |
| Total Bytes | 12 | |

Figure 128. Individual Attribute Data Structure

**Attribute ID Numbers**

Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports the following Attribute ID Numbers.

| ID | Attribute Name |
|---|---|
| 0 | Indicates that this entry in the data structure is not used |
| 1 | Raw Read Error Rate |
| 2 | Throughput Performance |
| 3 | Spin Up Time |
| 4 | Start/Stop Count |
| 5 | Reallocated Sector Count |
| 7 | Seek Error Rate |
| 8 | Seek Time Performance |
| 9 | Power-on Hours Count |
| 10 | Spin Retry Count |
| 12 | Device Power Cycle Count |
| 192 | Power-off Retract Count |
| 193 | Load Cycle Count |
| 194 | Temperature |
| 196 | Reallocation Event Count |
| 197 | Current Pending Sector Count |
| 198 | Off-line Scan Uncorrectable Sector Count |
| 199 | Ultra DMA CRC Error Count |

**Status Flag definitions**

| Bit | Definition |
|---|---|
| **0** | Pre-failure/advisory bit |
| | **0** An attribute value less than or equal to its corresponding attribute threshold indicates an advisory condition where the usage or age of the device has exceeded its intended design life period. |
| | **1** An attribute value less than or equal to its corresponding attribute threshold indicates a pre-Failure condition where imminent loss of data is being predicted. |
| **1** | On-line Collective bit |
| | **0** The attribute value is updated only during Off-line testing. |
| | **1** The attribute value is updated during On-line testing or during both On-line and Off-line testing. |
| **2 - 5** | Vendor specific |
| **6 - 15** | Reserved (0) |

**Normalized values**
The device performs conversion of the raw attribute values to transform them into normalized values, which the host can then compare with the threshold values. A threshold is the excursion limit for a normalized attribute value.

### 12.32.12.3 Off-line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates Automatic Off-line Data Collection Status.

| Bit 7 | Automatic Off-line Data Collection Status |
|---|---|
| **1** | Automatic Off-line Data Collection is enabled. |
| **0** | Automatic Off-line Data Collection is disabled. |

Bits 0 thru 6 represents a hexadecimal status value reported by the device.

| Value | Definition |
|---|---|
| **0** | Off-line data collection never started |
| **2** | All segments completed without errors. |
| **4** | Off-line data collecting suspended by interrupting command |
| **5** | Off-line data collecting aborted by interrupting command |
| **6** | Off-line data collection aborted with fatal error |

### 12.32.12.4 Self-test execution status

| Bit | Definition |
|---|---|
| **0-3** | Percent Self-test remaining. An approximate percentage of the self-test routine remaining until completion; given in in ten percent increments. Valid values are 0 through 9 |
| **4-7** | Current Self-test execution status |
| | **0** The self-test routine completed without error or has not been run |
| | **1** The self-test routine aborted by the host |
| | **2** The self-test routine interrupted by the host with a hard or soft reset |
| | **3** The device was unable to complete the self-test routine due to a fatal error or unknown test error |
| | **4** The self-test routine completed with unknown element failure |
| | **5** The self-test routine completed with electrical element failure |
| | **6** The self-test routine completed with servo element failure |
| | **7** The self-test routine completed with read element failure |
| | **15** The self-test routine in progress |

### 12.32.12.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

### 12.32.12.6 Off-line data collection capability

| Bit | Definition |
|---|---|
| **0** | Execute Off-line Immediate implemented bit<br>**0** SMART Execute Off-line Immediate subcommand is not implemented<br>**1** SMART Execute Off-line Immediate subcommand is implemented |
| **1** | Enable/disable Automatic Off-line implemented bit<br>**0** SMART Enable/disable Automatic Off-line subcommand is not implemented<br>**1** SMART Enable/disable Automatic Off-line subcommand is implemented |
| **2** | Abort/restart off-line by host bit<br>**0** The device suspends off-line data collection activity after an interrupting command and resume it after some vendor specific event<br>**1** The device aborts off-line data collection activity upon receipt of a new command |
| **3** | Off-line Read Scanning implemented bit<br>**0** The device does not support Off-line Read Scanning<br>**1** The device supports Off-line Read Scanning |
| **4** | Self-test implemented bit<br>**0** Self-test routine is not implemented<br>**1** Self-test routine is implemented |
| **5-7** | Reserved (0) |

### 12.32.12.7 S.M.A.R.T. capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

| Bit | Definition |
|---|---|
| **0** | Pre-power mode attribute saving capability<br><br>If bit = 1, the device will save its Attribute Values prior to going into a power saving model (Standby or Sleep mode). |
| **1** | Attribute Autosave capability<br><br>If bit = 1, the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command. |
| **2-15** | Reserved (0) |

### 12.32.12.8 Error logging capability

| Bit | Definition |
|---|---|
| **7-1** | Reserved (0) |
| **0** | Error Logging support bit |

If bit = 1, the device supports the Error Logging

### 12.32.12.9 Self-test failure check point

This byte indicates the section of the self-test where the device detected a failure.

### 12.32.12.10 Self-test completion time
These bytes are the minimum time in minutes to complete the self-test.

### 12.32.12.11 Data Structure Checksum
The Data Structure Checksum is the two's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

## 12.32.13 Device Attribute Thresholds Data Structure
The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Thresholds. All multibyte fields shown in these data structures are in byte ordering, that is, the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

| Description | Byte | Offset | Value |
|---|---|---|---|
| Data Structure Revision Number | 2 | 00h | 0010h |
| 1st Device Attribute | 12 | 02h | |
| ... | .. | | |
| ... | .. | | |
| 30th Device Attribute | 12 | 15Eh | |
| Reserved | 18 | 16Ah | 00h |
| Vendor specific | 131 | 17Ch | 00h |
| Data structure checksum | 1 | 1FFh | |
| | 512 | | |

Figure 129. Device Attribute Thresholds Data Structure

### 12.32.13.1 Data Structure revision number
This value is the same as the value used in the Device Attributes Values Data Structure.

### 12.32.13.2 Individual Thresholds Data Structure
The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure is in the same order and correspond to the entries in the Individual Attribute Data Structure.

| Description | Byte | Offset |
|---|---|---|
| Attribute ID Number (01h to FFh) | 1 | 00h |
| Attribute Threshold | 1 | 01h |
| Reserved (00h) | 10 | 02h |
| Total bytes | 12 | |

Figure 130. Individual Threshold Data Structure

### 12.32.13.3 Attribute ID numbers
Attribute I D Numbers supported by the device are the same as Attribute Values Data Structures.

### 12.32.13.4 Attribute Threshold
These values are preset at the factory and are not intended to be changeable.

### 12.32.13.5 Data Structure Checksum
The Data Structure Checksum is the two's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

## 12.32.14 SMART error log sector
The following figure defines the 512 bytes that make up the SMART error log sector. All multibyte fields shown in these data structures are in byte ordering.

| Description | Byte | Offset |
|---|---|---|
| SMART error log version | 1 | 00h |
| Error log pointer | 1 | 01h |
| 1st error log data structure | 90 | 02h |
| 2nd error log data structure | 90 | 5Ch |
| 3rd error log data structure | 90 | B6h |
| 4th error log data structure | 90 | 110h |
| 5th error log data structure | 90 | 16Ah |
| Device error count | 2 | 1C4h |
| Reserved | 57 | 1C6h |
| Data structure checksum | 1 | 1FFh |
| | 512 | |

Figure 131. SMART error log sector

### 12.32.14.1 SMART error log version
This value is set to 01h.

### 12.32.14.2 Error log pointer
This points to the most recent error log data structure. Only values 1 through 5 are valid.

### 12.32.14.3 Device error count
This field contains the total number of errors. The value will not roll over.

### 12.32.14.4 Error log data structure

Data format of error data structure is shown below.

| Description | Byte | Offset |
|---|---|---|
| 1st command data structure | 12 | 00h |
| 2nd command data structure | 12 | 0Ch |
| 3rd command data structure | 12 | 18h |
| 4th command data structure | 12 | 24h |
| 5th command data structure | 12 | 30h |
| Error data structure | 30 | 3Ch |
| | 90 | |

Figure 132. Error log data structure

**Command data structure**

Data format of each command data structure is shown below.

| Description | Byte | Offset |
|---|---|---|
| Device Control register | 1 | 00h |
| Features register | 1 | 01h |
| Sector count register | 1 | 02h |
| Sector number register | 1 | 03h |
| Cylinder Low register | 1 | 04h |
| Cylinder High register | 1 | 05h |
| Device/Head register | 1 | 06h |
| Command register | 1 | 07h |
| Timestamp(ms from Power On) | 4 | 08h |
| | 12 | |

Figure 133. Command data structure

**Error data structure:** Data format of error data structure is shown below.

| Description | Byte | Offset |
|---|---|---|
| Reserved | 1 | 00h |
| Error register | 1 | 01h |
| Sector count register | 1 | 02h |
| Sector number register | 1 | 03h |
| Cylinder Low register | 1 | 04h |
| Cylinder High register | 1 | 05h |
| Device/Head register | 1 | 06h |
| Status register | 1 | 07h |
| Extended error data (vendor specific) | 19 | 08h |
| State | 1 | 1Bh |
| Life timestamp (hours) | 2 | 1Ch |
| | 30 | |

Figure 134. Error data structure

The state field contains a value indicating the device state when the command was issued to the device.

| Value | State |
|---|---|
| x0h | Unknown |
| x1h | Sleep |
| x2h | Standby |
| x3h | Active/Idle |
| x4h | SMART Off-line or Self-test |
| x5h-xAh | Reserved |
| xBh-xFh | Vendor specific |

The value of 'x' is vendor specific.

## 12.32.15 Self-test log data structure

The following figure defines the 512 bytes that make up the Self-test log sector. All multibyte fields shown in these data structures are in byte ordering.

| Description | Byte | Offset |
|---|---|---|
| Data structure revision | 2 | 00h |
| Self-test number | 1 | n*18h+02h |
| Self-test execution status | 1 | n*18h+03h |
| Life time power on hours | 2 | n*18h+04h |
| Self-test failure check point | 1 | n*18h+06h |
| LBA of first failure | 4 | n*18h+07h |
| Vendor specific | 15 | n*18h+0Bh |
| ... | | |
| Vendor specific | 2 | 1FAh |
| Self-test log pointer | 1 | 1FCh |
| Reserved | 2 | 1FDh |
| Data structure checksum | 1 | 1FFh |
| | 512 | |

*Note: n is 0 through 20*

Figure 135. Self-test log data structure

The data structure contains the descriptor of Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable of containing up to 21 descriptors.

After 21 descriptors have been recorded, the oldest descriptor will be overwritten with a new descriptor.

The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there is descriptor(s) the value is 1 through 21.

## 12.32.16 Error reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

| Error condition | Status Register | Error Register |
|---|---|---|
| A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers. | 51h | 04h |
| A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device. | 51h | 04h |
| A S.M.A.R.T. FUNCTION SET command subcommand other than SMART ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. Disabled" state. | 51h | 04h |
| The device is unable to read its Attribute Values or Attribute Thresholds data structure. | 51h | 10h or 40h |
| The device is unable to write to its Attribute Values data structure. | 51h | 10h or 01h |

Figure 136. S.M.A.R.T. Error Codes

## 12.33 Standby (E2h/96h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 0 1 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 137. Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately and to set the auto power down time-out parameter (standby timer).

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the drive will respond to commands but there is a delay while waiting for the spindle to reach operating speed.

The automatic power down sequence is enabled and the timer starts counting down when the drive returns to Idle mode.

**Output Parameters To The Drive**

**Sector Count**

Time-out Parameter. If it is 0, the automatic power down sequence is disabled. If it is nonzero, the automatic power down sequence is enabled. The time-out interval is shown below:

| Value | Time-out |
|---|---|
| 0 | Timer disabled |
| 1-240 | Value * 5 seconds |
| 241-251 | Value-240) * 30 minutes |
| 252 | 21 minutes |
| 253 | 8 hours |
| 254 | 21 minutes 10 seconds |
| 255 | 21 minutes 15 seconds |

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the time-out interval expires with no drive access from the host. The time-out interval will be reinitialized if there is a drive access before the time-out interval expires.

## 12.34 Standby Immediate (E0h/94h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 - 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 0 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 138. Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down time-out parameter.

## 12.35 Write Buffer (E8h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | - - - - - - - - | | Sector Count | - - - - - - - - |
| Sector Number | - - - - - - - - | | Sector Number | - - - - - - - - |
| Cylinder Low | - - - - - - - - | | Cylinder Low | - - - - - - - - |
| Cylinder High | - - - - - - - - | | Cylinder High | - - - - - - - - |
| Device/Head | 1 – 1 D - - - - | | Device/Head | - - - - - - - - |
| Command | 1 1 1 0 1 0 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | 0 | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | – | – | 0 | – | V |

Figure 139. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized so that sequential Write Buffer and Read Buffer commands access the same 512 bytes within the buffer.

## 12.36 Write DMA (CAh/CBh)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 0 0 1 0 1 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| V | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | V | V | – | 0 | – | V |

Figure 140. Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device. The data is then written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that the data transfer has terminated and the status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. If 0 is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

| | |
|---|---|
| **H** | The head number of the first sector to be transferred. (L=0)<br>In LBA mode this register contains LBA bits 24 - 27. (L=1) |
| **R** | The retry bit. If set to 1, then retries are disabled. It is ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.) |

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0)<br>In LBA mode this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0)<br>In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the last transferred sector. (L=0)<br>In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

## 12.37 Write DMA Queued (CCh)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | V V V V V V V V | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 0 0 1 1 0 0 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| V | 0 | 0 | V | 0 | V | 0 | V |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | 0 | V | – | 0 | – | V |

Figure 141. Write DMA Queued Command (CCh)

This command executes in a similar manner to a WRITE DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

Once the data transfer has begun, the device does not perform a bus release until the entire data transfer has been completed.

**Output parameters to the device**

| | |
|---|---|
| **Feature** | number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred. |
| **Sector Count** | bits 7 - 3 (Tag) contain the Tag for the command being delivered. |
| **Sector Number** | starting sector number or LBA address bits 7 - 0. |
| **Cylinder High/Low** | starting cylinder number or LBA address bits 23 - 8. |
| **H** | starting head number or LBA address bits 27 - 24. |

**Input parameters from the device on bus release**

**Sector Count** bits 7 - 3 (Tag) contain the Tag of the command being bus released.

bit 2 (REL) is set to one.

bit 1 (I/O) is cleared to zero.

bit 0 (C/D) is cleared to zero.

**Sector Number, Cylinder High/Low, H** n/a.

**SRV** cleared to zero when the device performs a bus release. This bit is set to 1 when the device is ready to transfer data.

**Input parameters from the device on Command Complete**

**Sector Count** bits 7 - 3 (Tag) contain the Tag of the completed command.

bit 2 (REL) is cleared to 0.

bit 1 (I/O) is set to one.

bit 0 (C/D) is set to one.

**Sector Number, Cylinder High/Low, H**

sector address of unrecoverable error (applicable only when unrecoverable error has occurred.)

**SRV** cleared to 0.

## 12.38 Write Long (32h/33h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | 0 0 0 0 0 0 0 1 | | Sector Count | - - - - - - - V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 0 0 1 1 0 0 1 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | V | V | – | 0 | – | V |

Figure 142. Write Long Command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated sector from the host to the device. The data and the ECC bytes are then written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time; the ECC bytes are transferred 8 bits at a time. The number of ECC bytes is 4 or 40 according to the setting of the Set Feature option. The default number after power-on is 4 bytes.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. The Sector Count must be set to one.

**Sector Number** The sector number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

**H** The head number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

**R** The retry bit. If set to one, then retries are disabled.

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. |
| **Sector Number** | The sector number of the sector to be transferred. (L=0) |
| | In LBA mode this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the sector to be transferred. (L=0) |
| | In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the sector to be transferred. (L=0) |
| | In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

The drive internally uses 40 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that the 40 byte ECC mode be used for all tests to confirm the operation of the ECC hardware. Unexpected results may occur if such testing is performed using the 4 byte mode.

## 12.39 Write Multiple (C5h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 1 1 0 0 0 1 0 1 | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | V | V | – | 0 | – | V |

Figure 143. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, the data is written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

**H** The head number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 24 - 27. (L=1)

**Input Parameters From The Device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current 1.5 LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

## 12.40 Write Sectors (30h/31h)

| Command Block Output Registers | | | Command Block Input Registers | |
|---|---|---|---|---|
| Register | 7 6 5 4 3 2 1 0 | | Register | 7 6 5 4 3 2 1 0 |
| Data | - - - - - - - - | | Data | - - - - - - - - |
| Feature | - - - - - - - - | | Error | see below |
| Sector Count | V V V V V V V V | | Sector Count | V V V V V V V V |
| Sector Number | V V V V V V V V | | Sector Number | V V V V V V V V |
| Cylinder Low | V V V V V V V V | | Cylinder Low | V V V V V V V V |
| Cylinder High | V V V V V V V V | | Cylinder High | V V V V V V V V |
| Device/Head | 1 L 1 D H H H H | | Device/Head | - - - - H H H H |
| Command | 0 0 1 1 0 0 0 R | | Status | see below |

| Error Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC | UNC | 0 | IDN | 0 | ABT | T0N | AMN |
| 0 | 0 | 0 | V | 0 | V | 0 | 0 |

| Status Register | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BSY | RDY | DF | DSC | DRQ | COR | IDX | ERR |
| 0 | V | V | V | – | 0 | – | V |

Figure 144. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device; the data is then written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

**Output parameters to the device**

**Sector Count** The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

**Sector Number** The sector number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 0 - 7. (L=1)

**Cylinder High/Low** The cylinder number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

**H** The head number of the first sector to be transferred. (L=0)

In LBA mode this register contains LBA bits 24 - 27. (L=1)

**R** The retry bit. If it is set to one, retries are disabled. If it is ignored, write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

**Input parameters from the device**

| | |
|---|---|
| **Sector Count** | The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs. |
| **Sector Number** | The sector number of the last transferred sector. (L=0) |
| | In LBA mode, this register contains current LBA bits 0 - 7. (L=1) |
| **Cylinder High/Low** | The cylinder number of the last transferred sector. (L=0) |
| | In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1) |
| **H** | The head number of the last transferred sector. (L=0) |
| | In LBA mode this register contains current LBA bits 24 - 27. (L=1) |

# 13.0 Timings

The timing of BSY and DRQ in Status Register are shown in the figure below.

| Function | Interval | Start | Stop | Time-out |
|---|---|---|---|---|
| Power On | Device Busy After Power On | Power On | Status Register BSY=1 | 400 ns |
| | Device Ready After Power On | Power On | Status Register BSY=1 and RDY=1 | 31 sec |
| Software Reset | Device Busy After Software Reset | Device Control Register RST=1 | Status Register BSY=1 | 400 ns |
| | Device Ready After Software Reset | Device Control Register RST=0 After RST=1 | Status Register BSY=0 and RDY=1 | 31 sec |
| Hard Reset | Device Busy After Hard Reset | Bus RESET Signal Asserted | Status Register BSY=1 | 400 ns |
| | Device Ready After Hard Reset | Bus RESET Signal Asserted | Status Register BSY=0 and RDY=1 | 31 sec |
| Data In Command | Device Busy After Command Code Out | OUT To Command Register | Status Register BSY=1 | 400 ns |
| | Interrupt, DRQ For Data Transfer In | Status Register BSY=1 | Status Register BSY=0 & DRQ=1, Interrupt | 30 sec |
| | Device Busy After Data Transfer In | 256th Read From Data Register | Status Register BSY=1 | 10 us |
| Data Out Command | Device Busy After Command Code Out | OUT to Command Register | Status Register BSY=1 | 400 ns |
| | Data Request For Data Transfer Out | Status Register BSY=1 | Status Register BSY=0 and DRQ=1 | 700 us |
| | Device Busy After Data Transfer Out | 256th Write From Data Register | Status Register BSY=1 | 5 us |
| | Interrupt For Data Transfer Out | Status Register BSY=1 | Status Register BSY=0 and RDY=1 Interrupt | 30 sec |
| Non-Data Command | Device Busy After Command Code Out | OUT to Command Register | Status Register BSY=1 | 400 ns |
| | Interrupt For Command Complete | Status Register BSY=1 | Interrupt | 30 sec |
| DMA Data Transfer Command | Device Busy After Command Code Out | OUT to Command Register | Status Register BSY=1 | 400 ns |

Figure 145. Time-out values

Command category is referred to in 11.0 , “Command Protocol” on page 95.

The abbreviations "ns", "us", "ms," and "sec" mean nanoseconds, microseconds, milliseconds, and seconds, respectively.

If the host detects a timeout while waiting for a response from the device, we recommend that the host system execute a Soft reset and then retry the command.

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# 14.0 Appendix

## 14.1 Commands Support Coverage

Following table is provided to facilitate the understanding of DTLA-3XXXXX command support coverage comparing to the ATA-5 defined command set. The column entitled 'Implementation' shows the capability of DTLA-3XXXXX for those commands.

| Command Code | Command Name | Implementation for DTLA-3XXXXX | ATA-5 Category Type |
|---|---|---|---|
| 00h | NOP | Yes | Optional |
| 03h | CFA REQUEST EXTENDED ERROR CODE | No | Optional (7) |
| 08h | DEVICE RESET | No | Optional (7) |
| 1xh | RECALIBRATE | Yes | Obsoleted |
| 20h | READ SECTOR(S) (w/ retry) | Yes | Mandatory |
| 21h | READ SECTOR(S) (w/o retry) | Yes | Obsoleted |
| 22h | READ SECTOR(S) (w/ retry) | Yes | Obsoleted |
| 23h | READ LONG (w/o retry) | Yes | Obsoleted |
| 30h | WRITE SECTOR(S) (w/ retry) | Yes | Mandatory |
| 31h | WRITE SECTOR(S) (w/o retry) | Yes | Obsoleted |
| 32h | WRITE LONG (w/ retry) | Yes | Obsoleted |
| 33h | WRITE LONG (w/o retry) | Yes | Obsoleted |
| 38h | CFA TRANSLATE SECTORS W/O ERASE | No | Optional (7) |
| 3Ch | WRITE VERIFY (2) | Vendor specific | Obsoleted |
| 40h | READ VERIFY SECTOR (S) (w/retry) | Yes | Mandatory |
| 41h | READ VERIFY SECTORS (S) (w/o retry) | Yes | Obsoleted |
| 50h | FORMAT TRACK | Yes | Obsoleted |
| 7xh | SEEK | Yes | Mandatory |
| 87h | CFA TRANSLATE SECTORS | No | Optional |
| 90h | EXECUTE DEVICE DIAGNOSTIC | Yes | Mandatory |
| 91h | INITIALIZE DEVICE PARAMETERS | Yes | Mandatory |
| 92h | DOWNLOAD MICROCODE | Reserved | Optional |
| 94h–99h | Reserved | Reserved | Reserved |
| A0h | PACKET | No | Not to be used |
| A1h | IDENTIFY PACKET DEVICE | No | Not to be used |
| A2H | SERVICE | Yes | Not to be used |
| B0h | S.M.A.R.T. FUNCTION SET | Yes | Optional – (5) |
| C0h | CFA ERASE SECTORS | No | Optional |
| C4h | READ MULTIPLE | Yes | Mandatory |
| C5h | WRITE MULTIPLE | Yes | Mandatory |
| C6h | SET MULTIPLE MODE | Yes | Mandatory |
| C7h | READ DMA QUEUED | Yes | Optional |
| C8h | READ DMA (w/ retry) | Yes | Mandatory |
| C9h | READ DMA (w/o retry) | Yes | Obsoleted |

Figure 146. Command coverage (1 of 2)

| Command Code | Command Name | Implementation for DTLA-3XXXXX | ATA-5 Command Type |
|---|---|---|---|
| CAh | WRITE DMA (w/ retry) | Yes | Mandatory |
| CBh | WRITE DMA (w/o retry) | Yes | Obsoleted |
| CCh | WRITE DMA QUEUED | Yes | Optional |
| CDh | CFA WRITE MULTIPLE W/O ERASE | No | Optional – (7) |
| DAh | GET MEDIA STATUS | No | Optional (7) |
| DEh | MEDIA LOCK | No | Optional (7) |
| DFh | MEDIA UNLOCK | No | Optional (7) |
| E0h | STANDBY IMMEDIATE | Yes | Mandatory |
| E1h | IDLE IMMEDIATE | Yes | Mandatory |
| E2h | STANDBY | Yes | Mandatory |
| E3h | IDLE | Yes | Mandatory |
| E4h | READ BUFFER | Yes | Optional |
| E5h | CHECK POWER MODE | Yes | Mandatory |
| E6h | SLEEP | Yes | Mandatory |
| E7h | FLUSH CACHE | Yes | Mandatory |
| E8h | WRITE BUFFER | Yes | Optional |
| ECh | IDENTIFY DEVICE | Yes | Mandatory |
| EDh | MEDIA EJECT | No | Optional (7) |
| EEh | IDENTIFY DEVICE DMA | No | Obsoleted |
| EFh | SET FEATURES | Yes | Mandatory |
| F0h | SENSE CONDITION | Vendor specific | Vendor specific |
| F1h | SECURITY SET PASSWORD | Yes | Optional (6) |
| F2h | SECURITY UNLOCK | Yes | Optional (6) |
| F3h | SECURITY ERASE PREPARE | Yes | Optional (6) |
| F4h | SECURITY ERASE UNIT | Yes | Optional (6) |
| F5h | SECURITY FREEZE LOCK | Yes | Optional (6) |
| F6h | SECURITY DISABLE PASSWORD | Yes | Optional (6) |
| F7h | FORMAT UNIT | Vendor specific | Vendor specific |
| F8h | READ NATIVE MAX ADDRESS | Yes | Optional |
| F9h | SET MAX ADDRESS | Yes | Optional |
| FAh | ENABLE/DISABLE DELAYED WRITE | No | Vendor specific |
| FBh | Vendor specific | Reserved | Vendor specific |
| | Reserved: all remaining codes | Reserved | Reserved |

*Note:*

(1) *These commands have two command codes and appear in this table twice, once for each command code.*

(2) *The WRITE VERIFY command implemented vendor specific. The operation is same as WRITE SECTORS and verification is not performed.*

(3) *Protected Area Feature Set*

(4) *Power Management Feature Set*

(5) *S.M.A.R.T. Function Set*

(6) *Security Mode Feature Set*

(7) *Removable*

Figure . Command coverage (2 of 2)

## 14.2 SET FEATURES Command Support Coverage

The following table provides a list of Feature Registers, Feature Names, and implementation for the DTLA-3XXXXX models. The "Implementation" column indicates with a "Yes" or "No" whether or not the DTLA-3XXXXX models have the capability of executing the command in comparison to the ATA/ATAPI-5 defined command set. For detailed operation see 12.28, "Set Features (EFh)" on page 152.

| Features Register | Features Name | Implementation for DTLA-3XXXXX |
|---|---|---|
| 02h | Enable write cache | Yes |
| 03h | Set transfer mode | Yes |
| 05h | Enable Advanced Power Management | Yes |
| 06h | Enable Power-up in Standby feature set | Yes |
| 07h | Power-up in Standby feature set device spin-up | Yes |
| 09h | Enable Address Offset mode | Yes |
| 42h | Enable Automatic Acoustic Management | Yes |
| 44h | Set vendor specific bytes ECC | Yes |
| 55h | Disable read look–ahead feature | Yes |
| 5Dh | Enable release interrupt | Yes |
| 5Eh | Enable SERVICE interrupt | No |
| 66h | Disable reverting to power on defaults | Yes |
| 82h | Disable write cache | Yes |
| 85h | Disable Advanced Power Management | Yes |
| 86h | Disable Power up in Standby mode | Yes |
| 89h | Disable Address Offset mode | Yes |
| 95h | Enable Media Status Notification | No |
| AAh | Enable read look–ahead feature | Yes |
| BBh | Set 4 bytes ECC | Yes |
| C2h | Disable Automatic Acoustic Management | Yes |
| CCh | Enable reverting to power on defaults | Yes |
| DDh | Disable release interrupt | Yes |
| EEh | Disable SERVICE interrupt | No |
| others | Reserved | Reserved |

Figure 147. SET FEATURES command coverage

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