SECTION 1. GENERAL

1.1 Logic Set

Circuit Type	Function	Number per Package
A	2 input AND-INVERT	4
B	4 " " "	2
C	2 + 2 AND-OR-INVERT	2
D	D BISTABLE	2
E	JK BISTABLE	1
F	8 input AND-INVERT	1
G	4 input POWER AND-INVERT	2

1.2 Logic Rules

1.2.1 Virtual Gates

Outputs of elements may not be commoned to provide a virtual gate.

1.2.2 Unused Inputs

Unused inputs to gates must be connected to the input which is used. This does not increase the loading on the previous circuit but not more than four inputs may be commoned. The use of spare inputs for commissioning purposes etc. is covered in para. 1.4. Where an unused input cannot be paralleled with another input, as with say the S and R lines to a bistable, then they must either be connected to a suitable positive level, to the output of a gate held permanently in the high state or, if it is logically appropriate, grounded.

1.2.3 Fan-out

The fan-out of all the elements in the set, with the exception of the power gate Type G, is limited to 9. Where a greater fan-out is required the power gates must be used and the fan-out of this gate is limited to 30.

1.3 Power Consumption

1.3.1 All the circuits operate with a single power supply line of +5V $\pm$ 0.25V.

1.3.2 The maximum value of the mean power supply current taken per package is given in later sections of this document for each of the package types. This max. value assumes that the gates are being operated on a 50 : 50 'ON' to 'OFF' ratio at a low frequency. If under any conditions the number of gates in the 'ON' state is

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higher than the number in the 'OFF' state, then the power supply requirements are increased by a % which can be calculated by taking the % of the gates in the ON state and subtracint 50%. For higher frequencies these figures should be increased at the rate of 12.5% per mega-cycle. (The mean operating frequency of the circuits used in the PF50 test bed appears to be very low).

1.3.3 The chances of getting a set of 1000 or so packages all taking the maximum value of current allowed by the circuit specification are obviously remote. How close any set of 1000 will come to the maximum figures has yet to be determined. Tentatively it is proposed that power supplies should be designed to cater for 75% of these maximum figures.

1.4 Forcing of Logical Conditions for the purpose of commissioning or fault finding

1.4.1 While the circuits are protected against accidental shorting to ground of the outputs, they should not be so shorted for long periods of time. It follows that this should not be done for the purpose of commissioning or as a means of finding faults.

1.4.2 Logical conditions may be forced by disconnecting the input of a gate from the previous element and then connecting it to either ground by a suitable + voltage. An extender board is being provided which will have alterable links for this purpose. The resistor values on this board will be such that damage to circuits will be minimised if by mistake the output rather than the input of a circuit is so linked to ground or the positive voltage.

1.4.3 Where it is desired to provide facilities for forcing logical conditions without the use of extender boards, spare inputs to gates may be connected to a potential divider across the supply and these may thereafter be taken to the '0' level by grounding them.

1.5 Planning Rules

1.5.1 These planning rules will apply to all the circuits in the family.

1.5.2 The circuit packages will normally be soldered into printed boards and these boards plugged into edge connectors and connected together with back-wiring. In the case of small boards housing a few modules, these are likely to be double sided printed boards in order to minimise costs. With large arrays of modules a four layer board construction is to be preferred as this provides

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better earthing arrangements and minimises crosstalk between conductors on the board. Low impedance earth paths between packages is very important. On the small double sided boards additional earthing straps are necessary to minimise the earth impedance. The back plane will be in the form of a continuous copper sheet to maintain a low impedance between connectors. It may be that rules will have to be introduced for the wiring layout on the boards, but for the moment these rules are confined to the back-wiring and assume that reasonable precautions are taken with the board wiring.

1.5.3 The back-wiring will be in the form of open wiring or twisted pairs. Open wires are restricted to a string length of 15 inches. Twisted pairs may be used up to a string length of 4 feet but the distance between the output of one element and the input of another should not normally exceed 2 feet.
In calculating the maximum permitted length of a conductor which is partly open and partly twisted, the twisted length shall be divided by four and added to the length of the open wire so that the total does not exceed 15 inches.

1.5.4 Where the distance between the driving and the receiving element exceeds two feet, then coaxial cable driven by the power element type G and terminated as specified in para 2.7. shall be used.

1.6 Voltage Levels

1.6.1 The acceptable output voltage levels of the circuits, as measured between the output pin and the earth pin of that circuit are:-

High	+2.4	to	+4.0 volts
Low	-0.5	to	+0.4 volts.

1.6.2 The acceptable input voltages to the circuits, as measured between the input pin and the earth pin of that circuit are:-

High	+1.6	to	+4.0 volts
Low	-0.5	to	+1.05 volts.

It is to be expected that the input voltages will only approach these limits under pulse noise conditions.

1.6.3 The above limits apply over the device temperature range +10 to +60°C and even the worst circuits should operate with better limits at normal temperatures. The average circuits will be appreciably better.

1.7 Timing

All timing information in this document is given in the form of

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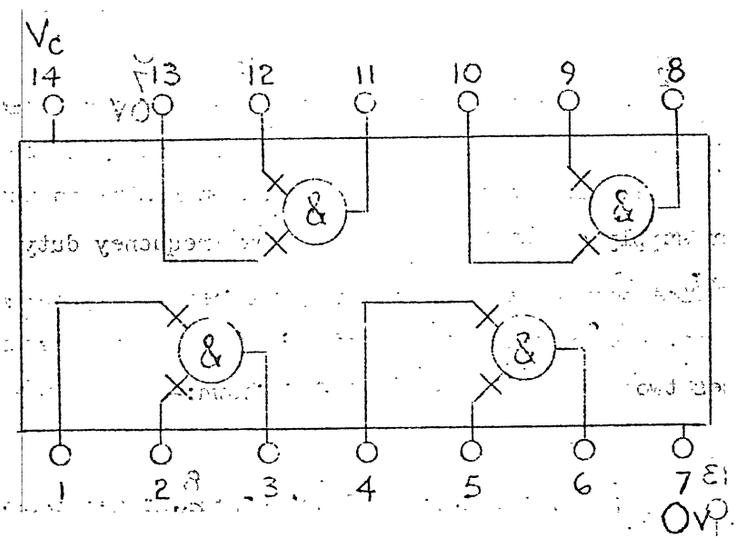
propagation delay times. These are the time delays between the 50% point of the input change and the 50% point of the output change.

There are conditions under which it is desirable to make an added allowance for transition delays (delays from 10 to 90% of transition). This will be further explained in a later addition to this document.

SECTION 2: GATING CIRCUITS

2.1 Type A

2.1.1 This comprises four two input gates as shown:-



The max power supply current on a 50 : 50 low frequency duty cycle is 20 mA.

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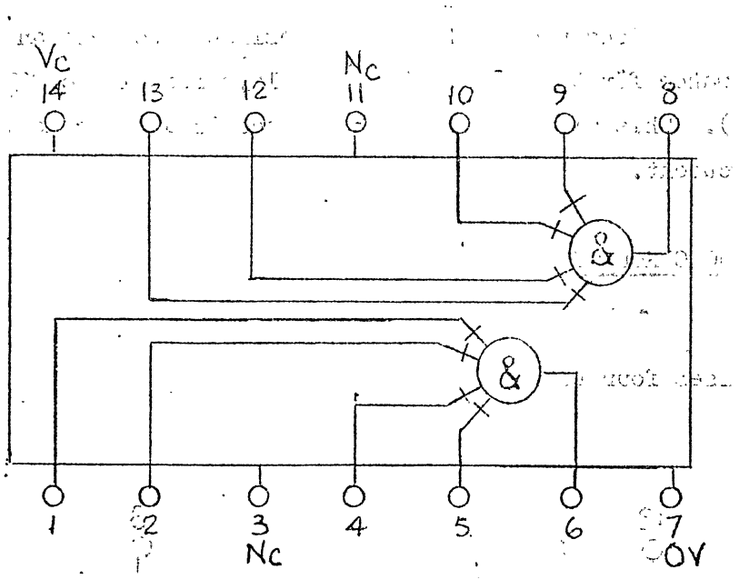
2.2 Type B

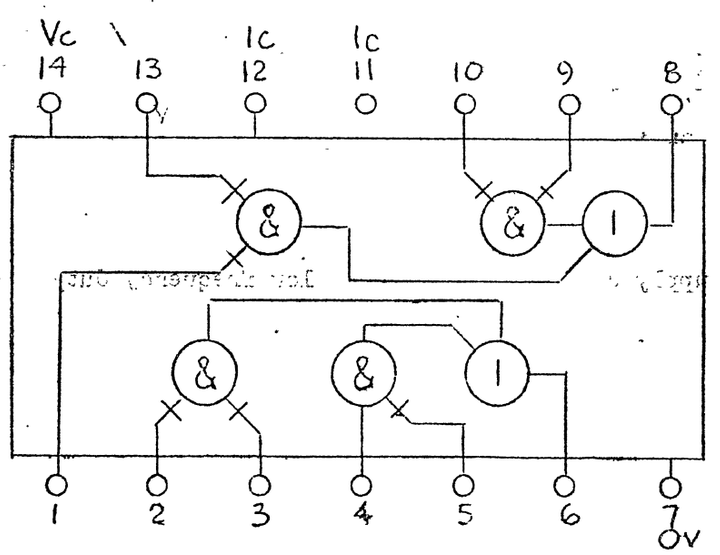
This comprises two four input gates as shown:-



The max power supply current on a 50 : 50 low frequeney duty cycle is 10 mA.

2.3 Type C

This comprises two sets of AND-OR gates as shown:-



The max power supply current on a 50 : 50 low frequeney duty cycle is 14.5 mA.

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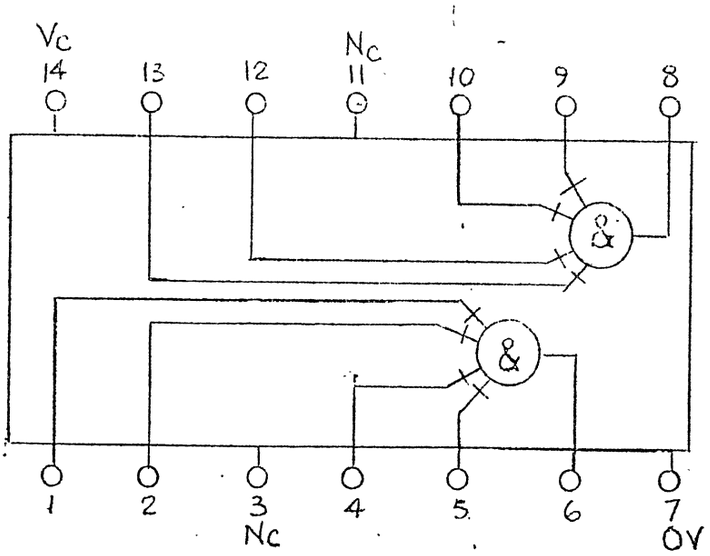
2.2 Type B

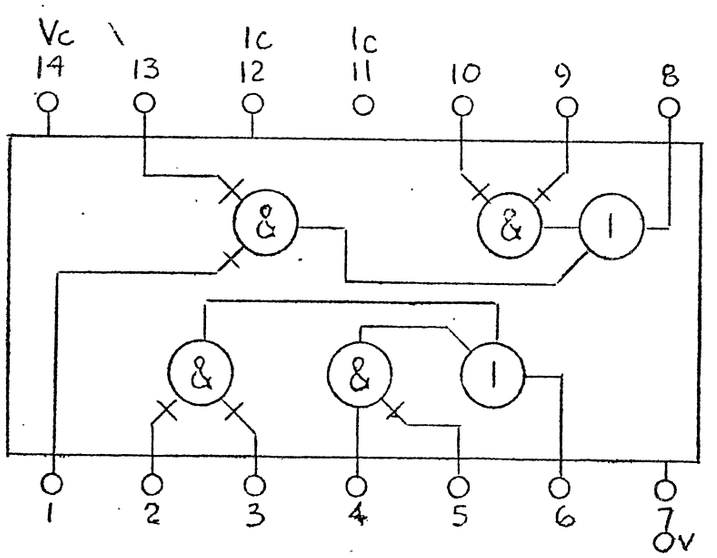
This comprises two four input gates as shown:-



The max power supply current on a 50 : 50 low frequency duty cycle is 10 mA.

2.3 Type C

This comprises two sets of AND-OR gates as shown:-



The max power supply current on a 50 : 50 low frequency duty cycle is 14.5 mA.

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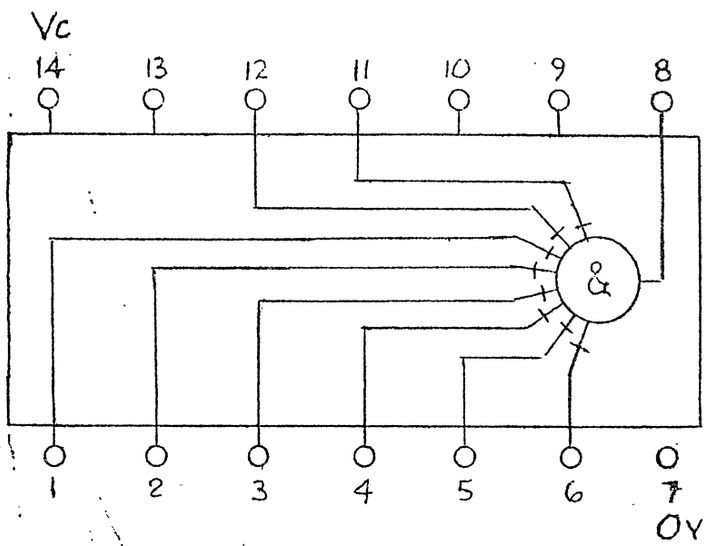
2.4 Type F

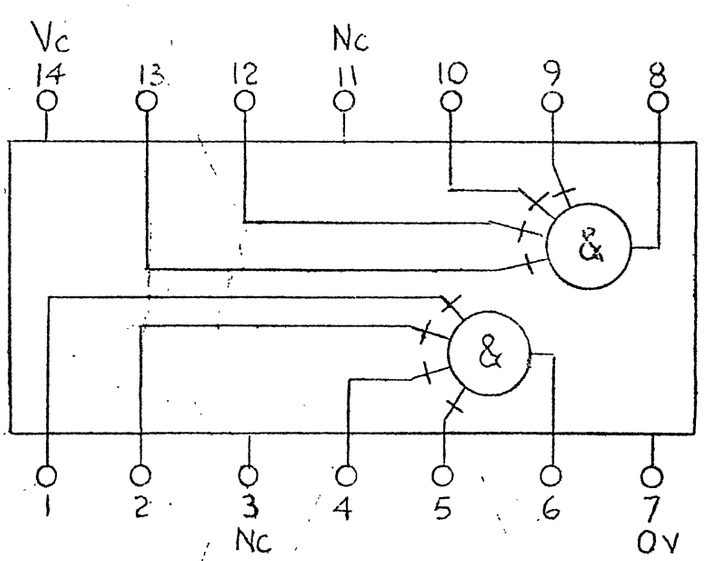
This is an eight input gate as shown:-



The max power supply current on a 50 : 50 low frequency duty cycle is 6 mA.

2.5 Type G

This comprises two four input power gates each having a fan-out of 30.



The max power supply current on a 50 : 50 low frequeney duty cycle is 31 mA.

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2.6 Propagation Delay Times

The propagation delay times as defined in para. 1.7. for all the gates are as follows:-

With a string length of 1 foot of wire on the output

Positive Delay			Negative Delay	
Min.	Max.		Min.	Max.
	F.O. = 9	F.O. = 30		
5	25 nS	45 nS	2	20 nS

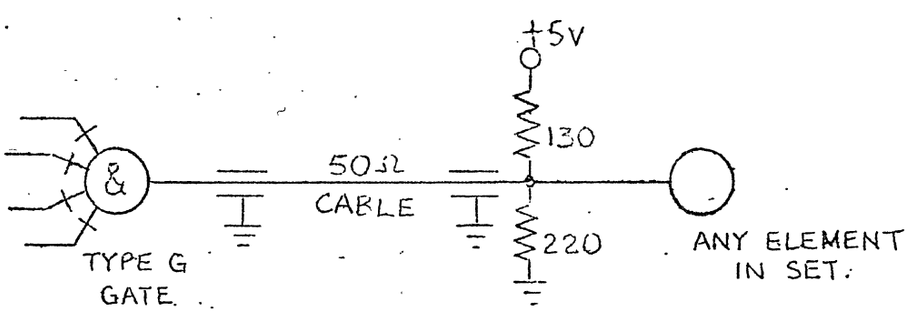
With a string length of 4 feet of wire on the output

Positive Delay			Negative Delay	
Min.	Max.		Min.	Max.
	F.O. = 9	F.O. = 30		
8	35 nS	55 nS	3	30 nS

2.7 Driving Coaxial Cables

The power gate type G may be used to drive coaxial cables having an impedance of 50 ohms. Such cables may be run between separate pieces of equipment providing that the difference between the earth points at which the cable is connected does not exceed 0.1 volt.

When this arrangement is used, the line should be terminated as shown below and the fan-out, which can be connected at either or both ends of the line, should be limited to 8.



The circuit propagation delay time for cable lengths up to 12 feet can be taken to be the same as the figures quoted in para. 2.6. for a fan-out of 9, plus 1.6 nS for each foot of cable length.

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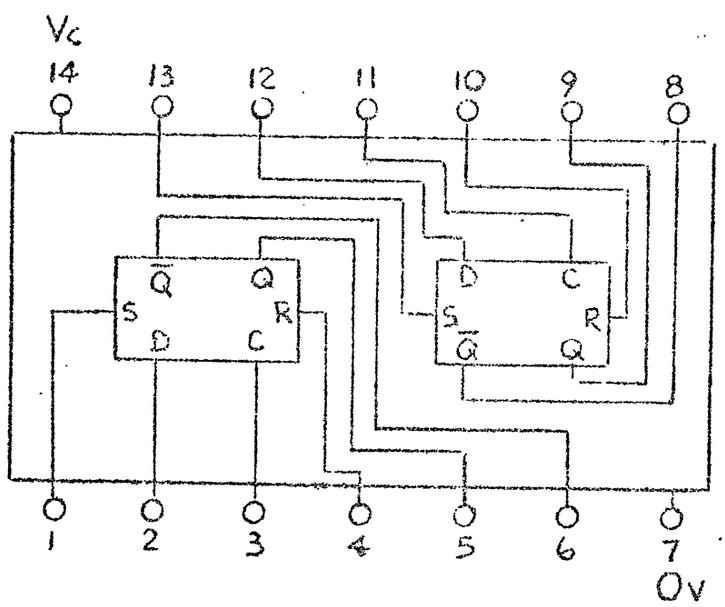
SECTION 3: BISTABLE TYPE D

3.1 General

3.1.1 This is a D type bistable and there are two in each package. It has very little or no immunity to clock skew and it should therefore not be used in any application involving the transfer of data between successive stages where the same clock pulse is applied to both stages.

3.1.2 This D type bistable is likely to stay at about half the price (per bistable) of the type E and, where clock skew immunity is not required, and the more limited input facilities are sufficient, it should be used in preference to the type E.

3.2 Connections



3.3 Loading Rules

D input	-	1 unit load.
S "	-	1 " "
R "	-	2 " "
Clock "	-	2 " - "

3.4 Logic Function

3.4.1 Set-Unset Operation.

To operate in this mode the clock input must be held low but the D line can be in either state.

The state of the bistable can be altered, in accordance with the following equations, by taking either the S or the R input into the low state. The bistable stays in the chosen state when the appropriate B or R line is returned to the high state

$$Q = \overline{S}$$

$$\overline{Q} = \overline{R}$$

3.4.2 Clocked Operation

To operate in this mode both S and R inputs must be held high. When the clock input is taken from the low state to the high state, the binary takes up the state of the D line.

$$Q = D$$

$$\overline{Q} = \overline{D}$$

In order to do this successfully, the D line must be steady over a period of time either side of the time when the clock input goes high (i.e. over time periods t set-up and t hold). Once the bistable has been set in this way, the D line is 'locked out' i.e. at the end of the t hold period of time the D line may be altered with the clock still high without changing the state of the bistable. The output from the bistable is available at a time T_{out} after the time when the clock input goes high. The clock input may be returned to the low state any time after T_{out} without affecting the state of the bistable.

3.5 Performance

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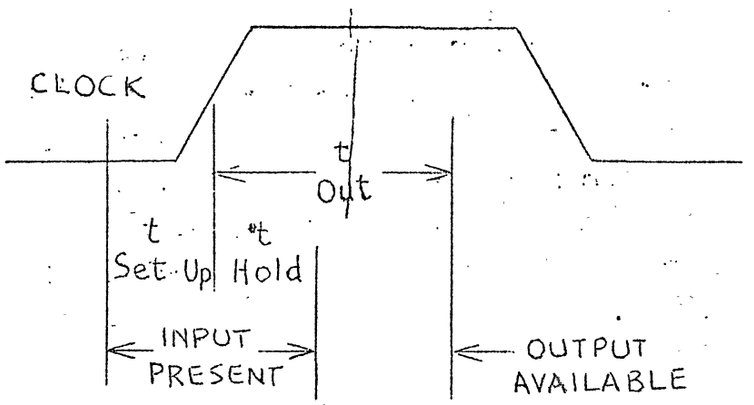
3.5.1



t set up	20 nS min.		
t hold	10 nS min.		
		1' of wire	4' of wire
to output	(to a '0') max	50 nS max	61 nS max
"	(to a '1') "	35 nS max	46 nS max

3.5.2 The max figures for t output apply for both clocked and set-unset operation.

The minimum figures for t output is not defined and no reliance should be placed on this being greater than zero.

3.6 Power Requirements

3.6.1 The max power supply current for low frequency operation is 35 mA.

SECTION 4: FASTER TT2 CIRCUITS

4.1 Specifications will later be written for a number of faster gating circuits, as the position with the suppliers of these circuits becomes clearer. The actual gate functions have yet to be selected.

4.2 The circuits selected will be fully compatible electrically and mechanically with the ones that have been described.

Subject to the wiring rules being obeyed, it will be possible to replace existing circuits with the faster one in order to speed up a given array of logic.

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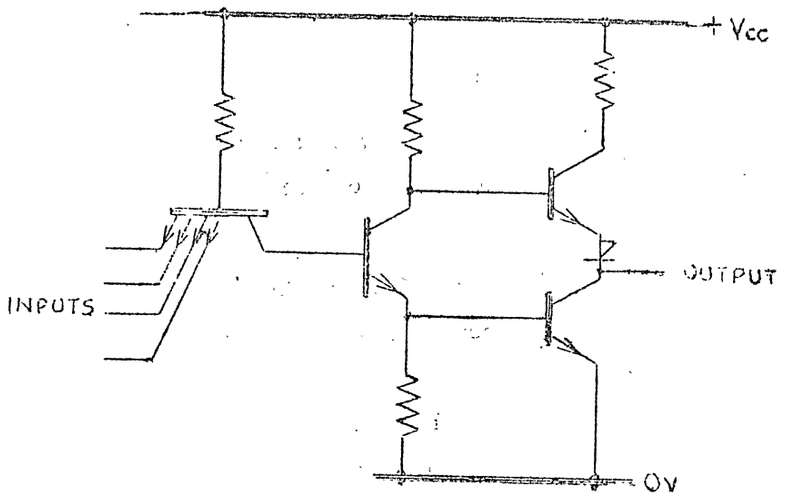
4.3 These additional circuits will be approximately twice as fast, i.e. max of 12 nS with worst fan-out and one foot of wire instead of a max of 25 nS.

4.4 The wiring rules with these circuits have yet to be worked out, but it is likely that the limit to open back wiring will be the order of 8" and that their use will really be confined to internal connections on multi-layer macro boards. Logical designers envisaging the future substitution of existing circuits by the faster circuits should think in terms of only doing so in this way.



Half of Type B Package

Multiple Emitter Transistor Input provides faster turn-off than other logic forms, thereby minimising propagation time. Output structure uses active pull-up and pull-down to provide low impedance driving source in both logic states. This also minimises propagation time, even in high fan-out applications. Current limiting resistor in active pull-up path gives short-duration short-circuit protection.

Supply voltage	5 ± 0.25 V
Min Input Voltage to maintain "Low" Output	2.0 V @ 40 uA In
Max Input Voltage to maintain "High" Output	0.8 V @ 1.6 mA Out
Min "High" Output Voltage (full load)	2.4 V @ 0.4 mA Out
Max "Low" Output Voltage (full load)	0.4 V @ 16 mA In
Fan-out	16

Propagation Time: