

I.C.T 1900 SERIES

CENTRAL PROCESSORS 1902 1903



- Programming compatibility throughout 1900 series
- Core store expansible and interchangeable on site
- Interchangeable with other processors in 1900 series
- All peripherals attached via I.C.T Standard Interface
- Simultaneous operation of peripheral devices

DESCRIPTION

The 1902 and 1903 are two of the smaller central processors that can be chosen for an I.C.T 1900 data processing system. 1902 is designed around a core store with a cycle time of six micro-seconds and 1903 on a store with a cycle time of two micro-seconds. The 1903 achieves two-and-a-half times the internal performance of the 1902. They can be specified for small, medium and largescale configurations which do not initially require the multi-programming facilities available with types 1904-1909 processors. However a 1902 or 1903 specified with communications facilities will work in real-time.

A wide range of input, output, storage and communications devices may be coupled to the Central Processor and connection is via one of eight I.C.T Standard Interface channels. If required, a channel can handle a control or multiplexor unit which in turn handles multiple devices.

Core store is expansible on site and a 1902 can be converted to a 1903 by substituting the faster store. Should a change to a still faster computer be required, the only device needing replacement would be the central processor. There is full upwards compatibility of instruction code, programs, software and peripheral devices within the 1900 range.

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Executive

Executive is a program which is contained within the core store at all times when the computer is in normal use. The main functions which it performs are:

- 1 Interpretation and execution of the operator's commands to the system, and provision of information for the operator concerning normal program running, incidents and peripheral devices that need attention.
- **2** Allocation of the time of the central processor among the programs in the system according to given priorities so as to achieve maximum utilization of the central processor and of the peripheral devices.
- **3** Monitoring of program and peripheral device performance.

Operation

Systems utilizing 1902 and 1903 processors are controlled by means of messages entered by the operator on a typewriter directly connected to the processor. In addition, pre-punched messages may be entered via a card reader or a paper tape reader. Executive takes the actions requested, and when necessary will type out messages for the information or action of the operator. This provides a printed record of the sequence of operational events. Facilities are also available for automatically sequencing jobs.

High Speed Stores

1902 stores are of six micro-second cycle time with 4,096, 8,192 or 16,384 words capacity. 1903 may have 8,192, 16,384 or 32,768 words with a two micro-second cycle time. This provides flexibility in the choice of an initial installation to meet small, medium or large-scale application requirements. Any store in an initial installation may be replaced or expanded to maximum on site. Operations on all stores are subjected to automatic parity checking.

Store Reservation

A check is made to ensure that programs do not over-write the part of store occupied by Executive.

Peripheral Transfers

Data transfers to and from peripheral devices are initiated by the Executive, which has direct control of the devices, at the request of the program. Once initiated the transfers proceed autonomously. A number of transfers may be in progress simultaneously. The central processor is caused to 'hesitate' only when necessary to allow a single character or word of four characters to be transferred between the store and a peripheral unit. The hesitation time varies according to the peripheral device, unit of transfer, and store cycle time. For example, to input a character from card or paper tape to a 2 microsecond store takes 7.6 micro-seconds about every 830 micro-seconds; to output a character to paper tape from a 6 micro-second store takes 13 micro-seconds about every 9090 micro-seconds. Internal processing proceeds therefore at a slightly reduced rate while a peripheral transfer is in progress. A transfer which fails accuracy checks is repeated by Executive a pre-determined number of times provided the peripheral device permits the automatic re-positioning of the medium (e.g. a magnetic tape deck). If the transfer is still in doubt after this, operator intervention is automatically requested.

On other devices a failure is notified to the operator immediately.

Word Length

The processor operates with words of 24 binary digits. Such a word can be used to represent:

one instruction

four alpha-numeric characters a decimal integer in the range -8,388,608 to +8,388,607 a decimal fraction in the range -1.0 to +0.9999999 with accuracy approximately equivalent to seven decimal digits.

Two words together may represent a double precision number having an accuracy equivalent to over thirteen decimal digits.

A number of separate data items may be packed into a word or group of words, and instructions are available to address single characters in the store.

Instruction Code

The first eight core store locations assigned to the program are designated as accumulators and are used for arithmetic, counting etc. Three of these may be further used for indexing. Most instructions carry a reference to a core store location and an accumulator. The comprehensive instruction repertoire contains arithmetic, transfer, logical and shifting operations, including multiplication, division and literal operand facilities. There are special provisions for multiple-length arithmetic, conversions between decimal and binary forms of numbers, and character handling.

Input/Output Channels

Peripheral devices are connected to the Central Processor by means of eight input/output channels which are housed in the processor cabinet. One channel can accept any peripheral device built to I.C.T Standard Interface. However a group of peripherals, e.g. magnetic tape decks, or communications links which are controlled by a multiplexor, will require only one channel.

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SPECIFICATION SUMMARY

Data unit 24-bit word Store checking One parity bit per word

Stores 2 micro-second cycle time with 8,192, 16,384, or 32,768 words capacity (1903) 6 micro-second cycle time with 4,096, 8,192 or 16,384 words (1902)

Accumulators Eight, of which three

may be used as index registers

Arithmetic Binary (instructions
include decimal conversion)

Addition time 18 micro-seconds with 1902 processor 7 micro-seconds with 1903 processor

Input/Output Eight Standard Interface channels

PHYSICAL CHARACTERISTICS

Height 49 inches 26 inches Depth Length 69 inches Weight 700 pounds

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