10077 Hardware/Software Manual

Multibus DR11-W Emulator

Ikon Corporation

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Table of Contents

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1. Introduction

This manual contains programming and hardware set-up information for the etched-board version of the IKON Model 10077 Multibus DR11-W emulator. The Model 10077 is a full emulation of a Digital Equipment Corporation DR11-W and will support any device or application supported by the DEC product.

The DR11-W emulator is a high-speed parallel DMA interface which may be used in interprocessor links based on cross-coupled DR11-Ws or emulators. Linkable systems include VAX, LSI-11, PDP-11, Gould/Sel, Data General, Harris, Perkin-Elmer, and IBM using other manufacturer's DR11-Ws, and Multibus, VERSAbus, VMEbus, and Prime systems using IKON's family of DR11-W emulators.

The 10077 can also be used to connect the Multibus to any peripheral device, network node, mainframe channel interface, or workstation with a DR11-W type interface -- including a wide variety of graphics equipment made by several manufacturers.

NOTE: The following registered trademarks are used in this manual for descriptive purpuses to identify compatibility:

VERSAbus - Motorola, Inc.

Multibus - Intel Corporation

DEC, PDP-11, VAX, LSI-11 - Digital Equipment Corporation

2. General Specifications

Slave Mode Access

8, 16, 20, or 24 bit address decode with inhibit capability.

I/O or memory mapped.

Register set requires 16 consecutive word locations.

16 bit data access only.

Interrupts

Non-bus-vectored interrupts, with switch selectable interrupt level.

DMA

24 bit linear address generation with 16 bit range (word) counter for up to 128k byte DMA blocks anywhere in a 16M byte address space.

DMA logic is all-bipolar, asynchronous, delay line driven for maximum speed and bus efficiency.

Parallel or serial bus arbitration.

Single transfer per arbitration--allowing maximum bus access by other devices.

2M byte/second+ maximum transfer rate (1M byte/second typical in interprocessor link).

External Interface

All DR11-W I/O modes supported, including control of bus address and range counter incrementation.

BUSY polarity switch selectable.

I/O connectors and pin-out identical to DEC format.

All input and output signals terminated and driven-received with high-hysteresis unified-bus type open collector transceivers.

Optional byte swapping to and from the external device with separate switches for P-I/O and DMA.

Power and Environmental

Power consumption - 3.5A

Commercial temperature range and humidity to 90% non-condensing.

3. Detailed Hardware Specifications

All timings are typical.

Multibus utility clock CCLK/ required for access to board -- slave mode timings below assume 10MHz CCLK/.

Slave Mode

address set up req'd	0ns
address hold req'd	0ns
data set up req'd	0ns
data hold req'd	0ns
read data stable to XACK	200ns
r/w strobe to XACK	450ns
read data hold time	40ns
XACK hold time	20ns
inhibit delay	30ns
command pulse width req'd	50ns

Interrupts

INTA width	na

DMA - Data Transfer Timing

address to r/w strobe set-up	100ns
address hold from r/w strobe	100ns
data to write strobe set-up	80ns
data hold from write strobe	100ns
XACK to r/w strobe negated	100ns

DMA - Bus Arbitration

BCLK to BREQ asserted	15ns
BCLK to BREQ negated	15ns
BPRN to BCLK set-up req'd	20ns
BCLK to BUSY asserted	17ns
BCLK to BUSY negated	17ns
BUSY to BCLK set-up req'd	25ns
BCLK to BPRO asserted	14ns
BCLK to BPRO negated	14ns
BPRN to BPRO propagated	10ns
BCLK to CBRQ asserted	16ns
BCLK to CBRQ negated	16ns
CBRQ to BCLK set-up req'd	na

Bus Interface

All bus receivers one 74LS load with hysteresis.

All strobe receivers one 74S load or less with hysteresis.

All bus drivers 74LS245 or equivalent.

All strobe drivers 74F240 or equivalent.

All open-collector drivers 74ALS38 or equivalent.

BPRO driver 74F00 or equivalent.

External Interface

All external signals terminated with 180 ohms to vcc and 390 ohms to ground.

All external signals received/driven with DS8838 type transceivers with 70ma sink capability and 1v hysteresis (1v and 2v thresholds).

Input de-skew (cycle request - CRQA or B - to input data & control signals latched) 125ns.

Output settling time (data valid to BUSY trailing edge) 250ns.

END CYCLE H pulse 200ns.

ACLO FNCT2 H, INIT H, GO H pulses 300ns.

FNCT1, 2, 3 signals change with the leading edge of GO H (these bits may also be changed without pulsing GO H).

Complete DMA cycle (cycle request to BUSY trailing edge) approximately 1000ns in system with 500ns memory access time.

4. On-Board Registers

The Model 10077 on-board registers occupy a 32 byte block of addresses which may be located anywhere in the Multibus I/O or memory maps. Address and map selection is via switches.

The low order five bits of the system address (actually 4 bits -- ADR0/ is ignored) are used to determine which on-board register is being accessed. The remaining address bits are examined to determine when the board is being addressed.

All on-board registers may be written and read only as words. Byte accesses are not supported.

4.1. On-Board Register Addressing

xxxx + 4 bits switch selectable -- all values in hex

Address	Write	Read
xxxx00	Control	Status
xxxx02	Data Out	Data In
xxxx04		
xxxx06	Pulse Command	
xxxx08		
xxxx0A		
xxxx0C		
xxxx0E		
xxxx10	DMA Control	
xxxx12	DMA Address Low	DMA Control Low
xxxx14	DMA Range Count	DMA Range Count
xxxx16		DMA Address Low
xxxx18		
xxxx1A	DMA Address High	DMA Control High
xxxx1C	DMA Range High	Dma Range High
xxxx1E		DMA Address High

Note that the DMA Address registers are accessed at different read and write addresses. This is a property of the 2940 bipolar DMA register chips used on the 10077.

The DMA Range High register is optional. This 8-bit register may be written and read, but has no effect on the DMA range count unless the option is enabled.

4.2. Register Formats

For all 16 bit registers, bit F is the most significant bit. Bit 7 is the MSB for all 8 bit registers.

Control

Bit	Name-Signal	Function
F	RDMA	reset DMAF flag
E	RATN	reset ATTF flag
D	RPER	reset PERR flag
C	MCLR	master clear board and pulse INIT H
B		
A		
9		
8	CYCL	force DMA cycle
7		
6	IENB	enable-disable interrupts
5		
4		
3	FCN3	FNCT3 H signal
2	FCN2	FNCT2 H signal
1	FCN1	FNCT1 H signal
0	GO	pulse GO H signal & enable DMA

RDMA Writing a 1 to this bit resets the DMA end of range flag and associated interrupt, if set.

RATN Resets the attention flag bit and its associated interrupt.

RPER Resets the parity error flag if set.

MCLR Resets all latched functions and flags in the interface, terminates DMA, and pulses the INIT H signal to the external device.

CYCL Forces an immediate DMA cycle if DMA is enabled. This bit is the software equivalent of an external cycle request.

IENB This is the master interrupt enable bit for the interface. If it is a 1, the interface will place an interrupt request on the bus whenever ATTF or DMAF is set. Interrupts may be disabled by setting this bit to 0.

FCNx The three function bit latches drive the FNCTx H signals to the external device. They may be set to 0 or 1, and are reset to 0 by MCLR. FCN2 also drives the ACLO FNCT2 H signal.

GO The go bit pulses GO H to the external device and enables DMA transfers. DMA transfers will not occurr unless the external device or the software generates cycle requests.

The above functions which are pulses--GO, CYCL, MCLR, RPER, RATN, RDMA, and a pulsed form of FCN2--are also available in the Pulse Command register.

Status

Bit	Name-Signal	Function
F	DMAF	DMA end-of-range flag
E	ATTF	attention flag
D	ATTN	state of ATTENTION H
C	PERR	parity error flag
B	STTA	state of STATUS A input
A	STTB	state of STATUS B input
9	STTC	state of STATUS C input
8	0	
7	REDY	interface ready indication
6	IENB	interrupt enable latch
5	0	
4	0	
3	FCN3	state of FCN3 latch
2	FCN2	state of FCN2 latch
1	FCN1	state of FCN1 latch
0	1	always 1 for 10077

DMAF DMA end-of-range flag. Set by last transfer in block. Causes an interrupt if IENB is true (1). Reset by MCLR or RDMA.

ATTF Set by a false-to-true transition on the ATTENTION H input. ATTF will cause an interrupt if IENB is true. Reset by MCLR or RATN.

ATTN This bit follows the state of the ATTENTION H input.

PERR The parity error flag is set by an external (DR11-W) parity error during a DMA input or P-I/O read. It is reset by MCLR or RPER, but otherwise will stay true once set by an error. Note that parity is an

IKON-only enhancement to the DR11-W specification and will work properly only when this interface is connected to a device which implements parity on the DR11-W I/O signals.

STTx The STTx bits follow the state of the STATUS x inputs.

REDY This bit reflects the state of the READY H output and indicates that the interface is ready for another command, such as GO. When REDY is false it indicates that the interface has been enabled to do DMA (by GO) and that the external device may issue cycle requests. REDY is reset by GO and set by MCLR, DMA end-of-range, or ATTENTION H.

IENB This bit reflects the state of the interrupt enable latch.

FCNx These bits indicate the states of the function bit latches, and are primarily diagnostic in nature.

Some CPU implementations on the Multibus (particularly those using 68000 processors) swap the bytes of all word transfers to and from a peripheral device register. This can cause considerable confusion when trying to implement a device driver for a peripheral board like the 10077. When the 10077 is set up for loop-back mode (J1 and J2 connected), the power-up state of the status register is hex 0081. If it appears to be 8100, the cpu is swapping bytes, and the driver software will have to take this into account. The 10077 has on-board byte swapping capability for data to and from the external device -- but not for the on-board register set. See the Hardware Switch options section of this manual for details of byte swapping.

Data Out

Data written to this register is latched and presented to the external device via the DO00-DO15 output signals. This register is also used during DMA output and should not be written when REDY is false.

Odd parity over 17 bits is maintained for output data. The 17th bit (POXX H) replaces a GROUND pin in the DEC DR11-W specification. Its use is optional.

Data In

This register contains the current state of the DI00-DI15 input signals from the external device. It is used during DMA input, and should not be read by the program when REDY is false. Parity is checked whenever this register is read by the program or by DMA input.

Odd parity over 17 bits is checked on input data and PIXX H.

Pulse Command

Bit	Name-Signal	Function
F	RDMA	reset DMAF flag
E	RATN	reset ATTF flag
D	RPER	reset PERR flag
C	MCLR	master clear board and pulse INIT H
B		
A		
9		
8	CYCL	force DMA cycle
7		
6		
5		
4		
3		
2	FCN2	pulse ACLO FNCT2 H
1		
0	GO	pulse GO H signal & enable DMA

All bits in the Pulse Command register are pulsed functions which only affect interface and device functions when written as 1s. Writing a 0 to any of these bits has no effect. They are included as a convenience to allow the programmer to generate pulses without having to worry about the static, latched functions in the Control register. This eliminates always having to carry a copy of the Control register and 'or' in the pulse bits. It also allows pulsing the ACLO FNCT2 H (typically used to interrupt the external device) wihtout having to set FNCT2 to 1 and then 0.

FCN2 Writing a 1 to this bit pulses the ACLO FNCT2 H output. Writing a 0 has no effect. Note that the ACLO signal is the 'or' of this pulse and the FCN2 latch

in the Control register.

See the Control register section of this manual for a description of the other bits in this register.

DMA Control

A write to this write-only register sets the internal control registers of all the on-board 2940 DMA register ICs. This register must be set to 0 prior to starting DMA transfers.

DMA Address

The DMA address register is a 24 bit counter that is accessed by the program as a pair of registers, one 16 bits and one 8 bits wide. Note that register bit 0 maps onto address bus bit 1, and so on. Any address value in this register is effectively multiplied by 2 before being applied to the bus. Prior to enabling the DMA mechanism, this register is loaded with the buffer starting address divided by 2 (right-shifted one place). After each DMA transfer the register is incremented by 1 unless counting is inhibited by the BA INC ENB H input signal being brought to GROUND.

DMA address register to Multibus address bus correspondence

DMA Address Low -- 16 bits

7	6	5	4	3	2	1	0
AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1

F	E	D	C	B	A	9	8
A10	ADF	ADE	ADD	ADC	ADB	ADA	AD9

DMA Address High -- 8 bits

7	6	5	4	3	2	1	0
x	A17	A16	A15	A14	A13	A12	A11

The Axx and ADx bits shown above correspond to the Multibus ADRxx/ address bits.

DMA Range Count

The DMA range counter is a 16 bit register that controls the number of words transferred to the external device during a DMA block transfer. Prior to starting the DMA mechanism, this counter is set to the number of words to be transferred minus 1. During each DMA transfer the counter is decremented by one unless counting is inhibited by the WC INC ENB H input signal being brought to GROUND. When the range counter goes negative, further DMA transfers are inhibited, the READY H output and REDY bit are asserted, the DMAF flag is set, and an interrupt is generated if enabled.

Hardware is available on the 10077 board to extend the range counter length to 24 bits -- making the maximum block size larger than addressable memory! Consult IKON for information on changing the range counter length if very large DMA blocks are desired.

NOTE: The DMA Control register must be set to 0 before enabling DMA transfers.

5. External Signals

It is important to understand the pin-numbering convention used by the IKON family of DR11-W emulators, and how this convention relates to the DEC scheme.

The 10077 external connectors correspond exactly--both electrically and physically to the DEC connectors. This means that the pin labelled on the connector as pin 1 (usually by an arrow or equivalent) corresponds to the DEC pin designated VV. The fact that DEC numbers (letters!) their pins in reverse order when compared to the physical connectors used has caused all kinds of grief to the customer trying to install DR11-W compatible products in a computer system. Some designers have chosen to make pin 1 correspond to DEC pin A which produces a connector that is physically backward from the DEC product--and only adds to the confusion.

A further confusing factor is that the preferred cables are assembled with a stripe on the pin 40 end! This is necessary since the cable's internal ground plane drain wire is at the striped end of the cable and must be terminated to pin 40.

Customers using this or any other DR11-W compatible product must determine from their various suppliers which pin numbering convention is used, and whether the cables need a half-twist between the connected devices. IKON cables are keyed, and can only be plugged in correctly at the IKON end.

It is strongly recommended that IKON's ground-plane cables or their equivalent be used for DR11-W applications. Ordinary ribbon cables have unsuitable impedance control and cross-talk characteristics when used with the DR11-W pin-out and may adversely affect data integrity.

Signals to External Device

All signals asserted when high

DO00-DO15 H — Output data lines. DO15 H is the msb. These lines follow the state of the Output Data register which is written by the program or by DMA output.

POXX H — This is the IKON-specified optional output parity signal. Odd parity is maintained over 17 bits (DOxx and POXX).

INIT H — Initialize signal to the external device. Asserted whenever the bus initialize signal INIT/ is true. Pulsed true for 300ns by writing a 1 to the MCLR bit in the Control or Pulse Command register.

FNCT1,2,3 H — User-defined function bits sent to the external device. Set by writing to the FCNx bits in the Control register. These bits change with the leading edge of GO H (if it is written--it is not necessary to pulse GO to change these bits).

READY H — Corresponds to the REDY bit in the Status register. When false it indicates that the DMA mechanism has been enabled and that the external device may issue cycle requests. It is set false by GO in the Control register and is set true by MCLR, system reset, DMA end-of-range, or ATTENTION H.

BUSY H — Indicates that the 10077 has received a valid cycle request and is doing a DMA cycle. The trailing edge of BUSY H indicates that the DMA cycle is complete and that the device may read the DOxx lines (if an output cycle) and issue another cycle request. The delay from stable output data to the trailing edge of BUSY H is 250ns.

BUSY H is normally asserted high. Its polarity is switch selectable. In interprocessor link applications it is asserted low so that its trailing edge causes a cycle request at the other end of the link. Many external devices also require that BUSY H be asserted low. The device documentation should be consulted for correct BUSY H polarity.

ACLO FNCT2 H — This signal is set by writing to FCN2 in the Control register or pulsed for 300ns by writing to FCN2 in the Pulse Command register. It is typically used to pulse ATTENTION H or its equivalent in the external device.

GO H — A 300ns pulse caused by writing a 1 to GO in the Control or the Pulse Command register. The leading edge of GO H occurs simultaneously with the true-to-false transition of READY H. It may be used to indicate to the external device that DMA has been enabled, or may be used as a strobe to indicate that the FNCTx H lines should be read by the external device.

END CYCLE H — This is a 200ns pulse that is simultaneous with the trailing edge of BUSY H. It may be used to strobe output data into the external device or instead of BUSY H as a handshake signal.

Signals from External Device

All signals true when high except BURST RQ L

Input terminations will hold floating inputs true.

All inputs except ATTENTION H and STATUS A, B, C H are latched following each cycle request. The latch delay (input de-skew) is 125ns.

DI00-DI15 H — Input data from the external device. DI15 is the MSB. The state of these lines may be read in the Data In register, or by doing DMA input. During DMA input these lines are latched 125ns after the cycle request is issued.

PIXX H — The IKON-specified optional input parity line. Odd parity is tested for over 17 bits (DIxx and PIXX).

C0,C1 CNTL H — DMA mode control lines. They are used by the external device to control the direction and type of the DMA transfer. These inputs are latched 125ns after each cycle request, and may be changed from one DMA word to the next.

Note that read-modify-write requests are actually handled in the 10077 as a read followed by a write and do not hold the bus between the read and the write.

C0 CNTL H	C1 CNTL H	OPERATION
0	0	Read Word
1	0	Read-Modify-Write
0	1	Write Word
1	1	Write Byte

During a Write Byte operation the byte selected is determined by the A00 H input signal. Model 10077 byte addressing follows the DEC format; A00 H low selects the low-order byte, A00 H high selects the high-order byte.

CYCLE RQ A,B H — A 0 to 1 transition on either of these lines while the other is held low, or a simultaneous 0 to 1 transition on both inputs will request a DMA cycle. If READY H is high, or if BUSY H is true cycle requests will be ignored. The end of the DMA cycle will be

indicated by the END CYCLE H pulse and by the trailing edge of BUSY H. All input data and control signals except ATTENTION H and STATUS x H are latched 125ns after the cycle request is issued.

The polarity of the cycle request inputs may be reversed (they will be falling edge active) by a cut and jumper option on the board. This may be useful when connecting to devices intended to interface to the DR11-B. Consult IKON for information on making this modification if desired. With either polarity, the inactive input (typically CYCLE RQ B) should be held low. There is a jumper available on the 10077 to accomplish this if for some reason it is not possible for the external device to control CYCLE RQ B H. Consult IKON for information.

ATTENTION H — The ATTENTION input signal can be used by the external device to terminate the DMA block (if DMA is in progress) and/or interrupt the CPU. ATTENTION H sets READY H and the REDY flag bit true and sets the ATTF flag bit in the Status Register. If ATTENTION H is held true it inhibits the starting of further DMA blocks and holds the ATTN bit in the Status register true.

STATUS A,B,C H — User defined input signals. They may be read as STTA, B, C in the Status register.

WC INC ENB H — This input signal controls DMA address register incrementation. It should be held true for sequential word transfers and set true every 2nd transfer for sequential byte transfers.

BA INC ENB H — This input signal controls range counter incrementation. It should be held true for sequential word transfers and set true every 2nd transfer for sequential byte transfers.

A00 H — This bit selects which byte of memory is written during Byte Write DMA cycles. DEC format byte addressing is used: A00 H low selects the low byte of the word, A00 H high selects the high byte of the word. There is a switch available to hold A00 H at 0 (ground). A00 should be grounded for interprocessor link mode operation or the last word of a DMA input block may be garbled.

Connector Pin-Out

J1 Pin-Out

IKON	DEC	Signal		DEC	IKON
1	VV	DO15 H	DO00 H	UU	2
3	TT	DO14 H	DO01 H	SS	4
5	RR	DO13 H	DO02 H	PP	6
7	NN	DO12 H	DO03 H	MM	8
9	LL	DO11 H	DO04 H	KK	10
11	JJ	DO10 H	DO05 H	HH	12
13	FF	DO09 H	DO06 H	EE	14
15	DD	DO08 H	DO07 H	CC	16
17	BB	POXX H	GROUND	AA	18
19	Z	CYCLE RQ B H	GROUND	Y	20
21	X	END CYCLE H	GROUND	W	22
23	V	STATUS C H	GROUND	U	24
25	T	STATUS C H	GROUND	S	26
27	R	STATUS B H	GROUND	P	28
29	N	INIT H	GROUND	M	30
31	L	STATUS A H	BURST RQ L	K	32
33	J	WC INC ENB H	GROUND	H	34
35	F	READY H	GROUND	E	36
37	D	ACLO FNCT2 H	GROUND	C	38
39	B	CYCLE RQ A H	GROUND	A	40

J2 Pin-Out

IKON	DEC	Signal		DEC	IKON
1	VV	DI15 H	DI00 H	UU	2
3	TT	DI14 H	DI01 H	SS	4
5	RR	DI13 H	DI02 H	PP	6
7	NN	DI12 H	DI03 H	MM	8
9	LL	DI11 H	DI04 H	KK	10
11	JJ	DI10 H	DI05 H	HH	12
13	FF	DI09 H	DI06 H	EE	14
15	DD	DI08 H	DI07 H	CC	16
17	BB	PIXX H	GROUND	AA	18
19	Z	GROUND	GROUND	Y	20
21	X	GO H	GROUND	W	22
23	V	FNCT1 H	GROUND	U	24
25	T	C1 CNTL H	GROUND	S	26
27	R	FNCT2 H	GROUND	P	28
29	N	C0 CNTL H	GROUND	M	30
31	L	FNCT3 H	FNCT3 H	K	32
33	J	BA INC ENB H	GROUND	H	34
35	F	A00 H	GROUND	E	36
37	D	ATTN H	GROUND	C	38
39	B	BUSY H	GROUND	A	40

6. Loopback Testing

The IKON model 10077, like most DR11-Ws and emulators is capable of extensive self-test. All programmed I/O, interrupt, and DMA features may be exercised and tested by 'looping back' the J2 connector to the J1 connector. This is done with a 40-conductor ribbon cable connected pin-for-pin between two 40-pin idc sockets. One of the standard IKON-supplied cables may be used for this purpose.

The signals connected in this way are shown below:

DO00-15 H	>	DI00-15 H
FNCT 1,2,3 H	>	STATUS C,B,A H
FNCT 1 H	>	C1 CNTL H
ACLO FNCT2 H	>	ATTENTION H
BUSY H	>	CYCLE RQ A H
POXX H	>	PIXX H

The loopback connection also causes (by virtue of the way the connector pin-outs line up) WC INC ENB H and BA INC ENB H to be asserted, and C0 CNTL H and CYCLE RQ B H to be held false.

BUSY H should be switched for low-assertion and A00 H should forced off with the available switch.

When set up for loopback, the 10077's various features may be tested as follows:

Programmed I/O is tested by writing a value to the Data Out register and verifying that the value appears in the Data In register.

Function and Status bits are tested by writing the FCNx bits in the Control register and reading the resulting STTx bits in the Status register. Note that FCN1 corresponds to STTC, and that FCN2 will also cause the ATTN, and ATTF Status bits to change.

Interrupts and various pulse commands are tested by setting up the board's interrupt mask, and then generating an ATTENTION interrupt by pulsing ACLO FNCT2 H by writing a 1 to FCN2 in the Pulse Command register.

DMA output is tested by setting up the range and address registers, setting FCN1 to 0, and then pulsing GO and CYCL in the Control register or Pulse Command register. GO enables DMA, and CYCL actually initiates the first transfer. The end of the first-and later-transfers cause BUSY H to go from low to high, which

causes another cycle request, continuing the handshake until the range counter has been exhausted. End-of-range sets the REDY and DMAF flags in the Status register, and causes an interrupt, if enabled.

If the data buffer has been previously set to a known pattern, the last word of that pattern should appear in the Data In register when the DMA block transfer is complete.

DMA input is tested in the same way except that FCN1 is set to one before starting DMA. If a known value has been previously written to the Data Out register it should be repeated in every word of the input buffer.

7. Interprocessor Links

The IKON model 10077 may be used in a high-speed parallel interprocessor link with other IKON DR11-W emulators, or those made by DEC or other manufacturers. This technique of linking processors and systems produces very high transfer rates -typically 1Mbyte/second- and can usually be implemented with a simple, efficient protocol.

The physical interprocessor link connection is made by connecting the J1 connector of each DR11-W to the J2 connector of the other DR11-w, switching for BUSY H asserted low and A00 H forced off.

The signal connection accomplished is similar to loop-back, and is shown below.

DR11-W #1		DR11-W #2
DO00-15 H	>	DI00-15 H
POXX H	>	PIXX H
DI00-15 H	<	DO00-15 H
PIXX H	<	POXX H
BUSY H	>	CYCLE RQ A H
CYCLE RQ A H	<	BUSY H
FNCT 1,2,3 H	>	STATUS C,B,A H
STATUS C,B,A H	<	FNCT 1,2,3 H
FNCT1 H	>	(loop back
C1 CNTL H	<	to #1)
(loop back	<	FNCT1 H
to #2)	>	C1 CNTL H
FNCT3 H	>	BURST RQ L
BURST RQ L	<	FNCT3 H
ACLO FNCT 2 H	>	ATTENTION H
ATTENTION H	<	ACLO FNCT 2 H
CYCLE RQ B H	<	0
C0 CNTL H	<	0
A00 H	<	0
WC INC ENB H	<	1
BA INC ENB H	<	1
0	>	CYCLE RQ B H
0	>	C0 CNTL H
0	>	A00 H
1	>	WC INC ENB H
1	>	BA INC ENB H

Note that each device's C1 CNTL H (direction control) is derived from its own FNCT 1 H output. If the device sets its FNCT 1 H output, it will be doing an input into its memory.

The exact software link protocol chosen is customer and application dependent, but most are based on the link protocol suggested by DEC in its DR11-W user's guide. This protocol involves exchanging single word messages via ATTENTION H interrupts to set up word count and data direction, and synchronize the start of DMA transfers. Block mode DMA accomplishes the actual data transfer. An example of an enhanced version of this protocol used by several of IKON's customers is available on request.

When ATTENTION H is used as part of a DMA protocol (typically driven by ACLO FNCT2 H as a clear-to-send indicator), it must be a pulse rather than a level. If the program that received the ATTENTION H signal attempts to start DMA while ATTENTION H is still asserted, DMA operation will be inhibited, and will not start when ATTENTION H is de-asserted. The end of the link generating the ATTENTION H signal should use a pulse that is as short as practical--which may be relatively long if more than one operating system call is required--and the end of the link receiving the ATTENTION H pulse should wait until it is removed before starting DMA.

The IKON Model 10077 pulse command register may be used to generate a 300ns ACLO FNCT2 H pulse at the IKON end of the link.

8. Hardware Switch Options

User selectable hardware options are controlled by DIP switches. The switch locations and layouts are shown below.

U34		U40	
1		1	ADRF/
2	force A00 H off	2	ADRE/
3	BUSY H asserted high	3	ADRD/
4	BUSY H asserted low	4	ADRC/
5	P-I/O byte swap	5	ADRB/
6	DMA byte swap	6	ADRA/
7	enb parity error flag	7	ADR9/
8		8	ADR8/

U42		U44	
1	ADR7/	1	ADR17/
2	ADR6/	2	ADR16/
3	ADR5/	3	ADR15/
4		4	ADR14/
5	16/20/24 bit address	5	ADR13/
6	8 bit address	6	ADR12/
7	20/24 bit address	7	ADR11/
8	8/16 bit address	8	ADR10/

U58		U70	
1	memory mapped read	1	INT0/
2	memory mapped write	2	INT1/
3	I/O mapped read	3	INT2/
4	I/O mapped write	4	INT3/
5	INH1/ driven	5	INT4/
6	serial bus arbitrarion	6	INT5/
7	CBRQ/ during request	7	INT6/
8	CBRQ/ always on	8	INT7/

Board Address Selection

The location of the 10077's on-board register set in the system memory or I/O map is determined by switches at U40, U42, and U44. A switch set to ON decodes a ONE in that address bit position.

The address width decoded is controlled by switches at U42.

U42 switch	5	6	7	8
8-bit decode	OFF	ON	OFF	ON
16-bit decode	ON	OFF	OFF	ON
20 and 24-bit decode	ON	OFF	ON	OFF

The switch settings are the same for 20 and 24 bit address widths. The 10077 has on-board pull-up resistors to hold the upper 4 address bits at 0 if they are not driven in the target Multibus system. If necessary, it is possible to completely disconnect the board's logic from the upper 4 address pins on the P2 connector (if a proprietary bus replaces the normal P2 signals, for example). Consult IKON for details.

Selection of I/O or memory mapped access to the 10077's registers is controlled by switches at U58. Although address map and width selections are made independently, the Multibus specification states that I/O map width may be 8 or 16 bits, and the memory map width may be 16, 20, or 24 bits.

U58 switch	1	2	3	4
Memory mapped access	ON	ON	OFF	OFF
I/O mapped access	OFF	OFF	ON	ON

Setting switch 5 of U58 ON causes the Multibus signal INH1/ to be asserted whenever the 10077 decodes its own address. This allows the interface register set to overlay portions of Multibus memory with inhibit capability.

Interrupt Level Selection

The bus interrupt level of the board is controlled by switches at U70. Only one switch at a time should be on. Consult system and CPU documentation for information on appropriate interrupt level selection.

The 10077 supports non-bus-vectored and polled interrupt operation. If interrupts are enabled, a condition which causes DMAF or ATTF in the Status register to set will cause the selected interrupt line to be asserted. The interrupt line will continue to be asserted until the status flag

causing the interrupt is reset by the program.

Bus Arbitration

The Multibus specification allows two non-compatible arbitration schemes: parallel and serial. Parallel arbitration allows an arbitrary number of bus masters to share the bus. Serial arbitration, since it requires the propagation of a bus priority signal through each potential bus master places severe requirements on the arbitration logic of each master. Because the priority signal must propagate within one cycle of the BCLK/ clock (typically 10MHZ) the maximum number of Multibus masters in a serial system is usually 3.

All boards in a Multibus system, and the Multibus backplane itself must be set up for the same arbitration scheme!!!!!!!!!

Switch 6 of U58 determines the arbitration scheme used by the Model 10077. It should be OFF for parallel operation, and ON for serial operation.

The common bus request signal - CBRQ/ - is used by most Multibus systems to indicate to the current master that some other board wants the bus. The 10077 is capable of generating CBRQ/, but does not monitor it, since it is a cycle-stealing DMA interface and always releases the bus after each transfer. The CBRQ/ mode used by the 10077 is selected by switches at U58.

U58 switch	7	8
CBRQ/ not driven	OFF	OFF
CBRQ/ driven during request	ON	OFF
CBRQ/ always on	OFF	ON

CBRQ/ driven during request is the appropriate setting for most Multibus systems.

External Device I/O Options

Byte Swap

Switches at U34 control the byte ordering of data to and from the external device.

U34 switch	5	6
swap P-I/O data	ON	X
no P-I/O swap	OFF	X
swap DMA data	X	ON
no DMA swap	X	OFF

Parity

This hardware option is an extension of the DEC DR11-W specification. It replaces a ground pin with a parity signal which provides parity checking and generation (odd parity over 16 data bits + 1 parity bit) for all P-I/O and DMA data to and from the external device. The external device or other DR11-W must have matching parity logic to take advantage of this enhancement. All IKON DR11-W emulators support matching parity generation and detection circuitry, making them particularly useful in high speed interprocessor links where data integrity is important.

The 10077 is shipped with the parity enhancement enabled. There are jumper option pads available on the board which allow converting the parity pins back to grounds per the DEC specification. This is normally not necessary, but may be useful when poor quality cable is being used or when operating in a particularly noisy environment. Consult IKON for information on implementing this option.

Outgoing parity is generated and latched whenever data is written to the Output Data register by P-I/O or DMA. Incoming parity is checked during P-I/O and DMA reads of the Input Data register. Any read parity error causes the PERR flag in the Status register to set and remain set until cleared by MCLR or RPER.

Switch 7 of U34 controls whether parity errors are reported in the status register. If it is OFF errors will not be reported and PERR will always be 0.

A00 H Disable

Setting switch 2 of U34 ON forces the incoming A00 H address line to 0, allowing only word transfers. This switch should be ON for interprocessor link operation and most other applications where DR11-W byte mode writes to memory are not required.

BUSY H Polarity

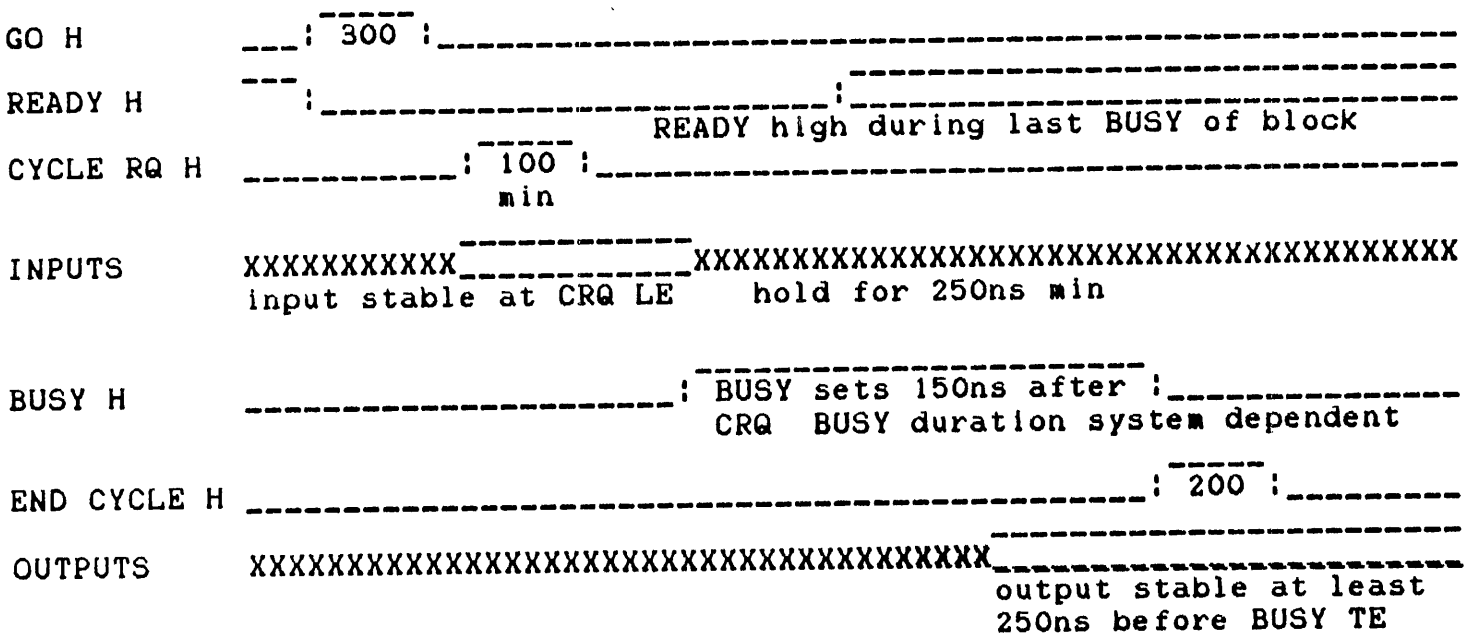
Switches at U34 control the polarity of the outgoing BUSY H signal. BUSY H is asserted LOW for interprocessor link operation and most general applications. It is asserted HIGH for what DEC calls 'device mode'. Consult target device documentation for appropriate polarity selection.

U34 switch	3	4
BUSY H asserted high	ON	OFF
BUSY H asserted low	OFF	ON

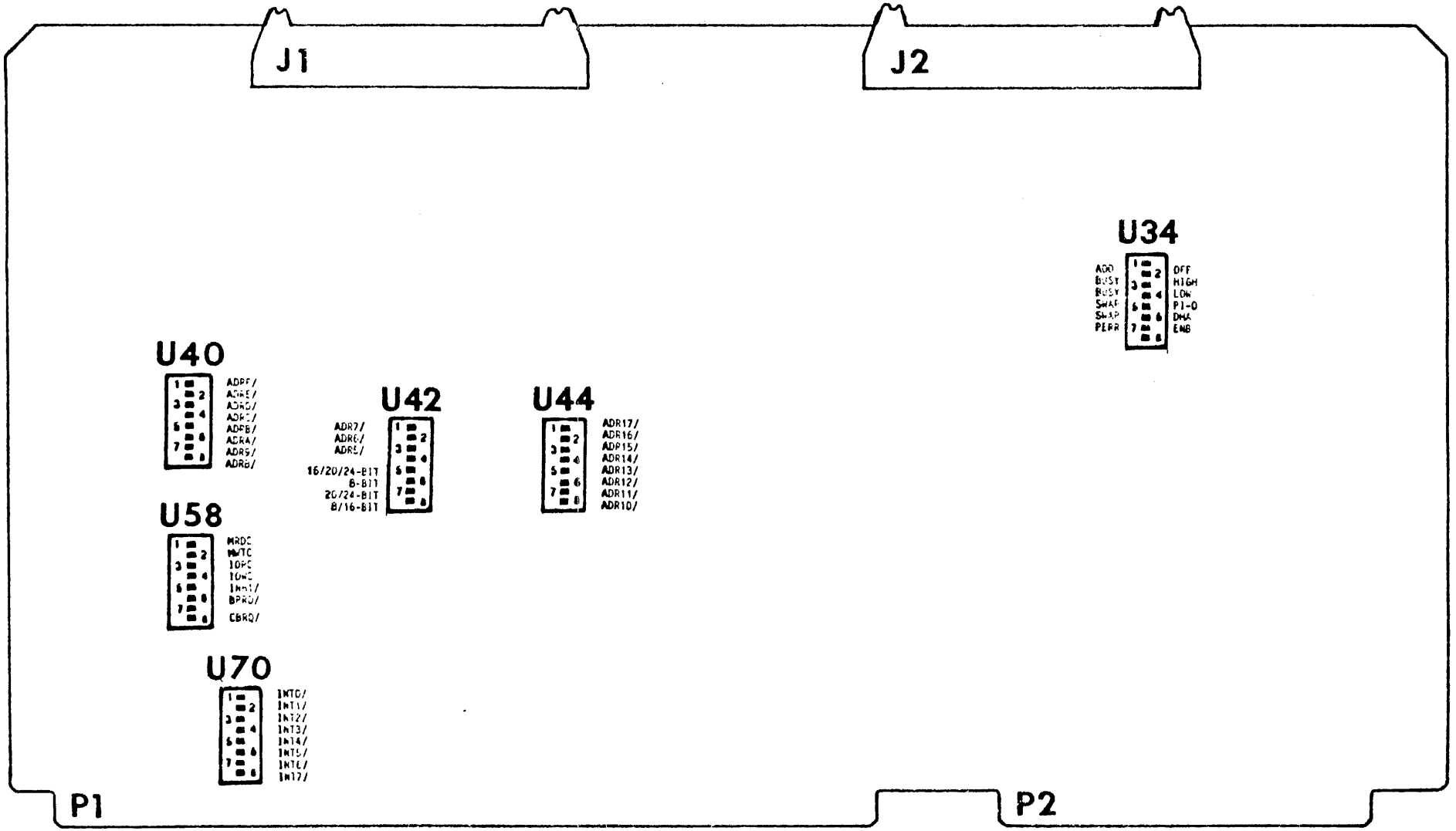
APPENDIX A

External I-O Signal Timing Diagram

IKON MODEL 10077 I/O TIMING



IKON MODEL 10077 DR11-W EMULATOR



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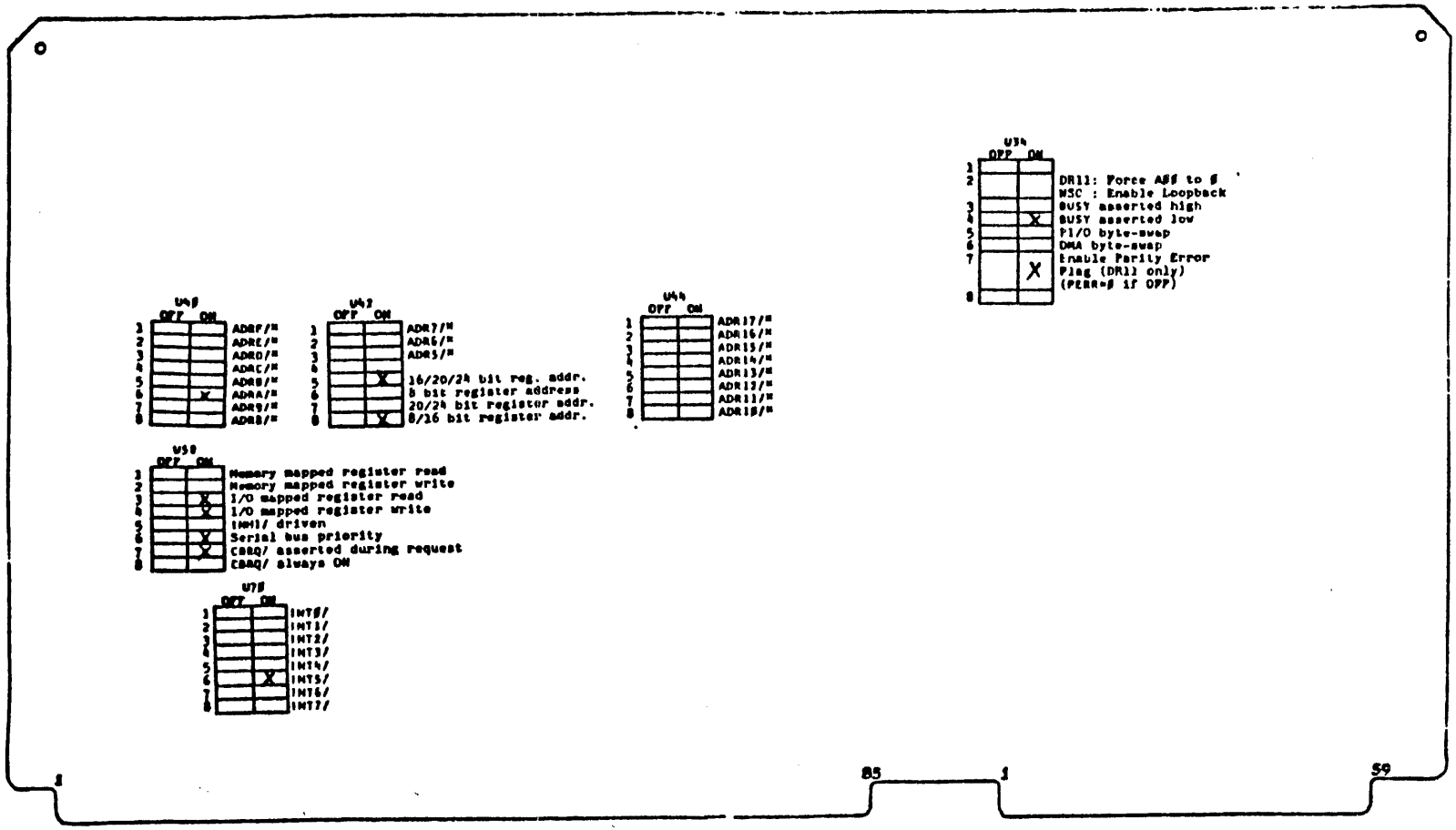
IKON Model 10077 Multibus*/DR11-W Emulator

Switch Layout and Settings



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