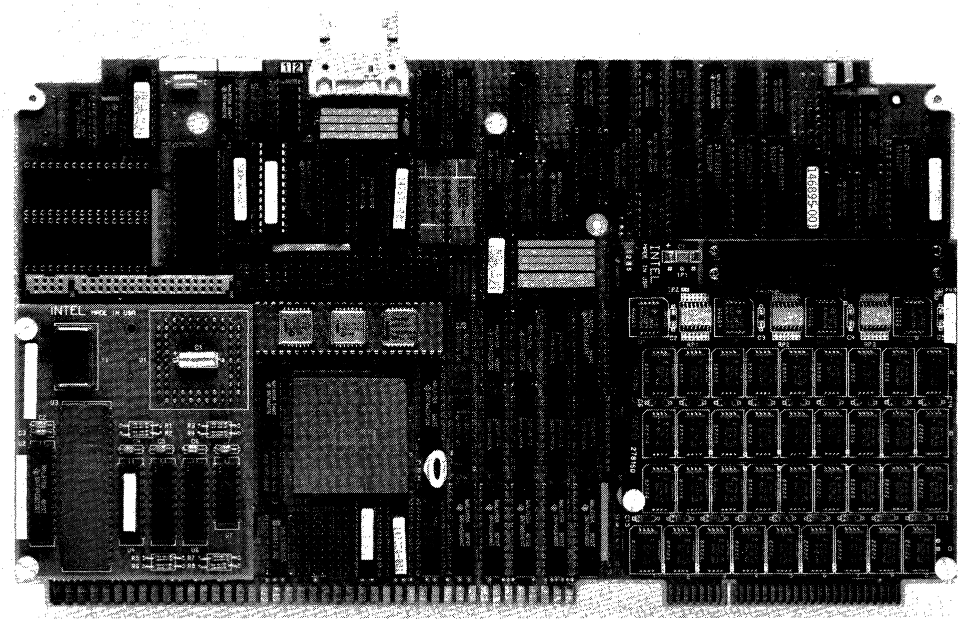
iSBC® 386/21/22/24/28 SERIES SINGLE BOARD COMPUTERS

- 16 MHz 80386 Microprocessor
- Available with 1, 2, 4, or 8 megabytes of on-board 32-bit memory, expandable to 16 megabytes using iSBC MM0x modules.
- High Speed 80287 floating point math coprocessor
- Uses iRMX 286 or UNIX* operating systems
- Two 32-bit JEDEC sites for up to 512 Kilobytes of EPROM memory
- RS232C interface for local/remote control and diagnostics
- iSBX interface for low cost I/O expansion
- 16 levels of direct vectored interrupt control
- 64 Kilobyte 0 wait-state cache memory

The iSBC® 386/2x series boards are Intel's highest performance MULTIBUS® I CPU boards. These boards feature a 16 MHz 80386 CPU, an 80287 math coprocessor, a 64k byte, 0 wait-state cache memory to support the CPU, and a 32-bit interface to 1, 2, 4, or 8 megabytes of dual-port parity DRAM memory. An additional 1, 2, 4, or 8 MB iSBC MM0x series memory module may be installed to provide up to 16 MB of on-board DRAM memory. The iSBC 386/2x boards also feature an 8/16-bit iSBX MULTIMODULE interface for low-cost I/O expansion, an asynchronous RS232C interface to support a local terminal or modem, two 16-bit programmable timer/counters, a 16-level direct-vectored interrupt controller, two 32-pin JEDEC sites for up to 512 kb of EPROM memory, and multimaster MULTIBUS arbitration logic. The iSBC 386/2x boards are ideal for applications needing 32-bit performance together with full MULTIBUS I compatibility.



*UNIX is a trademark of AT&T Bell Labs.

November 1986
Order Number 200409-001

OVERVIEW — iSBC 386/2x SERIES CPU BOARDS

The iSBC 386/21/22/24/28 boards (iSBC 386/2x series boards) are Intel's first 32-bit MULTIBUS I single board computers using the 80386 microprocessor. The boards employ a dual-bus structure, a 32-bit CPU bus for data transfers between the CPU and memory, and a 16-bit bus for data transfers over the MULTIBUS interface, iSBX interface, EPROM local memory, and I/O interfaces. In this manner, the boards take advantage of the 80386 CPU's 32-bit performance while maintaining full compatibility with the MULTIBUS I interface and iSBX MULTIMODULE boards.

The DRAM memory, which is on a module that is secured to the baseboard, may be expanded by installing a second 1, 2, 4, or 8M byte memory module. A block diagram of the board is shown in Figure 1.

The iSBC 386/2x series boards can be used in many applications originally designed for Intel's other 16-bit microcomputers, such as the iSBC 286/10A and iSBC 286/12/14/16, 8 MHz, 80286-based, single board computers. In this way, performance can be easily upgraded without requiring major hardware or software changes.

Central Processor Unit

The heart of the iSBC 386/2x CPU board is a 16 MHz 80386 microprocessor. This device utilizes address pipelining, a high speed execution unit, and on-chip memory management/protection to provide the highest level of system performance. The 80386 microprocessor also features an Address Translation Unit that supports up to 64 terabytes of virtual memory.

The 80386 CPU is upward compatible from Intel's 8088, 8086, 80186, and 80286 CPUs. Application software written for these other 8 and 16 bit microprocessor families can be easily recompiled to run on the 80386 microprocessor. Some minor changes to the software such as adjustment of software timing loops and changing I/O address references may be required. The 80386 microprocessor resides on the 32-bit wide CPU bus which interconnects the CPU with the math coprocessor and dual-port memory.

Instruction Set

The 80386 instruction set includes: variable length instruction format (including double operand

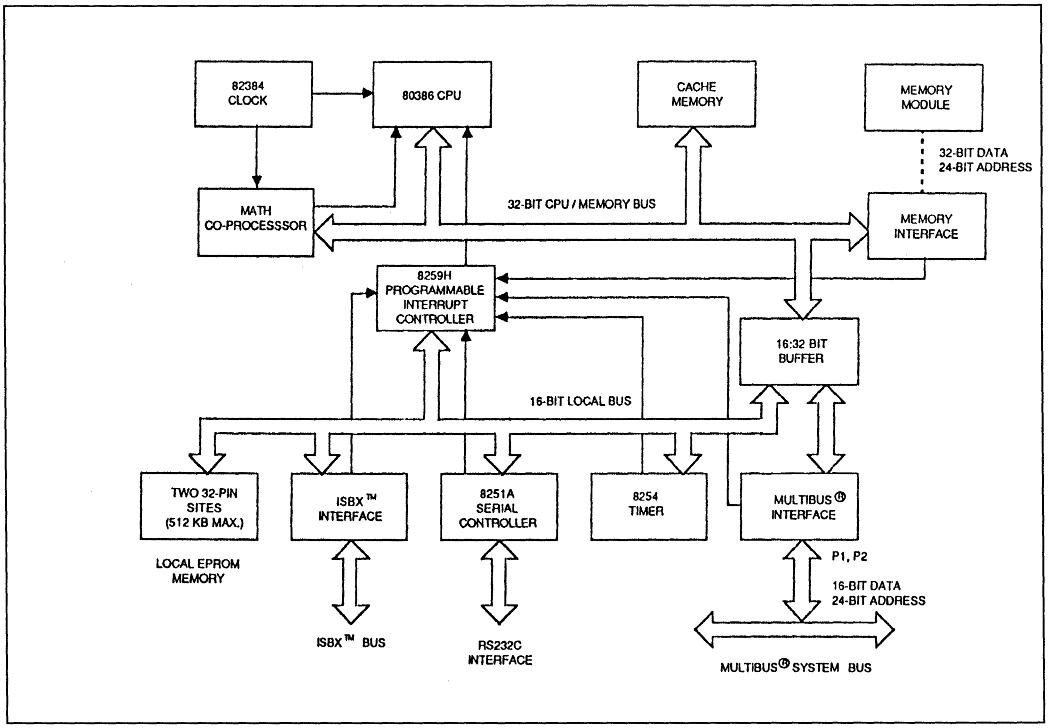


Figure 1. iSBC® 386/21/22/24/28 CPU Board Block Diagram

instructions; 8-, 16-, and 32-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data; and iterative word and byte string manipulation functions. All existing instructions have been extended to support 32-bit addresses and operands. New bit manipulation and other instructions have been added for extra flexibility in designing complex software.

Numeric Data Processor

For enhanced numerics processing compatibility, the iSBC 386/2x board includes an 80287-based math module which is installed on the iSBC 386/2x board. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The numeric data processor meets the IEEE P754 (Draft 7) standard for numeric data processing and maintains compatibility with 8087-based systems. Data transfers to and from the on-board CPU bus are 16-bits wide. Future iSBC 386/2x boards will use an 80387 numeric coprocessor in place of the math module. Boards that use an 80287-based math module may be easily upgraded by removing the module and installing an 80387 device. The 80387 will provide higher performance through a 32-bit data path to the CPU bus, added numeric instructions, and a faster clock.

Architectural Features

The 8086, 8088, 80188, 80286, and 80386 microprocessor family contain the same basic sets of registers, instructions, and addressing modes. The 80386 processor is upward compatible with the 8086, 8088, 80186, 80188, and 80286 CPU's.

Architectural Features

The 80386 operates in two modes: protected virtual address mode; and 8086 real address mode. In protected virtual address mode (also called protected mode), programs use virtual addresses. In this mode, the 80386 CPU automatically translates logical addresses to physical addresses. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. In 8086 real address mode, programs use real addresses with up to one megabyte of address space. Both modes provide the same base instruction set and registers.

Interrupt Control

Incoming interrupts are handled by two cascaded on-board 8259A programmable interrupt controllers and by the 80386's NMI line. Twenty interrupt sources are routed to the programmable controllers and the interrupt jumper matrix. Using this jumper matrix, the user can connect the desired interrupt sources to specific interrupt levels. The interrupt controllers prioritize interrupts originating from up to 15 sources and send them to the CPU. The user can connect a sixteenth interrupt to the 80386 NMI line. Table 1 includes a list of devices and functions supported by interrupts. Bus vectored interrupts are not supported.

Table 1. Interrupt Request Sources

Source	Function	Number of Interrupts
MULTIBUS® Interface	Requests from MULTIBUS® resident peripherals or other CPU boards	8
8251A Serial Controller	Indicates status of transmit and receive buffers and RI lead of the RS232C interface	3
8254 Timers	Timer 0, 1 outputs; function determined by timer mode (hardwired to interrupt controller)	2
iSBX™ Connector	Function determined by iSBX™ MULTIMODULE™ board	4
Bus Timeout	Indicates addressed MULTIBUS® or iSBX™ resident device has not responded to a command within 10 msec	1
Power Fail Interrupt	Indicates AC power is not within tolerance (signal generated by system power supply)	1
Parity Interrupt	Indicates on-board parity error	1
Programmable Register	Generate interrupt under program control	1

Memory Capabilities

The iSBC 386/2x boards support both EPROM local memory and dynamic RAM (DRAM), which is located on-board. The DRAM is supported by a high speed on-board cache memory.

DRAM Memory

The iSBC 386/2x series CPU boards come with 1, 2, 4, or 8M bytes of DRAM memory. This memory is on a low profile module that is installed on the baseboard. The module measures approximately 4″ x 4″ and uses surface mount DRAM devices. The DRAM memory supports byte-parity error detection and has a 32-bit wide data path to the 80386 CPU and 16-bit wide data path to the MULTIBUS interface.

The memory may be expanded by installing an additional iSBC MM0x series memory module, which is available in 1, 2, 4, or 8M byte sizes. All mounting hardware is included. Maximum DRAM memory is 16M bytes using an iSBC 386/28 CPU board and an 8M byte iSBC MM08 memory module. This combination requires only 1.8 inches of cardcage space.

Cache Memory

A 64K byte cache memory on the iSBC 386/2x board supports the 80386 and provides 0 wait-state reads for data and program code resident in the cache memory. The cache memory is updated whenever data is written into the dual-port memory or when the CPU executes a read cycle and the data or program code is not present in cache memory. This process is controlled by the cache replacement algorithm. Cache "misses" require additional wait-states to retrieve data from the DRAM memory. If the processor is in pipelined mode, 2 wait-states (4 clock cycles) are required to retrieve data. If the processor is in non-pipelined mode, 3 wait-states are required. All writes to DRAM memory require 2 (pipelined) or 3 (non-pipelined) wait-states.

The cache memory supports 16K entries, with each entry comprised of a 32-bit data field and an 8 bit tag field. The tag field is used to determine which actual memory word currently resides in a cache entry. The cache memory size and effective replacement algorithm are designed to optimize both the probability of cache "hits" and local bus utilization.

EPROM Memory

The EPROM memory consists of two 32-pin JEDEC sites that are intended for boot-up and system diagnostic/monitor routines, application code, and ROM-able operating system software. Maximum local memory capacity is 512K bytes using Intel 27020 (256k X 8) 2 megabit EPROM devices. The EPROM memory resides at the upper end of the 80386 device's memory space for both real address mode and PVAM operation.

Memory Map

In real address mode, the maximum amount of addressable physical memory is 1 Mbyte. In protected virtual address mode (PVAM), the maximum amount of addressable physical memory is 16 Mbytes. The system designer can easily change the CPU memory map to adapt the CPU board to the required overall system memory map. Reconfiguration is usually necessary for multiple processor-based systems with more than two CPU boards and/or intelligent I/O boards. By changing PAL devices and/or by moving jumpers, the designer can set:

- EPROM memory space
- Starting address of DRAM memory
- Amount of DRAM memory that is dual-ported to the CPU and MULTIBUS interface or single-ported to the CPU
- Access to off-board MULTIBUS address space

EPROM Memory

The EPROM memory space is set using four jumpers to accommodate 27256 (256 kb), 27512 (512 kb), 27010 (1 Mb), or 27020 (2 Mb) byte-wide devices. Smaller EPROM devices may be used, however the EPROM will appear more than once within the EPROM address space. Using a pair of 27020 EPROMs will provide 512k bytes of memory. The iSBC 386/2x series boards are designed to accommodate EPROM devices with access times ranging from 130-320 ns. In real address mode, the ending address of EPROM memory is always 1M byte (FFFFFH). In PVAM, the ending address of EPROM memory is always 4G bytes (FFFF FFFFH), which is the top of the 80386 address space.

DRAM Memory Size/Location

The iSBC 386/2x boards allow the user to control the location and size of the DRAM memory (on the iSBC 386/2x board) available for use by the CPU and other boards in the system. In PVAM, the starting address of DRAM can be set to start on any 1M byte boundary up through 15M bytes by setting jumpers and by installing a custom-programmed PAL device. In real address mode, the DRAM memory always starts at 0H (hex).

The ending address can be set on 64k byte boundaries using jumpers in both PVAM and real address mode. Setting the ending address at lower than the actual amount of installed memory effectively deselects a portion of DRAM and creates additional MULTIBUS address space.

MULTIBUS Address Space

Any address space not set aside as EPROM or DRAM memory automatically becomes address space the CPU can use to access other boards in the system. For example, Fig. 2A shows a real address mode CPU memory map for a 1M byte iSBC 386/21 board. With the DRAM ending address set at 512k bytes and 128k bytes of installed EPROM, 384k bytes of MULTIBUS address space is accessable by the CPU. Fig. 2B shows a typical PVAM configuration where the 4 Mbytes of DRAM has been set to start at 1M byte and end at 4.5M bytes. The address space from 0 to 1M byte and 4.5 to 16M bytes is the MULTIBUS address space accessable by the CPU.

Fig. 2C illustrates another way the board can establish additional MULTIBUS address space. If the DRAM memory starts at 0, a jumper on the board can be used to create additional MULTIBUS address space between 512k bytes and 1M byte. This feature is available both in real address mode and PVAM.

Dual-Port/Local Memory

A portion or all of the DRAM memory can be selected to be dual-port (shared) memory. Both the starting and ending addresses are set on 256k byte boundaries using jumpers on the board. Any DRAM memory that is not configured as dual-port memory is local (single-port) memory available only to the CPU.

Programmable Timer

Three 16-bit, programmable interval timer/counters are provided using an 8254 device, with one timer dedicated to the serial port for use as a baud rate generator. The other two timers can be used to generate accurate time intervals under software control. The timers are not cascadable. Four timer/counter modes are available as listed in Table 2. Each counter is capable of operating in either BCD or binary modes. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Rate generator	Divide by N counter. The output will go lwo for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go lwo for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.

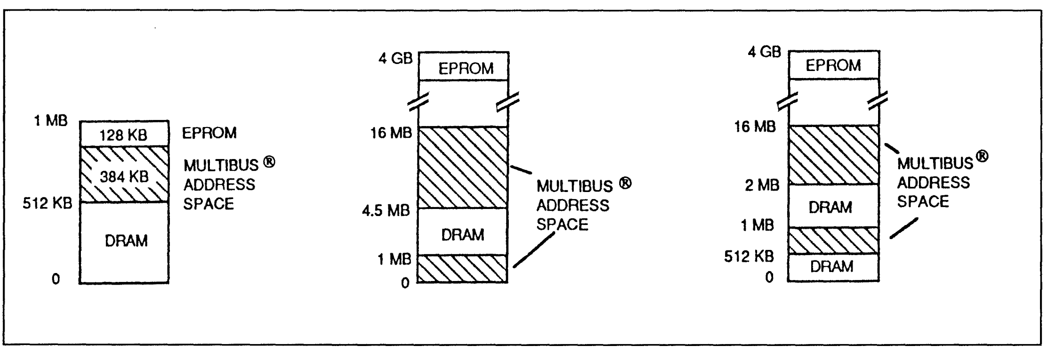


Fig. 2A. Real Address Mode iSBC® 386/21 Board Memory Map

Fig. 2B PVAM iSBC® 386/24 Board Memory Map

Fig. 2C. PVAM iSBC® 386/22 Board Memory Map

Serial I/O

The iSBC 386/2x board includes one RS232C serial channel, which is configured as an asynchronous, DTE interface. Data rates up to 19.2k baud may be selected. The serial channel can connect either to a host system for software development or to a stand alone terminal for field diagnostic support. For stand alone use, unhosted monitor software needs to be programmed by the user into the local EPROM memory. The serial channel may also be connected to a modem to provide remote diagnostic support or to download program codes. The physical interface is a 10-pin ribbon-style connector located on the front edge of the board.

iSBX™ Interface

For iSBX MULTIMODULE support, the iSBC 386/2x CPU board provides an 8/16-bit iSBX connector that may be configured for use with either 8- or 16-bit, single or double-wide iSBX MULTIMODULE boards. Using the iSBX interface, a wide variety of specialized I/O functions can be added easily and inexpensively to the iSBC 386/2x board.

Reset Functions

The iSBC 386/2x boards are designed to accept an Auxilliary Reset signal via the boards' P2 interface. In this way, system designs that require front panel reset switches are supported. The iSBC 386/2x boards use the AUX reset signal to reset all on-board logic (excluding DRAM refresh circuitry) and other boards in the MULTIBUS system. The iSBC 386/2x boards will also respond to an INIT reset signal generated by another board in the system.

LED Status Indicators

Mounted on the front edge of the iSBC 386/2x board are four LED indicators that indicate the operating status of the board and system. One LED is used to show that an on-board parity error or a MULTIBUS bus parity error has occurred. A second LED indicates that a MULTIBUS or iSBX bus access timeout has occurred. The third LED is triggered by the start of an 80386 bus cycle and will turn off if the 80386 CPU stops executing bus cycles. The fourth LED will light under software control if the program writes to a specific I/O location.

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the MULTIBUS system bus, the iLBX local bus extension and the iSBX MULTIMODULE expansion bus. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The iLBX bus, which is usually used for memory expansion, is not supported by the iSBC 386/2x boards since all DRAM memory is located on-board. The iSBX bus provides a low cost way to add I/O to the board.

System Bus — IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a broad array of board level products, VLSI interface components, detailed published specifications and application notes.

System Bus — Expansion Capabilities

The user can easily expand or add features to his system by adding various MULTIBUS boards to his system. Products available from Intel and others include: video controllers; D/A and A/D converter boards; peripheral controller cards for floppy disk, hard disk, and optical disk drives; communications/networking boards; voice synthesis and recognition boards: and EPROM/bubble memory expansion boards.

System Bus — Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers sharing system tasks through communication over the system bus), the iSBC 386/2x boards provide full system bus arbitration control logic. This control logic allows up to four bus masters to share the system bus using a serial (daisy chain) priority scheme. By using an external parallel priority decoder, this may be extended to 16 bus masters. In addition to multiprocessing, the multimaster capability also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

iSBX™ Bus MULTIMODULE™ On-Board Expansion

One 8-/16-bit iSBX MULTIMODULE interface is provided on the iSBC 386/2x microcomputer boards. Through this interface, additional on-board I/O functions may be added, such as parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., floppy disks), BITBUS Control, and other custom interfaces to meet specific needs. Compared to other alternatives such as MULTIBUS I boards, iSBX modules need less interface logic and power, and offer simpler packaging and lower cost. The iSBX interface connector on the iSBC 386/2x boards provides all the signals necessary to interface to the local on-board bus, and is compatible with both 8-bit and 16-bit MULTIMODULES. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed using Intel's "MULTIBUS I Architecture Reference Book" (order no. 210883) as a guide.

SOFTWARE SUPPORT

Operating Systems

Both the iRMX 286 Release 2 operating system and the System V/386 UNIX*-based operating system will support the iSBC 386/2x boards.

The iRMX 286 Release 2 operating system is a real-time multi-tasking and multi-programming software system capable of executing all the configurable layers of the iRMX 286 operating system on the 80386 microprocessor and the iSBC 386/2x single board computers. Up to 16 MB of physical system memory is supported. The iRMX 286 Operating System also allows the user to take advantage of the hardware traps built into the 80386 processor that provide expanded debug capabilities and increased code reliability.

The iRMX 286 Release 2 operating system is designed to support time-critical applications requiring real time performance in the industrial automation, financial, medical, communications, and data acquisition and control (including simulation) marketplaces.

Application code written under the iRMX 86 operating system can also run on the iSBC 386/2x boards. The code must first be recompiled using Intel's 286 compilers and then run under iRMX 286 release 2 software. Application code will require only minor changes.

Applications software written for Release 1 of the iRMX 286 Operating Systems is upward compatible with iRMX 286 Release 2 software. Assembly and many high level languages are supported by the iRMX Operating System and Intellec Series III and Series IV development systems. Language support for the iSBC 386/2x boards in real address mode includes Intel's ASM 286, PL/M 286, PASCAL 286, and FORTRAN 286. Programs developed in these languages can be downloaded from an Intel Series III or IV Development System to the iSBC 386/2X boards via the iSDM Release 3 System Debug Monitor. The iSDM release 3 monitor also provides on-target program debugging support including breakpoint and memory examination features.

For customers preferring a UNIX-based operating system, Intel will offer System V/386. Intel's System V/386 is a fully licensed derivative of UNIX V.3 enhanced by Intel to provide device driver support for Intel board products plus other features that yield greater flexibility, increased reliability, and easier configurability. Intel's System V/386 operating system has been optimized for use with the 80386 microprocessor and supports such features as on-chip memory management and protection that provide ease of portability and higher performance.

Languages and Tools

A wide variety of languages will be available for the iRMX and System V/386 operating systems. For the iRMX 286 Release 2 operating system, Intel will be offering UNIX, ASM 286, Pascal 286, PL/M 286, C 286, and FORTRAN 286. For the System V/386 Operating System several different software vendors will be providing complete selections of languages, including ASM, C, PASCAL, FORTRAN, COBOL, RPG, PL1, BASIC, and Artificial Intelligence programming languages LISP and Arity/Prolog. Software development tools will include PSCOPE Monitor 386 (PMON 386 and DMON 386), Softscope 286 (for iRMX 286 Release 2), and an ICE 386 in-circuit-emulator.

*UNIX is a trademark of AT&T Bell Labs

System Compatibility

The iSBC 386/2x Single Board Computers are complemented by a wide range of MULTIBUS hardware and software products from over 200 manufacturers worldwide. This product support enables the designer to easily and quickly incorporate the iSBC 386/2x boards into his system design to satisfy a wide range of high performance applications.

Applications that use other 16-bit MULTIBUS single board computers (such as Intel's iSBC 286/10A and iSBC 286/12 8 MHz, 80286 based single board computers) can be easily upgraded to use the iSBC 386/2x boards. Only minor changes to hardware and systems software (for speed and I/O configuration dependent code) may be required.

BOARD SPECIFICATIONS

Word Size

Instruction — 8, 16, 24, 32 or 40 bits
Data — 8, 16, 32 bits

System Clock

80386 CPU — 16 MHz
Numeric Processor — 80287 module — 10 MHz

Cycle Time

Basic Instruction — 16 MHz — 125 ns (assumes instruction in queue)

Note: Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles)

DRAM Memory

On-board parity memory:
- iSBC 386/21 board — 1M byte
- iSBC 386/22 board — 2M bytes
- iSBC 386/24 board — 4M bytes
- iSBC 386/28 board — 8M bytes

Memory expansion — One additional plug-in module:
- iSBC MM01 — 1M byte
- iSBC MM02 — 2M bytes
- iSBC MM04 — 4M bytes
- iSBC MM08 — 8M bytes

Maximum Addressable Physical Memory —
16 Megabytes (protected virtual address mode)
1 Megabyte (real address mode)

EPROM Memory

Number of sockets — Two 32-pin JEDEC Sites (compatible with 28-pin and 32-pin devices)
Sizes accommodated — 64 kb (8k x 8), 128 kb (16k x 8), 256 kb (32k x 8), 512 kb (64k x 8), 1 Mb (128k x 8), 2 Mb (256k x 8)
Device access speeds — 130 to 320 ns
Maximum memory — 512k bytes with 27020 (2M bit) EPROMs

I/O Capability

Serial Channel —

Type — One RS232C DTE asynchronous channel using an 8251A device

Data Characteristics — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; automatic break detect and handling; even/odd parity error generation and detection

Speed — 110, 150, 300, 600, 1.2 kb, 2.4 kb, 4.8 kb, 9.6 kb, 19.2 kb

Leads supported — TD, RD, RTS, CTS, DSR, RI, CD, SG

Connector Type — 10 pin ribbon

Expansion — One 8/16-bit iSBX interface connector for single or double wide iSBX MULTIMODULE board.

Interrupt Capacity

Potential Interrupt Sources — 21 (2 fixed, 19 jumper selectable)

Interrupt Levels — 16 using two 8259A devices and the 80386 NMI line

Timers

Quantity — Two programmable timers using one 8274 device

Input Frequency — 1.23 MHz ±0.1%

Output Frequencies/Timing Intervals

Function	Single Counter	
	Min	Max
Real-time interrupt	1.63 usec	53.3 ms
Rate Generator	18.8 Hz	615 kHz
Square-wave rate generator	18.8 Hz	615 kHz
Software triggered strobe	1.63 usec	53.3 ms

Interfaces

MULTIBUS Bus — All signals TTL compatible
iSBX Bus — All signals TTL compatible
Serial I/O — RS 232C, DTE

MULTIBUS® DRIVERS

Function	Type	Sink Current (ma)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	32
Bus Control	Open Collector	16/32

Power Requirements

iSBC 386/2x board
Maximum: +5V, 13A
±12V, 35 ma
Typical: +5V, 9A
±12V, 20 ma

Note: Does not include power for iSBX module, EPROM memory, or added iSBCMM0x memory module.

Environmental Requirements

Operating Temperature — 0 to 60°C at 300 LFM
Relative Humidity — 0 to 85% noncondensing
Storage Temperature — −40 to 70°C

Physical Characteristics

Dimensions
Width — 12.00 in. (30.48 cm)
Height — 7.05 in. (17.91 cm)
Depth — 0.86 in. (2.18 cm), 1.62 in. (4.11 cm) with added memory module

Recommended Minimum Cardcage Slot Spacing
1.2 in. (3.0 cm), with or without iSBX MULTIMODULE
1.8 in. (4.6 cm), with added iSBC MM0x memory module

Approximate Weight
26 oz. (738 gm)
29 oz. (823 gm), with added iSBC MM0x memory module

Reference Manual

149094 — iSBC 386/21/22/24/28 Hardware Reference Manual (order separately)

Ordering Information

Part Number	Description
SBC38621	16 MHz 80386 MULTIBUS I CPU Board with 1 MB DRAM Memory
SBC38622	16 MHz 80386 MULTIBUS I CPU Board with 2 MB DRAM Memory
SBC38624	16 MHz 80386 MULTIBUS I CPU Board with 4 MB DRAM Memory
SBC38628	16 MHz 80386 MULTIBUS I CPU Board with 8 MB DRAM Memory
SBCMM01	1 MB Parity DRAM Memory Expansion Module
SBCMM02	2 MB Parity DRAM Memory Expansion Module
SBCMM04	4 MB Parity DRAM Memory Expansion Module
SBCMM08	8 MB Parity DRAM Memory Expansion Module

Mating Connectors

Function	No. of Pins	Centers (in)	Connector Type	Vendor*	Vendor Part Number*
iSBX Bus Connector	44	0.1	Soldered	Viking	000293-0001
Serial RS232C Connector	10	0.1	Flat Crimp	3M	3399-6010
P2 Interface Edge Connector	60	0.1	Flat Crimp	Kel-AM T&B Ansley	RF30-2803-5 A3020

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TWX: 910-595-1114

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910-338-0255

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Colorado Springs 80907
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TWX: 710-456-1199

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Tel: (305) 869-5588

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TWX: 510-956-9407

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Nordisk Elektronic (Norge) A/S
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Smedsvingen 4
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Tel: (2) 846 210
TELEX: 17546

PORTUGAL

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Componentes E Electronica LDA
Av. Miguel Bombarda, 133
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Miguel Angel 21, 6 Piso
Madrid 10
Tel: (34) 14 1954 00
TELEX: 27461

Diode Espana
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28020 Madrid
Tel: 455 36 86
TELEX: 42148

SWEDEN

Nordisk Electronik AB
Huvudstagatan 1
Box 1409
S-171 27 Solna
Tel: (8) 734 97 70
TELEX: 10547

SWITZERLAND

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Market Street
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Tel: (344) 55333
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TELEX: 95142

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Tel: (190) 49307
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Rapid Recall, Ltd.
Rapid House/Denmark St
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Bucks HP11 2ER
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TELEX: 837931

YUGOSLAVIA

H. R. Microelectronics Enterprises
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