DIFFERENCES BETWEEN iSBC 86/12™ AND iSBC 86/12A™ SINGLE BOARD COMPUTER REFERENCE MANUAL 9800645-02

Manual Order Number: 9803092-01

NOTE

This addendum supplements the information presented in the iSBC 86/12™ Hardware Reference Manual.

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DESCRIPTION OF DIFFERENCES AND ADDED FEATURES

INTRODUCTION

The iSBC 86/12A Single Board Computer as shipped (factory default wiring) is functionally the same as the iSBC 86/12 Single Board Computer and is plug-to-plug compatible. This addendum describes the physical differences between the iSBC 86/12 Single Board Computer and the iSBC 86/12A Single Board Computer. The additional features that have been added to the iSBC 86/12A board are also described.

The iSBC 86/12 board contains a piggyback board at location J12 (lower left corner). This piggyback board handles the bus arbitration. On the iSBC 86/12A board, the piggyback board has been replaced by a single 8289 Bus Arbiter IC.

With the inclusion of the 8289 Bus Arbiter, the iSBC 86/12A board physically occupies only one card slot in an iSBC 604/614 Modular Cardcage.

The 8289 Bus Arbiter operates in conjunction with the 8288 Bus Controller to interface the 8086 processor to a Multibus interface. The 8289 Bus Arbiter can operate in several modes (which offer enhancements that were not on the iSBC 86/12 boards), depending on how it is jumper wired and the status of the Multibus interface signal Common Bus Request (CBRQ/). It is recommended that the 8289 data sheet be read before continuing with this addendum.

COMMON BUS REQUEST.

Common Bus Request (CBRQ/), a new bidirectional Multibus interface signal, is used to allow a bus master to retain control of the system bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the bus but not currently controlling it, asserts CBRQ/. This causes the controlling bus master to relinquish control of the bus when the proper surrender conditions exist (see table 1 for surrender conditions, figure 3 for CBRQ/timing, and tables 2 and 3 for DC and AC characteristics).

The CBRQ/ pins of all the bus master devices that support CBRQ/, are connected together on the iSBC 604/614 modular backplane (reference figure 1 and 2). When a bus master needs a bus resource, it informs the other bus masters that it is requesting the bus by activating CBRQ/, BREQ/ and/or BPRO/. When the controlling master releases the bus, the bus exchange operates the same as described in paragraph 4-26 of the iSBC 86/12 Single Board Computer Hardware Reference Manual.

The advantage of using CBRQ/ is to improve the bus access time by allowing a bus master to retain control of the bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus.

ANY REQUEST

The 8289 Bus Arbiter has a jumper option (ANY-RQST) that controls, in conjunction with BPRN/ and CBRQ/, under what conditions the Multibus interface will be surrendered. The following paragraphs describe this option.

When ANYRQST is jumpered to a low level (E130-E131), the Bus Arbiter that has control of the Multibus interface will retain control unless one of the following conditions exist.

- 1. A higher priority bus master requests the Multibus interface (as indicated by the BPRN/ signal going high).
- 2. The next machine cycle of the iSBC 86/12A board does not require the use of Multibus interface and CBRQ/ is low.

When ANYRQST is jumpered to a high level (E129–E130), it permits the Multibus interface to be surrendered to a higher priority bus master as well as a lower priority bus master as though it were a bus master of higher priority. A lower priority master indicates it is requesting the Multibus interface by activating CBRQ/. When this option is used, the bus master that is in control will surrender the bus as soon as possible.

If the CBRQ/pin on the 8289 Bus Arbiter is jumpered to ground (E144-E143), removing it from the Multibus interface, and ANYRQST is jumpered to a high level (E129-E130), the Multibus interface is surrendered after each transfer cycle (this is the factory wired default option).

SCHEMATIC DIAGRAM

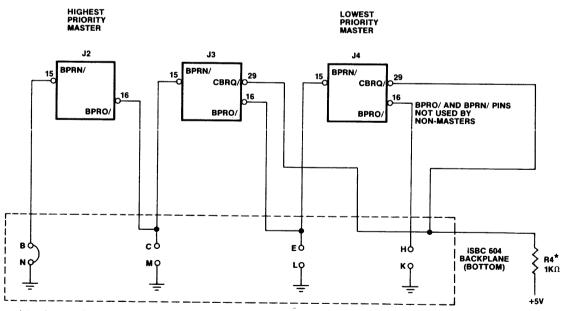
The schematic diagram (figure 5-2, sheet 3) of the bus arbiter, labeled J12, is pin-for-pin the same as the 8289 Bus Arbiter.

JUMPER CONFIGURATIONS

Table 1 lists the various jumper configurations for the 8239 Bus Arbiter.

Table 1. 8289 Bus Arbiter Jumper Configurations

ONFIGURATION NUMBER	JUMPER CONN	CBRQ/	ANYRQST	DESCRIPTION
1	E144-E145 E130-E131	Low	Low	The Bus Arbiter that has control of the Multibus interface will retain control unless a higher priority master activates CBRQ/ or if the next machine cycle does not require the use of the Multibus interface it will be relinquished to a lower priority device.
		High	Low	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2	E144-E145 E129-E130	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender control to the Bus Arbiter that is pulling CBRQ/low, regardless of its priority, upon completion of the current bus cycle.
		High	High	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
1	E143-E144* E129-E130*	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender the use of the Multibus interface after each transfer cycle.

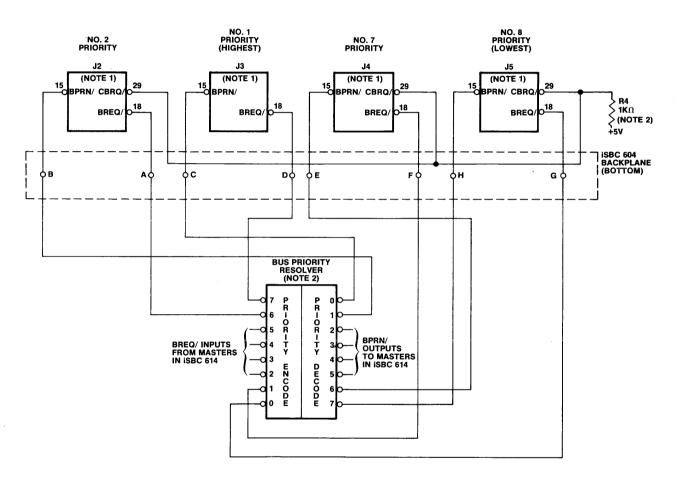


^{*}Pull-up resistor is supplied by the customer.

NOTE: All non CBRQ/ devices must have higher priority. If a non CBRQ/ device is placed at a lower priority, it will not be able to gain control of the Multibus interface.

PSI11

Figure 1. Serial Priority Resolution Scheme

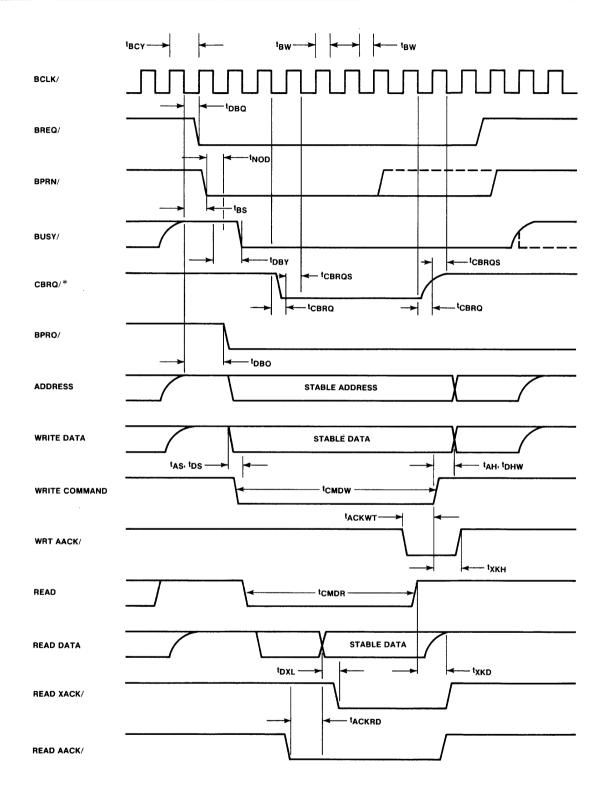


NOTES:

- 1. Refer to paragraph 2-20 in the iSBC 86/12 Single Board Computer Hardware Reference Manual regarding the disabling of BPRO/.
- 2. Supplied by the customer.

PSI13

Figure 2. Parallel Priority Resolution Scheme



 $^{^{*}}$ CBRQ/ timing not shown relative to other bus signals other than BCLK/.

PSI12

Figure 3. Bus Exchange Timing

Table 2. iSBC 86/12 DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	∙Max.	Units
AACK/, XACK/	V _{OL}	Output Low Voltage	I _{OL} = 16 mA		.04	٧
	VoH	Output High Voltage	$I_{OH} = -3 \text{ mA}$	2.0		V
	VIL	Input Low Voltage			8.0	V
	V _{IH}	Input High Voltage		2.0		V
	I _{IL}	Input Current at Low V	$V_{IN} = 0.4V$		-2.2	mA
	l _{IH}	Input Current at High V	$V_{IN} = 2.4V$		-1.4	mA
	*C _L	Capacitive Load			15	pF
ADR0/-ADRF/	V _{OL}	Output Low Voltage	I _{OL} = 32 mA		0.55	٧
ADR10/-ADR13/	Voн	Output High Voltage	$I_{OH} = 3 \text{ mA}$	2.4		V
	V _{IL}	Input Low Voltage			0.8	V
	V _{IH}	Input High Voltage		2.0		V
	l _{IL}	Input Current at Low V	$V_{IN} = 0.45V$		-0.50	mA
	Ин	Input Current at High V	$V_{IN} = 5.25V$		50	μ A
	1 _{LH}	Output Leakage High	$V_0 = 5.25V$		-0.50	mA
	ILL	Output Leakage Low	$V_0 = 0.45V$		-0.50	mA
	*C _L	Capacitive Load			18	pF
BCLK/	V _{OL}	Output Low Voltage	I _{OL} = 59.5 mA		0.5	٧
	Voh	Output High Voltage	$I_{OH} = -3 \text{ mA}$	2.7	i	V
	VIL	Input Low Voltage			0.8	V
	V _{IH}	Input High Voltage		2.0	'	V
	l _{IL}	Input Current at Low V	$V_{IN} = 0.45V$		-0.5	mA
	Ин	Input Current at High V	$V_{IN} = 5.25V$		40	μΑ
	*C _L	Capacitive Load			15	pF
BHEN/	V _{OL}	Output Low Voltage	I _{OL} = 16 mA		0.4	٧
	V _{OH}	Output High Voltage	$I_{OH} = -2.0 \text{ mA}$	2.4		V
	VIL	Input Low Voltage			0.8	V
	V _{IH}	Input High Voltage		2.0		V
	IIL	Input Current at Low V	$V_{IN} = 0.4V$		1.6	mA
	l _{IH}	Input Current at High V	$V_{IN} = 2.4V$		40	μΑ
	*CL	Capacitive Load			15	pF
BPRN/	VIL	Input Low Voltage			0.8	V
	V _{IH}	Input High Voltage		2.0		V
	I _{IL}	Input Current at Low V	$V_{IN} = 0.4V$		-0.5	mA
	l _{IH}	Input Current at High V	$V_{IN} = 5.25V$		50	μΑ
	*C _L	Capacitive Load			18	pF
BPRO/	V _{OL}	Output Low Voltage	I _{OL} = 3.2 mA		0.45	V
	Voн	Output High Voltage	$I_{OH} = -0.4 \text{ mA}$	2.4		V
	*C _L	Capacitive Load			15	pF
BREQ/	V _{OL}	Output Low Voltage	I _{OL} = 50 mA		0.45	V
	Voн	Output High Voltage	I _{OH} = 0.4 mA	2.4		V
	*CL	Capacitive Load			10	pF
BUSY/, CBRQ/,	V _{OL}	Output Low Voltage	I _{OL} = 20 mA		0.4	٧
INTROUT/ (OPEN COLLECTOR)	*CL	Capacitive Load			20	pF

Table 2. iSBC 86/12 DC Characteristics (Continued)

Voh	Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
PF C Capacitive Load 15 PF	CCLK/	V _{OL}	Output Low Voltage	I _{OL} = 60 mA		0.5	V
DATG-DATF/		V _{ОН}	Output High Voltage	$I_{OH} = -3 \text{ mA}$	2.7		V
Voh		*CL	Capacitive Load			15	pF
ViL	DAT0/-DATF/	V _{OL}	Output Low Voltage	I _{OL} = 32 mA		0.45	V
Vih		V _{ОН}	Output High Voltage	$I_{OH} = -5 \text{ mA}$	2.4		V
In Input Current at Low Vo Vo 0.45 Vo 0.25 Vo 0		1	· ·			0.80	
ILH					2.0		
**C _L		1	,	I			
INH1/		l .	1	$V_0 = 5.25V$			
V _{IH}		*C _L	Capacitive Load			18	pF
III	INH1/	VIL	Input Low Voltage			0.8	
I I I Input Current at High (SYSTEM RESET) Vol. Capacitive Load Vol. Capacitive Load I Input Low Voltage (SYSTEM RESET) Vol. Output Low Voltage Input Ligh Voltage Input Ligh Voltage Input Ligh Voltage Input Low Voltage Input Low Voltage Input Low Voltage Input Low Voltage Input Current at Low V Vin. 2.4V -4.2 mA Input Current at High V Vin. 2.4V -1.4 mA Input Current at Low V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.4V -1.6 mA Input Current at High V Vin. 2.525 Indicate Input Current at Low V Input Low Voltage Vol. Capacitive Load Input Current at Low V Input Low Voltage Vol. Capacitive Load Input Current at Low V Input High Voltage Vol. Input Low Voltage Vol. Input Current at Low V Vol. Input Current at High V Vol. Input Curren		V _{IH}	1 ' "		2.0		V
NITO/-INT7/ Vol. Capacitive Load Iab pF			1 '				
INIT/ (SYSTEM RESET)			1	$V_{IN} = 2.7V$			-
OPEN COLLECTOR OPE		*C _L	Capacitive Load			18	pF
V _{IL}		VoL	Output Low Voltage	I _{OL} = 44 mA		0.4	V
V _{IL}	(SYSTEM RESET)	V _{OH}	Output High Voltage	5			
VIH		Vii	Input Low Voltage	COLLECTOR		0.8	V
IIL Input Current at Low V VIN = 0.4V VIN = 2.4V -4.2 mA IIH Input Current at High V VIN = 2.4V -1.4 mA *CL Capacitive Load 15 pF INTO/-INT7/ VIL Input Low Voltage Input High Voltage Input High Voltage Input Low Voltage Input Current at Low V VIN = 0.4V -1.6 mA IIH Input Current at High V VIN = 2.4V 40 μA *CL Capacitive Load 18 pF IORC/. IOWC/ VOL Output Low Voltage IOL = 32 mA VIN = 2.4V VIN = 2.4V ILH Output Leakage High VO = 5.25V 100 μA ILL Output Leakage Low VO = 0.45V -100 μA *CL Capacitive Load 15 pF INTA/. MRDC/. VOL Output Low Voltage IOL = 30 mA ION = -5 mA 2.4 VIN = -5 mA VOL Output Low Voltage IOL = 30 mA ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA 2.4 VIN = -5 mA VOL Output High Voltage ION = -5 mA ION = -5 mA VOL Output High Voltage					2.0		
I			1	$V_{IN} = 0.4V$		-4.2	mA
*CL			Input Current at High V			-1.4	mA
V H Input High Voltage I IL Input Current at Low V V IN = 0.4V V Input Current at Low V V Input Current at High V V Input Current at Low V Input Current at Low V Input Current at Low V V Input Current at Low V V Input Current at High V		*C _L	Capacitive Load			15	pF
V H Input High Voltage I IL Input Current at Low V V IN = 0.4V V Input Current at Low V V Input Current at High V V Input Current at Low V Input Current at Low V Input Current at Low V V Input Current at Low V V Input Current at High V	INTO/-INT7/	V _{II}	Input Low Voltage			0.8	V
I I I Input Current at Low V I Input Current at High V V Input Current at High		1	_		2.0		V
*C _L Capacitive Load 18 pF		1	Input Current at Low V	$V_{IN} = 0.4V$		-1.6	mA
IORC/, IOWC/		I _{IH}	Input Current at High V	$V_{IN} = 2.4V$		40	μΑ
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		*C _L	Capacitive Load			18	pF
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	IORC/, IOWC/	Vol	Output Low Voltage	loi = 32 mA		0.45	V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			Output High Voltage		2.4		V
*CL Capacitive Load 15 pF INTA/, MRDC/. WOL Output Low Voltage $I_{OL} = 30 \text{ mA}$ 0.45 V VoL Output High Voltage $I_{OH} = -5 \text{ mA}$ 2.4 V VIL Input Low Voltage $I_{OH} = -5 \text{ mA}$ 0.95 V VIH Input High Voltage $I_{OH} = -20 \text{ mA}$ 2.0 mA Input Current at Low V Input Current at High V Input Current at High V VIN = 0.45V -2.0 mA Input Current at High V VIN = 5.25 1000 μ A			Output Leakage High			100	μA
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		ارر	Output Leakage Low	$V_0 = 0.45V$		-100	μΑ
MWTC/		*C _L	Capacitive Load			15	pF
MWTC/	INTA/, MRDC/. MWTC/	V _{OL}	Output Low Voltage	I _{OL} = 30 mA	1	0.45	٧
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			· -	1	2.4		V
I_{IL} Input Current at Low V $V_{IN} = 0.45$ V -2.0 mA Input Current at High V $V_{IN} = 5.25$ 1000 μA		VIL				0.95	V
I _{IH} Input Current at High V V _{IN} = 5.25 1000 μA		V _{IH}	Input High Voltage		2.0		V
		կլ	Input Current at Low V	i		-2.0	mA
*C _L Capacitive Load 25 pF		Iн	Input Current at High V	$V_{1N} = 5.25$		1000	μ A
		*C _L	Capacitive Load			25	pF

Table 3. iSBC 86/12 AC Characteristics (Master Mode)

Parameter	Minimum (ns)	Maximum (ns)	Description	Remarks
tas	50		Address setup time to command	
tah	50		Address hold time from command	
tos	50		Data setup to write CMD ,	
tDHW	50		Data hold time from write CMD	
tcy	198	202	CPU cycle time	
t _{CMDR}	430		Read command width	No wait states
tCMDW	430		Write command width	With 1 wait state
tcswr	380		Read-to-write command separation	In override mode
tcsrr	380		Read-to-read command separation	In override mode
tcsww	580		Write-to-write command separation	In override mode
tcsnw	580		Write-to-read command separation	In override mode
txACK1	-208		Command to XACK first sample point	In override mode
tsam	202	210	Time between XACK samples	In override mode
tacked	115		AACK to valid read data	When AACK is used
tackwt	205		AACK to write command inactive	When AACK is used
tohr	0		Read data hold time	
toxL	-115		Read data setup to XACK	
txkh	0		XACK hold time	
t _{XKD}	0		AACK or XACK turn off delay	
t _{BWS}	35	∞	Bus clock low or high intervals	Supplied by system
tes	23		BPRN to BCLK setup time	
t _{DBY}		55	BCLK to BUSY delay	
t _{CBRQ}	0	60	BCLK to CBRQ	
	35		CBRQ to BCLK setup time	
^t CBRQS ^t NOD		30	BPRN to BPRO delay	
t _{DBQ}	35		BCLK/ to bus request	
t _{DBO}	40		BCLK/ to bus priority out	
tBCY	108	109	Bus clock period (BCLK)	From iSBC 86/12 board when terminated
t _{BW}	35	74	Bus clock low or high interval	From iSBC 86/12 board when terminated
tinit	3000		Initialization width	After all voltages have stabilized