DIFFERENCES BETWEEN iSBC 86/12™ AND iSBC 86/12A™ SINGLE BOARD COMPUTER REFERENCE MANUAL 9800645-02

Manual Order Number: 9803092-01

NOTE

This addendum supplements the information presented in the iSBC 86/12™ Hardware Reference Manual.

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

Printed in U.S.A. A 72/679/7.5K DD

DESCRIPTION OF DIFFERENCES AND ADDED FEATURES

INTRODUCTION

The iSBC 86/12A Single Board Computer as shipped (factory default wiring) is functionally the same as the iSBC 86/12 Single Board Computer and is plug-to-plug compatible. This addendum describes the physical differences between the iSBC 86/12 Single Board Computer and the iSBC 86/12A Single Board Computer. The additional features that have been added to the iSBC 86/12A board are also described.

The iSBC 86/12 board contains a piggyback board at location J12 (lower left corner). This piggyback board handles the bus arbitration. On the iSBC 86/12A board, the piggyback board has been replaced by a single 8289 Bus Arbiter IC.

With the inclusion of the 8289 Bus Arbiter, the iSBC 86/12A board physically occupies only one card slot in an iSBC 604/614 Modular Cardcage.

The 8289 Bus Arbiter operates in conjunction with the 8288 Bus Controller to interface the 8086 processor to a Multibus interface. The 8289 Bus Arbiter can operate in several modes (which offer enhancements that were not on the iSBC 86/12 boards), depending on how it is jumper wired and the status of the Multibus interface signal Common Bus Request (CBRQ/). It is recommended that the 8289 data sheet be read before continuing with this addendum.

COMMON BUS REQUEST.

Common Bus Request (CBRQ/), a new bidirectional Multibus interface signal, is used to allow a bus master to retain control of the system bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus. A bus master requesting control of the bus but not currently controlling it, asserts CBRQ/. This causes the controlling bus master to relinquish control of the bus when the proper surrender conditions exist (see table 1 for surrender conditions, figure 3 for CBRQ/ timing, and tables 2 and 3 for DC and AC characteristics).

The CBRQ/ pins of all the bus master devices that support CBRQ/, are connected together on the iSBC 604/614 modular backplane (reference figure 1 and 2). When a bus master needs a bus resource, it informs the other bus masters that it is requesting the bus by activating CBRQ/, BREQ/ and/or BPRO/. When the controlling master releases the bus, the bus exchange operates the same as described in paragraph 4-26 of the *iSBC 86/12 Single Board Computer Hardware Reference Manual.*

The advantage of using CBRQ/ is to improve the bus access time by allowing a bus master to retain control of the bus without contending for it each transfer cycle, as long as no other master is requesting control of the bus.

ANY REQUEST

The 8289 Bus Arbiter has a jumper option (ANYRQST) that controls, in conjunction with BPRN/ and CBRQ/, under what conditions the Multibus interface will be surrendered. The following paragraphs describe this option.

When ANYRQST is jumpered to a low level (E130–E131), the Bus Arbiter that has control of the Multibus interface will retain control unless one of the following conditions exist.

1. A higher priority bus master requests the Multibus interface (as indicated by the BPRN/ signal going high).
2. The next machine cycle of the iSBC 86/12A board does not require the use of Multibus interface and CBRQ/ is low.

When ANYRQST is jumpered to a high level (E129–E130), it permits the Multibus interface to be surrendered to a higher priority bus master as well as a lower priority bus master as though it were a bus master of higher priority. A lower priority master indicates it is requesting the Multibus interface by activating CBRQ/. When this option is used, the bus master that is in control will surrender the bus as soon as possible.

If the CBRQ/ pin on the 8289 Bus Arbiter is jumpered to ground (E144-E143), removing it from the Multibus interface, and ANYRQST is jumpered to a high level (E129-E130), the Multibus interface is surrendered after each transfer cycle (this is the factory wired default option).

SCHEMATIC DIAGRAM

The schematic diagram (figure 5-2, sheet 3) of the bus arbiter, labeled J12, is pin-for-pin the same as the 8289 Bus Arbiter.

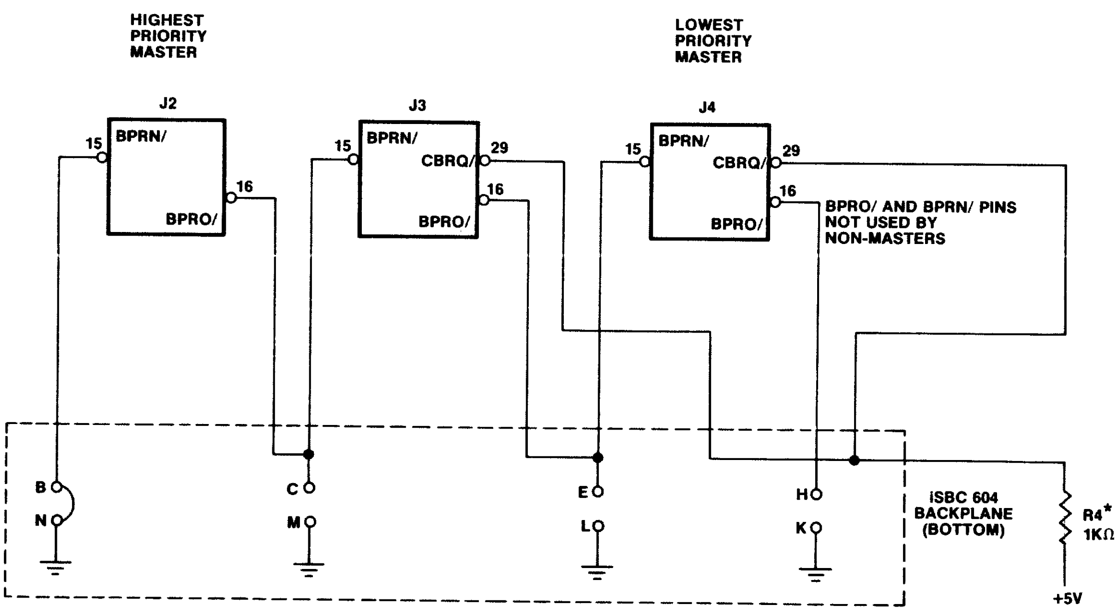
JUMPER CONFIGURATIONS

Table 1 lists the various jumper configurations for the 8239 Bus Arbiter.

Table 1. 8289 Bus Arbiter Jumper Configurations

CONFIGURATION NUMBER	JUMPER CONN	CBRQ/	ANYRQST	DESCRIPTION
1	E144-E145 E130-E131	Low	Low	The Bus Arbiter that has control of the Multibus interface will retain control unless a higher priority master activates CBRQ/ or if the next machine cycle does not require the use of the Multibus interface it will be relinquished to a lower priority device.
		High	Low	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
2	E144-E145 E129-E130	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender control to the Bus Arbiter that is pulling CBRQ/ low, regardless of its priority, upon completion of the current bus cycle.
		High	High	The Bus Arbiter that has control of the Multibus interface, retains control until another Bus Arbiter pulls CBRQ/ low. When CBRQ/ goes low, the conditions are as described above.
3	E143-E144* E129-E130*	Low	High	The Bus Arbiter that has control of the Multibus interface will surrender the use of the Multibus interface after each transfer cycle.

*Factory default wiring.

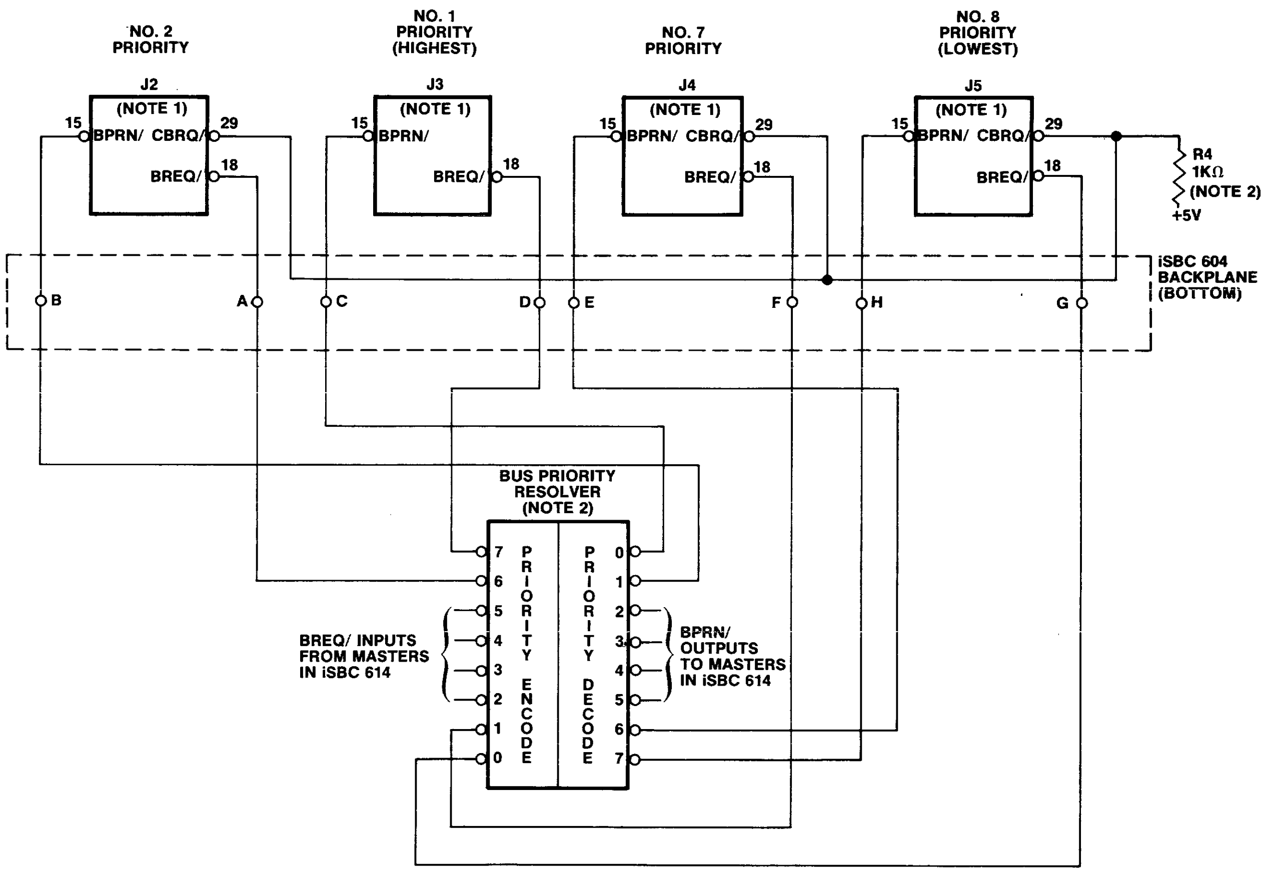


*Pull-up resistor is supplied by the customer.

NOTE: All non CBRQ/ devices must have higher priority. If a non CBRQ/ device is placed at a lower priority, it will not be able to gain control of the Multibus interface.

PSI11

Figure 1. Serial Priority Resolution Scheme

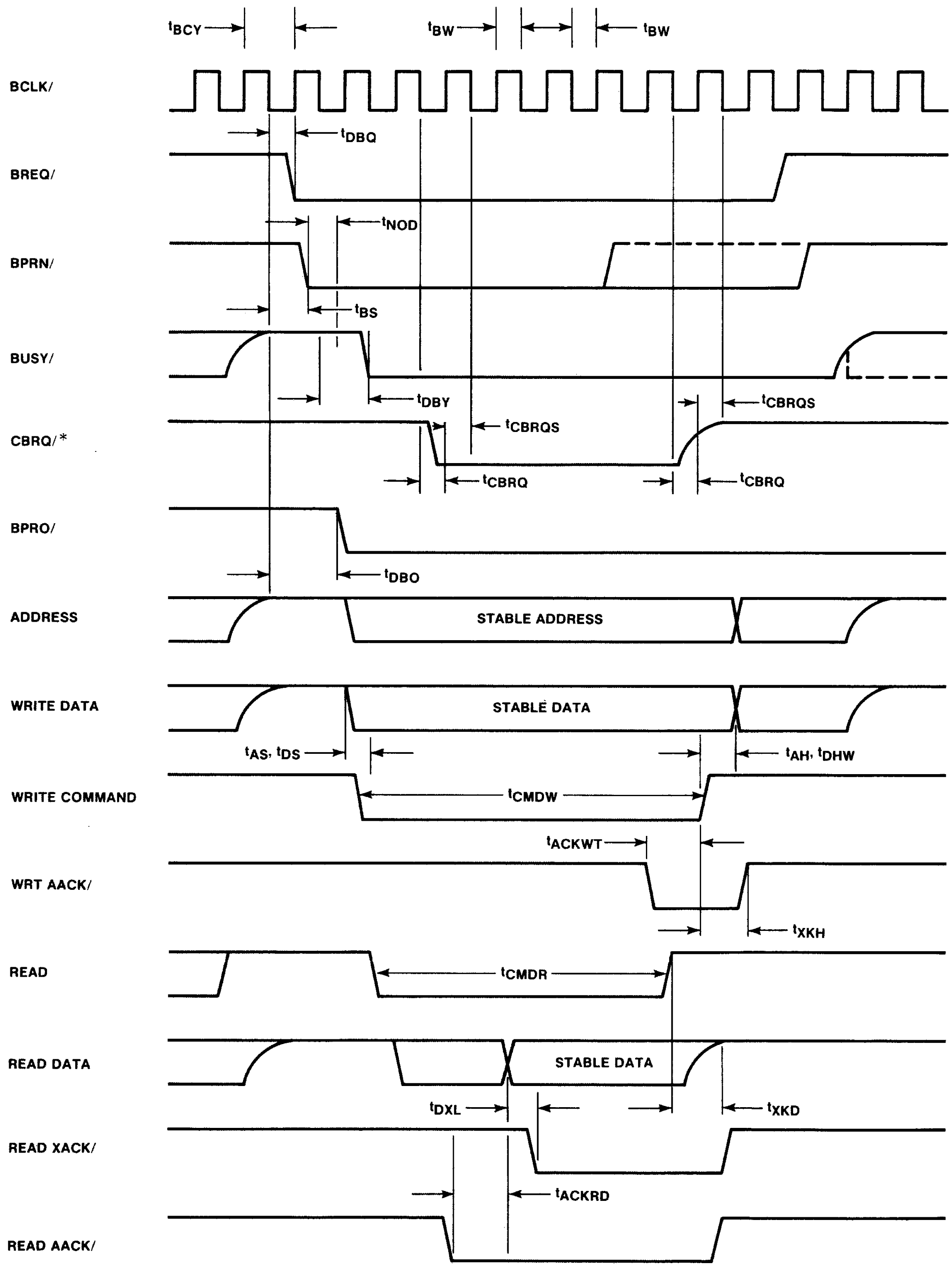


NOTES:

1. Refer to paragraph 2-20 in the iSBC 86/12 Single Board Computer Hardware Reference Manual regarding the disabling of BPRO/.
2. Supplied by the customer.

PSI13

Figure 2. Parallel Priority Resolution Scheme



* CBRQ/ timing not shown relative to other bus signals other than BCLK/.

PSI12

Figure 3. Bus Exchange Timing

Table 2. iSBC 86/12 DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	•Max.	Units
AACK/, XACK/	V_{OL}	Output Low Voltage	I_{OL}= 16 mA		.04	V
	V_{OH}	Output High Voltage	I_{OH} = –3 mA	2.0		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		–2.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		–1.4	mA
	*C_L	Capacitive Load			15	pF
ADR0/-ADRF/ ADR10/-ADR13/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.55	V
	V_{OH}	Output High Voltage	I_{OH} = 3 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.50	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA
	I_{LH}	Output Leakage High	V_O = 5.25V		-0.50	mA
	I_{LL}	Output Leakage Low	V_O = 0.45V		-0.50	mA
	*C_L	Capacitive Load			18	pF
BCLK/	V_{OL}	Output Low Voltage	I_{OL} = 59.5 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = –3 mA	2.7		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		–0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		40	μA
	*C_L	Capacitive Load			15	pF
BHEN/	V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		1.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	μA
	*C_L	Capacitive Load			15	pF
BPRN/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		–0.5	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25V		50	μA
	*C_L	Capacitive Load			18	pF
BPRO/	V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = –0.4 mA	2.4		V
	*C_L	Capacitive Load			15	pF
BREQ/	V_{OL}	Output Low Voltage	I_{OL} = 50 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = 0.4 mA	2.4		V
	*C_L	Capacitive Load			10	pF
BUSY/, CBRQ/, INTROUT/ (OPEN COLLECTOR)	V_{OL}	Output Low Voltage	I_{OL} = 20 mA		0.4	V
	*C_L	Capacitive Load			20	pF

*Capacitive load values are approximations.

Table 2. iSBC 86/12 DC Characteristics (Continued)

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
CCLK/	V_{OL}	Output Low Voltage	I_{OL} = 60 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = –3 mA	2.7		V
	*C_L	Capacitive Load			15	pF
DAT0/-DATF/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = –5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.80	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-0.20	mA
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	*C_L	Capacitive Load			18	pF
INH1/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low	V_{IN} = 0.5V		-2.0	mA
	I_{IH}	Input Current at High	V_{IN} = 2.7V		50	μA
	*C_L	Capacitive Load			18	pF
INIT/ (SYSTEM RESET)	V_{OL}	Output Low Voltage	I_{OL} = 44 mA		0.4	V
	V_{OH}	Output High Voltage	OPEN COLLECTOR			
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-4.2	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		-1.4	mA
	*C_L	Capacitive Load			15	pF
INT0/-INT7/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.4V		-1.6	mA
	I_{IH}	Input Current at High V	V_{IN} = 2.4V		40	μA
	*C_L	Capacitive Load			18	pF
IORC/, IOWC/	V_{OL}	Output Low Voltage	I_{OL} = 32 mA		0.45	V
	V_{OH}	Output High Voltage	I_{OH} = –5 mA	2.4		V
	I_{LH}	Output Leakage High	V_O = 5.25V		100	μA
	I_{LL}	Output Leakage Low	V_O = 0.45V		-100	μA
	*C_L	Capacitive Load			15	pF
INTA/, MRDC/, MWTC/	V_{OL}	Output Low Voltage	I_{OL} = 30 mA		0.45	V
	V_{OL}	Output High Voltage	I_{OH} = –5 mA	2.4		V
	V_{IL}	Input Low Voltage			0.95	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at Low V	V_{IN} = 0.45V		-2.0	mA
	I_{IH}	Input Current at High V	V_{IN} = 5.25		1000	μA
	*C_L	Capacitive Load			25	pF

***Capacitive load values are approximations.**

Table 3. iSBC 86/12 AC Characteristics (Master Mode)

Parameter	Minimum (ns)	Maximum (ns)	Description	Remarks
t_{AS}	50		Address setup time to command	
t_{AH}	50		Address hold time from command	
t_{DS}	50		Data setup to write CMD	
t_{DHW}	50		Data hold time from write CMD	
t_{CY}	198	202	CPU cycle time	
t_{CMDR}	430		Read command width	No wait states
t_{CMDW}	430		Write command width	With 1 wait state
t_{CSWR}	380		Read-to-write command separation	In override mode
t_{CSRR}	380		Read-to-read command separation	In override mode
t_{CSWW}	580		Write-to-write command separation	In override mode
t_{CSRW}	580		Write-to-read command separation	In override mode
t_{XACK1}	-208		Command to XACK first sample point	In override mode
t_{SAM}	202	210	Time between XACK samples	In override mode
t_{ACKRD}	115		AACK to valid read data	When AACK is used
t_{ACKWT}	205		AACK to write command inactive	When AACK is used
t_{DHR}	0		Read data hold time	
t_{DXL}	-115		Read data setup to XACK	
t_{XKH}	0		XACK hold time	
t_{XKD}	0		AACK or XACK turn off delay	
t_{BWS}	35	∞	Bus clock low or high intervals	Supplied by system
t_{BS}	23		BPRN to BCLK setup time	
t_{DBY}		55	BCLK to BUSY delay	
t_{CBRQ}	0	60	BCLK to CBRQ	
t_{CBRQS}	35		CBRQ to BCLK setup time	
t_{NOD}		30	BPRN to BPRO delay	
t_{DBQ}	35		BCLK/ to bus request	
t_{DBO}	40		BCLK/ to bus priority out	
t_{BCY}	108	109	Bus clock period (BCLK)	From iSBC 86/12 board when terminated
t_{BW}	35	74	Bus clock low or high interval	From iSBC 86/12 board when terminated
t_{INIT}	3000		Initialization width	After all voltages have stabilized