

COMMON UNIVERSAL LOGIC INTERFACE TEST

Consists of:

Program Description	B06-129M95R08A15
Program Listing	06-129M96R07A13
Bootstrap Loader Tape	06-129M17R07
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R09 PATCH INFORMATION
FOR TEST PROGRAM 06-129

To set up the Power Fail Save Area Pointer and the Data Formal Fault (Boundary Error) new PSW. Patches are mandatory on Series 3200 and are as follows:

<u>Location</u>	<u>Old</u>	<u>New</u>	
0A0C	B9AB	B1A3	
0A12	00F0	00EE	
0E54	962E	DA2E	WD R2,0 (R14)
0E56	9D25	0000	
0E58	2081	26E1	AIS R14,1
0E5A	4309	4300	B PATCH
0E5C	0004	11A0	
11A0	XXXX	05FE	PATCH CLHR R15,R14
11A2		4380	BNL X'E50'
11A4		0E50	
11A6		9D25	SSR R2,R5
11A8		2081	BTBS 8,1
11AA		4309	B 4 (R9)
11AC		0004	

Note: This patch to be incorporated in object labeled 06-129 R07.1 on Multimedia Packages.

1. COMMON UNIVERSAL LOGIC INTERFACE TEST PROGRAM DESCRIPTION

1.1 Related Documents:

Test Program Listing	06-129M96R07A13
Test Program Tape:	06-129M17R07
Universal Logic Interface	29-311
Instruction Manual	
Universal Interface Module	29-273
Instruction Manual (obsolete, but supported)	

1.2 Test programs to be run prior to loading this test:

1.2.1 For 16-Bit Processors

Memory Test	06-003
Series 16 Processor Test	06-106
5/16 Processor Test Part 1	06-215
5/16 Processor Test Part 2	06-216
8/16 Processor Test Part 1	06-209
8/16 Processor Test Part 2	06-210
8/16E Processor Test Part 1	06-211
8/16E Processor Test Part 2	06-212

1.2.2 For 32-Bit Processors

Series 32 Basic Test	06-158
Series 32 Processor Test	
Part 1	06-154
Part 2	06-155
Part 3	06-178
Series 32 Memory Test	06-156

1.2.3 Other Test Programs

Teletype Basic Confidence Test	06-004
CRT Test	06-146
Carousel 300 Test	06-183
Current Loop Interface Test	06-184

2. PURPOSE OF TEST

2.1 General Test Information

The Universal Logic Interface Test Program is used to check the proper operation of the Universal Logic Interface (ULI) or the Universal Interface Module (UIM). Halfword and byte data transfers are exercised. Output commands, status requests, and the interrupt mechanism are also exercised.

2.2 Test Description

The program checks the halfword and byte modes by writing a shifting data pattern that is alternately a one in a field of zeros and a zero in a field of ones. The data written is read back from the module and compared to the original pattern. The same pattern is used to test the returned status and command latches. After the data transfers are complete, the interrupt mechanism is tested. Output commands are used to disarm, arm and enable the ULI and to generate an interrupt. The device number on acknowledge is also checked.

3. MINIMUM HARDWARE REQUIRED

The following is a list of hardware necessary to perform this test:

1. Processor

Model 7/16 or equivalent
Model 7/32 or equivalent

2. Minimum Memory - 8KB

3. Console Input/Output Device (See Appendix 1) Teletype, CRT, or Carousel

4. Paper Tape Reader

Teletype or High Speed Paper Tape Reader

5. Device Under Test

ULI (Product #M48-013) or UIM (Obsolete Product #M48-009)

6. Test Cable (17-200)

4. REQUIREMENTS OF MACHINE UNDER TEST

4.1 Test Configuration

The 17-200 Test Cable must be attached to the ULI (UIM) at connector 3, assuming that the present signals on connector 3 are those wired at the factory. Refer to Appendix 5 and the ULI schematics (02-304D08). These schematics can be found in the Universal Logic Interface Instruction Manual, 29-311.

4.2 Device Address

The ULI should be strapped for device address X'8B'. If the address is different, the DEVADR option must be entered. Refer to Appendix 3.

4.3 Console Device

If the console device is other than a Teletype with device address of X'02', see Appendix 1 for program modification.

5. LOADING PROCEDURES

5.1 Test Tape Format

The format consists of an absolute non-zoned object tape (M17) with front-end boot loader. The test program occupies memory from X'A00' through X'1149'.

5.2 Normal Loading Procedure

1. Manually enter the X'50' sequence shown below:

<u>LOCATION</u>	<u>CONTENTS</u>
X'30'	X'0000'
X'32'	X'0000'
X'34'	X'0000'
X'36'	X'0050'
X'50'	X'D500'
X'52'	X'00CF'
X'54'	X'4300'
X'56'	X'0080'
for TTY	X'78'
for HS PTR	X'78'
for HS PTR/P	X'78'

2. Place the program tape (06-129M17R07) in the paper tape reader.
3. Execute at address X'30'.
4. When the Processor halts, observe the console display registers D1 and D2. If zero, loading is complete; otherwise, repeat the loading procedure.
5. Refer to Appendix 1 and set up the addresses for Console I/O Device.
6. Address memory location X'A00' for a 32-bit processor or X'A04' for a 16-bit processor.
7. Start the program execution. Observe the following title is printed on the console device:

COMMON ULI TEST 06-129R07

6. OPERATING PROCEDURES

6.1 Normal Testing (Universal Logic Interface 02-304)

1. Ascertain that the 17-200 test cable is properly plugged into the ULI connector 3.
2. When the asterisk is printed, enter the desired options via the console device. Refer to Appendix 2 for the option/command input structure and Appendix 3 for option explanation.
3. Enter the RUN command via the console device.
4. If no errors are detected, characters "NO ERRORS" are printed almost immediately after execution. Should an error occur, refer to Section 6.3 for the appropriate action.
5. To re-execute the test, enter the RUN command via the console device.

6.2 Optional Testing (Universal Interface Module 02-243)

The ULI Test Program may be used to test the Universal Interface Module (02-243). The test cable (17-200) must be attached and the test executed as though testing the ULI with the byte to halfword option.

To test I/O slots without interrupts the INTRPT option must be specified. Refer to Appendix 3.

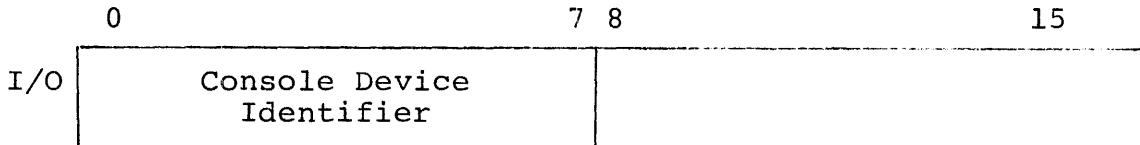
6.3 Error Procedures

If an error is encountered, the Processor loops on the failure, the error number is displayed on D1 of the Processor Display Panel, and the error number is printed on the console device. Refer to Appendix 4 for the meaning of the error number. To re-execute test after an error has occurred, address the desired memory location (step 6 in Section 5.2) and start program execution. Note, however, in case of unsolicited interrupt the program prints the error number each time it occurs and continues normal execution of the test program.

APPENDIX 1

CONSOLE DEVICE DEFINITION

1. The halfword labeled I/O (see the listing) has the default value for Teletype (address X'02') as the console device. If the configuration is different, the test program must be changed as follows:



Console Device Identifier	Explanation
X'01'	GDT/CRT on PASLA/PALM interface, strapped for FDX and the highest baud rate.
X'02'	TTY on TTY interface. GDT/CRT on Current Loop Interface
X'04'	Carousel 300 on PASLA/PALM interface, strapped for FDX and the highest baud rate.
X'05'	Micro I/O Bus Interface.
0,X'03,X'06'-X'FF'	Reserved. The program defaults it to 2.

2. The Teletype or Current Loop interface, if used, should be strapped for the device address of X'02'. If it is different, the halfword labeled TTYADR (see the listing) must be changed accordingly.
3. The Carousel, GDT (Graphical Display Terminal) or CRT; if used on PASLA interface should be strapped for the device address of X'10' and X'11' for receiving and transmitting sides respectively. If it is different, the halfword labeled CRTADR (in case of CRT) or CAROUADR (in case of carousel) must be changed accordingly (see listing).
4. The micro I/O Bus if used should be strapped for device address X'C0'. If the address is different, the halfword MICADR (see the listing) must be changed accordingly.

APPENDIX 2
OPTION/COMMAND INPUT STRUCTURE

An asterisk (*) is output to the console device to indicate that the program is waiting an option input. The options and option values may be printed out by typing in the command 'OPTION' followed by a carriage return.

The option values may be changed by typing in the option from the console device, followed by a space and the desired hexadecimal value. A carriage return (CR) is issued to terminate every option/command input. An invalid option/command causes a (?) followed by a carriage return (CR), line feed (LF), and an asterisk (*) to occur.

<u>OPTION</u>	<u>DEFAULT VALUE</u>	<u>DESCRIPTION</u>
DEVADR	X'8B'	Specifies the device address of the Universal Logic Interface.
MODE	0	Specifies whether the byte to half-word option is installed. 0 = option not installed. 1 = option installed.
INTLEV	0	Specifies the interrupt level that the Universal Logic Interface is physically attached to and consequently the register set to which an external interrupt from the ULI will vector to. INTLEV = F on 7/16 or equivalent INTLEV = 0 on 7/32 INTLEV = 0, 1, 2, or 3 on 8/32
INTOPT	0	Specifies whether ULI interrupts will be tested. 0 = interrupts will be tested 1 = interrupts will not be tested.

APPENDIX 3
FAILURE NUMBER DEFINITION

NUMBER		FAILURE
01	Halfword Mode Data Transfer	R4 = Data Written, R6 = Data Read
02	Byte Mode or Byte to Halfword Mode Data XFER	R4 = Data Written R6 = Data Read
03	Sense Status Bits (0:3)	R4(12:15) = Test Data R6(12:15) = Error Bits
04	Output Command Bits (4:7) or Sense Status Bits (4:7)	R4 = Output Command R6 = Returned Status
05	Unsolicited Interrupt	
06	No Interrupt	
07	Wrong Device Number Returned on Acknowledge	R4 = Received Device Number
08	Acknowledge Doesn't Reset Atn.	

Interrupt level is X, the register set that the interrupt has vectored to.

APPENDIX 4

17-200 TEST CONNECTOR

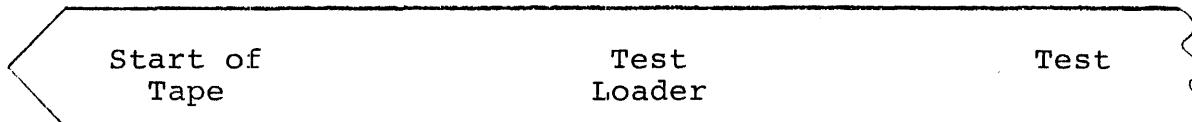
This appendix shows how the 17-200 test connector should be wired. See Page 3 of 02-304A20.

SIN000	to	DOT120
SIN010	to	DOT130
SIN020	to	DOT140
SIN030	to	DOT150
SIN040	to	COT040
SIN050	to	COT050
SIN060	to	COT060
SIN070	to	COT070
DIN000	to	DOT000
DIN010	to	DOT010
DIN020	to	DOT020
DIN030	to	DOT030
DIN040	to	DOT040
DIN050	to	DOT050
DIN060	to	DOT060
DIN070	to	DOT070
DIN080	to	DOT080
DIN090	to	DOT090
DIN100	to	DOT100
DIN110	to	DOT110
DIN120	to	DOT120
DIN130	to	DOT130
DIN140	to	DOT140
DIN150	to	DOT150

APPENDIX 5

TEST LOADER

The test loader must be loaded with the 50 Sequence as described in Section 5.2. The test loader resides in memory from X'80' to X'CE' and loads the test at the correct memory location. While reading the program tape, each data byte location is output to the Display Panel. While loading the test into memory, the loader performs an Exclusive OR of each instruction to verify that the test was loaded correctly, the loader halts the Processor with the last location of the test displayed on the Display Panel, and the loading procedures in Section 5.2 must be repeated. If the test did load correctly, the Display is zeroed and the Processor is put in the Wait state.



PROG= CULIP ASSEMBLED BY CAL 03-066R04-01 (32-BIT)

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1      CROSS
2      WIDTH 120
3      TARGT 16
4      SQCHK
5      * THIS TEST IS DESIGNED TO TEST THE UNIVERSAL LOGIC
6      * INTERFACE M48-013(35-479) AND THE UNIVERSAL INTERFACE MODULE
7      * M48-009(35-399).
8      *
9      * ASSUMPTIONS:
10     * IT IS ASSUMED THAT THE FOLLOWING TESTS HAVE BEEN RUN
11     * WITHOUT DETECTING AN ERROR PRIOR TO LOADING THE COMMON ULI TEST:
12     *
13     * 16 BIT PROCESSORS:
14     *    MEMORY TEST          06-003
15     *    SERIES 16 PROCESSOR TEST 06-106
16     *    5/16 PROCESSOR TEST PART 1 06-215
17     *    5/16 PROCESSOR TEST PART 2 06-216
18     *    8/16 PROCESSOR TEST PART 1 06-209
19     *    8/16 PROCESSOR TEST PART 2 06-210
20     *    8/16E PROCESSOR TEST PART 1 06-211
21     *    8/16E PROCESSOR TEST PART 2 06-212
22     *
23     * 32 BIT PROCESSORS:
24     *    SERIES 32 BASIC TEST   06-158
25     *    SERIES 32 PROCESSOR TEST
26     *      PART 1              06-154
27     *      PART 2              06-155
28     *      PART 3              06-178
29     *
30     *    SERIES 32 MEMORY TEST  06-156
31     *
32     * OTHER APPLICABLE TESTS:
33     *    TELETYPE BASIC CONFIDENCE TEST 06-004
34     *    CRT TEST                06-146
35     *    CAROUSEL 300 TEST        06-183
36     *    CURRENT LOOP INTERFACE TEST 06-184
37     *
38     * DESIGN SPECIFICATIONS:
39     *    THE 06-129R07 TESTS THE ULI FIRST IN HALFWORD DATA TRANSFERS,
40     *    CHECKS STATUS, AND THEN CHECKS BYTE OR BYTE TO HALFWORD TRANSFERS.
41     *    THEN THE TEST CHECKS THAT COMMAND BITS SET THE PROPER STATUS BITS,
42     *    THAT THE INTERFACE GIVES INTERRUPTS ON THE PROPER COMMANDS, AND
43     *    THAT THE INTERRUPTING INTERFACE GIVES THE CORRECT DEVICE ADDRESS
44     *    AND STATUS UPON ACKNOWLEDGEMENT OF THE INTERRUPT ON THE PROPER
45     *    INTERRUPT LEVEL.
46     *
47     *
48     *

```

ULI00010
 ULI00020
 ULI00030
 ULI00040
 ULI00060
 ULI00070
 ULI00080
 ULI00090
 ULI00100
 ULI00110
 ULI00120
 ULI00130
 ULI00140
 ULI00150
 ULI00160
 ULI00170
 ULI00180
 ULI00190
 ULI00200
 ULI00210
 ULI00220
 ULI00230
 ULI00240
 ULI00250
 ULI00260
 ULI00270
 ULI00280
 ULI00290
 ULI00300
 ULI00310
 ULI00320
 ULI00330
 ULI00340
 ULI00350
 ULI00360
 ULI00370
 ULI00380
 ULI00390
 ULI00400
 ULI00410
 ULI00420
 ULI00430
 ULI00440
 ULI00450
 ULI00460
 ULI00470
 ULI00480

50 * LOADING PROCEDURE:
51 * THE 06-129M17 PAPER TAPE IS LOADED USING THE STANDARD
52 * 50 SEQUENCE:
53 *
54 * LOC DATA
55 *
56 * X'0050' X'D500'
57 * X'0052' X'00CF'
58 * X'0054' X'4300'
59 * X'0056' X'0080'
60 *
61 * TTY X'0073' X'0294'
62 * HS PTR X'0078' X'0399'
63 * HS PTR/P X'0078' X'1399'
64 *
65 * USER OPTIONS:
66 * START THE PROGRAM AT X'A00' FOR A 32 BIT PROCESSOR, AND AT
67 * X'A04' FOR A 16 BIT PROCESSOR.
68 *
69 * DEFAULT
70 * OPTION VALUE DESCRIPTION
71 * ***** *****
72 *
73 * DEVADR X'8B' ULI INTERFACE ADDRESS
74 *
75 * INTRPT 0 INTERFACE TESTING UNDER INTERRUPTS
76 * 0 = YES 1 = NO
77 *
78 * NORMAL TESTING:
79 *
80 * DEFAULT
81 * OPTION VALUE DESCRIPTION
82 * ***** *****
83 *
84 * INTLEV 0 INTERRUPT LEVEL OF INTERFACE
85 * 7/16 OR EQUIV = F
86 * 7/32 = 0
87 * 8/32 = 0-3 FOR CORRECT INTERRUPT
88 * LEVEL
89 *
90 * MODE 0 0 = BYTE TRANSFERS
91 * 1 = BYTE TO HALFWORD TRANSFERS
92 *
93 * TO EXECUTE THE TEST, ENTER THE "RUN" COMMAND FOLLOWED BY A
94 * CARRIAGE RETURN. A "NO ERROR" OR THE APPROPRIATE ERROR MESSAGE WILL
95 * BE IMMEDIATELY PRINTED ON THE CONSOLE DEVICE. IF AN ERROR IS
96 * ENCOUNTERED, THE ERROR NUMBER WILL ALSO BE WRITTEN TO THE
97 * DISPLAY PANEL (D1).
98 *
99 * FOR COMPLETE INSTRUCTIONS, SEE 06-129M95R07A15 TEST DESCRIPTION.
100 *

ULI00500
ULI00510
ULI00520
ULI00530
ULI00540
ULI00550
ULI00560
ULI00570
ULI00580
ULI00590
ULI00600
ULI00610
ULI00620
ULI00630
ULI00640
ULI00650
ULI00660
ULI00670
ULI00680
ULI00690
ULI00700
ULI00710
ULI00720
ULI00730
ULI00740
ULI00750
ULI00760
ULI00770
ULI00780
ULI00790
ULI00800
ULI00810
ULI00820
ULI00830
ULI00840
ULI00850
ULI00860
ULI00870
ULI00880
ULI00890
ULI00900
ULI00910
ULI00920
ULI00930
ULI00940
ULI00950
ULI00960
ULI00970
ULI00980
ULI00990
ULI01000

102	*	ERROR PROCEDURES:			ULIO1020
103	*				ULIO1030
104	*	ERROR			ULIO1040
105	*	NUMBER	FAILURE	COMMENTS	ULIO1050
106	*				ULIO1060
107	*	01	HALFWORD MODE DATA TRANSFER	R4=DATA WRITTEN R6=DATA READ	ULIO1070
108	*				ULIO1080
109	*				ULIO1090
110	*	02	BYTE MODE OF BYTE TO HALFWORD MODE DATA XFER	R4=DATA WRITTEN R6=DATA READ	ULIO1100
111	*				ULIO1110
112	*				ULIO1120
113	*	03	SENSE STATUS BITS(0:3)	R4(RIGHT 4 BITS)=TEST DATA R6(RIGHT 4 BITS)=ERROR BITS	ULIO1130
114	*				ULIO1140
115	*				ULIO1150
116	*	04	OUTPUT COMMAND BITS 4:7 OR SENSE STATUS BITS (4:7)	R4=OUTPUT COMMAND R6=RETURNED STATUS	ULIO1160
117	*				ULIO1170
118	*				ULIO1180
119	*				ULIO1190
120	*	05	UNSOLICITED INTERRUPT		ULIO1200
121	*				ULIO1210
122	*	06	NO INTERRUPT		ULIO1220
123	*				ULIO1230
124	*	07	WRONG DEVICE NUMBER RETURNED ON ACKNOWLEDGE	16 BIT PROCESSOR, R4=RECIEVED DEVICE NUMBER 32 BIT PROCESSOR, R2 OF APPROPRIATE REGISTER SET=RECIEVED DEVICE NUMBER	ULIO1240 ULIO1250 ULIO1260 ULIO1270 ULIO1280
125	*				
126	*				
127	*				
128	*				
129	*				
130	*	08	ACKNOWLEDGE DOESN'T RESET ATTENTION		ULIO1290 ULIO1300
131	*				
132	*	INCORRECT INTERRUPT LEVEL = X			ULIO1310 ULIO1320
133	*				ULIO1330

ULI LOADER

0000 0000	135	R0	EQU	0	ULIO1350
0000 0001	136	R1	EQU	1	ULIO1350
0000 0002	137	R2	EQU	2	ULIO1370
0000 0003	138	R3	EQU	3	ULIO1380
0000 0004	139	R4	EQU	4	ULIO1390
0000 0005	140	R5	EQU	5	ULIO1400
0000 0006	141	R6	EQU	6	ULIO1410
0000 0007	142	R7	EQU	7	ULIO1420
0000 0008	143	R8	EQU	8	ULIO1430
0000 0009	144	R9	EQU	9	ULIO1440
0000 000A	145	R10	EQU	10	ULIO1450
0000 000B	146	R11	EQU	11	ULIO1460
0000 000C	147	R12	EQU	12	ULIO1470
0000 000D	148	R13	EQU	13	ULIO1480
0000 000E	149	R14	EQU	14	ULIO1490
0000 000F	150	R15	EQU	15	ULIO1500
	151	*			ULIO1510
	152	*			ULIO1520
0000P	153		ORG	X'30'	ULIO1530
	154	*			ULIO1540
	155	*			ULIO1550
0080 2421	156	LIS	R2,1		ULIO1560
0082 2303	157	BS	BOOT		ULIO1570
0084 0F48	158	DC	Z(PSWSAVE)	CURRENT PSW SAVE POINTER(32-BIT M/C)	ULIO1580
0086 0F50	159	DC	Z(RSAVE)	REGISTER SAVE POINTER(32-BIT M/C)	ULIO1590
0088 C810 0400	160	BOOT	LHI R1,ORIGIN1	R1 = ADR(ORIGIN1 BYTE OF TEST PROG)	ULIO1600
008C C830 0F45	161		LHI R3,LNZB+1	R3= ADR(LAST NON-ZERC BYTE)	ULIO1610
0090 4030 0022	162		STH R3,X'22'	REGISTER SAVE POINTER(16 BIT M/C)	ULIO1620
0094 2731	163	SIS	R3,1		ULIO1630
0096 C960 0000	164	MN	LHI R6,0	R6 = CHKSUM BYTE = X'MN'	ULIO1640
009A D340 0078	165		LB R4,X'78'	INPUT DEV ADR	ULIO1650
009E DE40 0079	166		OC R4,X'79'		ULIO1660
00A2 9D45	167	LEADER	SSR R4,R5		ULIO1670
00A4 2091	168		BTBS 9,1	DU,BSY	ULIO1680
00A6 9H45	169		RDR R4,R5		ULIO1690
00A8 0855	170		LDAR R5,R5		ULIO1700
00AA 2234	171		BZS LEADER	IGNORE LEADER	ULIO1710
00AC D251 0000	172	LOAD	STS R5,0(R1)	STORE 1ST NON ZERO & SUBSEQUENT BYTE	ULIO1720
00B0 D351 0000	173		LB R5,0(R1)	RELOAD DATA BYTE TO	ULIO1730
00B4 0765	174		XAR R6,R5	GENERATE CHECKSUM	ULIO1740
00B6 9481	175		EXBR R8,R1		ULIO1750
00B8 9828	176		WHR R2,R8	DISPLAY MEMORY ADDRESS	ULIO1760
00BA 9D45	177		SSR R4,R5		ULIO1770
00BC 2091	178		BTBS 9,1	DU,BUSY	ULIO1780
00BE 9845	179		RDR R4,R5		ULIO1790
00C0 C110 00AC	180		BXLE R1,LOAD	LOAD TILL LAST BYTE	ULIO1800
00C4 9486	181		EXBR R8,R6		ULIO1810
00C6 9828	182		WHR R2,R8	FINAL CHECKSUM	ULIO1820
00C8 2478	183	LDWT	LIS R7,8		ULIO1830
00CA 917C	184		SLLS R7,12	R7 = X'8000'	ULIO1840
00CC 9557	185		EPSR R5,R7	HALT PROCESSOR	ULIO1850
00CE 2203	186		BS LDWT		ULIO1860
	187	*			ULIO1870

		189	*		ULI01890
		190	*		ULI01900
00D0		191	ORG X'A00'		ULI01910
		192	*		ULI01920
		193	*		ULI01930
0A00	4300 0A1C	194	CRIGIN1 B START32	** START FOR 32 BIT PROCESSORS **	ULI01940
0A04	4300 0A20	195	SECOND B START16	** START FOR 16 BIT PROCESSORS **	ULI01950
		196	*		ULI01960
		197	* *****		ULI01970
		198	*		ULI01980
0A0B	A498 0000 0A09	199	READ1 DC X'A498'	READ/WRITE I/O COMMANDS	ULI01990
		200	WRITE1 EQU *-1		ULI02000
0A0A	A498	201	READ2 DC X'A498'	TTY I/O COMMANDS	ULI02010
0A0C	B9AB	202	READ3 DC X'B9AB'	PASLA I/O COMMANDS	ULI02020
0A0E	9212	203	READ4 DC X'9212'	MICROBUS I/O COMMANDS	ULI02030
		204	*		ULI02040
		205	* *****		ULI02050
		206	*		ULI02060
0A10	02C2	207	IO DC X'0202'	CONSOLE DEVICE POINTER	ULI02070
0A12	00	208	ADDRESS DB X'0'	CONSOLE DEVICE ADDRESS	ULI02080
0A13	FO	209	PADSET DB X'FO'	PASLA SPEED COMMAND	ULI02090
		210	*		ULI02100
		211	* / DEVICE POINTERS /		ULI02110
		212	* CRT ... 1		ULI02120
		213	* TTY ... 2		ULI02130
		214	* CAROUSEL ... 4		ULI02140
		215	* MICROBUS ... 5		ULI02150
		216	*		ULI02160
0A14	1011	217	CRTADR DC X'1011'	PASLA ADDRESS	ULI02170
0A15	02C2	218	TTYADR DC X'0202'	TTY ADDRESS	ULI02180
0A18	COCO	219	MICADDR DC X'COCO'	MICROBUS ADDRESS	ULI02190
0A1A	1011	220	CAROUADDR DC X'1011'	CAROUSEL ADDRESS	ULI02200
		221	*		ULI02210
		222	* *****		ULI02220
		223	*		ULI02230
0A1C	243F	224	START32 LIS R3,X'F'	MODEL FLAG = 'F'	ULI02240
0A1E	23C2	225	BS START		ULI02250
0A20	2430	226	START16 LIS R3,0	MODEL FLAG = '0'	ULI02260
0A22	4030 0F34	227	START STH R3,MODEL	STORE MODEL FLAG	ULI02270
0A25	C830 00F0	228	LHI R3,X'FO'		ULI02280
0A2A	9523	229	EPER R2,R3	GO TO RS F	ULI02290
0A2C	L330 0A10	230	L3 R3,IO		ULI02300
0A30	C530 0001	231	CLHI R3,1	IS I/O ON PASLA ?	ULI02310
0A34	4330 0A62	232	BE CRT	YES, BRANCH	ULI02320
0A38	C530 0004	233	CLHI R3,4		ULI02330
0A3C	4330 0A62	234	BE CRT		ULI02340
0A40	C530 0005	235	CLHI R3,5	IS I/O ON THE MICROBUS	ULI02350
0A44	4330 0A92	236	BE MICBUS	YES, BRANCH	ULI02360
		237	*		ULI02370
		238	*		ULI02380
0A48	4830 0A0A	239	TTY LH R3,READ2	NO	ULI02390
0A4C	4030 0A08	240	STH R3,READ1	STORE TTY COMMANDS	ULI02400
0A50	D330 0A16	241	LB R3,TTYADR		ULI02410
0A54	D230 0A12	242	STB R3,ADDRESS	STORE TTY ADDRESS	ULI02420
0A58	0733	243	XHR R3,R3		ULI02430
0A5A	4030 0F3C	244	STH R3,PASFLG	ZERO PASLA FLAG	ULI02440

0A5E	43C0 0A8	245	B	WRITLE	ULI02450	
		246	*		ULI02460	
		247	*		ULI02470	
0A62	4830 0A0C	248	CRT	LH R3,READ3	ULI02480	
0A66	4030 0A08	249	STH	R3,READ1	ULI02490	
0A6A	243F	250	LIS	R3,X'F'	ULI02500	
0A6C	4030 0F3C	251	STH	R3,PASFLG	ULI02510	
0A70	D330 0A10	252	L8	R3,IO	ULI02520	
0A74	C520 0001	253	CLHI	R3,1	ULI02530	
0A78	2336	254	BES	CRT1	ULI02540	
0A7A	D330 0A1A	255	L8	R3,CAROUADR	ULI02550	
0A7E	D230 0A12	256	STR	R3,ADDRESS	STORE CAPOUSEL ADDRESS	ULI02560
0A82	2305	257	BS	CMD	ULI02570	
0A84	D330 0A14	258	CRT1	LB R3,CRTADR	ULI02580	
0A88	D230 0A12	259	STB	R3,ADDRESS	STORE CRT ADDRESS	ULI02590
0A8C	DF30 0A13	260	CMD	OC R3,PADSET	OC TIMING TO PASLA	ULI02600
0A90	230C	261	BS	WRITLE	ULI02610	
		262	*		ULI02620	
		263	*		ULI02630	
0A92	4830 0A0E	264	MICBUS	LH R3,READ4	ULI02640	
0A96	4030 0A03	265	STH	R3,READ1	STORE MICROBUS COMMANDS	ULI02650
0A9A	C733	266	XHR	R3,R3	ULI02660	
0A9C	4030 0F3C	267	STH	R3,PASFLG	ZERO PASLA FLAG	ULI02670
0AA0	D330 0A18	268	L8	R3,MICADR	ULI02680	
0AA4	D230 0A12	269	STB	R3,ADDRESS	STORE MICROBUS ADDRESS	ULI02690
		270	*		ULI02700	
0AAB	4190 0E38	271	WRITLE	BAL R9,PRINT	"COMMON ULI TEST 06-129R07"	ULI02710
0AAC	01A6	272	DC	Z(TITLE)	ULI02720	
0AAE	0FC1	273	DC	Z(EDITITLE)	ULI02730	
0AB0	43C0 0A8	274	CRG	B TTYIN	ULI02740	
		275	*		ULI02750	
		276	*		ULI02760	
0AB4	0000	277	MODE	DC X'0',C'MODE'	ULI02770	
0AB6	414F4445					
	2020					
0ABC	006B	278	ULIAADR	DC X'8B',C'DEVADR'	ULI02780	
0ABE	44455641					
	4452					
0AC4	0000	279	INTLEV	DC X'0',C'INTLEV'	ULI02790	
0AC6	494E544C					
	4556					
0ACC	0000	280	INTRET	DC X'0',C'INTRPT'	ULI02800	
0ACE	494E5452					
	5054					
0AD4	0000	281	RUN	DC X'0',C'RUN'	ULI02810	
0AD6	52E54F20					
	2020					
0ADC	0000	282	OPTION	DC X'0',C'OPTION',X'0',X'FFFF'	ULI02820	
0ADE	4F505449					
	4F4F					
0AE4	0000					
0AE6	FFFF					
		283	*			
0AE8	4190 0E38	284	TTYIN	BAL R9,PRINT	PRINT **	ULI02830
0AEC	01C2	285	DC	Z(STAR)	ULI02840	
0AEE	01C9	286	DC	Z(STREND)	ULI02850	
					ULI02860	

0AF0	C8E0 2020	287	LHI	R14,X'2020'	LOAD ASCII SPACE	ULI02870
0AF4	40E0 0B80	288	STH	R14,TTYBUF	CLEAR CHR BUFFER	ULI02880
0AF8	40E0 0B82	289	STH	R14,TTYBUF+2		ULI02890
0AFc	40E0 0B84	290	STH	R14,TTYBUF+4		ULI02900
OB00	0711	291	XHP	R1,R1	CLEAR CHR BUFFER INDEX	ULI02910
OB02	4190 0E5E	292	RDCHR	R9,INPUT 4344 BCA	GET A CHARACTER	ULI02920
OB06	C5F0 C00D	293	CLHI	R14,X'0D'	IS IT A "CR" ?	ULI02930
OB0A	233A	294	BES	OKIN	YES, TRY TO MATCH IT TO TABLE	ULI02940
OB0C	C5E0 0020	295	CLHI	R14,X'20'	NO, IS IT A SPACE	ULI02950
OB10	2337	296	BES	OKIN	YES, TRY A MATCH	ULI02960
OB12	D2E1 0B80	297	STB	R14,TTYBUF(R1)	NO, STOR IN CHR BUFFER	ULI02970
OB16	2611	298	AIS	R1,1	INCREMENT INDEX	ULI02980
OB18	C510 0006	299	CLHI	R1,6	HAVE WE REACHED 6 CHARS ?	ULI02990
OB1C	203D	300	BNES	RDCHR	NO, GET ANOTHER	ULI03000
OB1E	0711	301	OKIN	XHP	YES, CLEAR TABLE INDEX	ULI03010
OB20	0733	302	OKIN2	XHP	CLEAR CHR BUFFER INDEX	ULI03020
OB22	0841	303	LHR	R3,R3	SET NEW TABLE INDEX	ULI03030
OB24	48F4 0A36	304	LOOKUP	LH	R15,ORG+6(R4)	ULI03040
OB28	4210 0B86	305	BM	QMARK	IF MINUS PRINT "?"	ULI03050
OB2C	45F3 0B80	306	CLH	R15,TTYBUF(R3)	COMPARE TO CHR BUFFER	ULI03060
OB30	2333	307	BES	INC	IF EQUAL CHECK NEXT HALFWORD IN BUF	ULI03070
OB32	2618	308	AIS	R1,8	IF NOT EQUAL INCREMENT TABLE INDEX	ULI03080
OB34	22CA	309	BS	OKIN2	CHECK NEXT TABLE ENTRY	ULI03090
OB35	2642	310	INC	AIS	INCREMENT TABLE INDEX	ULI03100
OB38	2632	311	AIS	R3,2	INCREMENT CHR BUFFER INDEX	ULI03110
OB3A	C520 0006	312	CLHI	R3,6	HAVE WE FOUND 3 EQUAL HALFWORDS ?	ULI03120
OB3E	203E	313	BNES	LOOKUP	NO, CHECK NEXT TABLE ENTRY	ULI03130
OB40	C510 3020	314	MATCH	CLHI	IS THIS THE RUN OPTION ?	ULI03140
OE44	4320 0B22	315	BE	EXECUTE	YES, EXECUTE TEST	ULI03150
OB48	C510 0028	316	CLH	R1,X'28'	IS THIS THE COMMAND 'OPTION'	ULI03160
OB4C	4230 0360	317	BNE	QM	NO, BRANCH	ULI03170
OB50	4190 0E5E	318	BAL	R9,INPUT		ULI03180
OB54	C5F0 000D	319	CLHI	R14,X'0D'	IS IT A 'CR' AFTER CMD 'OPTION'	ULI03190
OB58	4330 CDEE	320	EE	PROPT	YES, BRANCH TO PROPT	ULI03200
OB5C	43C0 CB86	321	B	QMARK	NO, PRINT A "?"	ULI03210
OB60	C5F0 000D	322	QM	CLH	IS IT A "CR"	ULI03220
OB64	4330 0B86	323	BE	QMARK	YES, PRINT A "?"	ULI03230
OB68	4190 0E5E	324	HEXASC	BAL	NO, GET OPTION VALUE	ULI03240
OB6C	0766	325	XHR	R6,R6	CLEAR BUFFER REGISTER	ULI03250
OB6E	C5E0 000D	326	CLH	R14,X'0D'	IS IT A "CR"	ULI03260
OB72	4320 0B86	327	BE	QMARK	PRINT A "?"	ULI03270
OB76	C5E0 0020	328	CLH	R14,X'20'	SKIP LEADING SPACES	ULI03280
OB7A	2239	329	BES	HEXASC		ULI03290
OB7C	C5E0 003A	330	HEXLP	CLH	CHECK IF VALID HEX CHARACTER	ULI03300
OB80	218A	331	BLS	HEX		ULI03310
OB82	C5E0 0041	332	CLH	R14,X'41'		ULI03320
OB86	4280 0B86	333	BL	QMARK		ULI03330
OB8A	C5E0 0047	334	CLH	R14,X'47'		ULI03340
OB8E	4320 0B86	335	BWL	QMARK		ULI03350
OB92	26F9	336	AIS	R14,9		ULI03360
OB94	C4E0 000F	337	HEX	NHI	R14,X'F'	ULI03370
OB98	9164	338	SLHLS	R6,4		ULI03380
OB9A	06EF	339	OHR	R6,R14	OR CHARACTER INTO REGISTER BUFFER	ULI03390
OB9C	4190 0E5E	340	BAL	R9,INPUT	GET NEXT CHARACTER	ULI03400
OB9D	C5E0 000D	341	CLH	R14,X'0D'	IS IT A "CR" ?	ULI03410
OB94	4230 0B7C	342	BNE	HEXLP	NO, CHECK IF VALID HEX CHARACTER	ULI03420

OBAB	4061	0AB4	343	STH	R6,OPG+4(R1)	YES, STORE HEX OPTION VALUE	ULI03430	
OBAC	4300	0AE8	344	B	TTYIN	PRINT AN **	ULI03440	
			345	*			ULI03450	
			346	*			ULI03460	
OBBO	00C0		347	TTYBUF	DC	X'0',X'0',X'0'	CHARACTER BUFFER	ULI03470
OBB2	00C0							
OBBA	00C0							
			348	*			ULI03480	
			349	*			ULI03490	
OBP6	4190	0E38	350	QMARK	BAL	R9,PRINT	CR,LF,"?",CR,LF	ULI03500
OB2A	0ED6		351		DC	Z(QMSG)		ULI03510
OBBC	0FDB		352		DC	Z(EDQMSG)		ULI03520
OBBE	4300	0AE8	353		B	TTYIN	RETURN	ULI03530
			354	*				ULI03540
			355	*				ULI03550
OBC2	48C0	0ABC	356	EXECUTE	LH	R12,ULIADR		ULI03560
OBC6	91C1		357		SLHLS	R12,1		ULI03570
OBC8	CAC0	00D0	358		AHI	R12,X'D0'		ULI03580
OBCB	40C0	0F38	359		STH	R12,IIP	STORE INTERRUPT TABLE ADDRESS	ULI03590
OBDO	2430		360		LIS	R3,0		ULI03600
OB22	4030	0F3A	361		STH	R3,LAST	ZERO LAST	ULI03610
			362	*				ULI03620
			363	*				ULI03630
OB26	4830	0ABC	364	RESTRRT	LH	R3,ULIADR		ULI03640
ORDA	07C0		365		XHR	R0,80	ZERO REGISTER 0	ULI03650
OBDC	4840	0F34	366		LH	R4,MCDEL	IS PROCESSOR 32 BIT	ULI03660
OB20	4230	02E4	367		ENZ	REP32	YES,BRANCH	ULI03670
OB24	4000	0044	368		STH	R0,X'44'	NO,SET UP INT PSW	ULI03680
OBE8	C840	0074	369		LHI	R4,ERRI		ULI03690
OBEC	4040	0046	370		STH	R4,X'46'		ULI03700
OBFO	43C0	0C15	371		B	REP15		ULI03710
OBF4	C8C0	00D0	372		REP32	LHI	LOAD DEVICE ADDRESS	ULI03720
OBF8	2412		373		LIS	R13,2		ULI03730
OBFA	C8E0	02CE	374		LHI	R14,X'2CE'		ULI03740
OBFE	C8F0	0074	375		LHI	R15,ERRI		ULI03750
OC02	40FC	0000	376	SIT32	STH	R15,0(R12)		ULI03760
OC06	C1C0	0C02	377		BXLE	R12,SIT32		ULI03770
OC0A	48C0	0F38	378		LH	R12,IIP		ULI03780
CC0E	C840	0074	379		LHI	R4,ERRI	LOAD LOC OF ERROR ROUTINE	ULI03790
OC12	404C	0000	380		STH	R4,0(R12)	STORE AT INTERRUPT LOC	ULI03800
OC16	C8C0	70F0	381	REP16	LHI	R12,X'70F0'		ULI03810
OC1A	959C		382		EPSR	R9,R12	ENABLE INTERRUPTS	ULI03820
			383	*				ULI03830
OC1C	2451		384		LIS	R5,1	DATA	ULI03840
OC1E	0845		385	LOOP1	LHR	R4,R5	ONE THRU ZEROS	ULI03850
OC20	41F0	0CFC	386		BAL	R15,TESTDS	TEST DATA AND STATUS	ULI03860
OC24	C740	FFFF	387		XHI	R4,X'FFFF'	ZERO THRU ONES	ULI03870
OC28	41E0	0CFC	388		BAL	R15,TESTDS	TEST DATA AND STATUS	ULI03880
OC2C	0A5E		389		AHR	R5,R5	SHIFT DATA PATTERN	ULI03890
OC2E	228A		390		BNCS	LOOP1	LOCP	ULI03900
			391	*				ULI03910
			392	*				ULI03920
OC30	2474		393		LIS	R7,4	ERROR NUMBER 04	ULI03930
OC32	C744		394		XHR	R4,R4	CHECK THAT COMMAND	ULI03940
OC34	9E34		395	LOOP2	OCR	R3,R4	BITS 04:07 RETURN	ULI03950
OC36	9E36		396		SSR	R3,R6	ON STATUS BITS 04:07	ULI03960

OC38	C460 000F	397	NHI	R6,X'F'		ULI03970	
OC3C	0546	398	CLHR	R4,R6		ULI03980	
OC3E	2334	399	BES	INCRE	OK	ULI03990	
OC40	41D0 0D9A	400	BAL	R13,ERROR	ERROR 04	ULI04000	
OC44	22C8	401	BS	LOOP2	LOOP ON FAILURE	ULI04010	
OC45	2641	402	INCRE	AIS	INCREMENT PATTERN	ULI04020	
OC48	C340 0010	403	THI	R4,X'10'		ULI04030	
OC4C	223C	404	BZS	LOOP2		ULI04040	
		405	*			ULI04050	
		406	*	TEST INTERRUPTS		ULI04060	
		407	*			ULI04070	
OC4E	4870 0ACC	408	LH	R7,INTRPT	INTERRUPTS ?	ULI0408C	
OC52	4230 0DE2	409	BNZ	AOK	NO, BRANCH	ULI04090	
OC56	0777	410	XHR	R7,R7	YES, ERROR NUMBER	ULI04100	
OC58	DE30 0F41	411	CC	R3,ATN	SHOULDN'T INTERRUPT	ULI04110	
OC5C	DE30 0F42	412	OC	R3,DRMATN	SHOULDN'T INTERRUPT	ULI04120	
OC60	DE30 0F3F	413	OC	R3,DBLATN	SHOULDN'T INTERRUPT	ULI04130	
OC64	9E37	414	DROP	OCR	R3,R7	ULI04140	
OC65	DE30 0F40	415	CC	R3,EBL	SHOULDN'T INTERRUPT	ULI04150	
OC5A	48C0 0F34	416	LH	R12,MODEL	IS PROCERROR 32 BIT ?	ULI04160	
OC68	2338	417	BZS	DR15	NO, BRANCH	ULI04170	
OC70	C840 0C38	418	LHI	R4,INTSVR	YES, CONTINUE	ULI04180	
OC74	48C0 0F38	419	LH	R12,IIR		ULI04190	
OC78	4C4C 0000	420	STH	R4,0(R12)	ESTABLISH INTERRUPT TABLE POINTER	ULI04200	
OC7C	2305	421	BS	DR32		ULI04210	
OC7E	C840 0C9A	422	DR16	LHI	R4,INTSVC	ULI04220	
OC82	4040 0046	423	STH	R4,X'46'	SET UP INT PSW	ULI04230	
OC86	DF30 0F3E	424	DR32	OC	R3,EBLATN	ULI04240	
OC8A	247F	425	LIS	R7,X'F'	SHOULD INTERRUPT	ULI04250	
OC8C	2771	426	WAIT1	SIS	R7,1	ULI04260	
OC8E	2031	427	BNZS	WAIT1		ULI04270	
OC90	2476	428	LIS	R7,6	ERROR NUMBER 06	ULI04280	
OC92	41D0 0D9A	429	SAL	R13,ERROR		ULI04290	
OC96	4300 0C64	430	B	DROP	LOOP	ULI04300	
		431	*			ULI04310	
		432	*			ULI04320	
OC9A	9F45	433	INTSVC	ACKR	R4,R5	ACKNOWLEDGE	ULI04330
OC9C	0543	434	CLHR	R4,R3		ULI04340	
OC9E	2335	435	BES	INT8	DEV NO. OK ?	ULI04350	
OCA0	2477	436	LIS	R7,7	ERROR 07	ULI04360	
OCA2	41D0 0D9A	437	BAL	R13,ERROR		ULI04370	
OCA6	2206	438	BS	INTSVC	AGAIN	ULI04380	
OCA8	9F45	439	INT8	ACKR	R4,R5	SHOJLD GET FALSE SYNC	ULI04390
OCAA	0543	440	CLHR	R4,R3		ULI04400	
OCAC	4230 0DE2	441	BNE	AOK		ULI04410	
OCB0	2478	442	LIS	R7,8	ERROR 08	ULI04420	
OCB2	41D0 0D9A	443	BAL	R13,ERROR	ATN DIDN'T DROP	ULI04430	
OCB6	2207	444	BS	INT8	AGAIN	ULI04440	
		445	*			ULI04450	
		446	*			ULI04460	
OCB8	9599	447	INTSVR	EPSR	R9,R9	SAVE PSW (RS)	ULI04470
OCBA	C490 00F0	448	NHI	R9,X'F0'		ULI04480	
OCBE	9094	449	SRHLS	R9,4		ULI04490	
OCC0	4590 0AC4	450	CLH	R9,INTLEV	IS INTERRUPT LEVEL CORRECT (RS) ?	ULI04500	
OCC4	4230 0DBC	451	BNE	INTERL	NO, BRANCH TO ERROR	ULI04510	
OCC8	4520 0ABC	452	INT9	CLH	R2,ULIADR	YES, IS INTER DEV = ULI ?	ULI04520

0CCC	2336	453	BES	CONTINT	YES, BRANCH	ULI04530	
0CCE	2411	454	LIS	R1,1	NO	ULI04540	
0CD0	2477	455	LIS	R7,7	ERROR 7	ULI04550	
CCD2	41D0 0D9A	456	BAL	R13,ERROR		ULI04560	
0CD6	2207	457	BS	INT9	AGAIN	ULI04570	
CCD8	C8C0 0CF4	458	CONTINT	LHI	R12,ERRINT	ULI04580	
0CDC	4890 0F38	459	LH	R9,IIR		ULI04590	
0CE0	40C9 0000	460	STH	R12,0(R9)		ULI04600	
0CE4	C890 70F0	461	INTSVQ	LHI	R9,X'70F0'	ULI04610	
0CEF	95C9	462	EPSR	R12,R9	ENABLE INTERRUPTS	ULI04620	
0CEA	24CF	463	LIS	R12,X'F'		ULI04630	
0CEC	27C1	464	WAIT2	SIS	R12,1	ULI04640	
0CEE	2031	465	BNZS	WAIT2	WAIT	ULI04650	
0CF0	4300 0DE2	466	E	AOK	AOK	ULI04660	
		467	*			ULI04670	
		468	*			ULI04680	
0CF4	2478	469	ERRINT	LIS	R7,8	ULI04690	
0CF5	41D0 0D9A	470	BAL	R13,ERROR	ERROR 8	ULI04700	
0CFA	2208	471	BS	INTSVQ	LOOP	ULI04710	
		472	*			ULI04720	
		473	* DATA TEST (HALFWORD)			ULI04730	
		474	*			ULI04740	
0CF6	DE30 0F43	475	TESTDS	OC	R3,RW	SELECT HALFWORD MODE	ULI04750
0D00	9834	476	WHR	R3,R4		HALFWORD DATA TRANSFER	ULI04760
0D02	9936	477	RH2	R3,R6			ULI04770
0D04	94C4	478	EXBR	R0,R4		JUSTIFY REGISTER 4	ULI04780
0D06	2440	479	LIS	R4,0			ULI04790
0D08	9440	480	EXBR	R4,R0			ULI04800
0D0A	9406	481	EXBR	R0,R6		JUSTIFY REGISTER 6	ULI04810
0D0C	2460	482	LIS	R6,0			ULI04820
0D0E	9460	483	EXBR	R6,R0			ULI04830
0D10	0546	484	CLRR	R4,R6		CHECK DATA	ULI04840
0D12	2335	485	BES	TSTDS1			ULI04850
0D14	2471	486	LIS	R7,1		ERROR 01	ULI04860
0D16	41D0 0D9A	487	BAL	R13,ERROR			ULI04870
0D1A	22CF	488	BS	TESTDS	LOOP ON ERROR		ULI04880
		489	*				ULI04890
		490	* STATUS TEST				ULI04900
		491	*				ULI04910
0D1C	9D36	492	TSTDS1	SSR	R3,R6		ULI04920
0D1E	9064	493	SRHLS	R6,4		TEST THAT D08:11	ULI04930
0D20	0764	494	XHR	R6,R4		RETURNS ON STATUS	ULI04940
0D22	C460 000F	495	NHI	R6,X'F'		BITS 04:07	ULI04950
0D26	2335	496	BES	TSTDS2			ULI04960
0D28	2473	497	LIS	R7,3		ERROR 03	ULI04970
0D2A	41D0 0D9A	498	BAL	R13,ERROR			ULI04980
0D2E	2209	499	BS	TSTDS1	LOOP		ULI04990
		500	*				ULI05000
		501	* DATA TEST (BYTE)				ULI05010
		502	*				ULI05020
0D30	DE30 0F44	503	TSTDS2	OC	R3,BYTE	SELECT BYTE MODE	ULI05030
0D34	9374	504	LBR	R7,R4			ULI05040
0D36	9444	505	EXPB	R4,R4			ULI05050
0D38	0766	506	XHY	R6,R6		CLEAR REG. 5	ULI05060
0D3A	4860 0AE4	507	LH	R6,MODE		FIND OUT OPTION	ULI05070
0D3E	4220 0P6A	508	BTC	2,BTH			ULI05080

0D42	9A34	509	WDR	R3,R4	WRITE FIRST BYTE	ULI05090	
0D44	9B36	510	RDP	R3,R6	READ FIRST BYTE	ULI05100	
0D46	9A37	511	WDP	R3,R7	WRITE SECOND BYTE	ULI05110	
0D48	9B37	512	PDR	R3,R7	READ SECOND BYTE	ULI05120	
0D4A	9466	513	EXBR	R6,P6		ULI05130	
0D4C	0667	514	CHR	R6,R7		ULI05140	
0D4E	9444	515	RTN	EXBR	R4,R4	ULI05150	
0D50	9404	516	EXBR	R0,R4	JUSTIFY REGISTER 4	ULI05160	
0D52	2440	517	LIS	R4,0		ULI05170	
0D54	9440	518	EXBR	R4,R0		ULI05180	
0D56	94C6	519	EXBR	R0,R6	JUSTIFY REGISTER 6	ULI05190	
0D58	2460	520	LIS	R6,0		ULI05200	
0D5A	9460	521	EXBR	R6,R0		ULI05210	
0D5C	0546	522	CLHR	R4,R6	IS DATA OK ?	ULI05220	
0D5E	033F	523	BER	R15	YES, RETURN	ULI05230	
0D60	2472	524	LIS	R7,2	NO, ERROR 02	ULI05240	
0D62	41D0 0D9A	525	BAL	R13,ERROR		ULI05250	
0D66	4300 0D30	526	B	TSTDS2	LOOP	ULI05260	
		527	*			ULI05270	
		528	*	DATA TEST (BYTE TO HALFWORD)		ULI05280	
		529	*			ULI05290	
0D6A	9A34	530	BTH	WDR	R3,R4	WRITE HIGH BYTE	ULI05300
0D6C	9A37	531	WDR	R3,R7	WRITE LOW BYTE	ULI05310	
0D6E	9936	532	RHR	R3,R6	READ BOTH BYTES	ULI05320	
0D70	4300 0D4E	533	B	RTN		ULI05330	
		534	*			ULI05340	
		535	*			ULI05350	
0D74	2475	536	ERR1	LIS	R7,5	ERROR 05	ULI05360
0D76	41D0 0D9A	537	BAL	R13,ERROR		ULI05370	
0D7A	07EE	538	XHR	R14,R14		ULI05380	
0D7C	40E0 0F3A	539	STH	R14, LAST		ULI05390	
0D80	48C0 0F34	540	LH	R12, MODEL		ULI05400	
0D84	2133	541	BNZS	ERR1		ULI05410	
0D86	C2C0 0040	542	IPS4	X'40'	RESTORE PSW & RETURN	ULI05420	
0D8A	24C0	543	ERR1	LIS	R12,0		ULI05430
0D8C	959C	544	EPSR	R9,R12		ULI05440	
0D8E	4010 0F36	545	STH	R1,LOCPSW		ULI05450	
0D92	9510	546	EPSR	R1, R0	RESTORE PSW	ULI05460	
0D94	48C0 0F36	547	LH	R12,LOCPSW		ULI05470	
0D98	03CC	548	BR	R12	RETURN	ULI05480	
		549	*			ULI05490	
		550	*			ULI05500	
0D9A	2481	551	ERROR	LIS	R8,1		ULI05510
0D9C	9A87	552	WDR	R8,R7	ERROR NUMBER	ULI05520	
0D9E	C670 0030	553	OHI	R7,X'30'	R7 = ERR.NO. IN ASCII	ULI05530	
0DA2	D270 0F03	554	STB	R7,ERRNO+1		ULI05540	
0DA6	4870 0F3A	555	LH	R7, LAST		ULI05550	
0DAA	023D	556	BNZR	R13		ULI05560	
0DAC	4190 0E38	557	BAL	R9,PRINT	"ERROR XX"	ULI05570	
0DB0	0EFA	558	DC	Z(ERRMSG)		ULI05580	
0DB2	0F03	559	DC	Z(ERRMSZ)		ULI05590	
0DB4	24EF	560	LIS	R14,X'F'		ULI05600	
0DB6	40E0 0F3A	561	STH	R14, LAST		ULI05610	
0DB8	03CD	562	BR	R13		ULI05620	
		563	*			ULI05630	
		564	*			ULI05640	

0DBC	08A9	565	INTERL	LHR	R10,R9		ULI05650
0DBE	4190 0E38	566		BAL	R9,PRINT	"INCORRECT INTERRUPT LEVEL ="	ULI05660
0DC2	0E0C	567		DC	Z(MSGINT)		ULI05670
0DC4	0FF9	568		DC	Z(EDMSGINT)		JLI05680
CDC6	C6A0 0030	569		OHI	R10,X'30'	CONVERT INTERRUPT LEVEL TO ASCII	ULI05690
CDCA	C5A0 003A	570		CLHI	R10,X'3A'		ULI05700
0DCE	2182	571		BLS	HDIT		ULI05710
0DD0	26A7	572		AIS	R10,7		ULI05720
0DD2	9A2A	573	HDIT	WDR	R2,R10	WRITE INTERRUPT LEVEL	ULI05730
0DD4	9C20	574		SSA	R2,80		ULI05740
0DD5	2081	575		BTBS	8,1	WAIT FCR NOT BUSY	ULI05750
0DD8	C8F0 70F0	576		LHI	R14,X'70F0'	GO TO RS F	ULI05760
0DDC	95F8	577		EPSR	R15,214		ULI05770
0DDE	4300 0AE8	578		E	TTYIN		ULI05780
		579	*				ULI05790
		580	*				ULI05800
0DE2	4190 0E38	581	AOK	BAL	R9,PRINT	"NO ERROR"	ULI05810
0DE5	C6CA	582		DC	Z(MSG)		ULI05820
0DE8	CED5	583		DC	Z(EDMSG)		ULI05830
0DEA	4300 0AE8	584		B	TTYIN	RETURN	ULI05840
		585	*				ULI05850
		586	*				ULI05860
0DEE	243A	587	PROPT	LIS	R3,10	ROUTINE TO DISPLAY OPTIONS AND	ULI05870
0DF0	0799	588		XHR	R9,R9	OPTION VALUES.	ULI05880
0DF2	48F9 0A34	589	PROPT1	LH	R15,MODE(R9)	LOAD IN THE OPTION VALUE	ULI05890
0DF6	0700	590		XHR	R0,R0		ULI05900
0DF8	08EF	591		LHR	R14,R15	LOAD THE OPTION VALUE IN REG.14	ULI05910
0DFA	90E4	592		SRHLS	R14,4	SHIFT TO GET THE MOST SIG. DIGIT	ULI05920
0DFC	2302	593		RS	PROPT3		ULI05930
0DFE	0AEE	594	PROPT2	LHR	R14,R15	GET THE LEAST SIG. DIGIT	ULI05940
0E00	C450 000F	595	PROPT3	NHI	R14,X'F'		ULI05950
0E04	C6E0 0030	596		OHI	R14,X'30'	CONVERT TO ASCII	ULI05960
0E08	C5E0 003A	597		CLHI	R14,X'3A'		ULI05970
0E0C	2182	598		PLS	PROPT4		ULI05980
0E0E	26E7	599		AIS	R14,7		ULI05990
0E10	D2E3 0F04	600	PROPT4	STB	R14,OPTMSG(R3)	STORE THE VALUE IN MSG LOC.	ULI06000
0E14	2631	601		AIS	R3,1		ULI06010
0E16	26C1	602		AIS	R0,1		ULI06020
0E18	C500 0001	603		CLHI	R0,1		ULI06030
0E1C	4330 0DFF	604		BE	PROPT2		ULI06040
0E20	263A	605		AIS	R3,10		ULI06050
0E22	2698	606		AIS	R9,8		ULI06060
0E24	C590 0020	607		CLHI	R9,32		ULI06070
0E28	4230 0DF2	608		BNE	PROPT1		ULI06080
0E2C	4190 0E38	609		BAL	R9,PRINT	PRINT THE OPTIONS AND OPT. VALUES	ULI06090
0E30	0FC4	610		DC	Z(OPTMSG)		ULI05100
0E32	0F33	611		DC	Z(ENOPTMSG)		ULI06110
0E34	4300 0AE8	612		B	TTYIN		ULI06120
		613	*				ULI06130
		614	*				ULI06140
0E38	D320 0A12	615	PRINT	LB	R2,ADDRESS	LOAD I/O ADDRESS	ULI06150
0E3C	48F9 0000	616		LH	R14,0(B9)	LOAD START ADDR OF MSG	ULI06160
0E40	48F9 0002	617		LH	R15,2(B9)	LOAD END ADDR OF MSG	ULI06170
0E44	48F0 0F3C	618		LH	R11,PASFLG	IS I/O ON PASLA ?	ULI06180
0E48	2332	619		SZS	GO	NO,BRANCH	ULI06190
0E4A	2621	620		AIS	R2,1	YES, MODIFY I/O ADDRESS	ULI06200

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0E4C	DE20 0A09	621	GO	CC	R2, WRITE1	OC WRITE MODE	ULI06210
0E50	9E25	622		SSR	R2,R5		ULI06220
0E52	2081	623		BTBS	8,1	WAIT FOR NOT BUSY	ULI06230
0E54	9E2E	624		WBR	R2,P14	WRITE	ULI06240
0E56	9E25	625		SSR	R2,95		ULI06250
0E58	2081	626		BTBS	8,1	WAIT FOR NOT BUSY	ULI06260
0E5A	43C9 0004	627		B	4(P9)	RETURN	ULI06270
		628	*				ULI06280
		629	*				ULI06290
0E5E	D320 0A12	630	INPUT	LB	R2, ADDRESS	LOAD I/O ADDRESS	ULI06300
0E62	CSE0 00F0	631		LHI	R14,X'F0'		ULI06310
0E66	95FE	632		EPSR	R15,R14	SET UP NEW PSW	ULI06320
0E68	D3C0 0A10	633		LB	R12,IO		ULI06330
0E6C	C5C0 0005	634		CLHI	R12,5	IS MICROBUS ON IO	ULI06340
0E70	433C 0E86	635		BE	INPUT1	YES BRANCH	ULI06350
0E74	DE20 0A08	636		OC	R2,PEAD1	NO, SET IO IN READ MODE	ULI06360
0E78	9D20	637		SSR	R2,PO		ULI06370
0E7A	2281	638		BFBS	8,1		ULI06380
0E7C	9E20	639		SSR	R2,PO		ULI06390
0E7E	2081	640		BTBS	8,1		ULI06400
0E80	9E2E	641		RDR	R2,R14	READ CHARACTER	ULI06410
0E82	43C0 0E94	642		B	INPUT2	BRANCH	ULI06420
0E86	DE20 0A08	643	INPUT1	OC	R2,READ1	SET MICROBUS IN READ MODE	ULI06430
0E8A	9E20	644		RDR	R2,PO	DUMMY READ	ULI06440
0E8C	9E20	645		SSR	R2,PO		ULI06450
0E8E	2081	646		BTBS	8,1		ULI06460
0E90	9E2E	647		RDR	R2,R14	READ CHARACTER	ULI06470
0E92	9A2E	648		WDR	R2,R14	ECHO CHARACTER	ULI06480
0E94	C4E0 007F	649	INPUT2	NHI	R14,X'7F'		ULI06490
0E98	C5F0 005F	650		CLHI	R14,X'5F'	CHECK FOR LOWER CASE CHARACTERS	ULI06500
0E9C	432C 0E44	651		BNP	INPUT3	NO, BRANCH	ULI06510
0EA0	C8E0 0020	652		SHI	R14,X'20'	YES, CONVERT TO UPPER CASE	ULI06520
0EA4	03C9	653	INPUT3	BR	R9	RETURN	ULI06530
		654	*				ULI06540
		655	*				ULI06550
0EA6	0DCA	656	TITLE	DC	X'0DOA', C'COMMON ULI TEST 06-129R07'		ULI06560
0EA8	434F4D4D 4F4E2055 4C492054 45E35420 30362231 32395230 3720 0000 0EC1	657	EDTITLE	EQU	*-1		
		658	*				ULI06570
0EC2	00C0	659	STAR	DC	X'0', X'0DOA', X'0', C'* '		ULI06580
0EC4	0DCA						ULI06590
0EC6	00C0						
0EC8	2120 0000 0EC9	660	STREND	EQU	*-1		ULI06600
		661	*				ULI06610
0ECA	0DCA	662	MSG	DC	X'0DOA', C'NO ERRORS'		ULI06620
0ECC	4E4F2045 52E24F52 5320 0000 0ED5	663	EDMSG	EQU	*-1		ULI06630

		664	*		ULI06640
		665	*		ULI06650
OED6	ODCA	666	QMSG	DC X"0DOA",C"?",X"0DOA"	ULI06660
OED8	203F				
OEDA	ODCA				
	0000 0EDB	667	EDQMSG	EQU *-1	ULI06670
		668	*		ULI06680
		669	*		ULI06690
		670	*		ULI06700
		671	*		ULI06710
OEDC	ODCA	672	MSGINT	DC X"0DOA",C"INCORRECT INTERRUPT LEVEL = "	ULI06720
OEDE	494E434F				
	52524543				
	5420494E				
	54455252				
	55505420				
	4C455645				
	4C203520				
	0000 0EF9	673	EDMEGINT	EQU *-1	ULI06730
		674	*		ULI06740
		675	*		ULI06750
OEEA	ODCA	676	ERRMSG	DC X"0DOA",C"ERROR "	ULI06760
OEEC	45E52524F				
	5220				
OF02	3030	677	ERRNC	DC C"00"	ULI06770
	0000 OF03	678	ERRMSZ	EQU *-1	ULI06780
		679	*		ULI06790
		580	*		ULI06800
OF04	ODCA	581	CPTMSG	DC X"0DOA",C"MODE = "	ULI06810
OF06	4D4E4445				
	2020203D				
	2020				
OF10	0ECA	582		DC X"0DOA",C"DEVADR = "	ULI06820
OF12	44455E41				
	4452203D				
	2020				
OF1C	0ECA	683		DC X"0DOA",C"INTLEV = "	ULI06830
OF1E	494E544C				
	45E6203D				
	2020				
OF28	0ECA	684		DC X"0DOA",C"INTRPT = "	ULI06840
OF2A	494E5452				
	50E4203D				
	2020				
	0000 0F33	685	ENOPTMSG	EQU *-1	ULI06850
		686	*		ULI06860
		687	* *****		ULI06870
		588	*		ULI06880
OF34	0000	689	MODEL	DC X"0" O = 7/16; F = 7/32	ULI06890
OF36	0000	690	LOCPSW	DC X"0" RETURN LOC FROM ERRI	ULI06900
OF38	0000	691	IIR	DC X"0" IMMED INTERR POINTER LOC	JLI06910
OF3A	0000	692	LAST	DC X"0" O=NC ERRORS; F=ERRORS]	ULI06920
OF3C	0000	693	PASFLG	DC X"0" PASLA FLAG	JLI06930
		694	*		ULI06940
		695	* *****		ULI06950
		696	*		ULI06960

OF3E	48	697	EBLATN	DB	X'48'	ULI06970	
OF3F	88	698	DBLATN	DB	X'88'	ULI06980	
OF40	40	699	EBL	DB	X'40'	ULI06990	
OF41	08	700	ATN	DB	X'08'	ULI07000	
OF42	C8	701	DRMATN	DB	X'C8'	ULI07010	
OF43	E0	702	HW	DB	X'E0'	ULI07020	
OF44	C0	703	BYTE	DB	X'C0'	ULI07030	
	00C0 OF44	704	LNZB	EQU	*-1	ULI07040	
OF48	00C0 0000	705	PSWEAVE	DCY	0,0	ULI07050	
OF4C	00C0 0000						
OF50		706	RSAVE	DS	S12	ULI07060	
		707	*	CHKSUM		ULI07070	
		708	*	(THE FOLLOWING CODE IS NOT PART OF THE TEST.)		ULI07080	
		709	*			ULI07090	
		710	*			ULI07100	
1150	24C0	711	SCHKSUM	LIS	R0,0	PUNCH M17 TAPE WITH CHECKSUM	ULI07110
1152	9510	712		EPSR	R1,R0	SELECT REG. SET 0	ULI07120
		713	*				ULI07130
1154	C810 0A00	714	LDAI	R1,ORIGIN1		START	ULI07140
1159	2421	715	LIS	R2,1		INCREMENT	ULI07150
115A	C830 0F44	716	LDAI	R3,LNZB		FINAL	ULI07160
115E	2440	717	LIS	R4,0		CHECKSUM BYTE	ULI07170
1160	D351 0000	718	SGEN	LB	R5,0(R1)		ULI07180
1164	0745	719	XAR	R4,R5			ULI07190
1165	C110 1160	720	BXLE	R1,SGEN			ULI07200
116A	D240 0099	721	STH	R4,MN+3		CHECKSUM BYTE TO BOOT LOADER	ULI07210
		722	*				ULI07220
116E	C810 0080	723	STAPE	LHI	R1,X'0080'		ULI07230
1172	9E21	724	CCR	R2,R1		DISPLAY : NORMAL MODE	ULI07240
1174	9444	725	EXBR	R4,R4			ULI07250
1175	9824	726	WHR	R2,R4		CHECKSUM BYTE TO D1	ULI07260
1178	9411	727	EXBP	R1,R1			ULI07270
117A	9501	728	EPSR	R0,R1		HALT PROCESSOR.	ULI07280
117C	D360 007A	730	SPUNCH	LB	R6,X'7A'	GET BOUTDV (PUNCH) ADDRESS.	ULI07300
1180	DE60 0078	731		CC	R6,X'7B'	START TAPE PUNCH	ULI07310
1184	9D60	732		SSR	R6,RO		ULI07320
1186	2081	733		BTBS	8,1		ULI07330
1188	41F0 11CA	734		BAL	R15,STAPL	PUNCH LEADER	ULI07340
118C	9411	735		EXRR	R1,R1	(R1) = X'0080'	ULI07350
118E	C830 00CF	736		LHI	R3,X'CF'		ULI07360
1192	DAE1 0000	737	SPNCH1	WD	R6,0(R1)	PUNCH BOOT LOADER	ULI07370
1195	9D60	738		SSR	R6,RO		ULI07380
1198	2081	739		BTBS	8,1		ULI07390
119A	C110 1192	740		BXLE	R1,SPNCH1		ULI07400
119E	41F0 11D0	741		BAL	R15,STAPL1	PUNCH ONE-FOLD GAP.	ULI07410
		742	*				ULI07420
11A2	D340 0099	743		LB	R4,MN+3	GET CHECKSUM BYTE	ULI07430
11A6	C810 0A00	744		LDAI	R1,ORIGIN1	(NORMALLY X'A00')	ULI07440
11AA	C830 0F44	745		LDAI	R3,LNZB		ULI07450
11AE	D351 0000	746	SPNCH2	LB	R5,0(R1)	PUNCH PROGRAM	ULI07460
11B2	0745	747		XAR	R4,R5		ULI07470
11B4	9A65	748		WDR	R6,R5		ULI07480
11B6	94C1	749		EXBR	R0,R1		ULI07490
11B8	9820	750		WHR	R2,RO	DATA ADDRESS TO DISPLAY.	ULI07500

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11BA	9D60	751	SSR	R6, R0		ULI07510
11BC	2081	752	BTBS	8,1		ULI07520
11BE	C110 11AE	753	BXLE	R1, SPNCH2		ULI07530
11C2	41F0 11CA	754	BAL	R15, STAPL	PUNCH TRAILER.	ULI07540
11C6	4300 115E	755	B	STAPE	DISPLAY CHECKSUM, HALT PROCESSOR.	ULI07550
11CA	C800 0100	757	STAPL	LHI	TO PUNCH BLANK LEADER	ULI07570
11CE	23C3	758	BS	STAPLP		ULI07580
11DO	C800 0055	759	STAPL1	LHI	TO PUNCH 1-FOLD GAP	ULI07590
11D4	27C1	760	STAPLP	SIS	RETURN	ULI07600
11D6	032F	761	BNP8	R15		ULI07610
11D8	2430	762	LIS	R3,0		ULI07620
11DA	9A63	763	WDR	R6, R3	PUNCH BLANK FRAME	ULI07630
11DC	9DE8	764	SSR	R6, R8		ULI07640
11DE	2081	765	BTBS	8,1		ULI07650
11EO	22C6	766	BS	STAPLP	CONTINUE.	ULI07660
		767	*			ULI07670
11E2		768	END			ULI07680

NO ERRORS 0 SQUEZ PASSES

CAL 04-01

SCHKSUM	1150					
SGEN	1160	720				
SPNCH1	1192	740				
SPNCH2	11AE	753				
SPUNCH	117C					
STAPE	116E	755				
STAPL	11CA	734	754			
STAPL1	11D0	741				
STAPLP	11D4	758	766			
ARSTOP	11E2					
ADC	0002					
ADDRESS	0A12	615	630			
ACK	0DE2	409				
ATN	0E41	411				
POOT	0088	157				
BTH	0D6A					
BYTE	0F44					
CARDUADR	0A1A					
CMD	0ABC					
CONTINT	0CD8					
CRT	0A62	232	234			
CRT1	0A64					
CRTADR	0A14					
DBLAIN	0F3F	413				
DR16	0C7E	417				
DR32	0C86	421				
DRMATN	0F42	412				
DROP	0C64	430				
EBL	0F40	415				
EBLATN	0F3E	424				
EDMSG	0ED5	583				
EDMSGINT	0FF9	568				
EDQMSG	0EDB					
EDTITLE	0EC1					
FNOPTMSG	0F33	611				
ERRI	0D74					
ERRI1	0D8A	541				
ERRINT	0CF4					
ERRMEG	0EFA	558				
ERRMSZ	0F93	559				
ERRNO	0F02	554				
ERROR	0D9A	400	429	437	525	537
EXECUTE	0BC2					
GO	0E4C	619				
HDIT	0DD2	571				
HEX	0B94					
HEXASC	0B68					
HEXLP	0B7C					
HW	0F43					
IIP	0F38	419				
IMPTOP	0000R					
INC	0B36					

NO ERRORS 0 SQUEZ PASSES

CAL 04-01

SCHKSUM	1150					
SGEN	1160	720				
SPNCH1	1192	740				
SPNCH2	11AE	753				
SPUNCH	117C					
STAPE	116E	755				
STAPL	11CA	734	754			
STAPL1	11D0	741				
STAPLP	11D4	758	766			
ARSTOP	11E2					
ADC	0002					
ADDRESS	0A12	615	630			
ACK	0DE2	409				
ATN	0E41	411				
PCOT	0088	157				
BTH	0D6A					
BYTE	0E44					
CAROUADR	0A1A					
CMD	0ABC					
CONTINT	0CD8					
CRT	0A62	232	234			
CRT1	0A84					
CRTADR	0A14					
DBLAIN	0F3F	413				
DR16	0C7E	417				
DR32	0C86	421				
DRMATN	0F42	412				
DROP	0C64	430				
EBL	0F40	415				
EBLATN	0F3E	424				
EDMSG	0ED5	583				
EDMSGINT	0FF9	568				
EDQMSG	0EDB					
EDTITLE	0EC1					
FNOPTMSG	0F33	611				
ERRI	0D74					
ERRI1	0D8A	541				
ERRINT	0CF4					
ERRMSG	0EEA	558				
ERRMSZ	0F03	559				
ERRNO	0F02	554				
ERROR	0D9A	400	429	437	525	537
EXECUTE	0BC2					
GO	0E4C	619				
HDIT	0DD2	571				
HEX	0B94					
HEXASC	0B68					
HEXL	0B7C					
HW	0F43					
IIP	0F38	419				
IMPTOP	0000R					
INC	0B36					

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TSTD\$1	0D1C	
TSTD\$2	0D30	526
TTY	0A48	
TTYADR	0A15	
TTYBUF	0B30	
TTYIN	0AE3	578 584 578 584 512
ULIADR	0ABC	
WAIT1	0C8C	427
WAIT2	0CEC	
WRITE1	0A09	521
WRTITLE	0FA8	