FLOATING POINT PROCESSOR

INSTRUCTION MANUAL

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 June 1978

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-568

TITLE Floating Point Processor Instruction Manual

REVISION R05 DATE June 1978

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ii	R05	6/78
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CHAPTER 1
BLOCK DIAGRAM ANALYSIS

1.1 INTRODUCTION

Floating point is a means of representing quantity in any numbering system. This representation takes the form of a series of digits multiplied by a base number which is raised to some power. The convenience with which extremely large or small numbers can be compactly expressed in floating point notation, makes it ideally applicable to scientific computations. (Appendix 1 contains background information on floating point notation.) When floating point is used in the INTERDATA 8/16 and 7/32 CII computers, the decimal numbering system is replaced by the hexadecimal system.

The INTERDATA Floating Point Processor (FPP) provides a preprogrammed means of manipulating scientific data expressed as floating point numbers. When a host processor, such as the 8/16 or 7/32 CII is required to perform calculations involving floating point numbers, it presents the numbers to the FPP. The FPP contains ROM controlled hardware that performs the calculations and the results are sent back to the host processor.

The block diagram (Figure 1-1) shows that the Floating Point Processor (FPP) is organized between two 64-bit buses. The D-bus is used to present data from the external Data Register to a processor containing an ALU and internal registers. The S-bus transfers the ALU output back to the external Data Register. The Data Register is used both for temporary storage and to facilitate I/O operations. The sources, destinations, and functions of the ALU are controlled by a micro-program contained in the Read-Only-Memory (ROM).

1.2 INSTRUCTION REGISTER

A 16-bit instruction register is formed by the combination of the user operation code (OP) (8 bits), and the YD and YS address fields (4 bits each). It is normally loaded from the memory data bus of the host processor. The exceptions are for power-up and power-down routines, and for console display support. In these three cases a multiplexor can select the Input/Output bus of the host processor instead.

1.3 DROM (Decoder Read Only Memory)

The DROM interprets the user OP code to determine a starting address in the FPP microprogram for the particular floating-point instruction being emulated. In addition the DROM indicates to the hardware whether a single or double precision instruction is present, and whether the OP field contains a legal floating-point instruction for the particular implementation of the FPP.

1.4 ROM Address Register

Locations in the ROM are addressed by the 8-bit ROM Address Register (RAR). Micro-instructions are normally located at sequential addresses in the ROM. The RAR is an up-counter which increments by one as each new micro-instruction is read into the ROM Data Register (RDR). It, therefore, holds the address of the next micro-instruction to be executed. When it becomes necessary to jump out of sequence, the RAR can be loaded with a new address from the RDR or it can be cleared to 0 by the hardware. Initially the RAR is loaded with a starting address from the DROM.

1.5 ROM (Read Only Memory) and RDR (ROM Data Register)

The ROM is a non-destructive memory of 256 words. Each word is 28 bits long and represents one micro-instruction. Each word read out of ROM is placed in the 28-bit ROM Data Register (RDR). Micro-instructions are executed in one machine cycle of 215 nanoseconds, except for 64-bit arithmetic instructions which require one extra cycle. The results of the instructions become available some time before the end of the appropriate machine cycle so that, at the start of the next cycle, the selected destination register is loaded (and other specified action taken) and the next micro-instruction is fetched.

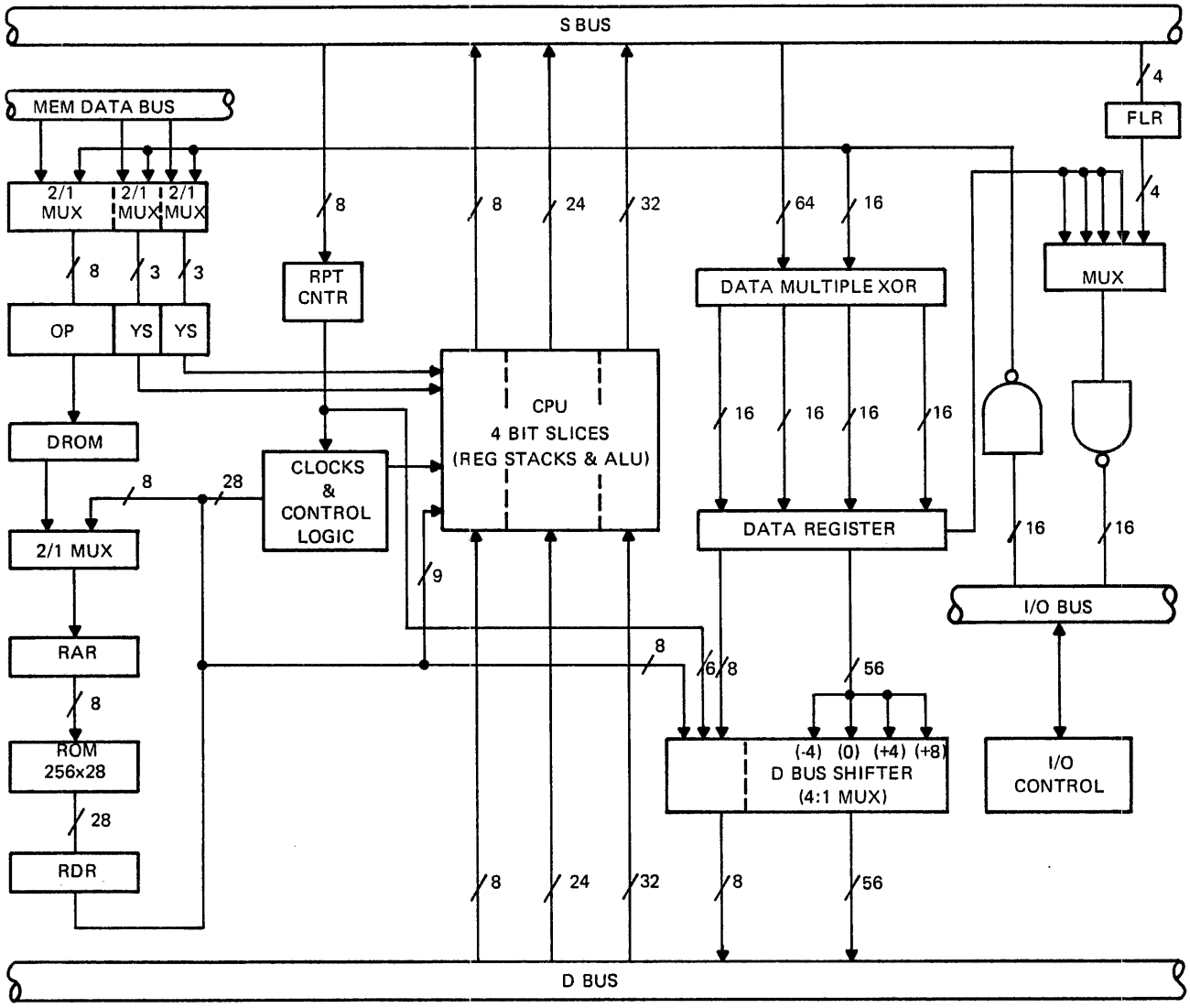


Figure 1-1 FLOATING POINT PROCESSOR BLOCK DIAGRAM

1.6 REPEAT COUNTER

The Repeat Counter is an 8-bit counter which can be loaded from the S-Bus, and incremented and cleared by the hardware. The counter allows a selected micro-instruction to be executed a given number of times and can record how many times a particular micro-instruction was executed until some condition was satisfied.

1.7 FLR (FLAGS)

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater than Zero (G), and Less than Zero (L). These flags are modified at the conclusion of the floating point instruction to reflect the result of that operation.

1.8 LSI ALU and REGISTER STACKS

Sixteen 4-bit wide LSI circuits make up the 64-bit wide processor. Together the LSI circuits contain a 64-bit Arithmetic Logic Unit (ALU), a two port Random Access Memory (RAM) stack of sixteen 64-bit Floating Point Registers and one 64-bit temporary storage register (Q). Also included are shift circuits for right, left, and no shift for both the RAM stack and the Q-register.

1.9 CLOCK

The basic system clock is variable and nominally set for a period of 215 nanoseconds. It is non-stoppable. From this are derived several other stoppable clocks for the RAR, RDR, DR, and processor circuits.

1.10 CONTROL LOGIC

The Control Logic hardware interprets the contents of the RDR and provides control signals to the processor, Multiplexor, all Registers, and I/O Control for the current operation.

1.11 DATA MULTIPLEXORS

The Data Multiplexor selects, as a source for the Data Register (DR), either the 64-bit S-bus or the 16-bit I/O bus repeated four times. The Data Register is a 64-bit Register used both for temporary storage by the micro-program and as an I/O Register.

The D-Bus shifter is comprised of 64 four-to-one multiplexors. For the fraction field (bits 8 to 63) the D-bus determines whether the shift operation will be: no shift, 1 hexadecimal digit right, 2 hexadecimal digits right, or one hexadecimal digit left. For the exponent field (bits 0 to 7) the D-bus selects among the following: the DR (bits 0 to 7); the Repeat Counter Output bits; Immediate Data bits from the RDR; the result sign from the hardware sign determination logic followed by 7 zeros.

1.12 I/O CONTROL

The I/O Multiplexor selects which one of four 16-bit data fields from the DR is to be sent out on the I/O bus to the host processor. The I/O Multiplexor also selects the Flag Register to send the condition code when appropriate.

The I/O Control controls the handshaking between the FPP and the host processor. The control also loads the Instruction Register when a legal floating point instruction is detected.

CHAPTER 2
MICROPROGRAM DESCRIPTION

2.1 INTRODUCTION

Microprogramming is a means for implementing the control logic of a digital processor. The Floating Point Processor (FPP) is designed to execute micro-instructions stored in a Control Store or Read Only Memory (ROM). A micro-instruction is an elemental step or instruction to the actual hardware of the FPP. Each micro-instruction causes one or more hardware functions to be performed, such as transferring the contents of one register to another, an arithmetic or logical operation between two specified operands, or communicating with the host processor.

A series of micro-instructions is called a microprogram. The microprogram of the FPP is, by definition, an emulator. It emulates the single precision and double precision floating point instructions as described in the *INTERDATA User's Manual (16 Bit),* Publication Number 29-509 and in the *32-Bit Series Reference Manual,* Publication Number 29-365. The FPP accepts the user level instruction and the necessary data (for RX type of user level instructions); performs the specified floating point operation; presents the resulting Condition Code (and the result, if necessary) to the host processor; and then waits for the next floating point instruction to emulate.

The FPP is an optional module of the host processor, communicating with the host processor through the Input/Output Multiplexor Bus. Within the FPP itself, there is an option of either single precision only or both single and double precision floating point instructions.

The following sections outline the FPP hardware functions from a micro-programmer's point of view including data and micro-instruction formats, user instruction emulation and display support.

2.2 DATA FORMATS

All the internal data paths of the FPP are 64-bits wide for Double Precision and 32 bits wide for Single Precision. Hence, the basic operand is a 64-bit or a 32-bit precision floating point number. The most significant bit (bit 0) is the sign bit. Bits 1:7 contain the exponent (base 16) in excess-64 notation. Bits 8:63 (or Bits 8:31 for single precision) contain the fraction. The processor has a capability of operating on the exponent field, the fraction field, or the whole floating point number.

In case of single precision floating point numbers, Bits 32:63 are normally zero except for intermediate steps in the instruction emulation.

2.3 INSTRUCTION FORMATS

The FPP micro-instructions can be in one of three formats designated as Register-to-Register, Immediate-to-Register and Branch Control instruction. Each micro-instruction is 28 bits wide. The Instruction Word Chart is shown in Table 2-1 and the Instruction Formats are shown in Table 2-2.

As shown in Table 2-2, the first data field (bits 0, 1, 2) designates the format of the micro-instruction. That is, whether the format is Register-to-Register, Immediate-to-Register or a Branch Control instruction. Table 2-3 shows that the instruction is specified by the bits in the data field. Specifically, Register-to-Register instructions are specified by the last four commands shown in Table 2-3 (100, 101, 110, 111). A branch instruction is specified by bit positions 010 and 011, and an Immediate-to-Register instruction is designated by bits 001.

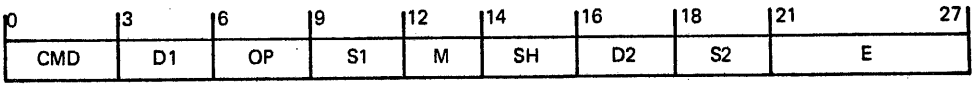
TABLE 2-1. FLOATING POINT PROCESSOR INSTRUCTION WORD CHART

	CONT	DEST	ALU OP	SOURCE	OP MODE	SHIFT	IMM EXT DEST	IMM EXT SOURCE	E FIELD	
	0 1 2	3 4 5	6 7 8	9 10 11	12 13	14 15	16 17	18 19 20	21 22 23 24 25 26 27	
NOP	0 0 0			LFR	0 0				0 0 0 0 0 0 0	NULL
IMM	0 0 1			EX	0 1		0 0	NULL	0 0 0 0 0 1	EOJ
BT	0 1 0			FR	1 0		0 1	CNTR	0 0 0 0 1 0	DEOJ
BF	0 1 1			<64>	1 1		1 0	DR	0 0 0 1 0 0	F
CNM	1 0 0	←				1 1			0 1 0 0 0 0	SETV
CEQ	1 0 1	←				0 1			1 0 0 0 0 0	SETC
MPY	1 1 0	1 0 0	0 0 0	0 1 1					0 1 0 0 0 0 0	MOD816
DIV	1 1 1	1 1 0	0 0 0	1 0 1					0 0 0 0 0 1	JAMCI
LOAD Q; ALU OUTPUT		0 0 0							0 0 0 0 1 0	SETGD
NULL; ALU OUTPUT		0 0 1							0 0 0 1 0 0	F
LOAD YD; A OUTPUT		0 1 0			1 0 ↔	0 0	SR8		0 1 0 0 0 0	ORBIT11
LOAD YD; ALU OUTPUT		0 1 1			1 0 ↔	0 1	SR4	DR	1 0 0 0 0 0	T.KOP
LOAD YD&Q; SR; ALU OUTPUT		1 0 0				1 0	NO SHIFT	SOURCE	1 0 0 0 0 0 0	
LOAD YD; SR; ALU OUTPUT		1 0 1							0 0 0 0 0 1	AGB
LOAD YD&Q; SL; ALU OUTPUT		1 1 0			1 0 ↔	1 1	SL4		0 0 0 1 0 0	ALB
LOAD YD; SL; ALU OUTPUT		1 1 1			0 1 ↔	1 1	CNTR	SOURCE	0 0 1 0 0 0	F
		R + S	0 0 0						0 1 0 0 0 0	RCO
		S - R	0 0 1						1 0 0 0 0 0	IFNRC
		R - S	0 1 0						0 0 0 0 0 0	YDP2
		R OR S	0 1 1						0 0 0 0 0 1	EOJ
		R AND S	1 0 0						0 0 0 1 0 0	ALBAGB
		$\overline{R}$ AND S	1 0 1						0 0 1 0 0 0	F
		R XOR S	1 1 0						0 1 0 0 0 0	RXWAIT
		R XNOR S	1 1 1						1 0 0 0 0 0	DRSIGN
						0 0		0 1 1	GDIGIT	
								1 0 0	ASIGN	
								1 0 1	BSIGN	
								1 1 0	ADDSIGN	
								1 1 1	MDSIGN	
		R / S								
		YS / Q		0 0 0						
		YS / YD		0 0 1						
		0 / Q		0 1 0						
		0 / YD		0 1 1						
		0 / YS		1 0 0		0 1 ↔	0 0	0 0 0	'00'	
EXTERNAL SOURCE		D / YD		1 0 1			0 0	0 0 1	'01'	
		D / Q		1 1 0			0 0	1 0 0	'08'	
		D / 0		1 1 1			1 0	0 0 0	'40'	
							1 0	1 0 0	'48'	
							1 0	1 1 0	'46'	
							1 1	1 1 1	'7F'	
							0 0	0 1 0	'06'	

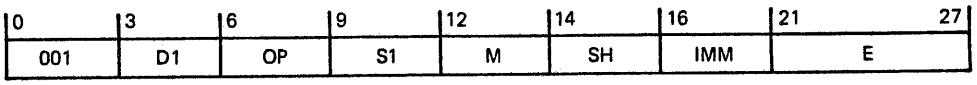
	BRANCH CONDITION						BRANCH ADDRESS	
	3 4 5	6 7 8	9 10 11	12 13	14 15	16 17	18 19 20	21 22 23 24 25 26 27
DR0	0 0	0 0 0	0 0 0	0 0	1 0	0	0 0	NULL
DR8	0 0	0 0 0	0 0 0	0 0	0 1	0	0 1	SET DR0
G	1 0	0 0 0	0 0 0	0 0	0 0	0	1 0	CLR CNTR
C	0 1	0 0 0	0 0 0	0 0	0 0	1	0 0	UCC
CE	0 0	1 0 0	0 0 0	0 0	0 0			
CF	0 0	0 1 0	0 0 0	0 0	0 0			
YDC	0 0	0 0 1	0 0 0	0 0	0 0			
>6	0 0	0 0 0	1 0 0	0 0	0 0			
NORM	0 0	0 0 0	0 1 0	0 0	0 0			
UNCOND	0 0	0 0 0	0 0 1	0 0	0 0			
DRHD0	0 0	0 0 0	0 0 0	1 0	0 0			
DRHD1	0 0	0 0 0	0 0 0	0 1	0 0			
	3 4 5	6 7 8	9 10 11	12 13	14 15	16 17	18 19 20	21 22 23 24 25 26 27

TABLE 2-2. INSTRUCTION WORD FORMAT

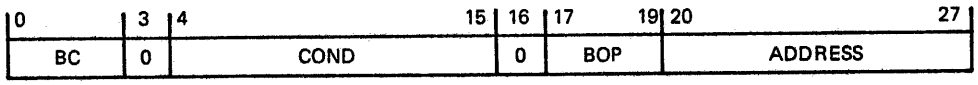
REGISTER-TO-REGISTER



IMMEDIATE-TO-REGISTER



BRANCH



INSTRUCTION WORD FIELDS

FIELD	MEANING
CMD	NORMALIZE, EQUALIZE, MULTIPLY OR DIVIDE COMMAND
D1	SHIFT LEFT, SHIFT RIGHT BY ONE BIT
D1 AND D2	DESTINATION FIELDS
OP	ALU OPERATION
S1	SELECT TWO SOURCES OF ALU
S2	SELECT EXTERNAL (TO ALU) SOURCE
M	MODE OF OPERATION: EXPONENT, FRACTION OR WHOLE NUMBER
SH	SHIFT LEFT, SHIFT RIGHT BY FOUR OPERATION
E	EXTENDED OPTION FIELD
IMM	IMMEDIATE DATA FIELD
BOP	BRANCH OPTIONS
BC	BRANCH CONTROL
COND	BRANCH CONDITION
ADDRESS	BRANCH ADDRESS

TABLE 2-3 FIRST DATA FIELD

INSTRUCTION WORD BITS 012	MEANING
000	NOP: NO OPERATION
001	IMM: REGISTER TO IMMEDIATE INSTRUCTION
010	BT: BRACH ON TRUE CONDITION
011	BF: BRACH ON FALSE CONDITION
100	CNM: COMMAND NORMALIZE
101	CEQ: COMMAND EQUALIZE
110	MPY: COMMAND MULTIPLY
111	DIV: COMMAND DIVIDE

BT — If a specified condition is true, a branch is taken to the specified ROM address.

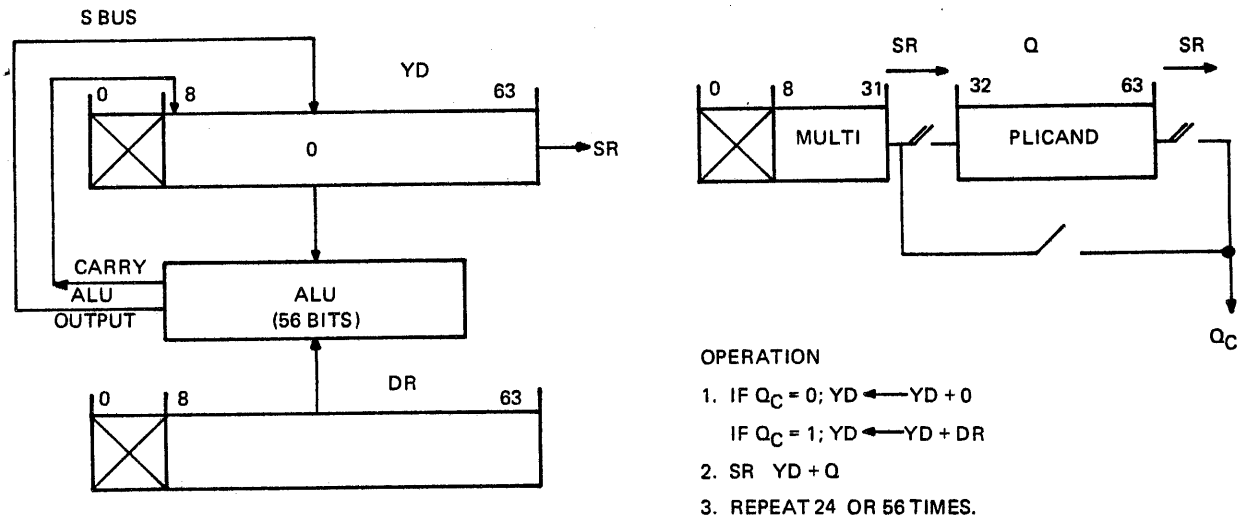
CEQ — The CNTR contains the exponent difference. The DR contains the fraction portion of the floating point number to be equalized. The CEQ command shifts the fraction in DR right hexadecimally (4 Bits at a time) and CNTR is decremented by one for each hexadecimal shift until CNTR is zero. In double precision the fraction bits are shifted right and lost. In single precision the fraction bits are shifted right into the least significant half of DR and all of them are retained for further computation.

MPY — Two unsigned fractions, 24 Bits or 56 Bits wide, are multiplied. The logical set up for MPY command is as shown in Figure 2-1.

BF — If a specified condition is false, a branch is taken to the specified ROM address. An unconditional branch micro-instruction assembles as a branch on true micro-instruction.

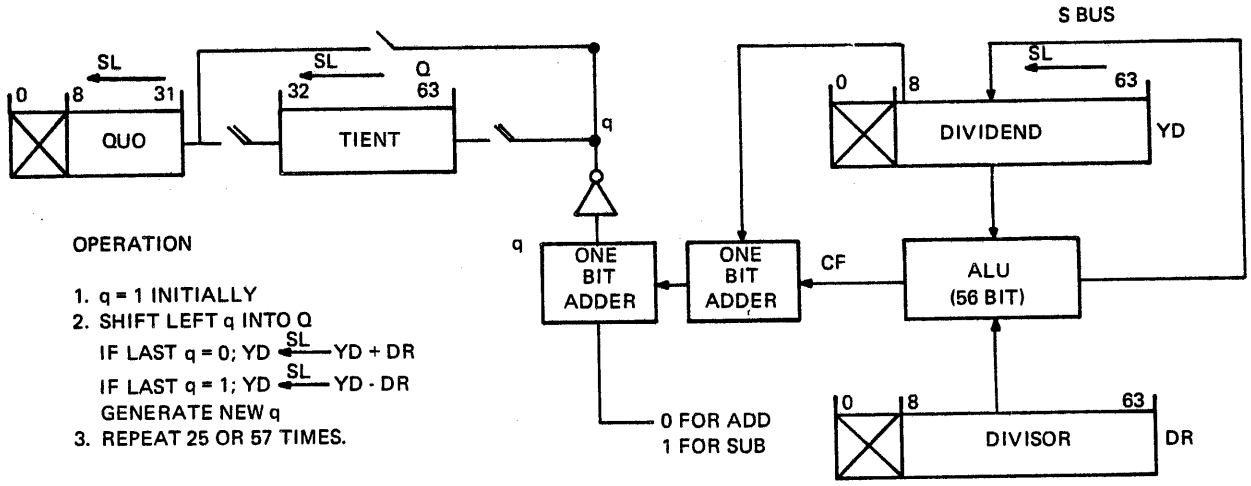
CNM — The fraction contained in DR is non-zero and unnormalized. The fraction contained in DR is shifted left hexadecimally (4 Bits at a time) and CNTR is incremented by one for each hexadecimal shift until the fraction is normalized. The net result of CNM is a normalized fraction in DR and an exponent count in CNTR. The DR Bits 8:63 participate in this operation. Thus, positions 32:63 are brought into significance during the execution of this command, thus increasing precision.

DIV — The unsigned division is performed using the non-restoring division algorithm. The dividend, divisor and quotient are all 24 or 56 bits wide for single precision or double precision respectively. The logical set up for the DIV command is as shown in Figure 2-2.



NOTES:
1. THE SWITCHES ——//—— ARE CLOSED FOR DOUBLE PRECISION ONLY.
2. THE SWITCH ——/—— IS CLOSED FOR SINGLE PRECISION ONLY.
3. BITS 0:7 OF THE REGISTERS DO NOT PARTICIPATE IN THE MPY COMMAND AND REMAIN UNCHANGED.
4. FOR SINGLE PRECISION, DR(32:63) = 0.
5. GUARD DIGIT = BIT 32 ON S BUS DURING THE LAST CYCLE OF MPY COMMAND.
6. YD(8:31) OR YD(8:63) = FINAL MPY RESULT.
7. HARDWARE SETS THE COUNTER (CNTR=24 OR 56).
8. THE MPY COMMAND REQUIRED 24 OR 56 CYCLES.

Figure 2-1. Register Connections Caused By The Multiply Command



NOTES: THE UNSIGNED DIVISION IS PERFORMED USING THE NON-RESTORING DIVISON METHOD.
1. THE SWITCHES ——\\—— ARE CLOSED FOR DOUBLE PRECISION ONLY.
2. THE SWITCH ——\—— IS CLOSED FOR SINGLE PRECISION ONLY.
3. BITS 0:7 OF THE REGISTERS DO NOT PARTICIPATE IN THE DIV COMMAND AND REMAIN UNCHANGED.
4. FOR SINGLE PRECISION, DR(32:63) AND YD(32:63) = 1.
5. GUARD DIGIT = q GENERATED DURING THE LAST CYCLE OF DIV COMMAND.
6. Q(8:31) OR Q(8:63) = FINAL DIV RESULT.
7. HARDWARE SETS THE COUNTER (CNTR = 25 OR 57).
8. THE DIV COMMAND REQUIRES 25 OR 57 CYCLES.

Figure 2-2. Register Connections caused by the Divide Command

2.4 REGISTER-TO-REGISTER AND IMMEDIATE-TO-REGISTER INSTRUCTIONS

2.4.1 Mode of Operation (M)

Bits 12 and 13 of the instruction word specify the mode. Table 2-4 shows what the bit positions designate.

TABLE 2-4 MODE OF OPERATION

INSTRUCTION WORD BITS 12	13	MEANING	RELATED CARRY
1	1	64-BIT OPERATION	C
0	1	EXPONENT (BITS 0:7) OPERATION	CE
1	0	FRACTION (BITS 8:63) OPERATION	CF
0	0	LOWER HALF OF FRACTION (BITS 32:63) OPERATION	–

2.4.2 Shift Options (D1 and SH)

Shift options can be specified by bits 3, 4, 5 and bits 14, 15 as shown in Table 2-5.

TABLE 2-5 SHIFT OPTION BITS

OPTION 3 – 5	MEANING	SOURCE MUST BE	DESTINATION MUST BE
SL	SHIFT LEFT BY ONE	–	YD OR YD&Q
SR	SHIFT RIGHT BY ONE	–	YD OR YD&Q
14 – 15			
SL4	SHIFT LEFT BY FOUR	DR	–
SR4	SHIFT RIGHT BY FOUR	DR	–

2.4.3 Extended Field Options (E)

The Extended Field Options (bits 21 through 27) provide convenience of specifying desired hardware functions necessary in the course of emulation. Any micro-instruction, except Branch, can specify up to five E Field options that belong to any one of the four groups shown in Table 2-6.

TABLE 2-6 EXTENDED FIELD OPTIONS

INSTRUCTION WORD BITS 21	22	23	24	25	26	27	OPTION	MEANING
0	0	0	0	0	0	0	NULL	
		0	0	0	0	1	EOJ	END OF JOB
		0	0	0	1	0	DEOJ	DOUBLE PRECISION END OF JOB
		0	0	1	0	0	F	UPDATE C, CE, CF, G AND L FLAGS
		0	1	0	0	0	SETV	SET V FLAG
		1	0	0	0	0	SETC	SET C FLAG
0	1	0	0	0	0	0	MOD816	DETERMINES SIZE OF FIXED POINT REGISTER
		0	0	0	0	1	JAMCI	FORCE A CARRY IN FOR THIS OPERATION
		0	0	0	1	0	SETGD	SET GUARD DIGIT
		0	0	1	0	0	F	UPDATE C, CE, CF, G AND L FLAGS
		0	1	0	0	0	ORBIT11	OR IN BIT 11 ON TO S BUS
		1	0	0	0	0	TAKOP	TAKE OVER ALU OPERATION
1	0	0	0	0	0	0		
		0	0	0	0	1	AGB	A > B
		0	0	0	1	0	ALB	A < B
		0	0	1	0	0	F	UPDATE C, CE, CF, G AND L FLAGS
		0	1	0	0	0	RCO	UPDATE ROUNDING CARRY (CF) FLAG ONLY
		1	0	0	0	0	IFNRC	ALLOW DESTINATION CLOCK IF NO ROUNDING CARRY
1	1	0	0	0	0	0	YDP2	INCREMENT YD FIELD BY 2
		0	0	0	0	1	EOJ	END OF JOB
		0	0	0	1	0	ALBAGB	A < B OR A > B
		0	0	1	0	0	F	UPDATE C, CE, CF, G AND L FLAGS
		0	1	0	0	0	RXWAIT	WAIT FOR DR DATA
		1	0	0	0	0	DRSIGN	UNLOAD DR SIGN ALSO

EOJ — End of Job. Specifying the EOJ option terminates the emulation sequence. The host processor is signalled that the Condition Code or data are ready to be transferred to the host processor. EOJ also forces a branch in the microcode to the power up ROM address where DR is cleared.

DEOJ — Double precision End of Job. Specifying the DEOJ option terminates the emulation of a double precision floating point instruction. It signals the host processor that the Condition Code is ready to be transferred. DEOJ also forces a Branch in the microcode to the power up ROM address where DR is cleared.

F — Flags. The F option updates the following flags (depending on the mode of operation) reflecting the result of the micro-instruction specifying F. The previous state of the flag is ignored.

C: Carry flag in FLR consisting of the Carry out of or borrow into Bit 0. (<64>)
CE: Exponent Carry, i.e. , state of Bit 0. (EX mode)
CF: Fraction Carry, i.e., carry out of or borrow into Bit 8 (FR mode)
G: Greater than zero flag in FLR.

Bits 1:63	<64>	mode
Bits 1:7	EX	mode
Bits 8:63	FR	mode

If all the bits in the specified mode are zero, G=0; otherwise G=1 provided L=0.

L: Less than zero flag in FLR. In the <64> mode, L=Bit 0. This flag is not affected in the EX, FR or LFR mode.

SETV — Set V flag.. When specified, the V flag in the Flag Register (FLR) is set.

SETC — Set C flag. When specified, the C flag in the Flag Register (FLR) is set.

SETGD — Set Guard Digit. Specifying the SETGD option sets, for single precision only, the Guard Digit as follows:

Guard Digit = Bit 32 on S Bus for Add, Subtract and Multiply
= last q (quotient bit) generated for Divide

ORBIT11 — Or Bit 11. When specified, a logic one (1) is ORed into bit 11 of the D Bus.

YDP2 — YD Plus 2. When specified, the YD field of the Instruction Register (IR) is incremented by 2. When YD field changes from 'E' to '0', a YD Carry (YDC) flag is set.

AGB — A Greater Than B. This option specifies, to the result sign computation logic, that A (the first operand) is algebraically greater than B (the second operand).

ALB — A less Than B. This option specifies, to the result sign computation logic, that A (the first operand) is algebraically less than B (the second operand).

TAKOP — Takeover Operation. This option refers to the ALU operation. The microcode specifies two operands R and S. Specifying this option determines the ALU operation as shown in Table 2-7.

TABLE 2-7 TAKEOVER OPERATION

ASIGN ⊕ BSIGN	CF	OPERATION	INSTRUCTION BITS 6:8
0 (EQUAL)	X	R + S	000
1 (DIFFER)	0	S - R	001
1 (DIFFER)	1	R - S	010

X = DON'T CARE

RCO — Rounding Carry. This option is specified in a micro-instruction trying to determine if rounding produces a carry into the exponent field. When this option is specified the Fraction Carry (CF) flag is set or reset depending on whether a fraction carry is produced or not. All other flags remain unchanged.

IFNRC — If No Rounding Carry. When this option is specified the following function is performed.
1. If CF=0, load the destination register with data on S Bus.
2. If CF=1, the destination register remains unchanged, i.e., skip the destination clock.

DRSIGN — DR Sign participates. Normally the sign of a floating point number in DR (Bit 0 of DR) is not unloaded onto the B Bus. But when DRSIGN option is specified, the DR sign is unloaded onto the B Bus and the whole floating point number participates as an operand to the ALU.

ALBAGB — A Less than B or B Less than A. This option specifies, to the result sign computation logic, whether A (the first operand), is algebraically less than, equal to, or greater than B (the second operand). The function is performed in the following manner:

CF	C	Specify
0	0	A=B
0	1	A>B
1	X	A<B

RXWAIT — For RX instructions, wait for DR data. When an RX-type of user level instruction is decoded, the emulation sequence is started at an appropriate ROM location. At that time the second operand may not be yet established in DR. When this option is specified and the second bit of the IR (RX) is set, the micro-instruction execution is suspended (clocks are stopped), unless and until the second operand is established in DR.

In addition, FLR (op code=2F) and FLDR (op code=3F) wait for DR data. When this option is specified and IR05:07 = 111, the micro-instruction execution is suspended (clocks are stopped), unless and until the second operand is established in DR.

MOD816 — The FPP is strapped according to whether the fixed point register in the host processor is 16-bit or 32-bit. This option informs the FPP microcode of which configuration to use.

JAMCI — Forces the Carry In to a one for the current operation.

2.5 BRANCH CONTROL INSTRUCTIONS

A branch micro-instruction can specify any of twelve conditions. The micro-instruction word bits, symbolic conditions and their meanings are shown in Table 2-8.

TABLE 2-8 BRANCH CONTROL INSTRUCTIONS

WORD BITS 4 5 6 7	8 9 10 11	12 13 14 15	NAME	MEANING OF TRUE CONDITION
1 0 0 0	0 0 0 0	0 0 0 0	G	THE RESULT IS NON-ZERO
0 1 0 0	0 0 0 0	0 0 0 0	C	CARRY (BORROW) OUT OF BIT 0 OCCURRED
0 0 1 0	0 0 0 0	0 0 0 0	CE	CARRY (BORROW) OUT OF BIT 1 OCCURRED
0 0 0 1	0 0 0 0	0 0 0 0	CF	CARRY (BORROW) OUT OF BIT 8 OCCURRED
0 0 0 0	1 0 0 0	0 0 0 0	YDC	CARRY OUT OF YD FIELD OCCURRED
0 0 0 0	0 1 0 0	0 0 0 0	> 5	(CNTR) > 6 OR (CNTR) > 13
0 0 0 0	0 0 1 0	0 0 0 0	NORM	THE RESULT IS NORMALIZED
0 0 0 0	0 0 0 1	0 0 0 0	UNCOND	UNCONDITIONAL BRANCH
0 0 0 0	0 0 0 0	1 0 0 0	DRHD0	DR HEX. DIGIT ZERO (BITS 0:3) = 0
0 0 0 0	0 0 0 0	0 1 0 0	DRHD1	DR HEX. DIGIT ONE (BITS 4:7) = 0
0 0 0 0	0 0 0 0	0 0 1 0	DR0	BIT 0 OF DR
0 0 0 0	0 0 0 0	0 0 0 1	DR8	BIT 8 OF DR

G,C,CE,CF,YDC	These branch conditions are flags as explained under Extended Field options (E).
NORM	This condition is true (=1) when the fraction in DR is normalized, i.e., bits DR08:11 are not all equal to 0.
UNCOND	An unconditional branch is taken to the specified ROM address.
DRHD0	This condition is true (=1) when the DR hexadecimal digit zero (bits DR00:03) is non-zero.
DRHD1	This condition is true (=1) when the DR hexadecimal digit one (bits DR04:07) is non-zero.
DRO	This condition is true (=1) when Bit 0 of the DR equals a one.
DR8	This condition is true (=1) when bit 8 of the DR equals a on e.

Any ROM address from X'00' through X'FF' can be specified as a branch address in any Branch micro-instruction.

2.6 MICROPROGRAM OPERATION

2.6.1 Floating Point Processor Initialization

On power up or after depressing the INIT key, the following FPP elements are cleared:

1. ROM Address Register (RAR)
2. The Counter Register (CNTR)
3. The Flag Register (FLR)
4. The flags CE, CF, YDC, >5

2.6.2 Instruction Decoding

When a host processor fetches a user level instruction from the main memory, the first halfword of that instruction is captured by the FPP from the memory bus. The instruction halfword is placed in the Instruction Register (IR).

The most significant byte of the IR (IR00:07) contains the operation code of the user level instruction. The op-code is used as an address to index into the Decoder ROM (DROM). The DROM is a 256 word x 8 bits Read Only Memory. Each word in the DROM contains data in the format shown in Figure 2-3.

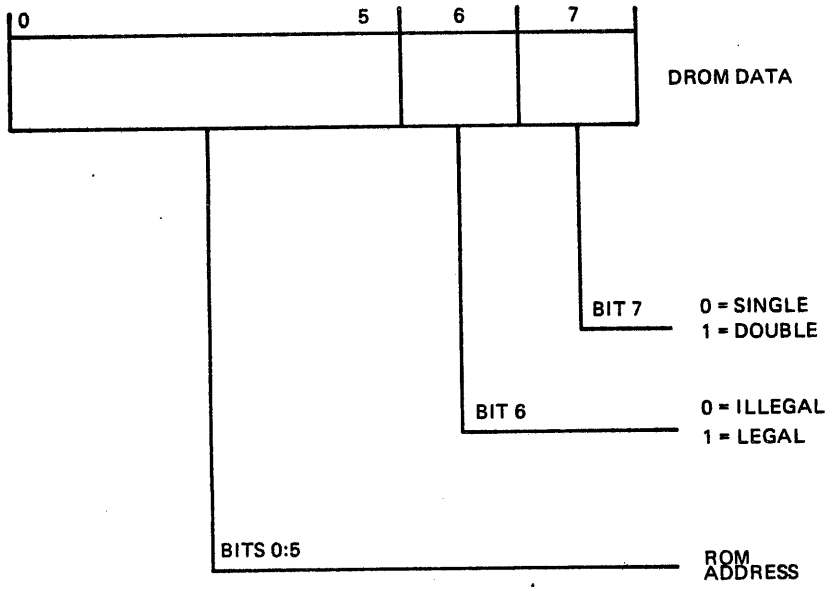


Figure 2-3. Decoder Read Only Memory (DROM) Data Word Format

Bits 0:5 form the ROM address. This set up imposes a restriction that an emulation sequence for any user level instruction must start on a four-word boundary. Three ROM words between two four-word boundary addresses can be utilized by branching there for a short sequence. For RX instructions, the address is made odd.

Bit 6 defines whether or not the op-code belongs to the floating-point instruction op-code map.

Bit 7 defines whether the FPP instruction is a single-precision or double-precision type.

The FPP has two versions of DROM. One DROM legalizes both single precision as well as double precision floating-point instructions (a total of 34 user level instructions). The other legalizes only the single precision floating-point instructions (17 user level instructions).

2.6.3 User Instruction Emulation

The FPP decodes all the op-codes until a floating-point instruction op-code is decoded. It then starts the emulation sequence. To emulate all the RX type of user level instructions and the FLR and FLDR instructions, the FPP waits for the second operand data from the host processor. When the data is made available, the emulation sequence resumes. In the case of the remaining RR type of user level instructions, the FPP has both the operands, and the emulation can begin without any waiting.

There are 17 emulation sequences for the 17 user level floating-point instructions. There is no distinction in the microcode between single and double precision floating point instructions; except where rounding is done, the single precision and the double precision user level instructions are emulated by the same code. Rounding is done for the single precision Add, Subtract, Multiply and Divide floating point instructions. However, because of the way DEOJ (E Field option) is defined, the rounding in a single precision floating point instruction does not slow down the execution times of double precision operations.

The instruction emulation terminators function as follows:

DEOJ:
1. Terminate the emulation of a double precision floating point instruction. If a single precision floating point instruction is being emulated, then continue micro-instruction execution.
2. For double precision floating point instructions, signal the host processor that the Condition Code is ready to be transferred.

EOJ: For single as well as double precision floating point instruction:
1. Terminate the emulation sequence.
2. Signal the host processor that the Condition Code or data are ready to be transferred.

When the instruction emulation is terminated, an automatic (hardware) branch is taken to the ROM address X'00' where DR is cleared.

2.6.4 Display Support

For power up, power down and floating point register display, the host processor needs the services of the FPP. The host processor communicates its requirement over the I/O Multiplexor Bus in the form of a user level instruction. In effect, the host processor loads an instruction in the FPP Instruction Register. The procedure is explained below.

In Power Up, the host processor loads X'7200' (LME) in the FPP IR and presents data for the single precision floating point registers. Then it loads X'7F00' (LMD) in the FPP IR and presents data for the double precision registers.

In Power Down, the host processor loads X'7100' (STME) in the FPP IR and receives data contained in the single precision registers. Then it loads X'7E00' (STMD) into the FPP IR and receives data contained in the double precision registers.

In order to get the data contained in the single precision register number N, the host processor loads X'6ONO' (STE) in the IR and then receives the data. In order to get the data contained in the double precision register number N, the host processor loads X'7ONO' (STD) in the IR and then receives the data.

The FPP unloads the data over the I/O Multiplexor Bus in response to the Acknowledge signal from the host processor.

CHAPTER 3
FUNCTIONAL SCHEMATIC ANALYSIS

3.1 INTRODUCTION

The material in this chapter is designed to help the technician understand the functional operation of the Floating Point Processor, so that the technician can perform maintenance and repair in a minimum of time. Prior to attempting to read the chapter material, the reader should read Chapter 1 Block Diagram Analysis and Chapter 2 Microcode Description. The material in this chapter assumes the reader has acquired the information contained in these two chapters.

The schematic diagram referenced herein is Functional Schematic 02-449D08, Sheets 1-22. This schematic diagram contains the information for both the FPP-A and FPP-B boards used in all three models of the Floating Point Processor. In the following circuit descriptions references are made to the schematic sheet numbers and to the coordinates on a sheet.

3.2 CLOCK CONTROL

The clock generator, shown on Sheet 18, employs a free running oscillator, which is adjusted by a variable resistor. The oscillator output (second waveform in Figure 3-1) is used as the clock input to three flip-flops arranged as a feedback delay counter. These flip-flops determine the duty cycle of all clocks. When decoded they provide the basic system clock (CLK1), a delayed clock (DCLK1), and a special narrower clock for the repeat counter logic (SCLK11). The counter is initialized by SCLR0 from the host processor.

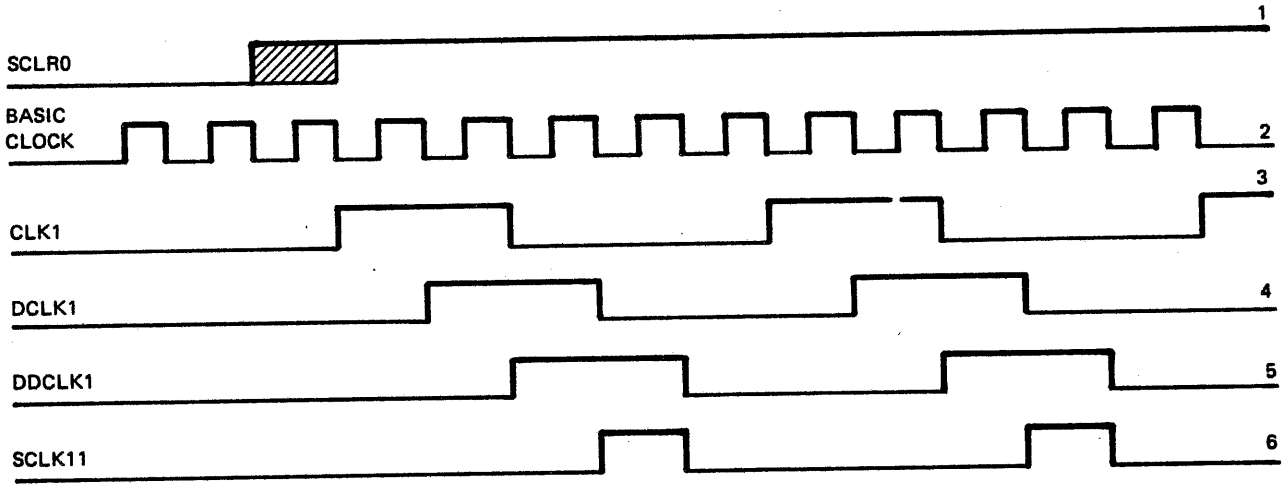


Figure 3-1. Control Timing

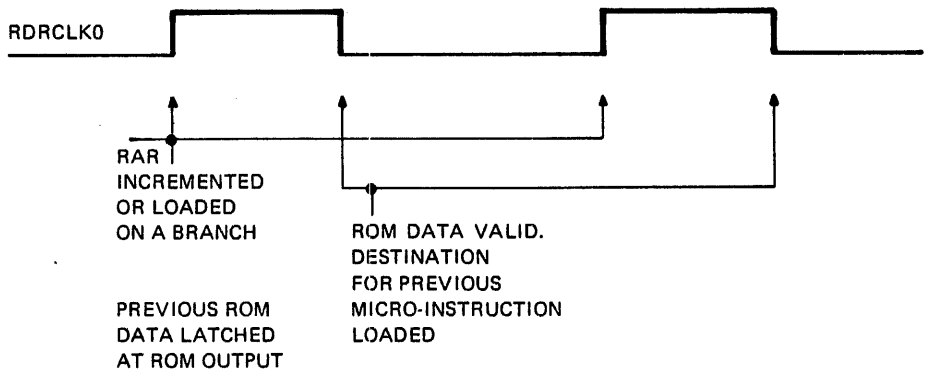


Figure 3-2. ROM Data Clock Timing

From CLK1 are derived three types of stoppable system clocks. The first of these is the ROM Data Clock (RDRCLK0). It is disabled by RDSTP0 when it is necessary to repeat a specific micro-instruction a number of times (refer to Figure 3-2). It is also stopped by TASTP0 when any of the following occur:

1. An I/O operation,
2. an external stop from the Test Aid, or
3. a skip clock is indicated by the current micro-instruction.

(In the last case the stop occurs for one clock period only).

Next we have four processor clocks which operate on different portions of the 64 bit data word as follows:

CPUCLKEX0	BITS	0:7
CPUCLKFR00	BITS	8:15
GCPUCLKFR00	BITS	16:31
CPUCLKFR10	BITS	32:63

These clocks occur when specified by the current micro-instruction (see MICRO-PROGRAM DESCRIPTION and Table 3-1), assuming no CPUSTP0 is present. The CPUSTP0 stops the processor clocks when either a branch is occurring or a TASTP0 occurs as explained previously.

TABLE 3-1 CPU CLOCKS

SPECIFIED OP FROM MICRO-INSTRUCTION	BITS AFFECTED
EX	0:7
* FR	8:63
LFR	32:63
LFR + MOD 816 + 8/16 HOST PROCESSOR	16:63

Finally, there are five DR clocks operating on different portions of the 64 bit Data Register as follows:

DRCLKEX0	BITS	0:7
DRCLKFR10	BITS	8:15
DRCLKFR20	BITS	16:31
DRCLKFR30	BITS	32:47
DRCLKFR40	BITS	48:63

These clocks occur when the DR is specified as a destination register in the microcode. The combinations of clocks according to the designated field are as follows:

SPECIFIED OP	CLOCKS	BITS AFFECTED
EX	DRCLKEX0	0:7
FR	DRCLKFR10,20,30,40	8:63
LFR	DRCLKRFR30,40	32:63

The reason there are more DR clocks than combinations in the microcode is to facilitate I/O operations in 16 bit groupings. (See the I/O description.)

3.3 DECODER READ ONLY MEMORY

The Decoder Read Only Memory (DROM) located at15C2 consists of two 256x4 ROM chips. The DROM is always decoding the eight-bit OP field of the IR. If a legal instruction is detected, output DECO61 will go active. Outputs DEC001:DEC051 then yeld a starting ROM address to be loaded into the ROM Address Register (RAR). If legal, then output DEC071 active indicates a double precision instruction, while DEC071 inactive indicates a single precision instruction.

3.4 ROM ADDRESS REGISTER

The ROM Address Register (RAR) located at 15K2 consists of two 4 bit counters yielding an 8-bit address. The RAR is loaded on the positive edge of RDRCLK0 when RARLD0 is active. If the RARLD0 is inactive then the counter will increment its present value. The RAR is initialized by RARCLR0 (21M5) to address X'00'. Two Quad 2-to-1 multiplexors (15G2) select between the DROM starting address and the ROM Data Register (RDR) output bits which provide branch addresses. Figure 3-3 shows the RAR timing diagram.

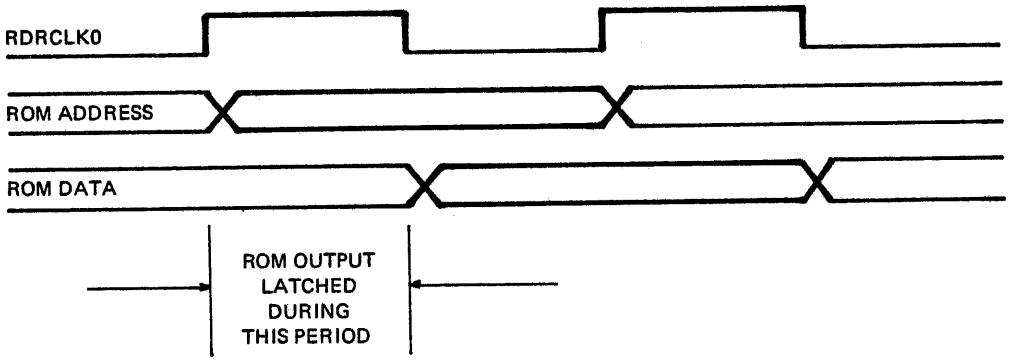


Figure 3-3. ROM Timing For The RAR

3.5 READ ONLY MEMORY (ROM) AND ROM DATA REGISTER (RDR)

Sheet 15 shows seven 256 x 4 bit ROM chips which yield 256 twenty-eight bit words. They are addressed by the 8-bit output of the RAR. The ROM outputs URD001:URD271 are then latched in the flip-flops shown on Sheet 16. This occurs on the positive edge of RDRCLK1.

3.6 DATA REGISTER AND DATA MULTIPLEXOR

The Data Register (DR) and Data Multiplexor, shown on sheets are comprised of sixteen, "Quad 2:1 Mux with storage" chips. The DR is loaded either from the S-Bus, (WAIT1 inactive) or from the I/O bus (WAIT1 active) on the trailing edge of the appropriate DR clock. Refer to Sheet 19 of the Functional Schematic for the DR clock logic. During I/O operations the DR is loaded 16-bits at a time and is controlled by the Load sequencer (17L5). WAIT1 active selects the I/O bus as source for the load which occurs on the appropriate DR clock depending on the position of the DR being operated on. Otherwise, the S bus is selected as source.

3.7 REPEAT COUNTER

The Repeat Counter is composed of two cascaded 4-bit counter chips (18E4). The Counter is initialized by CLRCNT0 upon command by the micro-code (21L2). Two "Quad 2:1 Multiplexors select between two sources for a load operation. One source is the S-Bus; the other source is a predetermined value for Multiply and Divide iterations. Since these are inverting multiplexers, the counter is actually loaded with a one's complement so that it can be incremented until a carry is produced. The Counter loads on the positive edge of CNTCLK when RD170 is active and increments on the positive edge of CNTCLK when RD001 is active and RD170 is inactive. CNTCLK consists of the basic system clock CLK1, ORed with SCLK11 when CNTBY21 (2157) is active. G5R131 (18R7) active indicates that for single precision the counter contains a number greater than 6 and for double precision greater than 13.

3.8 INSTRUCTION REGISTER

The Instruction Register (IR) is shown on Sheet 14. IRMSEL is a logic low except for display support and power up-power down routines. When low, it causes the Memory Data bus to be selected as source for the IR. When high, the I/O bus is selected. The IR is loaded on the positive edge of LDIR0. The 4-bit YD address field can be incremented when YDINC1 (20M5) is active and an RD clock occurs. YDCLK1 (19F7) is a logic OR of LDIR0 and RDRCLK1. The double inversion of LDIR0 to the YD register delays the loss of LDIR0 as a logic low load signal while the positive edge of LDIR0 is clocking the register.

3.9 FLAGS

See sheet 20 and refer to the micro-program description of flag operations.

3.10 CARRY LOOKAHEAD LOGIC

Four carry lookahead chips (3M2, 4M2, 5M2, 6M2) organize the 64 bit data word into 16-bit groupings. Then a fifth carry lookahead chip (12M1) coordinates the information they develop. The logic in the upper left corner of sheet 3 allows bits 0:7 to participate with the rest of the data word for 64-bit (S4BT1 active) operations. If just an exponent operation (EX) is specified then the two uppermost processor slices will ripple the carry-from bits 4:7 to bits 0:3 and not make use of the carry lookahead logic. FKCRY1 provides an active high to the least significant bit of the portion of the data word being operated on, for all micro-code subtract operations.

3.11 YD and YS MULTIPLEXOR

The YD and YS Multiplexor is shown at 3C8. In order for the micro-code word chart to be correct in its source fields for the processor chips, as specified by RD bits 9, 10 and 11, it is necessary to place the YD address on the YS inputs to the bit slices when RD090 is active. This is also done when MPY0 is active, but only for timing considerations.

3.12 SIGN LOGIC

BG2 (21R8) is the latched result sign for user add or subtract instructions as determined by any of the ALB, AGB, or ALBAGB commands from the micro-code.

SNMX (22J5) contains one of the following operand signs selected by the micro-code:

ASN1	Sign of first operand (YD)
BSN1	Sign of second operand (YS or data from host processor)
AXORB1	Exclusive-OR of ASN1 and BSN1 for Multiply and Divide Instructions
BG2	Result sign for Add and Subtract Instructions

For all four sources, an additional inversion may take place if specified by the microcode. DRSN (20L5) allows the sign bit of the operand residing in the DR to participate in the current operation when specified by the microcode.

3.13 BRANCH LOGIC

The Branch Logic is shown on Sheet 21. The 12 input gate at 21E2 ORs together all allowable combinations of branch conditions, whether those conditions are true or false. Then if BT0 or BF0 is active and the appropriate condition is satisfied RARLD0 goes active, and a processor stop is generated. Then on the next RD clock the RAR can be loaded with the address specified in the branch microinstruction. BNCH1 goes active when a branch instruction is encountered regardless of whether the specified condition is present or not.

3.14 FORCED BITS

In several cases certain RDR bits are modified by the hardware before reaching selected destinations. Their mnemonics are then written as FRDXX1. They are as follows:

RD071:FRD071
RD081:FRD081

These two RD bits are complemented as specified under the TAKOP description under Extended Field Options in the microprogram description.

RD091:FRD091
RD101:FRD101

These two RD bits are complemented as specified under the DIV algorithm in the microprogram description.

RD151:FRD151

This bit is disabled to a logic low when CEQ1 and CNTBY21 are active. In effect it causes all equalize shifts after the first one to be by two hexadecimal digits. The first shift will also be by two hexadecimal digits if CNTBY21 is active then. If inactive, it will automatically become active for any shifts after the first.

3.15 D-BUS SHIFTER

The D-Bus Shifter is comprised of 32 'Dual 2:1 Multiplexor' chips. The Shifter is steered by RD141 and RD151 for the Exponent field bits 0:7, and by RD141A and FRD151A for the Fraction field bits 8:63. Bits 8:63 are disabled to a logic low when QGX (22H8) is at logic high.

The Exponent field bits select among the following sources:

1. Eight Counter Output bits,
2. Data Register bits 0:7,
3. An 8-bit Immediate Data source derived from a group of five encoded RD bits, and
4. SNMX for Bit 0 and a logic low for bits 1:7.

The fraction field Bits 8:63 always selects the Data Register but either a no shift, a 1 hexadecimal digit left shift, or a 1 or 2 hexadecimal digit right shift.

ORBT11 active allows a one to enter D bus bit 11 when a right shift by one hexadecimal digit is specified.

3.16 I/O CONTROL

3.16.1 Input for User Instruction

Whenever FINR0 from the host processor goes active, an LDIR0 is generated which loads the FPP instruction register from the Memory Data bus. If the DROM decodes the instruction as a legal one, and upon receipt of FDEC10 from the host processor, and if IDLE1 is active, then a flip-flop at (17K2) is set asynchronously. When the next falling edge of CLK1 occurs the FSYN1 flip-flop is set (17K3). On the rising edge of DCLK1 the flip-flop at (17K2) will be cleared. On the falling edge of CLK1 the FSYN1 flip-flop and the IDLE1 (17B8) flip-flop will be cleared. The current operation is now synchronized to the FPP clock.

With FSYN1 and IDLE1 active, SRAR (21K3) steers the RAR multiplexor so that the DROM starting address can be loaded into the RAR. At this point RARLD0 also indicates a load rather than an increment to the RAR.

At the time FSYN1 was set, TASTP0 went inactive, and the next CLK1 will be allowed to propagate through the system clocks. This clock will cause the RAR to be loaded with the starting address for the current user instruction.

3.16.2 Data Input From Host Processor

When RXWAIT1 is active and RD091 is active (indicating DR as a destination), and RXINST1 active (indicating an RX instruction is being emulated), and FSYN0 is active, then TASTP0 is made active and the clocks are stopped until all data is recieved. The WAIT1 (19M5) also goes active now and steers the DR input multiplexor to the I/O bus. At the time the instruction was being received and FSYN1 went inactive a 4-bit shift register (17L5) was loaded with a one in its least significant position causing BI001 to go active. Also a 4-bit counter (17L7) was loaded with a 1100 or a 1110. The first case is for all double precision instructions except FLOAT. The second case is for all single precision instructions and FLOAT.

When LDREG0 is active, two one-shots (17D2) form a pulse that causes CIODR1 to go active enabling the DR I/O clocks. Since BI001 is active, the I/O bus is loaded into DR bits 0:15. The LDREG0 pulse also increments the counter and shifts the shift register by one bit causing BIO11 to go active readying DR bits 16:31 for a load. This continues until all data is loaded, at which point the carry out of the counter causes the flip-flop at 17K2 to set. Then FSYN1 is active on the next falling edge of CLK1. The circuit is now resynchronized and ready to resume FPP processing.

3.16.3 Data Output to Host Processor

When RXWAIT1 is active and RD090 is active (17B4) (indicating DR as a source) then FWAIT0 goes inactive on the next RD clock. This causes TASTP0 to go active (19M5) and the clocks are stopped until all data is transmitted to the host processor. The load sequencer comprised of the 4-bit counter and 4-bit shift register is again (as for data in) used to select which 16-bit group will be sent to the host processor. Each RACK0 received from the host causes GDAT1 to go active enabling the output drivers to the I/O bus. The RACK0 will also increment the counter and shift the shift register until a carry is produced by the counter. When all data are sent out, resynchronization will occur as in 'Data In' and the clocks will be allowed to restart.

3.16.4 End of Job

If DEOJ1 and DECO71 are active, or if EOJ0, is active then END1 goes active (21L5). This sets a flip flop on the next RD clock (17BG) and clears the RAR to X'00'. At the same time if FUCC1 is active (indicating that the condition code is to be returned to the host processor) another flip flop is set (17DG). This causes FWAIT0 to go inactive and creates a clock stop (19HG). The condition code is returned in the same way as data (see Data Out description).

The CCMSEL (17ES) active high allows the I/O output drivers to select the condition code instead of the Data Register. When the clock stop is removed, the IDLE1 flip flop is set on the next RD clock. This RD clock increments the RAR to X'01'. At this time the clocks are stopped again until a new instruction sequence is begun.

3.16.5 Display Support and Power Up-Power Down Routines

Read the microprogram description of these events first.

When the LDREG0 is active it causes IRMSEL (17C2) to be active high causing the I/O Bus to be input for an IR load. In this case IDLE1 is still active due to no instruction being received by the IR. Therefore an LDIR0 is generated which loads the IR with the I/O bus. Data is then handled in the normal manner.

CHAPTER 4
INSTALLATION PROCEDURES

4.1 INTRODUCTION

This chapter provides the necessary information for installing the following listed Floating Point Processor units

Model 02-449 and 02-450 for the INTERDATA Model 8/16 Computer
Model 02-451 and 02-528 for the INTERDATA Model 7/32 CII Computer.

The Models 02-449 and 02-451 units handle both single and double precision floating point operations. The Model 02-450 and 02-528 handle single precision floating point operations only.

4.2 UNPACKING

When installed at the factory, no unpacking instructions are provided for the floating point processor because the system is ready for use. If the package is purchased separately, it should be unpacked and inspected for any damage.

The single and double precision, 02-449, package consists of the following items:

1 each	FPP-A 35-632 F03
1 each	FPP-B 35-633 F01
1 each	50 PIN RIBBON CABLE 17-191F01
1 each	34 PIN RIBBON CABLE 17-317
1 each	FPP Maintenance Manual 29-568
1 each	Series 16 Floating Point Test Package 06-205

The single precision only, 02-450, package consists of the following items:

1 each	FPP-A 35-632 F01
1 each	FPP-B 35-633 F02
1 each	50 PIN RIBBON CABLE 17-191 F01
1 each	34 PIN RIBBON CABLE 17-317
1 each	FPP Maintenance Manual 29-568
1 each	Series 16 Floating Point Test Package 06-205

The Floating point processor, 02-451, package consists of the following items:

1 each	FPP-A 35-632 F02
1 each	FPP-A 35-633 F01
1 each	50 PIN RIBBON CABLE 17-191F01
1 each	34 PIN RIBBON CABLE 17-317
1 each	FPP Maintenance Manual 29-568
1 each	Series 32 Floating Point Test Package 06-193

The single precision only, 02-528, package consists of the following items:

1 each	FPP-A 35-632F04
1 each	FPP-B 35-633F02
1 each	50 PIN RIBBON CABLE 17-191F01
1 each	34 PIN RIBBON CABLE 17-317
1 each	FPP Maintenance Manual 29-568
1 each	Series 32 Floating Point Test Package 06-193

4.3 INSTALLATION IN THE 8/16 COMPUTER

4.3.1 Physical Location

The FPP Models 02-449 and 02-450 interface to the I/O Multiplexor bus and the Memory Data bus of the Model 8/16 Computer. Figure 4-1 shows the physical configuration of the computer with the FPP-A board located in slot 4 and the FPP-B board installed in slot 3. The two ribbon cables, 17-191F01 and 17-317 are installed between the FPP-A and FPP-B boards.

Variations in the computer configuration can occur since both half-boards in slot 6 are optional, and the number of memories or I/O boards in slots 2, 1 and 0 may vary with the desired installation.

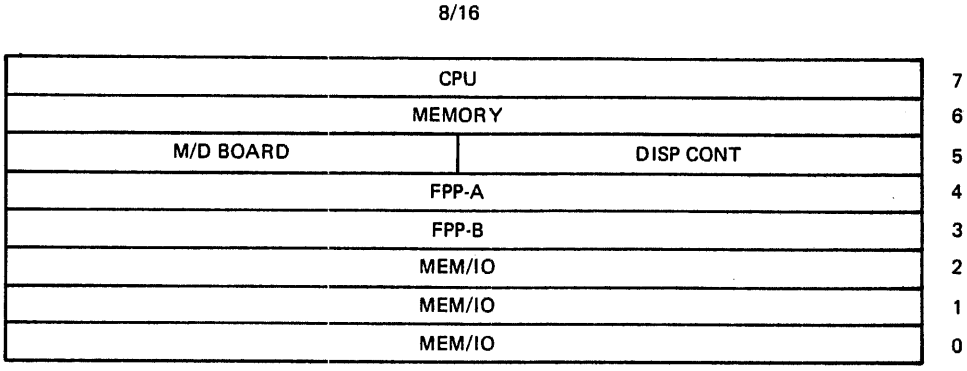


Figure 4-1. Model 8/16 Computer Physical Configuration Showing The Floating Point Processor Locations

4.3.2 I/O Interrupt Strapping

The Floating Point Processor must have the highest I/O interrupt priority. The Floating Point Processor does not generate an interrupt, however, the looped jumper on RACK0/TACK0 must be removed between Pins 122 and 222 of Connector 1 on slot 4 (FPP-A board). The FPP unit will receive and transmit RACK0/TACK0 and transmit SYN0 when transferring data between the unit and the host processor. When the FPP unit is not performing any floating point operations the unit will receive and transmit RACK0/TACK0.

4.3.3 Strapping the FPP Boards

Strapping is required on FPP-A to denote the difference between the type of host processor supporting the FPP unit (8/16 or 7/32 CII). The following strap must be added for the appropriate typ e of processor.

8/16 – strap A TO B
7/32 CII – strap B TO C

Refer to 02-449D08 schematic sheet 19 for locations.

4.3.4 Processor Board (35-604) F05 or F06 Strapping

The 8/16 processor contains a Decoder Read Only Memory (DROM). There are four different functional variations that are used when the FPP unit is installed. Refer to Table 4-1 for the correct DROM functional variation number. When installing the Double Precision Floating Point Option remove the jumper between M and N on the 35-604F06 Processor board. (Refer to sheet 14 of the functional schematics (01-094D08) for location.)

There are five additional wires that must be added to the processor backpanel when the Floating Point Processor is installed. The following four wires must be added between the host processor in slot 7 and the FPP-A in slot 4.

1. LIRH0 – 117-1 TO 124-1
2. FDEC10 – 118-1 TO 125-1
3. LDREG0 – 128-1 TO 134-0
4. M/DO – 228-1 TO 234-0

Add a wire between 127-0 and 241-0 at slot 7.

This indicates to the processor that Floating Point is present.

TABLE 4-1. DROM FUNCTIONAL VARIATIONS FOR 19-186

INSTRUCTIONS EQUIPPED	FUNCTIONAL VARIATION NUMBER
BASIC INSTRUCTION SET	F27
BASIC, + MULTIPLY AND DIVIDE	F28
BASIC + MULTIPLY AND DIVIDE + SINGLE PRECISION FLOATING POINT	F29
BASIC + MULTIPLY AND DIVIDE + SINGLE AND DOUBLE PRECISION FLOATING POINT	F30

4.3.5 Installation Checks

The following checks should be made to ensure proper installation of the Floating Point Processor in the 8/16 Computer.

1. Check that FPP-A and FPP-B are installed in the correct slots and are fully seated.
2. Check to ensure that the two ribbon cables are installed and correctly seated.
3. Insure that all wiring and strap options are properly installed.
4. Perform the final installation check by running the series 16 Floating Point Test (06-205) according to the test program description.

4.4 INSTALLATION IN THE 7/32 CII COMPUTER

4.4.1 Physical Location

The FPP unit (Model 451and 528) interfaces to the I/O Multiplexor bus and the Memory Data bus of the Model 7/32 CII Computer. Figure 4-2 shows the physical configuration of the computer with 256KB of memory, that is, eight 32KB memory modules. Regardless of the number of memory modules, the FPP boards are installed into the first two empty slots of the card file after the memory modules. The FPP-A board goes into the top slot and the FPP-B board is inserted into the following empty slot. The ribbon cables 17-191F01 and 17-317 are installed between the FPP-A and FPP-B boards.

When the computer has eight memory modules as shown in Figure 4-2, the Multiplexor and Memory Data busses must be extended to interface with the FPP. Therefore, the busses are wired between slot 4 and slot 3 of the lower half of the processor card file.

4.4.2 I/O Interrupt Strapping

The FPP must have the highest I/O Interrupt priority. The Floating Point Processor does not generate an interrupt, however, the looped jumper on RACK0/TACK0 must be removed between pins 122 and 222 of Connector 1 on the FPP-A slot. The FPP unit will receive and transmit RACK0/TACK0 and transmit SYN0 when transferring data between the unit and the host processor. When the FPP unit is not performing any floating point operations the unit will receive and transmit RACK0/TACK0.

4.4.3 Strapping the FPP Boards

Strapping is required on FPP-A to denote the difference between the type of host processor supporting the FPP unit (7/32 CII or 8/16). The following strap must be added for the appropriate type of processor:

8/16 – strap A TO B
7/32 CII – strap B TO C

Refer to 02-449D08 schematic sheet 19 for locations.

CPU-A	7
CPU-B	6
CPU-C	5
MAC	4
MEM/IO	3
MEM/IO	2
MEM/IO	1
MEM/IO	0
MEM/IO	7
MEM/IO	6
MEM/IO	5
MEM/IO	4
FPP-A OR I/O	3
FPP-B OR I/O	2
I/O	1
I/O	0

Figure 4-2. Model 7/16 CII Computer Physical Configuration Showing The Floating Point Processor Location

4.4.4 Processor CPU-A Board (35-624) Strapping

The micro-code detects the presence of the FPP unit by testing HWA1. If HWA1 is a logic ONE, the micro-code assumes that the FPP unit is present. When installing the Floating Point Processor package HWA1 must be strapped to the ONE state. To accomplish this, the following must be done:

1. Remove strap E4 to E5
2. Strap E4 to E3

4.4.5 Processor CPU-B Board (35-625F03, F04) Strapping

When the Floating Point Processor is installed into the 7/32 CII, the CPU-B board, 35-625, must be at the F03 or F04 functional variation level. The 35-625F03 is used for single and double precision instructions. The 35-625F04 is used for single precision only.

The CPU-B Processor board contains a Decoder Read ONLY Memory (DROM) that must be strapped to allow execution of the single and double precision or single precision only user instructions. Refer to Figure 4-3 for the location of these straps and to Table 4-2 for the type of strapping to be installed.

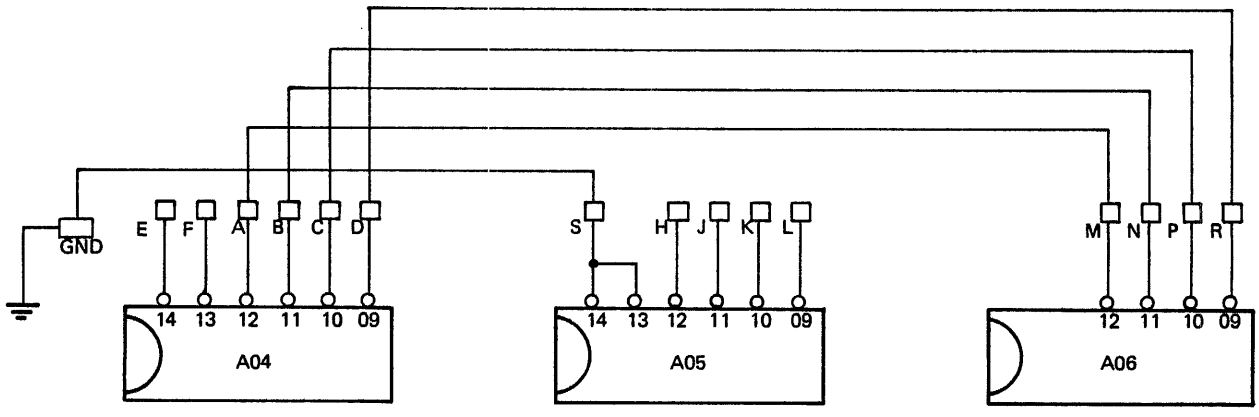


Figure 4-3 DROM Location

TABLE 4-2. DROM STRAPPING

INSTRUCTIONS EQUIPPED	DROM STRAPPING
BASIC SET	E TO H
BASIC SET AND COMMUNICATION	E TO H, L
BASIC SET AND FLOATING POINT	E TO H, K
BASIC SET AND FLOATING POINT AND COMMUNICATION	E TO H, L, K
BASIC SET AND SINGLE PRECISION ONLY FPP	E TO H, J
BASIC SET AND SINGLE PRECISION ONLY FPP AND COMMUNICATION	E TO H, L, J

4.4.6 Processor Card File

The following four wires must be added to the Processor backpanel when the Floating Point Processor is installed. These wires are from the CPU-A board to the FPP-A board.

1. FINR0: 234-1 Slot 7 TO 124-1 OF FPP-A Slot
2. FDEC10: 238-1 Slot 7 TO 125-1 OF FPP-A Slot
3. BCNTO: 218-0 Slot 7 TO 134-0 OF FPP-A Slot
4. BADR0: 130-0 Slot 7 TO 234-0 OF FPP-A Slot

4.4.7 Installation Checks

The following checks should be made to ensure proper installation of the Floating Point Processor in the 7/32 CII Computer.

1. Check that FPP-A and FPP-B are installed in the correct slots and are fully seated.
2. Insure that the two ribbon cables are installed and correctly seated.
3. Insure that all wiring and strap options are properly installed.
4. Perform the final installation check by running the series 32 Floating Point Test (06-193) according to the directions supplied.

APPENDIX 1
FLOATING POINT NOTATION

1. INTRODUCTION

Floating point is not a numbering system, but rather a means of representing quantity in any numbering system. This representation takes the form of a series of digits multiplied by a base number (usually the base of the numbering system used) raised to some power. For example, the decimal number 4567 can be represented in many forms. The following examples are all equal to 4567.

4567×10^0
456.7×10^1
45.67×10^2
4.567×10^3
$.4567 \times 10^4$
$.04567 \times 10^5$

It can be readily observed in the above example that the decimal point has in fact moved. Hence, we have a floating point number that defines the precision of the entire quantity. In scientific notation, the significant digits are usually fractional and will be referred to for the remainder of this discussion as the fraction. The power to which the base number is raised will be called the exponent. For example, in the number $.7642 \times 10^3$, .7642 is the fraction and 3 is the exponent. Both the exponent and the fraction may have a + or - sign. If, for example, the floating point notation is represented in the format (sign) (exponent) (fraction) then the following numbers are represented as:

		sign	exponent	fraction
$.7642 \times 10^3$	as	+	+3	7642
$-.1234 \times 10^6$	as	-	+6	1234
$.0590 \times 10^{-2}$	as	+	-2	0590
$-.9207 \times 10^{-9}$	as	-	-9	9207

The convenience with which extremely large or small numbers can be compactly expressed in floating point, makes it ideally applicable to situations, such as scientific computation, where such magnitudes are frequently used. This compactness is illustrated in the following examples:

+	+15	630
-	-12	123

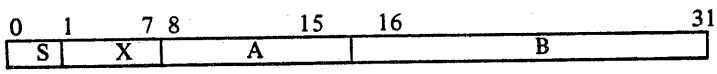
$= .630 \times 10^{15} = 630{,}000{,}000{,}000{,}000$
$= -.123 \times 10^{-12} = -.000\ 000\ 000\ 000\ 123$

Thus far, this discussion has used decimal examples with apparently no restriction on magnitude, or physical size. When floating point is implemented in the 8/16 or 7/32 CII Computer for example, the decimal numbering system is replaced by the hexadecimal system and a limit is imposed on physical size and, indirectly, on magnitude.

2. FLOATING POINT DATA WORD

A floating point quantity in this format is represented in 32 bits, and consists of an exponent and a signed fraction. The magnitude expressed by this quantity is the product of the fraction and the base number 16, raised to the power of the exponent. The seven-bit exponent is expressed in excess $64_{(10)}$ binary notation; the 24-bit fraction is expressed as a hexadecimal number (six digits of precision) having a radix point to the left of the high order digit.

Each floating point value requires two halfwords. The floating point format is:



where S = Sign of the fraction
AB = Fraction
X = Exponent, in excess $64_{(10)}$

The EXPONENT field, in excess 64 notation, represents the power of 16 the fraction is multiplied by. For example, if the fraction is to be multiplied by 16^1, the EXPONENT field would appear as follows:

0	1	2	3	4	5	6	7
S	1	0	0	0	0	0	1

or hexadecimal 41. Subtracting 64 decimal, which is 40 hexadecimal, from this number, to get hexadecimal 01.

41 - 40 = 01

If the fraction is to be multiplied by 16^{-1}, the Exponent field would appear as follows:

0	1	2	3	4	5	6	7
S	0	1	1	1	1	1	1

or hexadecimal 3F. Subtracting hexadecimal 40 from this gives -01.

3F - 40 = -01

Thus both positive and negative exponents can be represented. Exponent range is summarized below.

	EXCESS 40_{16}	HEXA-DECIMAL	DECIMAL
POSITIVE EXPONENT	40 to 7F	00 to 3F	00 to 63
NEGATIVE EXPONENT	3F to 00	-01 to -40	-01 to -64

The FRACTION field consists of six hexadecimal digits as shown below:

0	1 – 7	8 – 11	12 – 15	16 – 19	20 – 23	24 – 27	28 – 31
S	X	.F1	F2	F3	F4	F5	F6

The value of the floating point fraction can be expressed as:

$$\text{sign } (F1 \cdot 16^{-1} + F^2 \cdot 16^{-2} + F^3 \cdot 16^{-3} \ldots\ldots + F^6 \cdot 16^{-6})$$

Sample values are shown in Table 1 where the value of the floating point number is represented as:

$$\text{sign } \left[(F_1 \cdot 16^{-1} + F_2 \cdot 16^{-2} \text{ — } + F_6 \cdot 16^{-16}) \times 16^{x-64}\right]$$

where sign can be + or -; and x is the exponent converted to decimal.

A normalized floating point number has a non-zero, high-order hexadecimal fraction digit (F_1). If one or more high-order fraction digits (F_1F_2.....) are zero, the number is said to be unnormalized.

The range of magnitude (M) of a normalized floating point number is:

$$16^{-65} \leqslant M \leqslant (1 - 16^{-6}) \cdot 16^{63}$$

or approximately

$$5.4 \cdot 10^{-79} \leqslant M \leqslant 7.2 \cdot 10^{75}$$

TABLE 1. SAMPLE FLOATING POINT VALUES

DATA IN HEXADECIMAL	VALUE IN HEXADECIMAL
0000 0000	0
4110 0000	1.0
C110 0000	-1.0
4123 0000	2.3
3E45 6000	.00456
BD89 ABCD	-.00089ABCD
FFFF FFFF	* $-(1-16^{-6}) .16^{63}$
8010 0000	* -16^{-65}

*Note that this notation implies a hexadecimal fraction and a decimal exponent of the base 16.

All floating point numbers are assumed to be normalized prior to their use as operands. No prenormalization is performed, all results are post normalized. The floating point Load instruction will normalize unnormalized floating point numbers. Exponent Overflow is defined as a resultant exponent greater than +63. Exponent Underflow is defined as a resultant exponent less than -64. Either case will set Overflow Flag. If Overflow, the exponent and fraction of the result are set to all ones, the largest possible magnitude and therefore the closest possible answer.

The floating point value in which all data bits are zero is called true zero. A true zero may arise as the result of an arithmetic operation that caused an exponent Underflow, or when a result fraction becomes zero due to lack of significance. In general, zero values participate as normal numbers in all arithmetic operations.

There are a few terms in floating point to be familiar with, the first is normalization. This means that the hexadecimal digit in the F1 field is non zero. Since all number are expressed as fractions the number will have probably been shifted left and the exponent is changed to reflect the number of shifts (to keep up with the "Floating Radix Point"). For example: If, after conversion from decimal to hexadecimal floating point, the result was 4005, the zero cannot exist therefore the fraction must be shifted left one place so the number is 4050. The number 40 is the exponent value so bits 0:15 would become 3F50 and this is the number. Once the F1 field is non zero the number is normalized.

Another is Excess 64 notation. The exponent with no shift is a $64_{(10)} = 40_{(16)}$. A hexadecimal 40 in bits 0:7 indicates 16^0, 41 would be 16^1 and 3F would be 16^{-1}. The exponent is acquired by subtracting 40 from the exponent, i.e., if the exponent is 44 then 44 - 40 = 16^4 or 30 - 40 = -10 = 16^{-16}. Anything greater than hexadecimal 40 is a positive exponent and anything less than hexadecimal 40 is a negative exponent.

The third is compare and equalize: This step must be done before an addition or subtraction. It is the same in power of 10. For example:

$$+\begin{array}{l} 2.5 \times 10^1 \\ .25 \times 10^2 \end{array}$$

These two numbers cannot be added because of the unequal exponents, therefore, make the $.25 \times 10^2$ @ 2.5×10^1 and this gives:

$$+\begin{array}{l} 2.5 \times 10^1 \\ 2.5 \times 10^1 \end{array}$$

5.0×10^1 or $50_{(10)}$

This exponent equalization must be done before adding two floating point numbers.

Example:

```
  43 120000
+ 41 120000
```

Cannot be added because the exponents are not equal.

Take the 4112, shift the fraction hexadecimally twice to the right and make it 43001200. The numbers would then be:

```
  4312 0000
+ 4300 1200
-----------
  4312 1200
```

The number 4312 1200 would have to be converted back to decimal and in order to do that the radix part would be shifted right 3 places making the exponent 6 - (121.2) in hexadecimal = 289.0124 in decimal. For exponent values see Tables 2 and 3.

TABLE 2 EXPONENT VALUES

HEX	VALUE	HEX	VALUE
7F	16^{63}	5F	16^{31}
7E	16^{62}	5E	16^{30}
7D	16^{61}	5D	16^{29}
7C	16^{60}	5C	16^{28}
7B	16^{59}	5B	16^{27}
7A	16^{58}	5A	16^{26}
79	16^{57}	59	16^{25}
78	16^{56}	58	16^{24}
77	16^{55}	57	16^{23}
76	16^{54}	56	16^{22}
75	16^{53}	55	16^{21}
74	16^{52}	54	16^{20}
73	16^{51}	53	16^{19}
72	16^{50}	52	16^{18}
71	16^{49}	51	16^{17}
70	16^{48}	50	16^{16}
6F	16^{47}	4F	16^{15}
6E	16^{46}	4E	16^{14}
6D	16^{45}	4D	16^{13}
6C	16^{44}	4C	16^{12}
6B	16^{43}	4B	16^{11}
6A	16^{42}	4A	16^{10}
69	16^{41}	49	16^{9}
68	16^{40}	48	16^{8}
67	16^{39}	47	16^{7}
66	16^{38}	46	16^{6}
65	16^{37}	45	16^{5}
64	16^{36}	44	16^{4}
63	16^{35}	43	16^{3}
62	16^{34}	42	16^{2}
61	16^{33}	41	16^{1}
60	16^{32}	40	16^{0}

TABLE 3 EXPONENT VALUES

HEX	VALUE	HEX	VALUE
3F	16^{-1}	1F	16^{-33}
3E	16^{-2}	1E	16^{-34}
3D	16^{-3}	1D	16^{-35}
3C	16^{-4}	1C	16^{-36}
3B	16^{-5}	1B	16^{-37}
3A	16^{-6}	1A	16^{-38}
39	16^{-7}	19	16^{-39}
38	16^{-8}	18	16^{-40}
37	16^{-9}	17	16^{-41}
36	16^{-10}	16	16^{-42}
35	16^{-11}	15	16^{-43}
34	16^{-12}	14	16^{-44}
33	16^{-13}	13	16^{-45}
32	16^{-14}	12	16^{-46}
31	16^{-15}	11	16^{-47}
30	16^{-16}	10	16^{-48}
2F	16^{-17}	0F	16^{-49}
2E	16^{-18}	0E	16^{-50}
2D	16^{-19}	0D	16^{-51}
2C	16^{-20}	0C	16^{-52}
2B	16^{-21}	0B	16^{-53}
2A	16^{-22}	0A	16^{-54}
29	16^{-23}	09	16^{-55}
28	16^{-24}	08	16^{-56}
27	16^{-25}	07	16^{-57}
26	16^{-26}	06	16^{-58}
25	16^{-27}	05	16^{-59}
24	16^{-28}	04	16^{-60}
23	16^{-29}	03	16^{-61}
22	16^{-30}	02	16^{-62}
21	16^{-31}	01	16^{-63}
20	16^{-32}	00	16^{-64}

APPENDIX 2
FLOATING POINT PROCESSOR MNEMONICS

ALICE1	Test Aid Stop
ASN1	Arithemtic sign of one operand flip flop
AXORB1	Exclusive or of ASN1 and BSN1
BADR0	Box Address Line from 7/32 CII
BCNT0	Box Control Line from 7/32 CII
BF0	Branch on False
BG2	Add/Subtract Sign Bit flip flop Output
BI001 BI031	Enable different 16 bit bytes for I/O
BNCH1	True if either a BT0 or BF0 was detected
BOZ1	Active if RD231 RD271 are all zero
BSN1	Arithmetic sign of one operand flip flop
BT0	Branch on True
CCM001:CCM031	Contain either data or condition code (see CCM SEL)
CIODR1	Enables loading of DR by I/O
CLK0/1	Main FPP clock Non stoppable
CLRCNT0	Clears the counter to 0
CMPRD81	Inverts RD81 in certain cases
CNI1:CNI4	Carry In to successive 16 bit bytes of the data word
CNTCLK	Counter Clock
CNTREQ10	Active when counter contains a 1
CNTREQ20	Active when counter contains a 2
CNTBY21	Indicates whether first equalize will be by 1 or 2 hexadecimal digits
CNT010	Counter Output Bit
CNT020	Counter Output Bit
CNT040	Counter Output Bit
CNT080	Counter Output Bit
CNT160	Counter Output Bit
CNT320	Counter Output Bit
CNT640	Counter Output Bit
CNT1280	Counter Output Bit
CN041	Connect Carry Lookahead logic between boards
CN56	Carry out of fraction field

CN64	Carry out of entire data field
CPUCLKEX0	Clock for Exponent field of ALU Bits 0:7
CPUCLKFR00	Clock for Partial fraction field of ALU Bits 8:31
CPUCLKFR10	Clock for Partial fraction field of ALU Bits 32:63
CPU STP0	ALU Stop
DCLK0/1	Delayed clock
DEC061	Active if a legal floating point instruction is detected
DEC070/1	Indicates single or double precision instruction
DEOJ1	Double precision end of job
DIV0	FPP Command Divide instruction
DI001:DI631	External inputs to ALU
DRCLKEX0	Clock for Exponent field of Data Register Bits 0:7
DRCLKFR10	Clock for Partial fraction field of Data Register Bits 8:15
DRC LKFR20	Clock for Partial fraction field of Data Register Bits 16:31
DRCLKFR30	Clock for Partial fraction field of Data Register Bits 32:47
DRCLKFR40	Clock for Partial fraction field of Data Register Bits 48:63
DROM000/1:DROM070/1	Instruction Register Output Bits
DRSTP0	Data Register Stop - active when a branch or an Immediate instruction is specified
DRSN	Gated Bit 0 of Data Register
DR001:DR631	Data Register Bits
D000/1:D150/1	I/O Bus Bits
EG11	E field group 1
EG21	E field group 2
EG31	E field group 3
EG41	E field group 4
END1	Or of EOJO and DEOJ1
EOJ0	End of Job
EX1	Indicates and Exponent operation
FDEC10	Decode one flip flop
FINR0	Instruction Read from Host processor
FKCRY1	Inverts the active state of Carry In for ALU subtract operations
FRCRY0	Exclusive OR of FRCRY0 and CN56

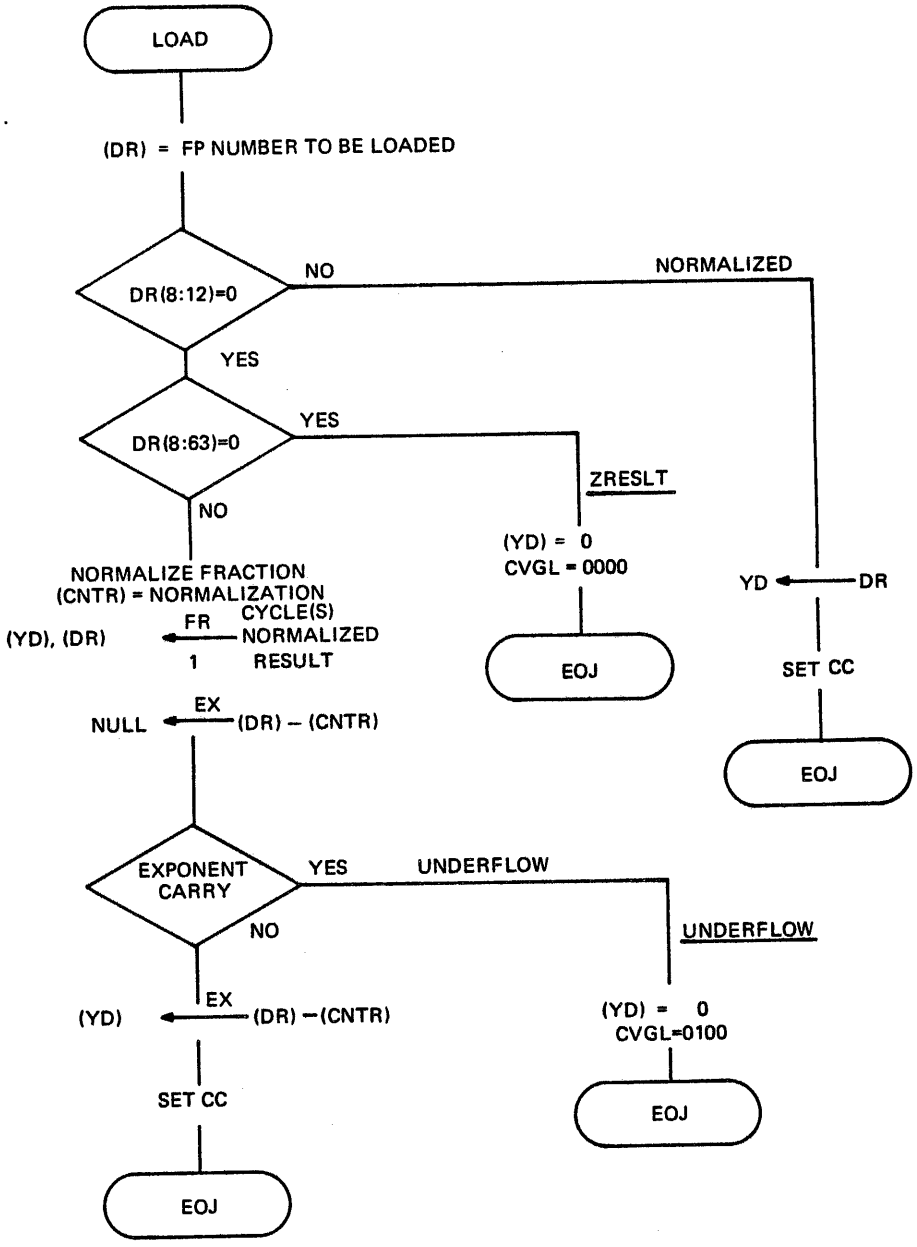
FRD071	Switches between ALU add and subtract instructions for COMMAND DIVIDE
FRD081	Switches between ALU add and subtract instructions for COMMAND DIVIDE
FRD091	Switches between "0" and the RAM register stack as a source for COMMAND MULTIPLY
FRD101	Switches between "0" and the RAM register stack as a source for COMMAND MULTIPLY
FRD150	Shift right by one or by two hexadecimal digits i n equalize
FRD151A	Buffered and inverted FRD150
FSYN0/1	Synchronoized SYNC flip flop
FUCC1	Unload Condition Code flip flop
FWAIT0	Wait flip flop
FYS01:FYS21	Outputs of MUX that selects YD or YS address
GCPUCLKFR00	Clock for Instruction bits 16:31
GDAT1	Gate Data for I/O Bus
GDCLK0	Sets the guard digit flip flop for use in rounding
GF08630	Active if any of ALU bits 8:63 are set
GF170	Active if any of ALU bits 0:7 are set
G0015	Carry generate for bits 0:15
G041	Carry generate for bits 4:7
G1631	Carry generate for bits 16:31
G3247	Carry generate for bits 32:47
G4863	Carry generate for bits 48:63
G5R131	Indicates whether the number of equlization cycles is within bounds for single and for double precision.
IDLE0/1	Idle mode flip flop
IMM0	Immediate data to be inputted by ALU
IOS01	I/O Select 0
IOS11	I/O Select 1
IRMSEL	Selects either Memory Data Bus or I/O Bus
LDIR0	Load Instruction Register
LDREG0	Load Register from 8/16
LDR001	Data Register Sign bit F/F
MD0	Multiply/Divide Control Line from 8/16
MD000:MD1500	Memory Data Bus
MPY0/1	FPP Command Multiply Instruction

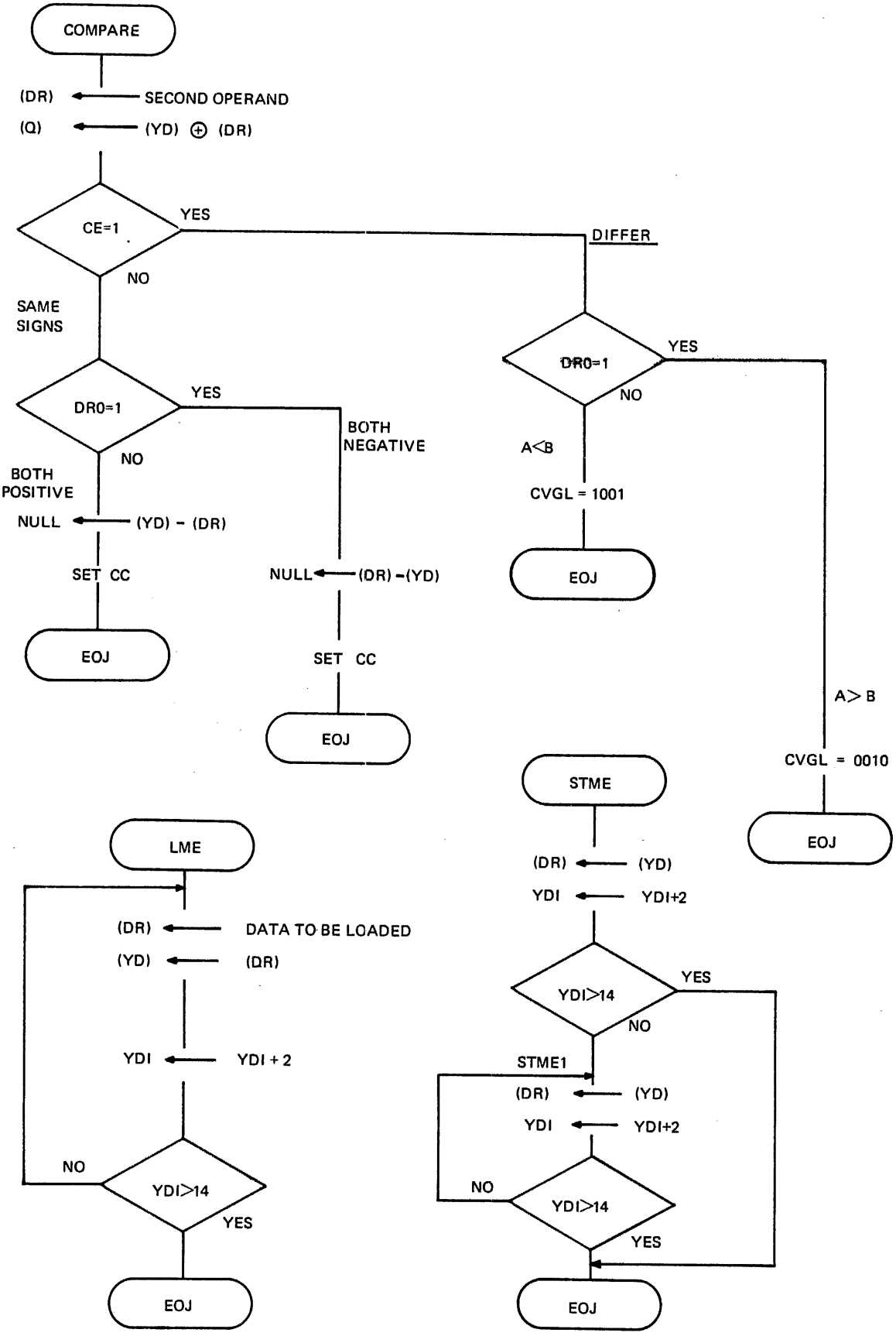
NBRI1	Active when no branch instruction is specified
NORM1	Data in Data Register is normalized
ORBIT11	OR in a one to fractin Bit 11 on Mantissa Carry out
P0015	Carry propagate for bits 0:15
P041	Carry propagate for bits 4:7
P1631	Carry propagate for bits 16:31
P3247	Carry propagate for bits 32:47
P4863	Carry propagate for bits 48:63
QCE1	Exponent Carry F/F
QCF0/1	Fraction Carry F/F
QC641	Data Word Carry (32 or 64 bits) F/F
QDIV0/1	Determine Operation for Command Divide F/F
QGX	Enables Data Register Mux as input to ALU for Fraction Field
QGXA	Buffered QGX
QG1	G flag F/F
QLI1	Quotient Bit for Command Divide
QL1	L flag F/F
QL63	Shift connection for Q Register bit 63
QOV1	Overflow flag F/F
Q1516	Shift Connection between Q Register bits 15 and 16
Q310T	Shift Connection for Q Register bit 31
Q32IN	Shift Connection for Q Register bit 32
Q4748	Shift Connection between Q Register bits 47 and 48
RACK0	Receive Acknowledge Control Line
RARCLR0	Clears the ROM address register to 0
RARLD0	Loads the ROM address register
RAR000:RAR070	ROM address bits
RDRCLK0/1	ROM data clock
RDRCLK1A	Buffered ROM clock
RDSTP0	ROM stop
RD000/1 RD270/1	Latched ROM outputs
RH08	Shift connection for RAM stack bit 8

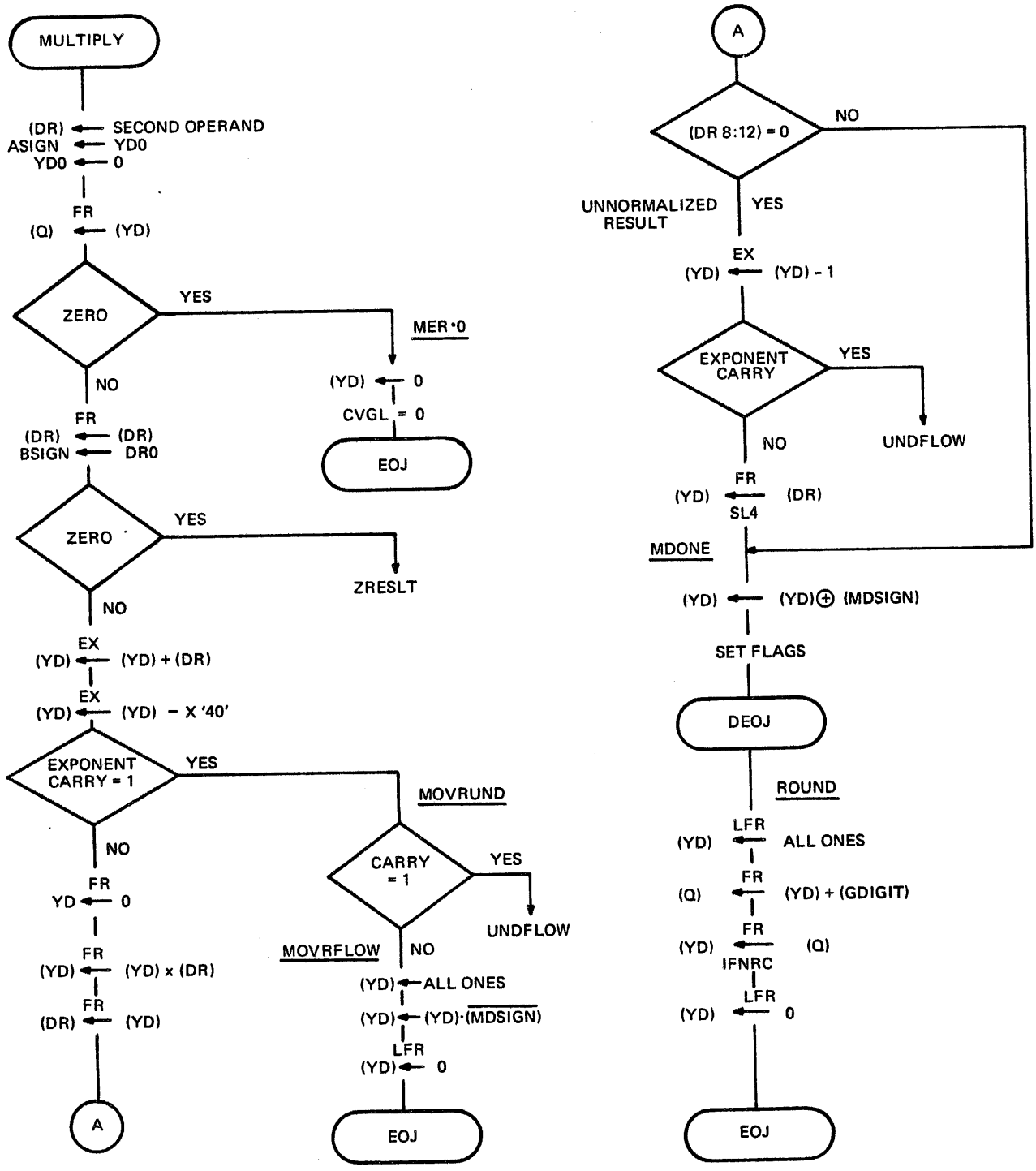
RL63	Shift connection for RAM stack bit 63
RXINST1	Indicates a Register to Memory Instruction
RXWAIT1	Indicates place in microcode to wait for Data to be sent or received.
R1516	Shift connection between RAM stack bits 15 and 16
R3132	Shift connection between RAM stack bits 31 and 32
R4748	Shift connection between RAM stack bits 47 and 48
SCLK11	Clock occuring between system clocks for use with counter
SCLR0	System clear from host processor
SCLR0A	Buffered SCLR0
SDRCLK0	Clock that sets BSN1
SGD1	Force the present Carry In to a 1
SL1	Indicates a shift left of the RAM register stack or the Q register
SNMX	Result sign for the current instruction
SRAR	Steers the ROM address inputs between the Memory Data and the I/O busses
SR071	Shift connection for RAM stack bit 7
SR1	Indicates a shift right of the RAM register stack or the Q register
SR641:SR671	Double Precision guard digit outputs
SUB1	Exclusive OR of RD071 and RD081
SYN0	Synchronize control line to host processor
S001:S631	ALU output bits
S4BT1	Operation to take place on entire data word
TABCLK0	Buffered Clock for Test Aid
TACK0	Transmit acknowledge Control Line
TASTP0	Total Stop
UQG1	Input to G flag F/F
URD001:URD271	Unlatched Outputs of the ROM
WAIT1	Selects I/O Bus or S Bus for Data Register Inputs
XNORM1	Data will be normalized after 1 more hexadecimal digit
XRP	Pullup Resistor
XX	Indicates to I/O whether 32 or 64 bits are involved

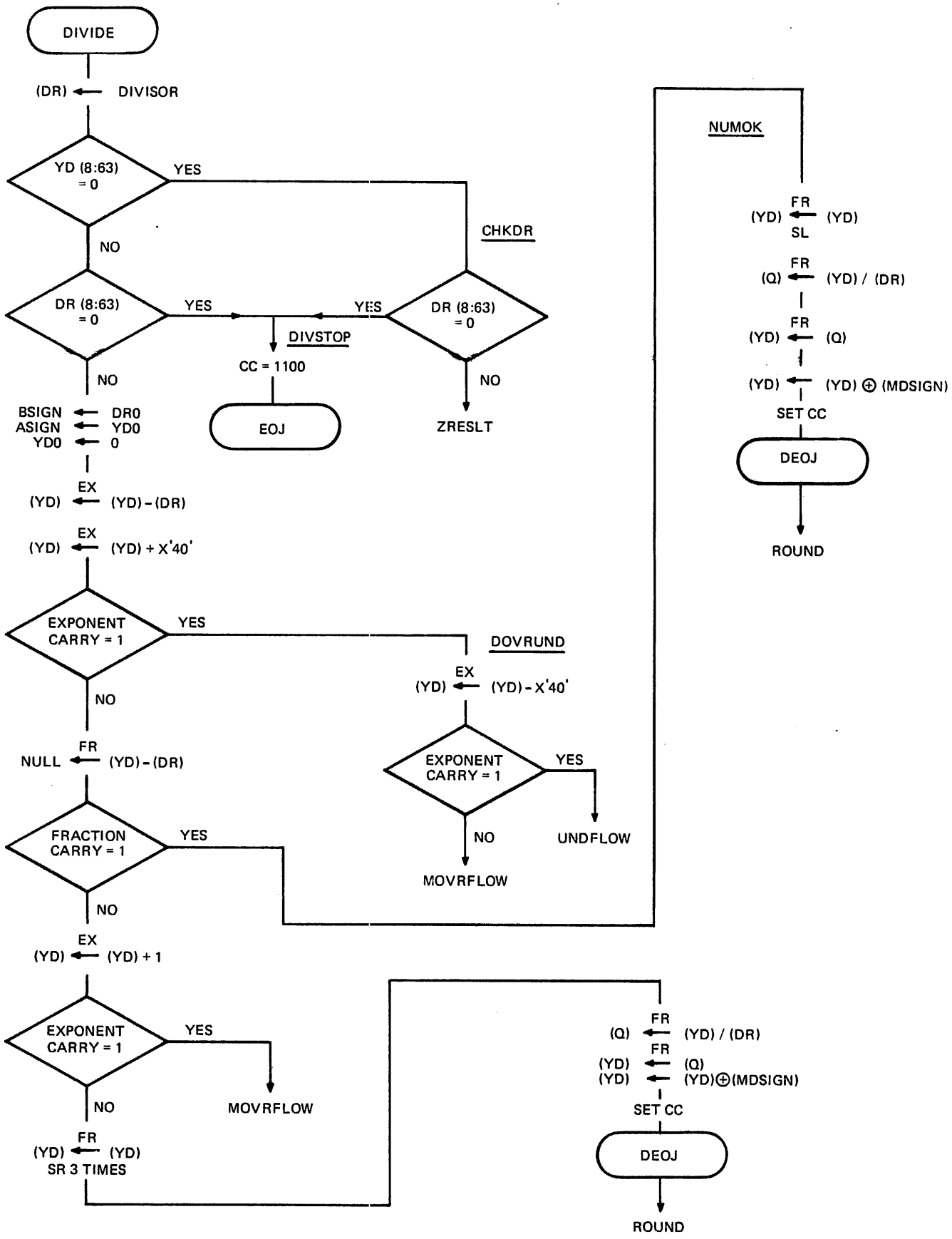
XYZ1	Enables guard digit into carry in logic
YDASN0	Used to strip the arithmetic sign form an operand stored in the register stack
YDCLK1	Clock for the YD register
YDCRY1	Indicates that the top YD register has been reached
YDINC1	Increment the YD register
YD01:YD21	User Destination Register
YS01:YS21	User Source Register

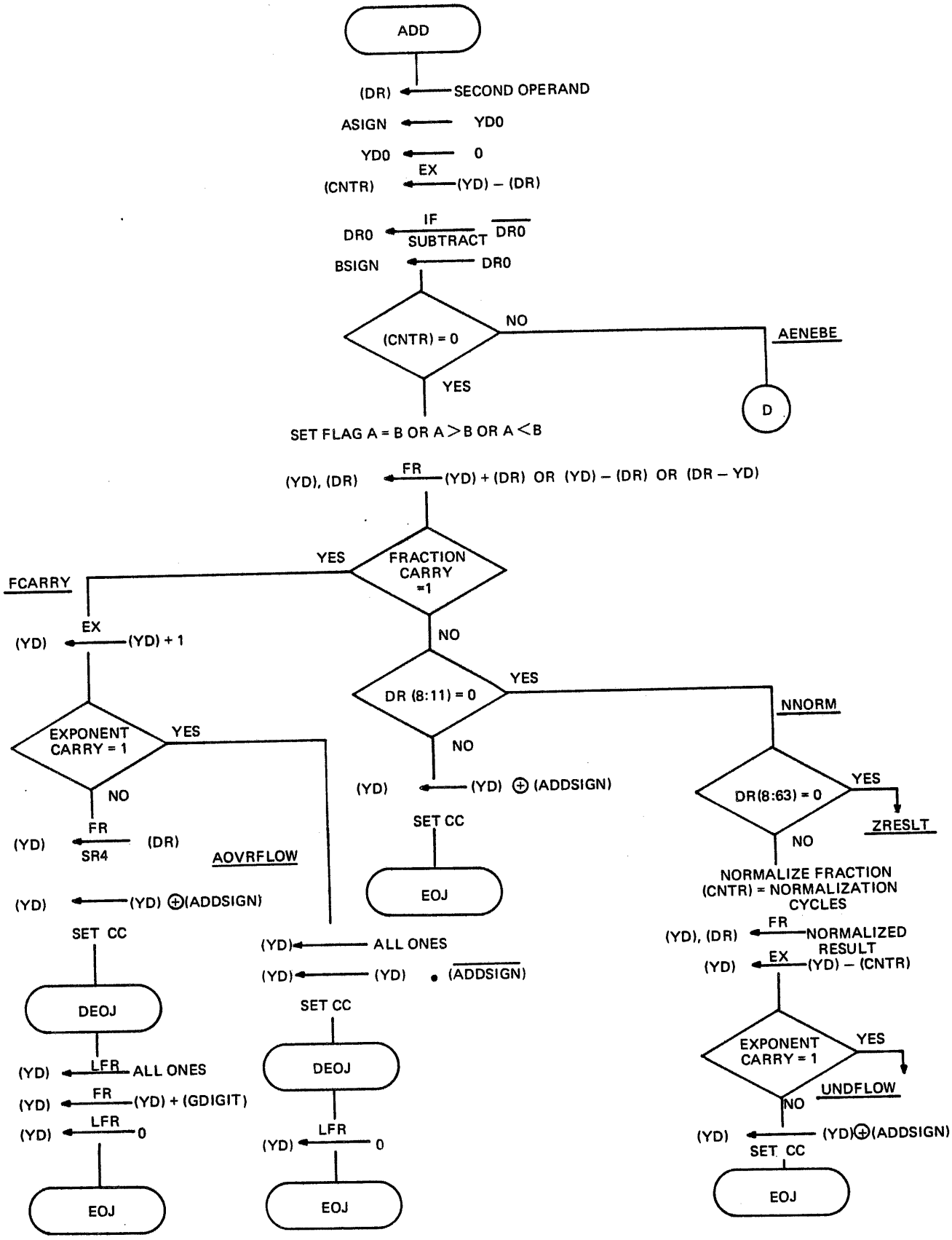
APPENDIX 3
FPP MICROCODE FLOWCHARTS

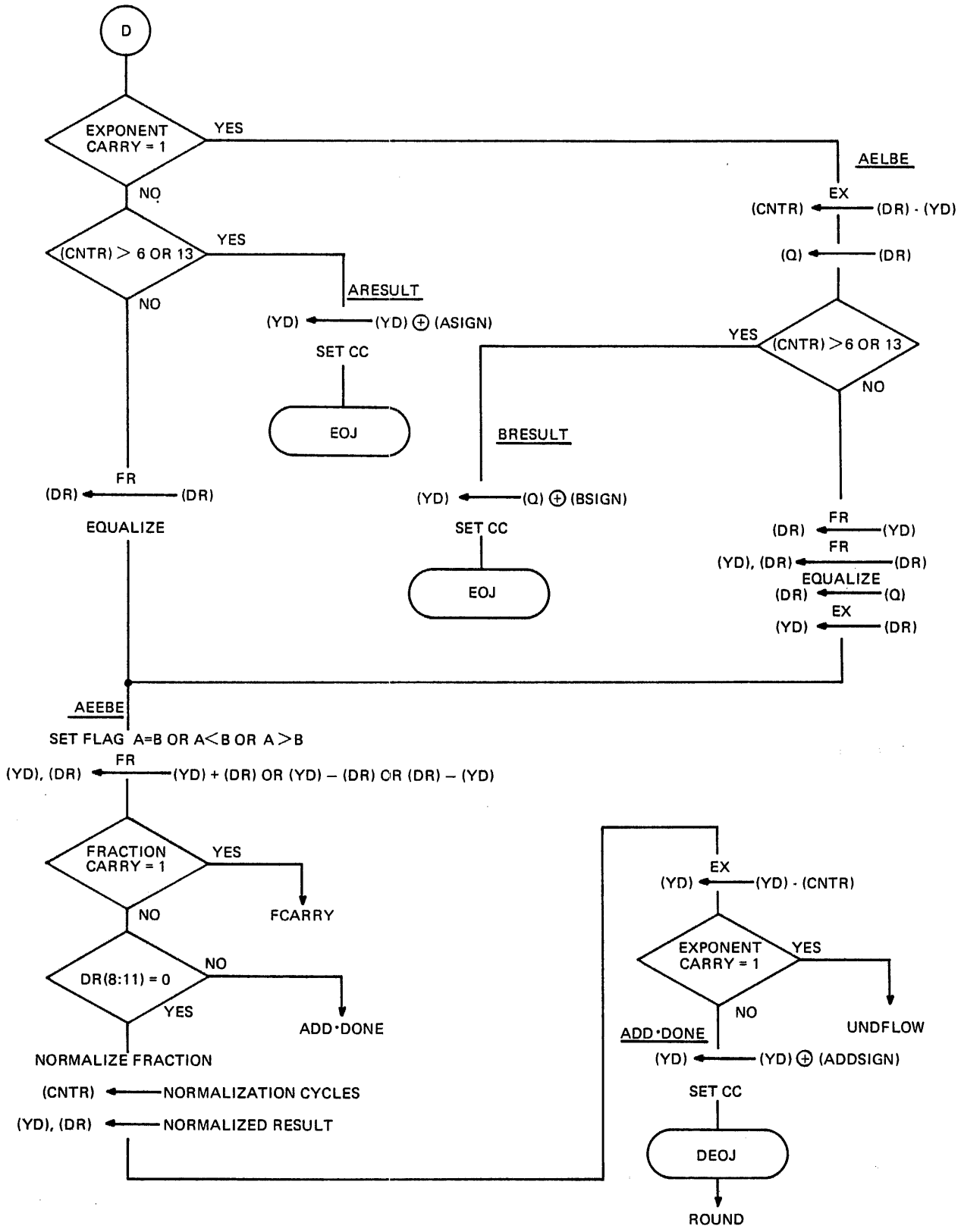


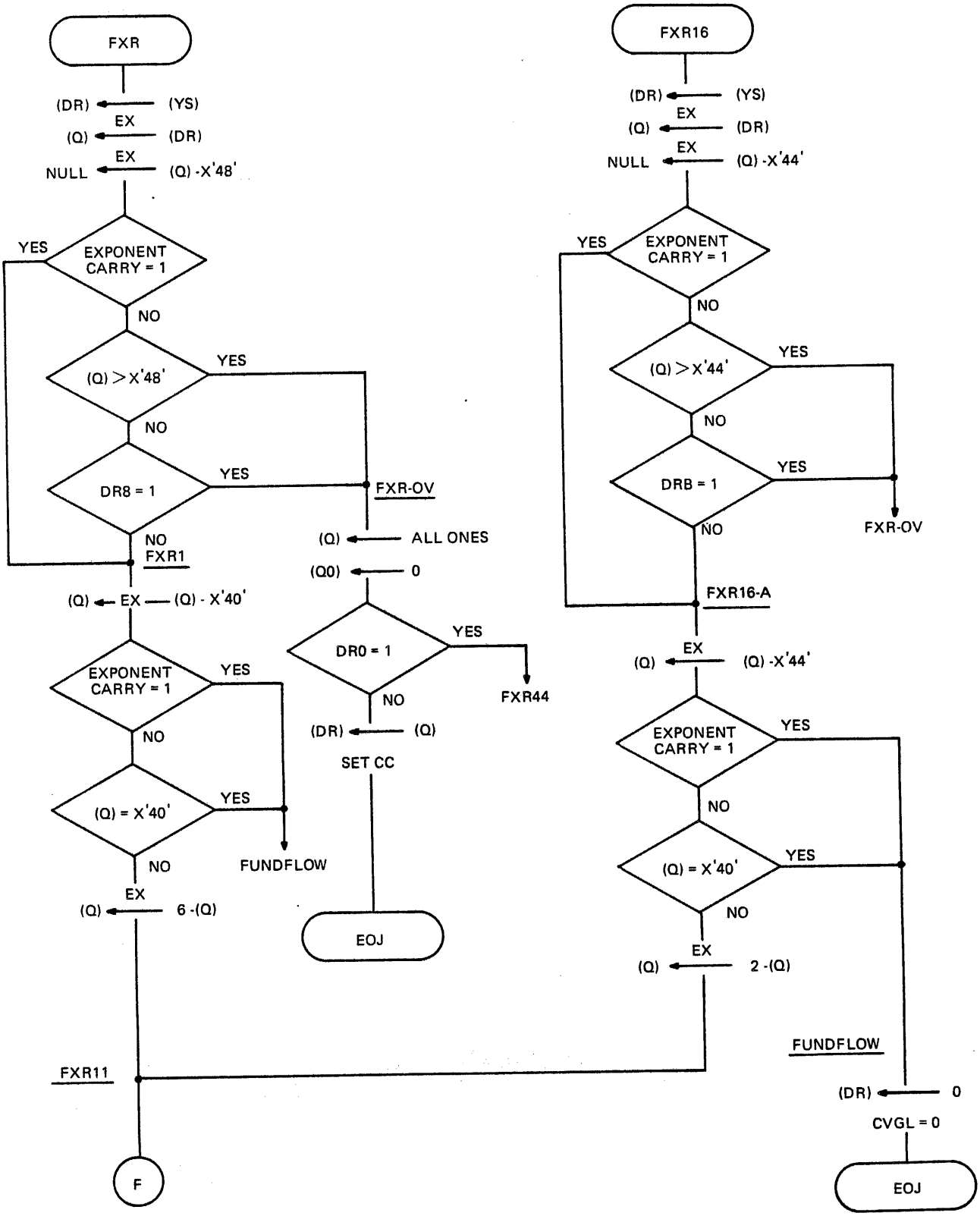

COMPARE
(DR) ← SECOND OPERAND
(Q) ← (YD) ⊕ (DR)
CE=1
YES
DIFFER
NO
SAME SIGNS
DR0=1
YES
BOTH NEGATIVE
NO
BOTH POSITIVE
NULL ← (YD) - (DR)
SET CC
EOJ
NULL ← (DR) -(YD)
SET CC
EOJ
DR0=1
YES
NO
A<B
CVGL = 1001
EOJ
A> B
CVGL = 0010
EOJ
LME
(DR) ← DATA TO BE LOADED
(YD) ← (DR)
YDI ← YDI + 2
NO
YDI>14
YES
EOJ
STME
(DR) ← (YD)
YDI ← YDI+2
YDI>14
YES
NO
STME1
(DR) ← (YD)
YDI ← YDI+2
NO
YDI>14
YES
EOJ

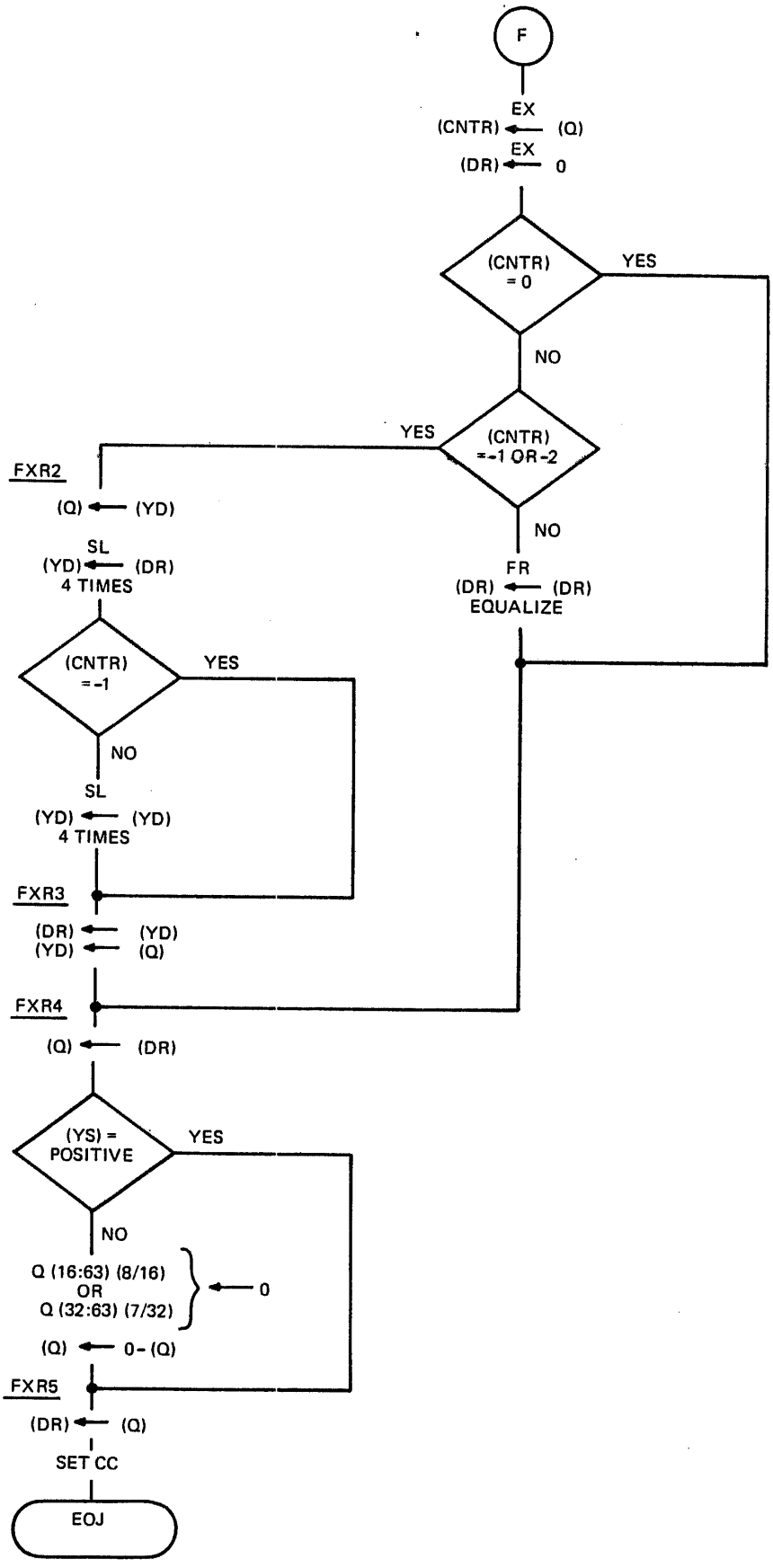

MULTIPLY
(DR) ← SECOND OPERAND
ASIGN ← YD0
YD0 ← 0
FR
(Q) ← (YD)
ZERO
YES
MER*0
(YD) ← 0
CVGL = 0
EOJ
NO
FR
(DR) ← (DR)
BSIGN ← DR0
ZERO
YES
ZRESLT
NO
EX
(YD) ← (YD) + (DR)
EX
(YD) ← (YD) − X '40'
EXPONENT CARRY = 1
YES
MOVRUND
CARRY = 1
YES
UNDFLOW
MOVRFLOW
NO
(YD) ← ALL ONES
(YD) ← (YD)·(MDSIGN)
LFR
(YD) ← 0
EOJ
NO
FR
YD ← 0
FR
(YD) ← (YD) x (DR)
FR
(DR) ← (YD)
A
A
(DR 8:12) = 0
NO
UNNORMALIZED RESULT
YES
EX
(YD) ← (YD) - 1
EXPONENT CARRY
YES
UNDFLOW
NO
FR
(YD) ← (DR)
SL4
MDONE
(YD) ← (YD)⊕ (MDSIGN)
SET FLAGS
DEOJ
ROUND
LFR
(YD) ← ALL ONES
FR
(Q) ← (YD) + (GDIGIT)
FR
(YD) ← (Q)
IFNRC
LFR
(YD) ← 0
EOJ

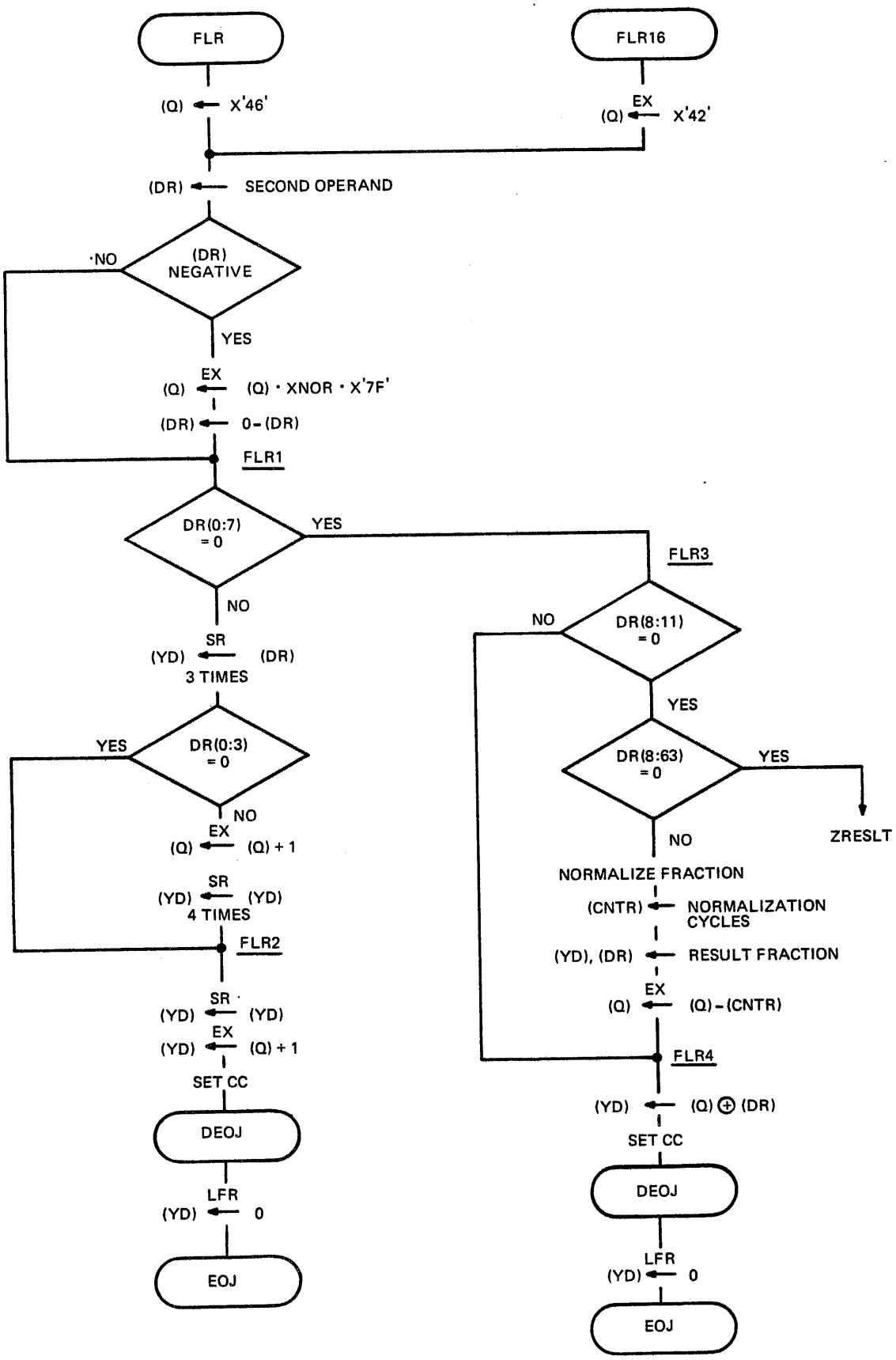

DIVIDE
(DR) ← DIVISOR
YD (8:63) = 0
YES
NO
CHKDR
DR (8:63) = 0
YES
YES
DR (8:63) = 0
DIVSTOP
CC = 1100
EOJ
NO
NO
ZRESLT
BSIGN ← DR0
ASIGN ← YD0
YD0 ← 0
EX
(YD) ← (YD) - (DR)
EX
(YD) ← (YD) + X'40'
EXPONENT CARRY = 1
YES
DOVRUND
EX
(YD) ← (YD) - X'40'
NO
FR
NULL ← (YD) - (DR)
EXPONENT CARRY = 1
YES
UNDFLOW
NO
MOVRFLOW
FRACTION CARRY = 1
YES
NO
EX
(YD) ← (YD) + 1
EXPONENT CARRY = 1
YES
MOVRFLOW
NO
FR
(YD) ← (YD)
SR 3 TIMES
NUMOK
FR
(YD) ← (YD)
SL
FR
(Q) ← (YD) / (DR)
FR
(YD) ← (Q)
(YD) ← (YD) ⊕ (MDSIGN)
SET CC
DEOJ
ROUND
FR
(Q) ← (YD) / (DR)
FR
(YD) ← (Q)
(YD) ← (YD)⊕(MDSIGN)
SET CC
DEOJ
ROUND


ADD
(DR) ← SECOND OPERAND
ASIGN ← YD0
YD0 ← 0
(CNTR) ← EX (YD) – (DR)
DR0 ← IF SUBTRACT $\overline{DR0}$
BSIGN ← DR0
(CNTR) = 0
NO
AENEBE
D
YES
SET FLAG A = B OR A > B OR A < B
(YD), (DR) ← FR (YD) + (DR) OR (YD) – (DR) OR (DR – YD)
FRACTION CARRY =1
YES
FCARRY
(YD) ← EX (YD) + 1
NO
DR (8:11) = 0
YES
NNORM
NO
EXPONENT CARRY = 1
YES
NO
(YD) ← (YD) ⊕ (ADDSIGN)
SET CC
EOJ
DR(8:63) = 0
YES
ZRESLT
NO
NORMALIZE FRACTION
(CNTR) = NORMALIZATION CYCLES
(YD), (DR) ← FR NORMALIZED RESULT
(YD) ← EX (YD) – (CNTR)
EXPONENT CARRY = 1
YES
UNDFLOW
NO
(YD) ← (YD)⊕(ADDSIGN)
SET CC
EOJ
(YD) ← FR (DR)
SR4
AOVRFLOW
(YD) ← (YD) ⊕(ADDSIGN)
SET CC
DEOJ
(YD) ← LFR ALL ONES
(YD) ← FR (YD) + (GDIGIT)
(YD) ← LFR 0
EOJ
(YD) ← ALL ONES
(YD) ← (YD) • $\overline{(ADDSIGN)}$
SET CC
DEOJ
(YD) ← LFR 0
EOJ


D
EXPONENT CARRY = 1
YES
NO
AELBE
EX
(CNTR) ← (DR) - (YD)
(Q) ← (DR)
(CNTR) > 6 OR 13
YES
NO
ARESULT
(YD) ← (YD) ⊕ (ASIGN)
SET CC
EOJ
(CNTR) > 6 OR 13
YES
NO
BRESULT
(YD) ← (Q) ⊕ (BSIGN)
SET CC
EOJ
FR
(DR) ← (DR)
EQUALIZE
FR
(DR) ← (YD)
FR
(YD), (DR) ← (DR)
EQUALIZE
(DR) ← (Q)
EX
(YD) ← (DR)
AEEBE
SET FLAG A=B OR A<B OR A>B
FR
(YD), (DR) ← (YD) + (DR) OR (YD) – (DR) OR (DR) – (YD)
FRACTION CARRY = 1
YES
NO
FCARRY
DR(8:11) = 0
NO
YES
ADD·DONE
NORMALIZE FRACTION
(CNTR) ← NORMALIZATION CYCLES
(YD), (DR) ← NORMALIZED RESULT
EX
(YD) ← (YD) - (CNTR)
EXPONENT CARRY = 1
YES
NO
UNDFLOW
ADD·DONE
(YD) ← (YD) ⊕ (ADDSIGN)
SET CC
DEOJ
ROUND


FXR
(DR) ← (YS)
EX
(Q) ← (DR)
EX
NULL ← (Q) -X'48'
YES
EXPONENT CARRY = 1
NO
(Q) > X'48'
YES
NO
DR8 = 1
YES
FXR-OV
NO
FXR1
(Q) ← EX — (Q) - X'40'
EXPONENT CARRY = 1
YES
NO
(Q) = X'40'
YES
NO
FUNDFLOW
EX
(Q) ← 6 -(Q)
(Q) ← ALL ONES
(Q0) ← 0
DR0 = 1
YES
FXR44
NO
(DR) ← (Q)
SET CC
EOJ
FXR11
F
FXR16
(DR) ← (YS)
EX
(Q) ← (DR)
EX
NULL ← (Q) -X'44'
YES
EXPONENT CARRY = 1
NO
(Q) > X'44'
YES
NO
DRB = 1
YES
FXR-OV
NO
FXR16-A
EX
(Q) ← (Q) -X'44'
EXPONENT CARRY = 1
YES
NO
(Q) = X'40'
YES
NO
EX
(Q) ← 2 -(Q)
FUNDFLOW
(DR) ← 0
CVGL = 0
EOJ


F
EX
(CNTR) ← (Q)
EX
(DR) ← 0
(CNTR) = 0
YES
NO
(CNTR) = -1 OR -2
YES
FXR2
(Q) ← (YD)
SL
(YD) ← (DR)
4 TIMES
NO
FR
(DR) ← (DR)
EQUALIZE
(CNTR) = -1
YES
NO
SL
(YD) ← (YD)
4 TIMES
FXR3
(DR) ← (YD)
(YD) ← (Q)
FXR4
(Q) ← (DR)
(YS) = POSITIVE
YES
NO
Q (16:63) (8/16) OR Q (32:63) (7/32)
← 0
(Q) ← 0 - (Q)
FXR5
(DR) ← (Q)
SET CC
EOJ


FLR
FLR16
(Q) ← X'46'
EX (Q) ← X'42'
(DR) ← SECOND OPERAND
(DR) NEGATIVE
NO
YES
EX (Q) ← (Q) · XNOR · X'7F'
(DR) ← 0 - (DR)
FLR1
DR(0:7) = 0
YES
NO
FLR3
NO
DR(8:11) = 0
YES
SR (YD) ← (DR) 3 TIMES
DR(0:3) = 0
YES
NO
DR(8:63) = 0
YES
NO
ZRESLT
EX (Q) ← (Q) + 1
SR (YD) ← (YD) 4 TIMES
FLR2
NORMALIZE FRACTION
(CNTR) ← NORMALIZATION CYCLES
(YD), (DR) ← RESULT FRACTION
EX (Q) ← (Q) - (CNTR)
SR (YD) ← (YD)
EX (YD) ← (Q) + 1
FLR4
SET CC
(YD) ← (Q) ⊕ (DR)
SET CC
DEOJ
DEOJ
LFR (YD) ← 0
LFR (YD) ← 0
EOJ
EOJ

```
                                1           SCRAT                                                                FPP0002
                                2           CROSS                                                                FPP0003
                                3           SOCHK                                                                FPP0003
                                4   *                                                                            FPP0004
                                5   * COPYRIGHT INTERDATA INC.   OCTOBER 1976                                    FPP0005
                                6   *                                                                            FPP0006
                                7   * DHEMA MAHAJAN                                                              FPP0007
                                8   *                                                                            FPP0008
                                9   *                                                                            FPP0009
                               10   * THE MICRODE IS CONTAINED IN THE FOLLOWING 256 X 4 (1K) ROM CHIPS           FPP0010


                               12           PARTS 19-188R00F10,19-188R00F11,19-188R00F12,19-188R00F13            FPP0012
                               13           PARTS 19-188R00F14,19-188R00F15,19-188R00F16                         FPP0013


                               15   * IMMEDIATE OPERAND EQUATES                                                  FPP0015
                               16   *                                                                            FPP0016
                               17   X02     EQU   '02'                                                          FPP0017
0002                           18   X06     EQU   '06'                                                          FPP0018
0006                           19   X08     EQU   '08'                                                          FPP0019
0008                           20   X40     EQU   '10'                                                          FPP0020
0010                           21   X42     EQU   '12'                                                          FPP0021
0012                           22   X44     EQU   '14'                                                          FPP0022
0014                           23   X46     EQU   '16'                                                          FPP0023
0016                           24   X48     EQU   '18'                                                          FPP0024
0018                           25   X7F     EQU   '1F'                                                          FPP0025
001F


                               27   *                                                                            FPP0027
                               28   * ON POWER UP OR AFTER EOJ/DEOJ, COME HERE.                                  FPP0028
                               29   * FPP IS IN IDLE STATE                                                       FPP0029
                               30   *                                                                            FPP0030
                               31   *                                                                            FPP0031
000    022 E800                32           CLR   DR&0                  CLEAR DR & Q REGISTERS                   FPP0032
                               33   *                                                                            FPP0033
                               34   *                                                                            FPP0034
                               35   * WHEN A USER INSTRUCTION IS FETCHED FROM MAIN MEMORY                        FPP0035
                               36   * BY THE HOST PROCESSOR, THE FIRST HW IS CAPTURED IN THE                     FPP0036
                               37   * INSTRUCTION REGISTER OF FPP.                                               FPP0037
                               38   *                                                                            FPP0038
                               39   * THE OP-CODE IS DECODED                                                     FPP0039
                               40   * IF IT IS A LEGAL FLOATING POINT INSTRUCTION AND THE                        FPP0040
                               41   * HOST PROCESSOR DOES NOT DETECT AN INTERRUPT TO BE                          FPP0041
                               42   * HONOURED, A BRANCH IS TAKEN TO THE APPROPRIATE                            FPP0042
                               43   * EMULATION SEQUENCE.                                                       FPP0043
                               44   *                                                                            FPP0044
                               45   * FIRST OPERAND IS REFERED TO AS 'A'                                         FPP0045
                               46   * SECOND OPERAND IS REFERED TO AS 'B'                                        FPP0046
                               47   *                                                                            FPP0047
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FLOATING POINT PROCESSOR MICROCODE  05-066R00A13          PAGE   2

001                         49          ORG   '04'                                    FPP0049
                            50    *                                                   FPP0050
                            51    * LOAD REGISTER : LER(28),LDR(38)                   FPP0051
                            52    *                                                   FPP0052
004    09B E800             53    LER       L     DR,YS              (DR) = SECOND OPERAND  FPP0053
                            54    *                                                   FPP0054
                            55    * LOAD : LE(68),LD(78)                             FPP0055
                            56    *                                                   FPP0056
                            57    *                                                   FPP0057
005    05F A86C             58    LE        L     DR,DR,FR+F+RXWAIT  LOOK @ FRACTION     FPP0058
006    402 040E             59              BT    NORM,LDONE,UCC     IF NORMALIZED, DONE FPP0059
007    680 0228             60              BF    G,ZRESLT,CLRCNTR   IF ZERO, BRANCH     FPP0060
008    8C7 8800             61              CNM                      1:13 NORMALIZATION CYCLES  FPP0061
                            62    *                                 (YD8:63)=(DR8:63)=NORMALIZED FRACTION  FPP0062
009    01F 7000             63              L     Q,CNTR,EX                            FPP0063
00A    056 6004             64              RS    NULL,DR,Q,EX+F     LOOK @ RESULT EXPONENT  FPP0064
00B    420 0029             65              BT    CE,UNDFLOW         UNDERFLOW OCCURED   FPP0065
00C    0D6 6070             66              RS    YD,DR,Q,DRSIGN+EX  (YD0:7) = RESULT SIGN + EXPONENT  FPP0066
00D    00B E005             67              L     YD,YD,F+EOJ        SET G/L FLAG, QUIT  FPP0067
00F    00F E075             68    LDONE     L     YD,DR,DRSIGN+F+EOJ SET G/L FLAG, QUIT  FPP0068


00F                         70              ORG   '10'                               FPP0070
                            71    *                                                   FPP0071
                            72    * COMPARE REGISTER : CER(29),CDR(39)               FPP0072
                            73    *                                                   FPP0073
010    09B E800             74    CER       L     DR,YS              (DR) = SECOND OPERAND  FPP0074
                            75    *                                                   FPP0075
                            76    * COMPARE : CE(69),CD(79)                          FPP0076
                            77    *                                                   FPP0077
011    035 607C             78    CE        X     Q,YD,DR,DRSIGN+F+EX+RXWAIT FOR RX INSTRUCTIONS WAIT  FPP0078
                            79    *                                 TILL DATA IS AVAILABLE IN 'DR'  FPP0079
012    420 0516             80              BT    CE,DIFFER,SETDR0+UCC BRANCH IF SIGNS DIFFER  FPP0080
013    400 2015             81              BT    DR0,NEG            BRANCH IF 2ND OP IS NEGATIVE  FPP0081
014    04D E005             82              S     NULL,YD,DR,F+EOJ   (A) - (B), SET CC, QUIT  FPP0082
015    055 E075             83    NEG       RS    NULL,DR,YD,DRSIGN+F+EOJ (B) - (A), SET CC, QUIT  FPP0083
                            84    *                                                   FPP0084
016    400 2018             85    DIFFER    BT    DR0,AGB                            FPP0085
017    23F D015             86              INVI  Q,'00',F+SETC+EOJ  CVGL = 1001     FPP0086
018    21F 5085             87    AGB       LI    Q,'01',EX+F+EOJ    CVGL = 0010     FPP0087


019                         89              ORG   '1D'                               FPP0089
                            90    *                                                   FPP0090
                            91    * LOAD MULTIPLE : LME(72),LMD(7F)                  FPP0091
                            92    *                                                   FPP0092
01D    0DF E078             93    LME       L     YD,DR,RXWAIT+DRSIGN WAIT TILL DATA IS AVAILABLE IN 'DR'  FPP0093
01E    01A E060             94              L     Q,Q,YDP2           BUMP YD FIELD   FPP0094
01F    608 041D             95              BF    YDC,LME,UCC        LOOP TILL (YD) > 14  FPP0095
020    01A E001             96              L     Q,Q,EOJ                            FPP0096


021                         98              ORG   '21'                               FPP0098
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                                  99  *                                                                                  FPP0099
                                 100  * STORE MULTIPLE : STME(71),STMD(7E)                                              FPP0100
                                 101  *                                                                                  FPP0101
021   05B E868                   102  STME     L     DR,YD,RXWAIT          LOAD DR & WAIT                           FPP0102
022   01A E060                   103              L     Q,Q,YDP2              POINT TO NEXT REGISTER                   FPP0103
023   408 0027                   104              BT    YDC,STDONE                                                     FPP0104
024   05B E868                   105  STME1    L     DR,YD,RXWAIT          WAIT TILL PREVIOUS DR DATA IS TAKEN      FPP0105
025   01A E060                   106              L     Q,Q,YDP2                                                       FPP0106
026   608 0024                   107              BF    YDC,STME1             LOOP TILL (YD) > 14                      FPP0107
027   01A E001                   108  STDONE   L     Q,Q,EOJ                                                        FPP0108
                                 109  *                                                                              FPP0109
                                 110  * COMMON TERMINATION ROUTINES                                                  FPP0110
                                 111  *                                                                              FPP0111
028   2DF D005                   112  ZRESLT   LI    YD,0,F+EOJ            RESULT IS ZERO; (CVGL) = 0000            FPP0112
029   2DF D00D                   113  UNDFLOW  LI    YD,0,SETV+F+EOJ       EXPONENT UNDERFLOW; (CVGL) = 0100        FPP0113
02A   21F D01D                   114  DIVSTOP  LI    Q,0,SETC+SETV+F+EOJ   DIVIDE STOP CONDITION; (CVGL) = 1100    FPP0114
02B   0DD C205                   115  ARESULT  O     YD,YD,ASIGN,F+EOJ     (RESULT) = FIRST OPERAND                 FPP0115
02C   0DE C285                   116  BRESULT  O     YD,Q,BSIGN,F+EOJ      (RESULT) = SECOND OPERAND                FPP0116
                                 117  *                                                                              FPP0117
02D   2FF D008                   118  AOVRFLOW INVI  YD,0,SETV             EXPONENT OVERFLOW IN ADDITION            FPP0118
02E   0ED C306                   119              N2    YD,YD,ADDSIGN,F+EOJ (CVGL) = 0101 OR 0110                    FPP0119
02F   2DF 1001                   120              LI    YD,0,LFR+EOJ                                                 FPP0120


                                 122              ORG   '31'                                                           FPP0122
030                              123  *                                                                              FPP0123
                                 124  * STORE : STE(60),STD(70)                                                      FPP0124
                                 125  *                                                                              FPP0125
031   05B E869                   126  STE      L     DR,YD,RXWAIT+EOJ      WAIT TILL 'DR' DATA IS TAKEN             FPP0126
                                 127  *                                    BY HOST PROCESSOR, THEN QUIT             FPP0127
                                 128  *                                                                              FPP0128
                                 129  *                                                                              FPP0129
                                 130              ORG   '34'                                                           FPP0130
032                              131  *                                                                              FPP0131
                                 132  * MULTIPLY REGISTER : MER(2C),MDR(3C)                                           FPP0132
                                 133  *                                                                              FPP0133
034   09B E800                   134  MER      L     DR,YS                 (DR) = SECOND OPERAND                    FPP0134
                                 135  *                                                                              FPP0135
                                 136  * MULTIPLY : ME(6C),MD(7C)                                                      FPP0136
                                 137  *                                                                              FPP0137
035   2A5 5F80                   138  ME       NI    YDA,YD,X7F,EX         (YD0) = 0 ; (YD1:7) = EXPONENT           FPP0138
                                 139  *                                    ASIGN IS UPDATED                         FPP0139
036   01B A004                   140              L     Q,YD,FR+F             (Q 8:63) = MULTIPLICAND FRACTION         FPP0140
037   680 044D                   141              BF    G,MER,0,UCC           BRANCH IF ZERO                           FPP0141
038   05F A86C                   142              L     DR,DR,FR+F+RXWAIT     (DR 8:63) = MULTIPLIER FRACTION          FPP0142
039   680 0128                   143              BF    G,ZRESLT,SETDR0       BSIGN IS UPDATED                         FPP0143
03A   0C5 6000                   144              A     YD,YD,DR,EX           ADD EXPONENTS                            FPP0144
03B   2CD 5804                   145              SI    YD,YD,X40,EX+F        (YD1:7) = EXCESS-64 EXPONENT             FPP0145
03C   420 0049                   146              BT    CE,MOVRUN0            RESULT EXPONENT TOO LARGE/SMALL          FPP0146
                                 147  * OPERANDS ARE OK. PROCEED WITH MULTIPLICATION                                  FPP0147
03D   31F 9000                   148              DC    '31F9000'             (YD8:63) = 0, SR Q                       FPP0148
03E   D03 A000                   149              MPY   FR                    24/56 MULTIPLICATION CYCLES              FPP0149
                                 150  *                                       (YD8:63) = RESULT FRACITON               FPP0150
03F   05B A822                   151              L     DR,YD,FR+SETGD                                                 FPP0151
040   402 0044                   152              BT    NORM,MDONE            IF NORMALIZED, DONE                      FPP0152
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FLOATING POINT PROCESSOR MICROCODE  05-066R00A13          PAGE   4

  041    2CD 5084        153              SI     YD,YD,'01',EX+F      DECREMENT RESULT EXPONENT FOR          FPP0153
                         154     *                                    ONE NORMALIZATION CYCLE                FPP0154
  042    420 0029        155              BT     CE,UNDFLOW                                                  FPP0155
  043    0DF B022        156              DC     '0DFB022'                                                   FPP0156
  044    0DD C386        157     MDONE    O      YD,YD,MDSIGN,F+DEOJ  SET RESULT SIGN                       FPP0157
                         158     *                                    QUIT IF DOUBLE PRECISION               FPP0158
  045    2FF 1000        159     ROUND    INVI   YD,0,LFR                                                    FPP0159
  046    005 A1C8        160              A      Q,YD,GDIGIT,FR+RCO   ADD GUARD DIGIT                       FPP0160
  047    0DA A050        161              L      YD,Q,FR+IFNRC        UPDATE RESULT IF NO ROUNDING CARRY     FPP0161
  048    2DF 1001        162              LI     YD,0,LFR+EOJ         DONE                                   FPP0162
                         163     *                                                                           FPP0163
                         164     *                                                                           FPP0164
  049    440 0029        165     MOVRUND  BT     C,UNDFLOW            CARRY OUT OF BIT ZERO : UNDERFLOW      FPP0165
                         166     *                                                                           FPP0166
  04A    2FF D008        167     MOVRFLOW INVI   YD,0,SETV            EXPONENT OVERFLOW IN MULTIPLICATION    FPP0167
  04B    0ED C386        168              N2     YD,YD,MDSIGN,F+DEOJ  (CVGL) = 0101 OR 0110                  FPP0168
  04C    2DF 1001        169              LI     YD,0,LFR+EOJ                                               FPP0169
                         170     *                                                                           FPP0170
  04D    2DF D06D        171     MER,0    LI     YD,0,RXWAIT+F+EOJ    WAIT TILL 'DR' DATA IS LOADED          FPP0171
                         172     *                                    BY HOST PROCESSOR. THEN QUIT           FPP0172
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04F                 ORG    '50'                                            FPP0174
              *                                                            FPP0175
              * DIVIDE REGISTER : DER(2D),DDR(3D)                          FPP0176
              *                                                            FPP0177
050  09B E800 DER     L     DR,YS              (DR) = SECOND OPERAND       FPP0178
              *                                                            FPP0179
              * DIVIDE : DE(6D),DD(7D)                                     FPP0180
              *                                                            FPP0181
051  0DB A004 DE      L     YD,YD,FR+F         SEE IF DIVIDEND IS ZERO     FPP0182
052  680 046F         BF    G,CHKDR,UCC        YES                         FPP0183
053  05F A86C         L     DR,DR,FR+F+RXWAIT  SEE IF DIVISOR IS ZERO      FPP0184
054  680 012A         BF    G,DIVSTOP,SETDRO   UPDATE BSIGN                FPP0185
055  2A5 5F80         NI    YDA,YD,X7F,EX      STRIP & SAVE ASIGN          FPP0186
056  0CD 6000         S     YD,YD,DR,EX        SUBTRACT EXPONENTS          FPP0187
057  2C5 5804         AI    YD,YD,X40,EX+F     BACK TO EXCESS-64 NOTATION  FPP0188
058  420 006C         BT    CE,DOVRUND         RESULT EXPONENT IS TOO LARGE/SMALL FPP0189
              * OPERANDS ARE OK. PROCEED WITH DIVISION                     FPP0190
059  04D A004         S     NULL,YD,DR,FR+F    TRIAL SUBTRACT              FPP0191
05A  410 0064         BT    CF,NUMOK           OK                          FPP0192
05B  2C5 5084         AI    YD,YD,'01',EX+F    GOES. BUMP DIVIDEND EXPONENT FPP0193
05C  420 004A         BT    CE,MOVRFLOW                                    FPP0194
05D  15B A000         LSR   YD,YD,FR                                       FPP0195
05E  15B A000         LSR   YD,YD,FR                                       FPP0196
05F  15B A000         LSR   YD,YD,FR           (YD8:63) = ADJUSTED DIVIDENT FR. FPP0197
060  F85 A022         DIV   FR+SETGD           25/57 DIVIDE CYCLES         FPP0198
              *                                (Q8:63) = RESULT FRACTION   FPP0199
061  0DA A000         L     YD,Q,FR                                        FPP0200
062  0DD C386         O     YD,YD,MDSIGN,F+DEOJ OR IN SIGN. DONE FOR DPFP  FPP0201
063  401 0045         B     ROUND                                          FPP0202
              *                                                            FPP0203
064  1DB A004 NUMOK   LSL   YD,YD,FR+F         (YD8:63) = ADJUSTED DIVIDEND FR. FPP0204
065  F85 A022         DIV   FR+SETGD           (Q8:63) = QUOTIENT          FPP0205
066  0DA A000         L     YD,Q,FR                                        FPP0206
067  0DD C386         O     YD,YD,MDSIGN,F+DEOJ OR IN SIGN                 FPP0207
              *                                                            FPP0208
068  2FF 1000         INVI  YD,0,LFR                                       FPP0209
069  005 A1C8         A     Q,YD,GDIGIT,FR+RCO ADD GUARD DIGIT             FPP0210
06A  0DA A050         L     YD,Q,FR+IFNRC      UPDATE RESULT IF NO ROUNDING CARRY FPP0211
06B  2DF 1001         LI    YD,0,LFR+EOJ       DONE                        FPP0212
              *                                                            FPP0213
              * EXPONENT UNDERFLOW OR OVERFLOW DETECTED                     FPP0214
              *                                                            FPP0215
06C  2CD 5804 DOVRUND SI    YD,YD,X40,EX+F                                 FPP0216
06D  620 004A         BF    CE,MOVRFLOW                                    FPP0217
06E  2DF D00D         LI    YD,0,SETV+F+EOJ    UNDERFLOW                   FPP0218
              *                                                            FPP0219
06F  05F A86C CHKDR   L     DR,DR,FR+F+RXWAIT  SEE IF DIVISOR IS ZERO      FPP0220
070  680 002A         BF    G,DIVSTOP          YES                         FPP0221
071  2DF D005         LI    YD,0,F+EOJ         ZERO RESULT                 FPP0222
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072                           ORG   '74'                                   FPP0224
                        *                                                  FPP0225
                        * ADD REGISTER      : AER(2A),ADR(3A)              FPP0226
                        * SUBTRACT REGISTER : SER(2B),SDR(3B)              FPP0227
                        *                                                  FPP0228
074    39B E800         AER       L     DR,YS              (DR) = SECOND OPERAND  FPP0229
                        *                                                  FPP0230
                        * ADD      : AE(6A),AD(7A)                         FPP0231
                        * SUBTRACT : SE(6B),SD(7B)                         FPP0232
                        *                                                  FPP0233
075    2A5 5F80         AE        NI    YDA,YD,X7F,EX       STRIP & SAVE 1ST OP SIGN (ASIGN)  FPP0234
076    04D 646C                   S     CNTR,YD,DR,EX+RXWAIT+F (CNTR) = EXPONENT DIFFERENCE  FPP0235
077    480 0589                   BT    G,AENEBE,UCC+SETDR0 BRANCH IF EXPONENTS DIFFER  FPP0236
                        *                                   COMPLEMENT DR SIGN IF SUBTRACT  FPP0237
                        *                                   SAVE 2ND OP SIGN (BSIGN)  FPP0238
078    04D A066                   S     NULL,YD,DR,FR+F+ALBAGB FRACTIONS : A=B, A>B, A<B  ?  FPP0239
079    0C5 A834                   A     YD&DR,YD,DR,FR+TAKOP+F (YD&DR) = YD+DR/YD-DR/DR-YD  FPP0240
07A    410 0082                   BT    CF,FCARRY           FRACTION CARRY (ADD)  FPP0241
07B    602 007D                   BF    NORM,NNORM          SEE IF NORMALIZED (SUB)  FPP0242
07C    0DD C305                   O     YD,YD,ADDSIGN,F+EOJ YES, OR IN SIGN, QUIT  FPP0243
                        *                                                  FPP0244
                        * RESULT FRACTION IS NOT NORMALIZED                FPP0245
                        *                                                  FPP0246
07D    680 0228         NNORM     BF    G,ZRESLT,CLRCNTR    BRANCH IF ZERO. CLEAR CNTR  FPP0247
07E    8C7 B800                   CNM                       NORMALIZE (UPTO 5/13 CYCLES)  FPP0248
                        *                                  (YD8:63)=(DR8:63)=NORMALIZED FRACTION  FPP0249
07F    0CD 7004                   S     YD,YD,CNTR,EX+F     ADJUST RESULT EXPONENT  FPP0250
080    420 0029                   BT    CE,UNDFLOW                         FPP0251
081    0DD C305                   O     YD,YD,ADDSIGN,F+EOJ OR IN SIGN. QUIT  FPP0252
                        *                                                  FPP0253
                        * FRACTION CARRY OCCURED IN ADD OR SUBTRACT        FPP0254
                        *                                                  FPP0255
082    2C5 5084         FCARRY    AI    YD,YD,'01',EX+F     BUMP EXPONENT  FPP0256
083    420 002D                   BT    CE,AOVRFLOW                        FPP0257
084    0DF 902A                   DC    '0DF902A'                          FPP0258
                        *                                                  FPP0259
085    0DD C306                   O     YD,YD,ADDSIGN,F+DEOJ OR IN SIGN, QUIT FOR DPFP  FPP0260
086    2FF 1000                   INVI  YD,0,LFR                           FPP0261
087    0C5 A180                   A     YD,YD,GDIGIT,FR     ADD GUARD DIGIT  FPP0262
088    2DF 1001                   LI    YD,0,LFR+EOJ        (YD32:63) = 0  FPP0263
                        *                                                  FPP0264
                        * EXPONENTS OF TWO OPERANDS DIFFER                 FPP0265
                        *                                                  FPP0266
089    420 008D         AENEBE    BT    CE,AELBE            IF CARRY, A(EXP) < B(EXP)  FPP0267
08A    404 002B                   BT    >5,ARESULT          IF (CNTR) > 5 OR > 13; BRANCH  FPP0268
08B    A47 9841                   CEQ   DR,DR,FR+AGB        EQUALIZE 2ND OP  FPP0269
08C    401 0094                   B     AEEBE                              FPP0270
08D    055 6400         AELBE     RS    CNTR,DR,YD,EX       (CNTR) = 2ND OP EX - 1ST OP EX  FPP0271
08E    01F E000                   L     Q,DR                SAVE DR IN Q   FPP0272
08F    404 002C                   BT    >5,BRESULT                         FPP0273
090    05B A842                   L     DR,YD,FR+ALB                       FPP0274
091    AC7 9800                   CEQ   YD&DR,DR,FR         EQUALIZE 1ST OP  FPP0275
092    05A E800                   L     DR,Q                RESTORE DR     FPP0276
093    0DF 6000                   L     YD,DR,EX            (YD 1:8) = RESULT EXPONENT  FPP0277
                        *                                                  FPP0278
                        * NOW BOTH OPERAND'S EXPONENTS ARE EQUAL           FPP0279
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                        280   *                                                                    FPP0280
094     040 A004        281   AEEBE     S     NULL,YD,DR,FR+F      SEE IF A=B, A<B OR A>B         FPP0281
095     0C5 A836        282               A     YD&DR,YD,DR,FR+F+TAKOP+SETGD A+B OR A-B OR B-A     FPP0282
096     410 0082        283               BT    CF,FCARRY                                          FPP0283
097     402 029B        284               BT    NORM,ADD,DONE,CLRCNTR                              FPP0284
098     8C7 B822        285               CNm   SETGD                 SET GUARD BIT                FPP0285
                        286   *                                       (YD8:63)=(DR8:63)=NORMALIZED FRACTION FPP0286
099     0CD 7004        287               S     YD,YD,CNTR,EX+F       ADJUST RESULT EXPONENT       FPP0287
09A     420 0029        288               BT    CE,UNDFLOW                                         FPP0288
09B     0DD C306        289   ADD,DONE    0     YD,YD,ADDSIGN,F+DEOJ QUIT FOR DPFP                 FPP0289
09C     401 0045        290               B     ROUND                                              FPP0290
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FIX REGISTER & FLOAT REGISTER

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09D                     292             ORG   'A0'                                                    FPP0292
                        293     *                                                                     FPP0293
                        294     * FIX REGISTER : FXR(2E),FXDR(3E)                                     FPP0294
                        295     *                                                                     FPP0295
                        296     *                                                                     FPP0296
                        297     * COME HERE IF FPP IS STRAPPED FOR 32 BIT PROCESSOR                   FPP0297
                        298     *                                                                     FPP0298
0A0   098 E800          299     FXR     L     DR,YS             (DR) = FP NUMBER TO BE FIXED        FPP0299
0A1   01F 6000          300             L     Q,DR,EX           (01:7) = EXPONENT, (00)=0           FPP0300
0A2   24E 5C04          301             SI    NULL,Q,X48,EX+F                                       FPP0301
0A3   420 05A6          302             BT    CE,FXR1,UCC+SETDR0                                    FPP0302
                        303     *                               SAVE DR SIGN INTO ESIGN & DR0       FPP0303
0A4   480 00C3          304             BT    G,FXR,OV          BRANCH IF EXP GREATER THAN '48'     FPP0304
0A5   400 10C3          305             BT    DR8,FXR,OV                                            FPP0305
0A6   20E 5804          306     FXR1    SI    Q,Q,X40,EX+F                                          FPP0306
0A7   420 00C8          307             BT    CE,FUNDFLOW       UNDERFLOW IF EXP LESS THAN '40'     FPP0307
0A8   680 00C8          308             BF    G,FUNDFLOW        UNDERFLOW IF EXP IS '40'            FPP0308
                        309     *                               (Q) = 1,2,3,4,5,6,7,8               FPP0309
0A9   216 5304          310             RSI   Q,X06,Q,EX+F      (Q) = 5,4,3,2,1,0,-1,-2             FPP0310
                        311     * ROUTINE COMMON TO 16 AND 32 BIT PROCESSORS                          FPP0311
0AA   05A 6400          312     FXR11   L     CNTR,Q,EX         SET UP COUNTER FOR POSSIBLE EQUALIZ. FPP0312
0AB   062 6800          313             CLR   DR,EX             (DR0:7) = 0                         FPP0313
0AC   680 00BD          314             BF    G,FXR4            BRANCH IF (CNTR) = 0                FPP0314
0AD   420 00B0          315             BT    CE,FXR2           BRANCH IF (CNTR) = -1,-2            FPP0315
0AE   A47 9800          316             CEQ   DR,DR,FR          1:5 EQUALIZATION CYCLES             FPP0316
0AF   401 00BD          317             B     FXR4                                                  FPP0317
                        318     *                                                                     FPP0318
0B0   226 5084          319     FXR2    NI    Q,Q,'01',EX+F     SUBTRACT TO DIFFERENCIATE           FPP0319
                        320     *                               BETWEEN (Q 0:8) = -1 OR -2          FPP0320
0B1   018 E000          321             L     Q,YD              SAVE YD IN Q                        FPP0321
0B2   1DF E000          322             LSL   YD,DR             (DR0:7) = 0 ; (DR8:63) = FRACTION   FPP0322
0B3   1DB E000          323             LSL   YD,YD             SHIFT LEFT BY 1                     FPP0323
0B4   1DB E000          324             LSL   YD,YD             *             1                     FPP0324
0B5   1DB E000          325             LSL   YD,YD             *             1                     FPP0325
0B6   480 00BB          326             BT    G,FXR3            BRANCH IF (Q1:7) WAS = -1           FPP0326
0B7   1DB E000          327             LSL   YD,YD             SHIFT LEFT BY 1                     FPP0327
0B8   1DB E000          328             LSL   YD,YD             *             1                     FPP0328
0B9   1DB E000          329             LSL   YD,YD             *             1                     FPP0329
0BA   1DB E000          330             LSL   YD,YD             *             1                     FPP0330
                        331     *                                                                     FPP0331
0BB   05B E800          332     FXR3    L     DR,YD             (DR0:63) = PROPERLY SHIFTED         FPP0332
                        333     *                                        FIXED POINT DATA           FPP0333
0BC   0DA E000          334             L     YD,Q              RESTORE YD                          FPP0334
                        335     *                                                                     FPP0335
                        336     * NOW (DR0) = 0 AND (DR1:63) = FIXED POINT DATA                       FPP0336
                        337     *                                                                     FPP0337
0BD   01F E000          338     FXR4    L     Q,DR              GET FIXED POINT DATA IN Q           FPP0338
0BE   600 20C1          339             BF    DR0,FXR5          BRANCH IF (YS) = POSITIVE NUMBER    FPP0339
0BF   21F 1020          340     FXR44   LI    Q,0,LFR+MOD816                                        FPP0340
0C0   012 E000          341             TWOS  Q,Q               GET FIXED POINT DATA IN 2'S         FPP0341
                        342     *                               COMPLEMENT NOTATION                 FPP0342
0C1   05A E86C          343     FXR5    L     DR,Q,F+RXWAIT     WAIT TILL DR DATA IS TAKEN          FPP0343
                        344     *                               BY HOST PROCESSOR                   FPP0344
0C2   01A E001          345             L     Q,Q,EOJ           THEN SEND CC, QUIT                  FPP0345
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FIX REGISTER & FLOAT REGISTER

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                              346   *                                                                  FPP0346
                              347   FXR.OV    EQU   *                 OVERFLOW DETECTED            FPP0347
 00C3
 00C3   23F D008              348             INVI  Q,0,SETV          OVERFLOW. SET V FLAG         FPP0348
 00C4   226 5F80              349             NI    Q,Q,X7F,EX        (Q 1:63) = ALL ONES          FPP0349
 00C5   400 208F              350             BT    DR0,FXR44         BRANCH IF (YS) = NEGATIVE NUMBER FPP0350
 00C6   05A E86C              351             L     DR,Q,F+RXWAIT     WAIT TILL DR DATA IS TAKEN   FPP0351
 00C7   01A E001              352             L     Q,0,EOJ           THEN SEND CC. QUIT           FPP0352
                              353   *                                                                  FPP0353
 00C8   062 E86C              354   FUNDFLOW  CLR   DR,F+RXWAIT       (DR) = 0, CVGL = 0000        FPP0354
 00C9   01A E001              355             L     Q,0,EOJ                                        FPP0355
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FLOATING POINT PROCESSOR MICROCODE  05-066R00#13          PAGE  10

   FIX REGISTER & FLOAT REGISTER

0CA                      357            ORG   'CC'                                                    FPP0357
                         358   *                                                                       FPP0358
                         359   * FLOAT REGISTER : FLR(2F),FLDR(3F)                                     FPP0359
                         360   *                                                                       FPP0360
                         361   *                                                                       FPP0361
                         362   * COME HERE IF FPP IS STRAPPED FOR 32 BIT PROCESSOR                     FPP0362
                         363   *                                                                       FPP0363
0CC    21F 5B68          364   FLR      LI    Q,X46,EX+RXWAIT    START WITH EXPONENT = '46' = (Q0:7)   FPP0364
0CD    05F E874          365   FLR.COM  L     DR,DR,DRSIGN+F     WAIT TILL 2ND OP IS AVAILABLE         FPP0365
                         366   *                                (DR32:63) = 0                         FPP0366
0CE    620 04D1          367            BF    L,FLR1,UCC         BRANCH IF 2ND OP IS NON-NEGATIVE      FPP0367
0CF    23E 5F80          368            XNORI Q,Q,X7F,EX         NOW EXPONENT = 'C6' (32 BIT)          FPP0368
                         369   *                                             'C2' (16BIT)             FPP0369
                         370   *                                                                       FPP0370
0D0    04F E874          371            TWOS  DR,DR,DRSIGN+F     (DR) = POSITIVE FIXED POINT NUMBER    FPP0371
0D1    600 C0DF          372   FLR1     BF    DRHD0+DRHD1,FLR3   BRANCH IF (DR0:7) = 0                FPP0372
0D2    15F E070          373            LSR   YD,DR,DRSIGN       SHIFT RIGHT BY 1                      FPP0373
0D3    15B E000          374            LSR   YD,YD              *               1                     FPP0374
0D4    15B E000          375            LSR   YD,YD              *               1                     FPP0375
0D5    600 80D8          376            BF    DRHD0,FLR2         BRANCH IF (DR0:3) = 0                 FPP0376
0D6    206 5080          377            AI    Q,Q,'01',EX        NOW EXPONENT = '47' OR 'C7'           FPP0377
0D7    15B E000          378            LSR   YD,YD              SHIFT RIGHT BY 1                      FPP0378
0D8    15B E000          379            LSR   YD,YD              *               1                     FPP0379
0D9    15B E000          380            LSR   YD,YD              *               1                     FPP0380
0DA    15B E000          381            LSR   YD,YD              *               1                     FPP0381
0DB    15B E000          382   FLR2     LSR   YD,YD              (YD8:63) = RESULT FRACTION            FPP0382
0DC    2C6 5080          383            AI    YD,Q,'01',EX       (YD1:7)  = RESULT EXPONENT           FPP0383
0DD    0DB E006          384            L     YD,YD,F+DEOJ       SET G/L FLAG                          FPP0384
0DE    2DF 1001          385            LI    YD,0,LFR+EOJ                                             FPP0384
                         386   *                                                                       FPP0385
0DF    402 00E3          387   FLR3     BT    NORM,FLR4          IF NORMALIZED, BRANCH                 FPP0386
0E0    680 0228          388            BF    G,ZRESLT,CLRCNTR   BRANCH IF (DR8:63) ALSO = 0           FPP0387
0E1    8C7 B800          389            CNM                      1:5 NORMALIZATION CYCLES              FPP0388
                         390   *                                (YD8:63)=(DR8:63)=NORMALIZED FRACTION FPP0389
0E2    00E 7000          391            S     Q,Q,CNTR,EX        (Q1:7) = ADJUSTED RESULT EXPONENT     FPP0390
0E3    0DE E006          392   FLR4     O     YD,Q,DR,F+DEOJ     SET G/L FLAG                          FPP0391
0E4    2DF 1001          393            LI    YD,0,LFR+EOJ                                             FPP0391


0E5                      395            ORG   'EC'                                                    FPP0393
                         396   *                                                                       FPP0394
                         397   * COME HERE IF FPP IS STRAPPED FOR 16 BIT PROCESSOR                     FPP0395
                         398   *                                                                       FPP0396
0EC    21F 5968          399   FLR16    LI    Q,X42,EX+RXWAIT    START WITH EXPONENT = '42' = (Q0:7)   FPP0397
0ED    401 00CD          400            B     FLR.COM                                                  FPP0398
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FIX REGISTER & FLOAT REGISTER

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                                                                                         FPP0400
0EE                          ORG   'F0'                                                  FPP0401
                     *                                                                   FPP0402
                     * COME HERE IF FPP IS STRAPPED FOR 16 BIT PROCESSOR                 FPP0403
                     *                                                                   FPP0404
 00F0                FXR16    EQU   *                                                    FPP0405
0F0    098 E800               L     DR,YS              (DR) = FP NUMBER TO BE FIXED      FPP0406
0F1    01F 6000               L     Q,DR,EX            (Q1:7) = EXPONENT! (Q0) = 0       FPP0407
0F2    24E 5A04               SI    NULL,Q,X44,EX+F                                      FPP0408
0F3    420 05F6               BT    CE,FXR16.A,UCC+SETDRO                                FPP0409
0F4    480 00C3               BT    G,FXR,OV           BRANCH IF EXP GREATER THAN '48'   FPP0410
0F5    400 10C3               BT    DR8,FXR,OV                                           FPP0411
0F6    20E 5804      FXR16.A  SI    Q,Q,X40,EX+F                                         FPP0412
0F7    420 00C8               BT    CE,FUNDFLOW        BRANCH IF EXP IS LESS THAN '40'   FPP0413
0F8    680 00C8               BF    G,FUNDFLOW         OR EQUAL TO '40'                  FPP0414
                     *                                 (Q) = 1,2,3,4                     FPP0415
0F9    216 5104               RSI   Q,X02,Q,EX+F       (+) = 1,0,-1,-2                   FPP0416
0FA    401 00AA               B     FXR11                                                FPP0417
0FB                           END
```

FIX REGISTER & FLOAT REGISTER

NO ERRORS

ADD.DONE	009B	284			
AE	0075				
AEEB	0094	270			
AELBE	008D	267			
AENEBE	0089	236			
AER	0074				
AGB	0018	85			
AOVRFLOW	002D	257			
ARESULT	002B	268			
BRESULT	002C	273			
CE	0011				
CER	0010				
CHKOR	006F	183			
DE	0051				
DER	0050				
DIFFER	0016	80			
DIVSTOP	002A	185	221		
DOVRUND	006C	189			
FCARRY	0082	241	283		
FLR	00CC				
FLR.COM	00CD	400			
FLR1	00D1	367			
FLR16	00EC				
FLR2	00D8	376			
FLR3	00DF	372			
FLR4	00E3	387			
FUNDFLOW	00C8	307	308	414	415
FXR	00A0				
FXR.OV	00C3	304	305	411	412
FXR1	00A6	302			
FXR11	00AA	418			
FXR16	00F0				
FXR16.A	00F6	410			
FXR2	00B0	315			
FXR3	00BB	326			
FXR4	00BD	314	317		
FXR44	00BF	350			
FXR5	00C1	339			
LDONE	000E	59			
LE	0005				
LER	0004				
LME	001D	95			
MDONE	0044	152			
ME	0035				
MER	0034				
MER.0	004D	141			
MOVRFLOW	004A	194	217		
MOVRUND	0049	146			
NEG	0015	81			
NNORM	007D	242			
NUMOK	0064	192			
ROUND	0045	202	290		
STDONE	0027	104			

FIX REGISTER & FLOAT REGISTER

STE	0031					
STME	0021					
STME1	0024	107				
UNDFLOW	0029	65	155	165	251	288
X02	0002	417				
X06	0006	310				
X08	0008					
X40	0010	145	188	216	306	413
X42	0012	399				
X44	0014	409				
X46	0016	364				
X48	0018	301				
X7F	001F	138	186	234	349	368
ZRESLT	0028	60	143	247	388	

PROG= FPPCROM1   ASSEMBLED BY MICROCAL II (32-BIT)

```
                              1          SCRAT                                              FPD0001
 0001                         2   FVERSION EQU   1            F01 : FOR MODEL 8/16 WITH SPFP  FPD0002
                              3          NLSTC                                              FPD0003
                              4          SQCHK                                              FPD0004
                              5   *                                                         FPD0005
                              6   * COPYRIGHT INTERDATA  INC.  NOVEMBER 1976                 FPD0006
                              7   *                                                         FPD0007
                              8   * DHEMA MAHAJAN                                           FPD0008
                              9   *                                                         FPD0009
                             10          PARTS 19-188R00F00,19-188R00F00,19-188R00F00 DUMMY PART #  FPD0010
                             12   * THE DATA IS CONTAINED IN THE FOLLOWING 1K (256X4) ROM CHIPS     FPD0011
                             13   *                                                         FPD0012
                             14   *                                                         FPD0013
 000                         15          IFZ   FVERSION-1                                   FPD0014
                             16          PARTS 19-188R00F17,19-188R00F18                    FPD0015
                             17   *                                                         FPD0016
                             18          ENDC                                               FPD0017
                             22          ENDC                                               FPD0021
                             26          ENDC                                               FPD0025
                             30          ENDC                                               FPD0025
                             31   *                                                         FPD0026
                             32   *                                                         FPD0027
 000                         33          DO    40                                           FPD0028
 000     000 0000            34          DC    0                                            FPD0029
 001     000 0000            34          DC    0                                            FPD0029
 002     000 0000            34          DC    0                                            FPD0029
 003     000 0000            34          DC    0                                            FPD0029
 004     000 0000            34          DC    0                                            FPD0029
 005     000 0000            34          DC    0                                            FPD0029
 006     000 0000            34          DC    0                                            FPD0029
 007     000 0000            34          DC    0                                            FPD0029
 008     000 0000            34          DC    0                                            FPD0029
 009     000 0000            34          DC    0                                            FPD0029
 00A     000 0000            34          DC    0                                            FPD0029
 00B     000 0000            34          DC    0                                            FPD0029
 00C     000 0000            34          DC    0                                            FPD0029
 00D     000 0000            34          DC    0                                            FPD0029
 00E     000 0000            34          DC    0                                            FPD0029
 00F     000 0000            34          DC    0                                            FPD0029
 010     000 0000            34          DC    0                                            FPD0029
 011     000 0000            34          DC    0                                            FPD0029
 012     000 0000            34          DC    0                                            FPD0029
 013     000 0000            34          DC    0                                            FPD0029
 014     000 0000            34          DC    0                                            FPD0029
 015     000 0000            34          DC    0                                            FPD0029
 016     000 0000            34          DC    0                                            FPD0029
 017     000 0000            34          DC    0                                            FPD0029
 018     000 0000            34          DC    0                                            FPD0029
 019     000 0000            34          DC    0                                            FPD0029
 01A     000 0000            34          DC    0                                            FPD0029
 01B     000 0000            34          DC    0                                            FPD0029
 01C     000 0000            34          DC    0                                            FPD0029
 01D     000 0000            34          DC    0
```

```
 01E    000 0000       34          DC    0                                 FPD0029
 01F    000 0000       34          DC    0                                 FPD0029
 020    000 0000       34          DC    0                                 FPD0029
 021    000 0000       34          DC    0                                 FPD0029
 022    000 0000       34          DC    0                                 FPD0029
 023    000 0000       34          DC    0                                 FPD0029
 024    000 0000       34          DC    0                                 FPD0029
 025    000 0000       34          DC    0                                 FPD0029
 026    000 0000       34          DC    0                                 FPD0029
 027    000 0000       34          DC    0                                 FPD0029
 028    000 0006       35          DC    '06'      LER  28                 FPD0030
 029    000 0012       36          DC    '12'      CER  29                 FPD0031
 02A    000 0076       37          DC    '76'      AER  2A                 FPD0032
 02B    000 0076       38          DC    '76'      SER  2B                 FPD0033
 02C    000 0036       39          DC    '36'      MER  2C                 FPD0034
 02D    000 0052       40          DC    '52'      DER  2D                 FPD0035
                       44          ELSE                                    FPD0039
 02E    000 00F2       45          DC    'F2'      FXR  2E   MODEL 8/16    FPD0040
 02F    000 00EE       46          DC    'EE'      FLR  2F   MODEL 8/16    FPD0041
                       47          ENDC                                    FPD0042
 030                   48          DO    8                                 FPD0043
 030    000 0000       49          DC    0                                 FPD0044
 031    000 0000       49          DC    0                                 FPD0044
 032    000 0000       49          DC    0                                 FPD0044
 033    000 0000       49          DC    0                                 FPD0044
 034    000 0000       49          DC    0                                 FPD0044
 035    000 0000       49          DC    0                                 FPD0044
 036    000 0000       49          DC    0                                 FPD0044
 037    000 0000       49          DC    0                                 FPD0044
                       57          ENDC                                    FPD0052
                       61          ENDC                                    FPD0056
                       65          ENDC                                    FPD0060
                       68          ELSE                                    FPD0063
 038                   69          DO    8                                 FPD0064
 038    000 0000       70          DC    0                                 FPD0065
 039    000 0000       70          DC    0                                 FPD0065
 03A    000 0000       70          DC    0                                 FPD0065
 03B    000 0000       70          DC    0                                 FPD0065
 03C    000 0000       70          DC    0                                 FPD0065
 03D    000 0000       70          DC    0                                 FPD0065
 03E    000 0000       70          DC    0                                 FPD0065
 03F    000 0000       70          DC    0                                 FPD0065
                       71          ENDC                                    FPD0066
                       72     *                                            FPD0067
 040                   73          DO    32                                FPD0068
 040    000 0000       74          DC    0                                 FPD0069
 041    000 0000       74          DC    0                                 FPD0069
 042    000 0000       74          DC    0                                 FPD0069
 043    000 0000       74          DC    0                                 FPD0069
 044    000 0000       74          DC    0                                 FPD0069
 045    000 0000       74          DC    0                                 FPD0069
 046    000 0000       74          DC    0                                 FPD0069
 047    000 0000       74          DC    0                                 FPD0069
 048    000 0000       74          DC    0                                 FPD0069
 049    000 0000       74          DC    0                                 FPD0069
 04A    000 0000       74          DC    0                                 FPD0069
```

```
04B     000 0000                74              DC      0                                       FPD0069
04C     000 0000                74              DC      0                                       FPD0069
04D     000 0000                74              DC      0                                       FPD0069
04E     000 0000                74              DC      0                                       FPD0069
04F     000 0000                74              DC      0                                       FPD0069
050     000 0000                74              DC      0                                       FPD0069
051     000 0000                74              DC      0                                       FPD0069
052     000 0000                74              DC      0                                       FPD0069
053     000 0000                74              DC      0                                       FPD0069
054     000 0000                74              DC      0                                       FPD0069
055     000 0000                74              DC      0                                       FPD0069
056     000 0000                74              DC      0                                       FPD0069
057     000 0000                74              DC      0                                       FPD0069
058     000 0000                74              DC      0                                       FPD0069
059     000 0000                74              DC      0                                       FPD0069
05A     000 0000                74              DC      0                                       FPD0069
05B     000 0000                74              DC      0                                       FPD0069
05C     000 0000                74              DC      0                                       FPD0069
05D     000 0000                74              DC      0                                       FPD0069
05E     000 0000                74              DC      0                                       FPD0069
05F     000 0000                74              DC      0                                       FPD0070
                                75      *                                                       FPD0071
060     000 0032                76              DC      '32'            STE     60              FPD0072
061                             77              DO      7                                       FPD0073
061     000 0000                78              DC      0                                       FPD0073
062     000 0000                78              DC      0                                       FPD0073
063     000 0000                78              DC      0                                       FPD0073
064     000 0000                78              DC      0                                       FPD0073
065     000 0000                78              DC      0                                       FPD0073
066     000 0000                78              DC      0                                       FPD0073
067     000 0000                78              DC      0                                       FPD0074
                                79      *                                                       FPD0075
068     000 0006                80              DC      '06'            LE      68              FPD0076
069     000 0012                81              DC      '12'            CE      69              FPD0077
06A     000 0076                82              DC      '76'            AE      6A              FPD0078
06B     000 0076                83              DC      '76'            SE      6B              FPD0079
06C     000 0036                84              DC      '36'            ME      6C              FPD0080
06D     000 0052                85              DC      '52'            DE      6D              FPD0081
06E     000 0000                86              DC      0                                       FPD0082
06F     000 0000                87              DC      0                                       FPD0083
                                88      *                                                       FPD0086
                                91              ELSE                                            FPD0087
070     000 0000                92              DC      0                                       FPD0088
                                93              ENDC                                            FPD0089
071     000 0022                94              DC      '22'            STME    71              FPD0090
072     000 001E                95              DC      '1E'            LME     72              FPD0091
073                             96              DO      5                                       FPD0092
073     000 0000                97              DC      0                                       FPD0092
074     000 0000                97              DC      0                                       FPD0092
075     000 0000                97              DC      0                                       FPD0092
076     000 0000                97              DC      0                                       FPD0092
077     000 0000                97              DC      0                                       FPD0093
                                98      *                                                       FPD0103
                               108              ELSE                                            FPD0104
078                            109              DO      8                                       FPD0105
078     000 0000               110              DC      0
```

```
079     000 0000            110             DC      0                       FPD0105
07A     000 0000            110             DC      0                       FPD0105
07B     000 0000            110             DC      0                       FPD0105
07C     000 0000            110             DC      0                       FPD0105
07D     000 0000            110             DC      0                       FPD0105
07E     000 0000            110             DC      0                       FPD0105
07F     000 0000            110             DC      0                       FPD0105
                            111             ENDC                            FPD0105
                            112     *                                       FPD0106
080                         113             DO      128                     FPD0107
080     000 0000            114             DC      0                       FPD0108
081     000 0000            114             DC      0                       FPD0109
082     000 0000            114             DC      0                       FPD0109
083     000 0000            114             DC      0                       FPD0109
084     000 0000            114             DC      0                       FPD0109
085     000 0000            114             DC      0                       FPD0109
086     000 0000            114             DC      0                       FPD0109
087     000 0000            114             DC      0                       FPD0109
088     000 0000            114             DC      0                       FPD0109
089     000 0000            114             DC      0                       FPD0109
08A     000 0000            114             DC      0                       FPD0109
08B     000 0000            114             DC      0                       FPD0109
08C     000 0000            114             DC      0                       FPD0109
08D     000 0000            114             DC      0                       FPD0109
08E     000 0000            114             DC      0                       FPD0109
08F     000 0000            114             DC      0                       FPD0109
090     000 0000            114             DC      0                       FPD0109
091     000 0000            114             DC      0                       FPD0109
092     000 0000            114             DC      0                       FPD0109
093     000 0000            114             DC      0                       FPD0109
094     000 0000            114             DC      0                       FPD0109
095     000 0000            114             DC      0                       FPD0109
096     000 0000            114             DC      0                       FPD0109
097     000 0000            114             DC      0                       FPD0109
098     000 0000            114             DC      0                       FPD0109
099     000 0000            114             DC      0                       FPD0109
09A     000 0000            114             DC      0                       FPD0109
09B     000 0000            114             DC      0                       FPD0109
09C     000 0000            114             DC      0                       FPD0109
09D     000 0000            114             DC      0                       FPD0109
09E     000 0000            114             DC      0                       FPD0109
09F     000 0000            114             DC      0                       FPD0109
0A0     000 0000            114             DC      0                       FPD0109
0A1     000 0000            114             DC      0                       FPD0109
0A2     000 0000            114             DC      0                       FPD0109
0A3     000 0000            114             DC      0                       FPD0109
0A4     000 0000            114             DC      0                       FPD0109
0A5     000 0000            114             DC      0                       FPD0109
0A6     000 0000            114             DC      0                       FPD0109
0A7     000 0000            114             DC      0                       FPD0109
0A8     000 0000            114             DC      0                       FPD0109
0A9     000 0000            114             DC      0                       FPD0109
0AA     000 0000            114             DC      0                       FPD0109
0AB     000 0000            114             DC      0                       FPD0109
0AC     000 0000            114             DC      0                       FPD0109
0AD     000 0000            114             DC      0                       FPD0109
```

```
0AE   000 0000   114   DC   0   FPD0109
0AF   000 0000   114   DC   0   FPD0109
0B0   000 0000   114   DC   0   FPD0109
0B1   000 0000   114   DC   0   FPD0109
0B2   000 0000   114   DC   0   FPD0109
0B3   000 0000   114   DC   0   FPD0109
0B4   000 0000   114   DC   0   FPD0109
0B5   000 0000   114   DC   0   FPD0109
0B6   000 0000   114   DC   0   FPD0109
0B7   000 0000   114   DC   0   FPD0109
0B8   000 0000   114   DC   0   FPD0109
0B9   000 0000   114   DC   0   FPD0109
0BA   000 0000   114   DC   0   FPD0109
0BB   000 0000   114   DC   0   FPD0109
0BC   000 0000   114   DC   0   FPD0109
0BD   000 0000   114   DC   0   FPD0109
0BE   000 0000   114   DC   0   FPD0109
0BF   000 0000   114   DC   0   FPD0109
0C0   000 0000   114   DC   0   FPD0109
0C1   000 0000   114   DC   0   FPD0109
0C2   000 0000   114   DC   0   FPD0109
0C3   000 0000   114   DC   0   FPD0109
0C4   000 0000   114   DC   0   FPD0109
0C5   000 0000   114   DC   0   FPD0109
0C6   000 0000   114   DC   0   FPD0109
0C7   000 0000   114   DC   0   FPD0109
0C8   000 0000   114   DC   0   FPD0109
0C9   000 0000   114   DC   0   FPD0109
0CA   000 0000   114   DC   0   FPD0109
0CB   000 0000   114   DC   0   FPD0109
0CC   000 0000   114   DC   0   FPD0109
0CD   000 0000   114   DC   0   FPD0109
0CE   000 0000   114   DC   0   FPD0109
0CF   000 0000   114   DC   0   FPD0109
0D0   000 0000   114   DC   0   FPD0109
0D1   000 0000   114   DC   0   FPD0109
0D2   000 0000   114   DC   0   FPD0109
0D3   000 0000   114   DC   0   FPD0109
0D4   000 0000   114   DC   0   FPD0109
0D5   000 0000   114   DC   0   FPD0109
0D6   000 0000   114   DC   0   FPD0109
0D7   000 0000   114   DC   0   FPD0109
0D8   000 0000   114   DC   0   FPD0109
0D9   000 0000   114   DC   0   FPD0109
0DA   000 0000   114   DC   0   FPD0109
0DB   000 0000   114   DC   0   FPD0109
0DC   000 0000   114   DC   0   FPD0109
0DD   000 0000   114   DC   0   FPD0109
0DE   000 0000   114   DC   0   FPD0109
0DF   000 0000   114   DC   0   FPD0109
0E0   000 0000   114   DC   0   FPD0109
0E1   000 0000   114   DC   0   FPD0109
0E2   000 0000   114   DC   0   FPD0109
0E3   000 0000   114   DC   0   FPD0109
0E4   000 0000   114   DC   0   FPD0109
0E5   000 0000   114   DC   0
```

```
0E6     000 0000        114             DC      0                       FPD0109
0E7     000 0000        114             DC      0                       FPD0109
0E8     000 0000        114             DC      0                       FPD0109
0E9     000 0000        114             DC      0                       FPD0109
0EA     000 0000        114             DC      0                       FPD0109
0EB     000 0000        114             DC      0                       FPD0109
0EC     000 0000        114             DC      0                       FPD0109
0ED     000 0000        114             DC      0                       FPD0109
0EE     000 0000        114             DC      0                       FPD0109
0EF     000 0000        114             DC      0                       FPD0109
0F0     000 0000        114             DC      0                       FPD0109
0F1     000 0000        114             DC      0                       FPD0109
0F2     000 0000        114             DC      0                       FPD0109
0F3     000 0000        114             DC      0                       FPD0109
0F4     000 0000        114             DC      0                       FPD0109
0F5     000 0000        114             DC      0                       FPD0109
0F6     000 0000        114             DC      0                       FPD0109
0F7     000 0000        114             DC      0                       FPD0109
0F8     000 0000        114             DC      0                       FPD0109
0F9     000 0000        114             DC      0                       FPD0109
0FA     000 0000        114             DC      0                       FPD0109
0FB     000 0000        114             DC      0                       FPD0109
0FC     000 0000        114             DC      0                       FPD0109
0FD     000 0000        114             DC      0                       FPD0109
0FE     000 0000        114             DC      0                       FPD0109
0FF     000 0000        114             DC      0                       FPD0109
                        115     *                                       FPD0110
100                     116             END                             FPD0111
```

!! ERRORS 3

FVERSION 0002

```
PROG= FPPDROM2     ASSEMBLED BY MICROCAL II  (32-BIT)
                                    1           SCRAT                                                       FPD0001
 0002                               2   FVERSION EQU   2                 F02 : FOR MODEL 8/16 WITH SPFP,DPFP   FPD0002
                                    3           NLSTC                                                       FPD0003
                                    4           SQCHK                                                       FPD0004
                                    5   *                                                                   FPD0005
                                    6   * COPYRIGHT INTERDATA  INC.  NOVEMBER 1976                          FPD0006
                                    7   *                                                                   FPD0007
                                    8   * DHEMA MAHAJAN                                                     FPD0008
                                    9   *                                                                   FPD0009
                                   10           PARTS 19-188R00F00,19-188R00F00,19-188R00F00 DUMMY PART #   FPD0010
                                   11           PARTS 19-188R00F00,19-188R00F00 DUMMY PART #                FPD0010
                                   12   * THE DATA IS CONTAINED IN THE FOLLOWING 1K (256X4) ROM CHIPS       FPD0011
                                   13   *                                                                   FPD0012
                                   14   *                                                                   FPD0013
                                   18           ENDC                                                        FPD0017
 000                               19           IFZ   FVERSION-2                                            FPD0018
                                   20           PARTS 19-188R00F17,19-188R00F19                             FPD0019
                                   21   *                                                                   FPD0020
                                   22           ENDC                                                        FPD0021
                                   26           ENDC                                                        FPD0025
                                   30           ENDC                                                        FPD0025
                                   31   *                                                                   FPD0026
                                   32   *                                                                   FPD0027
 000                               33           DO     40                                                   FPD0028
 000     000 0000                  34           DC     0                                                    FPD0029
 001     000 0000                  34           DC     0                                                    FPD0029
 002     000 0000                  34           DC     0                                                    FPD0029
 003     000 0000                  34           DC     0                                                    FPD0029
 004     000 0000                  34           DC     0                                                    FPD0029
 005     000 0000                  34           DC     0                                                    FPD0029
 006     000 0000                  34           DC     0                                                    FPD0029
 007     000 0000                  34           DC     0                                                    FPD0029
 008     000 0000                  34           DC     0                                                    FPD0029
 009     000 0000                  34           DC     0                                                    FPD0029
 00A     000 0000                  34           DC     0                                                    FPD0029
 00B     000 0000                  34           DC     0                                                    FPD0029
 00C     000 0000                  34           DC     0                                                    FPD0029
 00D     000 0000                  34           DC     0                                                    FPD0029
 00E     000 0000                  34           DC     0                                                    FPD0029
 00F     000 0000                  34           DC     0                                                    FPD0029
 010     000 0000                  34           DC     0                                                    FPD0029
 011     000 0000                  34           DC     0                                                    FPD0029
 012     000 0000                  34           DC     0                                                    FPD0029
 013     000 0000                  34           DC     0                                                    FPD0029
 014     000 0000                  34           DC     0                                                    FPD0029
 015     000 0000                  34           DC     0                                                    FPD0029
 016     000 0000                  34           DC     0                                                    FPD0029
 017     000 0000                  34           DC     0                                                    FPD0029
 018     000 0000                  34           DC     0                                                    FPD0029
 019     000 0000                  34           DC     0                                                    FPD0029
 01A     000 0000                  34           DC     0                                                    FPD0029
 01B     000 0000                  34           DC     0                                                    FPD0029
 01C     000 0000                  34           DC     0                                                    FPD0029
 01D     000 0000                  34           DC     0
```

```
    01E    000 0000          34          DC    0                                    FPD0029
    01F    000 0000          34          DC    0                                    FPD0029
    020    000 0000          34          DC    0                                    FPD0029
    021    000 0000          34          DC    0                                    FPD0029
    022    000 0000          34          DC    0                                    FPD0029
    023    000 0000          34          DC    0                                    FPD0029
    024    000 0000          34          DC    0                                    FPD0029
    025    000 0000          34          DC    0                                    FPD0029
    026    000 0000          34          DC    0                                    FPD0029
    027    000 0000          34          DC    0                                    FPD0029
    028    000 0006          35          DC    '06'          LER  28                FPD0030
    029    000 0012          36          DC    '12'          CER  29                FPD0031
                             37
**  S001  **
                             38
**  S001  **
                             39
**  S001  **
    02A    000 0076          40          DC    '76'          AER  2A                FPD0032
    02B    000 0076          41          DC    '76'          SER  2B                FPD0033
    02C    000 0036          42          DC    '36'          MER  2C                FPD0034
    02D    000 0052          43          DC    '52'          DER  2D                FPD0035
                             47          ELSE                                       FPD0039
    02E    000 00F2          48          DC    'F2'          FXR  2E   MODEL 8/16    FPD0040
    02F    000 00EE          49          DC    'EE'          FLR  2F   MODEL 8/16    FPD0041
                             50          ENDC                                       FPD0042
    030                      51          DO    8                                    FPD0043
    030    000 0000          52          DC    0                                    FPD0044
    031    000 0000          52          DC    0                                    FPD0044
    032    000 0000          52          DC    0                                    FPD0044
    033    000 0000          52          DC    0                                    FPD0044
    034    000 0000          52          DC    0                                    FPD0044
    035    000 0000          52          DC    0                                    FPD0044
    036    000 0000          52          DC    0                                    FPD0044
    037    000 0000          52          DC    0                                    FPD0044
    038                      53          IFP   FVERSION&2                           FPD0045
    038    000 0007          54          DC    '07'          LDR  38                FPD0046
    039    000 0013          55          DC    '13'          CDR  39                FPD0047
    03A    000 0077          56          DC    '77'          ADR  3A                FPD0048
    03B    000 0077          57          DC    '77'          SDR  3B                FPD0049
    03C    000 0037          58          DC    '37'          MDR  3C                FPD0050
    03D    000 0053          59          DC    '53'          DDR  3D                FPD0051
                             60          ENDC                                       FPD0052
                             64          ENDC                                       FPD0056
    03E                      65          IFZ   FVERSION-2                           FPD0057
    03E    000 00F3          66          DC    'F3'          FXDR 3E   MODEL 8/16    FPD0058
    03F    000 00EF          67          DC    'EF'          FLDR 3F   MODEL 8/16    FPD0059
                             68          ENDC                                       FPD0060
    040                      69          IFP   FVERSION&2                           FPD0061
                             70    *                                                FPD0062
                             74          ENDC                                       FPD0066
                             75    *                                                FPD0067
    040                      76          DO    32                                   FPD0068
    040    000 0000          77          DC    0                                    FPD0069
    041    000 0000          77          DC    0                                    FPD0069
    042    000 0000          77          DC    0                                    FPD0069
```

```
043   000 0000     77         DC    0                          FPD0069
044   000 0000     77         DC    0                          FPD0069
045   000 0000     77         DC    0                          FPD0069
046   000 0000     77         DC    0                          FPD0069
047   000 0000     77         DC    0                          FPD0069
048   000 0000     77         DC    0                          FPD0069
049   000 0000     77         DC    0                          FPD0069
04A   000 0000     77         DC    0                          FPD0069
04B   000 0000     77         DC    0                          FPD0069
04C   000 0000     77         DC    0                          FPD0069
04D   000 0000     77         DC    0                          FPD0069
04E   000 0000     77         DC    0                          FPD0069
04F   000 0000     77         DC    0                          FPD0069
050   000 0000     77         DC    0                          FPD0069
051   000 0000     77         DC    0                          FPD0069
052   000 0000     77         DC    0                          FPD0069
053   000 0000     77         DC    0                          FPD0069
054   000 0000     77         DC    0                          FPD0069
055   000 0000     77         DC    0                          FPD0069
056   000 0000     77         DC    0                          FPD0069
057   000 0000     77         DC    0                          FPD0069
058   000 0000     77         DC    0                          FPD0069
059   000 0000     77         DC    0                          FPD0069
05A   000 0000     77         DC    0                          FPD0069
05B   000 0000     77         DC    0                          FPD0069
05C   000 0000     77         DC    0                          FPD0069
05D   000 0000     77         DC    0                          FPD0069
05E   000 0000     77         DC    0                          FPD0069
05F   000 0000     77         DC    0                          FPD0069
                   78    *                                     FPD0070
060   000 0032     79         DC    '32'          STE   60     FPD0071
061                80         DO    7                          FPD0072
061   000 0000     81         DC    0                          FPD0073
062   000 0000     81         DC    0                          FPD0073
063   000 0000     81         DC    0                          FPD0073
064   000 0000     81         DC    0                          FPD0073
065   000 0000     81         DC    0                          FPD0073
066   000 0000     81         DC    0                          FPD0073
067   000 0000     81         DC    0                          FPD0073
                   82    *                                     FPD0074
068   000 0006     83         DC    '06'          LE    68     FPD0075
069   000 0012     84         DC    '12'          CE    69     FPD0076
06A   000 0076     85         DC    '76'          AE    6A     FPD0077
06B   000 0076     86         DC    '76'          SE    6B     FPD0078
06C   000 0036     87         DC    '36'          ME    6C     FPD0079
06D   000 0052     88         DC    '52'          DE    6D     FPD0080
06E   000 0000     89         DC    0                          FPD0081
06F   000 0000     90         DC    0                          FPD0082
                   91    *                                     FPD0083
070                92         IFP   FVERSION&2                 FPD0084
070   000 0033     93         DC    '33'          STD   70     FPD0085
                   96         ENDC                             FPD0088
071   000 0022     97         DC    '22'          STME  71     FPD0089
072   000 001E     98         DC    '1E'          LME   72     FPD0090
073                99         DO    5                          FPD0091
073   000 0000    100         DC    0                          FPD0092
```

```
074    000 0000        100            DC     0                                          FPD0092
075    000 0000        100            DC     0                                          FPD0092
076    000 0000        100            DC     0                                          FPD0092
077    000 0000        100            DC     0                                          FPD0092
                       101      *                                                       FPD0093
078                    102            IFP    FVERSION&2                                 FPD0094
078    000 0007        103            DC     '07'                 LD    78              FPD0095
079    000 0013        104            DC     '13'                 CD    79              FPD0096
07A    000 0077        105            DC     '77'                 AD    7A              FPD0097
07B    000 0077        106            DC     '77'                 SD    7B              FPD0098
07C    000 0037        107            DC     '37'                 MD    7C              FPD0099
07D    000 0053        108            DC     '53'                 DD    7D              FPD0100
07E    000 0023        109            DC     '23'                 STMD  7E              FPD0101
07F    000 001F        110            DC     '1F'                 LMD   7F              FPD0102
                       114            ENDC                                              FPD0106
                       115      *                                                       FPD0107
080                    116            DO     128                                        FPD0108
080    000 0000        117            DC     0                                          FPD0109
081    000 0000        117            DC     0                                          FPD0109
082    000 0000        117            DC     0                                          FPD0109
083    000 0000        117            DC     0                                          FPD0109
084    000 0000        117            DC     0                                          FPD0109
085    000 0000        117            DC     0                                          FPD0109
086    000 0000        117            DC     0                                          FPD0109
087    000 0000        117            DC     0                                          FPD0109
088    000 0000        117            DC     0                                          FPD0109
089    000 0000        117            DC     0                                          FPD0109
08A    000 0000        117            DC     0                                          FPD0109
08B    000 0000        117            DC     0                                          FPD0109
08C    000 0000        117            DC     0                                          FPD0109
08D    000 0000        117            DC     0                                          FPD0109
08E    000 0000        117            DC     0                                          FPD0109
08F    000 0000        117            DC     0                                          FPD0109
090    000 0000        117            DC     0                                          FPD0109
091    000 0000        117            DC     0                                          FPD0109
092    000 0000        117            DC     0                                          FPD0109
093    000 0000        117            DC     0                                          FPD0109
094    000 0000        117            DC     0                                          FPD0109
095    000 0000        117            DC     0                                          FPD0109
096    000 0000        117            DC     0                                          FPD0109
097    000 0000        117            DC     0                                          FPD0109
098    000 0000        117            DC     0                                          FPD0109
099    000 0000        117            DC     0                                          FPD0109
09A    000 0000        117            DC     0                                          FPD0109
09B    000 0000        117            DC     0                                          FPD0109
09C    000 0000        117            DC     0                                          FPD0109
09D    000 0000        117            DC     0                                          FPD0109
09E    000 0000        117            DC     0                                          FPD0109
09F    000 0000        117            DC     0                                          FPD0109
0A0    000 0000        117            DC     0                                          FPD0109
0A1    000 0000        117            DC     0                                          FPD0109
0A2    000 0000        117            DC     0                                          FPD0109
0A3    000 0000        117            DC     0                                          FPD0109
0A4    000 0000        117            DC     0                                          FPD0109
0A5    000 0000        117            DC     0                                          FPD0109
0A6    000 0000        117            DC     0                                          FPD0109
```

0A7	000 0000	117	DC	0	FPD0109
0A8	000 0000	117	DC	0	FPD0109
0A9	000 0000	117	DC	0	FPD0109
0AA	000 0000	117	DC	0	FPD0109
0AB	000 0000	117	DC	0	FPD0109
0AC	000 0000	117	DC	0	FPD0109
0AD	000 0000	117	DC	0	FPD0109
0AE	000 0000	117	DC	0	FPD0109
0AF	000 0000	117	DC	0	FPD0109
0B0	000 0000	117	DC	0	FPD0109
0B1	000 0000	117	DC	0	FPD0109
0B2	000 0000	117	DC	0	FPD0109
0B3	000 0000	117	DC	0	FPD0109
0B4	000 0000	117	DC	0	FPD0109
0B5	000 0000	117	DC	0	FPD0109
0B6	000 0000	117	DC	0	FPD0109
0B7	000 0000	117	DC	0	FPD0109
0B8	000 0000	117	DC	0	FPD0109
0B9	000 0000	117	DC	0	FPD0109
0BA	000 0000	117	DC	0	FPD0109
0BB	000 0000	117	DC	0	FPD0109
0BC	000 0000	117	DC	0	FPD0109
0BD	000 0000	117	DC	0	FPD0109
0BE	000 0000	117	DC	0	FPD0109
0BF	000 0000	117	DC	0	FPD0109
0C0	000 0000	117	DC	0	FPD0109
0C1	000 0000	117	DC	0	FPD0109
0C2	000 0000	117	DC	0	FPD0109
0C3	000 0000	117	DC	0	FPD0109
0C4	000 0000	117	DC	0	FPD0109
0C5	000 0000	117	DC	0	FPD0109
0C6	000 0000	117	DC	0	FPD0109
0C7	000 0000	117	DC	0	FPD0109
0C8	000 0000	117	DC	0	FPD0109
0C9	000 0000	117	DC	0	FPD0109
0CA	000 0000	117	DC	0	FPD0109
0CB	000 0000	117	DC	0	FPD0109
0CC	000 0000	117	DC	0	FPD0109
0CD	000 0000	117	DC	0	FPD0109
0CE	000 0000	117	DC	0	FPD0109
0CF	000 0000	117	DC	0	FPD0109
0D0	000 0000	117	DC	0	FPD0109
0D1	000 0000	117	DC	0	FPD0109
0D2	000 0000	117	DC	0	FPD0109
0D3	000 0000	117	DC	0	FPD0109
0D4	000 0000	117	DC	0	FPD0109
0D5	000 0000	117	DC	0	FPD0109
0D6	000 0000	117	DC	0	FPD0109
0D7	000 0000	117	DC	0	FPD0109
0D8	000 0000	117	DC	0	FPD0109
0D9	000 0000	117	DC	0	FPD0109
0DA	000 0000	117	DC	0	FPD0109
0DB	000 0000	117	DC	0	FPD0109
0DC	000 0000	117	DC	0	FPD0109
0DD	000 0000	117	DC	0	FPD0109
0DE	000 0000	117	DC	0	FPD0109

```
0DF     000 0000            117             DC      0                       FPD0109
0E0     000 0000            117             DC      0                       FPD0109
0E1     000 0000            117             DC      0                       FPD0109
0E2     000 0000            117             DC      0                       FPD0109
0E3     000 0000            117             DC      0                       FPD0109
0E4     000 0000            117             DC      0                       FPD0109
0E5     000 0000            117             DC      0                       FPD0109
0E6     000 0000            117             DC      0                       FPD0109
0E7     000 0000            117             DC      0                       FPD0109
0E8     000 0000            117             DC      0                       FPD0109
0E9     000 0000            117             DC      0                       FPD0109
0EA     000 0000            117             DC      0                       FPD0109
0EB     000 0000            117             DC      0                       FPD0109
0EC     000 0000            117             DC      0                       FPD0109
0ED     000 0000            117             DC      0                       FPD0109
0EE     000 0000            117             DC      0                       FPD0109
0EF     000 0000            117             DC      0                       FPD0109
0F0     000 0000            117             DC      0                       FPD0109
0F1     000 0000            117             DC      0                       FPD0109
0F2     000 0000            117             DC      0                       FPD0109
0F3     000 0000            117             DC      0                       FPD0109
0F4     000 0000            117             DC      0                       FPD0109
0F5     000 0000            117             DC      0                       FPD0109
0F6     000 0000            117             DC      0                       FPD0109
0F7     000 0000            117             DC      0                       FPD0109
0F8     000 0000            117             DC      0                       FPD0109
0F9     000 0000            117             DC      0                       FPD0109
0FA     000 0000            117             DC      0                       FPD0109
0FB     000 0000            117             DC      0                       FPD0109
0FC     000 0000            117             DC      0                       FPD0109
0FD     000 0000            117             DC      0                       FPD0109
0FE     000 0000            117             DC      0                       FPD0109
0FF     000 0000            117             DC      0                       FPD0109
                            118     *                                       FPD0110
100                         119             END                             FPD0111
```

NO ERRORS

FVERSION 0001

PROG= FPPDROM3   ASSEMBLED BY MICROCAL II (32-BIT)

```
                               1             SCRAT                                            FPD0001
 0003                          2      FVERSION EQU   3                F03 : FOR MODEL 7/32    FPD0002
                               3             NLSTC                                            FPD0003
                               4             SQCHK                                            FPD0004
                               5      *                                                       FPD0005
                               6      * COPYRIGHT INTERDATA  INC.  NOVEMBER 1976              FPD0006
                               7      *                                                       FPD0007
                               8      * DHEMA MAHAJAN                                         FPD0008
                               9      *                                                       FPD0009
                              10             PARTS 19-188R00F00,19-188R00F00,19-188R00F00 DUMMY PART #  FPD0010
                              11             PARTS 19-188R00F00,19-188R00F00 DUMMY PART #    FPD0010
                              12      * THE DATA IS CONTAINED IN THE FOLLOWING 1K (256X4) ROM CHIPS  FPD0011
                              13      *                                                       FPD0012
                              14
** S001 **
                              15      *                                                       FPD0013
                              19             ENDC                                             FPD0017
                              23             ENDC                                             FPD0021
                              24             IFZ   FVERSION-3                                 FPD0022
 000                          25             PARTS 19-188R00F20,19-188R00F19                  FPD0023
                              26      *                                                       FPD0024
                              27             ENDC                                             FPD0025
                              31             ENDC                                             FPD0025
                              32      *                                                       FPD0026
                              33      *                                                       FPD0027
 000                          34             DO    40                                         FPD0028
 000      000 0000            35             DC    0                                          FPD0029
 001      000 0000            35             DC    0                                          FPD0029
 002      000 0000            35             DC    0                                          FPD0029
 003      000 0000            35             DC    0                                          FPD0029
 004      000 0000            35             DC    0                                          FPD0029
 005      000 0000            35             DC    0                                          FPD0029
 006      000 0000            35             DC    0                                          FPD0029
 007      000 0000            35             DC    0                                          FPD0029
 008      000 0000            35             DC    0                                          FPD0029
 009      000 0000            35             DC    0                                          FPD0029
 00A      000 0000            35             DC    0                                          FPD0029
 00B      000 0000            35             DC    0                                          FPD0029
 00C      000 0000            35             DC    0                                          FPD0029
 00D      000 0000            35             DC    0                                          FPD0029
 00E      000 0000            35             DC    0                                          FPD0029
 00F      000 0000            35             DC    0                                          FPD0029
 010      000 0000            35             DC    0                                          FPD0029
 011      000 0000            35             DC    0                                          FPD0029
 012      000 0000            35             DC    0                                          FPD0029
 013      000 0000            35             DC    0                                          FPD0029
 014      000 0000            35             DC    0                                          FPD0029
 015      000 0000            35             DC    0                                          FPD0029
 016      000 0000            35             DC    0                                          FPD0029
 017      000 0000            35             DC    0                                          FPD0029
 018      000 0000            35             DC    0                                          FPD0029
 019      000 0000            35             DC    0                                          FPD0029
 01A      000 0000            35             DC    0                                          FPD0029
 01B      000 0000            35             DC    0                                          FPD0029
```

```
01C     000 0000            35              DC      0                                                       FPD0029
01D     000 0000            35              DC      0                                                       FPD0029
01E     000 0000            35              DC      0                                                       FPD0029
01F     000 0000            35              DC      0                                                       FPD0029
020     000 0000            35              DC      0                                                       FPD0029
021     000 0000            35              DC      0                                                       FPD0029
022     000 0000            35              DC      0                                                       FPD0029
023     000 0000            35              DC      0                                                       FPD0029
024     000 0000            35              DC      0                                                       FPD0029
025     000 0000            35              DC      0                                                       FPD0029
026     000 0000            35              DC      0                                                       FPD0029
027     000 0000            35              DC      0                                                       FPD0029
028     000 0006            36              DC      '06'            LER     28                              FPD0030
029     000 0012            37              DC      '12'            CER     29                              FPD0031
02A     000 0076            38              DC      '76'            AER     2A                              FPD0032
02B     000 0076            39              DC      '76'            SER     2B                              FPD0033
02C     000 0036            40              DC      '36'            MER     2C                              FPD0034
02D     000 0052            41              DC      '52'            DER     2D                              FPD0035
02E                         42              IFP     FVERSION-2                                              FPD0036
02E     000 00A2            43              DC      'A2'            FXR     2E      MODEL 7/32              FPD0037
02F     000 00CE            44              DC      'CE'            FLR     2F      MODEL 7/32              FPD0038
                            48              ENDC                                                            FPD0042
030                         49              DO      8                                                       FPD0043
030     000 0000            50              DC      0                                                       FPD0044
031     000 0000            50              DC      0                                                       FPD0044
032     000 0000            50              DC      0                                                       FPD0044
033     000 0000            50              DC      0                                                       FPD0044
034     000 0000            50              DC      0                                                       FPD0044
035     000 0000            50              DC      0                                                       FPD0044
036     000 0000            50              DC      0                                                       FPD0044
037     000 0000            50              DC      0                                                       FPD0044
038                         51              IFP     FVERSION&2                                              FPD0045
038     000 0007            52              DC      '07'            LDR     38                              FPD0046
039     000 0013            53              DC      '13'            CDR     39                              FPD0047
03A     000 0077            54              DC      '77'            ADR     3A                              FPD0048
03B     000 0077            55              DC      '77'            SDR     3B                              FPD0049
03C     000 0037            56              DC      '37'            MDR     3C                              FPD0050
03D     000 0053            57              DC      '53'            DDR     3D                              FPD0051
                            58              ENDC                                                            FPD0052
03E                         59              IFZ     FVERSION-3                                              FPD0053
03E     000 00A3            60              DC      'A3'            FXDR    3E      MODEL 7/32              FPD0054
03F     000 00CF            61              DC      'CF'            FLDR    3F      MODEL 7/32              FPD0055
                            62              ENDC                                                            FPD0056
                            66              ENDC                                                            FPD0060
040                         67              IFP     FVERSION&2                                              FPD0061
                            68      *                                                                       FPD0062
                            72              ENDC                                                            FPD0066
                            73      *                                                                       FPD0067
040                         74              DO      32                                                      FPD0068
040     000 0000            75              DC      0                                                       FPD0069
041     000 0000            75              DC      0                                                       FPD0069
042     000 0000            75              DC      0                                                       FPD0069
043     000 0000            75              DC      0                                                       FPD0069
044     000 0000            75              DC      0                                                       FPD0069
045     000 0000            75              DC      0                                                       FPD0069
046     000 0000            75              DC      0                                                       FPD0069
```

```
047    000 0000         75           DC     0                              FPD0069
048    000 0000         75           DC     0                              FPD0069
049    000 0000         75           DC     0                              FPD0069
04A    000 0000         75           DC     0                              FPD0069
04B    000 0000         75           DC     0                              FPD0069
04C    000 0000         75           DC     0                              FPD0069
04D    000 0000         75           DC     0                              FPD0069
04E    000 0000         75           DC     0                              FPD0069
04F    000 0000         75           DC     0                              FPD0069
050    000 0000         75           DC     0                              FPD0069
051    000 0000         75           DC     0                              FPD0069
052    000 0000         75           DC     0                              FPD0069
053    000 0000         75           DC     0                              FPD0069
054    000 0000         75           DC     0                              FPD0069
055    000 0000         75           DC     0                              FPD0069
056    000 0000         75           DC     0                              FPD0069
057    000 0000         75           DC     0                              FPD0069
058    000 0000         75           DC     0                              FPD0069
059    000 0000         75           DC     0                              FPD0069
05A    000 0000         75           DC     0                              FPD0069
05B    000 0000         75           DC     0                              FPD0069
05C    000 0000         75           DC     0                              FPD0069
05D    000 0000         75           DC     0                              FPD0069
05E    000 0000         75           DC     0                              FPD0069
05F    000 0000         75           DC     0                              FPD0069
                        76    *                                            FPD0070
060    000 0032         77           DC     '32'          STE   60         FPD0071
061                     78           DO     7                              FPD0072
061    000 0000         79           DC     0                              FPD0073
062    000 0000         79           DC     0                              FPD0073
063    000 0000         79           DC     0                              FPD0073
064    000 0000         79           DC     0                              FPD0073
065    000 0000         79           DC     0                              FPD0073
066    000 0000         79           DC     0                              FPD0073
067    000 0000         79           DC     0                              FPD0073
                        80    *                                            FPD0074
068    000 0006         81           DC     '06'          LE    68         FPD0075
069    000 0012         82           DC     '12'          CE    69         FPD0076
06A    000 0076         83           DC     '76'          AE    6A         FPD0077
06B    000 0076         84           DC     '76'          SE    6B         FPD0078
06C    000 0036         85           DC     '36'          ME    6C         FPD0079
06D    000 0052         86           DC     '52'          DE    6D         FPD0080
06E    000 0000         87           DC     0                              FPD0081
06F    000 0000         88           DC     0                              FPD0082
                        89    *                                            FPD0083
070                     90           IFP    FVERSION&2                     FPD0084
070    000 0033         91           DC     '33'          STD   70         FPD0085
                        94           ENDC                                  FPD0088
071    000 0022         95           DC     '22'          STME  71         FPD0089
072    000 001E         96           DC     '1E'          LME   72         FPD0090
073                     97           DO     5                              FPD0091
073    000 0000         98           DC     0                              FPD0092
074    000 0000         98           DC     0                              FPD0092
075    000 0000         98           DC     0                              FPD0092
076    000 0000         98           DC     0                              FPD0092
077    000 0000         98           DC     0                              FPD0092
```

```
                         99    *                                      FPD0093
078                     100         IFP   FVERSION&2                 FPD0094
078     000 0007        101         DC    '07'       LD    78        FPD0095
079     000 0013        102         DC    '13'       CD    79        FPD0096
07A     000 0077        103         DC    '77'       AD    7A        FPD0097
07B     000 0077        104         DC    '77'       SD    7B        FPD0098
07C     000 0037        105         DC    '37'       MD    7C        FPD0099
07D     000 0053        106         DC    '53'       DD    7D        FPD0100
07E     000 0023        107         DC    '23'       STMD  7E        FPD0101
07F     000 001F        108         DC    '1F'       LMD   7F        FPD0102
                        112         ENDC                             FPD0106
                        113    *                                     FPD0107
080                     114         DO    128                        FPD0108
080     000 0000        115         DC    0                          FPD0109
081     000 0000        115         DC    0                          FPD0109
082     000 0000        115         DC    0                          FPD0109
083     000 0000        115         DC    0                          FPD0109
084     000 0000        115         DC    0                          FPD0109
085     000 0000        115         DC    0                          FPD0109
086     000 0000        115         DC    0                          FPD0109
087     000 0000        115         DC    0                          FPD0109
088     000 0000        115         DC    0                          FPD0109
089     000 0000        115         DC    0                          FPD0109
08A     000 0000        115         DC    0                          FPD0109
08B     000 0000        115         DC    0                          FPD0109
08C     000 0000        115         DC    0                          FPD0109
08D     000 0000        115         DC    0                          FPD0109
08E     000 0000        115         DC    0                          FPD0109
08F     000 0000        115         DC    0                          FPD0109
090     000 0000        115         DC    0                          FPD0109
091     000 0000        115         DC    0                          FPD0109
092     000 0000        115         DC    0                          FPD0109
093     000 0000        115         DC    0                          FPD0109
094     000 0000        115         DC    0                          FPD0109
095     000 0000        115         DC    0                          FPD0109
096     000 0000        115         DC    0                          FPD0109
097     000 0000        115         DC    0                          FPD0109
098     000 0000        115         DC    0                          FPD0109
099     000 0000        115         DC    0                          FPD0109
09A     000 0000        115         DC    0                          FPD0109
09B     000 0000        115         DC    0                          FPD0109
09C     000 0000        115         DC    0                          FPD0109
09D     000 0000        115         DC    0                          FPD0109
09E     000 0000        115         DC    0                          FPD0109
09F     000 0000        115         DC    0                          FPD0109
0A0     000 0000        115         DC    0                          FPD0109
0A1     000 0000        115         DC    0                          FPD0109
0A2     000 0000        115         DC    0                          FPD0109
0A3     000 0000        115         DC    0                          FPD0109
0A4     000 0000        115         DC    0                          FPD0109
0A5     000 0000        115         DC    0                          FPD0109
0A6     000 0000        115         DC    0                          FPD0109
0A7     000 0000        115         DC    0                          FPD0109
0A8     000 0000        115         DC    0                          FPD0109
0A9     000 0000        115         DC    0                          FPD0109
0AA     000 0000        115         DC    0                          FPD0109
```

0AB	000 0000	115	DC	0	FPD0109
0AC	000 0000	115	DC	0	FPD0109
0AD	000 0000	115	DC	0	FPD0109
0AE	000 0000	115	DC	0	FPD0109
0AF	000 0000	115	DC	0	FPD0109
0B0	000 0000	115	DC	0	FPD0109
0B1	000 0000	115	DC	0	FPD0109
0B2	000 0000	115	DC	0	FPD0109
0B3	000 0000	115	DC	0	FPD0109
0B4	000 0000	115	DC	0	FPD0109
0B5	000 0000	115	DC	0	FPD0109
0B6	000 0000	115	DC	0	FPD0109
0B7	000 0000	115	DC	0	FPD0109
0B8	000 0000	115	DC	0	FPD0109
0B9	000 0000	115	DC	0	FPD0109
0BA	000 0000	115	DC	0	FPD0109
0BB	000 0000	115	DC	0	FPD0109
0BC	000 0000	115	DC	0	FPD0109
0BD	000 0000	115	DC	0	FPD0109
0BE	000 0000	115	DC	0	FPD0109
0BF	000 0000	115	DC	0	FPD0109
0C0	000 0000	115	DC	0	FPD0109
0C1	000 0000	115	DC	0	FPD0109
0C2	000 0000	115	DC	0	FPD0109
0C3	000 0000	115	DC	0	FPD0109
0C4	000 0000	115	DC	0	FPD0109
0C5	000 0000	115	DC	0	FPD0109
0C6	000 0000	115	DC	0	FPD0109
0C7	000 0000	115	DC	0	FPD0109
0C8	000 0000	115	DC	0	FPD0109
0C9	000 0000	115	DC	0	FPD0109
0CA	000 0000	115	DC	0	FPD0109
0CB	000 0000	115	DC	0	FPD0109
0CC	000 0000	115	DC	0	FPD0109
0CD	000 0000	115	DC	0	FPD0109
0CE	000 0000	115	DC	0	FPD0109
0CF	000 0000	115	DC	0	FPD0109
0D0	000 0000	115	DC	0	FPD0109
0D1	000 0000	115	DC	0	FPD0109
0D2	000 0000	115	DC	0	FPD0109
0D3	000 0000	115	DC	0	FPD0109
0D4	000 0000	115	DC	0	FPD0109
0D5	000 0000	115	DC	0	FPD0109
0D6	000 0000	115	DC	0	FPD0109
0D7	000 0000	115	DC	0	FPD0109
0D8	000 0000	115	DC	0	FPD0109
0D9	000 0000	115	DC	0	FPD0109
0DA	000 0000	115	DC	0	FPD0109
0DB	000 0000	115	DC	0	FPD0109
0DC	000 0000	115	DC	0	FPD0109
0DD	000 0000	115	DC	0	FPD0109
0DE	000 0000	115	DC	0	FPD0109
0DF	000 0000	115	DC	0	FPD0109
0E0	000 0000	115	DC	0	FPD0109
0E1	000 0000	115	DC	0	FPD0109
0E2	000 0000	115	DC	0	FPD0109

```
0E3     000 0000            115             DC    0                   FPD0109
0E4     000 0000            115             DC    0                   FPD0109
0E5     000 0000            115             DC    0                   FPD0109
0E6     000 0000            115             DC    0                   FPD0109
0E7     000 0000            115             DC    0                   FPD0109
0E8     000 0000            115             DC    0                   FPD0109
0E9     000 0000            115             DC    0                   FPD0109
0EA     000 0000            115             DC    0                   FPD0109
0EB     000 0000            115             DC    0                   FPD0109
0EC     000 0000            115             DC    0                   FPD0109
0ED     000 0000            115             DC    0                   FPD0109
0EE     000 0000            115             DC    0                   FPD0109
0EF     000 0000            115             DC    0                   FPD0109
0F0     000 0000            115             DC    0                   FPD0109
0F1     000 0000            115             DC    0                   FPD0109
0F2     000 0000            115             DC    0                   FPD0109
0F3     000 0000            115             DC    0                   FPD0109
0F4     000 0000            115             DC    0                   FPD0109
0F5     000 0000            115             DC    0                   FPD0109
0F6     000 0000            115             DC    0                   FPD0109
0F7     000 0000            115             DC    0                   FPD0109
0F8     000 0000            115             DC    0                   FPD0109
0F9     000 0000            115             DC    0                   FPD0109
0FA     000 0000            115             DC    0                   FPD0109
0FB     000 0000            115             DC    0                   FPD0109
0FC     000 0000            115             DC    0                   FPD0109
0FD     000 0000            115             DC    0                   FPD0109
0FE     000 0000            115             DC    0                   FPD0109
0FF     000 0000            115             DC    0                   FPD0109
                            116     *                                   FPD0110
100                         117             END                         FPD0111
```

!! ERRORS 1

FVERSION 0003

PROG= FPPDROM4   ASSEMBLED BY MICROCAL II (32-BIT)

```
                             1            SCRAT                                             FPD0001
 0004                        2   FVERSION EQU    4             F04 : FOR MODEL 7/32 WITH SPFP   FPD0002
                             3            NLSTC                                             FPD0003
                             4            SQCHK                                             FPD0004
                             5   *                                                          FPD0005
                             6   * COPYRIGHT INTERDATA  INC.  NOVEMBER 1976                 FPD0006
                             7   *                                                          FPD0007
                             8   * DHEMA MAHAJAN                                            FPD0008
                             9   *                                                          FPD0009
                            10            PARTS 19-188R00F00,19-188R00F00,19-188R00F00 DUMMY PART #  FPD0010
                            11            PARTS 19-188R00F00,19-188R00F00 DUMMY PART #      FPD0010
                            12   * THE DATA IS CONTAINED IN THE FOLLOWING 1K (256X4) ROM CHIPS  FPD0011
                            13   *                                                          FPD0012
                            14   *                                                          FPD0013
                            18            ENDC                                              FPD0017
                            22            ENDC                                              FPD0021
                            26            ENDC                                              FPD0025
 000                        27            IFZ   FVERSION-4                                  FPD0025
                            28            PARTS 19-188R00F20,19-188R00F17                   FPD0025
                            29   *                                                          FPD0025
                            30            ENDC                                              FPD0025
                            31   *                                                          FPD0026
                            32   *                                                          FPD0027
 000                        33            DO    40                                          FPD0028
 000     000 0000           34            DC    0                                           FPD0029
 001     000 0000           34            DC    0                                           FPD0029
 002     000 0000           34            DC    0                                           FPD0029
 003     000 0000           34            DC    0                                           FPD0029
 004     000 0000           34            DC    0                                           FPD0029
 005     000 0000           34            DC    0                                           FPD0029
 006     000 0000           34            DC    0                                           FPD0029
 007     000 0000           34            DC    0                                           FPD0029
 008     000 0000           34            DC    0                                           FPD0029
 009     000 0000           34            DC    0                                           FPD0029
 00A     000 0000           34            DC    0                                           FPD0029
 00B     000 0000           34            DC    0                                           FPD0029
 00C     000 0000           34            DC    0                                           FPD0029
 00D     000 0000           34            DC    0                                           FPD0029
 00E     000 0000           34            DC    0                                           FPD0029
 00F     000 0000           34            DC    0                                           FPD0029
 010     000 0000           34            DC    0                                           FPD0029
 011     000 0000           34            DC    0                                           FPD0029
 012     000 0000           34            DC    0                                           FPD0029
 013     000 0000           34            DC    0                                           FPD0029
 014     000 0000           34            DC    0                                           FPD0029
 015     000 0000           34            DC    0                                           FPD0029
 016     000 0000           34            DC    0                                           FPD0029
 017     000 0000           34            DC    0                                           FPD0029
 018     000 0000           34            DC    0                                           FPD0029
 019     000 0000           34            DC    0                                           FPD0029
 01A     000 0000           34            DC    0                                           FPD0029
 01B     000 0000           34            DC    0                                           FPD0029
 01C     000 0000           34            DC    0                                           FPD0029
 01D     000 0000           34            DC    0
```

```
01E     000 0000            34              DC      0                                                       FPD0029
01F     000 0000            34              DC      0                                                       FPD0029
020     000 0000            34              DC      0                                                       FPD0029
021     000 0000            34              DC      0                                                       FPD0029
022     000 0000            34              DC      0                                                       FPD0029
023     000 0000            34              DC      0                                                       FPD0029
024     000 0000            34              DC      0                                                       FPD0029
025     000 0000            34              DC      0                                                       FPD0029
026     000 0000            34              DC      0                                                       FPD0029
027     000 0000            34              DC      0                                                       FPD0029
028     000 0006            35              DC      '06'            LER   28                              FPD0030
029     000 0012            36              DC      '12'            CER   29                              FPD0031
02A     000 0076            37              DC      '76'            AER   2A                              FPD0032
02B     000 0076            38              DC      '76'            SER   2B                              FPD0033
02C     000 0036            39              DC      '36'            MER   2C                              FPD0034
02D     000 0052            40              DC      '52'            DER   2D                              FPD0035
02E                         41              IFP     FVERSION-2                                              FPD0036
02E     000 00A2            42              DC      'A2'            FXR   2E    MODEL 7/32                FPD0037
02F     000 00CE            43              DC      'CE'            FLR   2F    MODEL 7/32                FPD0038
                            47              ENDC                                                            FPD0042
030                         48              DO      8                                                       FPD0043
030     000 0000            49              DC      0                                                       FPD0044
031     000 0000            49              DC      0                                                       FPD0044
032     000 0000            49              DC      0                                                       FPD0044
033     000 0000            49              DC      0                                                       FPD0044
034     000 0000            49              DC      0                                                       FPD0044
035     000 0000            49              DC      0                                                       FPD0044
036     000 0000            49              DC      0                                                       FPD0044
037     000 0000            49              DC      0                                                       FPD0044
                            57              ENDC                                                            FPD0052
                            61              ENDC                                                            FPD0056
                            65              ENDC                                                            FPD0060
                            68              ELSE                                                            FPD0063
038                         69              DO      8                                                       FPD0064
038     000 0000            70              DC      0                                                       FPD0065
039     000 0000            70              DC      0                                                       FPD0065
03A     000 0000            70              DC      0                                                       FPD0065
03B     000 0000            70              DC      0                                                       FPD0065
03C     000 0000            70              DC      0                                                       FPD0065
03D     000 0000            70              DC      0                                                       FPD0065
03E     000 0000            70              DC      0                                                       FPD0065
03F     000 0000            70              DC      0                                                       FPD0065
                            71              ENDC                                                            FPD0066
                            72      *                                                                       FPD0067
040                         73              DO      32                                                      FPD0068
040     000 0000            74              DC      0                                                       FPD0069
041     000 0000            74              DC      0                                                       FPD0069
042     000 0000            74              DC      0                                                       FPD0069
043     000 0000            74              DC      0                                                       FPD0069
044     000 0000            74              DC      0                                                       FPD0069
045     000 0000            74              DC      0                                                       FPD0069
046     000 0000            74              DC      0                                                       FPD0069
047     000 0000            74              DC      0                                                       FPD0069
048     000 0000            74              DC      0                                                       FPD0069
049     000 0000            74              DC      0                                                       FPD0069
04A     000 0000            74              DC      0                                                       FPD0069
```

```
04B   000 0000   74        DC    0                      FPD0069
04C   000 0000   74        DC    0                      FPD0069
04D   000 0000   74        DC    0                      FPD0069
04E   000 0000   74        DC    0                      FPD0069
04F   000 0000   74        DC    0                      FPD0069
050   000 0000   74        DC    0                      FPD0069
051   000 0000   74        DC    0                      FPD0069
052   000 0000   74        DC    0                      FPD0069
053   000 0000   74        DC    0                      FPD0069
054   000 0000   74        DC    0                      FPD0069
055   000 0000   74        DC    0                      FPD0069
056   000 0000   74        DC    0                      FPD0069
057   000 0000   74        DC    0                      FPD0069
058   000 0000   74        DC    0                      FPD0069
059   000 0000   74        DC    0                      FPD0069
05A   000 0000   74        DC    0                      FPD0069
05B   000 0000   74        DC    0                      FPD0069
05C   000 0000   74        DC    0                      FPD0069
05D   000 0000   74        DC    0                      FPD0069
05E   000 0000   74        DC    0                      FPD0069
05F   000 0000   74        DC    0                      FPD0069
                 75   *                                 FPD0070
060   000 0032   76        DC    '32'     STE   60      FPD0071
061              77        DO    7                      FPD0072
061   000 0000   78        DC    0                      FPD0073
062   000 0000   78        DC    0                      FPD0073
063   000 0000   78        DC    0                      FPD0073
064   000 0000   78        DC    0                      FPD0073
065   000 0000   78        DC    0                      FPD0073
066   000 0000   78        DC    0                      FPD0073
067   000 0000   78        DC    0                      FPD0073
                 79   *                                 FPD0074
068   000 0006   80        DC    '06'     LE    68      FPD0075
069   000 0012   81        DC    '12'     CE    69      FPD0076
06A   000 0076   82        DC    '76'     AE    6A      FPD0077
06B   000 0076   83        DC    '76'     SE    6B      FPD0078
06C   000 0036   84        DC    '36'     ME    6C      FPD0079
06D   000 0052   85        DC    '52'     DE    6D      FPD0080
06E   000 0000   86        DC    0                      FPD0081
06F   000 0000   87        DC    0                      FPD0082
                 88   *                                 FPD0083
                 91        ELSE                         FPD0086
070   000 0000   92        DC    0                      FPD0087
                 93        ENDC                         FPD0088
071   000 0022   94        DC    '22'     STME  71      FPD0089
072   000 001E   95        DC    '1E'     LME   72      FPD0090
073              96        DO    5                      FPD0091
073   000 0000   97        DC    0                      FPD0092
074   000 0000   97        DC    0                      FPD0092
075   000 0000   97        DC    0                      FPD0092
076   000 0000   97        DC    0                      FPD0092
077   000 0000   97        DC    0                      FPD0092
                 98   *                                 FPD0093
                108        ELSE                         FPD0103
078             109        DO    8                      FPD0104
078   000 0000  110        DC    0                      FPD0105
```

```
079     000 0000            110             DC      0                       FPD0105
07A     000 0000            110             DC      0                       FPD0105
07B     000 0000            110             DC      0                       FPD0105
07C     000 0000            110             DC      0                       FPD0105
07D     000 0000            110             DC      0                       FPD0105
07E     000 0000            110             DC      0                       FPD0105
07F     000 0000            110             DC      0                       FPD0105
                            111             ENDC                            FPD0106
                            112     *                                       FPD0107
080                         113             DO      128                     FPD0108
080     000 0000            114             DC      0                       FPD0109
081     000 0000            114             DC      0                       FPD0109
082     000 0000            114             DC      0                       FPD0109
083     000 0000            114             DC      0                       FPD0109
084     000 0000            114             DC      0                       FPD0109
085     000 0000            114             DC      0                       FPD0109
086     000 0000            114             DC      0                       FPD0109
087     000 0000            114             DC      0                       FPD0109
088     000 0000            114             DC      0                       FPD0109
089     000 0000            114             DC      0                       FPD0109
08A     000 0000            114             DC      0                       FPD0109
08B     000 0000            114             DC      0                       FPD0109
08C     000 0000            114             DC      0                       FPD0109
08D     000 0000            114             DC      0                       FPD0109
08E     000 0000            114             DC      0                       FPD0109
08F     000 0000            114             DC      0                       FPD0109
090     000 0000            114             DC      0                       FPD0109
091     000 0000            114             DC      0                       FPD0109
092     000 0000            114             DC      0                       FPD0109
093     000 0000            114             DC      0                       FPD0109
094     000 0000            114             DC      0                       FPD0109
095     000 0000            114             DC      0                       FPD0109
096     000 0000            114             DC      0                       FPD0109
097     000 0000            114             DC      0                       FPD0109
098     000 0000            114             DC      0                       FPD0109
099     000 0000            114             DC      0                       FPD0109
09A     000 0000            114             DC      0                       FPD0109
09B     000 0000            114             DC      0                       FPD0109
09C     000 0000            114             DC      0                       FPD0109
09D     000 0000            114             DC      0                       FPD0109
09E     000 0000            114             DC      0                       FPD0109
09F     000 0000            114             DC      0                       FPD0109
0A0     000 0000            114             DC      0                       FPD0109
0A1     000 0000            114             DC      0                       FPD0109
0A2     000 0000            114             DC      0                       FPD0109
0A3     000 0000            114             DC      0                       FPD0109
0A4     000 0000            114             DC      0                       FPD0109
0A5     000 0000            114             DC      0                       FPD0109
0A6     000 0000            114             DC      0                       FPD0109
0A7     000 0000            114             DC      0                       FPD0109
0A8     000 0000            114             DC      0                       FPD0109
0A9     000 0000            114             DC      0                       FPD0109
0AA     000 0000            114             DC      0                       FPD0109
0AB     000 0000            114             DC      0                       FPD0109
0AC     000 0000            114             DC      0                       FPD0109
0AD     000 0000            114             DC      0                       FPD0109
```

```
0AE   000 0000   114   DC   0   FPD0109
0AF   000 0000   114   DC   0   FPD0109
0B0   000 0000   114   DC   0   FPD0109
0B1   000 0000   114   DC   0   FPD0109
0B2   000 0000   114   DC   0   FPD0109
0B3   000 0000   114   DC   0   FPD0109
0B4   000 0000   114   DC   0   FPD0109
0B5   000 0000   114   DC   0   FPD0109
0B6   000 0000   114   DC   0   FPD0109
0B7   000 0000   114   DC   0   FPD0109
0B8   000 0000   114   DC   0   FPD0109
0B9   000 0000   114   DC   0   FPD0109
0BA   000 0000   114   DC   0   FPD0109
0BB   000 0000   114   DC   0   FPD0109
0BC   000 0000   114   DC   0   FPD0109
0BD   000 0000   114   DC   0   FPD0109
0BE   000 0000   114   DC   0   FPD0109
0BF   000 0000   114   DC   0   FPD0109
0C0   000 0000   114   DC   0   FPD0109
0C1   000 0000   114   DC   0   FPD0109
0C2   000 0000   114   DC   0   FPD0109
0C3   000 0000   114   DC   0   FPD0109
0C4   000 0000   114   DC   0   FPD0109
0C5   000 0000   114   DC   0   FPD0109
0C6   000 0000   114   DC   0   FPD0109
0C7   000 0000   114   DC   0   FPD0109
0C8   000 0000   114   DC   0   FPD0109
0C9   000 0000   114   DC   0   FPD0109
0CA   000 0000   114   DC   0   FPD0109
0CB   000 0000   114   DC   0   FPD0109
0CC   000 0000   114   DC   0   FPD0109
0CD   000 0000   114   DC   0   FPD0109
0CE   000 0000   114   DC   0   FPD0109
0CF   000 0000   114   DC   0   FPD0109
0D0   000 0000   114   DC   0   FPD0109
0D1   000 0000   114   DC   0   FPD0109
0D2   000 0000   114   DC   0   FPD0109
0D3   000 0000   114   DC   0   FPD0109
0D4   000 0000   114   DC   0   FPD0109
0D5   000 0000   114   DC   0   FPD0109
0D6   000 0000   114   DC   0   FPD0109
0D7   000 0000   114   DC   0   FPD0109
0D8   000 0000   114   DC   0   FPD0109
0D9   000 0000   114   DC   0   FPD0109
0DA   000 0000   114   DC   0   FPD0109
0DB   000 0000   114   DC   0   FPD0109
0DC   000 0000   114   DC   0   FPD0109
0DD   000 0000   114   DC   0   FPD0109
0DE   000 0000   114   DC   0   FPD0109
0DF   000 0000   114   DC   0   FPD0109
0E0   000 0000   114   DC   0   FPD0109
0E1   000 0000   114   DC   0   FPD0109
0E2   000 0000   114   DC   0   FPD0109
0E3   000 0000   114   DC   0   FPD0109
0E4   000 0000   114   DC   0   FPD0109
0E5   000 0000   114   DC   0   FPD0109
```

```
0E6     000 0000        114             DC      0                       FPD0109
0E7     000 0000        114             DC      0                       FPD0109
0E8     000 0000        114             DC      0                       FPD0109
0E9     000 0000        114             DC      0                       FPD0109
0EA     000 0000        114             DC      0                       FPD0109
0EB     000 0000        114             DC      0                       FPD0109
0EC     000 0000        114             DC      0                       FPD0109
0ED     000 0000        114             DC      0                       FPD0109
0EE     000 0000        114             DC      0                       FPD0109
0EF     000 0000        114             DC      0                       FPD0109
0F0     000 0000        114             DC      0                       FPD0109
0F1     000 0000        114             DC      0                       FPD0109
0F2     000 0000        114             DC      0                       FPD0109
0F3     000 0000        114             DC      0                       FPD0109
0F4     000 0000        114             DC      0                       FPD0109
0F5     000 0000        114             DC      0                       FPD0109
0F6     000 0000        114             DC      0                       FPD0109
0F7     000 0000        114             DC      0                       FPD0109
0F8     000 0000        114             DC      0                       FPD0109
0F9     000 0000        114             DC      0                       FPD0109
0FA     000 0000        114             DC      0                       FPD0109
0FB     000 0000        114             DC      0                       FPD0109
0FC     000 0000        114             DC      0                       FPD0109
0FD     000 0000        114             DC      0                       FPD0109
0FE     000 0000        114             DC      0                       FPD0109
0FF     000 0000        114             DC      0                       FPD0109
                        115     *                                       FPD0110
100                     116             END                             FPD0111
```

NO ERRORS

FVERSION 0004

INTERDATA

...e Oceanport New Jersey 07757

CABLE CONNECTOR MAP

TEST AID CONNECTOR LOCATED ON FPP-A (35-632) ONLY → Conn 4

LOCATED ON BOTH THE 35-632 & 35-633 BOARD → Conn 3, Conn 2

CONN	TERM. NO.	ROW 2	ROW 1
5	16		
5	15		
5	14		
5	13		
5	12		
5	11		
5	10		
5	09		
5	08		
5	07		
5	06		
5	05		
5	04		
5	03		
5	02		
5	01		
5	00		

CONN	TERM. NO.	ROW 1
4	18	RAR030
4	17	RAR040
4	16	RAR050
4	15	RAR070
4	14	RAR060
4	13	RAR020
4	12	GND
4	11	
4	10	RAR000
4	09	XRPZ
4	08	XRPZ
4	07	RAR010
4	06	P5
4	05	GND
4	04	TABCLK0
4	03	ALICE1
4	02	SCLR0A
4	01	P5
4	00	GND

CONN	TERM. NO.	ROW 2	ROW 1
3	16	GND	CLK0
3	15	GND	CMPR081
3	14	NORM1	XNRM1
3	13	SGD1	MPY1
3	12	GND	GDCLK0
3	11	GCPUCLKFR00	IOS01
3	10	IOS11	GND
3	09	GDAT1	DIV0
3	08	EX1	WAIT0
3	07	QGX	QC641
3	06	QOV1	QG1
3	05	QL1	ORBIT11
3	04	GND	DR081
3	03	GND	XY31
3	02	IDLE0	DEC070
3	01	SR071	CCMSEL
3	00	GND	GF08630
2	24	DR071	DR061
2	23	DR051	DR041
2	22	DR031	DR021
2	21	DR011	DR001
2	20	GND	RD031
2	19	[illegible]	RD051
2	18	RD061	FRD071
2	17	FRD081	RD091
2	16	RD101	RD111
2	15		RD140
2	14	FRD150	
2	13	YD11	YD01
2	12	FY501	YD21
2	11	FY521	FY511
2	10	GND	
2	09	GND	P041
2	08	GND	G041
2	07	GND	CN56
2	06	GND	CN041
2	05	GND	DRCLKFR10
2	04	GND	DRCLKFR20
2	03	GND	DRCLKFR30
2	02	GND	DRCLKFR40
2	01	GND	CPUCLKFR00
2	00	GND	CPUCLKFR[illegible]

BACK PANEL MAP

CONN	TERM NO	35-633 FPP-B BOARD ROW 1	35-633 FPP-B BOARD ROW 2	35-632 FPP-A BOARD ROW 1	35-632 FPP-A BOARD ROW 2
1	41	P5	GND	P5	GND
1	40	GND	GND	GND	GND
1	39				
1	38				
1	37				
1	36			MD130	MD140
1	35				MD120
1	34			MD090	MD100
1	33			MD070	MD080
1	32			MD050	MD060
1	31			MD030	MD040
1	30			MD010	MD020
1	29				MD000
1	28				
1	27				
1	26			SCLR0	
1	25			FDECIO	
1	24			FINR0	
1	23			SYN0	
1	22			RACK0	TACK0
1	21				
1	20				
1	19				
1	18	D140	D150	D140	
1	17	D120	D130	D120	D130
1	16	D100	D110	D100	
1	15	D080	D090	D080	D090
1	14	D060	D070	D060	D070
1	13	D040	D050	D040	D050
1	12	D020.	D030	D020	D030
1	11	D000	D010	D000	D010
1	10				
1	09				
1	08				
1	07				
1	06				
1	05				
1	04				
1	03				
1	02				
1	01	GND	GND	GND	GND
1	00	P5	GND	P5	GND
0	41	P5	GND	P5	GND
0	40	GND	GND	GND	GND
0	39				
0	38				
0	37				
0	36				
0	35				
0	34			LDREG0/BCNT0	MD0/BADR0
0	33				
0	32				
0	31				
0	30				
0	29				
0	28				
0	27				
0	26				
0	25				
0	24				
0	23				
0	22				
0	21				
0	20				
0	19				
0	18				
0	17				
0	16				
0	15				
0	14				
0	13				
0	12				
0	11				
0	10				
0	09				
0	08				
0	07				
0	06				
0	05				
0	04				
0	03				
0	02				
0	01	GND	GND	GND	GND
0	00	P5	GND	P5	GND

35-633 FPP-B BOARD

35-632 FPP-A BOARD

REVISIONS

108-3 WAS WAIT1, REVISED SHTS 7, 8, 9, 10, 13, 16, 17, 18, 20 AND 21; RELEASED AS R01.

B G	DJF	03862-02	—	1-6-77	R01

PRE PRODUCTION APPROVAL — INIT DATE — DEV DJF 1/13/77 — PROD

REVISED SHTS 1, 14, 15, 17, 19, 20, & 22. 35-632 F01-F03 WERE R01

JS	[initials]	03862-3		3-2-77	R02

RELEASED FOR PRODUCTION — [redacted]. ENG. DJF DATE 3/4/77

REVISED SHTS 3, 7, 14-22 AREA 9A & 8A, 35-632 F01-F03 WAS R02 ADDED 35-632F04

PM	[initials]	3249		6-16-77	R03

REVISED SHTS 1, 14, 15, 17 & 21. 35-632F01-F03 WAS R03. 35-632F04 WAS R00.

WTA	[initials]	3496		12-21-77	R04

REVISED SHTS 17, 18, 21 35-632 F01-F03 WERE R04 F04 WAS R01 ADDED USED IN MANUAL TABLE

GP	[initials]	3564		3-7-78	R05

REVISED SHT. 19 35-632 F01-F03 WERE R05, F04 WAS R02.

GP	[initials]	3696		5-23-78	R06

USED IN MANUAL 29-568

BOARD	REV LEVEL	SCHEMATIC SHEETS
35-632 F04	R03	3, 7 & 14 THRU 22
35-632 F03	R06	3, 7 & 14 THRU 22
35-633 F02	R01	3 THRU 13
35-633 F01	R02	3 THRU 13
35-632 F02	R06	3, 7 & 14 THRU 22
35-632 F01	R06	3, 7 & 14 THRU 22

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL — COVERED BY THE FOLLOWING SHEETS OF THIS DOCUMENT

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX																							
	REV	06		01				02	01	01	01			01	03	03	02	05	03	04	03	04	02
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22

NOTES:

1. ALL RESISTORS ARE 1/4W 5%

V. PERRI		11-9-76
R. CERO		3-4-77
		3-4-77
R.A. BARKER	Q.A.	1-28-77
D. FRANKENBERGER	MGR.	2-24-77

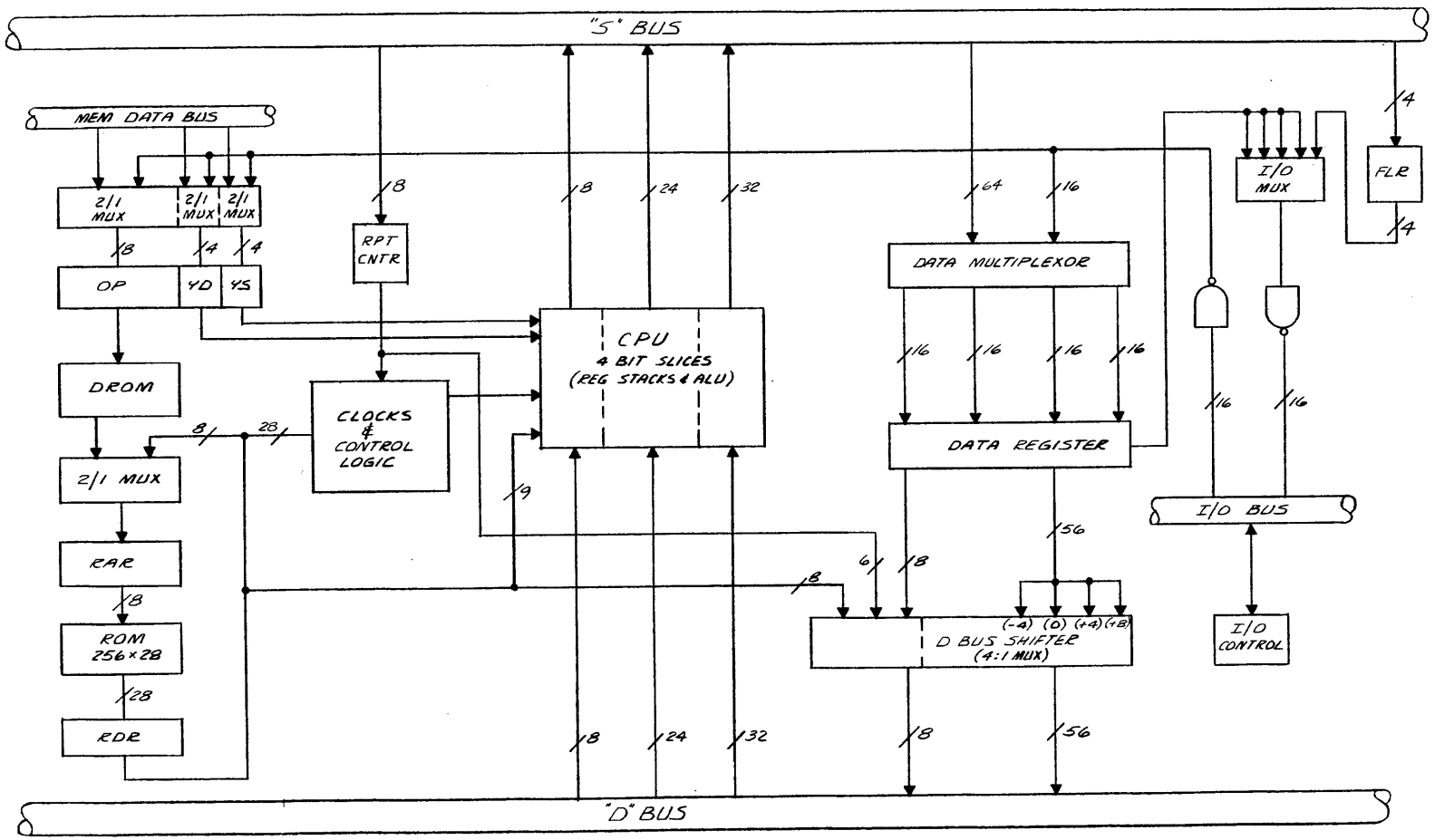
SCHEMATIC FLOATING POINT PROCESSOR

03862

02-449R06D08 1 22

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



FLOATING POINT PROCESSOR BLOCK DIAGRAM

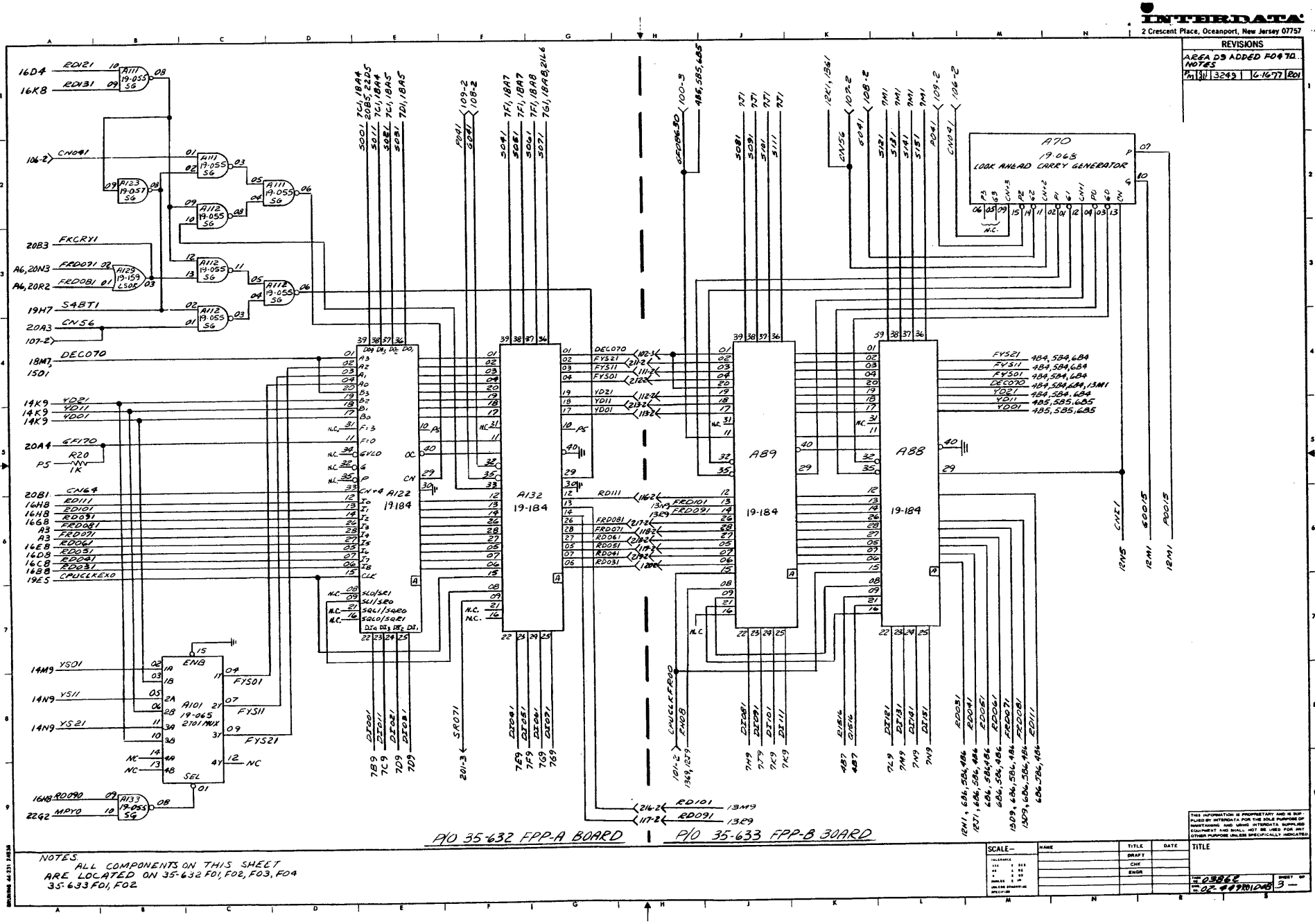
SCALE-

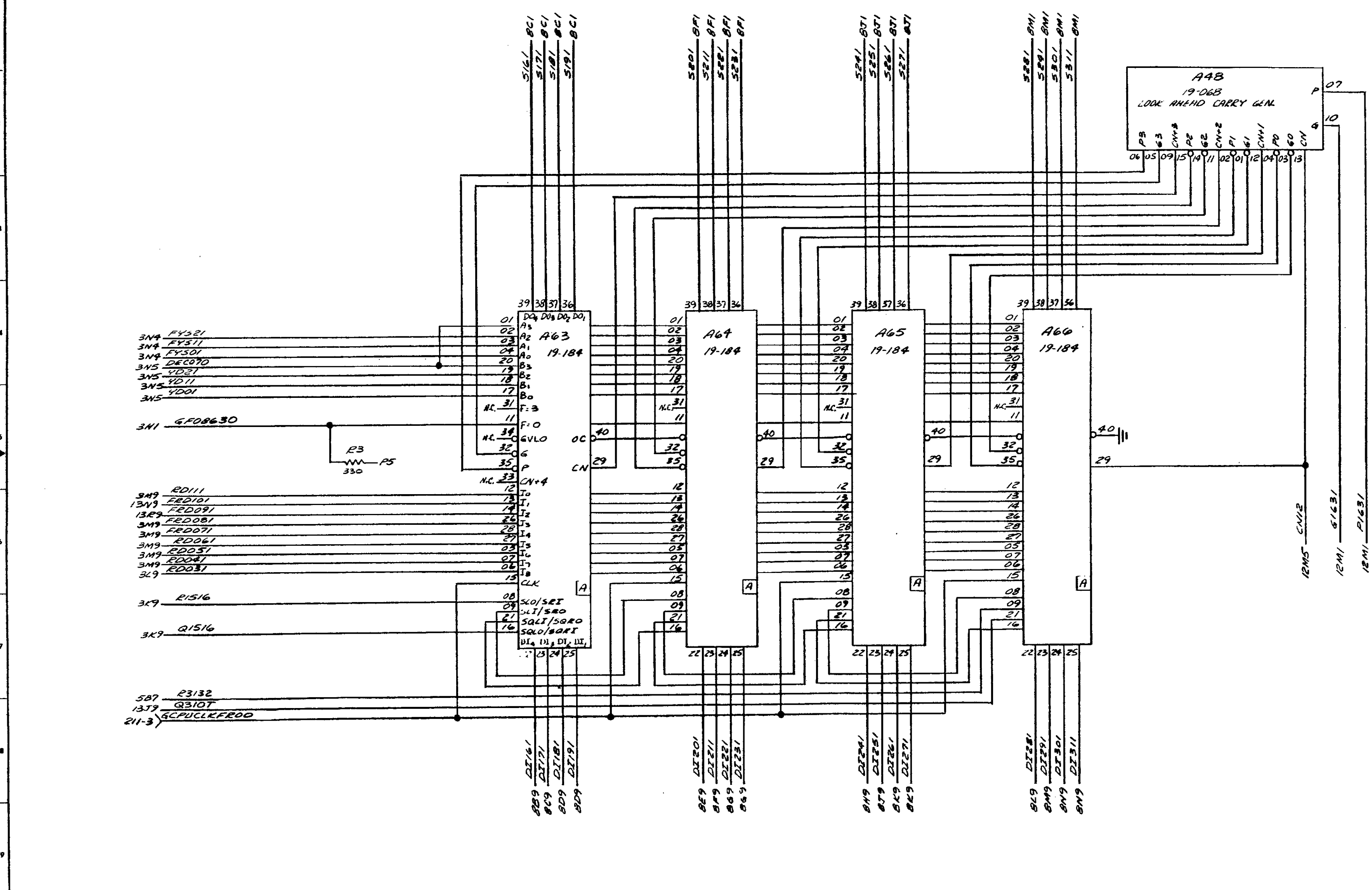
NAME	TITLE	DATE
V. PEZET	DRAFT	11-8-76
	CHK	
	ENGR	

TITLE

03-3262
02-449 D08

SHEET 2 OF —


INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757
REVISIONS
AREA D3 ADDED FOR 70 NOTES
A70 19-065 LOOK AHEAD CARRY GENERATOR
A89 19-184
A88 19-184
A132 19-184
A122 19-184
A101 19-065 2701 MUX
P/O 35-632 FPP-A BOARD
P/O 35-633 FPP-B BOARD
NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02, F03, F04 35-633 F01, F02
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED
SCALE—
NAME
TITLE
DRAFT
CHK
ENGR
DATE
TITLE
03862
SHEET 3
07-49701-03



INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

NOTES:
ALL COMPONENTS ON THIS SHEET
ARE LOCATED ON 35-633 F01 & F02

SCALE –

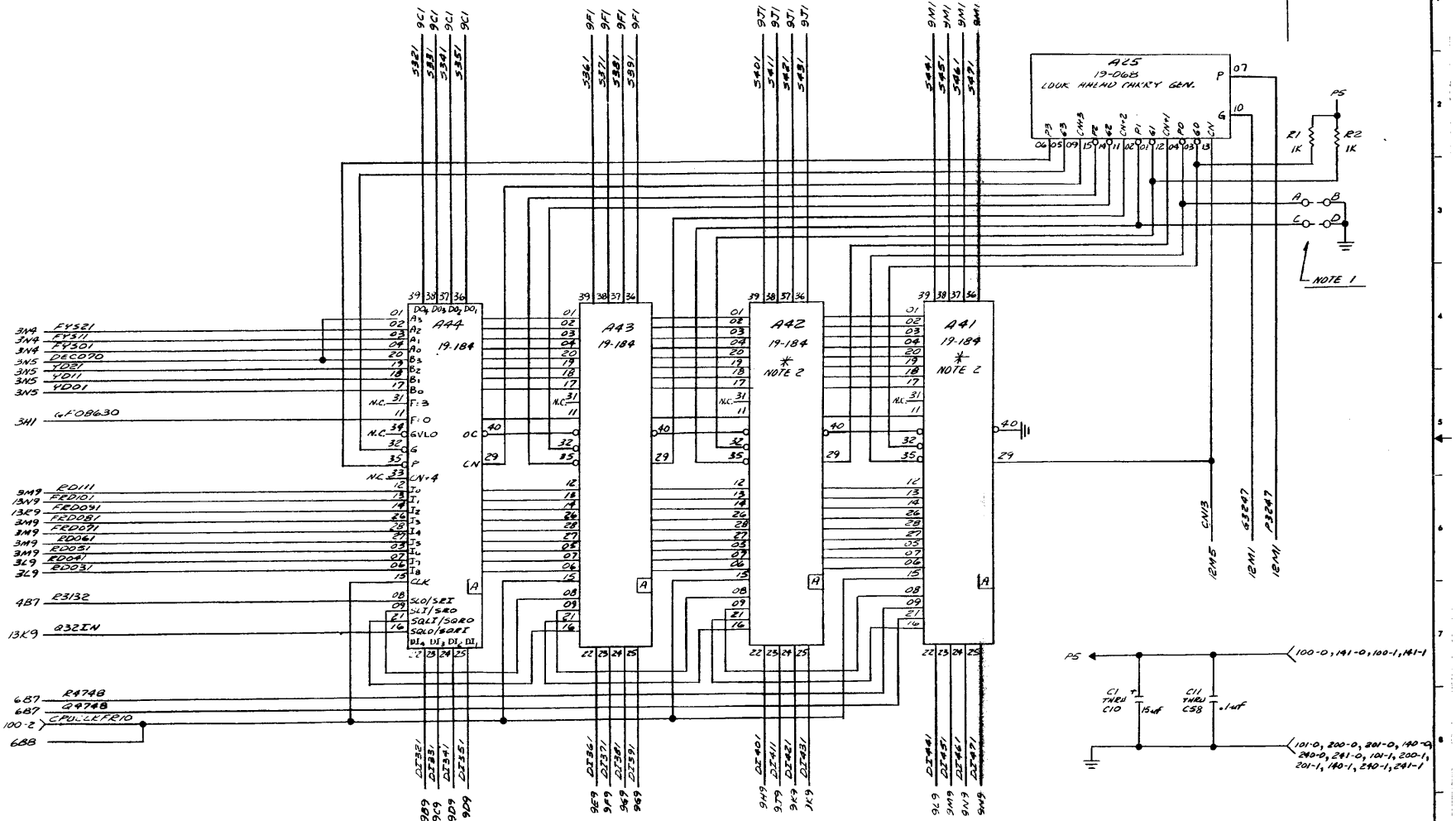
TITLE

02-449 D08

SHEET 4

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



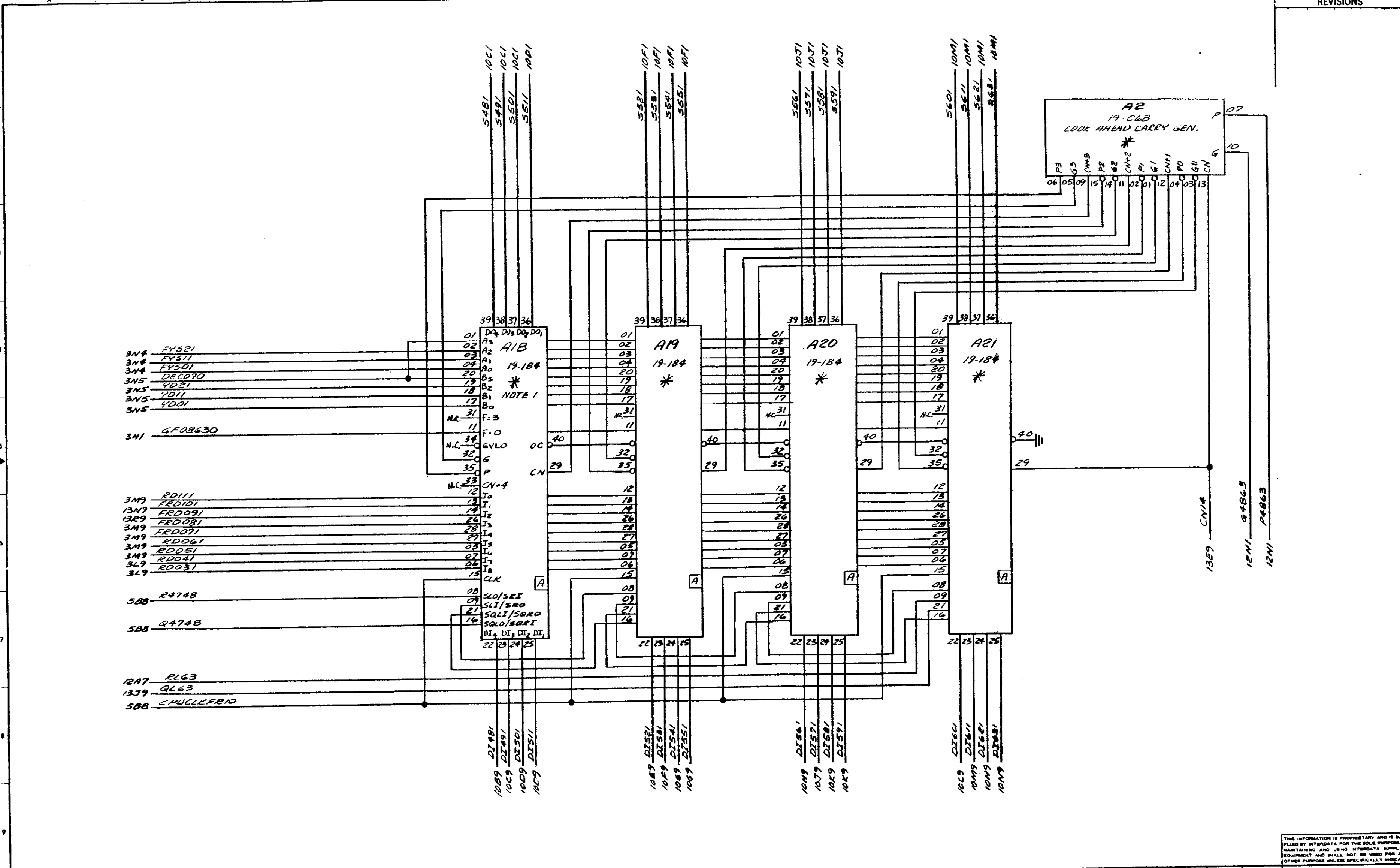
NOTE:
1. STRAP FOR >PFP
2. APPARATUS MARKED WITH AN ASTERISK ARE REMOVED FOR >PFP OPTION.
3. ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-633F01 & F02

SCALE –

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE

DWG 03868
REV 02-449
SHEET 5



NOTES:
1. APPARATUS MARKED WITH AN ASTERISK ARE REMOVED FOR SPFP OPTION.
2. ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-633 F01/F02

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

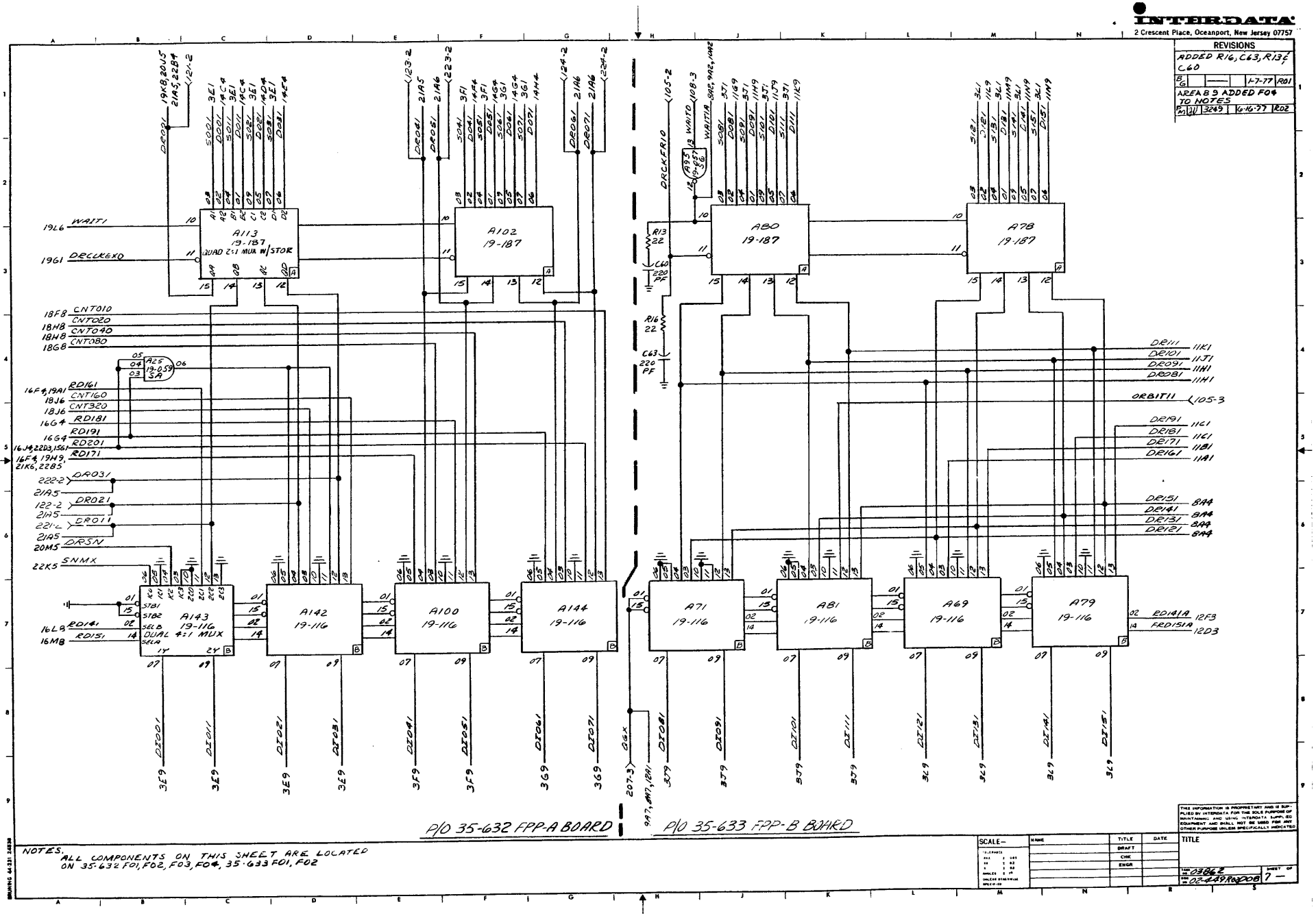
REVISIONS

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

SCALE –

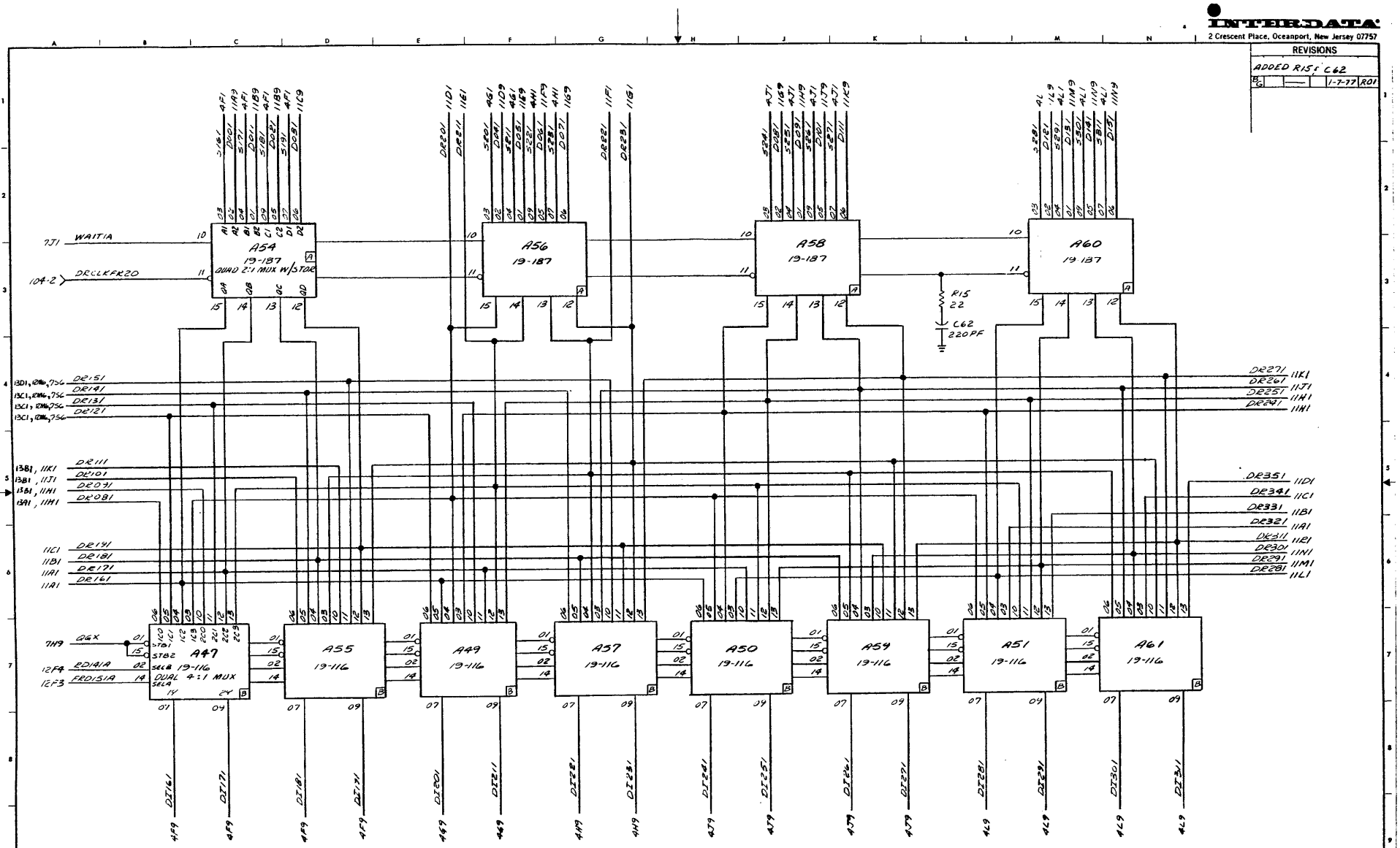
TITLE

02-449 D08 6


INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757
REVISIONS
ADDED R16, C63, R13 & C60
AREA B 9 ADDED FO4 TO NOTES
A113 19-187 QUAD 2:1 MUX W/STOR
A102 19-187
A80 19-187
A78 19-187
A143 19-116 DUAL 4:1 MUX
A142 19-116
A100 19-116
A144 19-116
A71 19-116
A81 19-116
A69 19-116
A79 19-116
A25 19-059 SM
WAIT1
DRCLKEXO
CNT01O
CNT02O
CNT04O
CNT08O
RD16I
CNT16O
CNT32O
RD18I
RD19I
RD20I
RD17I
DR03I
DR02I
DR01I
DRSN
SNMX
RD14I
RD15I
DRCLKERIO
WAIT1A
R13 22
C60 220 PF
R16 22
C63 220 PF
ORBIT1I
DR11I
DR10I
DR09I
DR08I
DR19I
DR18I
DR17I
DR16I
DR15I
DR14I
DR13I
DR12I
RD14IA
FRD15IA
P/O 35-632 FPP-A BOARD
P/O 35-633 FPP-B BOARD
NOTES:
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02, F03, F04, 35-633 F01, F02
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA COMPUTER EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED
SCALE—
NAME
TITLE
DATE
DRAFT
CHK
ENGR
TITLE
DRAWING 44 231 2830

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
ADDED R15, C62			
B		1-7-77	R01



NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-633F01, F02

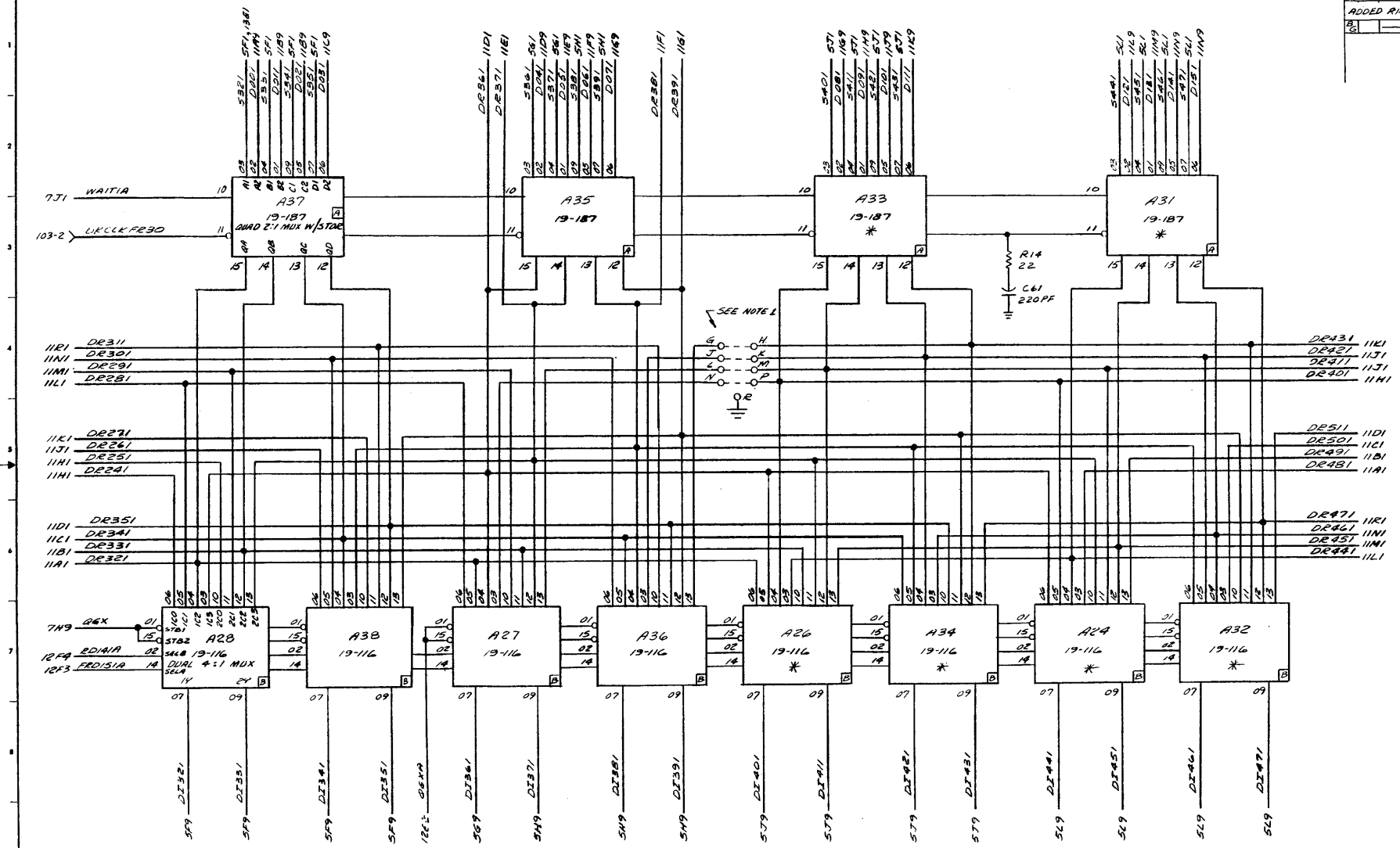
SCALE	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE

DWG 03862 SHEET 8 OF
REV 02-449R01D08

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
ADDED R14 & C61			
B/C	—	1-7-77	R01



NOTES:
1. FOR SP, STRAP G, J, L & N TO P.
2. APPARATUS MARKED WITH ANY ASTERISK ARE REMOVED FOR SPFP OPTION.
3. ALL COMPONENTS LOCATED ON THIS SHEET ARE LOCATED ON 35-633 F01 & F03

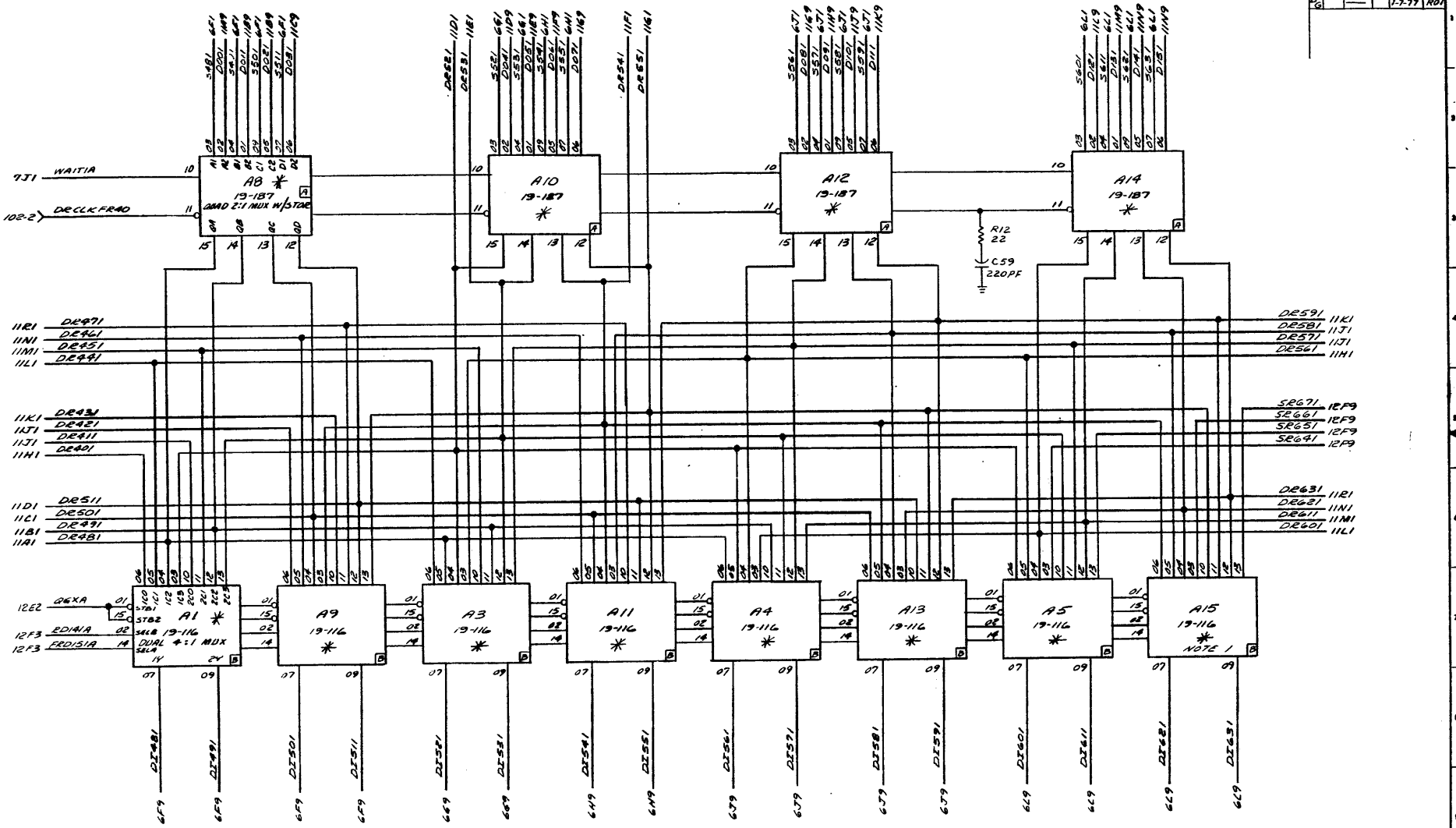
SCALE–	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE

DWG 03862 SHEET 9 OF 9
MFR NO. 02-449R01D06

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
ADDED R12 & C59			
B	—	1-7-77	ROI



NOTES:
1. APPARATUS MARKED WITH AN ASTERISK ARE REQUIRED FOR SPFP OPTION.
2. ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-633 F01 & F02

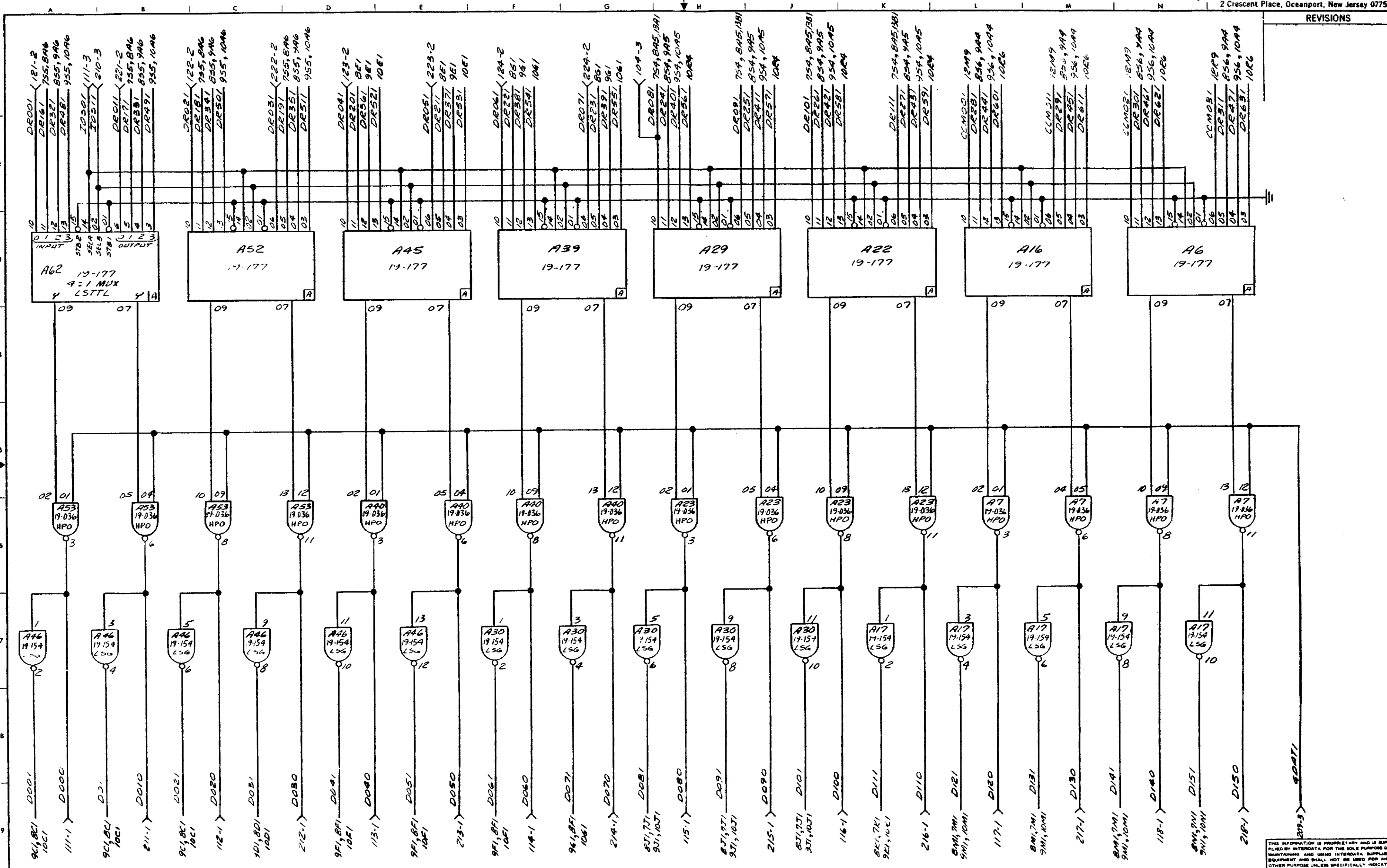
SCALE — | NAME | TITLE | DATE | DRAFT | CHK | ENGR

TITLE

SIZE 03862 | DWG 02-449 REV D08 | SHEET OF 10

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



NOTES.
ALL COMPONENTS ON THIS SHEET ARE
LOCATED ON 35-633F01, F0C

SCALE–

TITLE

03862

02-449 D08

11–

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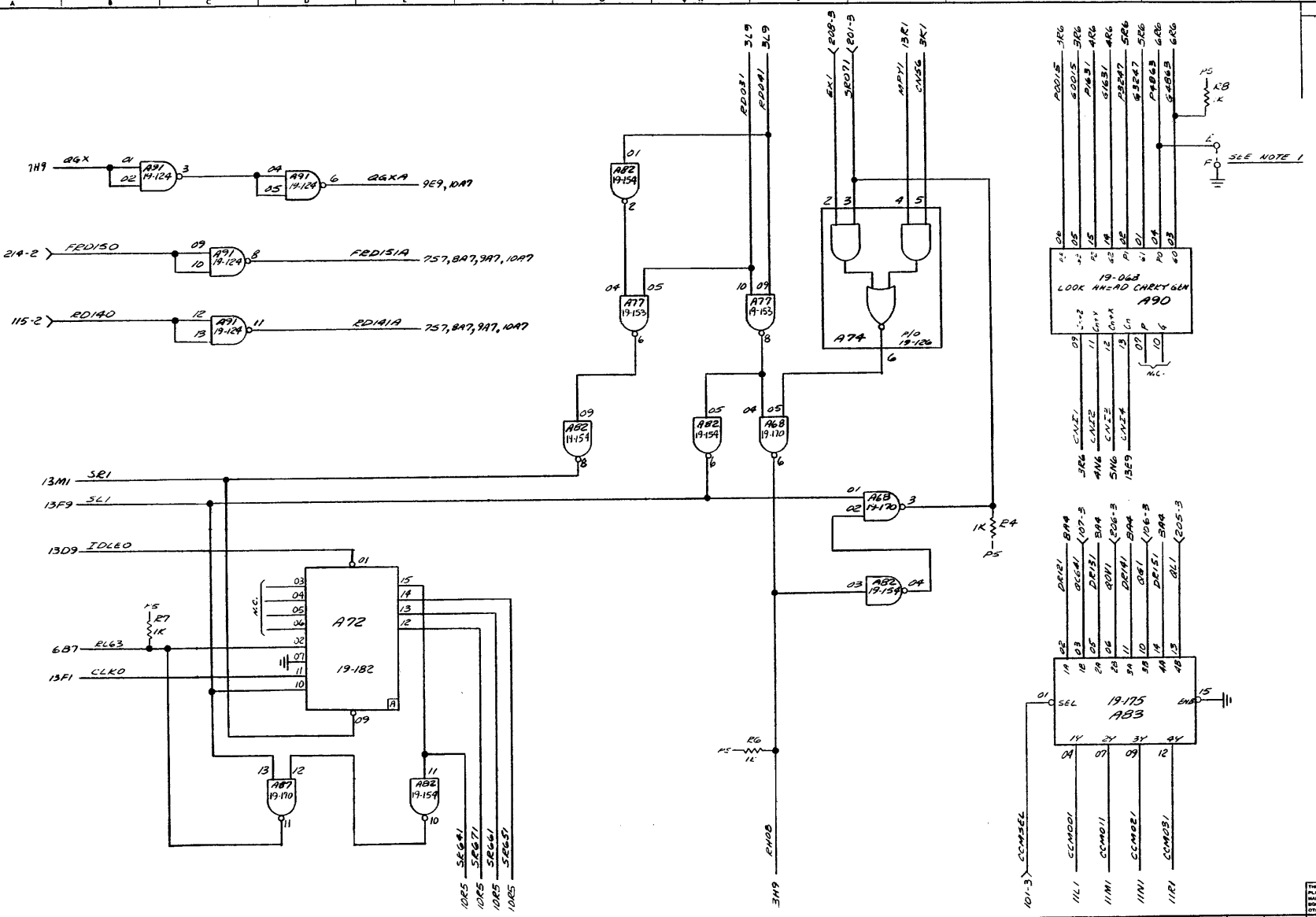
INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



NOTES:
1. IF SP ONLY, STRAP P4863 TO GND.
2. ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-633F01, F02

SCALE–

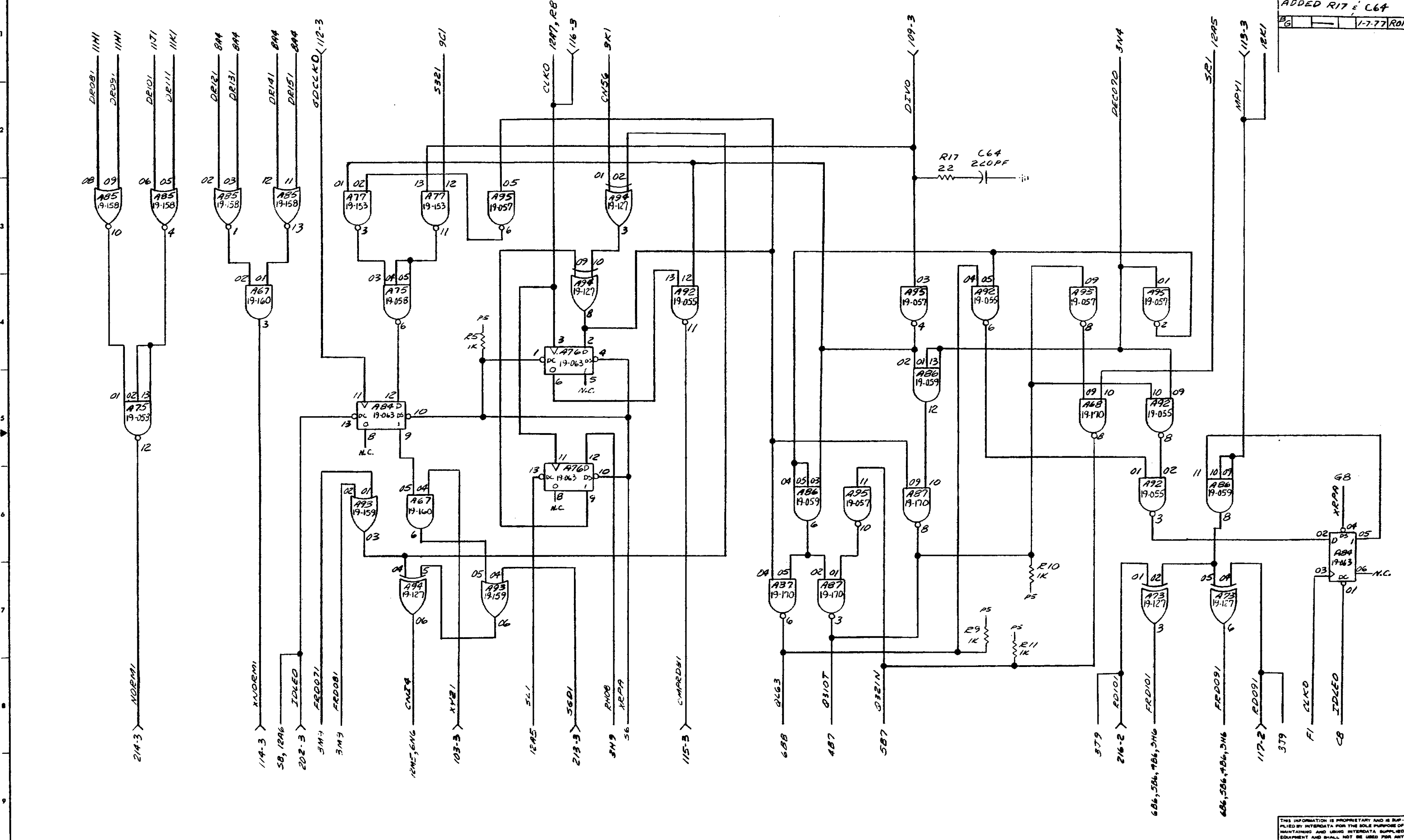
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE

DWG NO. 03862 REV 02-449 SHEET 12 OF DOG

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
ADDED R17 & C64				
B G			1-7-77	R01



NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED
ON 35-633F01:F02

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

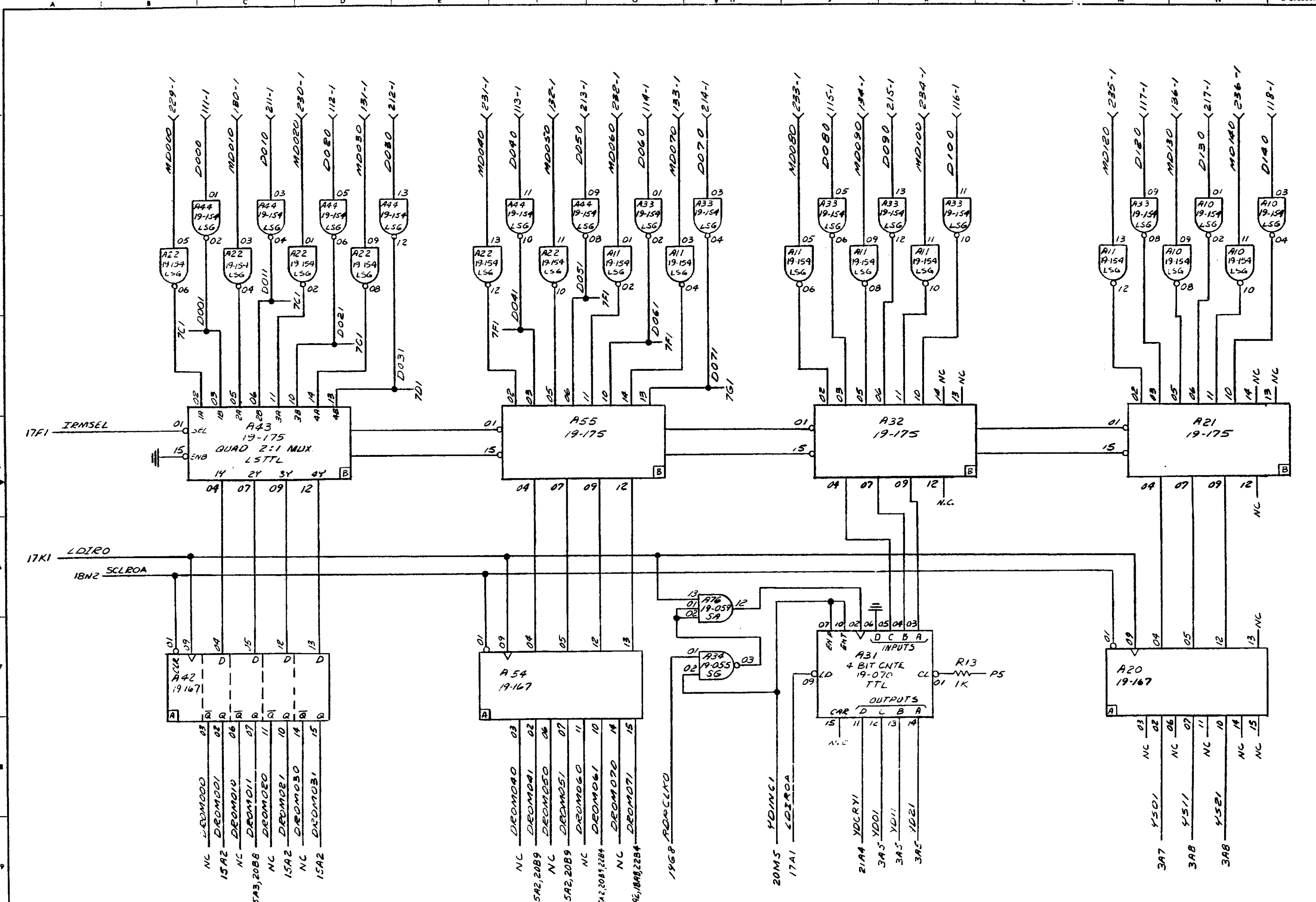
SCALE –

TITLE

03862
02-449R01D08
SHEET 13

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
AREA H7: A76, A34 & RELATED CIRCUITRY WAS NOT SPEC'D. A31-02 WAS TO MNE. YDCLK1.			
WS	03862-3	3-2-77	R01
AREA B6 SCLROA, 18N2 WAS R14(1K) PS. AREA C9 ADDED F04 TO NOTES.			
	3243	6-16-77	R02
AREA J7: A31 (19-070) WAS A31 (19-155).			
	3496	12-21-77	R03



NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632F01, F02, F03&F04

SCALE–	NAME	TITLE	DATE
		DRAFT	
		CHK	
		ENGR	

TITLE

03862
02-449R03D08
SHEET 14

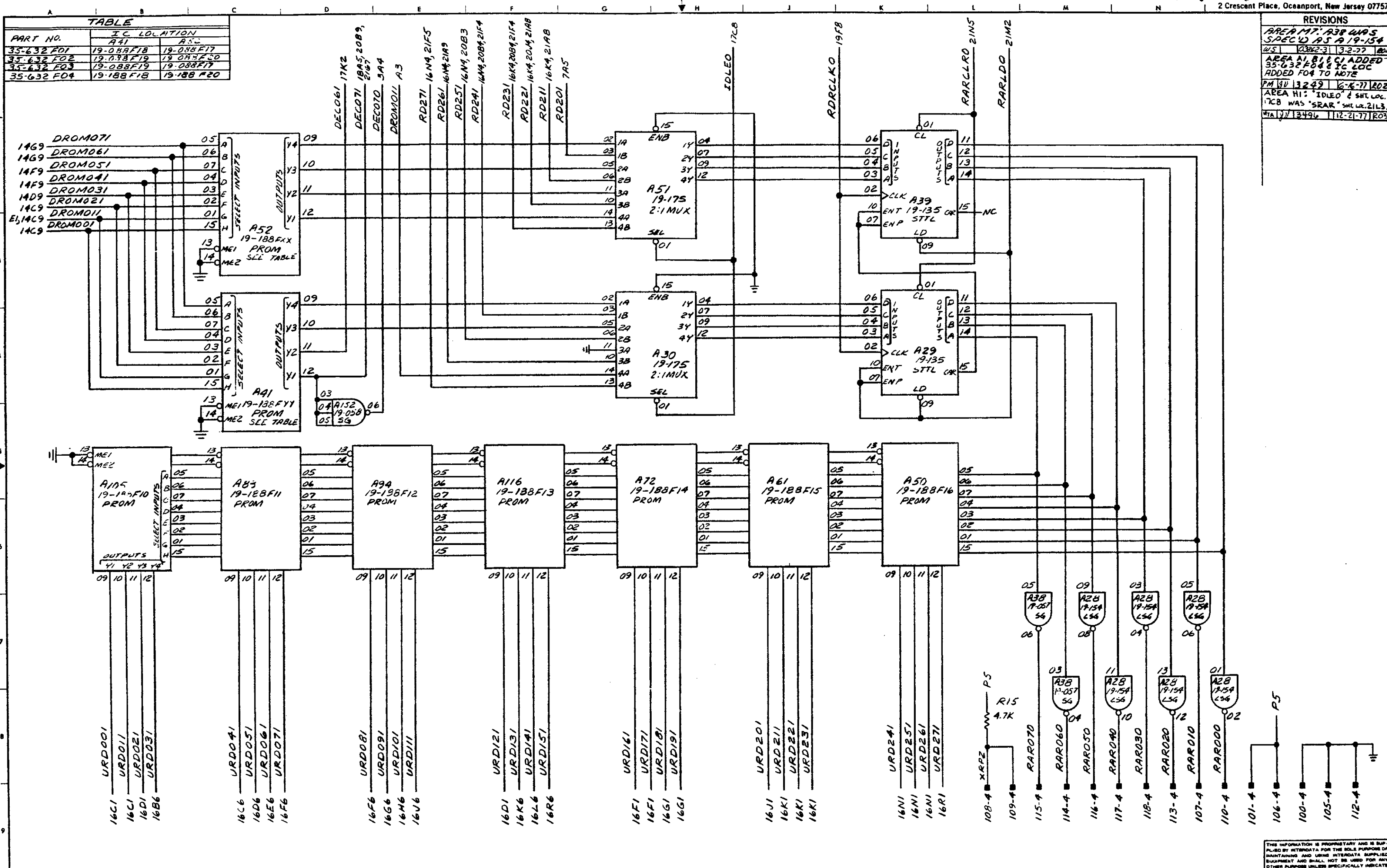
INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

TABLE

PART NO.	IC LOCATION A41	IC LOCATION A52
35-632 F01	19-088F18	19-088F17
35-632 F02	19-088F19	19-088F20
35-632 F03	19-088F19	19-088F17
35-632 F04	19-188F18	19-188F20

REVISIONS

AREA M7: A38 WAS SPEC'D AS A 19-154			
WS	03862-3	3-2-77	R01
AREA A1, B1 & C1 ADDED 35-632 F04 & IC LOC ADDED F04 TO NOTE			
PM / JU	3249	6-6-77	R02
AREA H1: "IDLE0" & SHT. LOC. 17C8 WAS "SRAR" SHT. LOC. 21L3.			
WTA / JJ	3496	12-21-77	R03

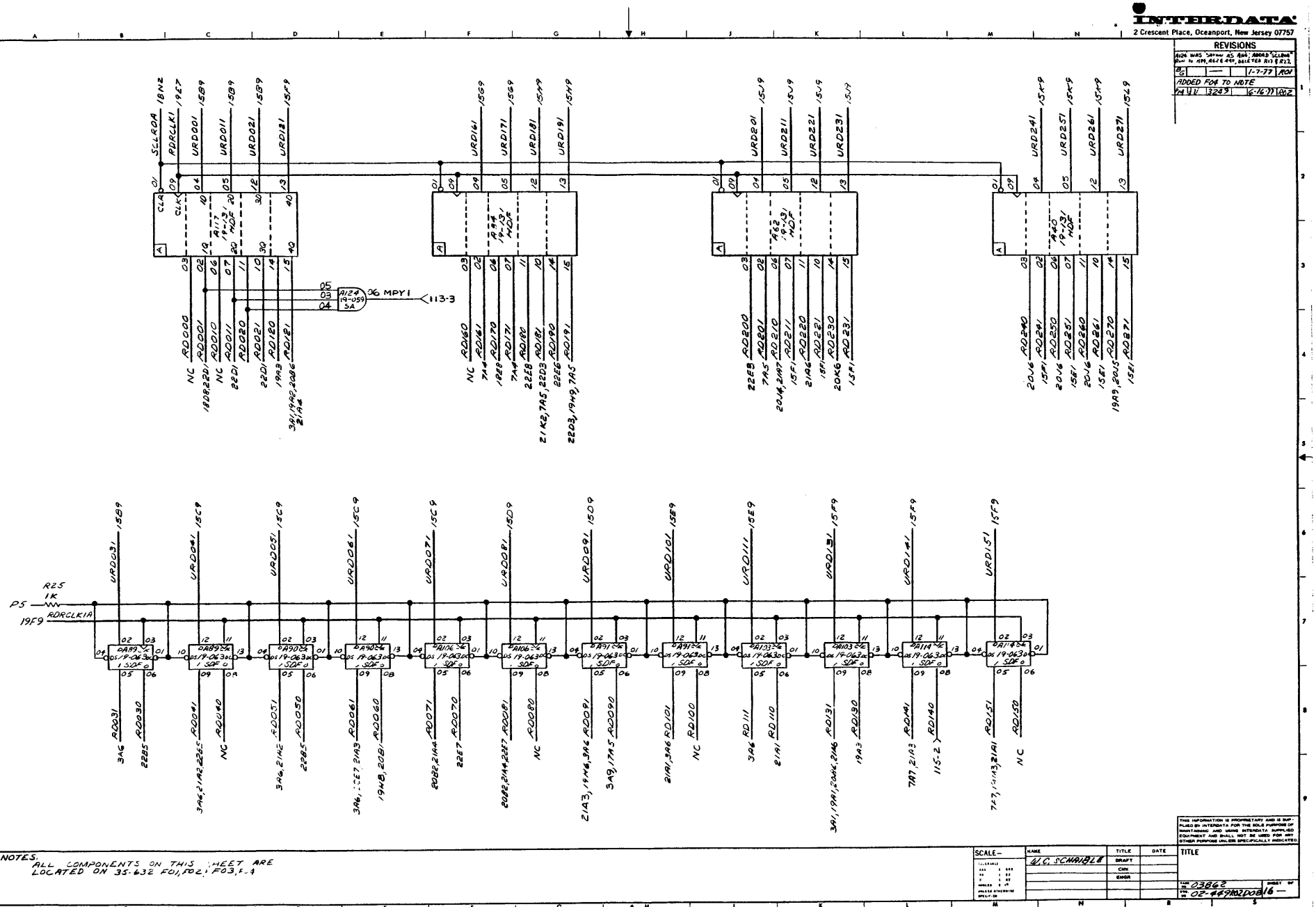


NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02 & F03, F04

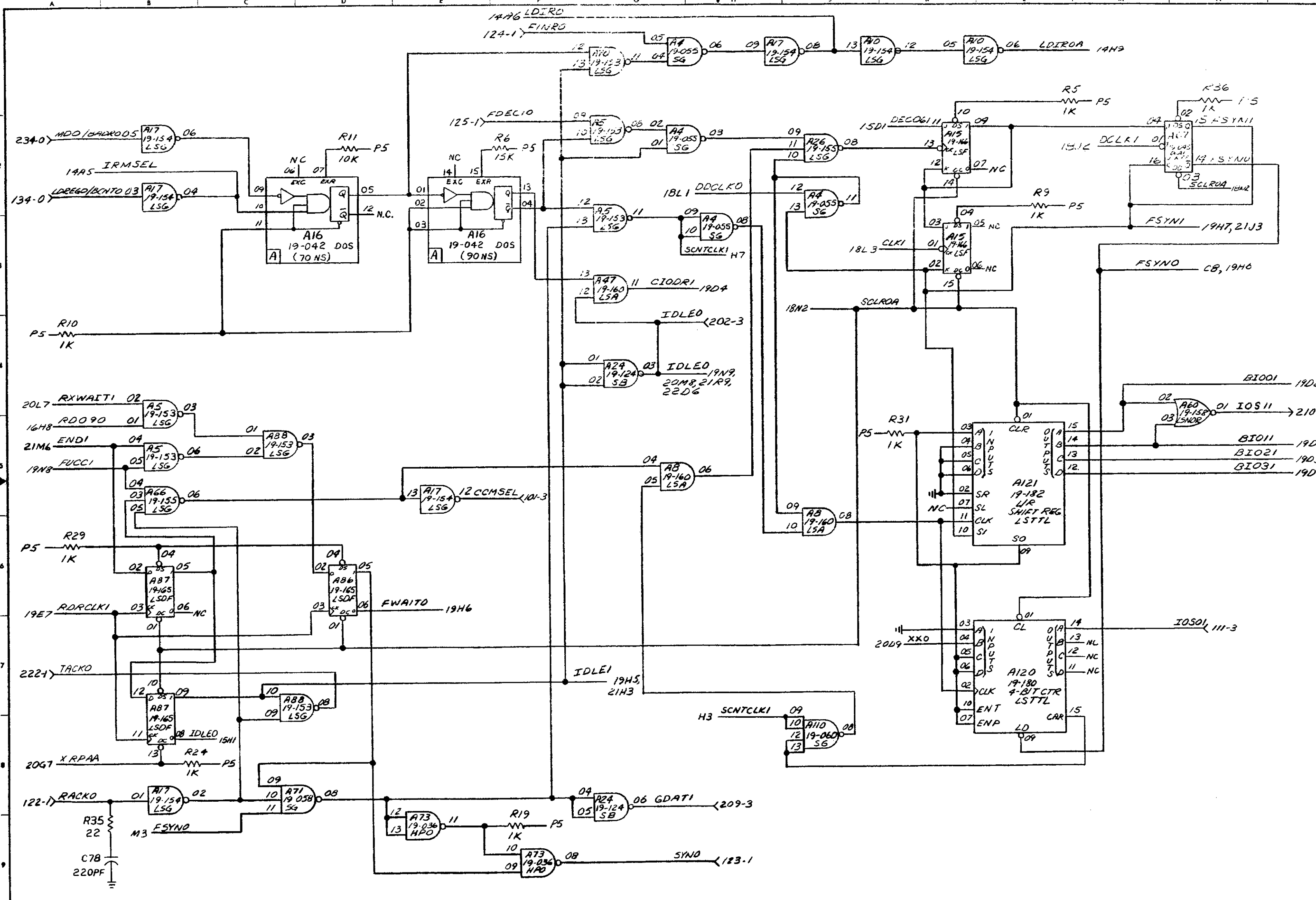
THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED

SCALE — | NAME | TITLE | DATE | TITLE
DRAFT
CHK
ENGR

03862
02-449R80D08
SHEET 15


INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757
REVISIONS
ADDED FOR TO NOTE
NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02, F03, F-4
SCALE—
DRAWN
C. SCHAIBLE
TITLE
DRAFT
CHK
ENGR
DATE
03862
02-44702D0B
16

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757



REVISIONS

AREA D2 A16-05 & 12 WERE TIED TOGETHER; AREA A9 ADDED R35 & C78; AREA K7 "XXO" WAS "XX". | 1-7-77 | R01

AREA F1: DELETED CROSS-REF 19F7 FROM LDIRO. | WS | 03823 | 3-6-77 | R02

AREA H2, A9 PIN 10 ADDED SCNTCLK1, H7. ADDED F04 AREA H7, A110 PINS ADDED SCNTCLK1, H3 ALSO A110 PIN 10 WAS TIED TO A110 PIN 12 | 3249 | 6-16-77 | R03

AREA C8: A87-08 WAS N.C. | 3496 | 12-21-77 | R04

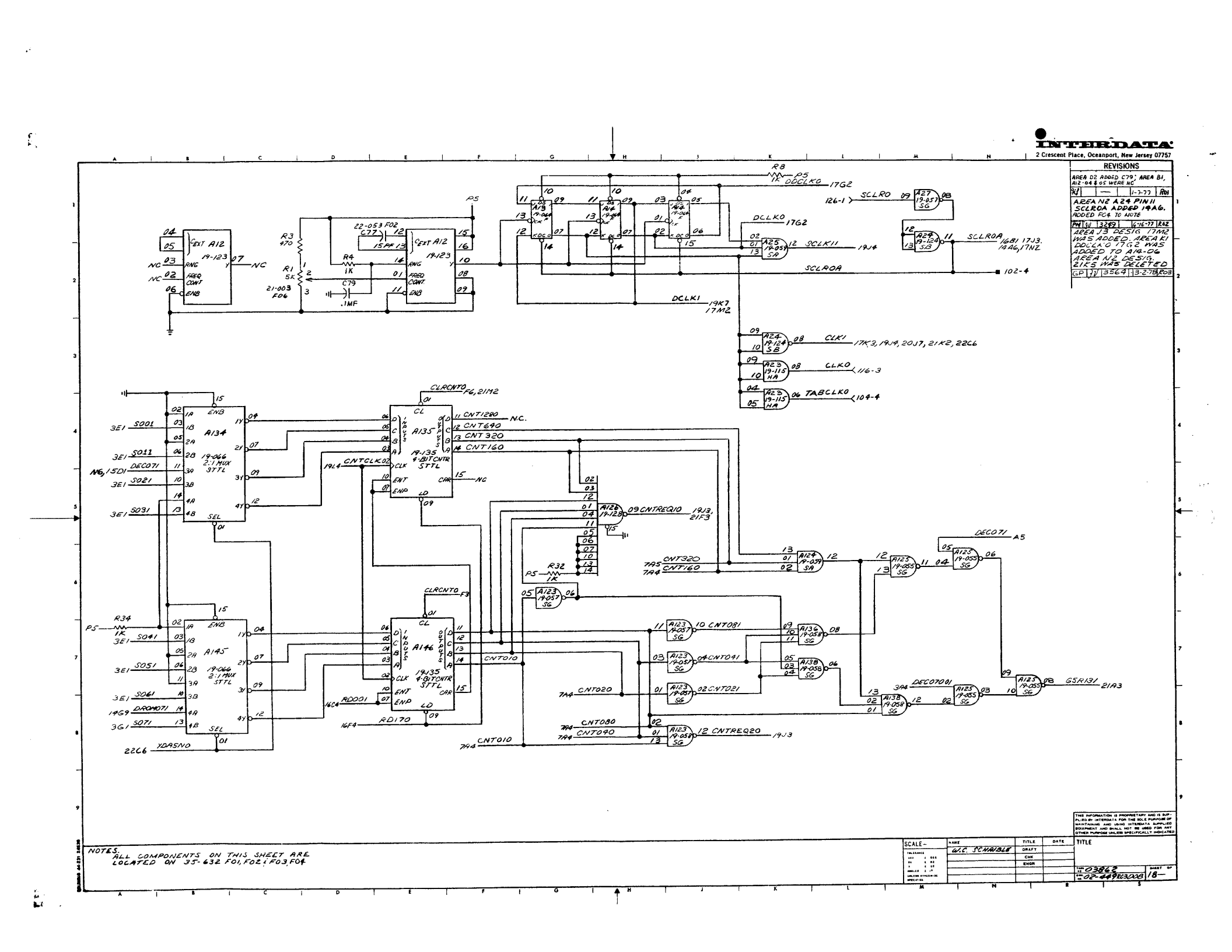
EXTENSIVE REVISIONS FOR PREVIOUS LEVEL SEE MICROFILM COPY | GP | 3564 | 3-1-78 | R05

NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02, F03, F04

SCALE–

TITLE

0386P
02-449 ROSDOB
SHEET 17



NOTES:
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02 & F03, F04

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

AREA L6 ADDED A79 GATE			
KJ	—	11-2-77	R01
AREA F2: DELETED A76 GATE A126-03 WAS TO A76-01, 02. AREA J1, J3: A38 WAS SPEC'D AS A 19-154			
45	03&23	3-2-77	R02
ADDED FO4 TO NOTE 2			
PM KW	3249	6-16-77	R03
EXTENSIVE REVISION FOR PREVIOUS REV. SEE R03 MICROFILM COPY IN FILES			
GP KW	3696	5-23-78	R04

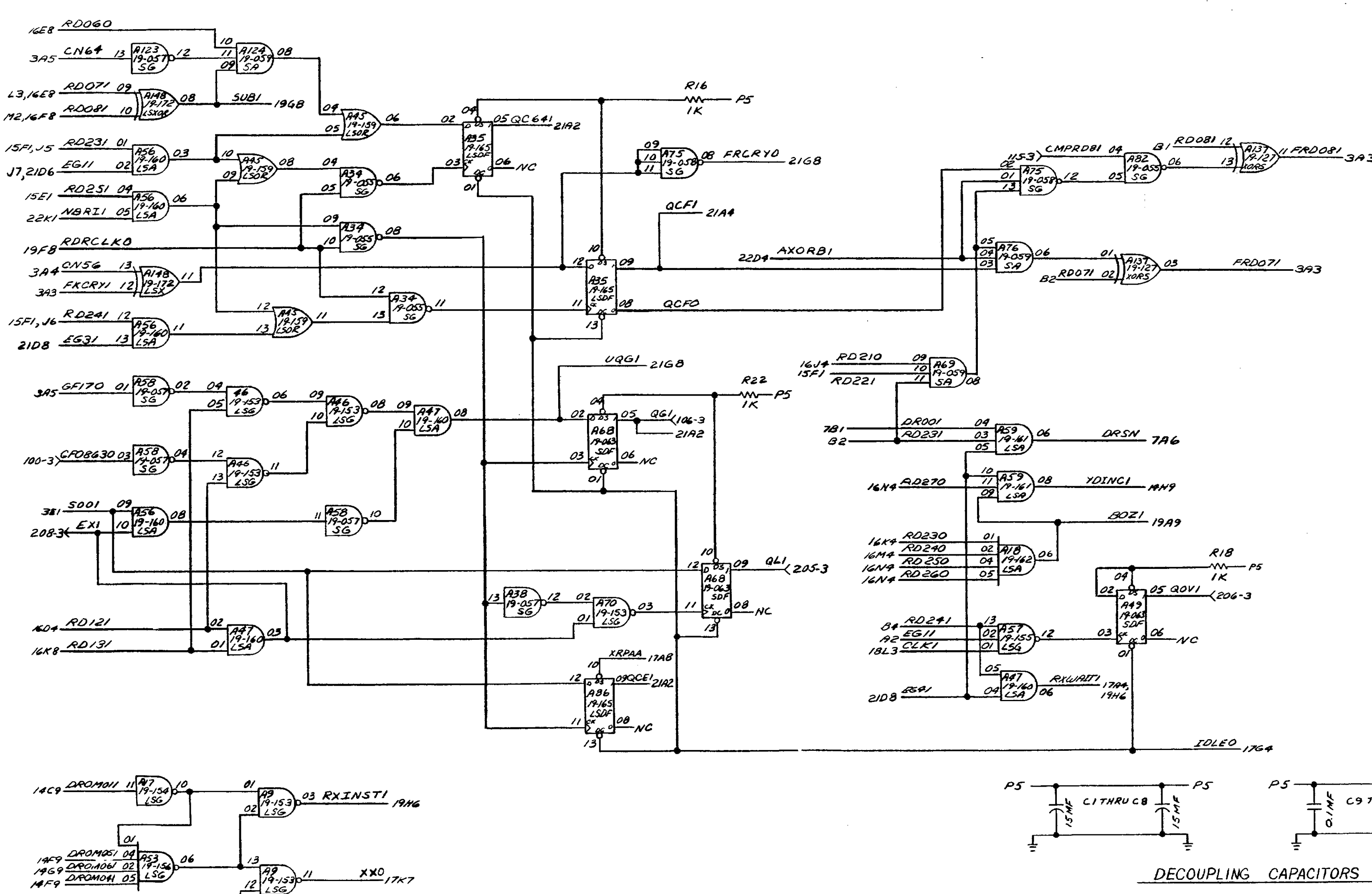
NOTES.
1. FOR 35-632 F01 & 35-632 F03 STRAP B TO A, 35-632 F02 STRAP B TO C.
2. ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02 & F03, F04

SCALE — | NAME | TITLE | DATE
DRAFT
CHK
ENGR

TITLE

ITEM 03862 SHEET 05
DWG 02-449 R04 DATE 19—

REVISIONS			
AREA D9 "XXO" WAS "XX"			
	—	1-7-77	R01
AREA D2, D3 E D4: A34 WAS SPEC'D AS A 19-153. AREA F7: A38 WAS SPEC'D AS A 19-154			
	03862-3	3-2-77	R02
ADDED F04 TO NOTE			
PM	3249	6-16-77	R03



DECOUPLING CAPACITORS

NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02, F03, F04

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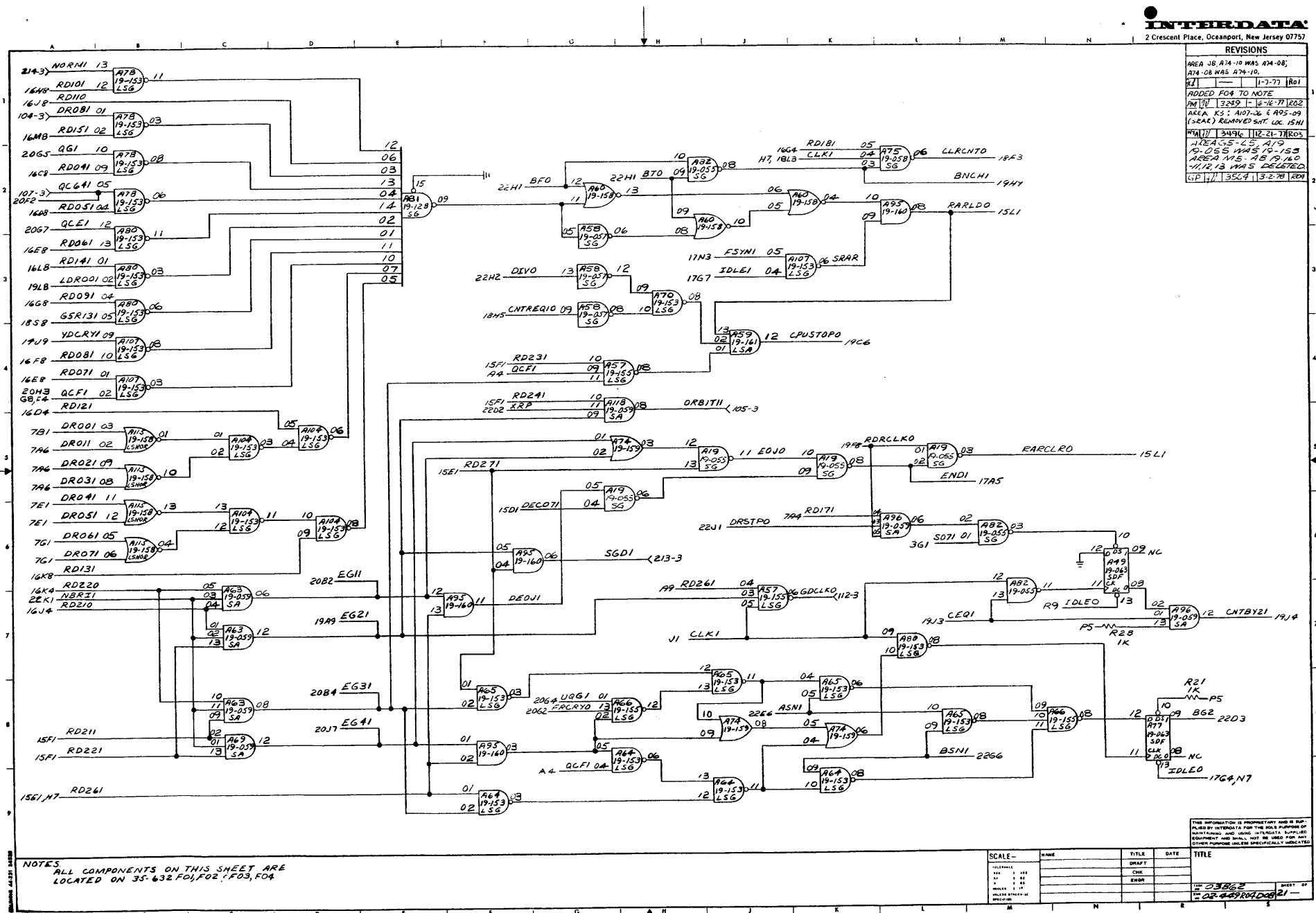
SCALE — | NAME | TITLE | DATE | DRAFT | CHK | ENGR

TITLE

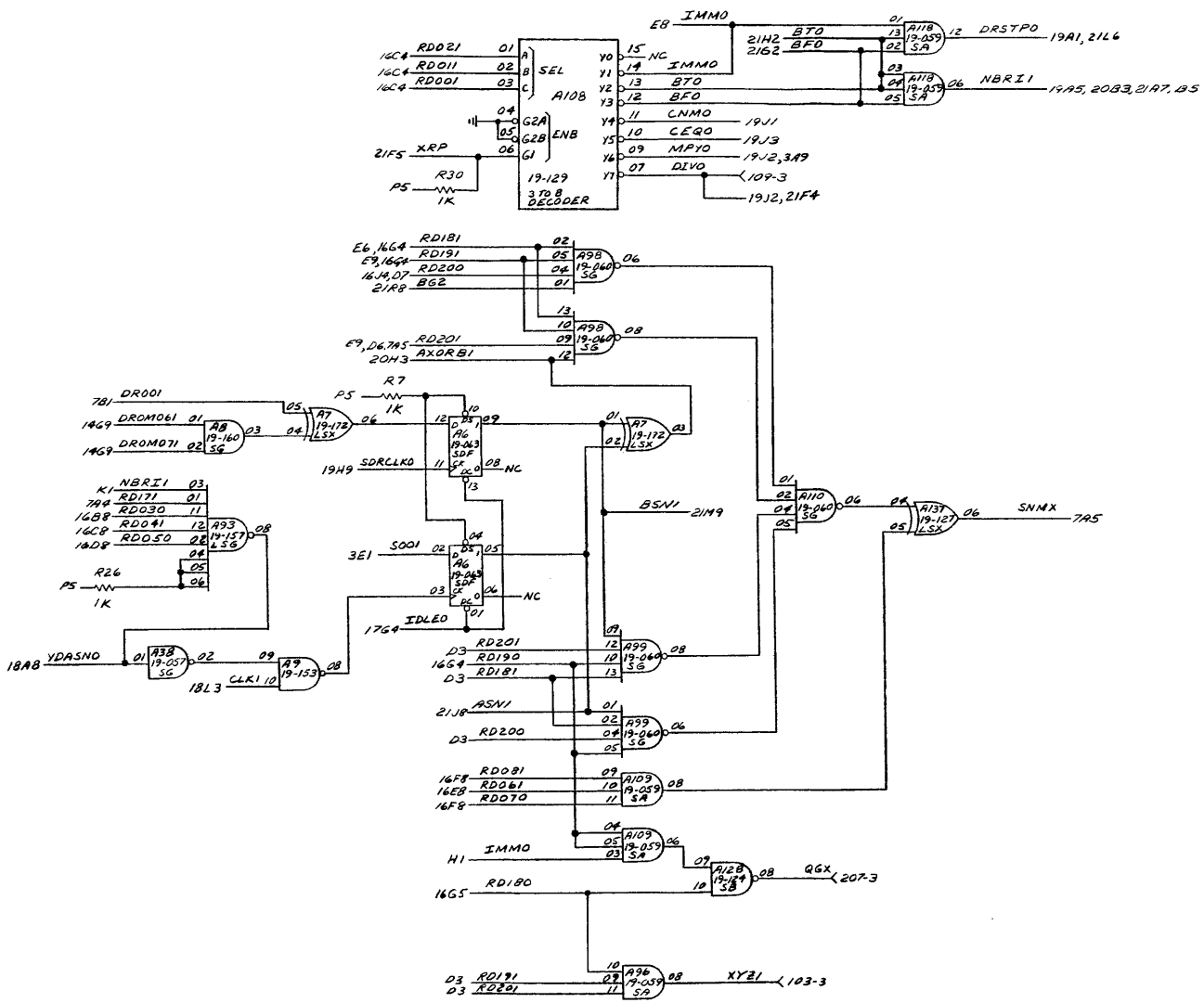
03862
02-449 R03 D08
SHEET 20



NOTES.
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 F01, F02, F03, F04

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
AREA CG: A30 & A35 SPECO AS 19-156				
AS	038623	3-2-77	MV	
AREA C9 ADDED FO4 TO NOTES				
MW	3249	6-16-77	BD2	



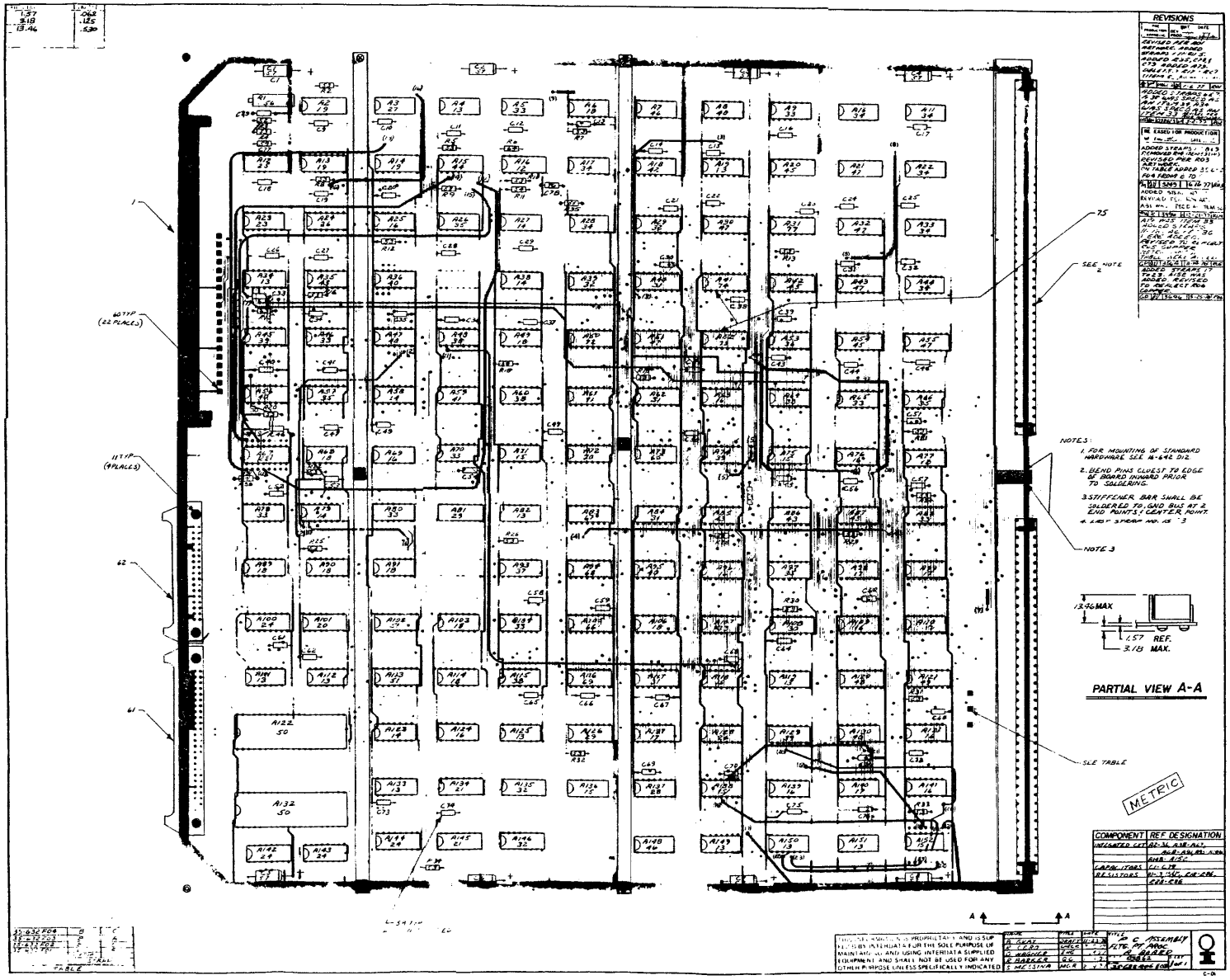
NOTES
ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-632 FO1, FO2, FO3 & FO4

SCALE –

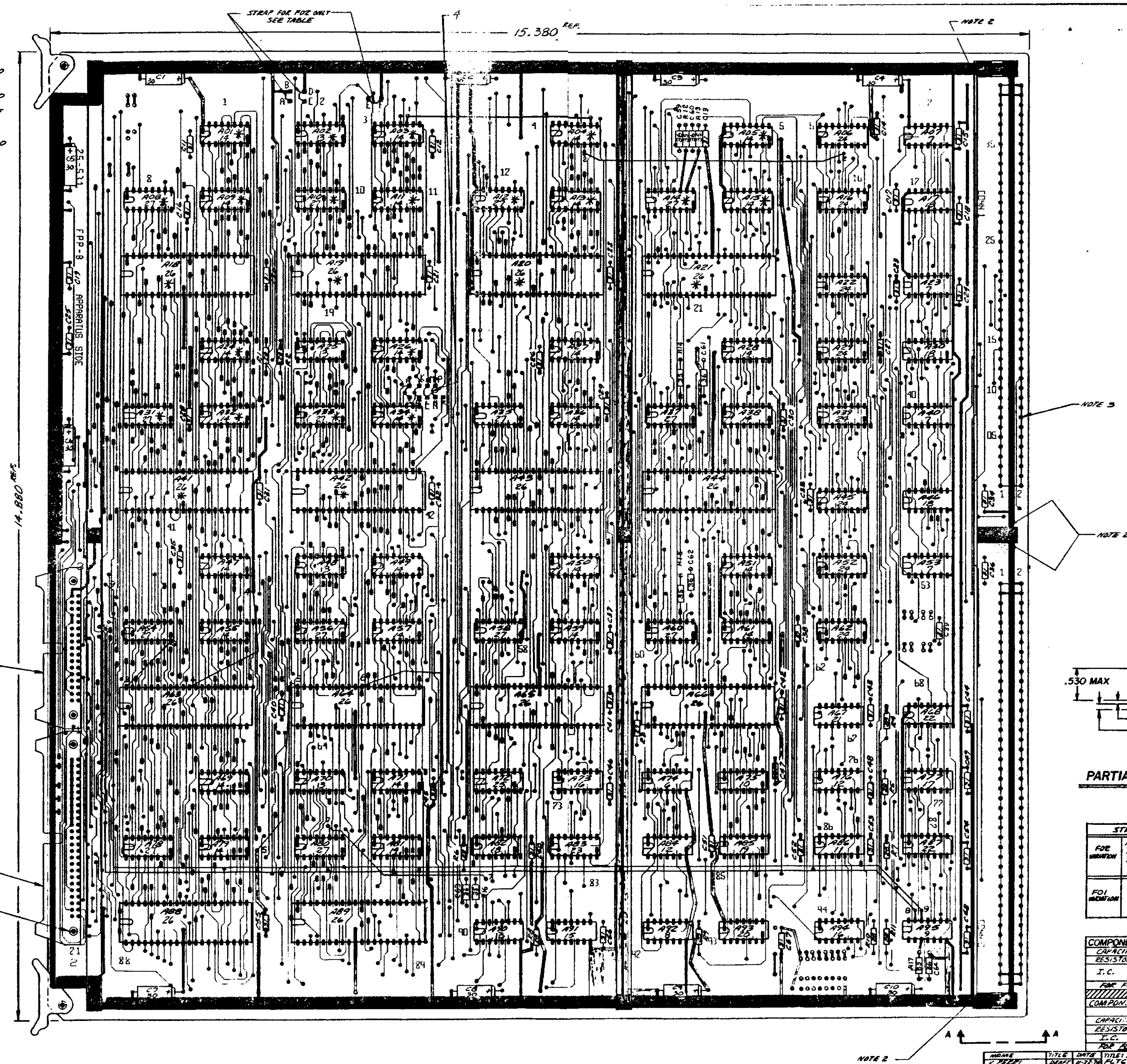
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

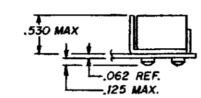
TITLE

SIZE 038623 SHEET 09
DWG NO 02-449 REV 22


NOTES:
1. FOR MOUNTING OF STANDARD HARDWARE SEE A-642 DIA.
2. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.
3. STIFFENER BAR SHALL BE SOLDERED TO GND BUS AT 8 END POINTS + CENTER POINT.
4. LAST STEAM NO. IS 3
NOTE 3
SEE NOTE 2
SLE TABLE
PARTIAL VIEW A-A
12.96 MAX
1.57 REF.
3.18 MAX.
METRIC
COMPONENT
REF DESIGNATION
PARTIAL VIEW A-A

NOTES:
1. FOR MOUNTING OF STANDARD HARDWARE SEE 16-642 DIR.
2. STIFFENER BAR SHALL BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
3. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
4. ITEMS MARKED WITH AN ASTERISK (*) ARE NOT EQUIPPED FOR F02 VARIATION.
5. ALL DIMENSIONS ARE IN INCHES.





PARTIAL VIEW A-A

REVISIONS

PRE PRODUCTION APPROVAL	DEV / PROD
ADDED C59 THRU C64 & R12 THRU R17, ADDED STRAPS 1 THRU 9; ADDED 9 SPARE COMPONENT POSITIONS & 1 SPARE IC POSITION.	
[illegible] 06862-2 [illegible] 1-6-77	R01

RELEASED FOR PRODUCTION
MFG. ENG. [illegible] DATE [illegible]

STRAPPING OPTIONS	
F02 VARIATION	A TO B, C TO D, G TO J, J TO L, L TO N, N TO R
F01 VARIATION	G TO H, J TO K, L TO M, N TO P

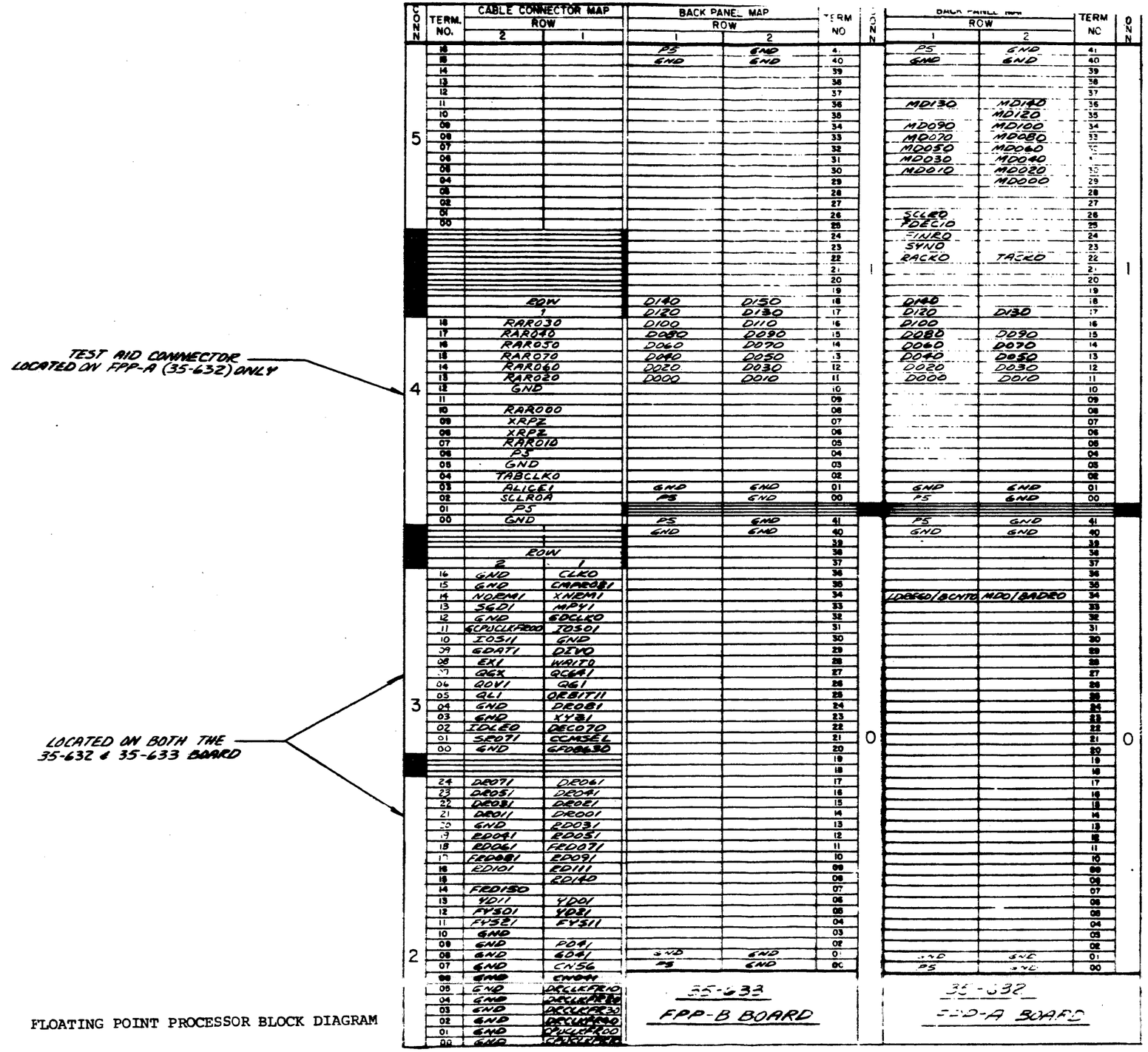
COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C64
RESISTOR	R1 THRU R17
I.C.	A6, A7, A16, A17, A22, A23, A25, A27 THRU A30, [illegible]
FOR F02 VARIATION ONLY	

COMPONENT	REF DESIGNATION
CAPACITOR	C1 THRU C64
RESISTOR	R1 THRU R17
I.C.	A01 THRU A95
FOR F01 VARIATION ONLY	

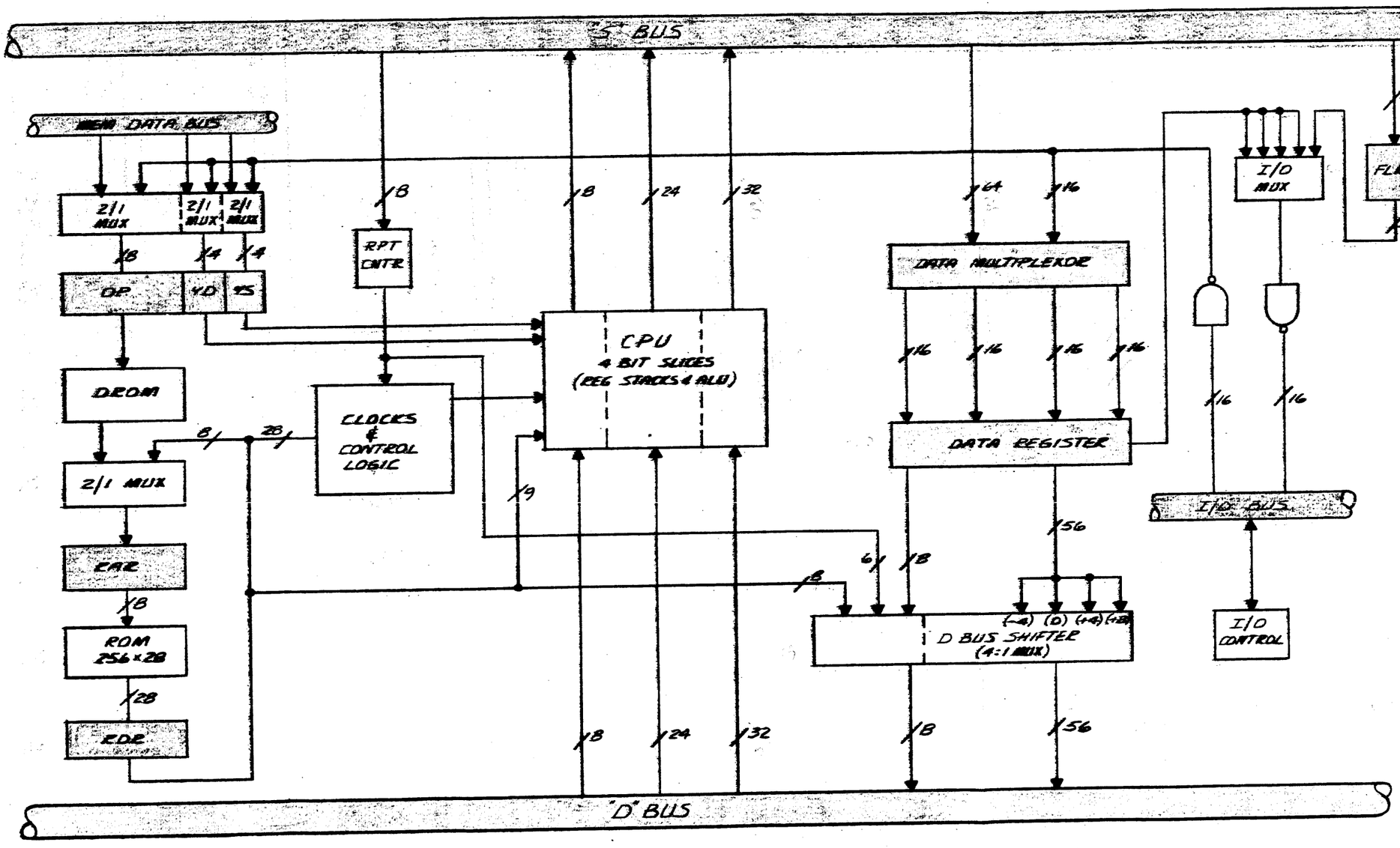
NAME	TITLE	DATE
V. PEZZI	DRAFT	11-22-76
	CHK	
D. WAGNER	ENGR.	2-24-77
E. A. BARKER	Q.C.	1-21-77
S. MESSINA	MGR.	2-24-77

TITLE: PC ASSEMBLY FLTG. PT. PROC. "B" BOARD
03076
35-633 R01 E03
SHEET 1-1

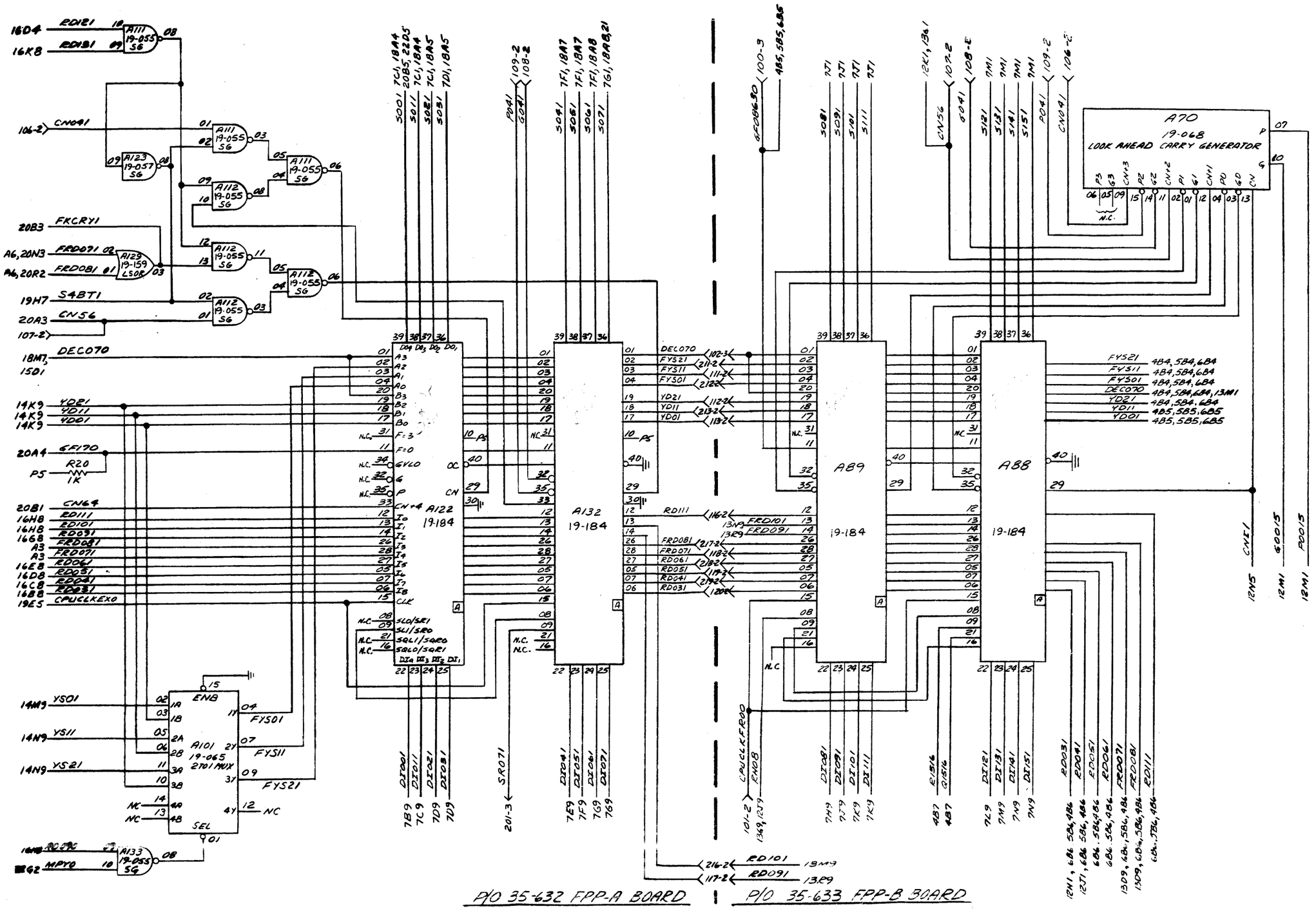
LAST STRAP IS NO. 9.

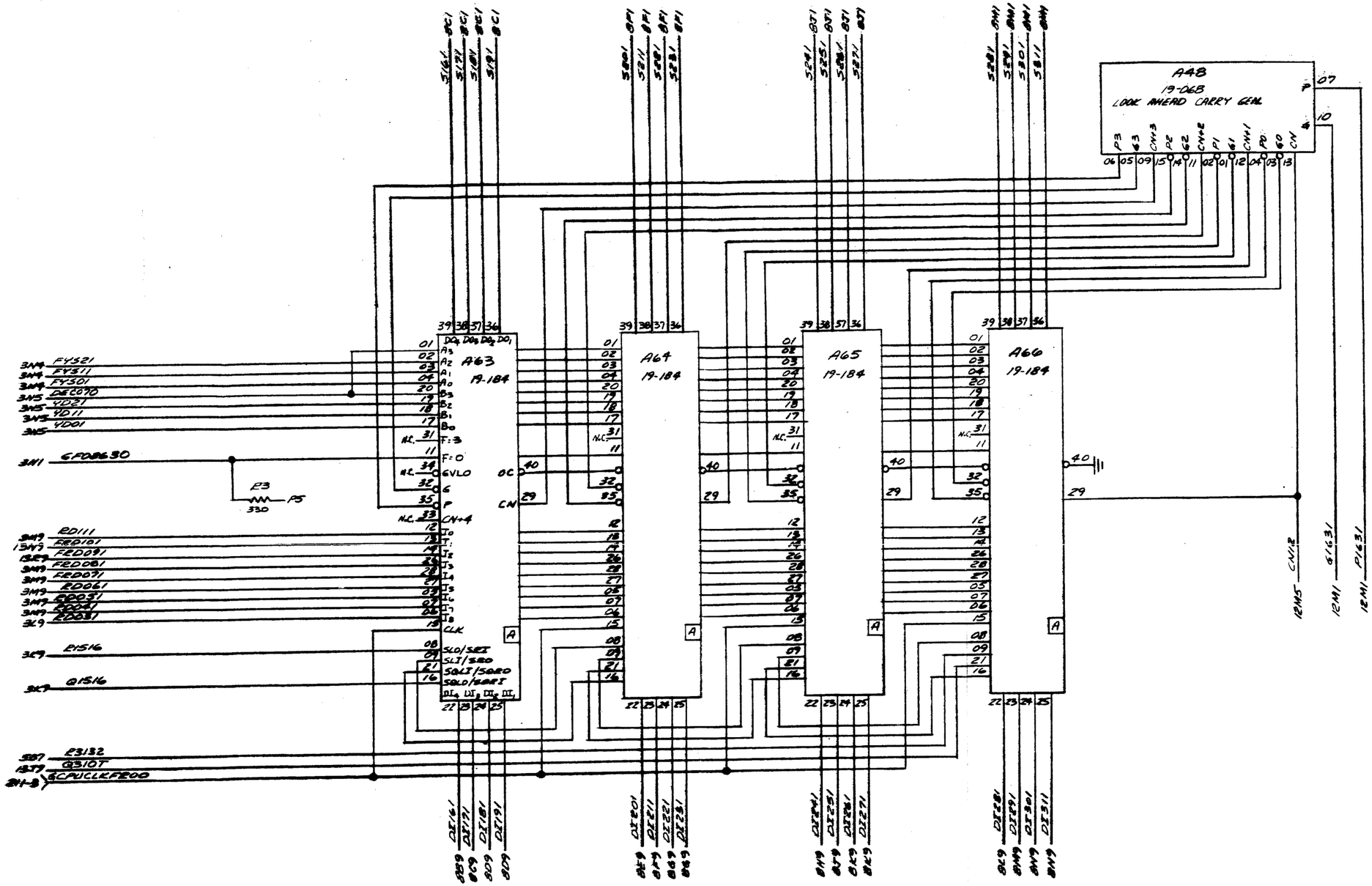


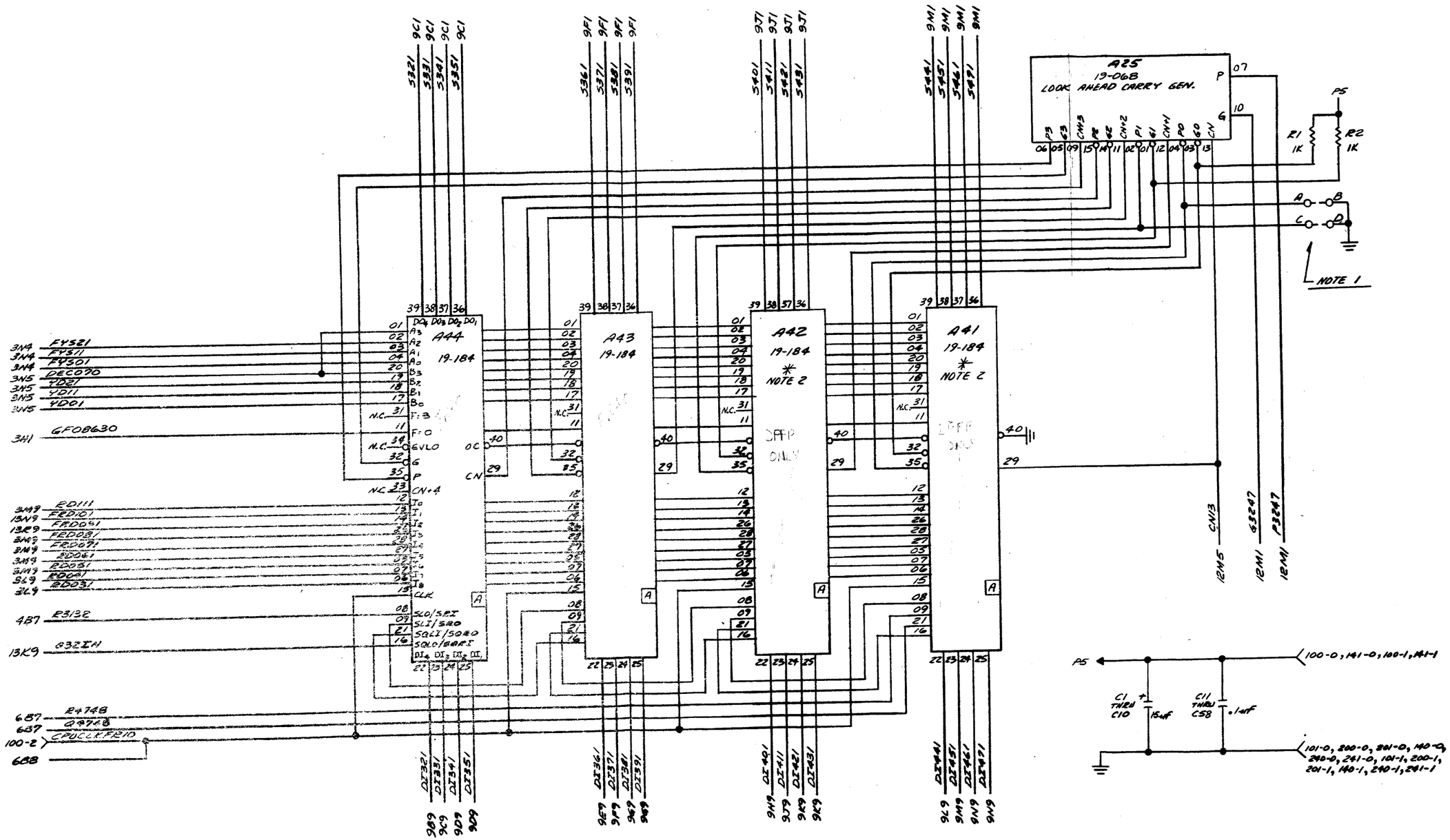
FLOATING POINT PROCESSOR BLOCK DIAGRAM

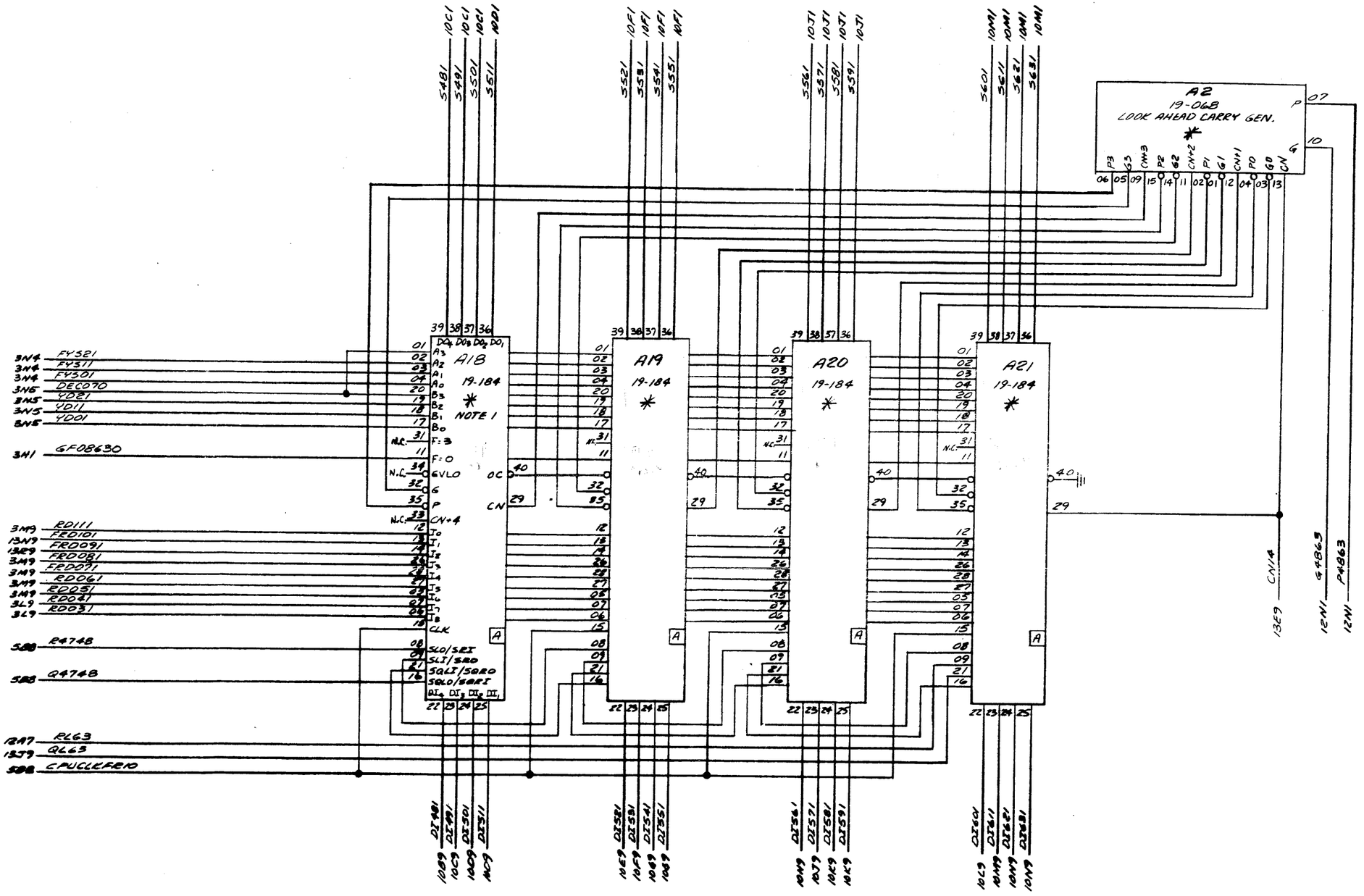


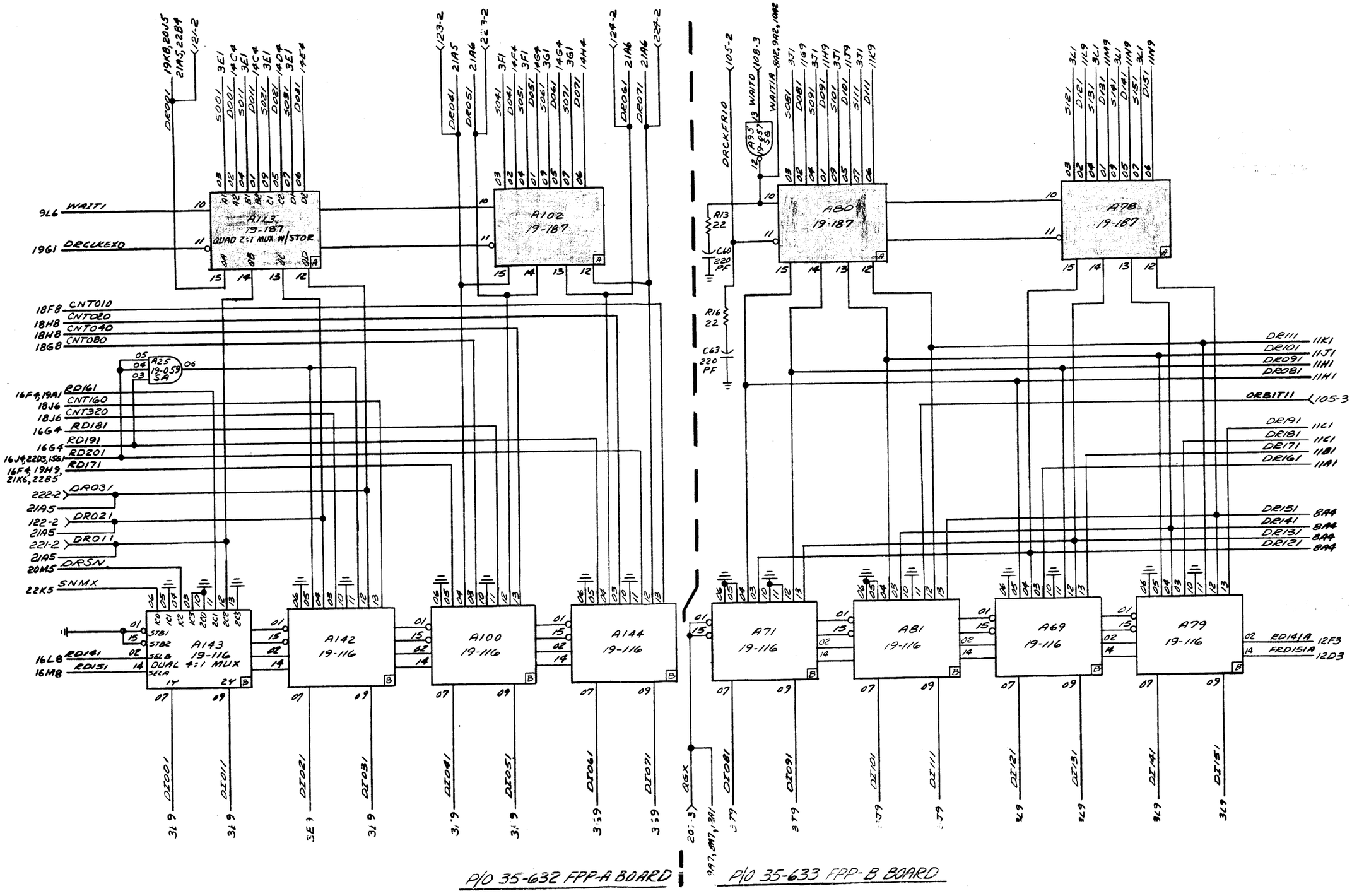
FLOATING POINT PROCESSOR BLOCK DIAGRAM

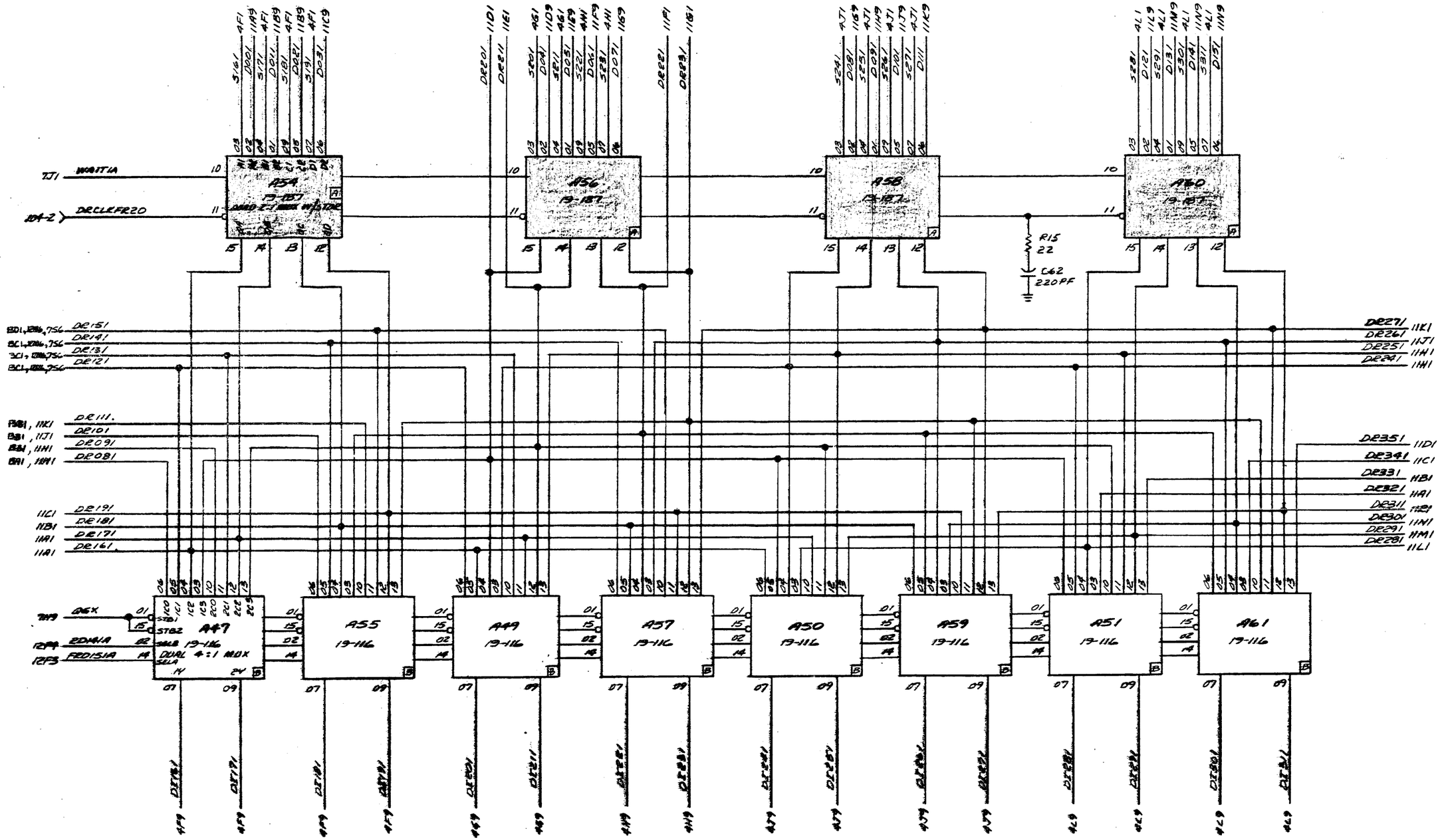

A70
19-068
LOOK AHEAD CARRY GENERATOR
A89
A88
A132
19-184
A122
19-184
A101
19-065
2101 MUX
ENB
SEL
FYS01
FYS11
FYS21
NC
P/O 35-632 FPP-A BOARD
P/O 35-633 FPP-B BOARD

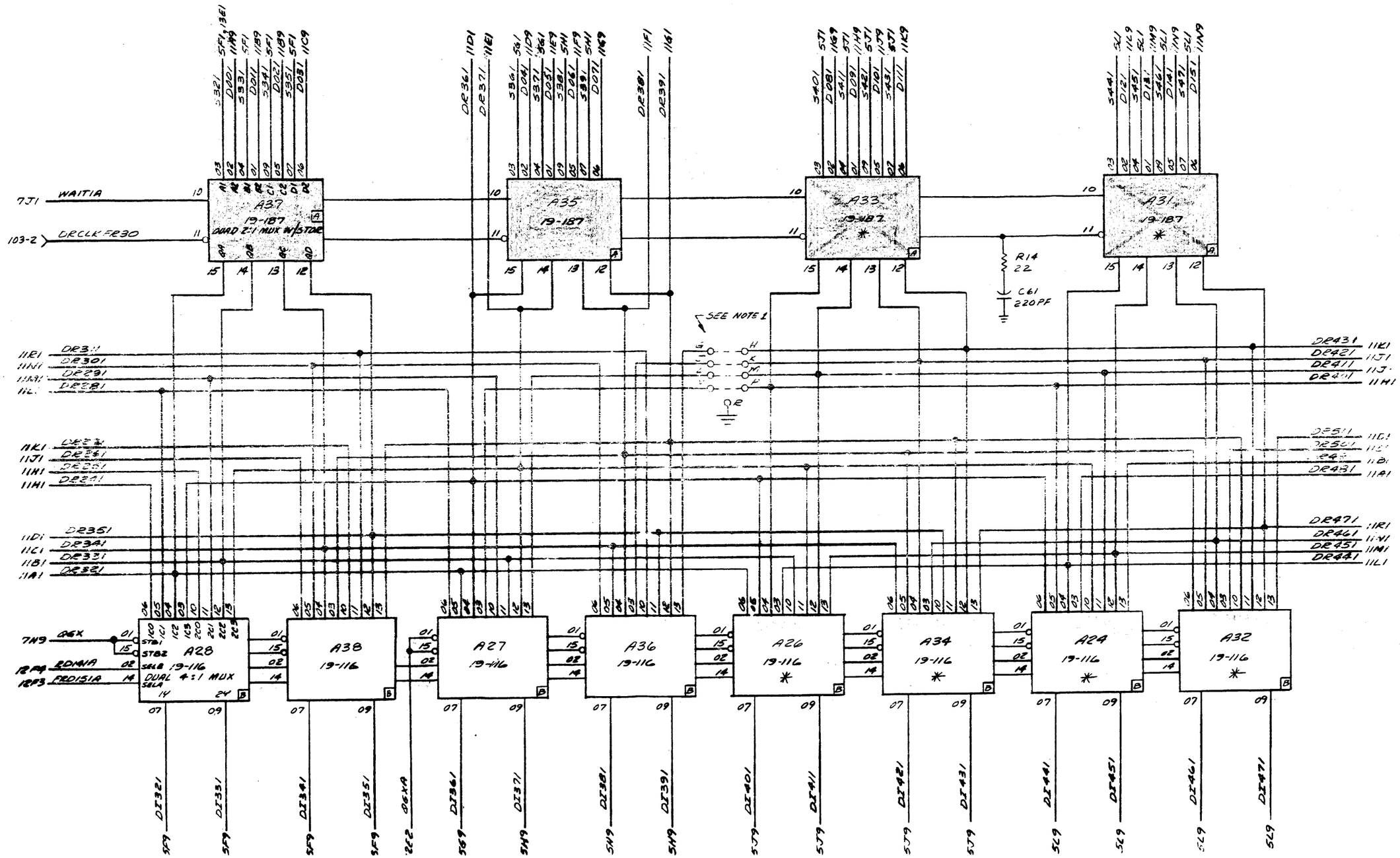

A48
19-068
LOOK AHEAD CARRY GEN.
A63
19-184
A64
19-184
A65
19-184
A66
19-184
A
3N4 FY521
3N4 FY511
3N4 FY501
3N5 DE2070
3N5 4D21
3N5 4D11
3N5 4D01
3N1 GFDB630
P3
330
P5
3N3 RD111
3N3 RD101
3N3 RD091
3N3 RD081
3N3 RD071
3N3 RD061
3N3 RD051
3N3 RD041
3N3 RD031
3L9 P1516
3L9 Q1516
5B7 E3132
4B7 Q3107
2N1-3 SCANCLKFE00
12M5 CN42
12M1 G163
12M1 P163

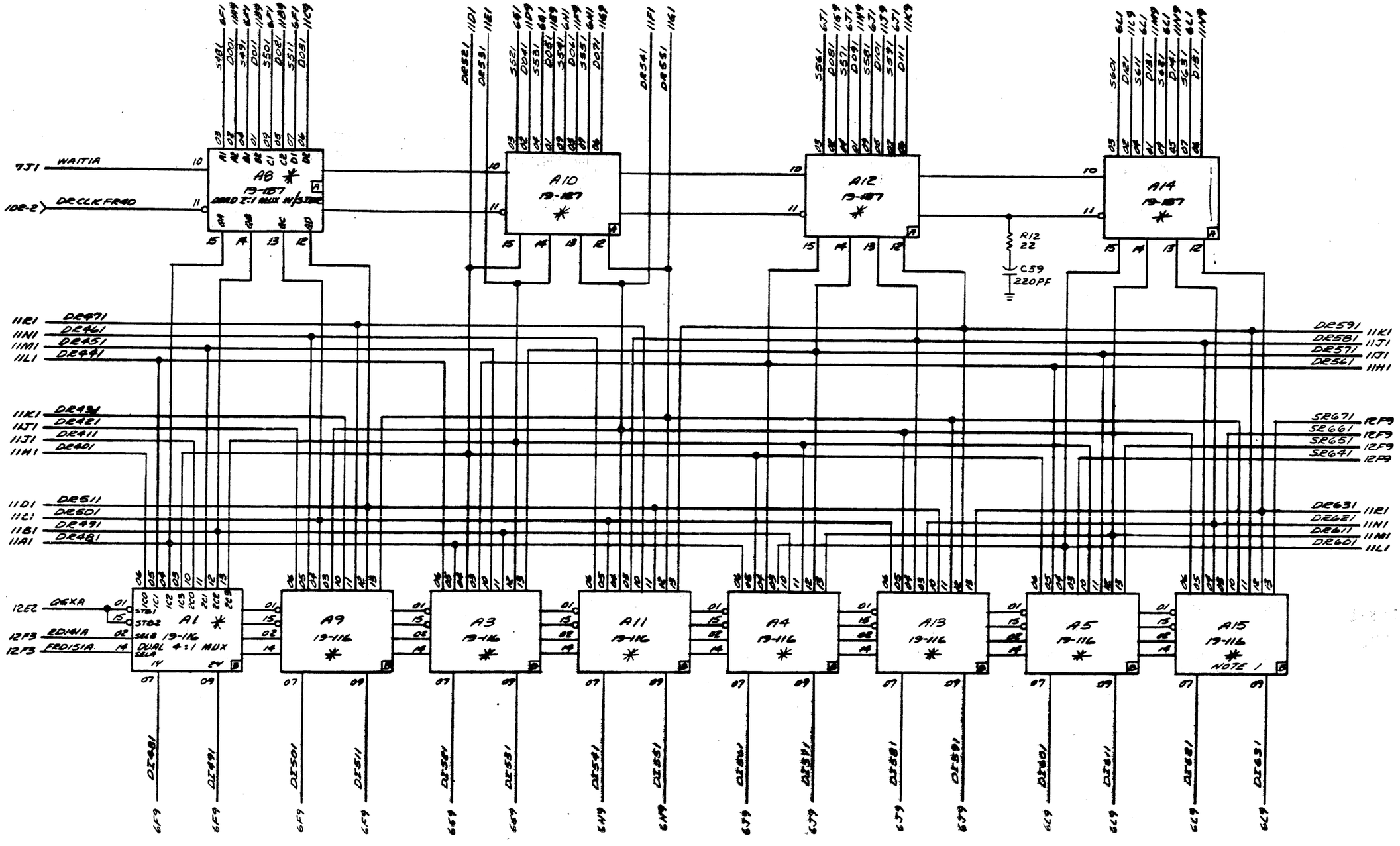

A44
A43
A42
A41
19-184
* NOTE 2
A25
19-068
LOOK AHEAD CARRY GEN.
NOTE 1
R1 1K
R2 1K
C1 TNRH C10 15uF
C11 TNRH C58 .1uF
100-0, 141-0, 100-1, 141-1
101-0, 200-0, 201-0, 140-0, 240-0, 241-0, 101-1, 200-1, 201-1, 140-1, 240-1, 241-1
FY521
FY511
FY501
DEC030
YD021
YD011
YD001
GF08630
EDIII
FRD101
FRD041
FRD081
FRD071
2D061
2D051
RD021
2D031
R3132
Q32IN
E4748
Q4748
CPUCLK.FR10

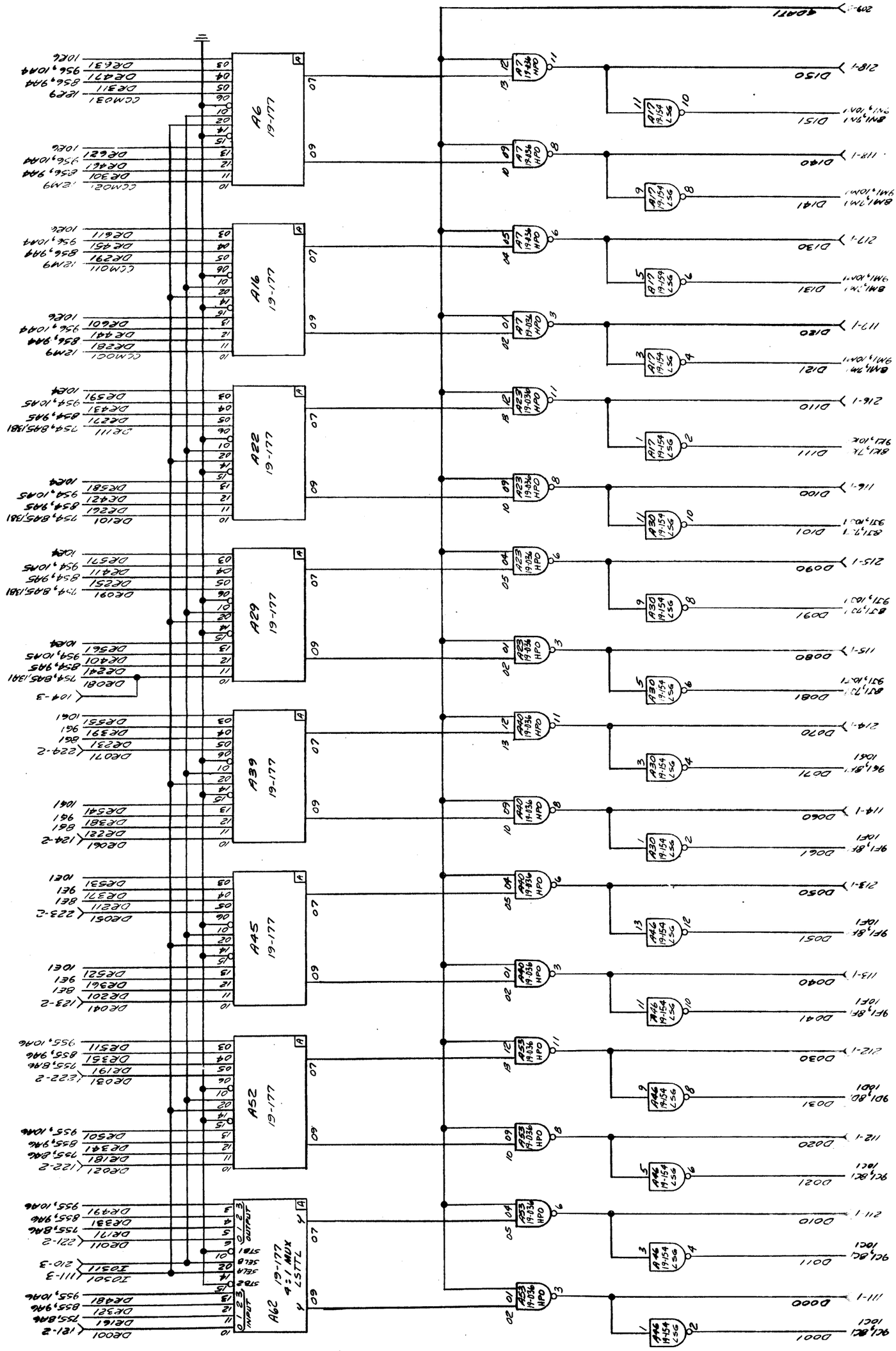

A2
19-068
LOOK AHEAD CARRY GEN.
A18
19-184
NOTE 1
A19
19-184
A20
19-184
A21
19-184
FY321
FY311
FY301
DEC070
4D21
4D11
4D01
GF08630
RD111
FRD101
FRD091
FRD081
FRD071
RD061
RD051
RD041
RD031
R4748
Q4748
RL63
QL63
CPUCLKFRD
CN14
P4863
G4863

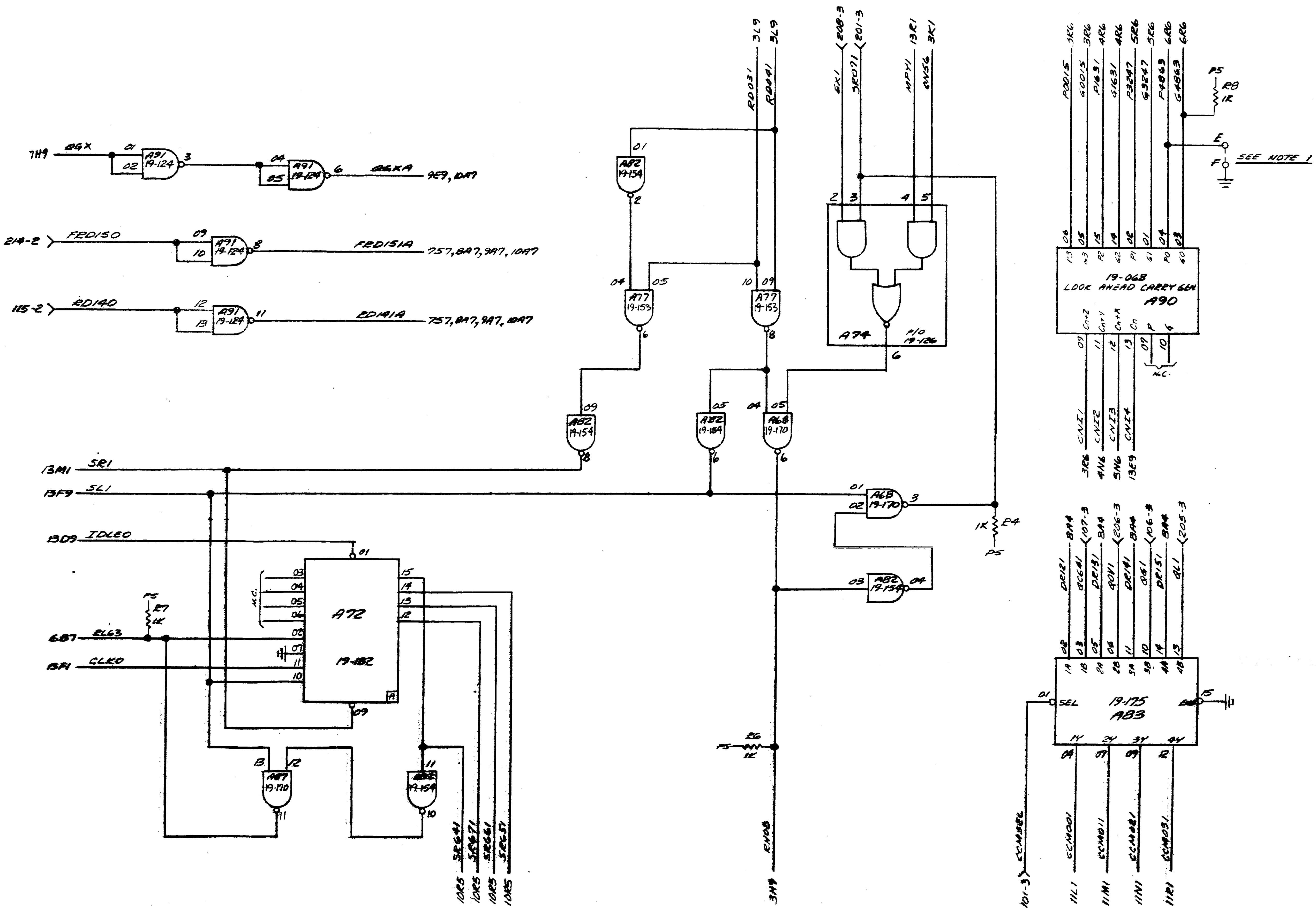

DR00L 19K8, 20J5, 21A5, 22B4 /121-2
/123-2 /124-2 /224-2
105-2
108-3
WAITA
A95 19-83
A13 19-187 QUAD 2:1 MUX W/STOR
A102 19-187
A80 19-187
A78 19-187
WAITI
DRCLKEXD
CNT010
CNT020
CNT040
CNT080
A25 19-059 3A
RD161
CNT160
CNT320
RD181
RD191
RD201
RD171
DR031
DR021
DR011
DRSN
SNMX
R13 22
C60 220 PF
R16 22
C63 220 PF
ORBIT11 /105-3
DR111 11K1
DR101 11J1
DR091 11H1
DR081 11H1
DR191 11C1
DR181 11B1
DR171 11B1
DR161 11A1
DR151 8A4
DR141 8A4
DR131 8A4
DR121 8A4
A143 19-116 DUAL 4:1 MUX
A142 19-116
A100 19-116
A144 19-116
A71 19-116
A81 19-116
A69 19-116
A79 19-116
RD141A 12F3
FRD151A 12D3
DZ001
DZ011
DZ021
DZ031
DZ041
DZ051
DZ061
DZ071
DZ081
DZ091
DZ101
DZ111
DZ121
DZ131
DZ141
DZ151
QSX
P/O 35-632 FPP-A BOARD
P/O 35-633 FPP-B BOARD

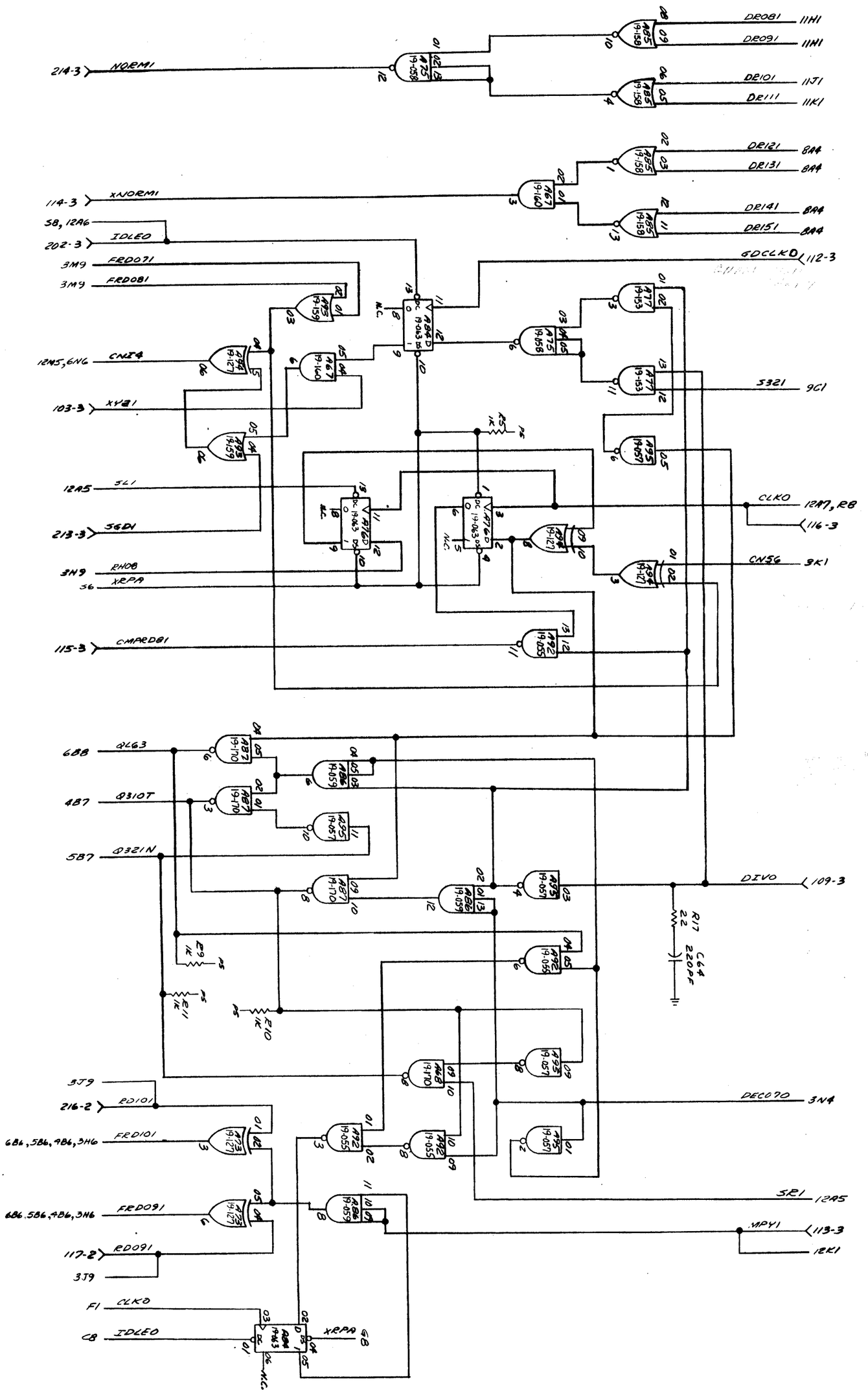

A54
A56
A58
A60
A47
A55
A49
A57
A50
A59
A51
A61
19-117
19-116
DUAL 4:1 MUX
R15
22
C62
220PF
DR271
DR261
DR251
DR241
DR351
DR341
DR331
DR321
DR311
DR301
DR291
DR281
DR151
DR141
DR131
DR121
DR111
DR101
DR091
DR081
DR191
DR181
DR171
DR161
DR01Y
DR11Y
DR21Y
DR31Y
DR41Y
DR51Y
DR61Y
DR71Y
DR81Y
DR91Y
DR01Z
DR11Z
DR21Z
DR31Z
DR41Z
DR51Z
DR61Z
DR71Z
DRCLKFR20
WAITIA
QSX
RDMAIA
FRDISIA

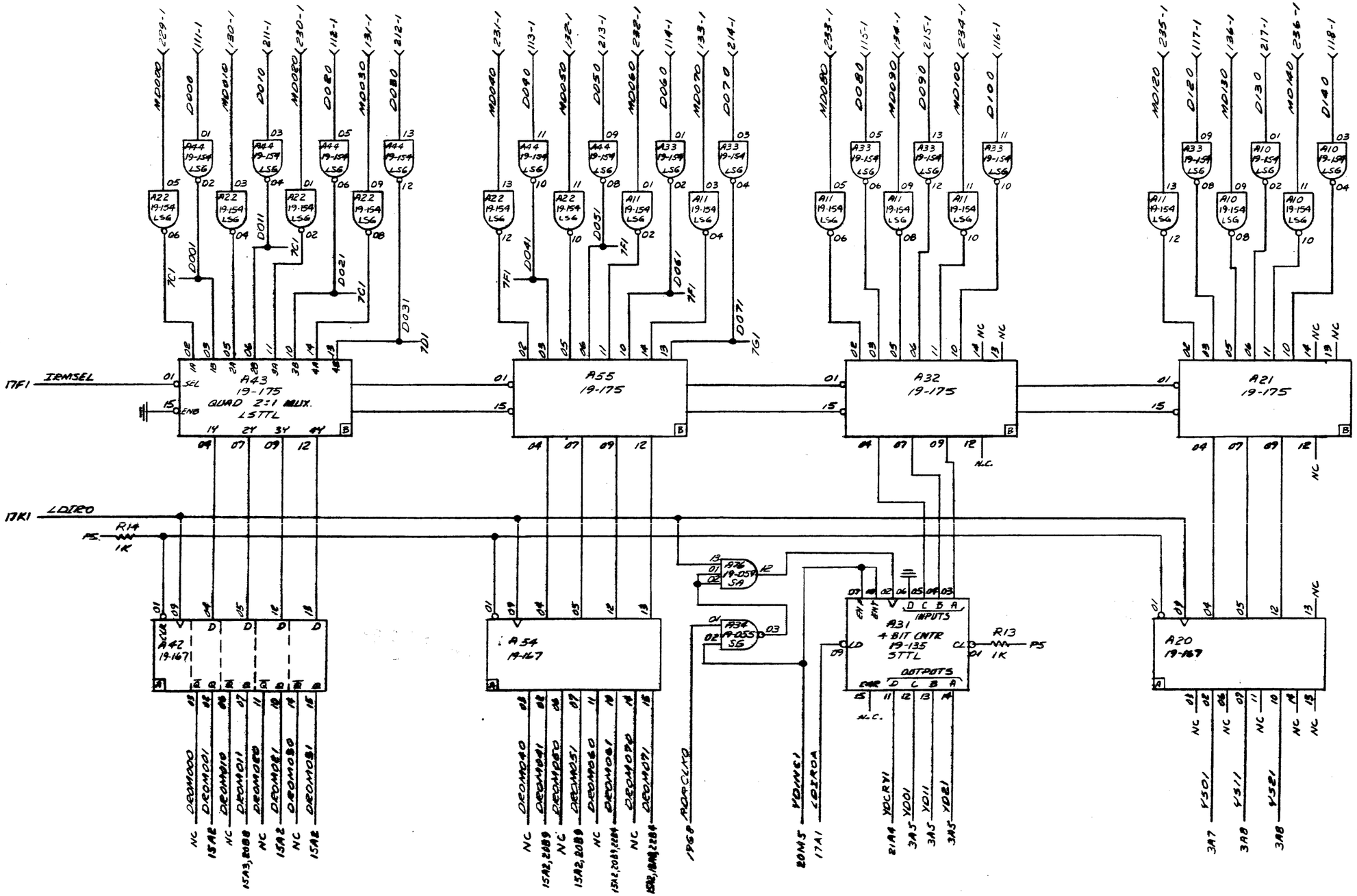

A37
19-187
QUAD 2:1 MUX W/STOR
A35
19-187
A33
19-187
A31
19-187
WAITIA
DRCLKFR30
R14
22
C61
220PF
SEE NOTE 1
DR431
DR421
DR411
DR401
DR471
DR461
DR451
DR441
DE361
DE371
DE381
DE391
DE321
DE331
DE341
DE351
DE401
DE411
DE421
DE431
DE441
DE451
DE461
DE471
A28
DUAL 4:1 MUX
A38
19-116
A27
19-116
A36
19-116
A26
19-116
A34
19-116
A24
19-116
A32
19-116
QGX
RDMIA
FRDI51A

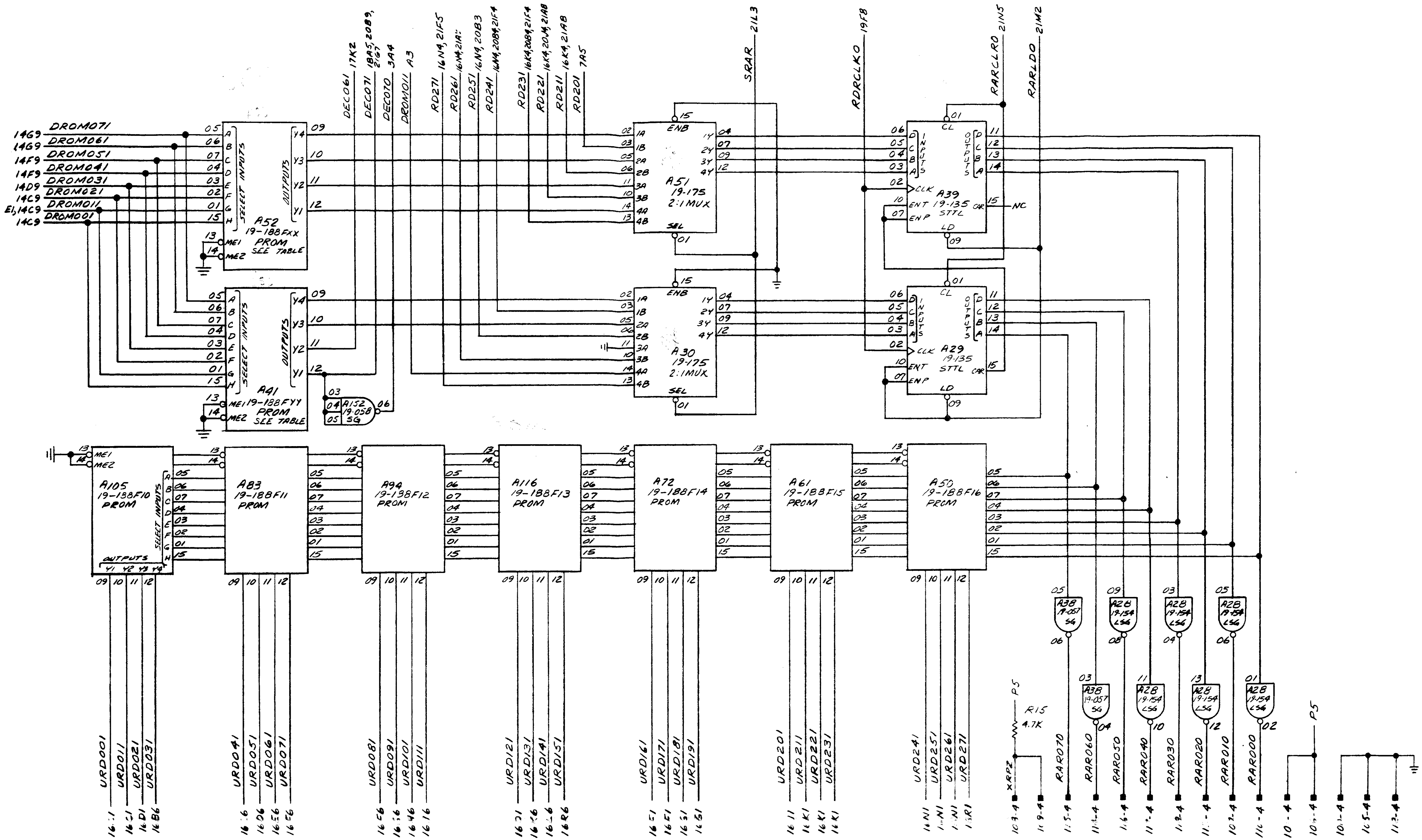

7J1 WAITIA
10E-2 DRCLKFRAD
A8 13-107 QUAD 2:1 MUX W/STORE
A10 13-107
A12 13-107
A14 13-107
R12 22
C59 220PF
11R1 DR471
11N1 DR461
11M1 DR451
11L1 DR441
11K1 DR431
11J1 DR421
11H1 DR411
11D1 DR511
11C1 DR501
11B1 DR491
11A1 DR481
DR591 11K1
DR581 11J1
DR571 11J1
DR561 11H1
SR671 12F9
SR661 12F9
SR651 12F9
SR641 12F9
DR631 11R1
DR621 11N1
DR611 11M1
DR601 11L1
12E2 DRXA
12F3 DRMA
12F3 FRDISIA
A1 DUAL 4:1 MUX
A9 13-116
A3 13-116
A11 13-116
A4 13-116
A13 13-116
A5 13-116
A15 13-116
NOTE 1


A6 19-177
A16 19-177
A22 19-177
A29 19-177
A39 19-177
A45 19-177
A52 19-177
A62 19-177 4:1 MUX TTL/STTL
INPUT 0 1 2 3
OUTPUT 0 1 2 3
STB0
SELA
SELB
STB1
A7 19-154 HPD
A17 19-154 LSG
A23 19-036 HPD
A30 19-154 LSG
A40 19-036 HPD
A46 19-154 LSG
A53 19-036 HPD
D000
D001
D010
D011
D020
D021
D030
D031
D040
D041
D050
D051
D060
D061
D070
D071
D080
D081
D090
D091
D100
D101
D110
D111
D120
D121
D130
D131
D140
D141
D150
D151

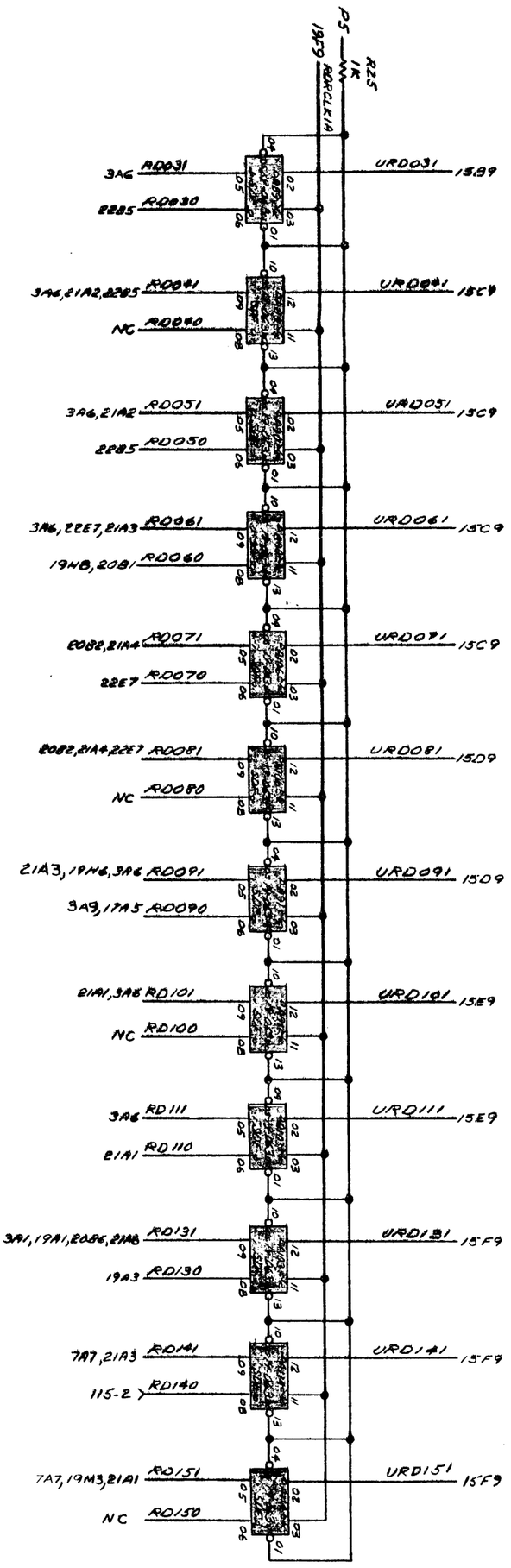


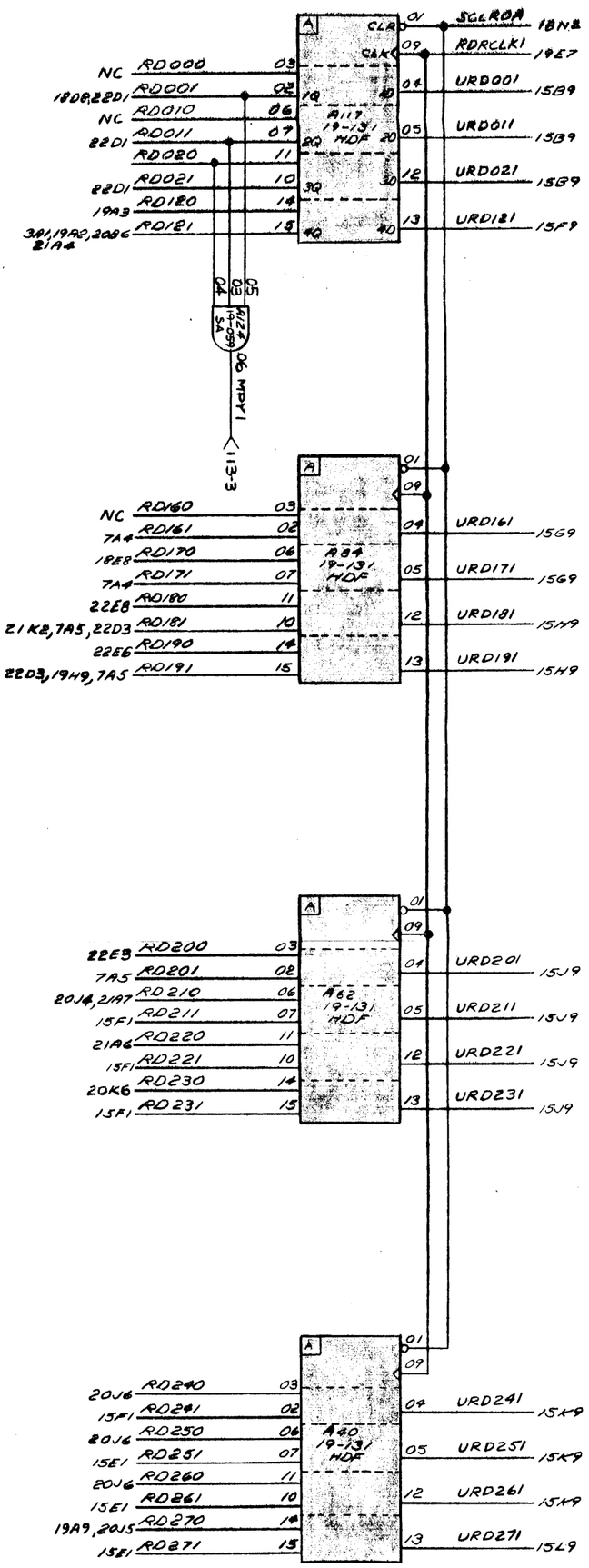

214-3 NORM1
114-3 XNORM1
58, 12A6
202-3 IDLEO
3M9 FRD071
3M9 FRD081
12N5,6NG CNI4
103-3 XY81
12A5 SL1
213-3 S6DI
3N9 RH08
36 XRPA
115-3 CMARD81
688 QL63
487 Q310T
5B7 Q321N
3J9
216-2 RD101
6B4,5B6,9B6,3H6 FRD101
6B6,5B6,9B6,3H6 FRD091
117-2 RD091
3J9
F1 CLK0
C8 IDLE0
XRPA C8
DR081 11H1
DR091 11H1
DR101 11J1
DR111 11K1
DR121 8A4
DR131 8A4
DR141 8A4
DR151 8A4
GDCLKD 112-3
5321 9C1
CLK0 12A7, R8
116-3
CN56 3K1
DIV0 109-3
DECO70 3N4
SR1 12A5
MPY1 113-3
12K1
R17 22
C64 220PF
R9 1K
R11 1K
R10 1K
R25 1K
N.C.

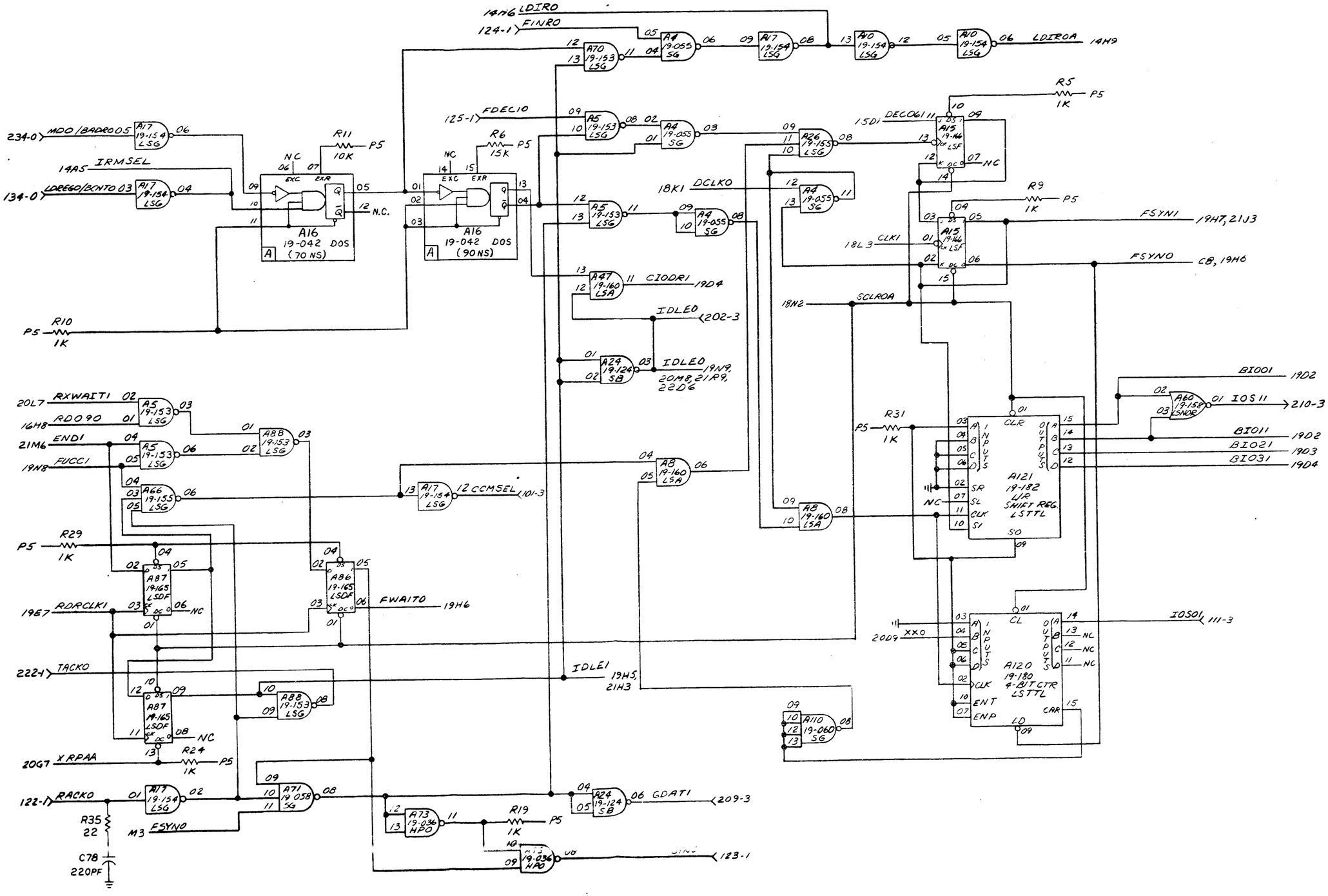

A43 19-175 QUAD 2:1 MUX. LSTTL
A55 19-175
A32 19-175
A21 19-175
A42 19-167
A54 19-167
A20 19-167
A31 4 BIT CNTR 19-135 STTL
A26 19-059 S9
A34 19-055 S6
R14 1K
R13 1K
IRMSEL
LOIRQ
A44 19-154 LSG
A33 19-154 LSG
A22 19-154 LSG
A11 19-154 LSG
A10 19-154 LSG
A33 19-154 LSG

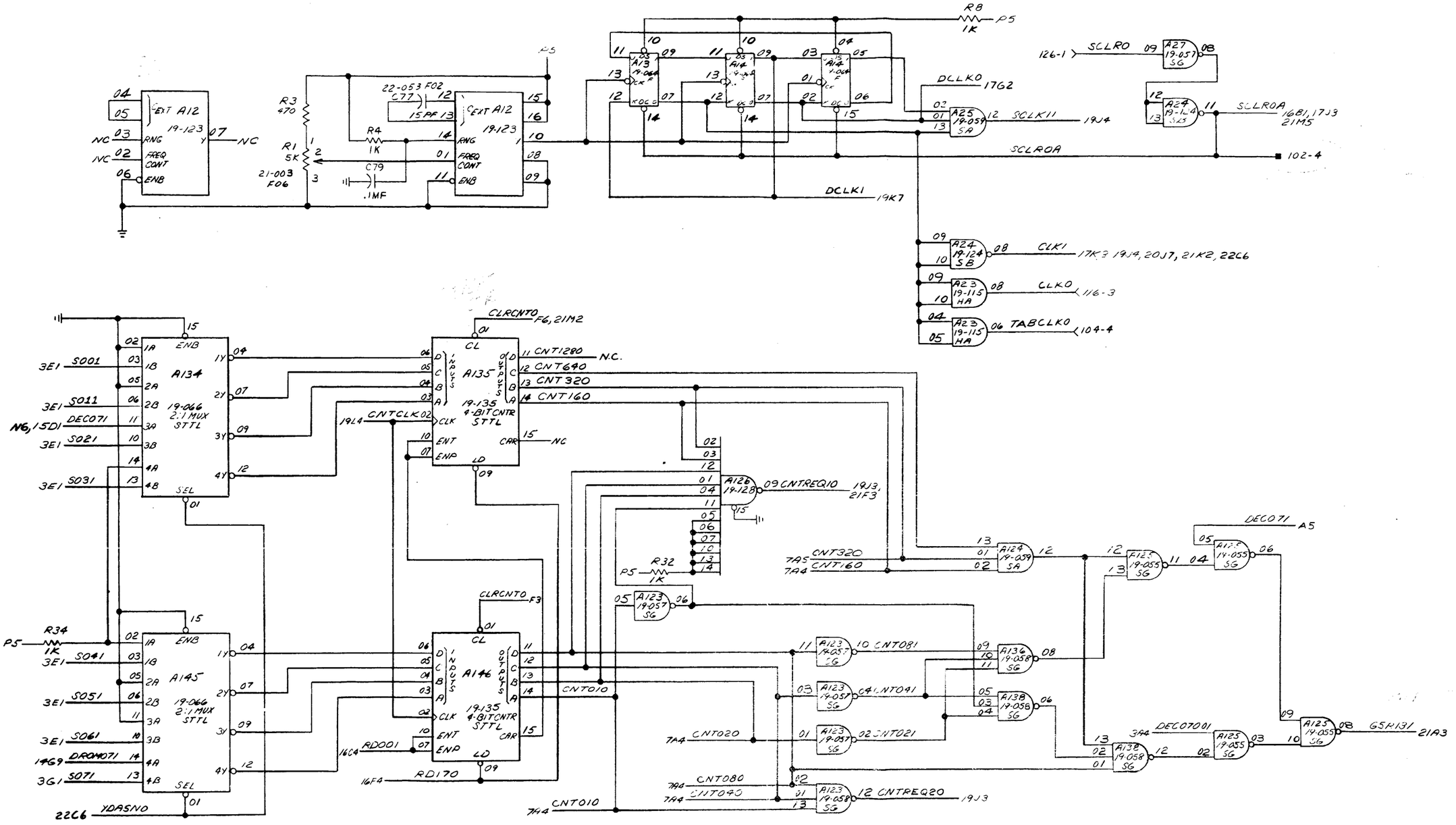


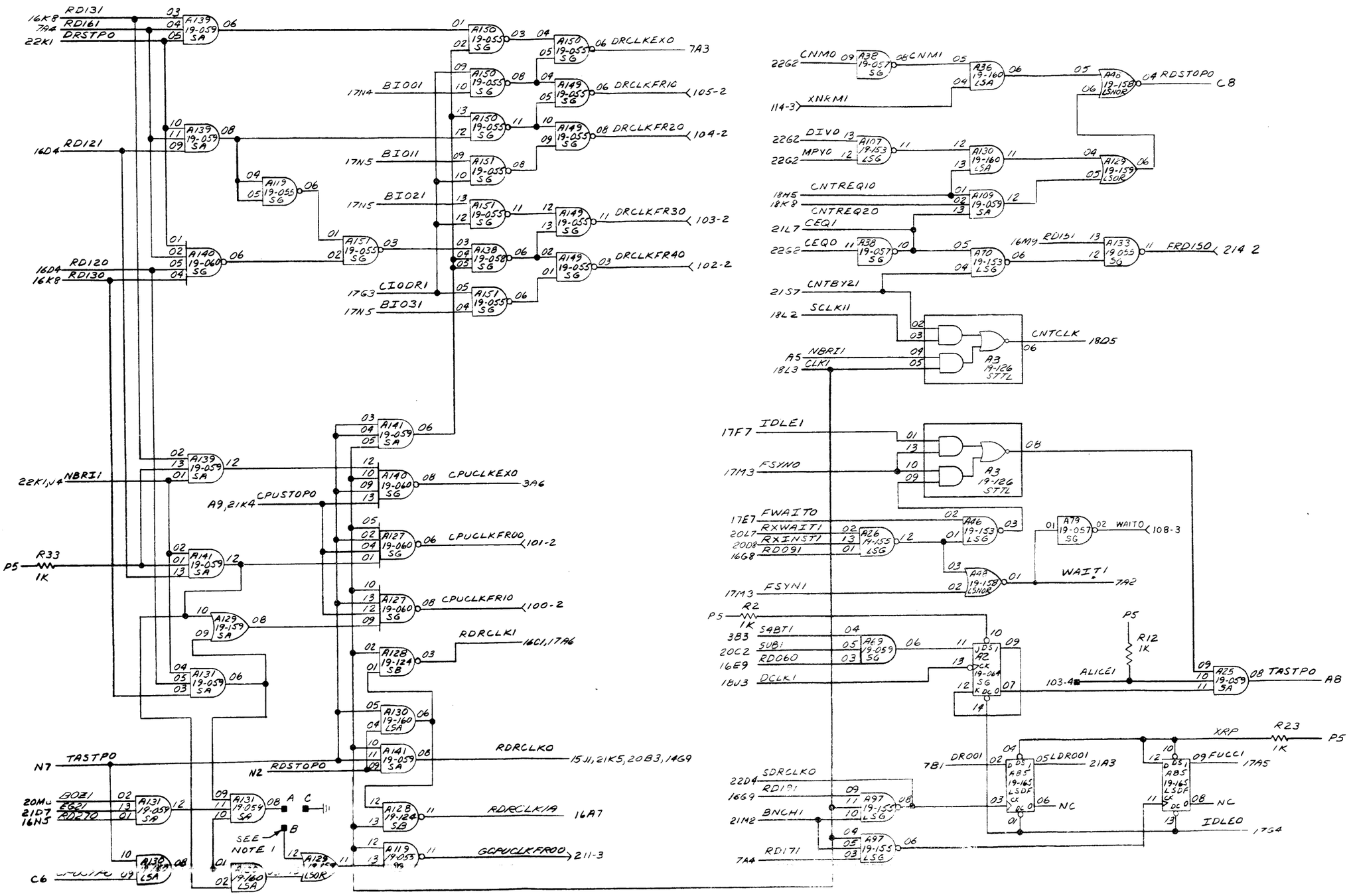
DROM071
DROM061
DROM051
DROM041
DROM031
DROM021
DROM011
DROM001
A52 19-188FXX PROM SEE TABLE
A41 19-188FYY PROM SEE TABLE
SELECT INPUTS
OUTPUTS
DEC061 17K2
DEC071 18A5, 20B9, 21G7
DEC070 3A4
DROM011 A3
RD271 16N4, 21F5
RD261
RD251 16N4, 20B3
RD241
RD231
RD221
RD211 16K4, 21A8
RD201 7A5
SRAR 21L3
A51 19-175 2:1MUX
A30 19-175 2:1MUX
RDRCLKO 19F8
RARCLRO 21N5
RARLDO 21M2
A39 19-135 STTL
A29 19-135 STTL
A152 19-058 SG
A105 19-188F10 PROM
A83 19-188F11 PROM
A94 19-188F12 PROM
A116 19-188F13 PROM
A72 19-188F14 PROM
A61 19-188F15 PROM
A50 19-188F16 PROM
URD001
URD011
URD021
URD031
URD041
URD051
URD061
URD071
URD081
URD091
URD101
URD111
URD121
URD131
URD141
URD151
URD161
URD171
URD181
URD191
URD201
URD211
URD221
URD231
URD241
URD251
URD261
URD271
P5
R15 4.7K
XRPZ
RAR070
RAR060
RAR050
RAR040
RAR030
RAR020
RAR010
RAR000
A38 19-057 SG
A28 19-154 LSG
NC

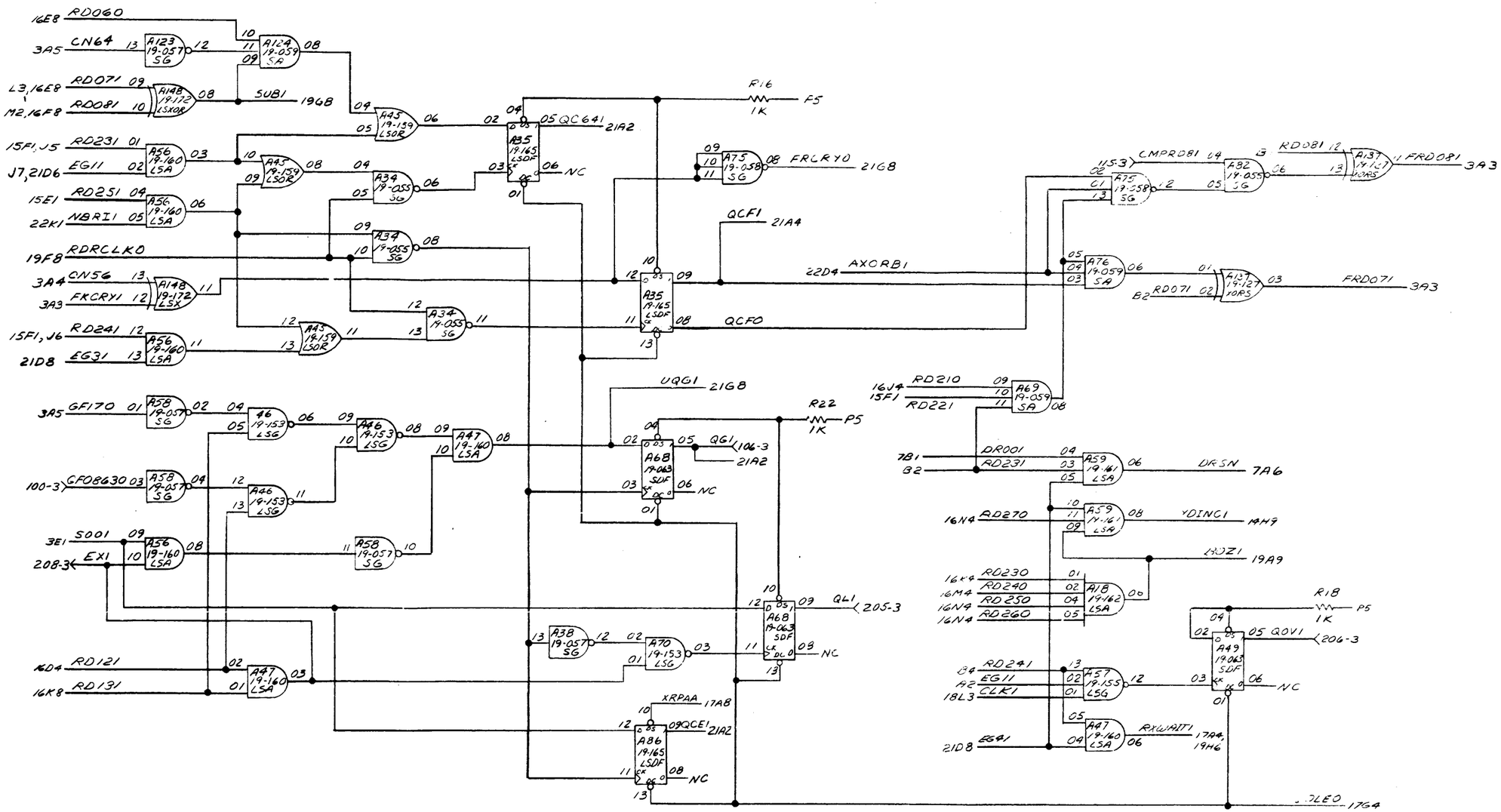

19F9 RDRCLK19
P5
1K
A25
3A6 RD031
URD031 15B9
2285 RD030
3A6,21A2,2285 RD041
URD041 15C9
NC RD040
3A6,21A2 RD051
URD051 15C9
2285 RD050
3A6,22E7,21A3 RD061
URD061 15C9
19N8,20B1 RD060
2082,21A4 RD071
URD071 15C9
22E7 RD070
2082,21A4,22E7 RD081
URD081 15D9
NC RD080
21A3,19N6,3A6 RD091
URD091 15D9
3A3,17A5 RD090
21A1,3A6 RD101
URD101 15E9
NC RD100
3A6 RD111
URD111 15E9
21A1 RD110
3A1,19A1,2086,21A8 RD131
URD131 15F9
19A3 RD130
7A7,21A3 RD141
URD141 15F9
115-2 RD140
7A7,19M3,21A1 RD151
URD151 15F9
NC RD150


A117 19-131 MDF
SGLROA 18N2
RDRCLK1 19E7
NC RD000
URD001 15B9
1808,22D1 RD001
NC RD010
URD011 15B9
22D1 RD011
RD020
URD021 15B9
22D1 RD021
RD120
URD121 15F9
19A3 RD121
3A1,19A2,2086,21A4
MBP1
113-3
A84 19-131 MDF
NC RD160
URD161 15G9
7A4 RD161
1828 RD170
URD171 15G9
7A4 RD171
RD180
URD181 15H9
22E8 RD181
21K2,7A5,22D3 RD190
URD191 15H9
22E6 RD191
22D3,19H9,7A5
A62 19-131 MDF
22E5 RD200
URD201 15J9
7A5 RD201
2014,2197 RD210
URD211 15J9
15F1 RD211
RD220
URD221 15J9
21A6 RD221
15F1
20K6 RD230
URD231 15J9
15F1 RD231
A40 19-131 MDF
20J6 RD240
URD241 15K9
15F1 RD241
20J6 RD250
URD251 15K9
15E1 RD251
20J6 RD260
URD261 15K9
15E1 RD261
19A9,2015 RD270
URD271 15L9
15E1 RD271

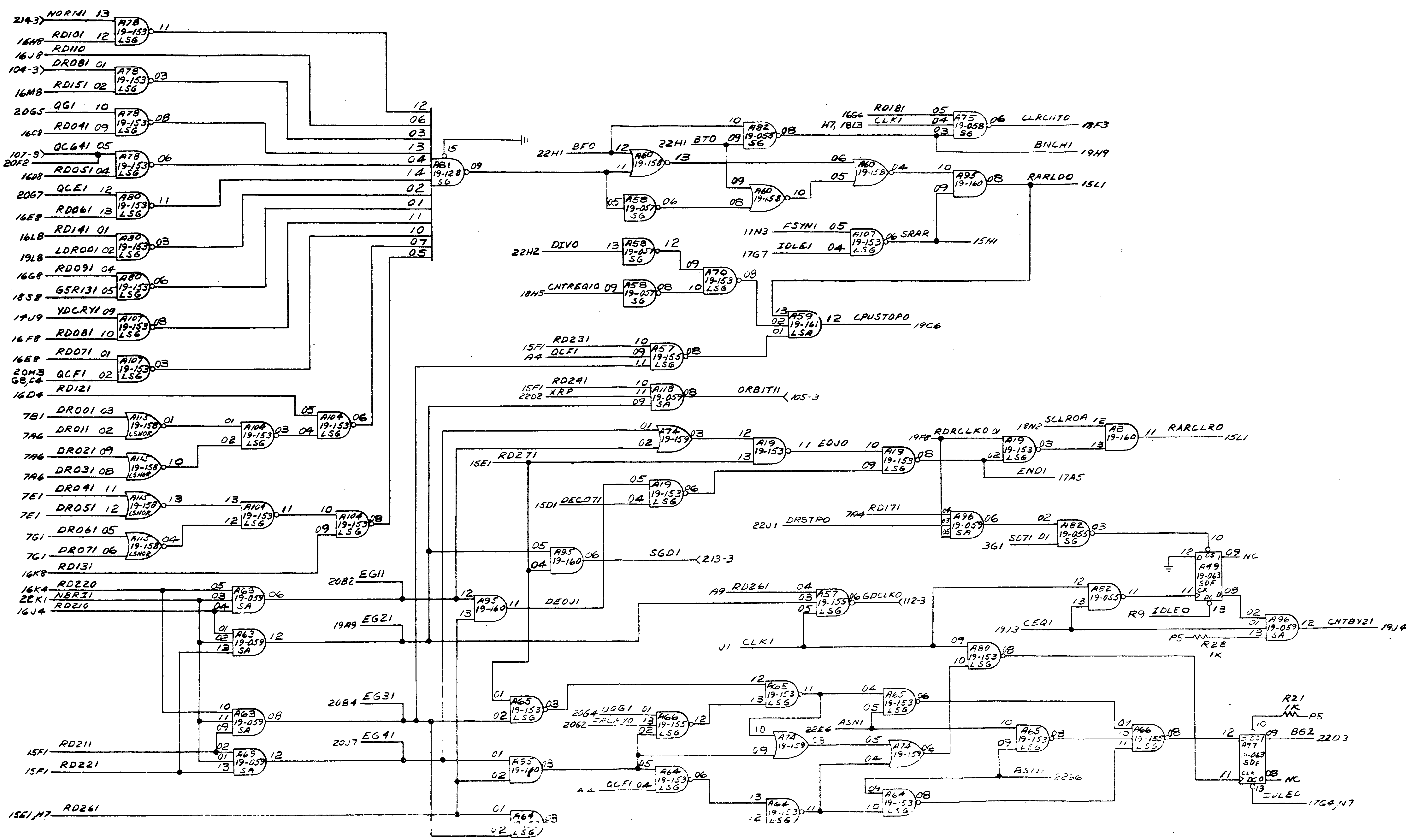

14H6 LDIRO
124-1 FINRO
A10 19-154 LSG
LDIROA 14H9
R5 1K P5
125-1 FDEC10
R6 15K P5
NC
A16 19-042 DOS (90NS)
234-0 MDO/BADRO05
14A5 IRMSEL
134-0 LDREGO/BCNTO03
R11 10K P5
A16 19-042 DOS (70NS)
N.C.
R10 P5 1K
15D1 DECO6
A15 19-166 LSF
NC
18K1 DCLKO
R9 1K P5
FSYN1 19H7, 21J3
18L3 CLK1
FSYNO CB, 19H6
18N2 SCLROA
CIODR1 19D4
IDLEO 202-3
IDLEO 19N9, 20M8, 21R9, 22D6
BIO01 19D2
IOS11 210-3
BIO11 19D2
BIO21 19D3
BIO31 19D4
R31 P5 1K
A121 19-182 U/R SHIFT REG LSTTL
20L7 RXWAIT1
16H8 RDO90
21M6 END1
19N8 FUCC1
12 CCMSEL 101-3
R29 P5 1K
19E7 RDRCLK1
FWAIT0 19H6
2224 TACKO
IDLE1 19H5, 21H3
2009 XXO
IOSO1 111-3
A120 19-180 4-BIT CTR LSTTL
20G7 XRPAA
R24 1K P5
122-1 RACKO
R35 22
C78 220PF
M3 FSYNO
R19 1K P5
GDAT1 209-3
123-1

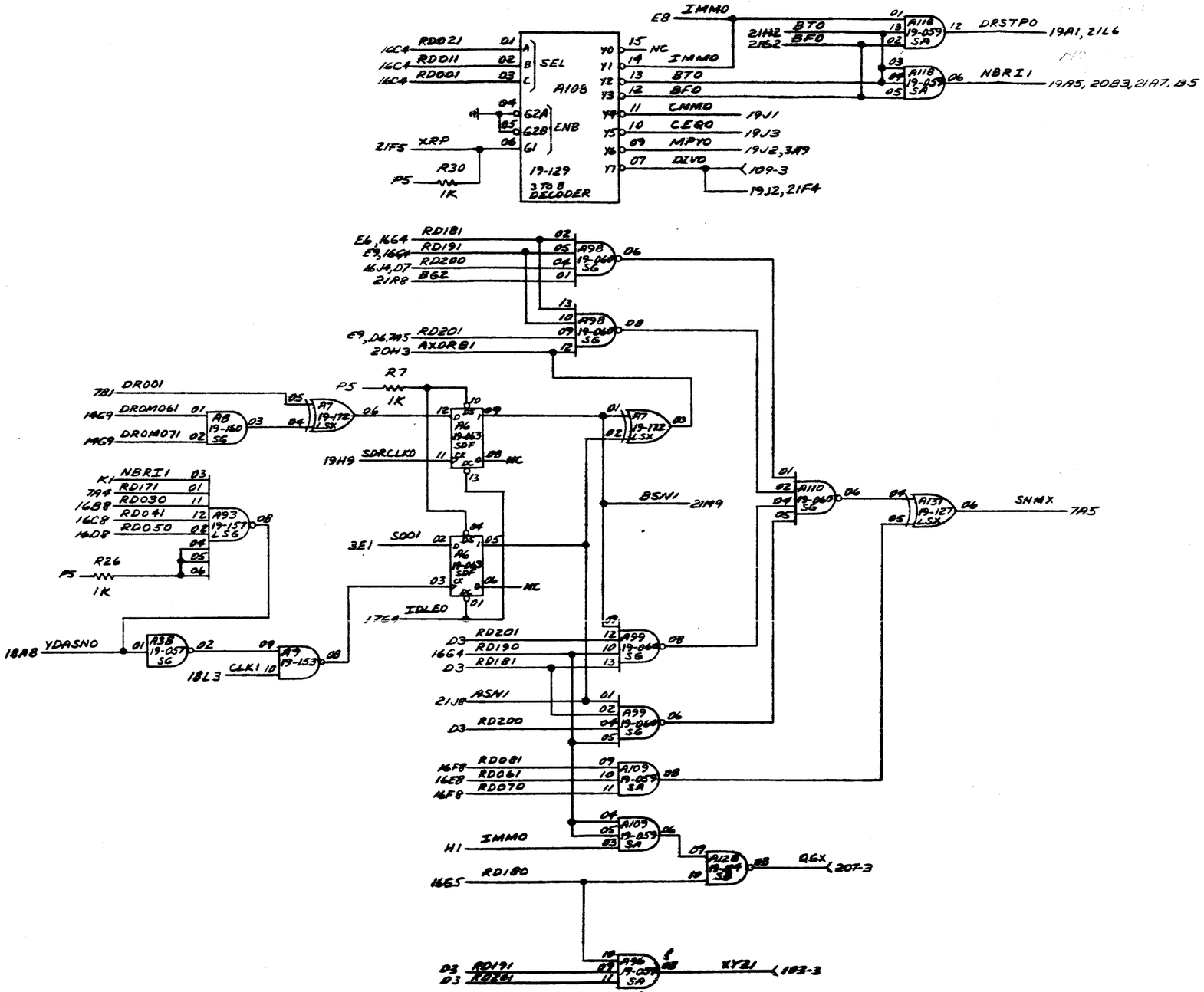

EXT A12
19-123
FREQ CONT
ENB
RNG
NC
R3 470
R1 5K
21-003 F06
R4 1K
C79 .1MF
22-053 F02
C77 15PF
P5
R8 1K
A13 19-064
A14 19-064
A15 1-064
DCLK0 17G2
DCLK1 19K7
A25 19-059 SA
SCLK11 19J4
SCLR0 126-1
A27 19-057 SG
A24 19-L4 SA3
SCLR0A 16B1, 17J3 21M5
102-4
A24 19-124 SB
CLK1 17K3 19J4, 20J7, 21K2, 22C6
A23 19-115 HA
CLK0 116-3
TABCLK0 104-4
A134
A135
A145
A146
ENB
SEL
2:1 MUX STTL
19-135 4-BIT CNTR STTL
CLRCNT0 F6, 21M2
CNTCLK0 19L4
CNT1280 N.C.
CNT640
CNT320
CNT160
CNT080
CNT040
CNT020
CNT010
CNTREQ10 19J3, 21F3
CNTREQ20 19J3
CNT081
CNT041
CNT021
RD001 16C4
RD170 16F4
YDASNO 22C6
DECO71 A5
DECO7001 3A4
GSR131 21A3
A123 19-057 SG
A124 19-039 SA
A125 19-055 SG
A126 19-128
A136 19-058 SG
A138 19-058 SG
R32 1K
R34 1K


RD131
RD161
DRSTP0
RD121
RD120
RD130
R33
1K
TASTP0
NBRI1
CPUSTOPO
RDSTOPO
BIOO1
BIO11
BIO21
BIO31
CIODRI
DRCLKEXO
DRCLKFRIO
DRCLKFR20
DRCLKFR30
DRCLKFR40
CPUCLKEXO
CPUCLKFRUO
CPUCLKFRIO
RDRCLKI
RDRCLKO
RDRCLK1A
GCPUCLKFROO
IDLE1
FSYNO
FSYNI
R2
1K
FWAITO
RXWAIT1
RXINST1
RDOO91
WAITO
WAIT1
S4BT1
SUB1
RDO6O
DCLK1
CNTREQ1O
CNTREQ2O
CEQ1
CEQO
CNTBY21
SCLK11
NBRI1
CLK1
CNTCLK
CNMO
CNM1
XNRM1
DIVO
MPYO
RDSTOPO
R12
1K
ALICE1
TASTPO
SDRCLKO
RD1?1
BNCH1
RD171
DROO1
LDROO1
XRP
R23
1K
FUCC1
NC
IDLEO



DECOUPLING CAPACITORS


NORM1
RD101
RD110
DR081
RD151
QG1
RD041
QC641
RD051
QCE1
RD061
RD141
LDR001
RD091
G5R131
YDCRY1
RD081
RD071
QCF1
RD121
DR001
DR011
DR021
DR031
DR041
DR051
DR061
DR071
RD131
RD220
NBRI1
RD210
RD211
RD221
RD261
EG11
EG21
EG31
EG41
BFO
BTO
DIVO
CNTREQ10
RD231
RD241
XRP
RD271
DECO71
DEOJ1
SGD1
RD181
CLK1
CLRCNTO
BNCH1
RARLDO
FSYN1
IDLE1
SRAR
CPUSTOPO
ORBIT11
EOJO
RDRCLKO
SCLROA
RARCLRO
END1
RD171
DRSTPO
SO71
GDCLKO
CEQ1
IDLEO
CNTBY21
ASN1
BS111
BG2
R21
R28
1K
NC


IMMO
BTO
BFO
DRSTPO
19A1, 21L6
NBRI1
19A5, 2083, 21A7, B5
SEL
A108
19-129
3 TO 8 DECODER
ENB
XRP
R30
1K
NC
CEQO
MPYO
DIVO
109-3
19J2, 21F4
19J1
19J3
19J2,3J9
RD181
RD191
RD200
B62
RD201
AXORB1
R7
DR001
DROM061
DROM071
SDRCLKO
SDF
BSN1
21M9
NBRI1
RD171
RD030
RD041
RD050
R26
SO01
IDLEO
YDASNO
CLK1
18L3
RD190
RD180
ASN1
RD081
RD061
RD070
IMMO
H1
QGX
207-3
SNMX
7A5
XY21
103-3

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