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M48-000, M48-061, M48-062 UNIVERSAL CLOCK (10 - BIT ADDRESS) (M02)

MAINTENANCE MANUAL

Consists of:

Installation Specification	02-240M02R03A20
Maintenance Specification	02-240M02R02A21
Schematic	02-240M02R03D08
Component Locator	35-398M02R01D03
Component Locator	35-757R01D03

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PAGE REVISION STATUS SHEET

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TITLE Universal Clock Maintenance Manual

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1	R03	9/80						
2	R03	9/80						
3/4	R02	9/79						
02-240M02A21								
1	R02	9/79						
2	R00	2/75						
3	R02	9/79						
4 thru 6	R00	2/75						
02-240M02D08								
1 thru 5	R03	2/80						
35-398M02D03								
1 of 1	R01	8/78						
35-757D03								
1 of 1	R01	11/80						

PREFACE

This manual provides the necessary information to install and maintain the M48-000, M48-061, and M48-062 Universal Clock Module. Information on board location, cables, connectors and strap options is provided in the Installation Specification. The Maintenance Specification contains a Block Diagram Analysis, Functional Diagram Analysis, Operation information, Circuit Analysis, Timing Diagrams, and a Mnemonics list. Functional Schematics and Component Locators are provided at the rear of the manual.

02-240M02R03A20
September 1980

UNIVERSAL CLOCK INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information to install the M48-000, M48-061 and M48-062 Universal Clock Module and the external clock option. The module assembly consists of one half board and one 17-177 cable. The half board must be strapped to a blank half board (PERKIN-ELMER 16-398 Half Board Kit) or an active half board (i.e. Memory Protect) to be installed in a chassis designed for full boards. The Universal Clock board, 35-398 or 35-757F01 may be used in either the right or left half position, as required. See Figure 1. The 35-398 Line Frequency Clock is for operation with 12 VAC while the 35-757F01 will function with either 5 VAC or 12 VAC. The 35-757F02 Line Frequency Clock operates on 5 VDC which it receives from the back panel pin 102-0. Therefore the 35-757F02 can only be installed on the 'O' side. (Care should be taken to insure correct priority on RACK0/TACK0 chain). This module assembly is not accompanied by the 17-177 cable. See Table 1.

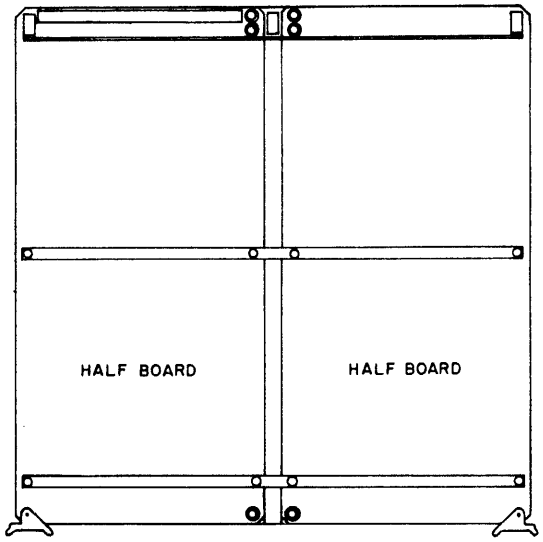

Figure 1. Half-Board Assembly

PCB#	MARKETING#	LINE FREQUENCY OPERATIONAL REQUIREMENTS
35-398	M48-000	12 VAC
35-757F01	M48-062	5 or 12 VAC
35-757F02	M48-061	5 VDC

TABLE 1

2. INSTALLATION

2.1 Unpacking

When the Universal Clock Module is shipped with a system, it is installed at the factory so there is no special unpacking procedure. It is only necessary to insure that the module is properly seated in its connectors. If the module assembly is purchased separately, it should be unpacked carefully and inspected for damage prior to installation.

2.2 Location

The 35-398 or 35-757F01 Universal Clock Module half board, strapped to a blank or active half board, may be installed in any I/O slot, while the 35-757F02 may be installed on any I/O slot on the 'O' side of the chassis. It is preferable to use the highest priority position available. After installing the module, remove the RACK0/TACK0 strap located on the back panel between Terminals 222 and 122 of the selected slot.

NOTES

1. When installing the 35-398 or 35-757F01 Universal Clock Module on the Model 5/16, the real time clock built into the 5/16 must be disabled. This is done by removing the ground wire between C3 and ground (Slot 5, Pin 141-1 to 127-1) on the CPU backpanel.

2. When installing the 35-398 or 35-757 F01 Universal Clock Module on a Series Sixteen CPU, the built-in real time clock must be disabled. This is done by disconnecting C3 wire from consolette to CPU backpanel lug. Also, add jumper Slot 5 from Pin 200-0 to 203-0 on CPU backpanel.

2.3 Cables and Connectors

Connect the 17-177 cable as shown in Figure 2. Note that the cable is long enough to allow the board to operate on an extender.

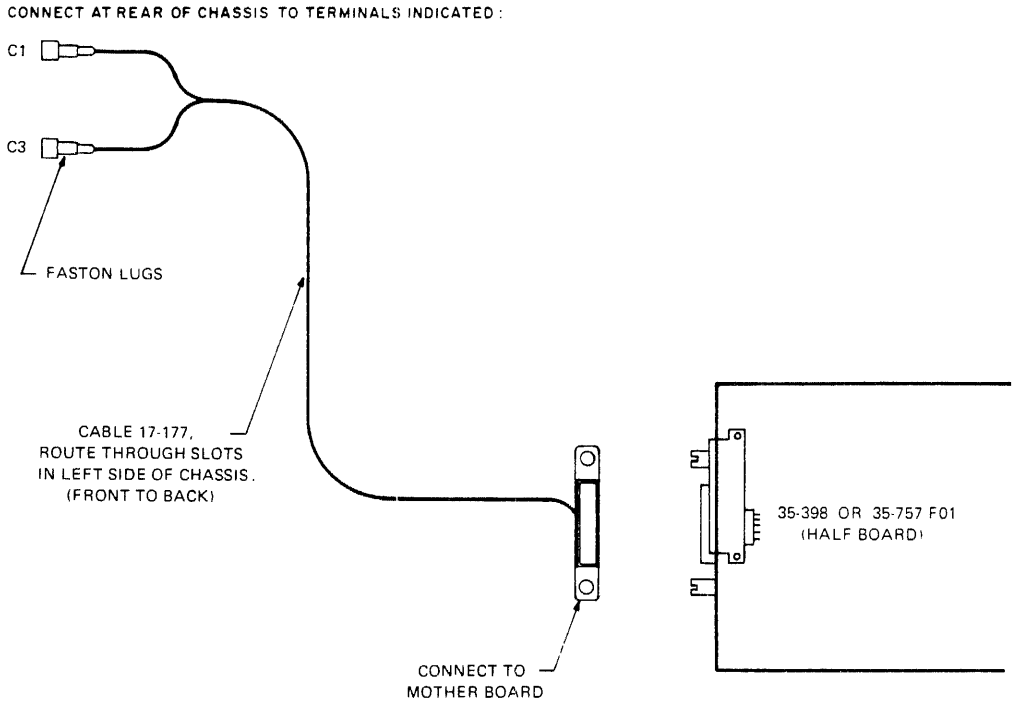

Figure 2. Cable Connections

3. EXTERNAL CLOCK OPTION

To use an external time base oscillator perform the following steps: (Refer to Schematics 02-240M02D08.)

1. Strap Test Point (TP) W to Test Point (TP) X.
2. Connect the external oscillator, via twisted pair, to Test Point EXT and Test Point EXG (TP EXG is ground).

Internal termination of the Universal Clock Module is shown in Figure 3.

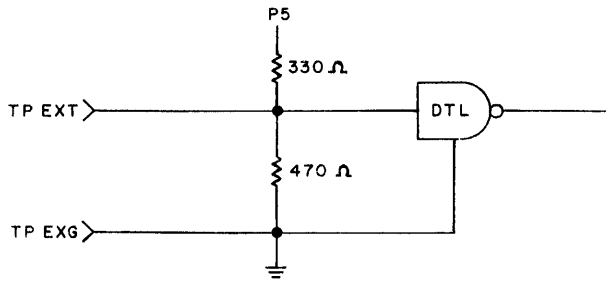

Figure 3. External Oscillator Connections, and Internal Termination

UNIVERSAL CLOCK MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-240M02, 02-240F01M02 and 02-240F02M02 Universal Clock Module consists of two I/O devices; 1. the programmable Precision Interval Clock (PIC), and 2. the AC Line Frequency derived Clock (LFC). The PIC provides the user with a Processor interrupt and a program accessible counter which is based on a dynamically variable (thru program control) Precision Resolution Clock and Interval Counter. The LFC is derived from the AC power line and provides the user with a Processor interrupt at twice the line frequency.

Since the PIC and LFC are completely independent of each other, they are covered in separate sections of this specification. Section 2 describes the PIC, and Section 3 describes the LFC. Both sections contain block diagram and functional schematic analysis, timing information, and sufficient notes to maintain this interface. A mnemonic list common to both sections is provided at the end of this specification.

2. PRECISION INTERVAL CLOCK

2.1 Block Diagram Analysis

As shown in the PIC block diagram on Sheet 4 of 02-240M02D08, the Count Input Buffer and Resolution Select input Buffer are loaded from the Multiplexor Bus. Upon initial start up or at the end of an Interval period, this information is transferred to the Interval Counter and Resolution Select Register. The Resolution Select Register enables one of the four Resolution Clock rates available from the Clock Divider. The selected Clock Divider output Count Pulse (COUNT0) decrements the Interval Counter until it reaches zero, the next count pulse produces the PIC Interrupt (XNT1) which is sent to the attention circuits, and the process is repeated. The Interval Counter may be monitored through the Counter Output Buffer to the Multiplexor Bus.

2.2 Functional Diagram Analysis

Refer to Functional Schematic 02-240M02D08 for the following analysis.

With the exception of common I/O bus buffering, the PIC logic is detached from the LFC. Status, Command, and Data Byte information is provided in the Programming Manual 29-531.

2.2.1 Operation. Initialization (SCLR0)(1L8) insures that the PIC is placed in the Disarm Mode by resetting the Enable PIC Interrupt (ENAX1) (1J1) and the PIC Disarm (XDSRM0) (1J2) flip-flops. The Resolution and Counter Input Buffers (2C1-9), and the Overflow (OVFL) (2H2), Data Byte Count (DBC1) (2H8), and Write Byte (WBC0) (2H3) flip-flops are cleared. In addition, the Address Select flip-flops are set (ADX1) (1J3), (ADH1) (1J4).

The Resolution and Interval data is initially loaded into the PIC's Input Buffers (2E1-9) in two data bytes by Load Data Low (LDL0)(2M6) and Load Data High (LDH0)(2M7). A Start Command (CMGX0·DAL21) momentarily sets the START1 flip-flop (1J8), the next Raw Clock pulse resets it (RCLK0)(1H8). This action resets the PIC Interrupt flip-flop (XNT0) (2G7), and loads the Resolution Select Register (2E1-2) and the Interval Counter (2E3-9) from the Input Buffers. XANT1 (3J2) goes active if enabled.

The Resolution Register outputs (SMS1, SHMS1, STMS1, and SCK1) enable one of the Clock Divider outputs (3D1-9) to produce COUNT0 (3M7). COUNT0 starts to decrement the Interval Counter. When zero, the next count pulse activates the borrow output from the Interval Counter (2E3-9) and the XNT1 flip-flop (2G7) momentarily sets, it is reset by CLK1. This causes an interrupt to be queued in the PIC Attention flip-flop (XANT1)(3J1) if not in the Disarm Mode. Attention goes active (ATN0)(3N1), if enabled. The XNT0 pulse reloads the Resolution Select and Interval Counter Registers from the Input Buffers. Operation now proceeds as previously described.

During the Interval (Interval Counter has not reached zero), the Input Buffers may be altered by two data bytes containing a new Resolution and/or Interval. When the present Interval concludes, the new data will be loaded from the Input Buffer in place of the old. However, if the Interval times out between the start of the first data byte transferred and the end of the second data byte transferred, the Write Byte Count flip-flop (WBC)(2H3) causes the Overflow flip-flop to set (OVFL)(2H2). This stops the Clock by holding START0 low (1J7). The clock will restart after the completion of the second data byte transfer or on receipt of a Start Command. OVFL remains set until the execution of a Sense Status, an Acknowledge Interrupt instruction, or Initialization.

The PIC is provided with an Output Buffer (3G1-9) so that the Interval Counter may be interrogated without disturbing its operation, by using two data byte transfers. The Output Buffer is normally loaded on every CLK1. The first Data Request gated (DRG0)(1R4) by Raw Clock (RCLK1)(1J9) latches up the Output Buffer by setting the Data Request SYNC flip-flop (DRSYN1)(2J7), which in turn holds Load Buffered Count high (LDBC0)(2K7). The Read Data Low (RDL0)(2L6) is activated and SYN0 is returned. The falling edge of DRG1 sets the Read Byte Counter. The second DRG1 activates Read Data High (RDH0)(2L7) and SYN0 is returned. The falling edge of the second DRG1 resets the Read Byte Counter, which in turn resets the DRSYN1 flip-flop.

2.2.2 Circuit Analysis. It should be noted that numerous 19-035 four bit up-down counters are used as registers and perform no counting operations. The One-Shot (3R6) which resets the PIC Attention flip-flop (XATN1)(3J1) is set to produce a 175 nanosecond pulse (approximately).

2.3 Timing

Refer to Figure 1.

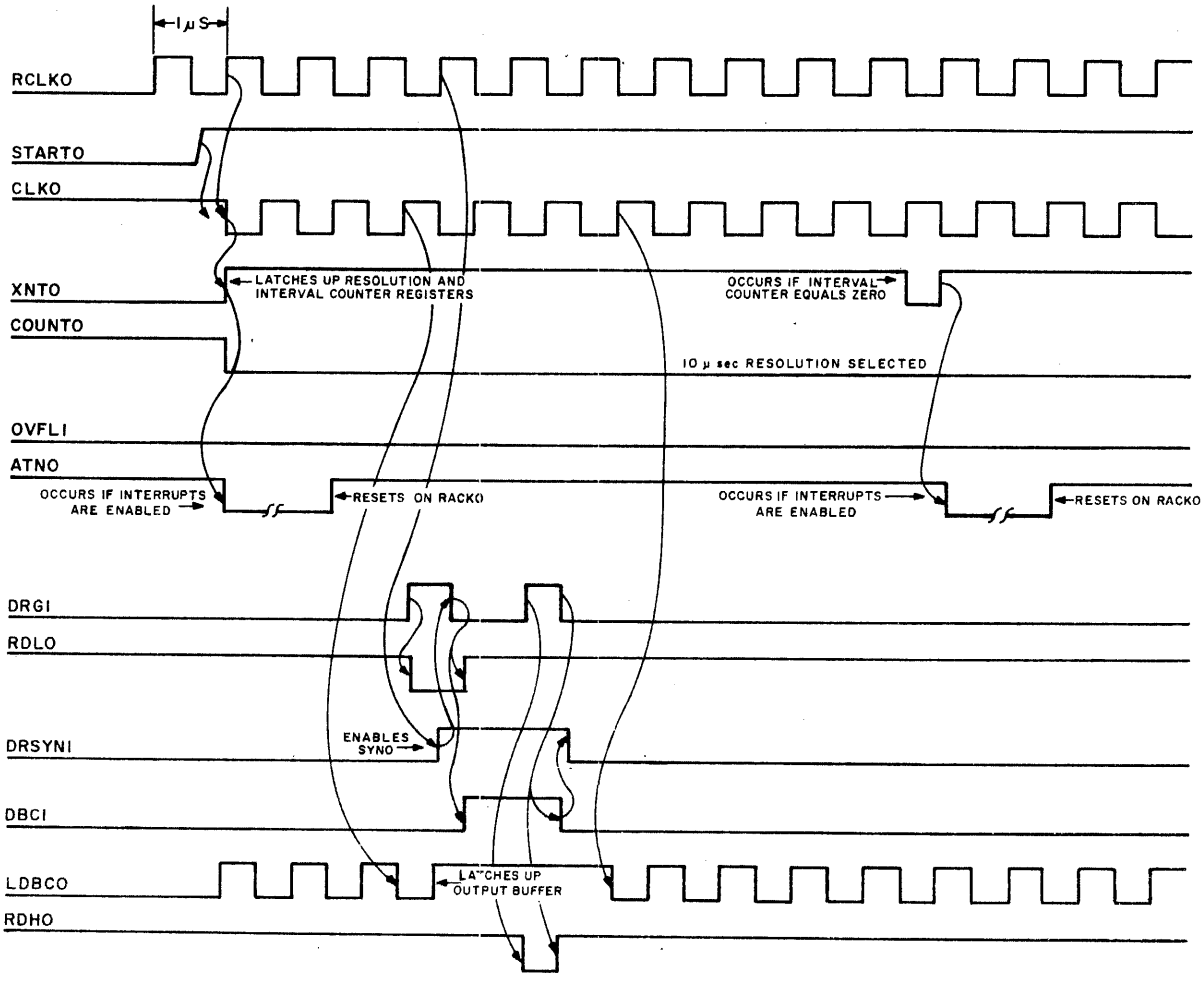

Figure 1. Precision Interval Clock Timing Diagram

2.4 Routine Maintenance, Adjustments, and Tests

The PIC requires no adjustments. The accuracy of the crystal oscillator should be checked with a digital frequency meter on RCLK0 (1J9) at Test Point Z (1MHZ ± .01%).

2.5 Troubleshooting

The PIC may be reasonably tested using a static check. Refer to the Programming Specification, 02-240M02A22, for set up procedures. Test Program 06-133 provides a dynamic check which can be monitored by appropriate test equipment.

3. LINE FREQUENCY CLOCK

3.1 Block Diagram Analysis

As shown in the LFC block diagram (Figure 2), the power supply provides a 5 VDC pulsed, 5 VAC or 12 VAC (depending on the system used) from which the LFC Interrupt (HNT1) (3R8) is derived. Although shown separately for clarity, the LFC I/O logic (Address, Command and ATN circuits) is combined with that of the PIC. This is described in Section 4.

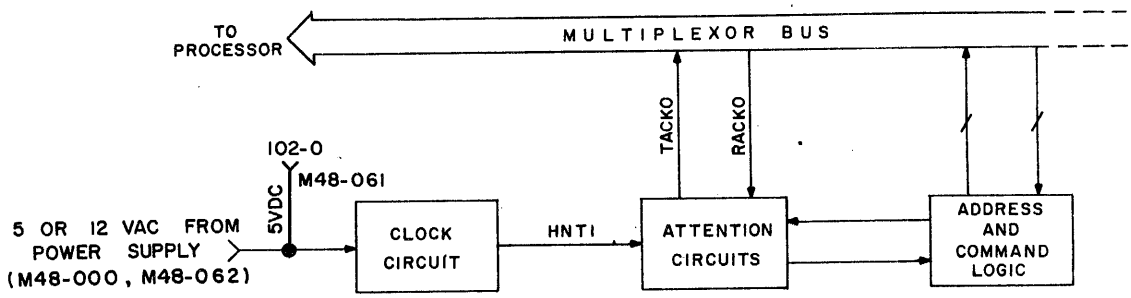

Figure 2. AC Line Derived Clock Block Diagram

3.2 Functional Diagram Analysis

As shown on Sheet 3 of Schematic 02-240M02D08, the clock circuit is driven by the 12 VAC or 5 VAC (M48-000 or M48-062) output from the system power supply when using 12 or 5 VAC. A full wave bridge rectifier, followed by a zero voltage detector whose output is fed through two gates, produces the HNT1 pulse (3R8) at twice the line frequency.5 VDC, when used is fed directly to the zero voltage detector. The LFC is placed in the Disarm Mode by SCLR0, resetting the Enable LFC Interrupt (ENAH1) (1J5) and the LFC Disarm (HDSRM0) (1J5) flip-flops. The LFC responds only to the Enable and Disable Commands. If the LFC is not in the Disarm Mode, HNT1 will toggle the LFC Attention flip-flop set (HATN1) (3K6) at twice the line frequency. Attention (ATN0) (3N1) is activated, if enabled.

4. PIC AND LFC I/O FUNCTIONAL ANALYSIS

The addresses of the PIC and LFC differ only by the state of Bit 15. The PIC address is always even (Bit 15 inactive), while the LFC address is always odd(Bit 15 active). The output from the PIC Address flip-flop (ADX1) (1J4) and LFC Address flip-flop (ADH1) (1J4) gates the control lines (DR0, DA0, SR0, and CMD0) to their respective logic. The Clock can respond to any of 1024 addresses depending on Hex Switch setting.

The interrupt logic (Sheet 3) is arranged so that the PIC has the highest interrupt priority. Refer to the Programming Manual, 29-531 for Command, Status, and Data Byte information.

5. MNEMONICS

The following list provides a brief description of each mnemonic found in the Universal Clock. The source of each signal on the Schematic Drawing, 02-240M02D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AD	Address - Bit-7 of device address returned on SRG.	3S4
ADH	Address LFC - Active when the LFC address is recognized.	1J4
ADR	Address - Decoded address.	1G3
ADRS	Address - The Processor presents an Address Byte on Data Lines D06:15. The device controller accepts the address Byte and responds with a SYN.	1K1
ADX	Address PIC - Active when the PIC address is recognized.	1J4
AG001:061	Address Gate Lines - Selected straps which generate a unique device address.	1F2-8
ATN (Test Point U)	Attention - Any device desiring to interrupt the Processor will activate the ATN line and hold this line until an ACK is received from the Processor.	3N1
ATSYN	Attention Synchronize - Strobes the address of the interrupting device to the Processor.	3S4
BCT00-11	Buffered Count Output - Output lines of Output Buffer.	3H2-8
CLK	Clock - Raw Clock gated.	1L9
CMD	Command - The Processor presents a Command Byte on Data Lines D08:15. The device controller accepts the Command Byte and responds with a SYN.	1K2
CMGH	Command Gated for LFC - Command gated by ADH.	1R5
CMGX	Command Gated for PIC - Command gated by ADX.	1R2
CNT00-11	Counter Output - Output lines from Interval Counter.	2F3-8
COUNT (Test Point S)	Count - Count pulse at selected Resolution Rate.	3M7
D060:150	Data Lines - Data Lines D060:150 are used to transfer one eight bit byte of data between the Processor and the device. One ten bit address or command byte is transferred from the Processor to the device over Data Lines 6:15 or D08:15 respectively when accompanied by either an Address (ADRS) or a Command (CMD) control line. One byte of data is transferred from the Processor to the device when accompanied by the Data Available (DA) control line. The device, in response to an Acknowledge (ACK) control line or a Sense Status (SR) control line, sends ten bits of address or a byte of status information to the Processor over Data Lines D06:15 or D08:15 respectively. In response to a Data Request (DR) control line, the device sends an eight bit byte of data to the Processor. The device always sends a Synchronize (SYN) signal to the Processor to indicate that it has either received the data from the Processor or that it has sent the data to the Processor. The SYN signal is removed immediately after the Processor removes the control line.	1A2-8

MNEMONIC	MEANING	SCHEMATIC LOCATION
DA	Data Available - The Processor presents data on Data Lines D080:150 for transfer to the device. The device controller accepts the low byte and responds with a SYN.	1K3
DAG	Data Available Gated - Data Available gated by ADX.	1R3
DAL00:70 01:71	Data Available Lines - Data Lines D080:150 buffered double rail for data transfer to the device.	1D2-8
DBC	Data Byte Count - Toggles on DAG or DRG.	2J8
DR	Data Request - The device controller presents data to Data Lines 8:15 followed by a SYN.	1K4
DRG	Data Request Gated - Data Request gated by ADX.	1R4
DRSYN	Data Request SYN - Enables SYN on DRG.	2J7
ENAH	Enable LFC Interrupt - Gates HATN to ATN.	1J5
ENAX	Enable PIC Interrupt - Gates XATN to ATN.	1J1
EXC	External Clock - External time base oscillator connection.	1H9
EXG	External Ground - Ground for EXC.	1H9
HATN	LFC Attention - Queue flip-flop for LFC Interrupt.	3K6
HDSRM	LFC Disarm - Holds HATN reset, when active.	1J5
HMS	100 microseconds - Clock Divider output for 100 microseconds.	3D6
HNT (Test Point V)	LFC Interrupt - Pulsed at twice line frequency.	3S?
LDBC	Load Buffered Count - Loads Output Buffer.	2K7
LDH	Load Data High - Loads high byte of Input Buffer	2L7
LDL	Load Data Low - Loads low byte of Input Buffer	2L7
MS	1 millisecond - Clock Divider output for one millisecond.	3D8
OVFL (Test Point R)	Overflow - Set on XNT· DBC	2H2
RACK	Receive Acknowledge - Control line activated by the Processor in response to an interrupt.	3G4
RCLK (Test Point Z)	Raw Clock - Buffered output of internal or external time base oscillator.	1J9
RDH	Read Data High - Enables High Byte from Output Buffer to data lines.	2L7
RDL	Read Data Low - Enables Low Byte from Output Buffer to data lines.	2L6
SCLK	Select Clock - Enable Clock Divider output for one microsecond.	2F1

MNEMONIC	MEANING	SCHEMATIC LOCATION
SCLR	System Clear - This is a metallic contact to ground that occurs during Power Fail, Power Up, or Initialize.	1L8
SHMS	Select 100 microseconds - Enable Clock Divider output for 100 microseconds.	2F1
SMS	Select one millisecond - Enable Clock Divider output for one millisecond.	2F1
SR	Status Request - The device controller must present device status to Data Lines D08:15 followed by a SYN.	1K3
SRG	Status Request Gated - Status Request gated by ADX.	1R4
SSTRT	Set Start - Sets Start flip-flop.	2K1
START	Start - Start Clock. Enables CLK1.	1K8
STMS	Select 10 microseconds - Enable Clock Divider output for 10 microseconds.	2F1
SYN	Synchronize - This signal is generated by the device to inform the Processor that it has properly responded to a control line.	1S1
TACK	Transmit Acknowledge - System daisy chain control line to the I/O system.	3S3
TMS	10 microseconds - Clock Divider output for 10 microseconds.	3D4
WBC	Write Byte Count - Toggles on DAG only.	2H4
XATN	PIC Attention - Queue flip-flop for PIC interrupt.	3J1
XDSRM	PIC Disarm - Holds XATN reset when active.	1J2
XNT (Test Point T)	PIC Interrupt - Pulsed on completion of Interval Count.	2G6
XRP	1K ohm resistor to P5 (+5VDC).	2F9

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REVISIONS
RELEASED FOR PRODUCTION
ENG. MC DATE 2/26/75
AREA L5 : ADDED I.C. A42. A31-02 WAS CONN TO A23-11. REVISED SHT 2. ADDED MANUAL NO AREA N9. AREA N9: 35-398M02 WAS R00
WTA | 3757 | 9-14-78 | R01
ADDED SHT 5 RESVD. SHT 3,4 AREA N9 ADDED 35-757 F01 & F02
JT | 4008 | M | 9-4-79 | R02
REVISION CONT'D AREA D9

NOTES:
1. STRAP TO GROUND TO USE EXTERNAL CLOCK.
2. STANDARD ADDRESS IS X'6C' AND '60'.

REVISED SHTS 1 & 5 35-757 F01 & F02 WERE R00.
KR | 4238 | M | 1-31-80 | R03

USED IN MANUAL 29-427

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

UNIV. CLK	35-757 F01 R01
UNIV. CLK	35-757 F02 R01

NOTE
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET	REV LEVEL	3	1	1	1	1
INDEX	SHEET NO	1	2	3	4	5

	NAME	TITLE	DATE
SCALE—	J.K. BIELSKIE	DRAFT	12-6-74
TOLERANCE	R. CRAIG	CHK	2-26-75
	T. CISSA	ENGR	2-26-75
	R. CHANEK	G.L.	2-26-75
	J. PISTRICK	MGR	2-26-75

TITLE FUNCTIONAL SCHEMATIC
UNIVERSAL CLOCK
TASK NO 03138
DWG NO 02-249M02R03
SHEET OF 1 — 5

BRUNING 44-231 24538

PERKIN ELMER
Computer Systems Division

IC2 DAL01
IC3 DAL11
IC4 DAL21
IC5 DAL31
IK8 XRP
M7 LDHO
IN7 SCLR1
46 19-035 4 BIT COUNTER CNT DWN CNT UP LOAD CLEAR BORROW CARRY N.C. N.C. P5
45 19-035 SMS1 3J8, SHMS1 3J7, STMS1 3J7, SCLK1 3J7, NC, NC
L5 OVFL1
IR3 DAGO
G6 XNT1
19-017 HG, 19-003 G, SSTRTO 1K7
IR3 SRGO
19-009 G, 19-004 G, 19-045 J-K FF, R (TP), NC, SCLR0A 1S8
XRP
IC5 DAL41
IC6 DAL51
IC7 DAL61
ID8 DAL71
36 19-035 NC NC
35 19-035 CNT001 3E2, CNT011 3E2, CNT021 3E2, CNT031 3E2, NC NC
K7 DAG1
19-004 G, 19-045 J-K FF, NC, 10 WBC0
44 19-035 NC NC
43 19-035 CNT041 3E4, CNT051 3E5, CNT061 3E5, CNT071 3E5, NC NC
M6 LDLO
IK8, START1 09
3D3 CLK1 06
IK8 START0 12
19-045 J-K FF, Y (TP), XNT1, F2, 3K2
XRP
COUNT0 3N7
IR2 CMGX0
1S8 SCLR0A
47 19-024 HA
34 19-035 NC NC
33 19-035 CNT081 3E7, CNT091 3E7, CNT101 3E7, CNT111 3E8, NC
IR3 DAGO
IR4 DRGO
19-003 G, 29 19-004 G
IK8, IK5 DRSYNO 3A1
19-045 J-K FF, DBC1, DBCO
1E2 AG001
3H4 BCT041
14 19-038 DATA INPUTS 1 OUTPUT 1, STROBE 1, SELECT A, SELECT B, DATA INPUTS 2 OUTPUT 2, STROBE 2 P5
19-036 HP, D080 1A2, D090 1A3, D100 1A3, D110 1A4
1E3 AG011
3H4 BCT051
1E4 AG021
3H5 BCT061
1E4 AG031
3H5 BCT071
19-016 HG, 19-025 HA
IR3 SRGO
3S4 ATSYNO
1E5 AG041
3H1 BCT001
3H7 BCT081
G1 OVFL1
3D3 CLK1
19-017 HG
16 19-038, D120 1A5, D130 1A6
1E6 AG051
3H2 BCT011
3H7 BCT091
19-003 G, RDLO, LDLO A7, LDHO A2, RDHO
1E6 AG061
3H2 BCT021
3H7 BCT101
17 19-038, D140 1A7
3S4 ADO
3H2 BCT031
3H7 BCT111
18 19-036 HP, D150 1A8

NOTES

REVISIONS			
AREA J7: REMOVED MNE11 'DRSYN1' & SHT LEG IK5 FROM A23-11. AREA J6: ADDED SHT LEG IK5 TO DRSYNC			
DFTA	3757	9-14-72	R01

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC UNIVERSAL CLOCK
TASK NO. 03138
DWG NO. 02-240M02 R01 003
SHEET 2-5

BRUNING 44-231 15043

PERKIN ELMER

Systems Division

2J6 DRSYNO

19-003 G

11 — 19-035 4 BIT COUNTER — A

INPUTS: D, C, B, A

OUTPUTS: D, C, B, A

COUNT DWN, COUNT UP, LOAD, CLEAR

BORROW CARRY

P5

1M9 CLKO

CLK1 1H7, 2J5, 2F7 J7

19-036 HP

R18 1K

TMSI J7

21 — 19-035 — A

P5 R9 1K

HMSI J7

32 — 19-035 — A

1K8 XRP

1K8 START1

MSI J8

1K8 STARTO

25 — 19-035 — A

2G3 CNTO01

2G3 CNTO11

2G3 CNTO21

2G4 CNTO31

BCTO01 2L5

BCTO11 2L6

BCTO21 2L8

BCTO31 2L9

LDBCO

24 — 19-035 — A

2G5 CNTO41

2G6 CNTO51

2G6 CNTO61

2G6 CNTO71

BCTO41 2L1

BCTO51 2L2

BCTO61 2L3

BCTO71 2L4

26 — 19-035 — A

2G8 CNTO81

2G8 CNTO91

2G8 CNTO101

2G8 CNTO111

BCTO81 2L5

BCTO91 2L6

BCTO101 2L8

BCTO111 2L9

1K8 XRP

19-045 HF

2H6 XNTI

1J2 XDSRMO

S5 RXATNO

C33 100 PF

R24 100

122 RACKO

R25 1K

1J5 HDSRMO

RHATNO

1J1 ENAX1

XATNI

R13 1K

19-089

SCLR0A 198

1J6 ENAHI

HATNI

XRP 1K8

5L2 HNTI

19-042 ONE SHOT

ATNO <223

TACKO <222

ATSYNO 2J5, 1R3 1A8

AD0 2L8

R10 6.8K C23 47PF

R8 6.8K C19 47 PF

RXATNO F3

53 — 19-026

2F1 SCLK1 / 223 CLK1

2F1 STMSI / F4 TMSI

2F1 SHMSI / F6 HMSI

2F1 SMSI / F8 MSI

COUNTO 2E8 (TP)

100, 141 P5

C1-C4, C34-C37 15 MF 25 V

C6-C17, C20-C22, C25-C33 0.1 MF

209, 241

NOTES

REVISIONS

RMVD. AREA H5 TO S8 TO SHT5 AREA D2 TO L2 AREA J6 HNTI WHS S5

NAME / TITLE / DATE

DRAFT

CHK

ENGR

DIR ENG

TITLE FUNCTIONAL SCHEMATIC UNIVERSAL CLOCK

TASK NO 03133

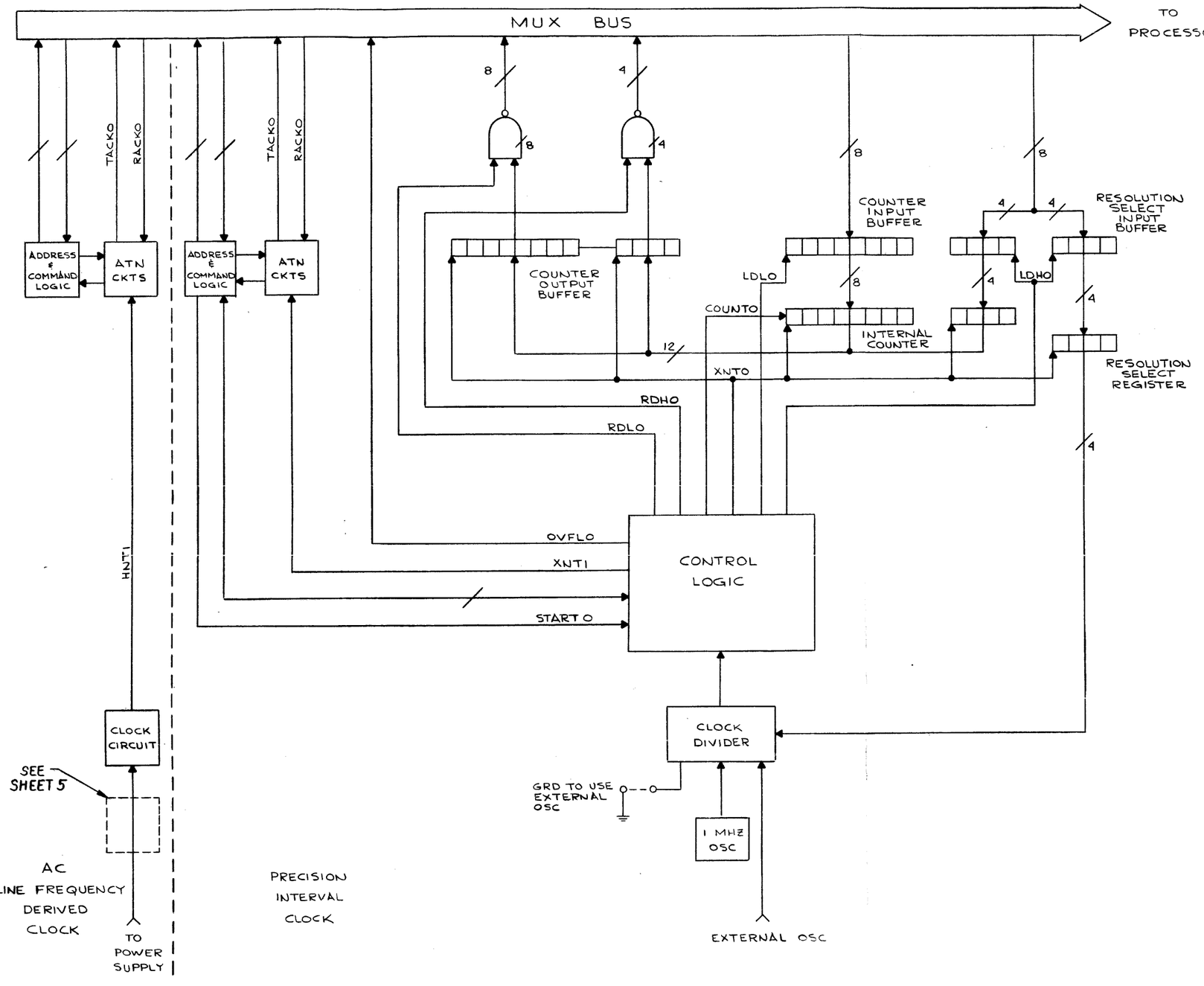
DWG NO 02 240 A02 5 1 003

SHEET 3 OF 5

BRUNING 44-231 15043

PERKIN ELMER
Systems Division

REVISIONS				
AREA AB ADDED DIAGRAM & NOTE SEE SHEET 5				
KR	[illegible]	4008	M	9-12-79	R01



BACK PANEL MAP

ROW 1	ROW 2	TERM NO.
P5	GND	41
		40
		39
		38
		37
		36
		35
		34
		33
		32
		31
		30
		29
		28
		27
CLRO		26
STPCLKO		25
		24
SYNO	ATNO	23
RACKO	TACKO	22
	DAO	21
DRO	CMDO	20
SRO	ADRSO	19
D140	D150	18
D120	D130	17
D100	D110	16
D080	D090	15
		14
		13
		12
		11
		10
		09
		08
		07
		06
		05
		04
		03
		02
		01
P5	GND	00

CONN 'A' PIN ASSIGNMENT

ROW 1	ROW 2	TERM NO.
C1	C3	04
		03
		02
		01
		00

TEST POINT INDEX

DESIG	MNEM	LOC
R	OVFLI	2H1
S	COUNTO	3M7
T	CLKO	1L9
Y	XNTI	2F2
Z	ECLKO	1H3
EXC		1G8
EXG		1G9

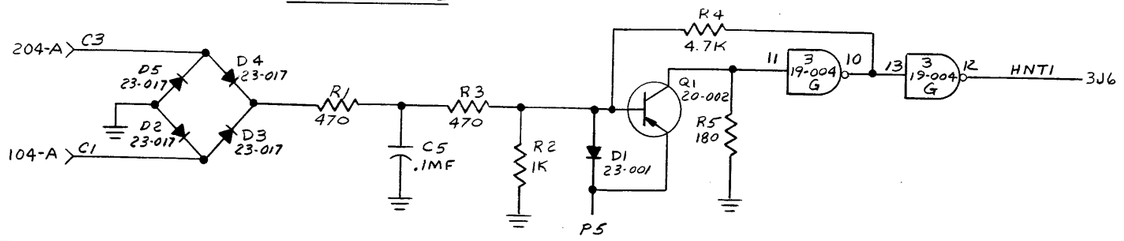
NOTES

NAME		TITLE	DATE
		DRAFT	
		CHK	
		ENGR	
		DIR ENG	

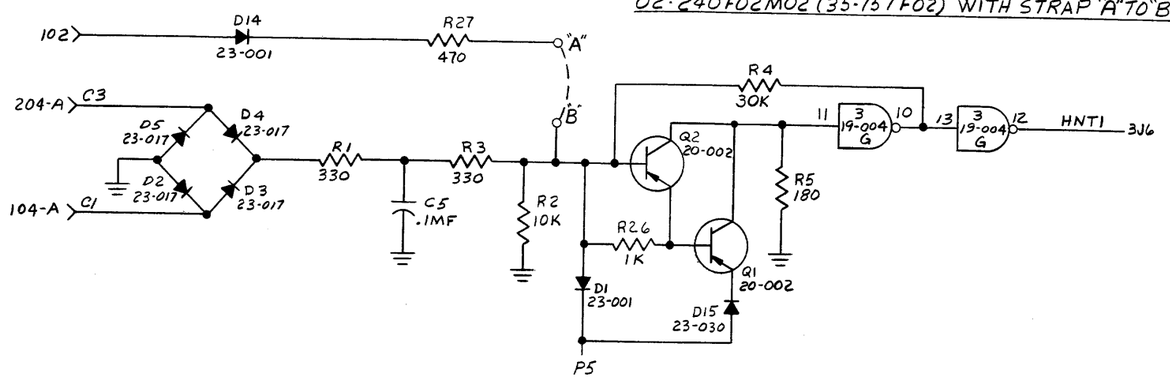
TITLE FUNCTIONAL SCHEMATIC
UNIVERSAL CLOCK
TASK NO. 03138
DWG NO. 02-240M02 Rev 008
SHEET OF 4 - 5

BRUNING 44231 15043

02-240 M02



02-240F01M02 (35-757F01) WITHOUT STRAP "A" TO "B"
02-240F02M02 (35-757F02) WITH STRAP "A" TO "B"



NOTES

BRUNING 44-131 40579

REVISIONS					
ARCA H9, R4 WAS 47K.					
KR	QV	4238	M	1-31-80	R01

UNLESS OTHERWISE SPECIFIED			
SCALE:		TOLERANCE:	
DIMENSIONS ARE IN INCHES		.XXX ±.005 .X ±.03 .XX ±.02 ANGLES ±1°	
NAME		TITLE	DATE
	J.TAMULEVICIUS	DES / DFT	8-31-79
		SUPV	
		CHK	
		ENG	
		MGR	
		QC	

PERKIN-ELMER

Computer Systems Division
Oceanport, N.J. 07757

TITLE FUNCTIONAL SCHEMATIC
UNIVERSAL CLOCK

TASK	SHT
DWG 02-240 M02 R01 D08	5 - 5

RELEASED FOR PRODUCTION
MFG. ENG. (NV) DATE 2-1-75

15.38 REF

7.44 REF

APP SIDE

25-45-69

C1 40 + C2 40 + C3 40 + C4 40 +

C34 40 + C35 40 + C36 40 + C37 40 +

4 INSTALL FROM SOLDER SIDE (2 PLACES)

5 (LAST STRAP NO. IS 2)

4 INSTALL FROM APP SIDE (4 PLACES)

49 INSTALL FROM APP SIDE (9 PLACES)

1

SEE NOTE 1

54

46 REF

1 REF

DETAIL A

NOTES:
1. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

CAPACITORS	C1 THRU C37
DIODES	D1 THRU D13
I Cs	A1 THRU A60
RESISTORS	R1 THRU R25
TRANSISTOR	Q1
CRYSTAL	Y1

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	2-1-75
R. CLIFFORD	CHK	2-26-75
T. CASSIDY	ENG	
R. BARKER	QC	2-26-75
J. PIECZKOWSKI	MGR	2-26-75

ASSEMBLY, PRINTED CIRCUIT UNIVERSAL CLOCK

03138

35-398M02R01 003

SHT 1 OF 1

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 12-4-79

15.38 REF

7.44 REF

APP SIDE

25-644

EXG
EXG
Z

GROUND

4 INSTALL FROM SOLDER SIDE (2 PLACES)

5

49 INSTALL FROM APP SIDE (11 PLACES)

4 INSTALL FROM APP SIDE (4 PLACES)

1

FO2 ONLY (SEE VARIATION TABLE)

SEE NOTE 1

54
46 REF
1 REF

DETAIL A

NOTES:
1. CONTACTS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

VARIATION TABLE		
FO1	WITHOUT STRAP	A TO B
FO2	WITH STRAP	A TO B

PERKIN ELMER

REVISIONS

STRAPS	1-5
CAPACITORS	C1 THRU C37
DIODES	D1 THRU D15
ICs	A1 THRU A60
RESISTORS	R1 THRU R27
TRANSISTOR	Q1 THRU Q2
CRYSTAL	Y1

NAME	TITLE	DATE
K. REED	DRAFT	7/24/79
J. VIGILANTE JJ	CHK	9/13/79
J. STARR	ENG	9/13/79
D. BARKER	QC	9/13/79
	MGR	

ASSEMBLY, PRINTED CIRCUIT UNIVERSAL CLOCK

ECN 4008

35-757 R01 003

SHT 1 OF 1

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