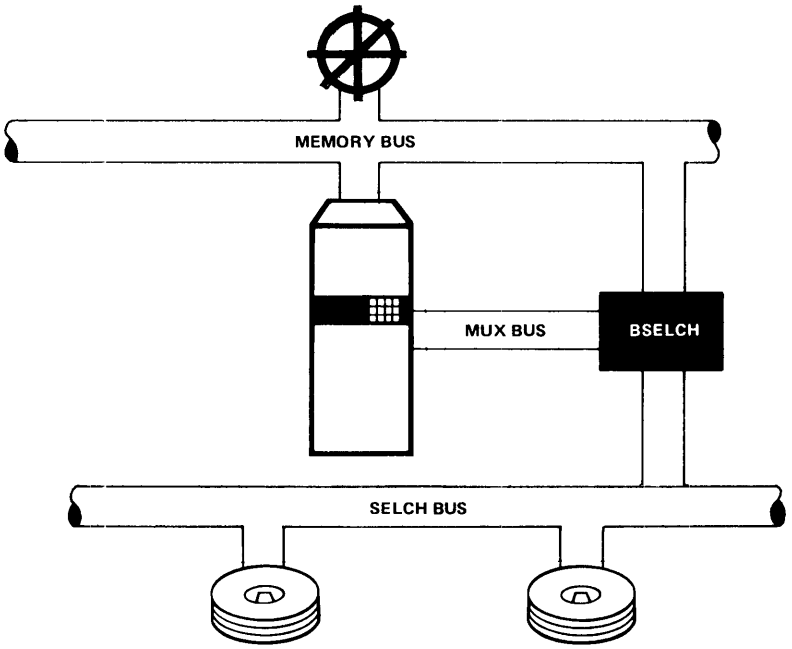
INTERDATA

SYSTEM MODULES



Buffered Selector Channel

PRODUCT DESCRIPTION

Interdata's Buffered Selector Channel (BSELCH) provides a completely independent,high-speed direct memory data transfer interface between an Interdata 8/32 processor memory and up to 16 device controllers.

The peak data transfer rate of the Buffered Selector Channel is an exceptionally fast 5.9 million bytes per second when transferring at the maximum burst size. The Buffered Selector Channel allows totally autonomous data transfer, without interfering with simultaneous multiplexer bus data transfers and other processing functions.

FEATURES

- 5,980,000 Bytes per Second Burst Transfer Rate
- Simultaneous Data Processing
- Halfword and Burst Mode
- Cycle Interleaving Direct Memory Access
- Direct Address Range of 1M bytes

OPERATIONAL CHARACTERISTICS

The Buffered Selector Channel transfers data by employing a cycle interleaving operation directly to the processor memory. Once initiated, the Buffered Selector Channel functions in a completely autonomous fashion with one controller or device actively transferring data at any one time.

Data transfer is initiated by loading a starting and ending address to specify the address range for the data transfer.

A GO command is then issued by the processor and the data transfer proceeds without further direction from, or interaction with, the processor. The GO command also inhibits activity with the processor and any other device on the Buffered Selector Channel private bus. All set-up commands for controller and channel operation are transferred via the multiplexer bus.

A 32-byte buffer allows the Buffered Selector Channel to transfer data to the device without regard to memory activity. The Buffered Selector Channel logic allows burst data transfers between the buffer and memory in a range from 2 halfwords to 14 halfwords, selected at system design time as a strap option.

Memory boundaries are transparent; the Buffered Selector Channel crosses contiguous bank boundaries under hardware-implemented logic control, eliminating software overhead.

Upon termination of a data block transfer the Buffered Selector Channel interrupts the processor to signal activity completion and returns the Buffered Selector Channel to an idle mode without further processor interrupt.

When idle, the Buffered Selector Channel private bus is connected to the multiplexer bus and functions as a bus buffer. Communication between the multiplexer and private bus devices takes place in the normal I/O bus manner using standard I/O programming conventions.

SPECIFICATIONS

Burst Data Transfer Rate (Buffered Selector Channel Memory)	Burst Size in halfwords	Read Rate(MB)	Write Rate(MB)
	2	2.58	4.17
	4	3.83	5.06
	6	4.56	5.45
	8	5.05	5.67
	10	5.39	5.81
	12	5.65	5.91
	14	5.85	5.98

Data Transfer Rate (Device-Buffered Selector Channel)	2,000,000 Bytes per second (maximum)
Maximum Number of Devices	16
Data Transfer Format (Device – Buffered Selector Channel)	Halfword (16 Bits) Byte (8 Bits)
Mode of Operation (strap selectable)	Burst Halfword (2 MB transfer rate limit)
Memory Access Method	Memory Cycle Interleaving
Addressing Capability	1 Million Bytes
Dimensions	15" x 15" (38.1 x 38.1 cm) Printed Circuit Board
Weight	3 pounds (1.4 kg)
Power Requirement	+5 VDC, 6 Amperes

INTERDATA PRODUCT NUMBER

M48-059 Buffered Selector Channel. Provides the 8/32 processor with direct memory access of up to 1,000,000 bytes of main memory. Includes burst/halfword mode selection, 16 halfword buffering and burst length select to 14 halfwords. Burst data transfer at rates up to 5.9 million bytes per second. Accommodates up to 16 device controllers.

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