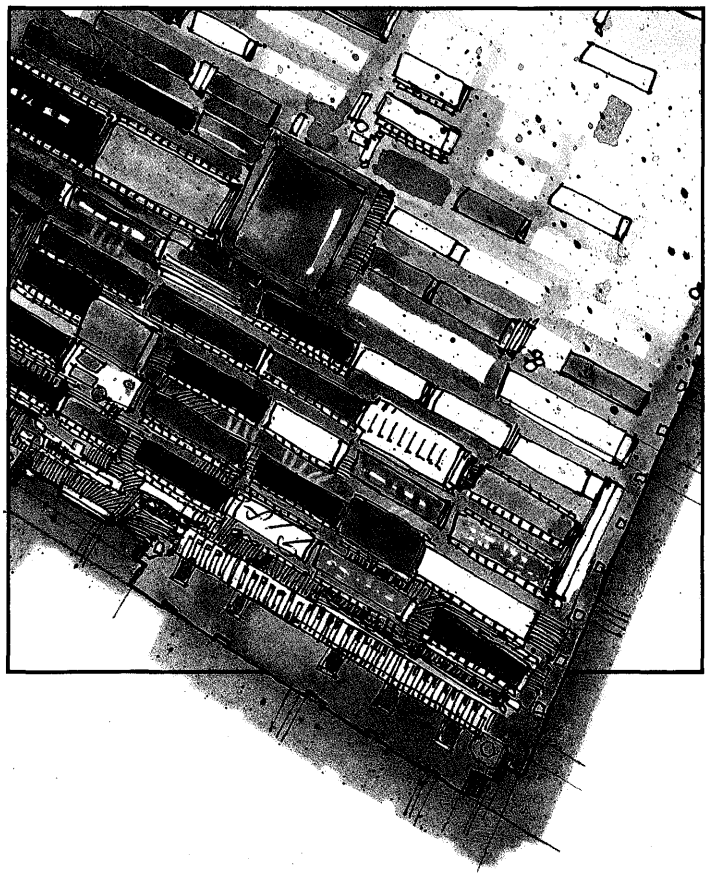
WNC 5190

High-performance Multibus® Network Controller

User's Guide



INTERPHASE® corporation

WNC 5190
High-performance Multibus® Network Controller
User's Guide

PRELIMINARY

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1.0 PREFACE

This Short Form User's Guide is intended to be a reference document for users who already have a general understanding of the function of Point-to-Point Full Duplex Communications Controllers, a general knowledge of Multibus system needs, and some exposure to peripheral devices themselves.

2.0 INTRODUCTION TO THE WNC 5190

The WIDE NETWORK CONTROLLER (WNC) 5190 is an intelligent 8X305-based serial communications controller for the Multibus (IEEE 796). It can support one high-speed (up to 2 Mbits/sec), full duplex data communications channel via a standard RS-449/422 interface. The WNC 5190 is ideally suited for high speed data communications between two local or remote CPU's. In another application, the WNC 5190 could serve as a bridge or gateway between two Local Area Networks.

The WNC 5190 has two separate 8K Byte buffers; one for buffering transmit data and the other for buffering receive data. These buffers permit large packet transfers and support variable packet sizes. The WNC 5190, operating as a bus master, controls all bus data transfers to/from system memory at 16 bits per transfer.

Simple high level commands (passed via an I/O Parameter Block built in system memory accessible by the WNC 5190) instruct the WNC 5190 to perform some function. Should an error occur while transmitting or receiving serial data, or while transferring packets across the Multibus, comprehensive error reporting is provided.

Two WNC 5190's may be connected directly via twisted-pair cable up to 200 ft. at the maximum data rate. For longer transmission distances, the INTERPHASE 5110 MAU can operate up to 4200 ft. using RG-59 coaxial cable and up to 32,000 ft. with appropriate cable. See Table 1 in Appendix D for further information about the 5110 MAU. Since the WNC 5190 excludes the Physical Layer, it can support a multitude of modems and media such as baseband coax (5110 MAU), cable tv, broadband coax, optical fiber, microwave, T1 carrier, Bell DDS (56 Kb), wide band service and others. See Appendix C for details on the serial interface.

3.0 HOW TO ISSUE A COMMAND

Using the WNC 5190 is easy due to the simple I/O Parameter Block structure and high level commands. The I/O Parameter Block (IOPB) is a list of parameters built in system memory accessible by the WNC 5190. This list contains parameters which are used to initialize the WNC 5190 and to define the exact function to be performed. In order to initiate data transmission, simply build the IOPB in memory, write a pointer to the IOPB into the WNC 5190 Address Registers, and a "GO" to the Command Register. The function is automatically completed by the WNC 5190. Both an "Operation Done" interrupt and "Done Status" are provided upon completion of the command. The IOPB is also updated by the WNC 5190 to indicate the status of completion and report any error conditions.

3.1 I/O REGISTERS

The WNC 5190 has four eight-bit Multibus write only registers and one six-bit read only register. Three of the write only registers (R1-R3) set up the address of the IOPB for a command, and the fourth one (R0) actually initiates command activity.

Figure 3.1-1 shows the format of the I/O registers. The registers are accessed using Multibus I/O reads and writes to I/O address space. The starting address is set by on board dip switches. The WNC 5190 uses 4 contiguous I/O addresses to access the registers. Either an 8 bit or 16 bit I/O addressing space can be selected by strap option. Sections 3.1.1 through 3.1.3 details the definitions of the bits and byte of the registers.

Command Register: (RO - Write Only)

7(MSB)	6	5	4	3	2	1	0(LSB)
GO	0	0	0	HRDWRE RESET	BRDEN	INTEN	CLEAR INTR

Status Register: (RO - Read Only - Same Address As Command Register)

7(MSB)	6	5	4	3	2	1	0(LSB)
0	0	BOARD FAIL	0	BUSY	BRDEN	INTEN	INTR

IOPB Address Registers: (R1 - Write Only - Command Register Address + 1)

7(MSB)	6	5	4	3	2	1	0(LSB)
IOPB ADDRESS						XMBYTE	

IOPB Address Registers: (R2 - Write Only - Command Register Address + 2)

7(MSB)	6	5	4	3	2	1	0(LSB)
IOPB ADDRESS						MSBYTE	

IOPB Address Registers: (R3 - Write Only - Command Register Address + 3)

7(MSB)	6	5	4	3	2	1	0(LSB)
IOPB ADDRESS						LSBYTE	

FIGURE 3.1-1 I/O REGISTERS

3.1.1 COMMAND REGISTER (RO -- WRITE ONLY)

BIT 0 - CLEAR INTERRUPT
Set this bit to a 1 to clear an interrupt. It is not necessary to turn off this bit. The source of the interrupt can be either the completion of the current command or a received data packet. The hardware interrupt on the Multibus is cleared instantaneously with the Multibus write to this bit. The "INTERRUPT PENDING BIT" in the status register is cleared within 100 nano seconds of setting this clear interrupt bit.

BIT 1 - INTERRUPT ENABLE
Set this bit to a 1 to enable Multibus interrupts. If this bit is set to 1, the WNC 5190 will generate interrupts on whatever level is selected by straps on the board --- 1 of 8 levels.

BIT 2 - BOARD ENABLE
Set this bit to a 1 to enable the WNC 5190. Before setting this bit the Address Registers should be initialized with the IOPB address (see section 3.1.3). Once enabled, the WNC 5190 will activate REQUEST TO SEND (RTS) at the communications interface and initiate transmission of SDLC FLAG CHARACTERS. FLAG transmission is used to fill idle time between packets. Once set, this bit should remain set, unless a hardware reset condition occurs.

BIT 3 - HARDWARE RESET
Set this bit to a 1, wait at least 15 microseconds, and then set it back to 0. This will cause the on board 8X305 and other devices to reset, and is the same as asserting the INIT/ line on the Multibus. The busy bit in the Status Register (see section 3.1.2) will go to a 1 while the board is in the reset condition and back to 0 when reset is removed.

BITS 4-6 - RESERVED
Always set these bits to 0.

BIT 7 - GO
Set this bit to a 1 after initializing Address Registers (R1-R3) and setting up the IOPB in order to issue a command to the WNC 5190. It is not necessary to turn off this bit.
The busy bit in the Status Register (see section 3.1.2) will go to a 1 50 nano seconds after GO is set to a 1.

3.1.2 STATUS REGISTER (R0 -- READ ONLY --- SAME ADDRESS AS COMMAND REGISTER)

BIT 0 - INTERRUPT PENDING
When set to 1, this bit indicates that the WNC 5190 has either completed the previous command or received a data packet and transferred it to system memory. To determine the source of the interrupt first examine IOPB byte 40 (Receive Interrupt Code). If set to 1 then a receive completion interrupt occured. If not set to 1 then examine IOPB byte 01H (SEND STATUS). If set to 1 or higher then the previous command has been completed or an error has occured. See section 3.2 for more detailed information on these IOPB bytes.

BIT 1 - INTERRUPTS ENABLED
When set to 1, this bit indicates that the WNC 5190 has Multibus interrupts enabled. That is, bit 1 in the Command Register has been set.

BIT 2 - BOARD ENABLED
When set to 1, this bit indicates that the WNC 5190 has been enabled. That is, bit 2 in the Command Register has been set.

BIT 3 - BUSY
When set to 1, this bit indicates that the WNC 5190 is busy working on a command. A 0 indicates the WNC 5190 is not busy. The WNC 5190 indicates busy during the reset function. The WNC 5190 also indicates busy during execution of the Power On Functional Integrity Test. When the test is completed, the WNC 5190 goes not busy indicating that Board Fail (Bit 5) is valid. There is a delay of 50 nano seconds from the setting of the "GO" bit in the command register to "BUSY" going high.

BIT 4 - UNUSED

BIT 5 - BOARD FAIL
This bit is only valid after a reset and before the WNC 5190's I/O Registers are initialized. Reset forces the 8X305 to execute its on board Functional Integrity Test. If all tests pass, this bit will be 0 when BUSY goes to 0. If a failure occurs, this bit will be 1 when BUSY goes to 0. If a failure was detected, a Self-Test Command should be issued to the WNC 5190 so it can report test results on a per test basis.

3.1.3 IOPB ADDRESS REGISTERS (R1-R3 -- WRITE ONLY)

R1 - XMBYTE
The most significant 8 bits of the 24 bit IOPB address.

R2 - MSBYTE
The middle 8 bits of the 24 bit IOPB address.

R3 - LSBYTE
The least significant 8 bits of the 24 bit IOPB address.

3.2 I/O PARAMETER BLOCK

The I/O Parameter Block (IOPB) tells the WNC 5190 exactly what to do. The IOPB consists of 56 contiguous bytes grouped into three sections: Send Control sub-Block (SCB), Initialization Control sub-Block (ICB), and Receive Control sub-Block (RCB). The IOPB should be built in memory space accessible by the WNC 5190 before issuing the GO bit. Since several bytes are updated by the controller, the IOPB must be located in RAM.

Rules:

The host CPU must not modify the Send Control Block between issuance of a 'GO' command to WNC 5190 Command Register and receipt of a command completion interrupt from WNC 5190. The WNC 5190 will modify the Send Control Block only during this period.

The host CPU must only modify the Receive Control Block during service of a receive interrupt from WNC 5190. The WNC 5190 will modify the Receive Control Block only when there is no pending interrupt to the host.

Figure 3.2-1 shows the IOPB format. A detailed description of each IOPB element follows.

IOPB Byte	
	Send Control (sub) Block:
00	Command code
01	Send Message Status/Error **
02	(RESERVED 00)
03	(RESERVED 00)
04	Send Header byte count (MSB)
05	Send Header byte count (LSB)
06	Send Data byte count (MSB)
07	Send Data byte count (LSB)
08-15	Send Message Tags 1-8 (8 bytes)
	Initialization Control (sub) Block:
16	Reserved (00)
17	Send header source address (XMB)
18	Send header source address (MSB)
19	Send header source address (LSB)
20	Reserved (00)
21	Send data source address (XMB)
22	Send data source address (MSB)
23	Send data source address (LSB)
24	Reserved (00)
25	Receive header destination address (XMB)
26	Receive header destination address (MSB)
27	Receive header destination address (LSB)
28	Reserved (00)
29	Receive data destination address (XMB)
30	Receive data destination address (MSB)
31	Receive data destination address (LSB)
32	DMA burst count (MSB) - in # of transfers
33	DMA burst count (LSB) - in # of transfers
34	Maximum packet size (MSB) - in bytes
35	Maximum packet size (LSB) - in bytes
36	Prom Version Number - ASCII **
37	Prom Revision Level - ASCII **
38	(RESERVED 00) **
39	(RESERVED 00) **
	Receive Control (sub) Block:
40	Interrupt code **
41	Receive Message Status/Error **
42	(RESERVED 00) **
43	(RESERVED 00) **
44	Receive Header byte count (MSB) **
45	Receive Header byte count (LSB) **
46	Receive Data byte count (MSB) **
47	Receive Data byte count (LSB) **
48-55	Receive Message Tags 1-8 **
56-71	Report Area for Self-Test Command (16 bytes) **

** THESE BYTES ARE UPDATED BY THE WNC 5190.

FIGURE 3.2-1 - IOPB FORMAT.

COMMAND CODE (Byte 0)
This byte identifies the nature of the operation to be performed. A list of command codes is found in Figure 3.2-2

SEND MESSAGE STATUS/ERROR (Byte 1)
This byte must be set to 0 when the Send Control Block (SCB) is being built. Upon completion of the current command, this byte is updated with completion status or an error code as shown in Figure 3.2-2

RESERVED (Byte 2)
This byte must be set to 0.

RESERVED (Byte 3)
This byte must be set to 0.

SEND HEADER BYTE COUNT - (Bytes 4 & 5)
These bytes specify how many header bytes are in a send packet. Header bytes and data bytes are essentially the same, however for maximum system flexibility, the two can be treated differently, and located at different areas in system memory. This count can be set to zero if header information is not needed.

SEND DATA BYTE COUNT - (Bytes 6 & 7)
These bytes specify how many data bytes are in a send packet. Header bytes and data bytes are essentially the same, however for maximum system flexibility, the two can be treated differently, and located at different areas in system memory. If header information is not needed, this count would contain the entire byte count of the send packet, and the SEND HEADER BYTE COUNT value would be set to zero.

SEND MESSAGE TAGS 1-8 (Bytes 8-15)
This 8 byte field is totally transparent to the WNC 5190 and is sent along with the packet to the receiving end. There it is transferred into bytes 48-55 of the Receive Control Block (RCB) for use as described by Host CPU software.

RESERVED (Byte 16)
This byte must be set to 0.

SEND HEADER SOURCE ADDRESS - (Bytes 17, 18, 19)
This three byte value points to the beginning of the send header area in system memory. Header information and data information are essentially the same, however for maximum system flexibility they can be separated into different areas of system memory. If the SEND HEADER BYTE COUNT is set to zero, these three bytes are don't cares. This address if used must fall on a even boundry (LSB even).

RESERVED (Byte 20)
This byte must be set to 0.

SEND DATA SOURCE ADDRESS - (Bytes 21, 22, 23)
This three byte value points to the beginning of the send data area in system memory. Header information and data information are essentially the same, however for maximum system flexibility they can be separated into different areas of system memory. This address if used must fall on a even boundry (LSB even).

RESERVED (Byte 24)
This byte must be set to 0.

RECEIVE HEADER DESTINATION ADDRESS - (Bytes 25, 26, 27)
This three byte value points to the beginning of where the receive header information will be put in system memory. Header information and data information are essentially the same, however for maximum system flexibility they can be separated into different areas of system memory. This address if used must fall on a even boundry (LSB even).

RESERVED (Byte 28)
This byte must be set to 0.

RECEIVE DATA DESTINATION ADDRESS - (Bytes 29, 30, 31)
This three byte value points to the beginning of where the receive data information will be put in system memory. Header information and data information are essentially the same, however for maximum system flexibility they can be separated into different areas of system memory. This address must fall on a even boundry (LSB even).

DMA BURST COUNT - (Bytes 32 & 33)
These bytes specify the maximum number of bus transactions (words) to allow in one burst (bus acquisition) across the multibus. The minimum count allowed is one and the maximum count allowed is 4088.

MAXIMUM PACKET SIZE - (Bytes 34 & 35)
These bytes set the maximum possible packet size that the WNC 5190 is expecting to receive. This aids the WNC 5190 in determining if a receive buffer overflow has occured. The Maximum Packet Size is defined as being equal to or more than the largest possible packet (in bytes) that either WNC 5190 can send. This number cannot exceed 8192 - 16 = 8176 (1FF0H) bytes due to buffer limitations. Both sides of the communications link must set this size to the same value.

PROM VERSION NUMBER AND REVISION LEVEL (Bytes 36 & 37)
These bytes indicate the firmware version number and revision level in ASCII. The bytes are written by the WNC 5190 to the Initialization Control Block (ICB) by the WNC 5190 during execution of the INIT command.

RESERVED (Bytes 38 & 39)
These bytes are written to at initialization time. The value in these bytes is arbitrary and may change in future revisions.

INTERRUPT CODE (Byte 40)
This byte is set to 1 by the WNC 5190 to indicate to the interrupt handler that a packet has been received. The interrupt handler should

set this byte to 0 before clearing the interrupt.

RECEIVE MESSAGE STATUS/ERROR (Byte 41)
This byte is set to 1 by the WNC 5190 to indicate an error free packet reception. Any nonzero number other than 1 is an error code (see Figure 3.2-2 for error code information). The interrupt handler should set this byte to 0 before clearing the interrupt.

RESERVED (Bytes 42 & 43) These bytes are reserved for future use. Presently the WNC 5190 writes zeroes to these bytes. The use of these bytes may change in future revisions.

RECEIVE HEADER BYTE COUNT - (Bytes 44 & 45)
These bytes are written to by the WNC 5190 when a packet has been received. These values are equal to the other WNC 5190's SEND HEADER BYTE COUNT.

RECEIVE DATA BYTE COUNT - (Bytes 46 & 47)
These bytes are written to by the WNC 5190 when a packet has been received. These values are equal to the other WNC 5190's SEND DATA BYTE COUNT.

RECEIVE MESSAGE TAGS 1-8 (Bytes 48-55)
This 8 byte field is totally transparent to the WNC 5190 and is received along with the packet from the transmitting end. It is then transferred into bytes 48-55 of the Receive Control Block (RCB) for use as described by Host CPU software.

REPORT AREA FOR SELF TEST COMMAND (Bytes 56-71)
This 16 byte field is used by the WNC 5190 for reporting results of the SELF TEST COMMAND. Currently 14 separate tests are supported. The SELF TEST COMMAND is described in detail in section 8.0.

Figure 3.2-2 below contains a list of command codes, interrupt codes, and status/error codes. More detailed information on these subjects is given in the following sections.

Command Codes:

00	No Operation	(Interrrupt immediately)
01	Send Data	Fetch data from system memory and transmit it.
02	Init	Report ASCII Prom Version and Rev Level. (4 bytes) at end of ICB in system memory.
03	Self-Test	16-byte report goes to end of Receive Control Block, bytes 56 - 71 of the IOPB.

Receive Control Block - Interrupt Codes:

00	
01	Receive Complete

Receive Control Block - Message Status/Error Codes:

00	
01	Received without error
02	Receiver Overrun
03	Framing Error
04	Abort
05	CRC error
06	Receive Buffer Overrun
07	Local multibus write transfer bus timeout
08	RCB invalid

Send Control Block - Message Status/Error Codes:

00	
01	Command completed without error
02	WNC 5190 not initialized
03	Transmitter Underrun
07	Local multibus read transfer bus timeout
08	SCB invalid

FIGURE 3.2-2 COMMAND/STATUS CODES

3.3 USE OF THE STATUS/ERROR BYTES

The Send Status/Error byte of the IOPB is normally initialized to 0 before the transaction is started. When the GO bit is set in R0 (WNC 5190 Command Register), the BUSY bit in the Status Register is set (less than 50 nano seconds of GO being set) and the WNC 5190 automatically fetches the 16 byte Send Control Block (SCB) starting at the address pointed to in R1,R2 and R3 as described earlier. The WNC 5190 then does all the work necessary to complete the transaction. If the transaction has been successfully completed the Send Status/Error byte is then set to 1 and an interrupt is generated (if enabled) assuming there is no current interrupt pending. If an error was detected an Error Code is written to the Send Status/Error byte (see Figure 3.2-2) and a interrupt is generated, if enabled, assuming there is no current interrupt pending.

The Receive Status/Error byte of the IOPB is normally initialized to 0 by the CPU during servicing of a receive interrupt and prior to clearing the interrupt. Before a receive interrupt is generated by the WNC 5190, the Interrupt Code of the RCB is set to 1. If the data packet has been received without error and successfully transferred to system memory, then the Receive Status/Error byte is set to 1 and an interrupt is generated (if enabled) assuming there is no current interrupt pending. If an error was detected an Error Code is written to the Receive Status/Error byte (see Figure 3.2-2) and a interrupt is generated, if enabled, assuming there is no current interrupt pending.

In any of the above cases, if an interrupt is already pending then the WNC 5190 will wait for the current interrupt to be cleared (acknowledged) before posting the new interrupt.

4.0 COMMANDS

The WNC 5190 automatically completes "MACRO" level commands after they are initiated with a "GO" bit. The first byte of the IOPB specifies such things as 'Initialize' and 'Send Data'. The WNC 5190 does the DMA and interrupts the CPU when done. A list of the supported commands is shown in Figure 3.2-2.

4.1 NO OPERATION (00H)

This command can be used to verify the integrity of the WNC 5190's Multibus interface. The WNC 5190 will set BUSY to 1; fetch the SCB; decode the 'NO OP' command; write a 1 to the Send Message Status/Error byte; set Busy to 0; and generate an interrupt, if enabled.

4.2 SEND DATA (01H)

The WNC 5190 will set BUSY to 1; fetch the SCB; decode the 'SEND DATA' command; fetch the Send Header Block if the Send Header Byte Count is nonzero; fetch the Send Data Block if the Send Data Byte Count is nonzero; verify that the maximum packet size (specified in the ICB) has not been exceeded; transmit the SCB, Header Block, and Data Block; write a 1 to the Send Message Status/Error byte; set Busy to 0; and generate an interrupt, if enabled.

Note that a 'Zero Length' packet can be transmitted by specifying 0 for Send Header and Send Data Byte Counts. Only the 16 byte SCB will be transmitted and DMA'ed into the RCB on the receiving end allowing Message Tags to be sent and received independent of data availability.

The WNC 5190 will reject all 'SEND DATA' commands if it has not first been initialized by an 'INITIALIZE' command.

4.3 INITIALIZE (02H)

The WNC 5190 must be initialized by the CPU before it can transmit and receive data packets. The WNC 5190 will set BUSY to 1; fetch the SCB; decode the 'INITIALIZE' command; fetch the ICB (IOPB bytes 16-35); write the Prom Version Number and Revision Level into the ICB; check the ICB for valid DMA Burst Count and Maximum Packet Size; enable the receiver; write a 1 to the Send Message Status/Error byte; set Busy to 0; and generate an interrupt, if enabled.

4.4 SELF TEST (03H)

The WNC 5190 will set BUSY to 1; fetch the SCB; decode the 'SELF TEST' command; execute 14 independent tests to verify functional integrity of the hardware; report completion status of each test in the area reserved at the end of the RCB; write a 1 to the Send Message Status/Error byte; set BUSY to 0; and generate an interrupt, if enabled. After the WNC 5190 executes the 'SELF TEST' command it must be initialized prior to sending and receiving packets. Note that the WNC 5190 does NOT have to be initialized in order to execute a 'SELF TEST' command. It only needs to be enabled via R0 assuming R1-R3 contain a valid pointer to the IOPB. Note that any data being received from another WNC 5190 while the self data is running will be ignored.

5.0 HOW TO INITIALIZE THE WNC 5190

To initialize the WNC 5190 it is necessary to first build the Initialization Control Block (ICB) in system memory. The ICB contents are used by the WNC 5190 only during execution of the 'INIT' command. Next, the Command Code byte in the SCB must be set to 02H and the Send Message Status/Error byte to 00H. The remaining parameters in the SCB have no meaning for this command and are don't cares.

The WNC 5190 will fetch all 16 bytes of the SCB, one byte at a time (the IOPB is always read in 8 bits at a time), decode the 'INIT'command, fetch all 20 bytes of the ICB, one byte at a time, and then update the Prom Version and Revision level bytes in the ICB. These 20 bytes are stored in on-board RAM and contain 6 parameters for initialization. These 6 parameters are defined below:

5.1 INITIALIZATION CONTROL BLOCK DESCRIPTIONS

1. Send Header Source Address - Indicates to the WNC 5190 the 24 bit address in system memory where the Send Header Block resides. When a 'Send Data' command is issued, the WNC 5190 will fetch the Send Header Block from this address if the Send Header Byte Count in the SCB is non-zero. This address must be even since transfers are word wide.

2. Send Data Source Address - Indicates to the WNC 5190 the 24 bit address in system memory where the Send Data Block resides. When a 'Send Data' command is issued, the WNC 5190 will fetch the Send Data Block from this address if the Send Data Byte Count in the SCB is non-zero. This address must be even since transfers are word wide.

3. Receive Header Destination Address - Indicates to the WNC 5190 the 24 bit address in system memory where the Receive Header Block should be DMA'ed to. When a data packet is received, the WNC 5190 will transfer the Receive Header Block to this address if the Receive Header Byte Count in the received SCB is non-zero. This address must be even since transfers are word wide.

4. Receive Data Destination Address - Indicates to the WNC 5190 the 24 bit address in system memory where the Receive Data Block should be DMA'ed to. When a data packet is received, the WNC 5190 will transfer the Receive Data Block to this address if the Receive Data Byte Count in the received SCB is non-zero. This address must be even since transfers are word wide.

5. DMA Burst Count - Must be non-zero and indicates to the WNC 5190 the number of word-wide transfers to make during each burst (bus acquisition). This number cannot exceed 4088 (0FF8).

6. Maximum Packet Size - Indicates to the WNC 5190 the maximum number of bytes a packet will ever have. This number should be set to be equal to or larger than the largest possible packet (in bytes) that either WNC 5190 can send. This number cannot exceed 8K - 16 = 8176 (1FFOH). Both WNC 5190s must specify the same size.

Once the ICB is built, the SCB and RCB should be filled with zeroes. Next, the command code (02H) for 'INIT' has to be written to the Command Code byte in the SCB. Finally, assuming the board is enabled (Bit 2 set to 1 in RO), output an 86H to RO for interrupt driven systems or an 84H for a polled environment. This action will force BUSY active (set to 1 in Status Register) and cause the WNC 5190 to fetch the SCB, decode the command type, fetch the ICB and initialize itself for data communications. After completing the transaction, the WNC 5190 will set the Send Message Status/Error byte in the SCB, set the BUSY bit to 0, and post an interrupt, if enabled. The Status should be a 1 for successful completion. Any other non-zero value will indicate an error condition. Error codes are shown in Figure 3.2-2.

If the system is interrupt driven, the interrupt handler must first determine that the interrupt was caused by transaction completion by checking for a non-zero value in the Send Message Status/Error byte of the SCB. Before exiting from the interrupt handler, the Send Message Status/Error byte should be set to 0 and the WNC 5190 interrupt signal cleared. To clear the interrupt signal output a 07H code to RO.

If the WNC 5190 is operating in a polled environment, the CPU should poll the INTERRUPT bit (Bit 0 = 1) in the Status Register and the Send Message Status/Error byte to determine when transaction completion occurs. The reason for not polling the BUSY bit (Bit 3 = 1) is that a "packet received" condition will not affect BUSY but will instead activate INTERRUPT. The CPU must first determine that the set INTERRUPT bit was caused by transaction completion by checking for a non-zero value in the Send Message Status/Error byte of the SCB. If it is transaction completion, the Send Message Status/Error byte should be set to 0 and the WNC 5190 interrupt bit cleared. To clear the interrupt bit output a 05H code to RO.

If the interrupt is caused by a receive condition, the Interrupt Code byte of the RCB will contain a 1 and the Receive Message Status/Error byte should be non-zero. These two bytes should be set to 0 prior to clearing the interrupt signal.

6.0 HOW TO SEND DATA

Prior to issuing the 'Send Data' command the Send Header Block (if any) and the Send Data Block (if any) must be built. The Command Code byte in the SCB must be set to 01H and the Send Message Status/Error byte to 00H. The next parameters to be set up are the 16 bit Send Header Byte Count (if any) and the 16 bit Send Data Byte Count (if any). Note that either or both may be zero, however, if both byte counts are nonzero, then the WNC 5190 will implement data gathering to build a packet using data from two different locations in system memory. Finally, the Message Tags (if any) should be written to the last 8 bytes of the SCB. Message Tags are transparent to the WNC 5190 meaning that they are obtained from the Sender's SCB, transmitted at the front of the packet, and DMA'ed directly into the Receiver's RCB. Their meaning and use is left up to the CPU software.

When the GO bit is set by the CPU, the BUSY bit will be set to 1, and the WNC 5190 will transfer all 16 bytes of the SCB from system memory to the Transmit Buffer. After decoding the 'SEND DATA' command, the WNC 5190 will check to verify that the sum of the Send Header Byte Count and the Send Data Byte Count does not exceed the value specified by the Maximum Packet Size in the ICB. If it does, an 'SCB INVALID' error (08H) is posted in the Send Message Status/Error byte of the SCB. The CPU is then interrupted if interrupts are enabled.

If the sum of the Send Header/Data Byte Counts is valid, the WNC 5190 checks for a nonzero Send Header Byte Count.

If the Send Header Byte Count is nonzero, the Send Header Block is transferred from system memory to the WNC 5190's Transmit Buffer, where it is located just behind and contiguous with the SCB. All data transfers (Header Block and Data Block) are accomplished 16 bits at a time. These transfers occur in bursts, and the number of transfers per burst is specified by the DMA Burst Count in the ICB.

If the Send Header Byte Count is zero, no bus transfers are made. The Send Data Byte Count is then checked.

If the Send Data Byte Count is nonzero, the Send Data Block is transferred from system memory to the WNC 5190's Transmit Buffer, where it is located just behind and contiguous with the Send Header Block (if any).

If the Send Data Byte Count is zero, no bus transfers are made. The WNC 5190 now begins transmitting the packet.
Each packet consists of a 16 byte link-level header (SCB) and one of the following:

A) Both the Send Header Block and the Send Data Block

B) Only the Send Header Block

C) Only the Send Data Block

D) Neither the Send Header Block nor the Send Data Block

After completing the transaction, the WNC 5190 will update the Send Message Status/Error in the SCB, set the BUSY bit to 0, and post an interrupt, if enabled. The Status should be a 1 for successful completion. Any other nonzero value will indicate an error condition. Error codes are shown in Figure 3.2-2.

As each character is transmitted, the 16 bit Frame Check Sequence (FCS) is generated. The FCS is the CRC-CCITT polynomial (x**16 + x**12 + x**5 + 1) preset to 1s. The FCS is appended to the end of the packet and used by the receiver for error detection.

It is important to understand that acknowledgement protocol and retries for successful packet transmission/reception are not performed by the controller. Therefore, higher level software is responsible for the acknowledgement protocol necessary in verifying successful packet transfer. A scheme involving packet (frame) sequence numbering similar to that used by SDLC could be implemented. This would allow multiple packets to be outstanding before an acknowledgement is required by the sending side. Although somewhat complex, this scheme maximizes data throughput.

A simpler scheme to implement, would require the receiving side to acknowledge receipt of a packet on a per packet basis. The obvious tradeoff, however, would be a significant reduction in data throughput.

Back-to-back packet transfers could potentially cause RECEIVE BUFFER OVERRUN errors (06H) or even lost packets at the receiver when the time between the first packet's transaction completion interrupt and the next packet's GO bit at the transmitter is very short. The simple scheme of acknowledging receipt of a packet on a per packet basis alleviates these potential problems.

One situation which might possibly cause a lost packet would involve the transmission of a very long packet followed by a very short one. With very little time between packets, the receiver might not have enough time to complete the DMA transfer of the first packet to system memory. Until the DMA completes, no more serial data can be received. If the sender initiates transmission of the second packet too soon, it will be lost with no error reported at either end.

To solve this potential problem, a built in delay between successive 'SEND DATA' commands might be warranted by system software. Many system parameters can have an effect on the amount of delay required including DMA Burst Count, access time of system memory, density of bidirectional traffic on the communications link, WNC 5190 priority level on the Multibus, and packet size.

It is recommended to start with no delay. Bring up the communications link and log statistics on each receiver and each transmitter. If an abnormally high number of lost packets or receive buffer overruns are occurring, a gradual increase in delay should minimize and eventually eliminate these problems.

7.0 HOW TO RECEIVE DATA

The WNC 5190 can only receive data after it is initialized by an 'INIT' command. The WNC 5190 is capable of receiving serial data at any time as long as its 8K byte receive buffer is empty. To receive a valid packet (shown below) it must be framed by SDLC flag characters and contain correct CRC.

BEGINNING. FLAG (7E)	5190 HEADER (SCB)	HEADER BLOCK	DATA BLOCK	CRC	ENDING FLAG (7E)

When the serial data transfer is completed, the receiver status is checked for errors. Any error condition, i.e. CRC or framing, will cause the WNC 5190 to post an error code for the specific error in the RCB (see Figure 3.2-2) and generate an interrupt if enabled; data transfers are suppressed. Definitions of the error codes appear in Appendix B. The WNC 5190 header (SCB) is checked to verify that the received Total Byte Count (Receive Header Byte Count + Receive Data Byte Count) does not exceed the Maximum Packet Size specified in the ICB. If it does, an 'INVALID RCB' error code is posted in the RCB and an interrupt is generated, if enabled.

Otherwise, the Receive Header Block (if any) is DMA'ed into system memory starting at the Receive Header Destination Address specified in the ICB. Data transfers, 16 bits wide, occur in bursts. The number of transfers per burst is specified by the DMA Burst Count in the ICB. While the receive buffer is being emptied, the receiver is disabled to prevent the current packet from being corrupted.

After completing the Receive Header Block DMA, the Receive Data Block (if any) is transferred to system memory starting at the Receive Data Destination Address specified in the ICB. Finally, if no Multibus interrupt is pending, the WNC 5190 will transfer the received SCB into the RCB in system memory and generate an interrupt. After generating the interrupt the WNC 5190 prepares itself to receive another packet. BUSY is not affected by receive operations.

The interrupt service routine, after determining that the interrupt was caused by a receive condition, should clear the Interrupt Code byte and the Receive Message Status/Error byte in the RCB prior to clearing the interrupt.

Note that a data scattering scheme can be implemented by using both sets of pointers, allowing Header information to be directed to one area in system memory and Data information to another.

8.0 POWER-ON INTEGRITY TEST AND SELF-TEST COMMAND DESCRIPTION.

After power-on, or activation of the Multibus INIT signal, or software reset via the WNC 5190's Multibus Command Register, an on-board Functional Integrity Test (F.I.T.) will be executed. This F.I.T. consists of the following fourteen tests:

1. I/O TEST.
   Tests the I/O path for a left bank output port and input port.

2. INTERNAL DATA BUS TEST.
   Tests the integrity of the 8X305's IV-bus and also the data bus common to the serial communications chip, receive buffer, transmit buffer, and 8253 timer.

3. 8K x 8 RECEIVE BUFFER.
   Tests the receive buffer and the address lines to the buffer. It also tests the address register PALs.

4. 8K x 8 TRANSMIT BUFFER.
   Tests the transmit buffer. It does not check the address lines to the memory, or the address register PALs. These tests are performed in test number 5.

5. TRANSMIT BUFFER ADDRESS LINES.
   Tests the address lines of the transmit buffer memory. Also tested are the address register PALs.

6. 8K x 1 RECEIVE STOP BIT RAM.
   Tests the receive stop bit ram.

7. 8K x 1 TRANSMIT STOP BIT RAM.
   Tests the transmit stop bit ram.

8. 256 x 8 SCRATCH PAD RAM.
   Tests the scratch pad ram.

9. SERIAL COMMUNICATIONS CHIP.
   Tests the MPCC (2652) chip in an internal loopback mode. To run this test, Rx and Tx clocks must be supplied to the MPCC, originating either onboard or offboard. See section 9.1 to determine how to select onboard or offboard clocking.

10. TIMER 0 AND TIMER 1.
    Tests timers 0 and 1 located in the 8253 timer chip. Both are tested at once because timer 0 is a prescaler to timer 1.

11. TIMER 2.
    Tests timer 2 located in the 8253 timer chip.

12. TIMER 3.
    Tests timer 3 located in the 96S02 one-shot to ensure it times out within the range of 1 msec - 2 msec.

13. INTERRUPT CIRCUITRY.
    Tests the interrupt PAL and return circuitry by looping a small frame of data from the transmit buffer through the MPCC and into the receive buffer under interrupt control.

14. DEAD MAN TIMER.
    Tests the dead-man timer (555 chip) to ensure it times out within the range of 34 msec - 70 msec.

15. TEST NOT DEFINED

16. TEST NOT DEFINED

After a board reset condition each test will be executed until an error occurs or until all tests have been successfully completed. The worst case execution time is less than 1 second. If after 1 second the WNC 5190 Multibus Status Register indicates that the WNC 5190 is still busy (BUSY=1), then the WNC 5190 has incurred a hard failure. If however, the WNC 5190 is not busy (BUSY=0), the board failure flag should be checked. If any test has failed, then the board failure flag will be set (BOARD FAIL=1) and the BOARD FAIL LED (#4) will be on. Note that the BOARD FAILURE FLAG and LED are only valid after BOARD RESET and before BOARD ENABLE.

Next, the Send Control Block (SCB) beginning address should be written into the WNC 5190's Multibus I/O Registers and the board then enabled. Now the 5190 should be directed to execute a Self-Test Command to determine which test(s) failed. Every test will be executed independent of the other tests with a status byte response for each one. Assuming the Multibus interface is healthy, the WNC 5190 will respond with 16 bytes appended to the end of the Receive Control Block (RCB). The following codes are used for reporting valid test status:

00 ----- TEST NOT DEFINED

01 ----- TEST COMPLETED WITHOUT ERROR

02 ----- TEST COMPLETED WITH ERROR

The Self-Test Command can be issued to the WNC 5190 regardless of whether the board has been initialized with an Initialize Command or not. However, for proper board operation (Transmitting and Receiving Data) after execution of the Self-Test Command, an Initialize Command must be issued.

9.0 OPTION STRAPS, SWITCHES, DISPLAYS

9.1 WNC 5190 OPTION STRAPS.

There are numerous option straps on the WNC 5190 to select various modes of operation, 8 or 16 bit I/O addressing, interrupt level, etc. Figure 9.1-1 on the following page lists each set of straps, 3-post and 2-post. The selection as shipped from the factory is indicated by (*). Those connections that are factory set and should not be changed without consulting the factory are indicated by (**).

Also provided is a physical layout diagram (Figure 9.1-2) showing the location of the option straps.

3-POST OPTIONS:

1 ---- 2 ---- 3

STRAP DESIG.	STRAP SELECTION		DESCRIPTION
CA	1 -- 2		PASS BPRN TO 5190 FROM HIGHER PRIORITY MASTER
CA	2 -- 3	*	WNC 5190 IS HIGHEST PRIORITY
CE	1 -- 2		8-BIT I/O ADDRESSING
CE	2 -- 3	*	16-BIT I/O ADDRESSING
CAU	1 -- 2	**	ENABLE DEADMAN TIMER (45 MSEC)
CAU	2 -- 3		DISABLE DEADMAN TIMER
CAW	1 -- 2	*	TX CLOCK RATE OF 2 MHz - CBA off
CAW	2 -- 3		TX CLOCK RATE OF 1 MHz - CBA off
CBB	1 -- 2		SETTING FOR OTHER VENDOR'S MAU
CBB	2 -- 3	*	SETTING WHEN CONNECTED TO 5110 MAU

2-POST OPTIONS:

1 ---- 2

CB0	ON		M-BUS INTERRUPT LEVEL 0
CB1	ON		M-BUS INTERRUPT LEVEL 1
CB2	ON		M-BUS INTERRUPT LEVEL 2
CB3	ON		M-BUS INTERRUPT LEVEL 3
CB4	ON		M-BUS INTERRUPT LEVEL 4
CB5	ON		M-BUS INTERRUPT LEVEL 5
CB6	ON	*	M-BUS INTERRUPT LEVEL 6
CB7	ON		M-BUS INTERRUPT LEVEL 7
CF	ON	*	SERIAL BUS PRIORITY
CF	OFF		PARALLEL BUS PRIORITY
CAS	ON	*	HONOR BPRN
CAS	OFF		OVERRIDE BPRN
CAT	ON	*	IGNORE COMMON BUS REQUEST
CAT	OFF		ENABLE COMMON BUS REQUEST
CBA	ON	*	TX CLOCK SUPPLIED EXTERNALLY
CBA	OFF		TX CLOCK SUPPLIED BY WNC 5190

NOTE: * INDICATES THE SELECTION AS SHIPPED FROM THE FACTORY. ** INDICATES A FACTORY SETTING AND SHOULD NOT BE CHANGED WITHOUT CONSULTING THE FACTORY.

FIGURE 9.1-1

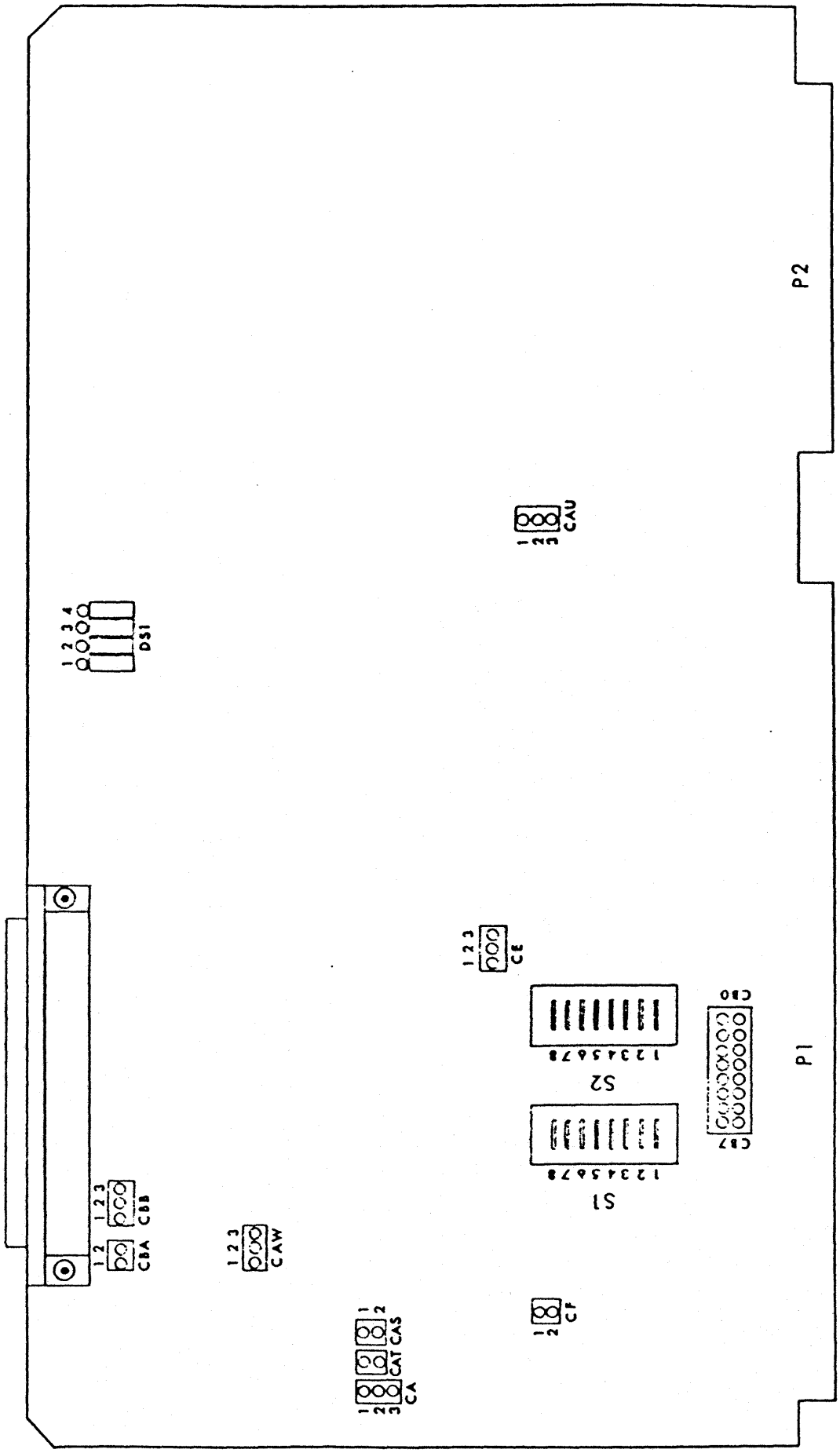

FIGURE 9.1-2 - PHYSICAL LAYOUT DIAGRAM

9.2 I/O ADDRESS SWITCH SETTING

The WNC 5190 has two 8 pole dip switches labeled "S1" and "S2" that are used to select the I/O address for the controller. Switch S2 is used to select the low byte of a 16 bit address and S1 is used to select the high byte. S1 is not used when operating in 8 bit I/O address mode. Refer to option strap 'CE' for selecting 8 or 16 bit modes, and Figure 9.1-2 for switch locations.

	S1	S2
	8 7 6 5 4 3 2 1	8 7 6 5 4 3 2 1
ON, 0	. . . . .	. . . . .
OFF, 1		*
ADDRESS	F E D C B A 9 8	7 6 5 4 3 2 X X

NOTE: X -- RESERVED

* -- MUST BE OFF WHEN USING AN INTERPHASE 5110 MAU
-- MUST BE ON WHEN USING ANOTHER VENDOR'S MAU

9.3 DIAGNOSTIC DISPLAYS

The WNC 5190 provides several LED based displays that are useful to help diagnose problems and observe normal operation. Refer to Figure 9.1-2 for the location of the LEDs. The 4 LED group is labeled DS1 and the individual LEDs are numbered 1 - 4.

DS1 - LED 1. MULTIBUS INTERRUPT PENDING
This LED is ON when the WNC 5190 is generating a Multibus interrupt with interrupts enabled.

DS1 - LED 2. REQUEST TO SEND
This LED is ON when the WNC 5190 is transmitting. Note that the WNC 5190, once enabled, is always transmitting SDLC FLAG characters during idle times when data transmission is not in progress. Because this controller operates in full duplex, Request to Send is always active.

DS1 - LED 3. BOARD ENABLE
This LED is ON when the WNC 5190 has been enabled by the CPU.

DS1 - LED 4. BOARD FAIL
This LED is ON when the WNC 5190 has failed one of the Power-On Functional Integrity Tests (FIT) after a reset condition. The LED is forced ON during reset and normally goes OFF after successful completion of the FIT.

APPENDIX A
FIGURES

********** APPENDIX A --- FIGURES **********

Command Register: (RO - Write Only)

7(MSB)	6	5	4	3	2	1	0(LSB)
GO	0	0	0	HRDWRE RESET	BRDEN	INTEN	CLEAR INTR

Status Register: (RO - Read Only - Same Address As Command Register)

7(MSB)	6	5	4	3	2	1	0(LSB)
0	0	BOARD FAIL	0	BUSY	BRDEN	INTEN	INTR

IOPB Address Registers: (R1 - Write Only - Command Register Address + 1)

7(MSB)	6	5	4	3	2	1	0(LSB)
IOPB		ADDRESS				XMBYTE	

IOPB Address Registers: (R2 - Write Only - Command Register Address + 2)

7(MSB)	6	5	4	3	2	1	0(LSB)
IOPB		ADDRESS				MSBYTE	

IOPB Address Registers: (R3 - Write Only - Command Register Address + 3)

7(MSB)	6	5	4	3	2	1	0(LSB)
IOPB		ADDRESS				LSBYTE	

FIGURE A-1. I/O REGISTERS

I/O PARAMETER BLOCK: (56 contiguous bytes)

IOPB Byte	
	Send Control (sub) Block:
00	Command code
01	Send Message Status/Error **
02	(RESERVED 00)
03	(RESERVED 00)
04	Send Header byte count (MSB)
05	Send Header byte count (LSB)
06	Send Data byte count (MSB)
07	Send Data byte count (LSB)
08-15	Send Message Tags 1-8 (8 bytes aligned on long-word boundary)
	Initialization Control (sub) Block:
16	Reserved (00)
17	Send header source address (XMB)
18	Send header source address (MSB)
19	Send header source address (LSB)
20	Reserved (00)
21	Send data source address (XMB)
22	Send data source address (MSB)
23	Send data source address (LSB)
24	Reserved (00)
25	Receive header destination address (XMB)
26	Receive header destination address (MSB)
27	Receive header destination address (LSB)
28	Reserved (00)
29	Receive data destination address (XMB)
30	Receive data destination address (MSB)
31	Receive data destination address (LSB)
32	DMA burst count (MSB) - in # of transfers
33	DMA burst count (LSB) - in # of transfers
34	Maximum packet size (MSB) - in bytes
35	Maximum packet size (LSB) - in bytes
36	Prom Version # - ASCII **
37	Prom Revision Level - ASCII **
38	(RESERVED 00) **
39	(RESERVED 00) **
	Receive Control (sub) Block:
40	Interrupt code **
41	Receive Message Status/Error **
42	(RESERVED 00) **
43	(RESERVED 00) **
44	Receive Header byte count (MSB) **
45	Receive Header byte count (LSB) **
46	Receive Data byte count (MSB) **
47	Receive Data byte count (LSB) **
48-55	Receive Message Tags 1-8 **
56-71	Report Area for Self-Test Command (16 bytes) **
**	THESE BYTES ARE UPDATED BY THE WNC 5190.

FIGURE A-2. IOPB FORMAT.

Command Codes:

00	No Operation	(Interrrupt immediately)
01	Send Data	Fetch data from system memory and transmit it.
02	Init	Report ASCII Prom Version and Rev Level. (4 bytes) at end of ICB in system memory.
03	Self-Test	16-byte report goes to end of Receive Control Block.

Receive Control Block - Interrupt Codes:

00	
01	Receive Complete

Receive Control Block - Message Status/Error Codes:

00	
01	Received without error
02	Receiver Overrun
03	Framing Error
04	Abort
05	CRC error
06	Receive Buffer Overrun
07	Local multi-bus write transfer bus timeout
08	RCB invalid

Send Control Block - Message Status/Error Codes:

00	
01	Command completed without error
02	WNC 5190 not initialized
03	Transmitter Underrun
07	Local multi-bus read transfer bus timeout
08	SCB invalid

FIGURE A-3. COMMAND/STATUS CODES

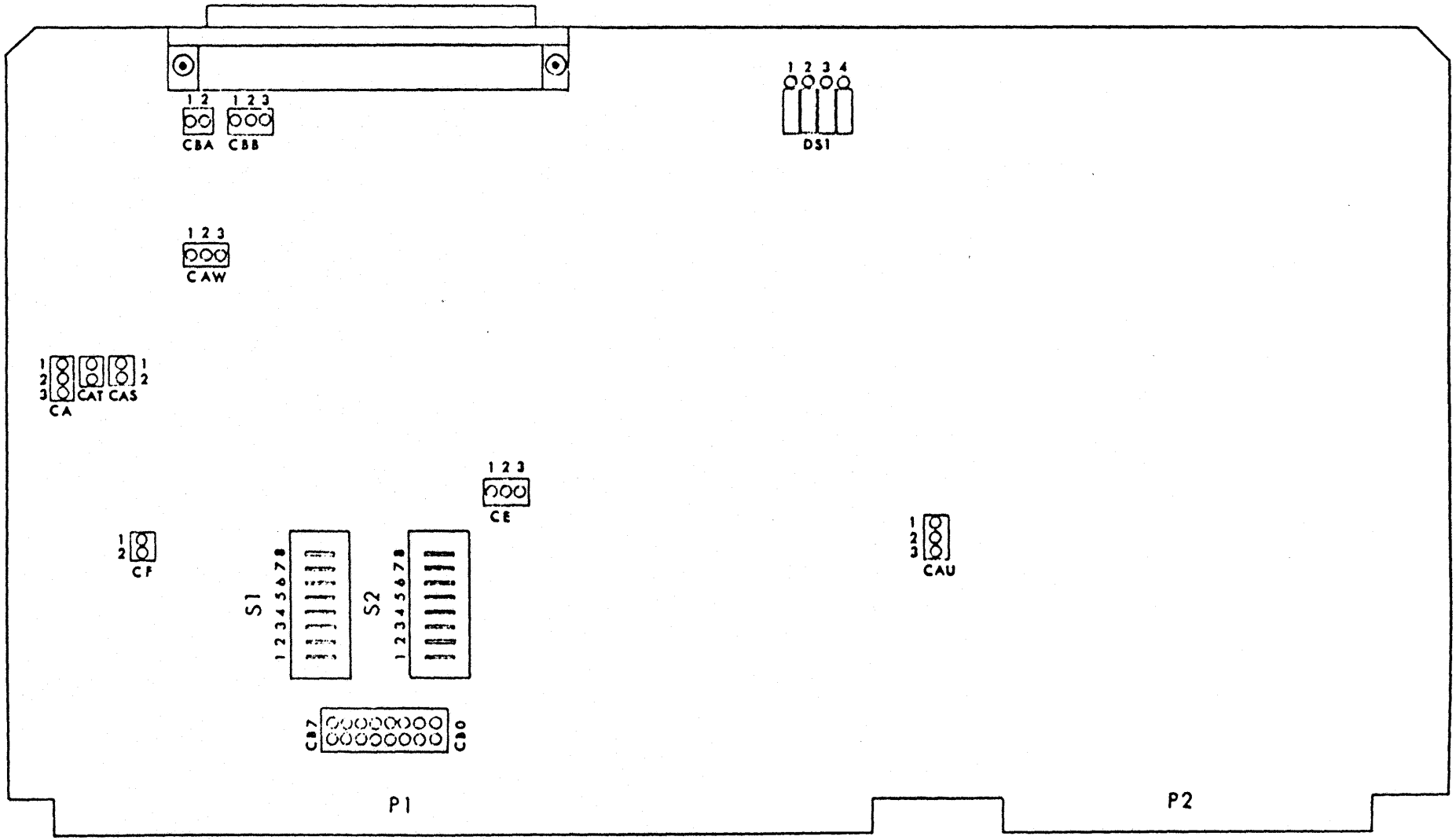

FIGURE A-4. PHYSICAL LAYOUT DIAGRAM

APPENDIX B
ERROR CODES

********** APPENDIX B --- ERROR CODES **********

When a transaction cannot be properly completed, the WNC 5190 reports the error condition in the Send Message Status/ Error byte of the SCB. Likewise, when an error occurs while receiving a packet, the WNC 5190 reports the error condition in the Receive Message Status/Error byte of the RCB. Four error codes are defined for reporting unsuccessful transaction completion and seven for reporting unsuccessful packet reception.

TRANSACTION RELATED ERROR CODES:

CODE	MEANING	
02	WNC 5190 NOT INITIALIZED --	OCCURS WHEN THE CPU ISSUES A 'SEND DATA' COMMAND PRIOR TO INITIALIZING THE WNC 5190.
03	TRANSMITTER UNDERRUN ------	THE 8X305 MICROCONTROLLER COULD NOT KEEP UP WITH THE TRANSMITTER. THEORETICALLY, THIS ERROR SHOULD NEVER OCCUR, BUT IF IT DOES, THE CPU SHOULD RE-ISSUE THE 'SEND DATA' COMMAND. IF THIS ERROR CONDITION PERSISTS, THE CONTROLLER PROBABLY REQUIRES SERVICING.
07	MULTIBUS TIMEOUT ERROR ----	THE WNC 5190 TIMED OUT EITHER ATTEMPTING TO ACCESS THE BUS (1.6 MSEC); OR AFTER HAVING ACQUIRED THE BUS AND INITIATED A MEMORY READ CYCLE, 'TRANSFER ACKNOWLEDGE' FROM SYSTEM MEMORY WAS NOT RETURNED WITHIN 64 uSEC.
08	SCB INVALID ----------	FOR A 'SEND DATA' COMMAND, THIS ERROR CODE IS REPORTED WHEN THE SEND HEADER BYTE COUNT PLUS THE SEND DATA BYTE COUNT EXCEEDS THE VALUE SPECIFIED IN THE ICB FOR MAXIMUM PACKET SIZE.

RECEIVE RELATED ERROR CODES:

CODE	MEANING	
02	RECEIVER OVERRUN ----------	THE 8X305 MICROCONTROLLER COULD NOT KEEP UP WITH THE RECEIVER. THEORETICALLY, THIS ERROR SHOULD NEVER OCCUR, BUT IF IT DOES, THE CPU SHOULD LOG IT IN A STATISTICS TABLE. IF THIS ERROR CONDITION PERSISTS, THE CONTROLLER PROBABLY REQUIRES SERVICING.
03	FRAMING ERROR ----------	THE LAST RECEIVED DATA CHARACTER DID NOT CONTAIN THE APPROPRIATE NUMBER OF BITS AND THE PACKET IS ASSUMED TO BE CORRUPTED.
04	ABORT ----------	AN SDLC ABORT CHARACTER WAS RECEIVED DURING RECEPTION OF THE CURRENT PACKET. A NOISY OR BROKEN CABLE COULD CAUSE THIS AS WELL AS TRANSMITTER UNDERRUN ON THE SENDING SIDE.
05	CRC ERROR ----------	A DATA ERROR WAS DETECTED IN THE RECEIVED PACKET. LOGGING THESE ERRORS CAN HELP TO DIAGNOSE A DEGRADING OR NOISY LINE.
06	RECEIVE BUFFER OVERRUN ----	THE PACKET RECEIVED EXCEEDS THE MAXIMUM PACKET SIZE SPECIFIED IN THE ICB.
07	MULTIBUS TIMEOUT ERROR ----	THE WNC 5190 TIMED OUT EITHER ATTEMPTING TO ACCESS THE BUS (1.6 MSEC); OR AFTER HAVING ACQUIRED THE BUS AND INITIATED A MEMORY WRITE CYCLE, 'TRANSFER ACKNOWLEDGE' FROM SYSTEM MEMORY WAS NOT RETURNED WITHIN 64 uSEC.
08	RCB INVALID ----------	FOR A RECEIVED PACKET, THIS ERROR CODE IS REPORTED WHEN THE SUM OF THE SEND HEADER BYTE COUNT AND THE SEND DATA BYTE COUNT EXCEEDS THE VALUE SPECIFIED IN THE ICB FOR MAXIMUM PACKET SIZE.

*

NOTE THAT NO DATA TRANSFERS OCCUR FROM THE WNC 5190 TO SYSTEM MEMORY FOR ERRORS 02-06 AND 08. ONLY THE RCB IS UPDATED FOR ERROR REPORTING.

IT IS NOT UNCOMMON FOR ONE OR MORE RECEIVE ERRORS TO BE DETECTED BY THE FIRST WNC 5190 TO BE POWERED UP AND INITIALIZED. THESE ERRORS (PROBABLY ABORT AND/OR FRAMING) ARE CAUSED BY THE SECOND WNC 5190 WHEN IT IS IN ITS POWER UP AND INITIALIZATION STAGE.

APPENDIX C
SERIAL INTERFACE

********** APPENDIX C --- SERIAL INTERFACE **********

The signals on the 37-pin J1 connector comply with the EIA Standard RS-422 for balanced circuits and with the EIA Standard RS-449 permitting increased data rates and cable lengths over EIA Standard RS-232-C. Pin descriptions for the J1 connector are listed in the following table.

NON-INVERTING TERMINAL A	INVERTING TERMINAL B	RS-449 CIRCUIT	RS-449 DESCRIPTION
19		SG	SIGNAL GROUND
37		SC	SEND COMMON
20		RC	RECEIVE COMMON
4	22	SD	SEND DATA
6	24	RD	RECEIVE DATA
7	25	RS	REQUEST TO SEND
9	27	CS	CLEAR TO SEND
11	29	DM	DATA MODE
12	30	TR	TERMINAL READY
13	31	RR	RECEIVER READY
17	35	TT	TERMINAL TIMING
5	23	ST	SEND TIMING
8	26	RT	RECEIVE TIMING
18		TM	TEST MODE
3	21		UNDEFINED - RESERVED AS SPARE INPUT TO WNC 5190.

TABLE 2. WNC 5190 SERIAL INTERFACE

Two WNC 5190s set up for direct connect via twisted-pair cable can communicate up to 400 Ft. at 1 Mbits/sec and up to 200 Ft. at 2 Mbits/sec. To configure each WNC 5190 for direct connect do the following:

1. Remove jumper option CBA and set jumper option CBB between 1 - 2 to generate Terminal Timing.
2. Set jumper option CAW to 1 - 2 for 2 Mbit/sec data rate or to 2 - 3 for 1 Mbit/sec data rate.
3. Set switch 2 of Switch Bank S2 to the ON position.

A special twisted-pair cable is required to connect two WNC 5190s directly and should be configured as shown on the next page.

5190 #1		5190 #2
J1-19 SIGNAL GROUND	.....	SIGNAL GROUND J1-19
J1-37 SEND COMMON	.....	RECEIVE COMMON J1-20
J1-20 RECEIVE COMMON	.....	SEND COMMON J1-37
J1-4 SEND DATA - A	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	RECEIVE DATA - A J1-6
J1-22 SEND DATA - B	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	RECEIVE DATA - B J1-24
J1-6 RECEIVE DATA - A	<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<	SEND DATA - A J1-4
J1-24 RECEIVE DATA - B	<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<	SEND DATA - B J1-22
J1-7 REQUEST TO SEND - A	>>>>>>>>>>>>>>>>>>>>>>>>	CLEAR TO SEND - A J1-9
J1-25 REQUEST TO SEND - B	>>>>>>>>>>>>>>>>>>>>>>>>	CLEAR TO SEND - B J1-27
J1-9 CLEAR TO SEND - A	<<<<<<<<<<<<<<<<<<<<<<<<	REQUEST TO SEND - A J1-7
J1-27 CLEAR TO SEND - B	<<<<<<<<<<<<<<<<<<<<<<<<	REQUEST TO SEND - B J1-25
J1-5 TERMINAL TIMING - A	>>>>>>>>>>>>>>>>>>>>>>>>	RECEIVE TIMING - A J1-8
J1-23 TERMINAL TIMING - B	>>>>>>>>>>>>>>>>>>>>>>>>	RECEIVE TIMING - B J1-26
J1-8 RECEIVE TIMING - A	<<<<<<<<<<<<<<<<<<<<<<<<	TERMINAL TIMING - A J1-5
J1-26 RECEIVE TIMING - B	<<<<<<<<<<<<<<<<<<<<<<<<	TERMINAL TIMING - B J1-23

APPENDIX D
INTERPHASE 5110 MEDIA ACCESS UNIT

******** APPENDIX D --- INTERPHASE 5110 MEDIA ACCESS UNIT ********

The Interphase 5110 Media Access Unit (MAU), used in conjunction with the WNC 5190, significantly extends transmission distances as shown in the following table.

DATA RATE (MBITS/SEC)	DISTANCE/CABLE TYPE RG-59 (FT)	RG-11 (FOAM) (FT)	JT3412J (FT)	JT3750J (FT)
1	5,000	12,000	20,000	32,000
2	4,200	9,500	15,000	25,000

The 5110 MAU is comprised of an asynchronous high speed modem mounted on a Multibus size PC Board, and will operate at data rates up to 2 Mbits/sec. It only requires power (+5VDC and +12VDC) from the Multibus backplane. The modem employs FSK modulation with an FM Carrier frequency of 5 MHz, as well as filtering, to reject EMI and RFI noise. FSK transmission and shielded coaxial cable provide reliable data transmission and immunity from high noise environments. It interfaces to the WNC 5190 via a 37-conductor flat ribbon cable.

Two coaxial cables are required for full duplex operation. Baseband data is transmitted via BNC connector J1; and baseband data is received via BNC connector J5. Each coaxial cable must be terminated into 75 ohms on both ends and are provided on board. Jumpers Y and Z must be on for proper termination. Listed below is the jumper configuration for the 5110 MAU that is set at the factory. The only one that is user selectable is 'W' which passes BPRN on the Multibus to BPRO when the jumper is ON. The rest should be left alone.

	JUMPER DESIGNATION	STRAP SELECTION		JUMPER DESIGNATION	STRAP SELECTION
	A	OFF		O	OFF
	B	OFF		P	OFF
	C	OFF		Q	1 - 2
	D	OFF		R	OFF
	E	OFF		S	1 - 2
	F	ON		T	1 - 2
	G	OFF		U	1 - 2
	H	OFF		V	2 - 3
*	J	ON		W	ON
*	K	ON		X	OFF
	L	ON		Y	ON
	M	OFF		Z	ON
	N	1 - 2			

* INDICATES STRAPS WHICH CAN BE LEFT OFF IF RELAY K2 PIN 1 IS JUMPERED TO RELAY K1 PIN 1; AND IF K2 PIN 2 IS JUMPERED TO +12VDC.

DIAGNOSTIC DISPLAYS

Six diagnostic LEDs are provided on the 5110 for diagnosing problems. A definition for the ON condition of each LED is listed below.

DS1	FLAT RIBBON CABLE CONNECTED TO POWERED ON WNC 5190
DS2	NOT APPLICABLE
DS3	REQUEST TO SEND (FROM WNC 5190)
DS4	NOT APPLICABLE
DS5	+12 VDC POWER
DS6	+5 VDC POWER

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