

# SUPERLETTER

Serving SuperBrain<sup>®</sup> Owners and Users Around the World

April/May 1982  
Vol. 2 No. 2

Your attention is drawn to the April issue of BYTE, specifically pages 74 and 75 (a two-page spread by Intertec) and page 434, which goes into detail about a new price cut plus a return and refund policy now being initiated by the factory.

In a nutshell, prices have been hacked on the entire Intertec line and the factory will now begin reimbursing freight expenses to customers for any new computers that must be returned to the Columbia plant during the warranty period.

We urged this type of customer protection action over a year ago in an open editorial. We're happy to see Intertec's actions. It's only a start, but an important one.

The BYTE article on page 414 also goes on to say that Intertec will now feature a company sponsored users-group and a new magazine for users. That raised eyebrows here, as you can imagine. Having published without a break for the last year and a half, we know what it takes to provide a true and beneficial service to computer users.

By the way, interfacing a SuperBrain to an 8" drive is a lot more difficult than we first imagined. Have any of you been able to do it at a reasonable price? Let us know. The CP/M Users Group software will have to wait until it's all ironed out.

Instead of listing the comparisons of the different BIOSs now becoming available, we're printing a complete run-down of each separately, so that you can decide (considering costs and features) which you prefer.

Incidentally, we do not sell, trade or give away the names of subscribers to any magazine, advertiser or mailing service under any circumstance. We believe in protecting the privacy and confidentiality of our subscribers.

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suggest they subscribe. Everybody benefits if we are able to grow and thus service your information needs even better in the months ahead.

*Albert Abrams*  
EDITOR

## Technical Corner

### HARDWARE INFORMATION ON THE SUPERBRAIN

*Third in a Series*

by Jonathan W. Platt

Special thanks to  
Paul L. Kelley, Ph.D.

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#### The Communication System

This system is comprised of three chips; two 8251 USARTs and the baud rate generator. The baud rate for each USART can be set by writing an eight bit digit to the generator (port 60H). The upper four bits output to the generator determine the main port baud rate while the lower four bits set the auxiliary port baud rate. There are 16 baud rates available. See further discussion, below, about the multipliers of the baud rates.

| Upper or lower nibble (hex) | Baud Rates |       |        |
|-----------------------------|------------|-------|--------|
|                             | x 1        | x 16  | x 64   |
| 0                           | 800        | 50    | 12.5   |
| 1                           | 1200       | 75    | 18.75  |
| 2                           | 1760       | 110   | 27.5   |
| 3                           | 2152       | 134.5 | 33.625 |
| 4                           | 2400       | 150   | 37.5   |
| 5                           | 4800       | 300   | 75     |
| 6                           | 9600       | 600   | 150    |
| 7                           | 19200      | 1200  | 300    |
| 8                           | 28800      | 1800  | 450    |
| 9                           | 32000      | 2000  | 500    |
| A                           | 38400      | 2400  | 600    |
| B                           |            | 3600  | 900    |
| C                           |            | 4800  | 1200   |
| D                           |            | 7200  | 1800   |
| E                           |            | 9600  | 2400   |
| F                           |            | 19200 | 4800   |

Communication to the outside world is done through the main and auxiliary serial interface ports. The main port has been made a bit more useful than the auxiliary port. It will support RTS, CTS, DSR, DTR, RI and internal and external transmit/receive clocks enabled by the dipswitches on the processor board. The RI (ring indicator) can be tested via PPIB-6. The auxiliary port will support only RTS and DSR. RTS for the auxiliary port, which is not documented in the manual, is shown on the schematics but may not be active.

A printer which supports reverse channel is well suited for connection to CTS of the main port. CTS must be true to transmit. DSR must be handled by specific software which is slower than a hardware protocol. If you have a device which needs no extensive protocol, it is better off on the aux port since DSR would probably be quite sufficient whereas the main port should be saved for higher speed devices. I recommend that the printer (e.g. NEC 5520) be put on the main port and the modem be put on the aux port (unless you need the ring indicator). Intertec, of course, recommends the opposite.

The 8251 USARTs are minimally programmable. The 8251 is programmed by writing two to four command codes to the status port. When the 8251 is first powered up or is reset, its logic assumes that a Mode Select Command Code will be the next byte of data sent to the status port. If the Mode Select Command specifies synchronous mode, the 8251 logic expects the subsequent command input to be the SYNC character - or if specified in the Mode Select Command, two SYNC characters; SYNC1 and SYNC2. As soon as a Mode Select Command Code - and SYNC characters, if needed - has been received, 8251 logic switches to expecting Control Select

*Continued on Page 2*

# New Products

## SuperBrain Operating System (SOS) 3.4

Jonathan W. Platt  
Pine Villa, Apt. 114  
200 East University Boulevard  
Melbourne, Florida 32901  
(305) 724-6148

### Product and Pricing Sheet

SOS 3.4 is a field tested SuperBrain BIOS with many features which extensively use the SuperBrain's real potential that the standard Intertec system does not provide. Increased versatility and ease of use makes this SOS system truly a Super System!

### SOS Features Include:

#### DISK SYSTEM (All selectable under program control)

- IE Systems PROM feature-compatibility
  - Variable track to track seek rate
  - Variable number of tracks (35 or 40, even 128)
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  - BIOS call for disk rotation speed check
  - Read-After-Write disk verification
- Single or double-sided disks settable for each drive

#### I/O SYSTEM (All selectable under program control)

- Full IOBYTE implementation
- Main and Auxiliary Port Communications:
  - 23 Selectable Baud rates
  - Synchronous or Asynchronous operation to both ports
  - Four selectable protocols (DSR, ^S/^Q, ETX/ACK or None)
  - 256 byte input buffer on READER device
  - 256 byte output buffer on LIST device
  - Warning beep every 10 seconds if data is sent to a port and there is no device attached
  - Selectable BREAK key sends the break signal to the PUNCH device and flushes the type-ahead buffer and the LIST output buffer if set to the same port
- Console/Screen:
  - Selectable video field
  - Time display (Intertec TIME program compatible)
  - Internal date (Intertec DATE program compatible)
  - 35 Programmable function keys. Five and three characters.
  - Any number of function keys can be "linked" together to create functions greater than five characters

- Selectable key-click volume
- Selectable auto-repeat delay
- Selectable auto-repeat rate

#### OTHER (All accessible through BIOS)

- Timer word keeps number of seconds since last cold boot
- More than thirty BIOS calls including:
  - Direct-to-device I/O and status
  - READER and PUNCH device status
  - Set key-click volume, repeat delay, repeat rate
  - Push/Pop cursor position (Up to 256 levels)

To receive any of the products summarized below, send check, certified check or money order for the amount listed payable to the above address.

When purchasing the SOS, send one diskette that has been SYSGENed on your machine. This makes your end-price cheaper since no royalties have to be paid to Digital Research with this "Software Consultant" method.

SOS 3.4 will only work on SuperBrains with 512 bytes/sector and 10 sectors/track using CP/M 2.2. Any IE Systems PROM or Intertec DOS 3.0 and above fit those requirements.

Upon request, a listing of the commented source for SOS 3.4 will be sent with the system and manual for an additional \$200. The SOS system itself must be bought for the right to buy the source. The source code, which is not usually available with any other systems, will allow a more comprehensive understanding of the SOS program. This will enable a user to change the SOS to satisfy his own personal needs should there be one that the SOS can't handle.

For those of you who are exasperated at the lack of technical information for the SuperBrain from Intertec, "Hardware Information on the SuperBrain" is a 20 page document describing the circuitry of the SuperBrain, the various subsystems and how they function from the system programming viewpoint.

### Price Summary

|   |          |
|---|----------|
| "Hardware Information on the SuperBrain" .....  | \$ 50.00 |
| SuperBrain Operating System (SOS) 3.4 plus "SETSYS" SOS Configuration Program SOS User's Manual, and partial BIOS listing ..... | \$140.00 |
| Commented Source Copy of SOS 3.4 .....  | \$200.00 |
| Commented Source Copy of SETSYS 1.0 .....   | \$100.00 |
| User's Manual .....   | \$ 50.00 |
| SOS PROM 3.4 .....  | \$ 50.00 |

\*All prices include shipping\*

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### Technical Corner, Continued from Page 1

Codes. This persists until the 8251 is reset or a special Control Select is output forcing the choice back to Mode Select. No buffering is necessary between commands (i.e. NOPs).

Intertec has CONFIGUR set the 8251 clocks to 1/16 the baud rate produced by the baud rate generator. This multiplier produces the baud rates as described above. If an even higher or lower baud rate than available is desired, a different multiplier may be used. The other multipliers available on the 8251 are one and 1/64 times the baud rate. The 8251 can run from DC up to 615/16K baud in asynchronous mode or 56K baud in synchronous mode. So you could go as low as 12.5 baud or as high as 38.4K baud via the baud rate generator. Even so, at 38.4K baud there is only time enough for about 150 CPU instructions before another character will arrive - not a whole lot of time to process it. The baud rate generator rates may be bypassed by using an external clock through the dipswitches as described in the user's manual. Of course, the clock rate should not exceed the system's clock frequency.

With the advent of Intertec's new DOS 3.1 (and a few more bugs), they have included code to handle the programming for synchronous mode. CONFIGUR now gives you a choice of asynchronous or synchronous mode with the main port only. They have their values a little mixed up, however. And until they get it fixed, when you specify one SYNC character, the code sets it for two SYNC characters and vice versa. Also, Clear-to-End-Of-Screen (CLEOS) does not work properly, the ^T time display toggle will turn on display but will not turn it off and when the break key is hit, the main port break signal turns on and STAYS on. At the time of this writing, Intertec just released DOS 3.2 which (hopefully) will alleviate those problems.→

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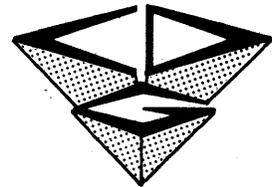
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## CONTINENTAL DATA GROUP

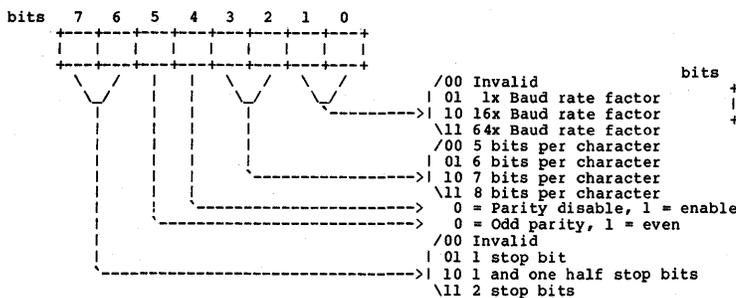
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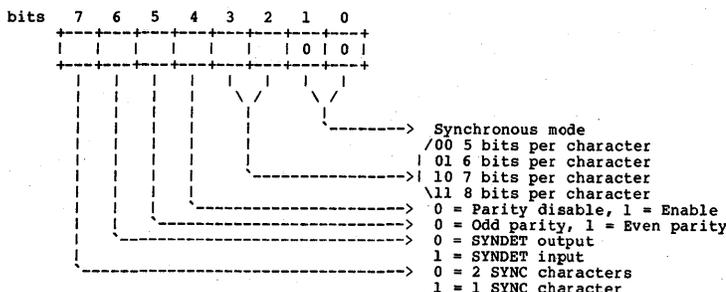


The Mode Select Command formats are as follows:

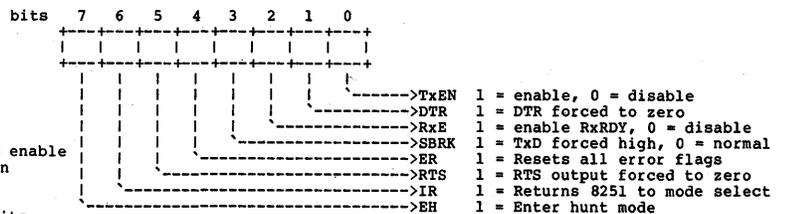
### Asynchronous Mode Select



### Synchronous Mode Select



After the Mode Selection and SYNC character(s), if necessary, the Control Command is written in the following format. Any subsequent write to the status port after this will be the Control Command unless bit 6 is set.



Input from the status port is as follows:

| Bit | Information                    |
|-----|--------------------------------|
| 0   | Set for transmit ready         |
| 1   | Set for receive ready          |
| 2   | Set for transmitter empty      |
| 3   | Set for parity error           |
| 4   | Set for overrun error          |
| 5   | Set for framing error          |
| 6   | SYNDET (SYNC character DETect) |
| 7   | Set for data set ready         |

Continued on Page 8

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## —Guest Article—

### The SuperBrain and a Lathe Machine: A Unique Application

by Henry Munro

Bristol Engineering Company  
210 Beaver Street, Box 696  
Yorkville, Illinois 60560

In early 1980 we started using the SuperBrain to store and transmit programs to a CNC lathe. We have a Sheldon H1710 lathe with a Bendix System 5 control, purchased in 1976. From the beginning we were searching for a system to eliminate the punching, handling and storing of the paper tapes. We got very little encouragement and finally pretty much struck out on our own. The first and primary hurdle was providing a suitable I/O interface between the CNC system and any computer system we might buy.

All Bendix had to offer was a "high speed punch output" accessory designed to drive either a Facit or Remex punch. This unit supposedly had baud rates available up to 600, which was still slow, but a lot better than the 110 baud output of the standard teletype connection. For an input to the system, Bendix offered a "BTR" (behind tape reader) manufactured by Dwight Instrument Co. of Lyndhurst, NJ. Both of these units provided an RS232C port for connection to the computer.

We had these two items installed on the Bendix control, and then got our first SuperBrain and began the marriage. There has never been any trouble with the output system provided by Bendix. This was their own design, and although it was advertised to go only to 600 baud, we found that there were DIP switch settings that provided much higher baud rates. We found the best (highest without garbling) rate to be 2400 baud. (Transmission is over a shielded, 3-conductor cable 110 feet long.)

Dwight Instrument's BTR was quite another matter. We found before we had made a good start on the marriage that the knowledgeable people had all left Dwight Instrument, and were at Digital Design, Inc. (Ed Gerry and Lou Dicianni, 201-839-8808.) Although these gentlemen were helpful to a point, it was apparent that they were not ready to do the amount of modification necessary to get the system working. This left us on our own.

Designed and programmed to receive data from a tape reader, the Bendix System 5 had certain characteristics and requirements that complicated the problem. If we had been in a position to modify the executive program for that unit we might have had an easier time, but getting help in that area was at least as difficult as getting programming help from Intertec.

This unit received the data in bursts of 256 characters, stopping briefly to dump the buffer into memory at the end of each burst. We quickly found that each time the transmission was stopped (the DSR signal went low) we lost one character. In trying to figure out how this BTR could have been used successfully elsewhere, we could only assume that it was used in a system that transmitted a block at a time, blocks being separated by a carriage-return-line-feed combination. Most machines receiving that type of transmission would act on the carriage-return, and probably never miss the line-feed character that was lost.

As each character transmitted serially to the BTR was received, a sprocket pulse output was generated, which caused the character to be entered into the machine in parallel. Since there would normally be one character in transit at the instant that the machine buffer became full and the DSR signal went low, this character must be stored in the UART until the next time the DSR signal goes high. No such gating of the sprocket pulse existed in the BTR as received, and this last character was dumped during the time the machine could not receive it. By adding a gate to the "Data Ready" output of the UART, preventing a sprocket pulse and the resultant "Data Ready Reset" from being generated, we were able to retain the otherwise lost character.

Bendix designed the System 5 to accept either EIA or ASCII code. Which code is to be received is determined by the first carriage-return (or EOB) character received. If this is a ODH then all subsequent characters have to be in ASCII, and more specifically in even parity, or a parity error occurs. If a 80H (EIA EOB) is received, then all subsequent characters have to be odd parity.

This system would work beautifully except for a quirk of the SuperBrain for which we have been unable to get help from anyone. The only command we have been able to use to get output from the main port is PIP PUN:. (On our first SuperBrain, with which most of this was worked out, the DSR was not implemented on the AUX port.) PIP PUN: is supposed to output a string of nulls before and after the file transmission for leader and trailer on the tape. For some unknown reason, the SuperBrain will not willingly output nulls, and instead outputs a random mixture of a few nulls, a lot of 80H codes, and a lot of COH (@) codes. Now, the COH codes don't hurt anything, but the 80H codes are EIA EOB codes, and cause the Bendix system to start looking for EIA code. Of course, the very next character, and practically all subsequent characters are then considered as parity errors.

Fortunately, along with a lot of other unnecessary logic, the BTR included its own parity checking system. This at first seemed to be giving us trouble because it was hard wired to accept even parity and locked up whenever one of the 80H codes was received. However, by rewiring this to gate the sprocket pulse output whenever a parity error occurred (just dropping the character rather than setting an alarm) we were able to filter out all the 80H codes, and get past the garbage that the SuperBrain was outputting.

Another problem came in developing a system that would properly terminate transmission and allow the computer to advance to the next step (in a SUBMIT program) to verify the transmission. When reading a tape, the Bendix system looks for either an "M02" or an "M30". On an "M02" followed by a carriage return, the tape reader is stopped, and the program is dumped into memory. An "M30" performs the same operation, except that the tape reader is reversed to rewind the tape, and a percent sign is searched to stop the rewind. In either case, the reader-forward signal (translated into the DSR) was terminated immediately upon receipt of the carriage-return. This left a line feed and a string of nulls for the computer to transmit before it was ready to proceed. If the "M02" or "M30" was omitted from the end of the program, the computer finished its transmission in great shape, but the Bendix system would not store the program.

Solving this mess involved several more changes in the logic of the Dwight Instrument BTR. It was necessary to generate a DSR output to the computer while the

*Continued on Page 6*

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**Guest Article, continued from Page 5**

Bendix unit was giving the "rewind" signal (tape reader reverse). Then it was necessary to include a timer to keep this signal high long enough for the computer to finish transmitting its string of nulls. In order to make these modifications work, each transmission is ended with an M30, CR, %, CR. When the "M30" is read, the reader forward signal stops, and the reader reverse signal goes true. This starts the timer and continues the DSR output to the computer. When the percent sign is received, the reader reverse signal goes false, but the timer maintains the DSR high long enough for the computer to dump everything.

Obviously, with the filtering of parity errors and other uncertainties of the system, it is necessary to verify all transmissions. The SUBMIT programs used to transmit and record the CNC programs provide for this. After the file is transmitted to the machine, the operator retransmits (punches) it back to the computer. It is stored as the same file except with type .VER. A BASIC program is then run which compares this file with the original file, line by line. Both versions of each line in which there is any variation are printed out (the line from the original file with a prefix "S" and the received line with the prefix "R"). This printout may then be taken to the machine and any errors corrected with the edit facility at the machine.

After a program has been run on the lathe, it is retransmitted to the computer for storage. (Frequent edits occur during the running as tooling and other conditions vary.) The program is "punched" back to the computer twice, and filed once as type .REC and once as type .VER. These two files are then compared with the same verification program used before. Then the type .REC file is compared with the original file. This final comparison gives the Engineering Dept. a listing of all edits that have occurred during the running of the program. If all edits are acceptable, and the revised program is to be filed, then the original program is renamed type .OLD and the type .REC file is renamed type .DAT. The type .VER file is erased.

It probably should be noted that the recording (or "punching") operation, which utilizes the Bendix designed high speed punch output, has been very nearly perfect, errors almost never showing up in the verification procedure. Unfortunately, there is still some room for improvement in the BTR and its ability to accurately receive the data as transmitted.

In summary, the SuperBrain has given us a very handy system for generating and

storing our CNC programs. However, anyone venturing into this kind of program should be aware that there's more involved than just transmitting data. You must be aware of the peculiarities of both systems as to what they require to initiate and terminate each transmission, and what they are able to output in initiating and terminating transmission. Compatibility in these areas seems to have been the biggest problem once the system was made to retain all characters when transmission was interrupted.

Most recently, we have added a Corvus 20 Mbyte disk to the system, but that's another story.

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## —Book Review—

**How To Patent Computer Programs**, by S. Pal Asija — a patent attorney who successfully secured a patent for a program that he designed.

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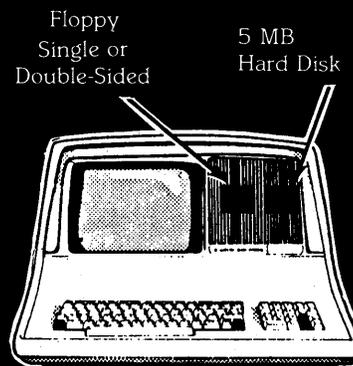
This unique "How To" guide is an appropriate reference book in the library of every company that develops any type of proprietary computer program, every attorney who is involved in copyright or patent law, and attorneys or accountants who are involved with research and development ventures.

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# Letters to the Editor

DEAR SUPERLETTER:

I have been receiving Superletter since the beginning and really look forward to it. There should be more pages but at least it concentrates on my computer.

The reason I'm writing is to bring your attention to my experiences with Systems Integration in New York. Like many others, I started out with the TRS-80 but at that time it wasn't capable of serious computing. Since the SuperBrain was being used where I worked, I decided to purchase one.

Fortunately, I bought it from Dale Walker of Systems Integration along with his implementation of CP/M called IOS. Not all of us have the time and experience to write system utilities or even to figure out things available from the CP/M networks. IOS did everything very nicely. With the operating system I received the following:

- Batch Monitor
- Sorted disk directory with attributes
- Memory tester
- Selective file eraser with recovery capability
- Keypad programmer (including top row of regular keyboard)
- Interface with clock from user program
- Directory sorter
- File splitter
- Spooling capability
- XFER (like PIP with much more)
- Auto program upon power-up
- And much, much more...

With IOS my access time is 6ms and would you believe that loading MBASIC requires only four seconds. My configuration is now so flexible that I can swap keypad assignments with ease.

Even better than his software is his knowledge of the SuperBrain and his willingness to share it. Finally, a vendor who will tell you which language is best for your application instead of just sending you the package off the shelf.

System Integration has my highest recommendation. I hope Superletter will someday interview Dale Walker for real insight into the world of SuperBrain.

Keep up the good work.

Darrell Bushnell  
23 Vineyard Place  
Passaic, New Jersey 07055

DEAR SUPERLETTER:

RE: Your letter to Heather Shanklin, Sales and SUPERLETTER Feb/March 1982 Vol. 2 No. 1

1) The information provided indicates that machine code can be written to address the CRT. At this time the language we develop our programs in, CBASIC, is not linkable to machine code directly but works through an interpreter.

2) It would be most helpful if we could get more information on the ESCAPE sequences used (page 2, col. 2, para. 7). We could then modify the ADDS, CRT definition to compute the program commands.

Again, thank you for your time and effort in this matter. Please let me know if you can help us obtain the needed CRT information.

Barbara W. Carleton  
Manager  
Customer Service Department  
Structured Systems Group, Inc.

*Editor's note: We're still working on this problem. We'll keep our readers informed.*

DEAR SUPERLETTER:

I would like to personally thank you for supplying the necessary information, making it possible for me to interface the Microline 83A printer by Okidata. I have enclosed all of the necessary settings, so that it may help others who are trying to use Microline 83A printer with the SuperBrain.

### SuperBrain Auxiliary Port Configuration

|                  |         |
|------------------|---------|
| Baud Rate        | 110*    |
| Stop Bit         | 1       |
| Character Length | 8       |
| DSR              | enabled |
| No parity        |         |

\*Note: The character losses at baud rates 300-1200 were too extensive for any use!!!

### RS-232-C Pin Connections

| SuperBrain            |     | Microline 83A            |
|-----------------------|-----|--------------------------|
| 1 (protective ground) | ==> | 1 (protective ground)    |
| 3 (transmitted data)  | ==> | 3 (received data)        |
| 7 (signal ground)     | ==> | 7 (signal ground)        |
| 20 (data set ready)   | ==> | 20 (data terminal ready) |

Note: M83A's pin #11, supervisory send data or BUSY equivalent, is not used. This pin should only be used when using higher baud rate than 300, and this also requires a X-on, X-off protocol.

### Microline Dip Switch Settings

#### Front Operating Panel Dip Switches

|     |      |   |
|-----|------|---|
| SW1 | —    | Setting selects   |
| SW2 |      | US ASCII  |
| SW3 |      | character set.  |
| SW4 |      |   |
| SW5 | —    | 8 code unit.  |
| SW6 | OFF: | Automatic carriage when received CR. Do not move paper up one line. |
| SW7 | OFF: | Ignore DEL code.  |
| SW8 | ON:  | Low speed serial interface. (OFF / parallel)                        |

#### Rear Control Circuit Board (LEPV-1) Dip Switch Settings

|     |      |   |
|-----|------|---|
| SW1 | OFF: | Pin #11, SSD polarity/Mark when Ready, Space when Busy. |
| SW2 | —    |   |
| SW3 |      | OFF: Baud Rate 110.                                     |
| SW4 |      |   |
| SW5 | —    | NOT USED  |
| SW6 | OFF: | No parity.  |

#### Rear Control Circuit Board Short Plugs Jumper Connections

|     |         |  |
|-----|---------|--|
| SP1 | SIDE B: | DTR Signal is for space (ON) after power on. |
| SP2 | SIDE A: | Unused state.                                |

#### Implementation of 2K High Speed Buffer Card on the Microline 83A

General Comments: At 1200 baud rate, the 2K buffer fills up after about five pages of text; and while the buffer is dumping, the buffer loses approximately two pages of text thereafter. The Supervisory Send Data, pin #11 on the printer, can be used to switch the polarity and send out the BUSY signal to the SuperBrain when the buffer is down to 139 characters or less. But the polarity does not switch back once the buffer is empty, unless one has the capability of X-ON and X-OFF Protocol. Therefore, I configured the SuperBrain's Auxiliary Port Baud Rate at 600 and did not use the SSD signal of the Microline printer.

### SuperBrain Auxiliary Port Configurations

|                  |         |
|------------------|---------|
| Baud Rate        | 600     |
| Stop Bit         | 1       |
| Character Length | 8       |
| DSR              | enabled |
| No parity        |         |

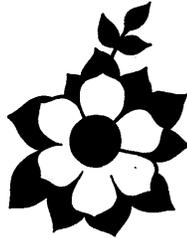
### RS-232-C Pin Connections

| SuperBrain            |     | Microline HS Buffer                   |
|-----------------------|-----|---------------------------------------|
| 1 (protective ground) | ==> | 1 (protective ground)                 |
| 3 (transmitted data)  | ==> | 3 (received data)                     |
|                       |     | 4-5 (request to send / clear to send) |
|                       |     | ↳ absolutely necessary.               |
| 7 (signal ground)     | ==> | 7 (signal ground)                     |
| 20 (data set ready)   | ==> | 20 (data terminal ready)              |

### Microline Dip Switch Settings

|     |   |  |
|-----|---|--|
| SW1 | — | US ASCII   |
| SW2 |   | character set.   |
| SW3 |   | 8 code unit.   |
| SW4 |   | OFF: Auto carriage/no line feed at CR.                         |
| SW5 |   | Ignore DEL code.   |
| SW6 |   | Parallel interface   |
| SW7 |   |  |
| SW8 | — | (used even though RS-232-C option is used on the buffer card.) |

Continued on Page 8



## FIRST CLASS

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**Technical Corner, Continued from Page 3**  
 The following was inadvertently omitted from Technical Corner's first installment of "Hardware Information on the SuperBrain" in the December 1981/January 1982 issue.

### CPU-2 Ports

|                         | Hex<br>Chip Location |
|-------------------------|----------------------|
| LS174 clock pin         | 10                   |
| FD1791-B01 FDC          |                      |
| Status/Command register | 08                   |
| Track Register          | 09                   |
| Sector Register         | 0A                   |
| Data Register           | 0B                   |

## SuperClassifieds

**EXTENDED ASSEMBLER:** Finally an assembler with the sophistication of mainframe software, designed specifically for the SuperBrain. Encompasses entire Z-80 instruction set, listing control, conditional assembly, macros, external text assembly, and the usual. An accompanying manual contains complete documentation and easy to reference tables. Only \$125, includes binary, 2 demo programs, manual, AND THE SOURCE CODE!... Send check or money order to **Morrow's Super Software**, Box 307, San Luis Rey, California 92068-0307.

**Letters to the Editor,**  
 Continued from Page 7

### Rear Control Circuit Board (LEPV-11) Dip Switch Settings

|     |   |
|-----|---|
| SW1 | OFF: SSD polarity/Mark when Ready, Space when Busy. |
| SW2 | OFF: 600 Baud Rate.                                 |
| SW3 | OFF:  |
| SW4 | ON: -   |
| SW5 | NOT USED.   |
| SW6 | OFF: No parity.                                     |

### Rear Control Circuit Board Short Plugs Jumper Connections

|     |  |
|-----|--|
| SP1 | SIDE B: DTR signal is for space (ON) after power on. |
| SP2 | SIDE A: Unused state.                                |

### Buffer Card Interface Circuit Board (RSCL-2) Dip Switch Settings

|      |  |
|------|--|
| SW1  | OFF: Even parity (invalid when SW2 is ON.)                     |
| SW2  | ON: No parity.   |
| SW3  | OFF: 8 data bits.  |
| SW4  | ON: -  |
| SW5  | ON:  |
| SW6  | OFF: 600 baud rate.  |
| SW7  | OFF: Block end code (LF) invalid in CENTRONICS UNBLOCKED MODE. |
| SW8  | UNUSED   |
| SW9  | OFF: -   |
| SW10 | OFF:   |
| SW11 | ON: -  |
| SW12 | ON: Space always after power on switching.                     |
| SW13 | ON: SSD polarity/Space at Busy state.                          |

|      |   |
|------|---|
| SW14 | OFF: Ready to receive regardless of Mark or Space of CD (PIN #8) signal.                      |
| SW15 | ON: RS-232-C interface selection.   |
| SW16 | ON: Change of current loop function (two-wire system). *) invalid in RS-232-C interface mode. |

*Note: Centronics Unblocked (mode-d) has a free block transfer format. Also, if SSD is used, the BUSY signal is sent out when buffer is less than or equal to 139 characters.*

*If Centronics RS-232 (mode-c) is selected, then the control-A must be sent to the printer to indicate SOH.*

*Other communication modes are a) Oki Simplex Busy, b) Oki Simplex Acknowledge, f) Centronics Blocked Duplex, and g) Dec Duplex.*

### Buffer Card Interface Circuit Board Short Plugs Jumper Connections

|     |  |
|-----|--|
| SP4 | SIDE A: Current supply to receiving circuit<br>*) Not supplied     |
| SP5 | SIDE B: Current supply to transmitting circuit<br>*) Not supplied. |

Elvin Park  
 918 Honeywood Road  
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 (213) 476-3792