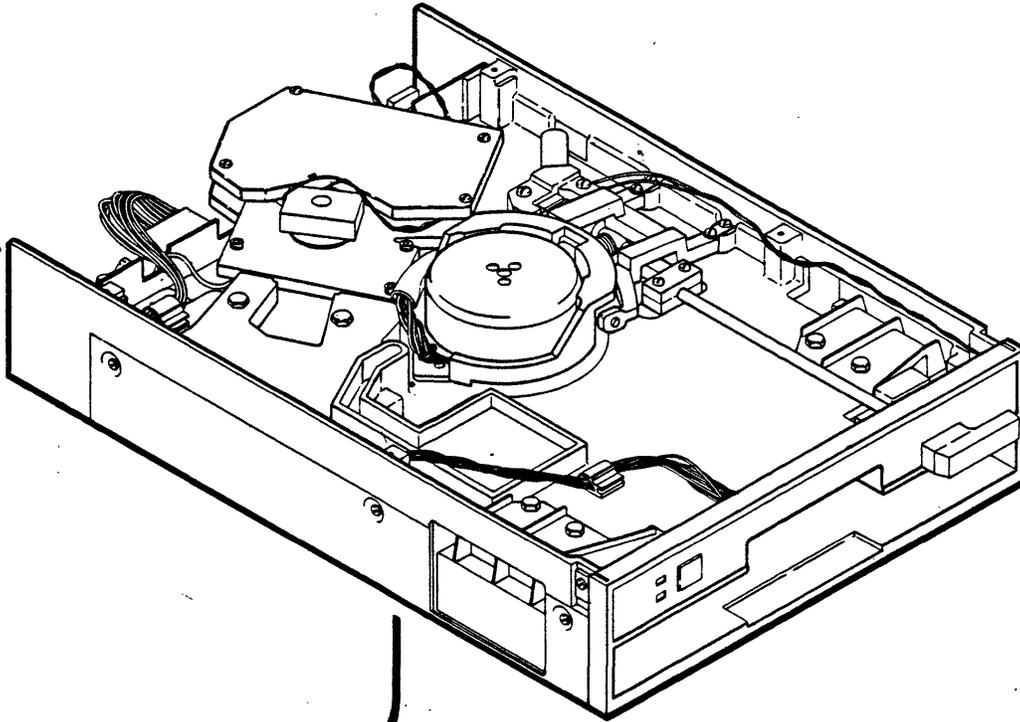


**IOMEGA®**

# TECHNICAL DESCRIPTION MANUAL



**OEM DISK STORAGE SUBSYSTEM**

**ALPHA-10H/10.5H™ WITH EXTENDED SCSI**

IOMEGA Corporation  
NOVEMBER 1984

1821 West 4000 South

Roy, Utah 84067  
00701300-000

**FCC WARNING**

**This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with this instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.**

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Normal precautions used in handling electrically powered equipment should be followed at all times. Never work on the Disk Storage Subsystem with the power source activated. IOMEGA assumes no liability for incidents resulting from careless or improper use of this equipment or inaccuracies in this manual.

**ALPHA-10H/10.5H™ OEM  
DISK STORAGE SUBSYSTEM  
WITH EXTENDED SCSI**

**TECHNICAL  
DESCRIPTION  
MANUAL**

**December 1984**



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## **PREFACE**

This Technical Description Manual provides information for interfacing of a 10/10.5 megabyte, 8 inch disk storage subsystem, identified by IOMEGA as Alpha-10H/10.5H™. The subsystem consists of a controller, up to two disk drives, and removable 10/10.5 megabyte cartridges. Through the flexible magnetic disk media and the unique design of its drive, the subsystem offers the advantages of (1) rigid disk, Winchester-like performance and reliability; and (2) removable, low cost flexible media.

This document provides original equipment manufacturers (OEMs) a source of information useful in understanding the function and operation of the subsystem. Specifically, the manual includes the following descriptive, interfacing, and operational information:

- SECTION 1.0, General Description, includes an introduction of the subsystem and provides an overall description of its physical characteristics, principles of operation, performance specifications, and special features.
- SECTION 2.0, Interface, contains information regarding SCSI and the hardware and software interface. This material is essential for normal host-to-subsystem SCSI interfacing.
- SECTION 3.0, Operational Information, includes techniques of cartridge use, a description of operator controls, and identification of cabling and connections.
- SECTION 4.0, Controller Options, explains the available options for the controller, operating principles, interface requirements, and operational impact.
- APPENDIX A, Diagnostic Port Error Codes for the 10/10.5 Megabyte, 8 Inch Disk Storage Subassembly with Extended SCSI, provides error code information for the subsystem.
- APPENDIX B, Interconnect Cable Ordering Information, includes cable information for interfacing with host and power supply.

Reference to IOMEGA or its Alpha-10H/10.5H™ product is not made in the text of this manual to allow the OEM to pass the document, with new cover and foreword, directly to the ultimate end user.

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## 1.0 GENERAL DESCRIPTION

The 10/10.5 megabyte, half height 8 inch disk storage subsystem (Figure 1) is a high capacity, high performance, direct access data storage device using flexible media. The subsystem, with Small Computer System Interface (SCSI), is intended for use with small to medium sized systems requiring on-line storage with removable cartridges of 10/10.5 megabytes each. The subsystem consists of a controller with an intelligent host level interface and up to two disk drives attached daisy-chain style to the controller.

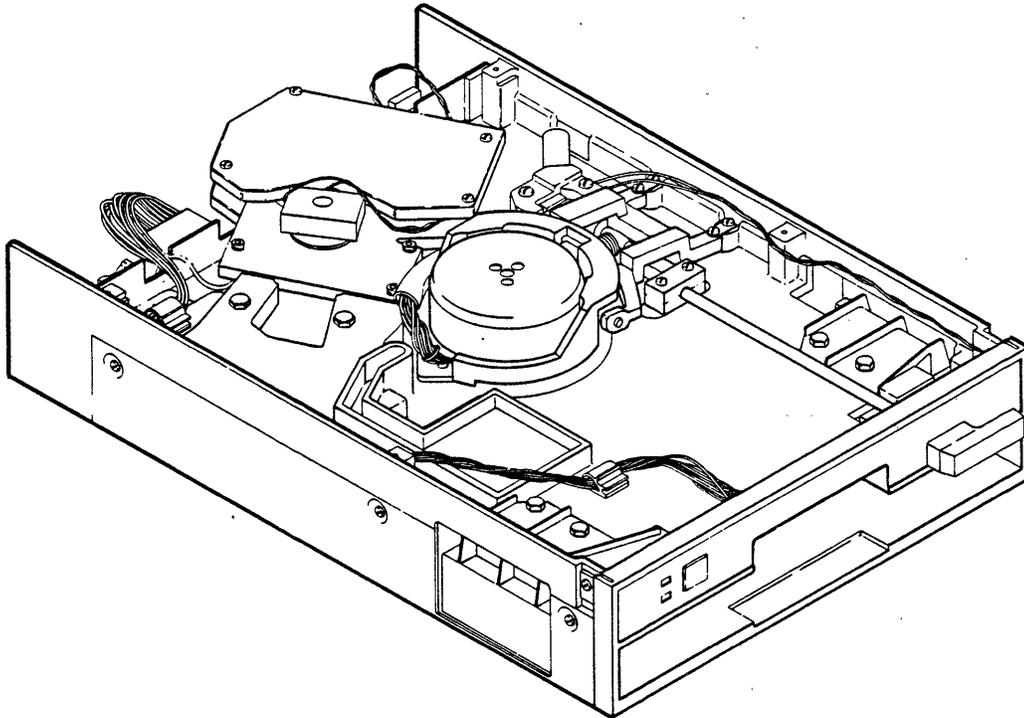


Figure 1. The 10/10.5 Megabyte, Half Height 8 Inch Disk Storage Subsystem

### 1.1 OVERVIEW OF SUBSYSTEM FEATURES

The subsystem incorporates a number of new and innovative technologies that make it a very versatile and adaptable data storage peripheral. The features described in this section include:

#### Drive and Controller

- One or two drives per controller.
- Removable, 10/10.5 megabyte data cartridge.
- Embedded servo control.
- Run length limited code (RLLC) encoding/decoding.
- User transparent error detection and correction (optional).
- Utility commands for sector and track sparing.
- A 1.13 megabyte/sec instantaneous transfer rate.

- Sector interleave capability.
- Data buffering on the controller.
- Logical block addressing.
- Comprehensive user command set.
- Automatic startup diagnostics.
- Automatic idle drive half speed dwell.
- Automatic media life enhancement routines.
- Automatic error recovery procedures.
- High level, intelligent host interface.
- All direct current (dc) power.

#### Data Cartridge

- Hard plastic enclosure for media protection.
- Preformatted media.
- Convenient 8-1/2 X 11 in. size.
- Cartridge write protect switch.
- Maintenance tracks for cartridge-specific information and diagnostics.

A more complete description of subsystem functions and performance characteristics is presented in subsection 1.2.

## 1.2 PHYSICAL/MECHANICAL CHARACTERISTICS

Subsystem function and operation are described in this subsection, as are characteristics of the drive, controller, and cartridge.

### 1.2.1 Function

The subsystem is a high performance disk storage device. Configured with a controller and up to two drives, the subsystem provides removable media storage capability to systems requiring up to a total of 20 megabytes online storage capacity per subsystem. Data cartridges are interchangeable, giving the assurance of drive-to-drive compatibility.

Major functions of the subsystem include disk rotation, head positioning, data transfer, host interfacing, and error identification.

Since these functions are handled by the subsystem controller, once the drive is installed in the system, routine operation is fully automated, requiring operator intervention only for cartridge exchange.

### 1.2.2 Drive Characteristics

The subsystem drive contains all functional mechanical components (base casting, drive motor, Bernoulli plate, head/actuator, and loading mechanism) and some electronic circuitry (read preamplifier write driver and power amplifiers for the head/actuator and drive motor). Figure 2 shows the architectural division of the drive and controller.

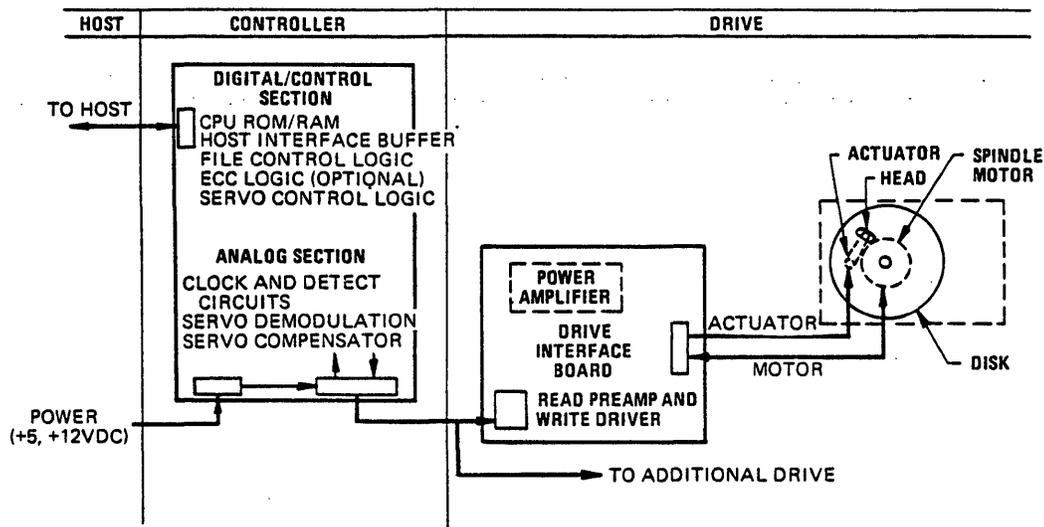


Figure 2. Disk Drive/Controller Architecture

### 1.2.3 Controller Characteristics

The subsystem controller integrates drive analog and digital functions and provides the host with an intelligent, high level interface. The controller consists of a printed circuit board divided between analog and digital functions (see Figure 2).

The controller provides the following important functions.

- Data detection and clocking.
- Servo demodulation.
- Command decode and execution.
- Buffering of data.
- Data serialization/deserialization.
- Data encoding/decoding.
- Subsystem diagnostics.
- Sector interleaving.
- Automatic idle drive half speed dwell.
- Automatic error recovery procedures.
- Automatic error correction (optional, see Section 4.0).
- Arbitration for host interface (optional, see Section 4.0).

## 1.2.4 Cartridge Characteristics

The subsystem cartridge consists of a durable polycarbonate enclosure containing a single flexible disk. The cartridge provides a protected environment for the media and a handy, transportable package for the user. The access door to the media is latched internally and opens upon cartridge insertion into the drive, thus preventing any user contact with the disk itself.

The disk is a 3 mil polyester based substrate having a high energy oxide coating. Disks are preformatted at the factory with servo positioning information, sector and track identifications, and two prewritten diagnostic tracks called the Z-tracks. Raw media defects occurring within sector and track boundaries are flagged when the disks are preformatted and alternate locations are assigned.

A summary of cartridge and media specifications is presented in subsection 1.5 of this manual.

## 1.3 SUBSYSTEM BLOCK DIAGRAMS

The block diagrams shown here represent the 10/10.5 megabyte half height subsystem drive (Figure 3), analog section (Figure 4), and digital/control section (Figure 5). These diagrams are for informational purposes only and should not be used as wiring documents. Explanations of the diagrams are presented in subsection 1.4.

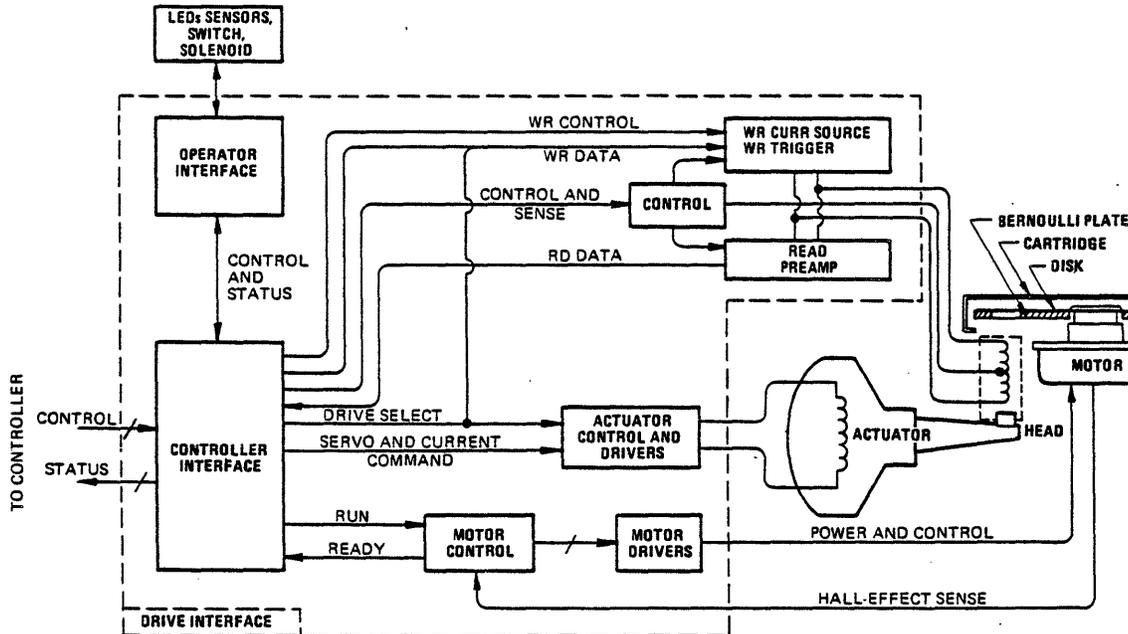


Figure 3. Block Diagram of the Subsystem Drive

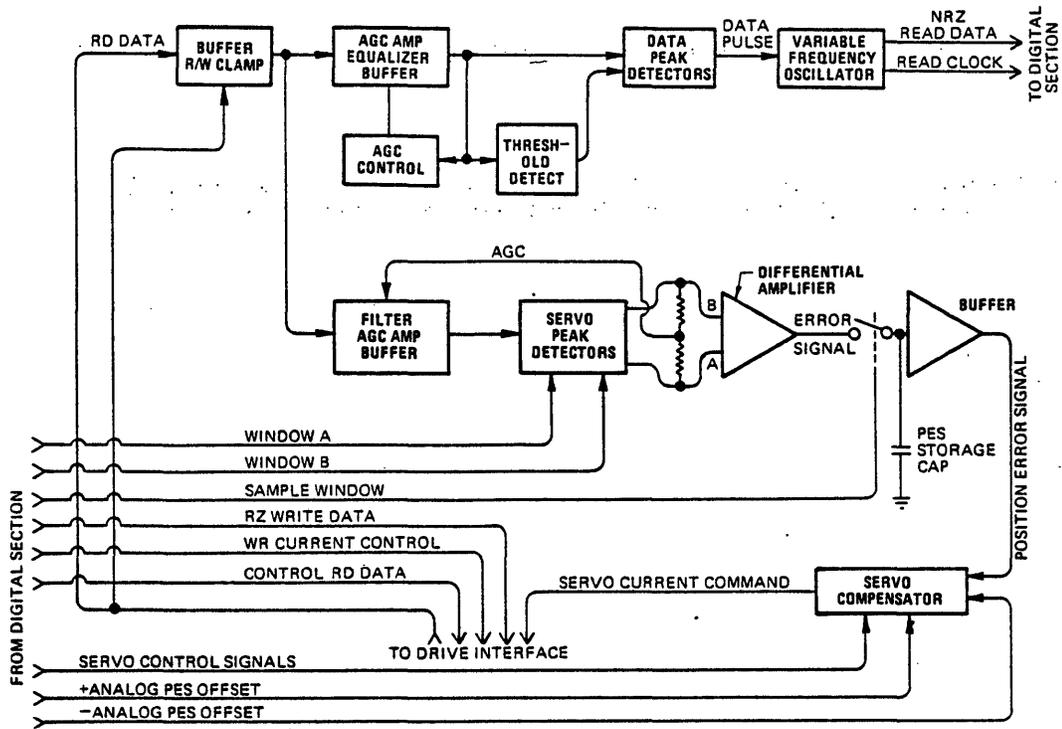


Figure 4. Block Diagram of the Subsystem Analog Functions

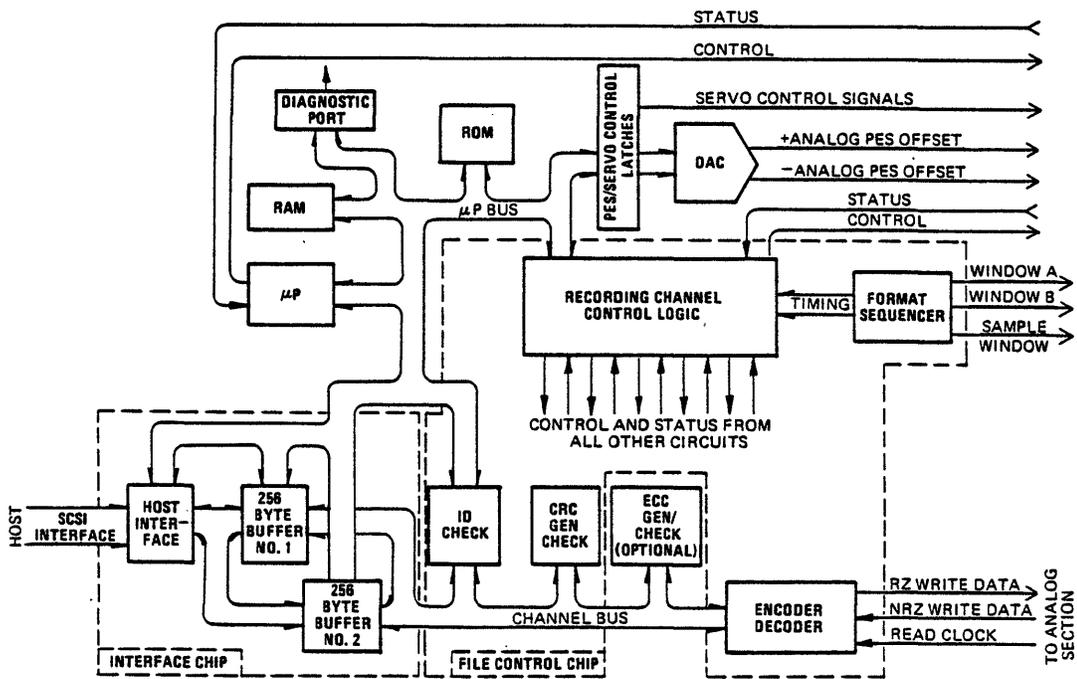


Figure 5. Block Diagram of the Subsystem Digital Functions

## **1.4 PRINCIPLES OF OPERATION**

The subsystem can be broken functionally into three parts: the drive with its associated electronics and the controller board with analog and digital sections. Figures 3 through 5 show the functional segments of these major parts.

### **1.4.1 Drive**

The drive (Figure 3) consists of the Bernoulli plate, spindle motor, read/write head, actuator, drive interface board, and operator controls and indicators. The major drive functions are to provide a constant spindle speed, move the head, preamplify read data, control data writes, and provide operator interface.

When a cartridge is inserted and the load lever is turned clockwise, the spindle motor is engaged and the disk spins up to a constant operating speed. As the disk rotates, it "flies" in close proximity to the Bernoulli plate on a cushion of air. Special coupling techniques allow the read/write head, which penetrates through an opening in the Bernoulli plate, to establish a stable recording environment. Motor control circuitry on the drive interface board senses motor speed and keeps the motor turning at 1,500 rpm. It also signals the controller that the disk is up to speed, flashes the green LED during spinup/spindown, and lights the green LED on the front of the drive when the motor is up to speed.

If the disk is not accessed over a period of time, a timeout occurs and the drive either begins a steady track-to-track seeking action (drive last used) or adjusts the motor to half speed (dual drive configuration only). This prevents the drive from dwelling on one track excessively. The length of time before the motor spins down to half speed can be programmed onto the Z-tracks. When the controller accesses the disk after a timeout, it either causes the motor to spin again to full speed, or initiates a seek to the track corresponding with the logical address requested by the command. Approximately 1 to 2 seconds are needed for the drive to become ready if it is at half speed.

#### **1.4.1.1 Cartridge Format**

Data cartridges are preformatted at the factory with information that divides the user recording surface into 306 data tracks of 64 (10 Mbyte) or 67 (10.5 Mbyte) data sectors. Each track also contains five spare sectors (10 Mbyte) or two spare sectors (10.5 Mbyte) and one error correction code (ECC) sector on each track, making a total of 70 sectors per track. Disk and track formats are shown in Figure 6. The 306 data tracks store the subsystem's 10/10.5 megabytes of data. Four spare tracks are available if any of the normal data tracks become damaged or unreliable. Two identical Z-tracks are present on each disk; one at the inner edge and one at the outer edge (Figure 6). The secondary Z-track becomes a backup in the event the primary Z-track becomes damaged. The Z-tracks are used for recording such cartridge

specific information as sector interleave, dwell timeout length, defective and spare track lists, and error correction status. Some sectors of the Z-tracks are used to record specific data patterns required by the internal self-test of the subsystem, or special customer data. The command for formatting the Z-tracks is presented in subsection 2.3.3.3.4. (Figure 18 in that text describes the format of the Z-tracks.)

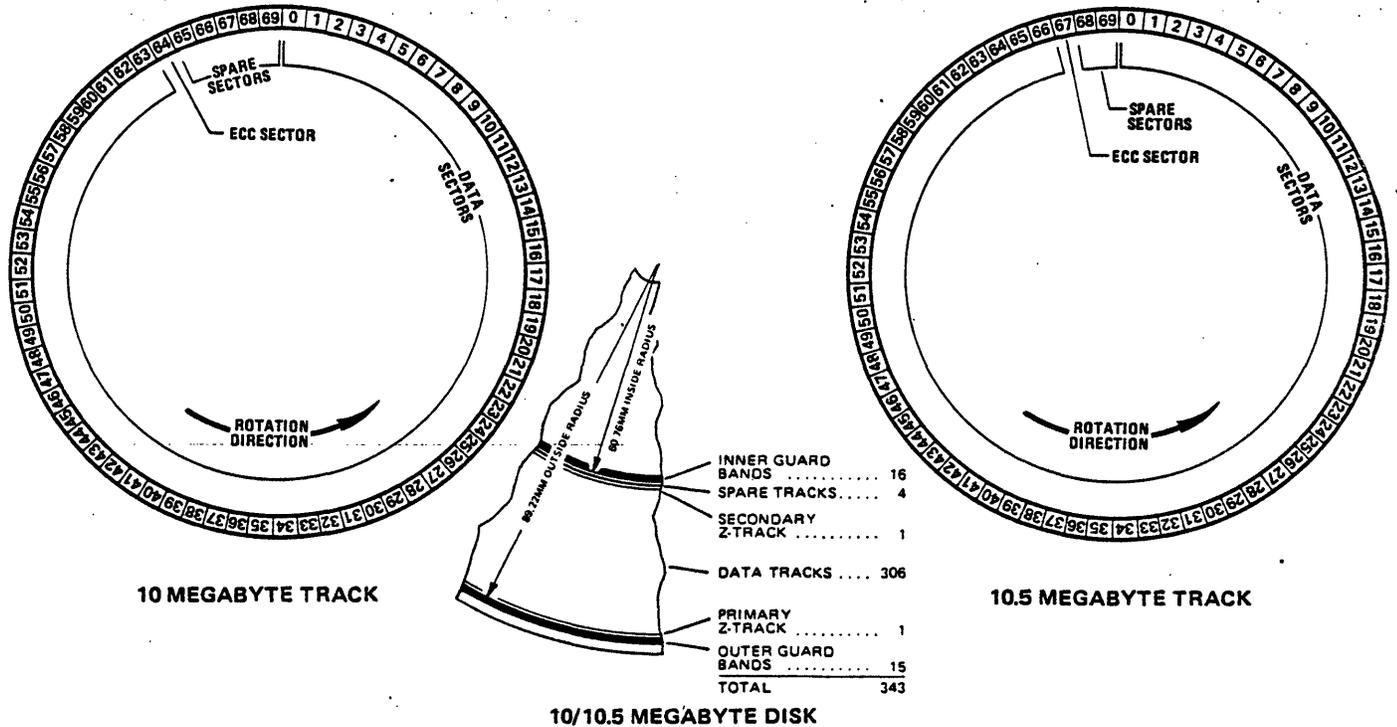


Figure 6. Disk and Track Formats

Each sector on a track is organized as shown in Figure 7. The PAD field provides space for sector overlap (caused by motor speed variations), and allows sufficient recovery time if switching from write to read mode. A uniquely coded sector timing mark identifies the start of a sector. The servo field allows head positioning circuitry on the controller board to keep the head centered on a track. Gaps provide the read circuits with timing information so they can synchronize to the frequency and phase of the data. The sector ID field identifies the sector and track number of each sector. A total of 512 bytes of data can be stored in each sector, 256 bytes per data field (also called a record). The two data fields can be addressed independently.

Sectors may be flagged as defective and reassigned to one of the spare sectors. One sector on each track may be used optionally for storing error correction information. Use of the ECC sectors (optional and specified on the Z-tracks) allows the correction of two complete data records per track (see Section 4.0).

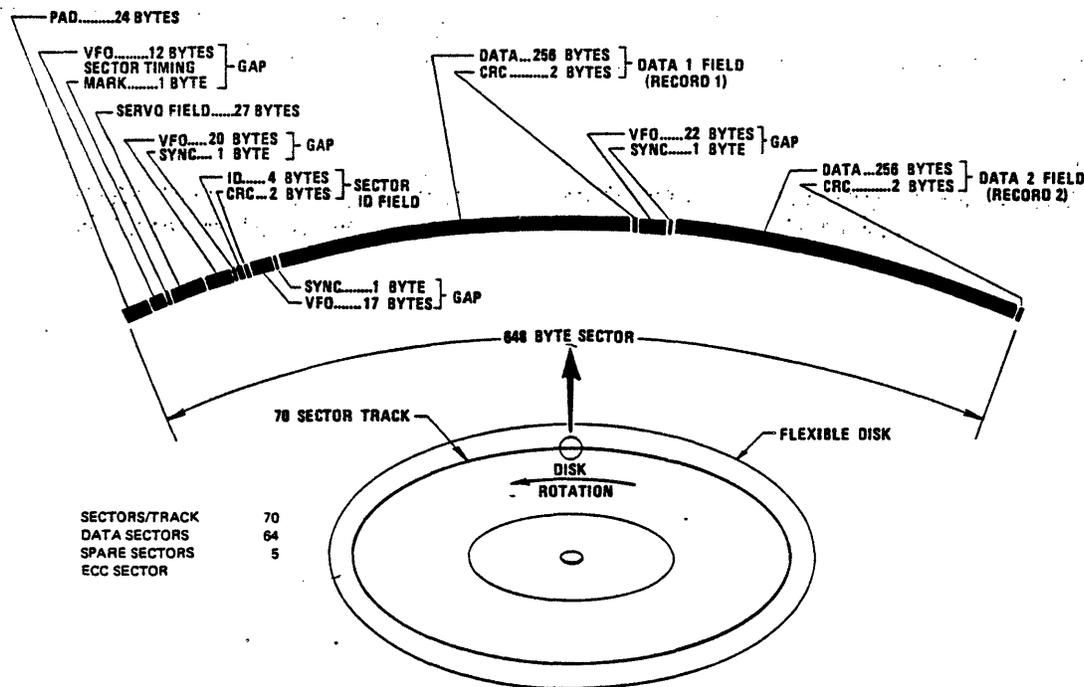


Figure 7. Sector Format

### 1.4.1.2 Drive Interface Board

The purpose of the drive interface board is to: (1) provide the first stage of head output amplification, (2) switch write current to the head, (3) provide motor speed control, (4) service the operator interface, and (5) drive the actuator.

#### 1.4.1.2.1 Preamp Section

The preamp section of the drive interface board is responsible for managing write and read signals traveling to and from the head. During a read function, low level signals from the head are amplified and sent on to the controller board for signal processing. Its close proximity to the head allows the preamplifier to provide primary amplification, thereby reducing the problems of external interference.

#### 1.4.1.2.2 Write Current Driver Section

During a write, write information developed on the controller board is routed to the preamplifier. Circuitry in the preamp section uses the write data signal to switch write current in the head.

On-board control circuitry enables write current only when all software and hardware conditions have been met. When not in the write mode, read circuitry is constantly enabled for the selected drive.

### **1.4.1.2.3 Motor Speed Control Section**

A single-chip microprocessor provides commutation of the motor phases, indication of motor speed within limits, and motor speed control to 1500 rpm. It also controls the latch pin solenoid, which inhibits unloading of the media while the motor is spinning.

### **1.4.1.2.4 Operator Interface Section**

The on-board microprocessor also senses the motor has been loaded, flashes the green LED when the motor is spinning up or down, and polls the console pushbutton (which initiates motor spindown). It also monitors and manipulates control lines that interface with the controller board.

### **1.4.1.2.5 Actuator Driver Section**

Actuator control and driver circuits use the Servo Current Command signal from the controller board to direct current to the actuator.

## **1.4.2 Controller Board**

The controller board is comprised of two areas: the analog section and the digital section.

### **1.4.2.1 Analog Section**

The main purposes of the analog section are to (1) provide a read clock that is synchronous with the frequency and phase of the data coming from the disk, (2) filter and shape the read data, (3) interpret servo information for head positioning, and (4) provide servo loop compensation.

#### **1.4.2.1.1 Read Channel**

Read data signals are buffered and shaped through a series of circuits designed to recover the original written data. Automatic gain control (AGC) and threshold detect circuits are included to compensate for changes in the relative strength of the read signal.

During a read process, the read data lines contain a series of positive and negative peaks that correspond to flux reversals recorded on the disk. After shaping and gain control, the peaks are fed into peak detectors that output uniform pulses for each peak encountered. A variable frequency oscillator (VFO) phase locks to the trailing edge of the pulses, providing a synchronous clock that is used to translate the data pulses into standard nonreturn to zero (NRZ) format. At this point the data bits have not been decoded, but are in a TTL form that can be used easily by the decoder in the digital section.

### 1.4.2.1.2 Servo Error Decoding

Servo information, available on the read data lines at the beginning of each sector, goes through a filter and gain control process similar to the read data.

Normal servo fields are written one-half track offset from data tracks, as shown in Figure 8. When the servo code is read, the relative amplitudes of the A and B field peaks indicate how far the head is from a track center.

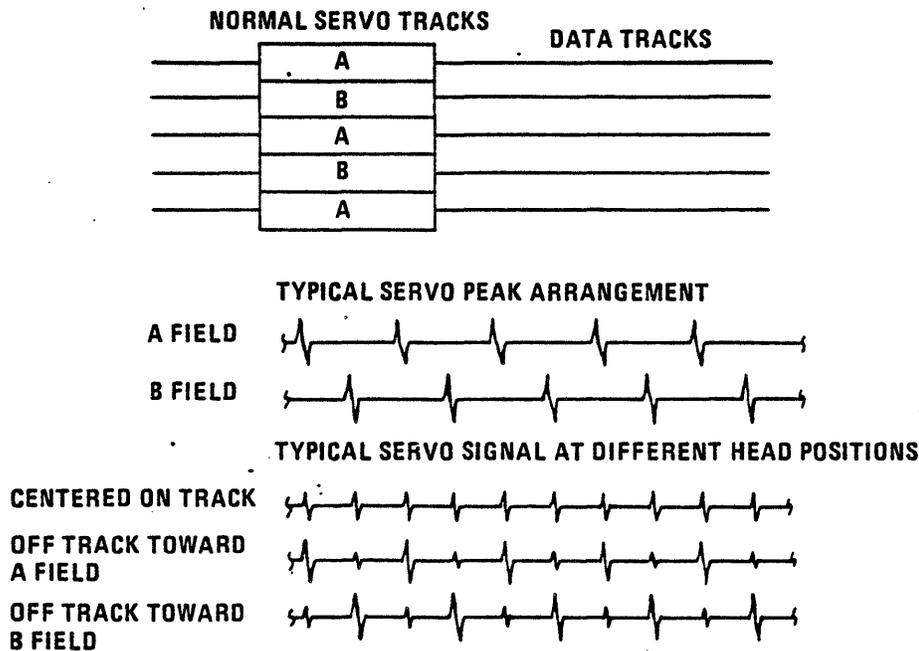


Figure 8. Servo Signals

Servo peak detectors on the controller board check the amplitude of the A and B peaks and send the results to a differential amplifier. The difference between the amplitude of the A and B peaks is an error signal whose amplitude will indicate the amount and direction off track. Window generation circuitry ensures that the peak detectors are turned on at the right time. This position error signal (PES) acts as an input to the compensator network, which adjusts the head position to obtain minimum positional error.

If the PES exceeds predefined limits, an error is reported to the digital section of the controller board.

### 1.4.2.2 Digital Section

The digital section of the controller performs the functions of format sequencing, data encoding and decoding, servo control for seek and track following, error detection, and host interfacing. Two major buses serve the digital controller: the microprocessor bus, which contains data for the microprocessor; and the channel bus, which carries data during reads or writes.

The digital controller uses two custom metal oxide semiconductor (MOS) chips (one for file control and one for host interface) as well as a Z80A microprocessor. The functions associated with these three major components are explained in this subsection.

#### **1.4.2.2.1 Microprocessor Circuitry**

The microprocessor circuitry is composed of a Z80-A microprocessor, read only memory (ROM), random access memory (RAM), and I/O ports. This circuitry monitors the drive status lines and controls drive initialization via the microprocessor. The microprocessor also monitors bit switches that indicate field programmable options, controls the idle drive half speed feature, and outputs status information to the diagnostic port.

The microprocessor monitors the host interface, recognizes a selection, accepts and decodes command and parameter bytes, schedules and controls command execution, and returns ending status to the host. Any errors encountered along the way are flagged to the host and specific error information is stored, available to the host via a REQUEST SENSE command.

#### **1.4.2.2.2 Servo Control**

To initiate a seek operation, the microprocessor introduces position error information and current offsets into the track following servo loop, which causes the head to move off track. By controlling the amount and timing of the offsets, the processor can control the acceleration, velocity, and position of the head.

#### **1.4.2.2.3 Interface Circuitry**

The host-to-controller interface is centered around a custom LSI chip that includes two 256 byte FIFO buffers. These buffers are controlled in a flip-flop mode so that data can be accepted from the disk simultaneously with data transmitted to the host.

Each transfer between controller and host is accompanied by a REQUEST-ACKNOWLEDGE (REQ-ACK) handshake. The microprocessor manipulates the handshake during the command and status phase. During the data phase of READ or WRITE commands, the microprocessor enables a hardware transfer mechanism that allows high speed transfers. A detailed explanation and description of the host interface is presented in Section 2.0 of this manual.

#### **1.4.2.2.4 File Control Circuitry**

The file control circuitry is centered around a custom MOS chip that: encodes and decodes, serializes and deserializes, generates and checks CRC, compares track and sector IDs, maintains synchronization with the disk, manipulates signals according to commands received from the microprocessor, and gathers and reports error status.

The subsystem uses a run length limited code that allows data to be tightly packed on the disk. The encoder/decoder translates data received from the host to the code and format required by the controller. It also detects special marks on the disk that allow bit and byte synchronization.

Each ID and data area on the disk is followed by a CRC field for error detection purposes. The CRC bytes, generated as the data bits are written to the disk, are appended to the data. As the data bits are read to the controller, the data and CRC are logically manipulated to check for errors. If an error is detected, the incorrect data will not be transferred to the host, but retries will be attempted to execute the command correctly. Six retries will be attempted in normal operation before error status is sent to the host. Optional ECC circuitry also may be invoked (see Section 4.0).

Before any read or write operation, the ID of the sector under the head is compared with that of the target sector. This function ensures that no customer data will be accidentally overwritten or mistaken for desired data.

A unique mark is written at several places in each sector on the disk. Detection of these marks enables the file control format sequencer to maintain synchronization with the disk. This sequencer in turn manipulates control signals required by the analog controller board.

At the beginning of each sector, an operation register is loaded by the microprocessor. This information is used in conjunction with the format timing to (1) enable write gates, (2) set bus directions, and (3) select the encoder or decoder. As errors occur, they are latched for later retrieval by the microprocessor. Serious errors will cause the operation to abort.

### **1.4.3 Interleaving and Error Correction Code**

A number of important factors control the performance of the subsystem. Some of these are data transfer rate, latency, interleaving, and the error correction option. Interleaving and how it affects system performance is described in this subsection. See Section 4.0 for ECC impacts.

#### **1.4.3.1 Interleaving**

Maximum data transfer rate of the subsystem is 1.13 megabytes/second. However, the actual rate achieved by the host system is a function of the host hardware and software plus the interleave selected. Poor choice in the interleave selection can dramatically degrade performance. Interleaving does not affect the performance of single sector or single record transfers nearly as much as does latency, but for multi-sector bursts, interleaving determines how quickly the drive will be ready to transfer the next block of data.

Interleaving is a system designed to achieve the highest possible performance when working with host systems that cannot transfer data as rapidly as the maximum transfer rate of the disk subsystem. During a data read, for

example, if the host could transfer data at 250,000 bytes/sec, the drive, with its two 256 byte buffers, would read 512 bytes of data, and before the host had emptied one of the buffers, would be ready to read the next sector. Having no place to put the data from this next sector, the disk then would have to complete a full revolution (40 msec) before the data could be transferred. Under these conditions, the effective data transfer rate would be only 12,800 bytes/sec.

Interleaving can minimize such loss in performance by leaving gaps between logically (not physically) adjacent sectors. These gaps increase performance by allowing additional time for the host to transfer data before the buffer is needed again. An interleave factor of 1 (no interleaving) means that the logical sectors are physically next to each other on the disk. A factor of 2 will leave one sector between logically adjacent sectors. The interleave factor specifies the number of sectors from one logical sector to the next.

This interleaving system does not waste disk space; it is a system of numbering the sectors to optimize performance. Any sectors used as gaps during one revolution will be used as data sectors during some subsequent revolution (see Figure 9).

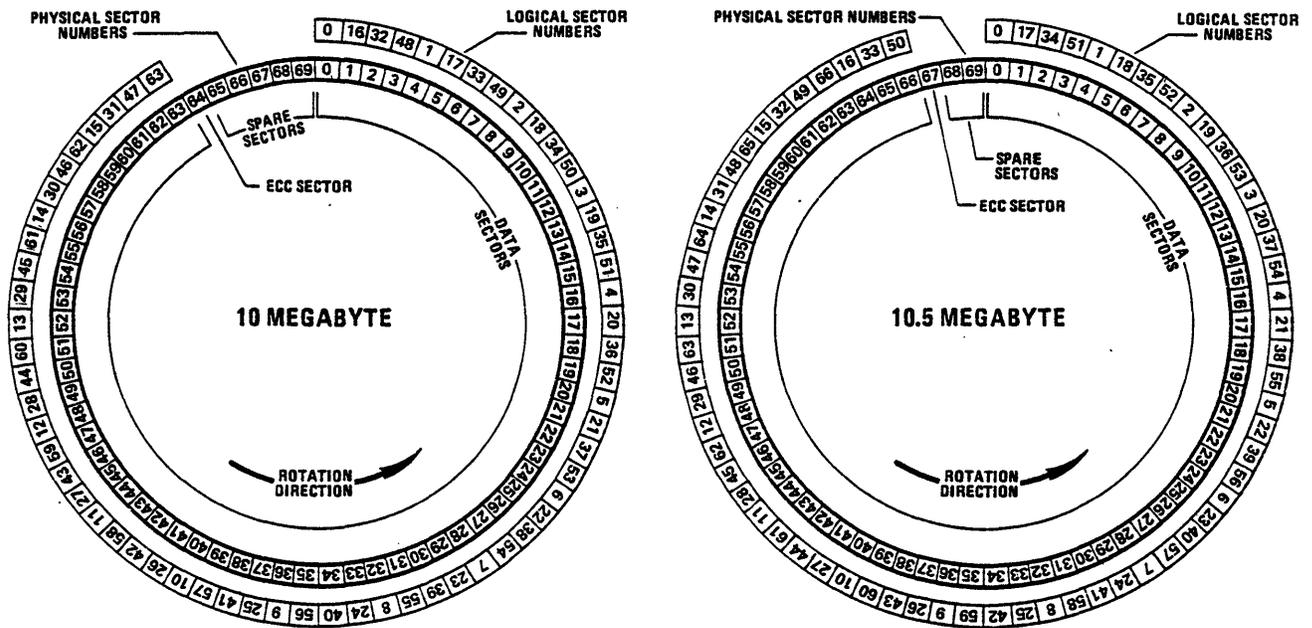


Figure 9. Example of Interleave 4

The importance of selecting the correct interleave factor for the application cannot be overemphasized. The following listing shows the available interleave factors and the data rate required for each. Select the lowest possible interleave value with a data rate equal to or less than that of the host system.

Interleave Factor		Sector-to-Sector Interval	Minimum Data Transfer Rate (bytes/sec)
10 Mbyte	10.5 Mbyte		
1	1	571 microsec	896,000
2	2	1.14 msec	448,000
4	4	2.29 msec	224,000
8	-	4.57 msec	112,000
16	-	9.14 msec	56,000
-	17	9.71 msec	52,700
32	-	18.3 msec	28,000
-	34	19.4 msec	26,350

The values shown are for multi-sector transfers without track crossings.

Interleave also can be used if the transfers are not multi-sectored. Each command sequence requires approximately 3 msec to transfer and decode before the drive begins seeking to the desired sector. This 3 msec transfer time allows six sectors to pass under the read/write head. Sequential single sector transfers can be optimized if this is taken into account. Also, a seek from one track to the next takes about 10 msec, or 18 sectors, to complete. For this reason, sectors are skewed 18 apart between tracks, providing maximum efficiency when crossing track boundaries.

### 1.4.3.2 Error Correction Code

The subsystem will support two levels of error correction options: post-write CRC checking and error correction code (ECC). All controller boards support post-write CRC checking, but ECC will be available only on boards populated with a special custom chip. Controllers with the ECC option will read or write to any cartridge, correctly observing the ECC status bits (enabled or disabled) on that cartridge. Controllers without the option will read and write to cartridges with ECC disabled, and will read cartridges with ECC enabled but will reject write commands since it has no capability to update ECC information. To allow write commands, a format of the Z-track must be invoked, setting the ECC status bit to disabled.

Post-write CRC causes the subsystem to verify data on the disk after write. This verification ensures that the write operation was successful while the host still has the data available, in case any retries are required. After a command has been completed, or whenever the transfer must continue on the next track (whichever comes first), the drive verifies that all the sectors written on the track during this command are readable. The overhead for this operation is one additional revolution, or 40 msec. This overhead can be substantial for multiple single sector transfers on the same track.

## 1.5 SUBSYSTEM SPECIFICATIONS

Capacity, performance, reliability, environment, power, physical, organization, and recording specifications for the subsystem are presented in this subsection. An unused cartridge from the factory can operate in either a 10 Mbyte or 10.5 Mbyte subsystem. However, once files have been written on it in either of these subsystems, a cartridge cannot be used in the other subsystem without loss of user data. In addition, a cartridge must have a minimum of 67 good sectors on 306 tracks to support the 10.5 megabyte capacity requirements.

### 1.5.1 Capacity

- User Available (Formatted) Capacity, Bytes Per:

	<u>10 Mbyte</u>	<u>10.5 Mbyte</u>
Drive	10,027,008	10,497,024
Cartridge	10,027,008	10,497,024
Surface	10,027,008	10,497,024
Track	32,768	34,304
Sector	512	512
Record	256	256

- Bytes Per Formatted Cartridge

User Available	10,027,008	10,497,004
Overhead	3,155,280	3,155,280
Spares Available for Media Flagging	924,672	454,656
Total	<u>14,106,960</u>	<u>14,106,960</u>

### 1.5.2 Performance

- Data Transfer Rate
  - Drive to Controller 1.13 Mbytes/sec
  - Controller to Host
  - Single Record Burst (256 bytes) 1.13 Mbytes/sec
  - Continuous Records (same track) 896 Kbytes/sec
- Seek Time (including settling time)
  - Minimum 10 msec
  - Average 35 msec
  - Maximum 75 msec
- Latency (average rotational delay) 20 msec
  - Spindle Speed 1,500 rpm  $\pm 0.5\%$
- Track to Track Access Time (consecutive records over track boundary) 10.3 msec
- Start/Stop Time (average) 5/5 sec

### 1.5.3 Reliability

- Error Rates
  - Data Recoverable 1 in  $10^{10}$  bits
  - Nonrecoverable 1 in  $10^{12}$  bits
  - Seek 1 in  $10^6$  seeks
- Mean Time Between Failures
  - Drive 15,000 hr
  - Subsystem (Drive and Controller) 8,000 hr
- Mean Time To Repair 0.5 hr
- Service Life 5 yr
- Cartridge Insertion/Removal Cycles 5,000 min

### 1.5.4 Environment

- Operating:
  - Temperature 10° to 46°C, 50° to 115°F
  - Relative Humidity (Noncondensing) 10 to 80%
  - Maximum Wet Bulb 26.6°C, 80°F
  - Maximum Temperature Gradient 12°C/hr, 22°F/hr
  - Altitude To 3048 m 10,000 ft
  - Shock\* 3 g for 20 msec
  - Vibration\* 0.85 g at 5-17 Hz  
0.25 g at 17-500 Hz

Air Cleanliness	Particle Size (micron)	Particles/m <sup>3</sup>
	<1.0	4 X 10 <sup>7</sup>
	<1.5	4 X 10 <sup>6</sup>
	<5.0	4 X 10 <sup>5</sup>

● Storage and Shipping	Storage (6 mo)	Shipping (96 hr)
Temperature		
Drive and Controller	-22° to 52°C -8° to 126°F	-40° to 60°C -40° to 140°F
Cartridge	10° to 52°C 50° to 126°F	-40° to 52°C -40° to 126°F

\*Each specified shock and vibration level is applied separately to each of the three mutually perpendicular planes of the drive; one of the planes being defined as the top, front, and side.

Relative Humidity (noncondensing)	10 to 90 %
Shock* (four drops)	40 g for 15 msec
Vibration*	1.3 g at 5-27 Hz 2 g at 27-60 Hz 5 g at 60-500 Hz

### 1.5.5 Power

- Voltage (see subsection 2.4, Table 1 for details).

<u>Voltage</u>	<u>Max Current (amps)</u>	
	<u>Continuous</u>	<u>Instantaneous</u>
5 ±5%	1.5 amps with 30 mv rms ripple max	1.5 amps peak with 120 mv p-p ripple max
12 ±5%	1.5 amps with 60 mv rms ripple max	3 amps peak, 25% duty cycle 300 mv p-p ripple max

- Power (max continuous power consumption in watts)

First Drive with Controller	25 watts
Additional Drive	10 watts

### 1.5.6 Physical

#### Dimensions

● Drive**		
Height	59.00 mm	2.32 in.
Width	217.00 mm	8.54 in.
Depth	305.00 mm	12.01 in.
● Front Panel Including Load Lever		
Height	59.00 mm	2.32 in.
Width	217.00 mm	8.54 in.
Depth	27.02 mm	1.06 in.

\*Each specified shock and vibration level is applied separately to each of the three mutually perpendicular planes of the drive; the planes being defined as the top, front, and side.

\*\*Without front panel and with or without controller.

● Cartridge		
Height	18.00 mm	0.71 in.
Width	209.00 mm	8.23 in.
Depth	280.00 mm	11.02 in.

● Flexible Disk	<u>Diameter</u>	<u>Thickness</u>
	198.0 mm	0.08 mm
	7.8 in.	0.003 in.

**Weights**

● Drive with Controller	2.95 kg	7.9 lb
● Drive without Controller	2.35 kg	6.3 lb
● Cartridge	0.59 kg	1.3 lb

The controller board is mounted completely within the drive casting. Thus, the dimensions shown below relate to a drive with or without a controller. Physical dimensions of the drive box, including the location and size of its mounting holes (Figure 10), conform to those of the industry standard diskette drive. The box can be mounted in any of the following positions.

- Vertically (on either side)
- Horizontally (load lever at right)

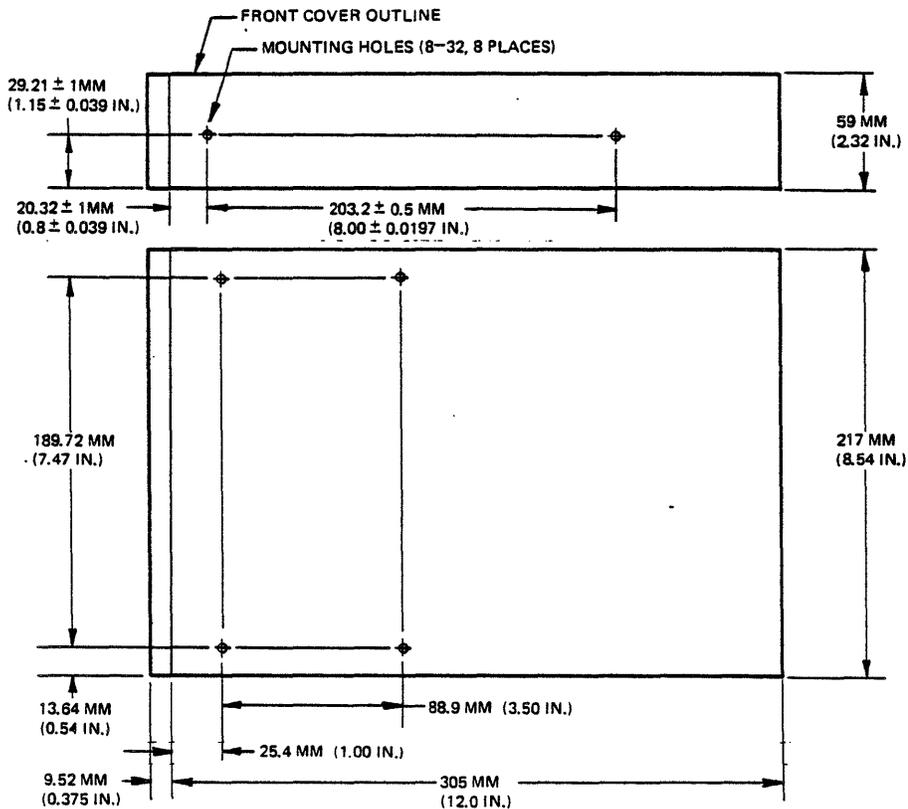


Figure 10. Drive Mounting Hole Locations

## 1.5.7 Organization

	<u>10 Mbyte</u>	<u>10.5 Mbyte</u>
● Configuration		
Drives per Controller	1 or 2	1 or 2
Cartridges per Drive	1	1
Recording Surfaces per Flexible Disk	1	1
Formatted (user available) Tracks per Surface	306	306
Formatted (user available) Sectors per Track	64	67
Records per Sector	2	2
Bytes per Record	256	256
● Formats		
Surface (No. tracks)		
Outer Guard Bands	15	15
Data	306	306
Z-Tracks	2	2
Spares, for Field Flagging	4	4
Inner Guard Bands	<u>16</u>	<u>16</u>
Total	343	343
Tracks (No. sectors)		
Data	64	67
ECC	1	1
Spares, for Factory and Field Flagging	<u>5</u>	<u>2</u>
Total	70	70
Sector (No. bytes)		
Data (2 Records of 256 bytes each)	512	512
Servo	27	27
CRC	6	6
ID	4	4
VFO, Timing Mark, Sync, and PAD	<u>99</u>	<u>99</u>
Total	648	648

## 1.5.8 Recording

● Encoding Method	RLLC
● Recording Density	24,000 bpi
● Flux Density	18,000 fci
● Track Density	300 tpi
● Areal Density	7.2 Mbits/in. <sup>2</sup>

## **2.0 INTERFACE**

The host interface used in the 10/10.5 megabyte disk storage subsystem is the extended version of the Small Computer System Interface (SCSI). General information about this interface and device-specific information about the implementation of the SCSI bus on this device are presented in this section.

### **2.1 SMALL COMPUTER SYSTEM INTERFACE (SCSI)**

The term SCSI is used to denote the American National Standards Institute (ANSI) Small Computer System Interface. A proposed SCSI standard is being evaluated by American National Standards Committee (ANSC) X3T9.2 to provide for efficient asynchronous communication between computers and peripheral input/output devices. Because of the developmental status of the SCSI standard, some variances might become evident later between it and the material presented in this manual.

The SCSI bus is oriented to intelligent peripheral devices. During typical operations across the bus, the peripheral devices take over bus control (at the request of the host Central Processing Unit) and monitor the successful completion of the operations. Because of this orientation and the versatility of the SCSI bus structure, a host CPU can communicate with a wide variety of peripherals by adding a single adapter to the interface between the host and the SCSI bus (Figure 11). Standardization of software command set structure makes the task even easier.

Up to eight devices can be connected to the SCSI bus at a time. Each device can have one SCSI bus port. Communication is allowed between a maximum of two ports at a time, all other ports being inactive.

Because of the wide range of devices that can use the SCSI bus, small differences in implementation may be expected from device to device. All true SCSI devices should support most of the SCSI hardware protocol and standard command set, however. If the device-specific implementations are fully documented, overcoming the differences should not be difficult.

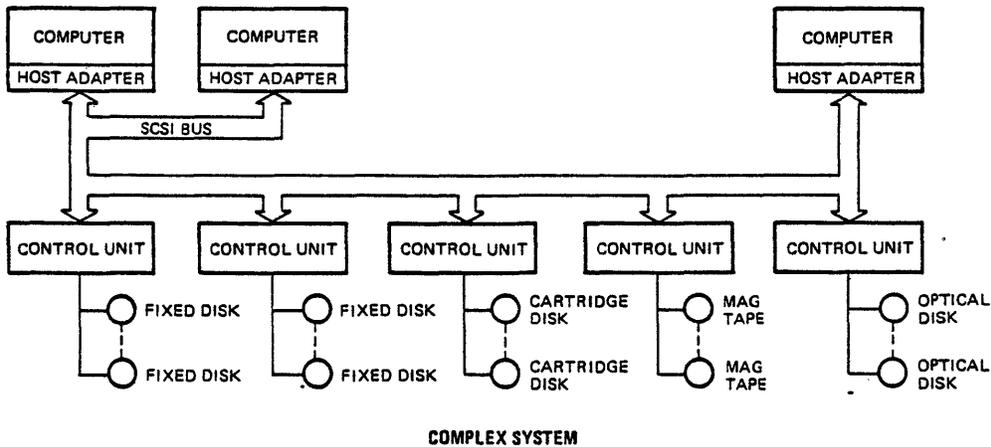
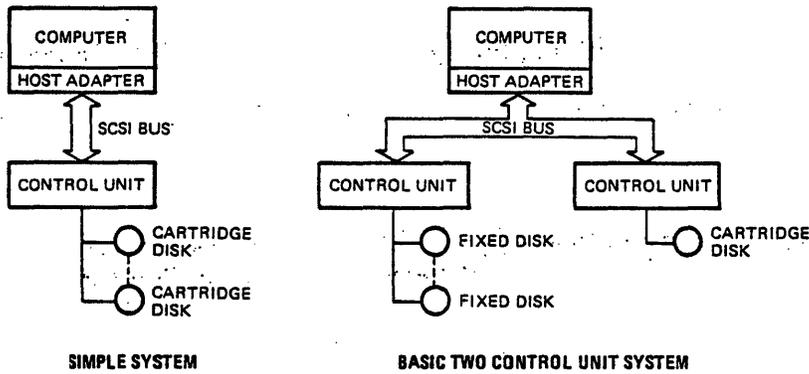
Additional information about the SCSI proposal is presented in the ANSC X3T9.2 documentation.

### **2.2 HARDWARE INTERFACE**

The SCSI hardware interface as implemented in the 10/10.5 megabyte disk subsystem is described in this subsection. The bus lines and theory of communication across the bus also are described.

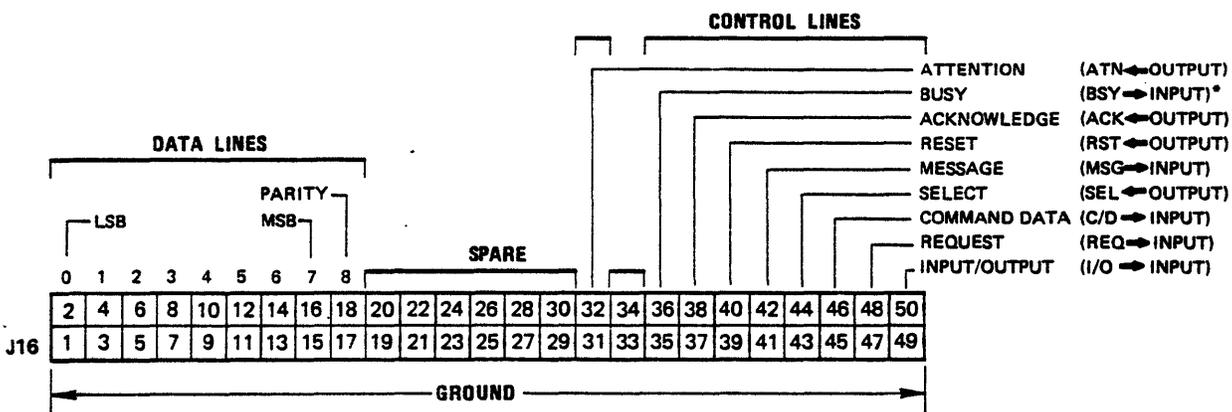
#### **2.2.1 Bus Lines**

The SCSI bus contains nine control lines and nine data lines (including parity). One control line (ATTENTION) is used only if the ECC/Arbitration Option is populated (see Section 4.0). The following signals are interfaced via connector J1. Figure 12 shows the pinouts.



UP TO EIGHT SCSI DEVICES CAN BE SUPPORTED BY THE SCSI BUS. THE DEVICES CAN BE ANY COMBINATION OF HOST CPUs AND INTELLIGENT CONTROLLERS.

Figure 11. Sample SCSI Configurations



\*Signals from host reference.

Figure 12. J1 Host Interface Connector Pinout

ATTENTION (ATN) assertion by the host of this signal indicates that the host wants to send a message to the controller. The controller will recognize the assertion of this control line only if the ECC/Arbitration option is installed (see Section 4.0).

BUSY (BSY) assertion by the controller indicates the controller is using the host interface.

ACKNOWLEDGE (ACK) assertion by the host of this handshake signal indicates each data byte on the bus has been either received by the host (read operation) or is ready to be received by the controller (write operation).

RESET (RST) assertion by the host for a minimum of 1  $\mu$ sec causes all operations in the controller to cease. If asserted during a write operation, the record being written at the time is not guaranteed to be correct and the ECC sector will not be updated. The reset line must be deasserted if further commands are to be issued.

MESSAGE (MSG) assertion by the controller indicates that valid status has been transmitted and the current selection is about to be terminated. This signal is accompanied by a REQ-ACK handshake, but the data signals on the bus have no significance. When the handshake is complete, the controller will deassert all control lines and return to an idle, bus-free state.

SELECT (SEL) assertion by the host along with the controller address bit on the data bus causes the desired controller to be selected. The line must be deasserted when the controller responds with BSY.

COMMAND DATA (C/D) assertion by the controller indicates that command or status information is on the bus. Deassertion indicates the presence of data on the bus.

REQUEST (REQ) assertion by the controller on a host-to-controller transfer indicates that the controller is ready to receive data and the deassertion indicates receipt of data. For a controller-to-host transfer, assertion indicates the presence of data on the bus.

INPUT/OUTPUT (I/O) assertion by the controller indicates data transfer from controller to host; deassertion indicates transfer of information from host to controller.

DATA (0-7) signals are bidirectional data lines used to transfer eight bit parallel data to/from the host adaptor. Bit 7 is the most significant bit.

PARITY is asserted to maintain odd parity on all data and status transfers to the host. The subsystem controller will test for odd parity on all command and data transfers to the controller unless the parity option is disabled. Parity will be generated in this instance by the controller but will not be checked.

## 2.2.2 Host Interface Protocol

The host communicates with the disk subsystem under certain rules of protocol and timing. Modes of operation are illustrated by the following communication transfers.

1. Selection
2. Command Transfer
3. Data Transfer
4. Ending Status Transfer
5. Busy Status Transfer
6. Abort

These modes of operation are described in following subsections of this manual.

The 10/10.5 megabyte disk storage subsystem does not respond to arbitration or reselection as described in the proposed ANSI SCSI standard unless the ECC/Arbitration option has been installed (see Section 4.0). Arbitration is a means of allowing more than one device to initiate operations on the bus, and assigning each such device a priority for cases when more than one device wants to initiate operations at any one time. Arbitration may be carried out by other devices on the bus.

Reselection allows a peripheral to reconnect to a host if the peripheral has disconnected itself (releasing the bus) for some reason before the operation is complete. The subsystem does not support reselection unless the ECC/Arbitration option has been installed (see Section 4.0).

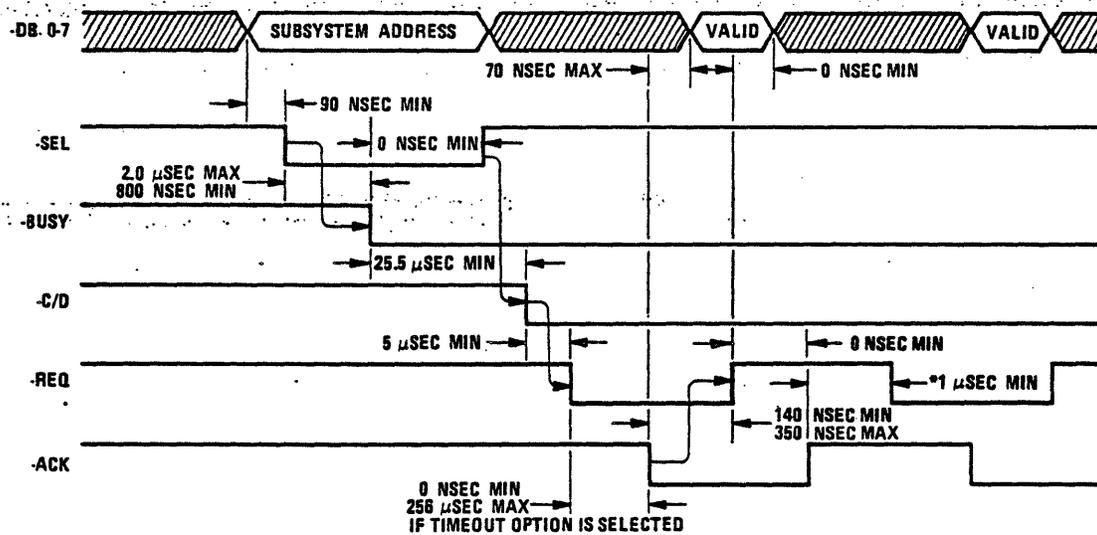
### 2.2.2.1 Selection Sequence

The controller first must be selected to initiate an operation. This is accomplished with a selection sequence (Figure 13).

First, the subsystem address must be placed on the data bus. This address is a 1 of 8 decode corresponding to the shunt position of the controller card. In a subsystem having multiple controllers, each controller would have a different address. If multiple hosts are attached to the interface, BUSY must be tested to see if the bus is available.

After assertion of the subsystem address, SEL is asserted.

The controller polls the select line and the bus. When the data line corresponding to the controller address jumper (preset at factory to bit 0) is asserted, BUSY is deasserted, and SEL is activated, the controller will issue BUSY. The only exceptions are at power on or following a hardware reset. Until certain confidence tests are performed (approximately 1 second in length), the controller will not respond to a selection sequence (see Startup Diagnostics, subsection 3.3).



NOTE: THE CONTROLLER CAN BE RESET AND CLEARED BY PULSING THE RESET LINE LOW FOR A MINIMUM OF 1 μSEC.

Figure 13. Select and Command Sequence Timing

After BSY has been asserted, the host must deassert SEL and the data bit. No further controller activity will occur until the SEL line has been deasserted. Throughout this sequence, I/O and C/D lines will remain deasserted.

### 2.2.2.2 Command Transfer Sequence

When BSY is asserted and SEL is deasserted, the controller asserts C/D and then REQ to prepare for receipt of the command byte. The host then places the command byte on the data bus and asserts ACK. When ACK is asserted, the controller samples the data bus, deasserts REQ, and decodes the command class. The processor then requests the appropriate number of parameter bytes for that type of command using the same REQ-ACK handshake.

If the command or parameter bytes are invalid, an abort sequence will be initiated.

### 2.2.2.3 Data Transfer Sequence

After the command sequence is completed, the controller will react in one or more of the following ways.

1. Seek
2. Start accepting data from the host (write operation).
3. Start transferring data to the host (read/status operation).
4. Return ending status.

If the command involves a data transfer, the controller deasserts C/D. For a read, the I/O line is asserted, and the interface hardware takes over to control the data transfer (Figure 14). Note that bytes passed for REQUEST SENSE, FORMAT UNIT, or similar commands are passed during the data phase, and are considered parameters.

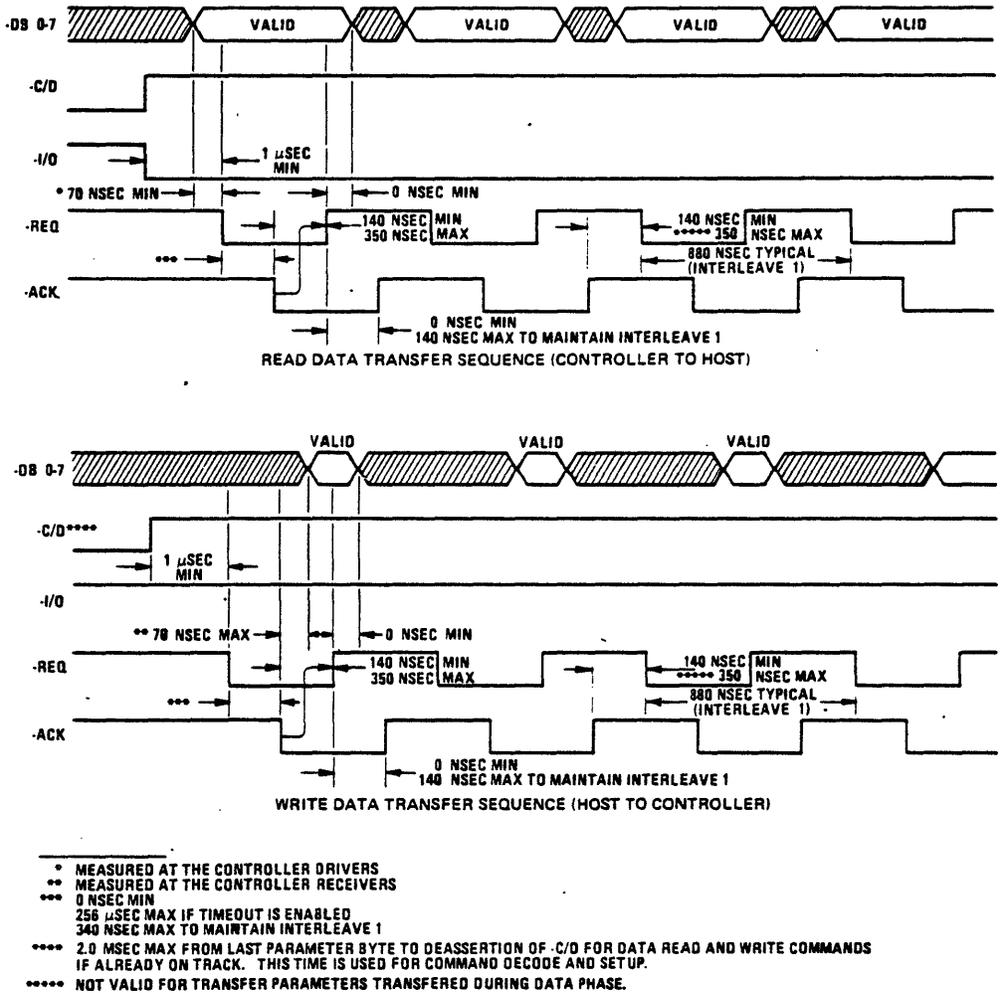


Figure 14. Data Transfer Sequence Timing

For a write operation, the hardware asserts REQ and the handshake continues until the entire record or records are transferred. By the overlapped use of the two 256 byte buffers, full instantaneous data rates of 1.13 Mbytes/sec may be sustained.

For read operation the hardware waits until the FIFO buffer has 256 bytes of data from the disk. It then begins the high-speed data transfer by asserting REQ. The REQ-ACK handshake continues until the read operation is completed.

## 2.2.2.4 Ending Status Transfer Sequence

After a command execution, the controller initiates an ending status sequence (Figure 15). The controller begins this sequence by asserting C/D and I/O. It then places the status byte on the interface bus and asserts REQ. REQ will stay asserted until ACK is received. The controller then will deassert REQ and the host must deassert ACK.

Following transfer of the status byte, an ending byte is transferred to indicate that the operation is complete. With C/D and I/O still being asserted MSG assertion is added. The ending byte is placed on the interface bus and REQ is asserted. REQ will stay asserted until ACK is received. All controller interface lines will be deasserted following transfer of the ending byte. The controller then will return to a polling mode and await the next transaction.

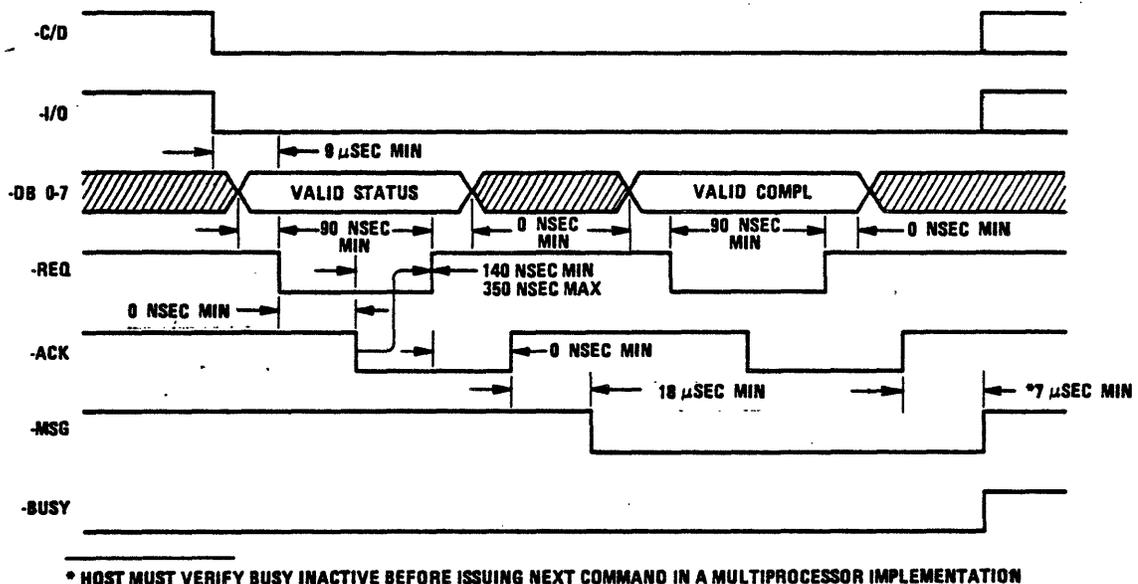


Figure 15. Ending Status Transfer Timing

Ending status byte information is decoded in the following way.

- Bit 0 = Parity error
  - 0 = No error
  - 1 = Parity error in command or parameter transfer from host
  
- Bit 1 = Completion status
  - 0 = Normal completion
  - 1 = Error occurred in command execution
  
- Bit 2 = 0

Bit 3 = Busy status  
 0 = Normal status  
 1 = Hardware busy (e.g., embedded seek)

Bit 4 = 0

Bits 5-6 = Drive number

Bit 7 = 0

### 2.2.2.5 Busy Status Transfer Sequence

At times the controller will be too busy to honor commands from the host. Some examples of this condition are when the controller is undergoing initial bringup, drive checkout, or an off-line seek. At such times, if a command is issued by the host, the controller will assert C/D, I/O, and REQ instead of accepting the command. This indicates to the host system that the controller is sending status. The status byte will reflect the busy condition (bit 3 set). After the ACK handshake, MSG, C/D, I/O, and REQ will be asserted. This is the normal command completion sequence. After the ACK, all control lines will become deasserted. This sequence will repeat until the controller is free to accept commands. At this time normal command transfer sequences will begin.

Since the busy sequence may be handled differently (internal to the hardware) the timings may be somewhat faster than a normal selection (see Figure 16).

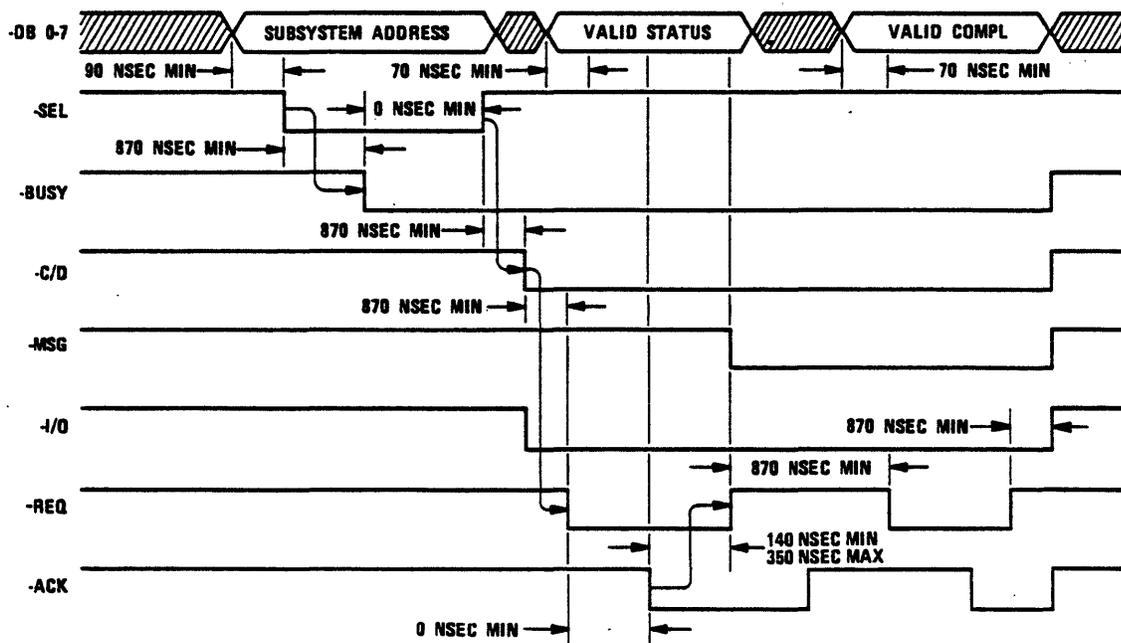


Figure 16. Hardware Busy Status Transfer Timing

### 2.2.2.6 Abort Sequence

The following conditions will cause the controller to initiate an abort sequence.

1. Receiving an invalid command byte.
2. Receiving parameter bytes that are out of the specified range.
3. Receiving a write command of any kind for a cartridge that is write protected.
4. Improper execution or completion of any data operation.
5. Parity error on the host bus.
6. Motor spinup or spindown (BUSY STATUS)

When any of these conditions occur, the controller will assert I/O and C/D immediately and execute an Ending Status Transfer Sequence (see subsection 2.2.2.4 for detail). The status byte gives information regarding the condition that precipitated the abort sequence. The controller then will return to a polling mode and await the next transaction.

### 2.2.3 Reset Condition

The reset condition of the SCSI bus is reached by dropping the reset line low for at least 1 microsec. The 10/10.5 megabyte disk storage subsystem will not create a reset, but will respond to one.

Upon a reset, the controller will deassert all bus lines and allow the bus to go into a bus-free state. Any operations that may have been taking place will be suspended immediately. Completion of any operation will not be guaranteed under this condition. The error status will not be cleared. A host reset will not create a Unit Attention error for the next command. Typical recovery time after a reset is 2 milliseconds.

### 2.2.4 Electrical Requirements

All SCSI bus signals operate at standard negative-true TTL levels. Interface lines are terminated at the subsystem controller with a 220/330 ohm network. The host interface adapter should be terminated similarly (see Figure 17). In a multiple host adaptor or controller system, only the end adapter or controller on the multidrop cable should be terminated. The controller is shipped with socketed 220/330 ohm terminators to allow for a simple multicontroller configuration. Devices driving the controller inputs should be an open collector capable of sinking at least 48 milliamps to a voltage level of less than 0.5 vdc (7438 or equivalent). Receivers with hysteresis are recommended for receiving the controller outputs to improve the noise margin (74LS240, 74LS14, or equivalent). The host adapter should not load the bus with more than one low power Shottky (LS) TTL input load per line.

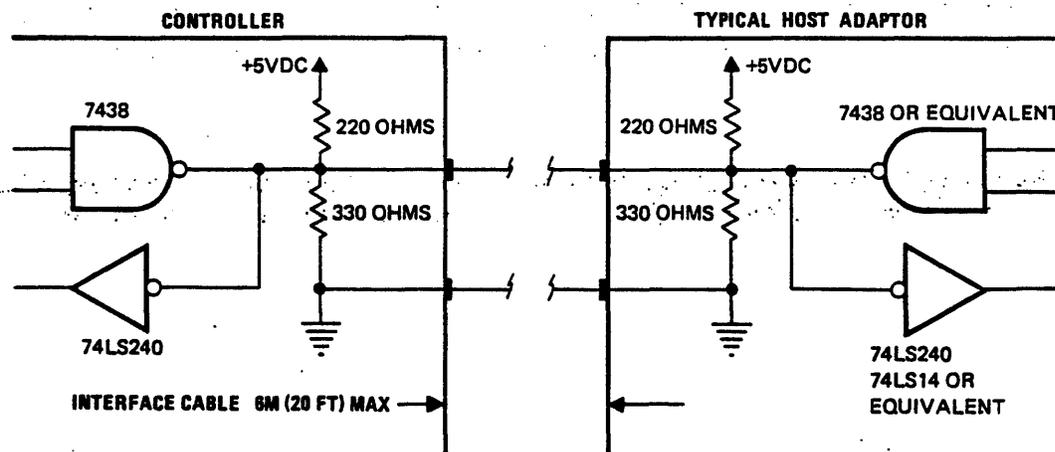


Figure 17. Host Adapter Bus Termination

## 2.3 SCSI SOFTWARE INTERFACE

The command set used by the 8 inch removable disk storage subsystem is described in this subsection. The set is structured to satisfy the extended command set under the proposed ANSI definition for the Small Computer System Interface.

### 2.3.1 Command Structure

An I/O request from the host is performed by passing a Command Description Block (CDB) to the controller. The first byte of this CDB contains a group code and the command's operation code (OPCODE). Subsequent bytes specify operation parameters, such as the Logical Unit Number (LUN), logical block address, and the number of blocks needed to transfer in a data transfer command. A typical CDB structure is shown in the following example.

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	GROUP CODE			OPCODE				
01	LOGICAL UNIT NUMBER			MSB LOGICAL BLOCK ADDRESS				
02	LOGICAL BLOCK ADDRESS							
03	LSB LOGICAL BLOCK ADDRESS							
04	NUMBER OF BLOCKS							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

Note that, according to SCSI proposed standards, a media change means a check condition must be reported. The SCSI class and code values are zeroes, which would indicate no error, but the Sense Key and Diagnostic Port error code will indicate the media changed status. This means that on all

powerups and every time the load lever of the drive is opened and then closed, the subsystem reports a check condition to the host after the next command since the media might have been changed. The command must be sent again for the operation to take place.

The LUN in byte 01 of a command indicates which drive on the selected controller is to respond to the command. Since up to two drives may be attached to each controller, the high order bits must always be a zero.

The operation code of the CDB specifies the particular command desired. The following commands are supported by this disk storage subsystem.

<u>OPCODE (Hex)</u>	<u>COMMAND</u>
00	Test Unit Ready
01	Rezero Unit
03	Request Sense
04	Format Unit
06	Format Track
07	Reassign Blocks
08	Read Data
0A	Write Data
0B	Seek
12	Inquiry
1B	Start/Stop
1D	Send Diagnostic
1E	Prevent/Allow Media Removal
25	Read Capacity
28	Extended Read
2A	Extended Write
2E	Write and Verify
E5	Read Long

These commands are described in subsection 2.3.3.

The last byte of a typical Command Data Block allows for device-specific interpretation of the SCSI command. The VU means vendor unique; RESERV indicates that these bits are reserved for future needs; and FLAG REQ and LINK allow command chaining options for special purpose application. Since none of these bits are needed or used by the subsystem, they are ignored. Any bits labeled Reserved also are ignored.

## **2.3.2 Logical Block Addressing**

All addressing of information stored on the disk is done by means of logical block addresses. This means that all operations (including data transfers, sector and track flagging, seeking, etc.) that specify a particular location on the disk, use logical addressing to make that specification. To access an individual block, the host specifies its block number. To access a particular track, the host specifies the block number of any one of the logical blocks on that track. If a command implies a seek to a track other than the current track, that seek will be executed automatically.

The blocks available on the 10 Mbyte 8 inch removable disk storage subsystem range from block zero to block 39,167 for the 10 Mbyte device and to block 41,004 for the 10.5 Mbyte drive. Each block is 256 bytes in length and corresponds to one record of a data sector (see subsection 1.4.1.1). The range of specified logical blocks allowed by the SCSI command structure far exceeds the blocks available on the devices. Attempts to specify a logical block number greater than the number available will result in an INVALID ADDRESS error.

### 2.3.3 Command Description

Implementation of the following commands may vary slightly to account for device differences. Thus, the careful study of each command is important to ensure proper operation.

#### 2.3.3.1 Test Unit Ready Command

COMMAND

BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0	0
01	LOGICAL UNIT NUMBER			RESERVED				
02	RESERVED							
03	RESERVED							
04	RESERVED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The TEST UNIT READY command returns zero status in the completion status byte if the addressed unit is powered on and a cartridge is loaded. This is not a request for unit self-test.

#### 2.3.3.2 Rezero Unit Command

COMMAND

BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0	1
01	LOGICAL UNIT NUMBER			RESERVED				
02	RESERVED							
03	RESERVED							
04	RESERVED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The REZERO UNIT command causes a seek to track zero, and clears any error status.

This command is an off-line command, meaning the controller relinquishes control of the bus while the operation is taking place. When the command is received, the controller immediately responds with normal completion status (bit 1=0), and releases the bus. The host then may break away and do other operations while the seek is taking place. The controller is unavailable for any operation until the seek is complete, and will respond with BUSY STATUS (see subsection 2.2.2.5) if selected. The host detects that the operation is complete when the controller accepts a new command. The first command after a REZERO UNIT or SEEK command logically may be a REQUEST SENSE command to determine if the operation was successfully completed.

### 2.3.3.3 Request Sense Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	0	0	0	1	1
01	LOGICAL UNIT NUMBER				RESERVED			
02	RESERVED							
03	RESERVED							
04	NUMBER OF BYTES REQUESTED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The REQUEST SENSE command is used by the host to request status and sense information from the disk subsystem. It is a multipurpose command in that several different amounts and types of information may be requested. Note that this is the only command that will not clear error status. Any error code present will not be cleared.

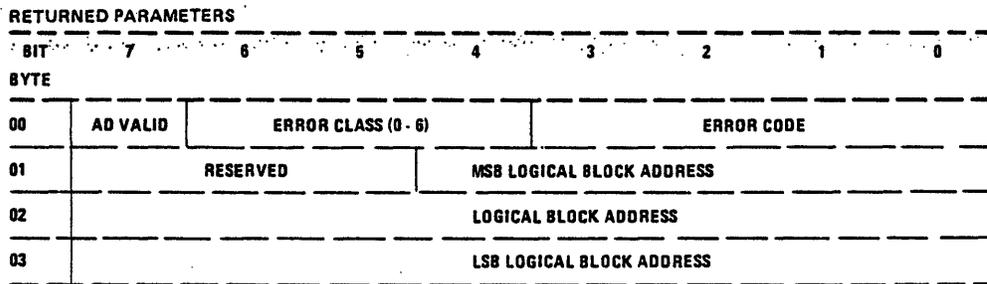
Byte 04, which specifies the number of bytes requested by the host, indicates how much information will be returned. As more bytes are requested, the controller returns more bytes and types of information as shown below.

<u>Number of Bytes Requested</u>	<u>Information Returned</u>
0 to 6	Regular sense data
7 to 8	Extended sense data
9 to 12	Extended sense plus original error class and code
13 to 82	The above plus Z-track data and current track number
83 to 98	The above plus sector ID data
99 to 255	The above plus flagged track listing

The types of information returned for the number of bytes requested are described in the following paragraphs. In accordance with the proposed SCSI protocol, the Media Check condition can occur during this command.

### 2.3.3.3.1 Regular Sense Data

If a request for zero to six bytes of data is made by the REQUEST SENSE command, four to six bytes of sense data will be returned. The first four bytes will have the following format.



If five or six bytes are requested, bytes 04 and 05 will be returned, but their data will be meaningless. A request for less than four bytes defaults to the four bytes.

If the address valid bit is set and the error class and code are zero, the address reported specifies the logical address on which the last operation took place. If the error class or code are non-zero and the address valid bit is set, the address is the location for which the codes are valid.

Error classes and codes are used by the Small Computer System Interface to determine the nature of a system failure. The error class specifies the general type of error and the error code indicates the particular error within that class. Five different error class types are used in this device: 0, 1, 2, 3, and 7. Classes 0, 1, and 2 indicate errors related to the drive, subsystem, and system, respectively. Class 3 reflects startup diagnostics error codes. Class 7 is a special error class number used for reporting extended sense data. Complete error class and code descriptions are presented in Appendix A of this document and in the appendix of the ANSC X3T9.2 SCSI proposal documents.

Status is not cleared by the host reset. If REQUEST SENSE is the first command after a reset, status posted prior to the reset will be reported.

### 2.3.3.3.2 Extended Sense Data

When more than six bytes of data are asked for by the REQUEST SENSE command, the following extended sense format is used.

Class 7, code 0 indicates the use of this format. The Sense Key divides errors into classes that require similar recovery actions. This allows device-independent software to recover from errors.

RETURNED PARAMETERS								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	ADVALID		CLASS 7			CODE 0		
01	RESERVED							
02	RESERVED				SENSE KEY			
03	RESERVED							
04	RESERVED							
05	MSB LOGICAL BLOCK ADDRESS							
06	LSB LOGICAL BLOCK ADDRESS							
07	ADDITIONAL SENSE LENGTH							
08-NN	ADDITIONAL SENSE BYTES							

Bytes 05 and 06 give the logical block address for the last operation. Byte 07 specifies the number of additional bytes that are valid for the response to the REQUEST SENSE command. Those additional bytes start with byte 08 and continue as requested. If only seven bytes of data are requested, bytes 0 through 06 will be sent. If eight bytes are requested, byte 07 will be added, but it will be zero.

### 2.3.3.3 Extended Sense Plus Error Class and Code

As stated, error class 7, code 0 indicates the use of the extended status reporting format. Using the class and code bits of byte 00 for this purpose precludes using them to indicate the nature of a failure. Therefore, if nine or more bytes of data are requested by the REQUEST SENSE command, byte 08 will contain the error class and code for the last operation in bits 6 through 0. Description of the error codes is presented in Appendix A.

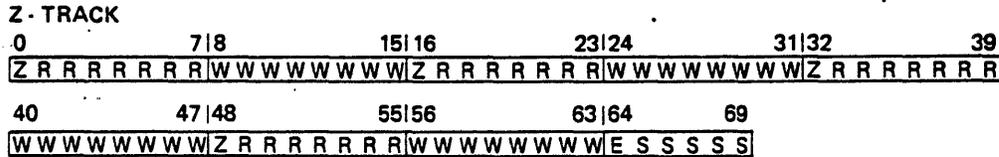
If exactly nine bytes are requested, the controller will respond with the extended sense information plus the error class and code. If 10, 11, or 12 bytes are requested, the requested number of bytes will be transferred, but all bytes past the ninth (byte 08) will be meaningless. Byte 07 will be 1 in each of these cases.

### 2.3.3.4 Z-Track Data and Current Track Number

Each cartridge in the disk storage subsystem has two maintenance tracks, called Z-tracks, which are used for diagnostic purposes and for recording cartridge-specific information. The Z-track format is shown in Figure 18. Format of the cartridge is described in subsection 1.4.1.1.

The information recorded on the Z-sectors of the Z-tracks includes the sector interleave value, ECC enable status, post-write CRC check status, and a dwell timer count. Sector interleaving (see Figure 19) is a way of inter-

placing logical sectors on a track to increase throughput by cutting out full revolution latencies when the host is slower than the disk subsystem. See subsection 1.4.4 for a description of interleaving. The ECC bit enables ECC operations on the cartridge (if the ECC option is present). The post-write CRC check forces a read back CRC check after all write operations. The dwell timer specifies the length of time the drive will remain spinning at full speed if no access is made to it. This timer count has an allowable range of two to 12 counts, with each count representing approximately 2.5 minutes. A count of 15, which will disable the dwell timer, also may be given.



NOTES:

Z: EIGHTEEN BYTES OF INFORMATION ARE REPEATED TO FILL EACH SECTOR DESIGNATED Z. THE 18 BYTES ASSIGNED ARE AS FOLLOWS.

BYTE 1				BYTES 3 THROUGH 18			
BITS		INTERLEAVE		MSB	LSB	MSB	LSB
7	6	5	4	3	2	1	0
X	X	0	0	0	0	0	0
X	X	0	0	0	0	1	0
X	X	0	0	1	0	0	0
X	X	0	0	1	0	0	0
X	X	0	1	0	0	0	0
X	X	0	1	0	0	0	0
X	X	1	0	0	0	0	0
X	X	1	0	0	0	0	0
X	X	1	0	0	0	0	1
X	X	1	0	0	0	0	1

BIT 6 = ECC/NON-ECC	
0	ECC
1	NON-ECC
BIT 7 = POST-WRITE CRC CHECK	
0	ENABLE
1	DISABLE

BYTE 2: DWELL TIMER

BITS 0-3 = TIMER COUNT (2.5 MIN/ COUNT; MIN 2, MAX 12 OR 15 = DISABLED)

BITS 4-7 = 0

3, 4*	00000000	00000000	FIRST BAD TRACK ADDRESS
5, 6	00000001	00110011	SPARE TRACK 1 ADDRESS (307)
7, 8*	00000000	00000000	SECOND BAD TRACK ADDRESS
9, 10	00000001	00110100	SPARE TRACK 2 ADDRESS (308)
11, 12*	00000000	00000000	THIRD BAD TRACK ADDRESS
13, 14	00000001	00110101	SPARE TRACK 3 ADDRESS (309)
15, 16*	00000000	00000000	FOURTH BAD TRACK ADDRESS
17, 18	00000001	00110110	SPARE TRACK 4 ADDRESS (310)

TRACK ADDRESS

R: SEVEN SECTORS REPEATED FOUR TIMES ON THE TRACK, HAVE BEEN PRE-WRITTEN AS NOTED BELOW AND ARE READ DURING STARTUP DIAGNOSTICS.

SECTOR 1.	CRC ERRORS
SECTOR 2.	ALL 1s
SECTOR 3.	STRESS PATTERN
SECTOR 4.	INCREMENTING PATTERN
SECTOR 5.	RESERVED
SECTOR 6.	RESERVED
SECTOR 7.	RESERVED

W: THESE SECTORS HAVE BEEN RESERVED FOR USE DURING EXTENDED STARTUP DIAGNOSTICS; THEY WILL BE WRITTEN WITH VARIOUS PATTERNS, READ BACK AND COMPARED TO ASSURE PROPER OPERATION OF THE READ AND WRITE CIRCUITRY.

E: THE ECC SECTOR FOR THE Z-TRACK.

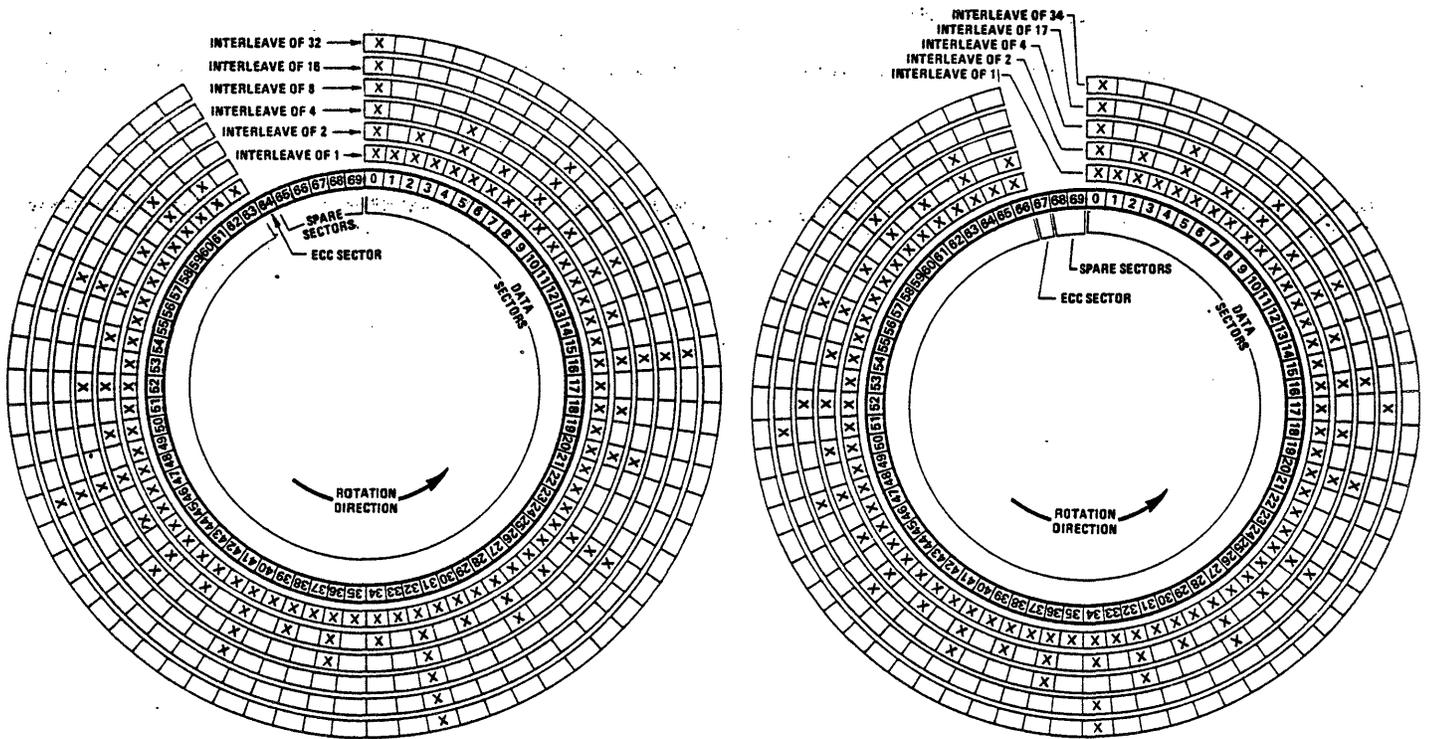
S: SPARE SECTORS.

\* If unused spare, FO hex in each byte; if flagged spare, FF hex in each byte; if used track, address in two bytes.

Figure 18. Z-Track Format

**WARNING**

The purpose of the dwell timer is to extend media life by spinning the drive at half speed after long periods of inactivity. Disabling the timer may affect media life.



**10 MEGABYTE INTERLEAVE**  
 INTERLEAVES OF 1, 2, 4, 8, 16, AND 32 ARE POSSIBLE.

**10.5 MEGABYTE INTERLEAVE**  
 INTERLEAVES OF 1, 2, 4, 17, AND 34 ARE POSSIBLE

Sector interleave is provided by the controller to help match the data rate (on a sector basis) between the disk and controller to that of the host peripheral channel. Without interleave, lengthy rotational delays (40 msec) would occur if the host could not keep up with the subsystem's maximum transfer speed.

Interleave is accomplished by writing consecutive records of data into sectors separated by a specified number of sectors. The number of spacing sectors varies according to a chosen interleave factor. This illustration shows the sectors that would be operated on (denoted by Xs) during the first revolution for each interleave level. The sectors skipped on the first revolution will be used on subsequent passes. For example, four revolutions are required to fill all sectors of a track with interleave 4.

Sector addressing for each interleave level is a function of the microprocessor-based controller. The physical sector IDs are not rewritten. Once programmed on the Z-tracks, interleaving is invisible to the user.

Figure 19. Sector Interleaving

To obtain this information contained in the Z-track controller, the host should send the REQUEST SENSE command and ask for 13 to 82 bytes of data. Any additional bytes requested past 13 and up through 82 will be transferred, but they will contain meaningless information. Byte 07 will be 5 in each of these cases.

### 2.3.3.3.5 Sector ID Data

The ability to read the Identification (ID) information from each sector on the track often is useful in determining the condition of a specific track. Requesting 83 or more bytes of information in a REQUEST SENSE command will cause the controller to send out, in order, 70 bytes of sector ID information of the track indicated in bytes 11 and 12. These 70 bytes correspond to one sector ID byte for each sector on the track. IDs are sent consecu-

tively starting at sector 0, if 0 is found on that track. If a sector has been flagged, the ID byte for that sector will contain F0 (hex). If the ID field of a sector is not readable, the byte representing that sector ID will contain a code that specifies the error. The error codes used (in hex) for this purpose are:

- 80 = ID Read Error (either ID Sync or ID CRC).
- 81 = ID PES Error (ID read error accompanied by a position error signal out of limits).
- 82 = Out of Sync (the controller has missed two sector marks in a row and the hardware apparently is out of sync with the disk).
- 83 = Sector Mark Error (no sector mark was detected).

The sector ID bytes will be sent back to the host in bytes 13 through 82 of the EXTENDED SENSE format. If 84 to 98 bytes are requested by the REQUEST SENSE command, all bytes after number 82 will be meaningless. Bytes 0 through 12 will contain the EXTENDED SENSE, error class and code, Z-track data, and current track number bytes as previously described. Byte 07 will contain 75 in all cases.

RETURNED PARAMETERS

BIT	7	6	5	4	3	2	1	0
00	ADVALID		CLASS 7			CODE 0		
01	RESERVED							
02	RESERVED				SENSE KEY			
03	LOGICAL BLOCK ADDRESS MSB							
04	LOGICAL BLOCK ADDRESS							
05	LOGICAL BLOCK ADDRESS							
06	LOGICAL BLOCK ADDRESS LSB							
07	ADDITIONAL SENSE LENGTH (5)							
08	ADVALID		ERROR CLASS			ERROR CODE		
09	POST-WRITE CRC CHECK 0=ENABLE 1=DISABLE	ECC 0=ENABLE 1=DISABLE	INTERLEAVE (1,2,4,8,16, OR 32 FOR 10 MBYTE; 1,2,4,17, OR 34 FOR 10.5 MBYTE)					
10	RESERVED				DWEELL TIMER COUNT (2-12 OR 15)			
11	CURRENT TRACK NUMBER MSB							
12	CURRENT TRACK NUMBER LSB							

### 2.3.3.3.6 Flagged Track Listing

To get a listing of the tracks that have been flagged on a cartridge, the host should send the REQUEST SENSE command and ask for 99 to 255 bytes of data. As a response, the controller will send sense bytes 0 through 83 and also add the flagged track list in bytes 83 through 98. Any bytes requested after byte 98 will be meaningless. (Byte 0 = first byte.)

The flagged track list is formatted in the following order:

- Byte 83 = MSB of Bad Track
- Byte 84 = LSB of Bad Track
- Byte 85 = MSB of Track 307 (the first spare track)
- Byte 86 = LSB of Track 307

This pattern is repeated three more times for spare tracks 308, 309, and 310 in bytes 87 through 98. If a spare track has not been assigned, the two bytes corresponding to the bad track number for that spare (e.g., bytes 83 and 84) will be F0 hex. Byte 07 will be 91 in all of these cases.

### 2.3.3.4 Format Unit Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	0	0	1	0	0
01	LOGICAL UNIT NUMBER			FMT DATA	COMP LST	DEFECT LST	LIST FMT	
02	RESERVED							
03	RESERVED							
04	RESERVED			INTERLEAVE				
05	RESERV	RESERV	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The FORMAT UNIT command permits the host to set parameters and flag defective areas on the disk. This standard SCSI command allows for device-specific implementation by using byte 01 bits 0 through 4 to specify vendor unique versions of the command.

The 8 inch removable disk subsystem allows multiple configurations of these bits. If bit 4 is zero, the proposed SCSI standard implementation will be performed. In this case, the values of bits 0 through 3 are disregarded. The extended implementation is performed if bit 4 is one and bit 2 is zero (bits 0, 1, and 3 are disregarded). A device-specific interpretation will occur when bits 1, 2, and 4 are set. Any other values for these bits will result in an ILLEGAL REQUEST error.

#### 2.3.3.4.1 Standard Implementation

The FORMAT UNIT command is executed off-line (see subsection 2.3.3.2).

The interleave value in byte 04 will be used to set the interleave value on the Z-tracks of the disk cartridge (see Figure 19 and paragraph 2.3.3.3.4 for a description of interleave). A value of zero in this field will default to an interleave of one. This bit configuration indicates media formatting with verification and an auto-flagging operation of defective areas on the disk cartridge and rearranges sector IDs physically on the disk. No

previously written user data can be recovered after this command begins. This process takes between 1.5 and 5 minutes to complete, depending on the condition of the media. No parameter bytes are sent after the command data block.

### 2.3.3.4.2 Extended Implementation

This command will be executed off-line; no action will begin until ending status has been transferred. (See section 2.3.3.2 for description of the off-line condition.) The defect list is transferred during the data phase of the command.

The host must send at least four bytes of data, the fourth byte indicating the number of additional bytes to be transferred. This number must be divisible by four, as each four bytes will represent one defective block address. The number must be in the range of 0 through 128, allowing a minimum of no defects and a maximum of 32 defects reported. Each four byte entry will contain the logical block address (most significant byte first) of a defect. The first two bytes of each defect address will always be zero for this device. Ending status will be issued as soon as the complete list has been transferred. The defect list must be in ascending order.

#### Format Unit Defect Media List

ADDITIONAL COMMAND PARAMETERS								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	RESERVED							
01	RESERVED							
02	RESERVED							
03	DEFECT LIST LENGTH: N BYTES							
	REPEAT N/4 TIMES WITHIN THE DEFINED LENGTH:							
00	RESERVED							
01	RESERVED							
02	MSB LOGICAL BLOCK ADDRESS							
03	LSB LOGICAL BLOCK ADDRESS							

The defect media list must be in ascending order.

The list of defects will be flagged and the media verified (additional defects may be flagged during verification) and reformatted. The interleave value then will be specified in byte 04 of the command to set the interleave value on the Z-tracks of the cartridge. A value of zero in this byte will default to an interleave of one. This process will take between 1.5 and 5 minutes, depending on the condition of the media and the number of entries in the defect list.

The controller will be in the Hardware Busy state until the operation is complete; no additional commands will be accepted. After the process, REQUEST SENSE may be used to determine the success of the operation. If an error occurs during defect flagging, the block number of the last defect will be returned. If media formatting requires flagging of a sector and there are no spares, the track will be flagged. If no spare tracks are available, the operation will abort.

### 2.3.3.4.3 Device-specific Implementation

Setting bits 1, 2, and 4 of byte 01 means that the interleave bits of the CDB will be ignored, and the host must send six additional parameter bytes to the subsystem to control five variations of this command. These bytes are transferred during the data phase of the command. The format for the six bytes is:

ADDITIONAL COMMAND PARAMETERS							
BIT	7	6	5	4	3	2	1 0
BYTE							
00	FORMAT Z-TRACKS	FLAG SECTOR	FLAG TRACK	UNFLAG TRACKS	REMAKE Z-TRACKS	RESERVED	
01	DEFINITION DEPENDS ON OPERATION SPECIFIED IN BYTE 00						
02	DEFINITION DEPENDS ON OPERATION SPECIFIED IN BYTE 00						
03	DEFINITION DEPENDS ON OPERATION SPECIFIED IN BYTE 00						
04	DEFINITION DEPENDS ON OPERATION SPECIFIED IN BYTE 00						
05	RESERVED						

Bits 3 through 7 of byte 00 specify which of the five operations is to take place. Starting at bit 7, the controller will perform the operation indicated by the first bit it finds set high. Only one operation will be executed each time the command is sent, so any bits in byte 00 to the right of the first set bit will be ignored. If none of the first five bits is set, an ILLEGAL REQUEST error will be indicated by the controller.

Definitions of the other bytes in this six byte extension depend on the operation being performed. These definitions and descriptions of the five new operations follow.

#### Format Z-Track, Remake Z-Track

The FORMAT Z-TRACK operation is used to change the cartridge-specific information on the Z-tracks (see subsection 2.3.3.3 and Figure 18).

If the Z-tracks become unreadable for any reason, the cartridge will not spin up and continue spinning, and no operations will be allowed on the drive (including FORMAT Z-TRACK). The REMAKE Z-TRACK operation has been implemented to provide a failsafe means of data recovery under these conditions. This operation will cause the disk to spin up and stay spinning regardless of the prior contents and condition of the Z-

tracks. The controller then will attempt to rewrite the Z-tracks according to specified parameters.

**WARNING**

**REMAKE Z-TRACK unflags all previously flagged tracks. The user is responsible for data integrity.**

For these two operations, the six byte extension of the FORMAT UNIT command follows

ADDITIONAL COMMAND PARAMETERS						
BIT	7	6	5	4	3	2 1 0
00	FORMAT Z-TRACKS	0	0	0	REMAKE Z-TRACKS	RESERVED
01	POST-WRITE CRC CHECK 0=ENABLE 1=DISABLE	ECC 0=ENABLE 1=DISABLE	INTERLEAVE (1,2,4,8,16, OR 32 FOR 10 MBYTE; 1,2,4,17, OR 34 FOR 10.5 MBYTE)			
02	RESERVED			DWEELL TIMER COUNT (2-12 OR 15)		
03	RESERVED					
04	RESERVED					
05	RESERVED					

**WARNING**

**If the cartridge is non-ECC and is to be changed to ECC, ALL customer data on the cartridge will be destroyed.**

**FURTHERMORE: The REMAKE Z-TRACK command with ECC enabled will ALWAYS destroy all customer data, even if ECC was already enabled.**

The six byte extension for this case is:

ADDITIONAL COMMAND PARAMETERS						
BIT	7	6	5	4	3	2 1 0
00	0	FLAG SECTOR	FLAG TRACK	0	0	RESERVED
01	RESERVED			MSB LOGICAL BLOCK ADDRESS		
02	LOGICAL BLOCK ADDRESS					
03	LSB LOGICAL BLOCK ADDRESS					
04	*ECC SECTOR	RESERVED				
05	RESERVED					

\* FLAG SECTOR ONLY

Flag Sector, Flag Track

The FLAG SECTOR and FLAG TRACK operations provide a means for logical replacement of defective areas on the disk. In each case, the bad

areas are replaced with spares, and any further accesses to the flagged data block will automatically reference the spare block assigned in its place. The host is not required to keep a defective block table. The data bytes are not moved from the defective block to the spare, so the maintenance of data integrity under these operations is up to the host and/or user.

**WARNING**

**Since data bytes are not transferred in this operation, the host is responsible for maintaining data integrity.**

During a FLAG SECTOR operation, a hex F0 pattern is written into the sector ID field of the defective sector, and the original sector ID is copied into the sector ID field of the next unflagged sector. The remaining unflagged sector IDs through the end of the track are all moved over one sector position to allow room for this operation. The host is responsible for moving the data for the flagged sector, and sectors on this track physically following the flagged sector, after this operation takes place. If no other spare sectors are available on that track, or an ID cannot be written, the command returns an abnormal completion in the ending status byte (bit 1=1). After verification that no other spare sectors are available (via a REQUEST SENSE command), the track should be flagged.

The REQUEST SENSE command should be issued after every check condition (bit 1=1 in ending status) to determine the disk location to be flagged. If the error was due to a media problem and the AD VALID bit was set, the logical block address returned should be sent as the address for the FLAG SECTOR command. If the error occurred on an ECC sector, a special error class and code are returned (1D Hex). In this case, the AD VALID bit is not set but the logical block address returned should be sent as the address for the FLAG SECTOR command. Also, bit 7 of byte 04 should be set indicating that it is the ECC sector on the same track as the logical block address to be flagged. If an ECC sector error did not occur and the AD VALID bit is not set, no sector flagging operation should take place since the exact error location is uncertain.

For FLAG TRACK operations, the defective track list for a cartridge is written on the Z-tracks. This information is read by the controller as part of the startup sequence each time a cartridge is inserted. If no spare tracks are available on the cartridge or the Z-tracks cannot be updated for some reason, an error condition will be reported by the controller. The logical block address given may fall anywhere on the track being spared.

#### Unflag Tracks

Issuing an UNFLAG TRACKS operation as part of the FORMAT UNIT command will unflag all flagged tracks on the cartridge. An F0F0 hex pattern will be written in the Z-track locations, thus clearing the bad track

table. Since data bytes are not transferred in this operation, the host is responsible for maintaining data integrity. The six byte extension to the format unit command for this operation is:

ADDITIONAL COMMAND PARAMETERS								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	UNFLAG TRACK	0	RESERVED		
01	RESERVED							
02	RESERVED							
03	RESERVED							
04	RESERVED							
05	RESERVED							

### 2.3.3.5 Format Track Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	0	0	1	1	0
01	LUN			MSB LBA				
02	LOGICAL BLOCK ADDRESS							
03	LSB LOGICAL BLOCK ADDRESS							
04	RESERVED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The FORMAT TRACK command allows the host to initiate a media checking/formatting sequence similar to the FORMAT UNIT command, but on a track basis rather than with the entire media. The track's sector IDs will be resequenced, the track checked for media defects, and sectors spared for any identified defects. If no spare sectors are available, the track will be spared. Recovery of user data for this track is not possible once execution of this command begins.

### 2.3.3.6 Reassign Blocks Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	0	0	1	1	1
01	LUN			RESERVED				
02	RESERVED							
03	RESERVED							
04	RESERVED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The REASSIGN BLOCKS command allows the host to spare media defects without affecting the integrity of any other blocks on the device (unlike the FLAG SECTOR command, which does alter other blocks on the same track). The defect media list is sent during the data phase of the command (see subsection 2.3.3.4.2 for a description of this list). The specified blocks will be re-assigned using spares.

**NOTE:** The ability of the subsystem to reassign a block is based on flagging a 512 byte sector. Therefore, two logical blocks will be reassigned for each block address passed in the defect list. If the address is an even numbered block, the next higher logical block also will be reassigned. If the address is an odd numbered block, the next lower logical block also will be reassigned. If both addresses of a physical sector are in the defect list, the controller will not reassign twice.

### 2.3.3.7 Read Data Command

COMMAND

BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	1	0
01	LOGICAL UNIT NUMBER			MSB LOGICAL BLOCK ADDRESS				
02	LOGICAL BLOCK ADDRESS							
03	LSB LOGICAL BLOCK ADDRESS							
04	NUMBER OF BLOCKS							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The READ DATA command initiates a transfer of data from the disk subsystem to the host. The starting block is specified by bytes 01, 02, and 03 of the CDB; and the number of blocks to be transferred is given in byte 04.

**WARNING**  
If byte 04 is 0, then 256 blocks are transferred.

### 2.3.3.8 Write Data Command

COMMAND

BIT	7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	0	0
01	LOGICAL UNIT NUMBER			MSB LOGICAL BLOCK ADDRESS				
02	LOGICAL BLOCK ADDRESS							
03	LSB LOGICAL BLOCK ADDRESS							
04	NUMBER OF BLOCKS							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The WRITE DATA command initiates a transfer of data from the host to the disk subsystem. The starting block address is specified by bytes 01, 02, and 03 of the CDB, and the number of the blocks to be transferred is given by byte 04.

**WARNING**  
**If byte 04 is 0, then 256 blocks are transferred.**

### 2.3.3.9 Seek Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	0	1	0	1	1
01	LOGICAL UNIT NUMBER			MSB LOGICAL BLOCK ADDRESS				
02	LOGICAL BLOCK ADDRESS							
03	LSB LOGICAL BLOCK ADDRESS							
04	RESERVED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The SEEK command requests the indicated drive to seek to the track containing the specified logical block address. This is an off-line command, like the REZERO UNIT command. (See subsection 2.3.3.2.)

### 2.3.3.10 Inquiry Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	1	0	0	1	0
01	LUN			RESERVED				
02	RESERVED							
03	RESERVED							
04	NUMBER OF BYTES REQUESTED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The INQUIRY command requests the controller to send device-specific information to the host. This can be used to allow device-independent software to adapt dynamically to the available hardware. Although only the first six returned parameter bytes currently have any meaning, the controller will transfer the number of bytes requested, but will return no bytes if a count of zero is given.

RETURNED PARAMETERS								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	DEVICE TYPE CODE (00)							
01	DEVICE TYPE QUALIFIER							
02	SCSI REVISION LEVEL (00)							
03	RESERVED							
04	ADDITIONAL LENGTH N BYTES							
05	RESERVED	RESERVED	1=10.0 0=10.5	1=ENABLE RETRIES 0=DISABLE RETRIES	1=DISABLE STARTUPS 0=ENABLE STARTUPS	1	1	RESERVED
ADDITIONAL UNIT PARAMETER BYTES								

Device type code is 00 for a direct access device. Device Qualifier code is 80 (hex) for a removable device without user assigned codes. Revision level is currently 00 for unspecified. Zeroes will be returned in any bytes after 05. Byte 04 contains a count of the additional bytes requested. The first unit parameter byte contains the current switch settings on the digital board as indicated above.

**NOTE:** This command does not check for, nor report, the UNIT ATTENTION status, nor does it clear it. The controller cannot distinguish between a drive that is not loaded and a drive that is not present. A 00 will be returned in byte 00 for any LUN queried on the controller.

### 2.3.3.11 Start/Stop Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	0	1	1	0	1	1
01	LUN			RESERVED				IMM
02	RESERVED							
03	RESERVED							
04	RESERVED							1=START 0=STOP
05	1=DISABLE DWELL 0=ENABLE DWELL SEEKS	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The START/STOP command allows the host to request that the spindle of the specified drive be spun up or down. If bit 0 of byte 04 is one, the specified drive will spin up. If bit 0 of byte 04 is zero, the specified drive will spin down. The drive cannot be spun up if the load lever is not vertical and a cartridge loaded. The drive will spin down, but the green light will keep flashing and the bezel is still locked when using a PREVENT MEDIA REMOVAL command with a STOP command.

As with loading a cartridge, the controller may require several seconds to spin up the drive. For this reason, the host is given the choice of doing this command on-line or off-line. If bit 0 of byte 01 is one, the command will be executed off-line, freeing the SCSI bus. If bit 0 of byte 01 is zero, the command will be executed on-line (and also tie up the SCSI bus).

If bit 7 of byte 05 is one, dwell seeks are disabled. If bit 7 of byte 05 is zero, dwell seeks are enabled.

**WARNING**

The purpose of the dwell seeks is to extend media life. By disabling dwell seeks, media life may be shortened.

**2.3.3.12 Send Diagnostic Command**

COMMAND

BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	1	1	0	1
01	LUN			RESERVED		1	0	0
02	RESERVED							
03	DATA VARIABLE LENGTH MSB							
04	DATA VARIABLE LENGTH LSB							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The SEND DIAGNOSTIC Command allows the host to invoke the startup diagnostic routines described in subsection 3.3 on the specified LUN. The controller will go off-line until the diagnostics are completed. Byte 02 must be issued as shown; the other SCSI options for this command are not supported. Any other configurations will generate an Illegal Request error.

**2.3.3.13 Prevent/Allow Media Removal Command**

COMMAND

BIT	7	6	5	4	3	2	1	0
00	0	0	0	1	1	1	1	0
01	LUN			RESERVED				
02	RESERVED							
03	RESERVED							
04	RESERVED							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

1=PREVENT  
0=ALLOW

The PREVENT/ALLOW MEDIA REMOVAL command allows the host to prevent removal of the cartridge at an undesirable time, such as when updating a directory or packing the files on the device. This command works by instructing the controller not to poll the bezel switch on the specified drive. The command

will remain in effect until explicitly enabled, or until a host reset or power-on reset occurs.

If bit 0 of byte 04 is one, media removal will be inhibited. If bit 0 of byte 04 is zero, media removal will be enabled.

### 2.3.3.14 Read Capacity Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	1	0	0	1	0	1
01	LUN			RESERVED				
02	LOGICAL BLOCK ADDRESS MSB							
03	LOGICAL BLOCK ADDRESS							
04	LOGICAL BLOCK ADDRESS							
05	LOGICAL BLOCK ADDRESS LSB							
06	RESERVED							
07	RESERVED							
08	PARTIAL/FULL MEDIA INDIC.							
09	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The ten byte READ CAPACITY command allows the host to determine the capacity and block size of a unit and also to determine track boundaries, where data transfer will encounter a substantial delay for a seek to occur. If byte 08 is 00, the address and size of the last block on the drive is reported. If byte 08 is one, this command will report the address and block size of the last logical block on the same physical track as on the specified block. The block size for this device is always 256. If bit 0 of byte 01 is set (an SCSI option), an Invalid Request error will be issued. The data format returned by this command is as follows.

RETURNED PARAMETERS								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	LOGICAL BLOCK ADDRESS MSB							
01	LOGICAL BLOCK ADDRESS							
02	LOGICAL BLOCK ADDRESS							
03	LOGICAL BLOCK ADDRESS LSB							
04	BLOCK SIZE MSB - ALWAYS 0							
05	BLOCK SIZE - ALWAYS 0							
06	BLOCK SIZE - ALWAYS 1							
07	BLOCK SIZE LSB - ALWAYS 0							

### 2.3.3.15 Extended Read Command

COMMAND

BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	1	0	1	0	0	0
01	LUN			RESERVED				RELATIVE ADDRESS
02	LOGICAL BLOCK ADDRESS MSB							
03	LOGICAL BLOCK ADDRESS							
04	LOGICAL BLOCK ADDRESS							
05	LOGICAL BLOCK ADDRESS LSB							
06	RESERVED							
07	NUMBER OF BLOCKS MSB							
08	NUMBER OF BLOCKS LSB							
09	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The EXTENDED READ command operates the same as the READ DATA command, but provides for larger capacity devices and also permits requests for more than 256 blocks. This command initiates a transfer of data to the host. The starting block address is specified in CDB bytes 02 through 05, and the block count is given in bytes 07 and 08. If zero blocks are requested, no data bytes are transferred, and no error is reported. If bit 0 of byte 01 is set (an SCSI option), an Illegal Request error will be issued.

### 2.3.3.16 Extended Write Command

COMMAND

BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	1	0	1	0	1	0
01	LUN			RESERVED				RELATIVE ADDRESS
02	LOGICAL BLOCK ADDRESS MSB							
03	LOGICAL BLOCK ADDRESS							
04	LOGICAL BLOCK ADDRESS							
05	LOGICAL BLOCK ADDRESS LSB							
06	RESERVED							
07	NUMBER OF BLOCKS MSB							
08	NUMBER OF BLOCKS LSB							
09	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The EXTENDED WRITE command operates the same as does the WRITE DATA command, but provides for larger capacity devices and also permits requests for more than 256 blocks. This command initiates a transfer of data from the host.

The starting block address is specified in the CDB bytes 02-05, and the block count is given in bytes 07 and 08. If zero blocks are requested, no data bytes are transferred, and no error is reported. If bit 0 of byte 01 is set (an SCSI option), an Illegal Request error will be issued.

### 2.3.3.17 Write and Verify Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	0	0	1	0	1	1	1	0
01	LUN			RESERVED				RELATIVE ADDRESS
02	LOGICAL BLOCK ADDRESS MSB							
03	LOGICAL BLOCK ADDRESS							
04	LOGICAL BLOCK ADDRESS							
05	LOGICAL BLOCK ADDRESS LSB							
06	RESERVED							
07	NUMBER OF BLOCKS MSB							
08	NUMBER OF BLOCKS LSB							
09	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The WRITE AND VERIFY command operates the same as does the WRITE DATA command, but provides post-write CRC checking. This command initiates a transfer of data from the host. The starting block address is specified in CDB bytes 02 through 05, and the block count is given in bytes 07 and 08. If zero blocks are requested, no data bytes are transferred, and no error is reported. If bits 0 or 1 of byte 01 is set (SCSI options), an Illegal Request error will be issued.

### 2.3.3.18 Read Long Command

COMMAND								
BIT	7	6	5	4	3	2	1	0
BYTE								
00	1	1	1	0	0	1	0	1
01	LUN			LOGICAL BLOCK ADDRESS MSB				
02	LOGICAL BLOCK ADDRESS							
03	LOGICAL BLOCK ADDRESS LSB							
04	NUMBER OF BLOCKS							
05	VU	VU	RESERV	RESERV	RESERV	RESERV	FLAG REQ	LINK

The READ LONG command functions identically to the READ DATA command, unless a CRC error is encountered. If a CRC error occurs using the standard READ

DATA command, the data will not be returned to the host. This command can be used if the host is capable of determining the usefulness of the data. Using this command, if an error occurs, the data will be passed to the host, then ending status will be sent with the check bit set. If an error is encountered, the command will be aborted after sending the suspect data block. The host is responsible for correction or integrity of the data. If no error occurs, this command will function the same as does the usual READ DATA command.

## 2.4 POWER INTERFACE

Power supply current requirements for the drive and controller are detailed in Table 1. The subsystem has a maximum continuous power consumption of 25 watts (single drive and controller). This maximum can be achieved only with the drive in a rapid random seek mode. Values are shown in Table 1.

TABLE 1  
MAXIMUM POWER REQUIREMENTS

Single Drive with Controller			Two Drives with One Controller	
+5 ±5%	1.5 amps (avg)	1.5 amps peak	1.8 amps (avg)	1.8 amps peak
Ripple	30 mv RMS	120 mv P-P	30 mv RMS	120 mv P-P
+12 ±5%	1.5 amps (avg)	3 amps 25% duty cycle	2.0 amps (avg)	3.5 amps peak
Ripple	60 mv RMS	300 mv P-P	60 mv RMS	300 mv P-P

Table 1 lists the maximum current requirements from each supply voltage for the different operating modes of the drive. Note that certain operations have instantaneous peak requirements of sufficient duration to specify the maximum drive requirement. In particular, disk spin-up requires up to 1.5 amps for approximately 4 sec from the +12 vdc supply. Also up to 1.4 amps (10 msec) are required for a seek. These peak requirements must be considered in the selection of subsystem power supplies.

Active seeking or track following can take place only on one drive at a time. Because of this and because one controller board can control two drives, power requirements for each additional drive are significantly less than for the initial system.

## **3.0 OPERATIONAL INFORMATION**

This manual section contains information needed to operate the disk storage subsystem. Cartridge loading, handling, write protection, and removal from the drive are explained.

Controls for operating the subsystem include a cartridge removal push button switch, a motor loading lever, and two LED indicators. These components, along with the cables and connectors needed for the host-to-subsystem interface, power supply, and the controller to drive interface are described in this section.

### **3.1 CARTRIDGE USE**

Proper use and care of the subsystem cartridge are important for the preservation of data integrity and assurance of long cartridge life. This portion of the manual deals with cartridge loading, handling, write protect, and removal procedures.

#### **3.1.1 Loading and Removal**

The cartridge may be inserted into the drive, access door end first, any time the motor load lever is parallel to the drive opening. The edge of the cartridge containing the access door should face toward the stop button on the front of the drive (see Figure 20). Interlocks in the system prevent improper cartridge insertion. As the cartridge is inserted, keys on the Bernoulli plate will interact with and open the access door, thus providing access to the disk.

Once the cartridge is in place, the load lever may be turned clockwise to load the motor and initiate drive spinup. When the lever has completely loaded the motor, the green LED on the front of the drive will begin to blink. At this time a latch pin will engage to lock the lever. As the drive motor reaches operating speed the green LED will glow steadily.

To remove the cartridge, push the stop button. The green LED then will begin to blink as the motor spins down. When the motor has come to a stop, the green LED turns off and the latch pin will disengage to allow the lever to unload the motor. At this time the lever may be turned counterclockwise and the cartridge removed.

If a command requiring a drive to spin up or down is received from the host, BUSY status will be reported and the drive will spin up. If a command is received by the subsystem from the host directly after a drive has spun down, an error status will be reported with Cartridge Not Loaded as the error specified in response to a request sense command. This allows time for the user to remove the cartridge. After a time delay of 10 seconds to 1 minute (depending upon system activity), the spun down drive will respond to a command by locking the load lever and spinning the drive motor. As the motor comes up to speed, of course, BUSY status will be reported to the host.

**WARNING**

If the cartridge is difficult to insert, check its orientation and try again. Do not force the cartridge into the drive. Do not insert objects into the cartridge opening in front of the drive since damage may result. Such action will void any manufacturer's warranty.

### 3.1.2 Handling

Although the cartridge protects the disk from most accidental damage, observation of the following cartridge handling rules is still important.

- Do not try to open the access door when the cartridge is outside the drive.
- Do not insert objects into the front slots of the cartridge.
- Remove the cartridge from the drive after use and store in its protective jacket.
- Do not exceed temperature or other specifications in shipping or storage.
- Do not expose the cartridge to direct sunlight or moisture.
- Do not expose the cartridge to magnetic fields greater than 30 oersteds.
- Protect the cartridge from dirt, spills, and harsh environments.
- Avoid handling the front edge of the cartridge since oils may be transferred from the hand to the Bernoulli plate or disk.

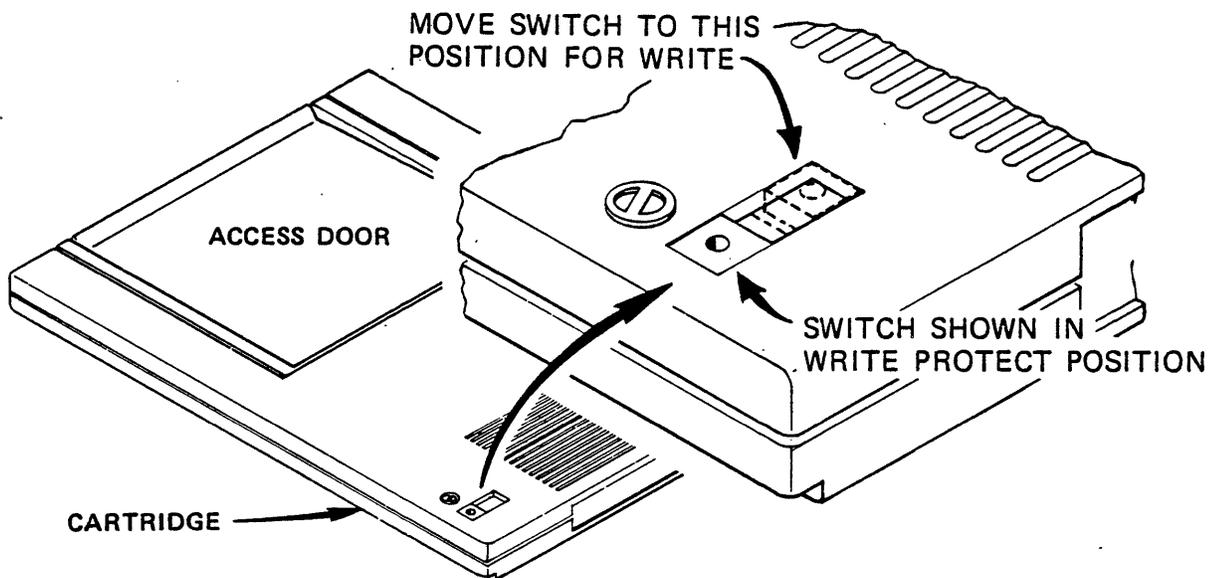


Figure 20. Cartridge with Write Protect Switch

### **3.1.3 Write Protect**

The write protect switch is located on one corner of the cartridge as depicted in Figure 20. The cartridge is write protected when the switch is closest to the edge of the cartridge as shown. The switch may be moved any time the cartridge is out of the drive.

## **3.2 OPERATOR CONTROLS**

The operator interface of the subsystem is made up of a push button switch, a motor load lever, and two LED indicators. The switch, lever, and indicators are located on the front of the drive.

### **3.2.1 Stop Button**

A push button switch is used to stop the disk and allow removal of the cartridge. Pushing the button signals the controller to finish the present operation and stop the spindle motor. Once the motor has stopped, the latch pin that locks the load lever will disengage and the lever will become free to unload the motor.

### **3.2.2 Load Lever**

The load lever is used to load the motor and also to prevent the cartridge from being removed while the motor is spinning. As the lever is rotated clockwise, it allows the motor to load. When the motor is completely seated, a switch is closed to signal the controller that the motor is loaded. At this time a latch pin is engaged, which prevents the load lever from being turned counterclockwise (and unloading the motor) while the motor is spinning. The lever is constructed to interfere with the cartridge unless the cartridge is fully inserted into the drive, and also to prevent the cartridge from being removed until the motor has been unloaded.

### **3.2.3 Indicators**

The green LED on the front of the drive is the READY indicator. When a cartridge is inserted and the load lever is rotated clockwise, the green LED will begin blinking to signify that the motor is coming up to speed. When the motor speed is at the operating point the green LED will glow steadily to signify that the drive is ready. If the drive is not used for an extended period, a dwell timeout may occur, which causes the drive motor to spin at half speed. The green LED will blink momentarily as it makes the transition from half to full speed. If the stop button is pushed while the drive motor is at either full or half speed, the green LED will blink as the motor spins down and then turns off as the latch pin disengages from the load lever to allow the cartridge to be unloaded.

The red LED will glow whenever the drive is actively servicing a command.

**WARNING**

Do not attempt to turn the load lever while the green LED is glowing, since mechanical binding will result.

### 3.3 STARTUP DIAGNOSTICS

Upon system powerup the interface controller will perform a self-check on RAM and ROM and will verify proper buffer operation. This test takes approximately 3 seconds. After completion, control is turned over to the normal operating firmware to begin execution of commands from the host.

If a failure occurs during these initial tests, the controller interface will not respond to a select, and the following error codes may be reported on the diagnostic display.

- 01 -- ROM CRC test failure
- 02 -- RAM test failure
- 03 -- Interface (buffer) test failure

If a more extensive self-check is desired, additional diagnostics that check the read channel and read/write capability of the drive can be appended to these tests. The read/write diagnostics use areas on the Z-tracks, leaving user data untouched. The diagnostics will be invoked following the normal 3 second test if switch 3 on S1 is in the ON position or upon request from the host via the **SEND DIAGNOSTIC** command. These diagnostics take approximately 10 additional seconds to complete and perform the following independent tests.

1. Seek Test -- Check various seek profiles and directions.
2. CRC Check -- Verify proper CRC error detection.
3. Overrun Check -- Verify proper overrun detection.
4. Data Sync/ID Sync Check -- Verify that data and ID sync errors are detected.
5. Data Pattern Read Tests -- Read and compare various data patterns from the Z-tracks.
6. Data Pattern Write Tests -- Write various test patterns to the Z-tracks. Read and compare.
7. ECC Check -- Verify proper ECC write and read capability.

If an error occurs in any of these diagnostic tests, the corresponding error code will be written to the diagnostic display. The host will be informed of a diagnostic failure when it attempts to issue the next command. This next command will be aborted, with completion status indicating an execution error (bit 1 high). The specific error code can be determined via the REQUEST SENSE command. Subsequent commands will be accepted normally, but because of the failure of diagnostic tests, the results cannot be guaranteed.

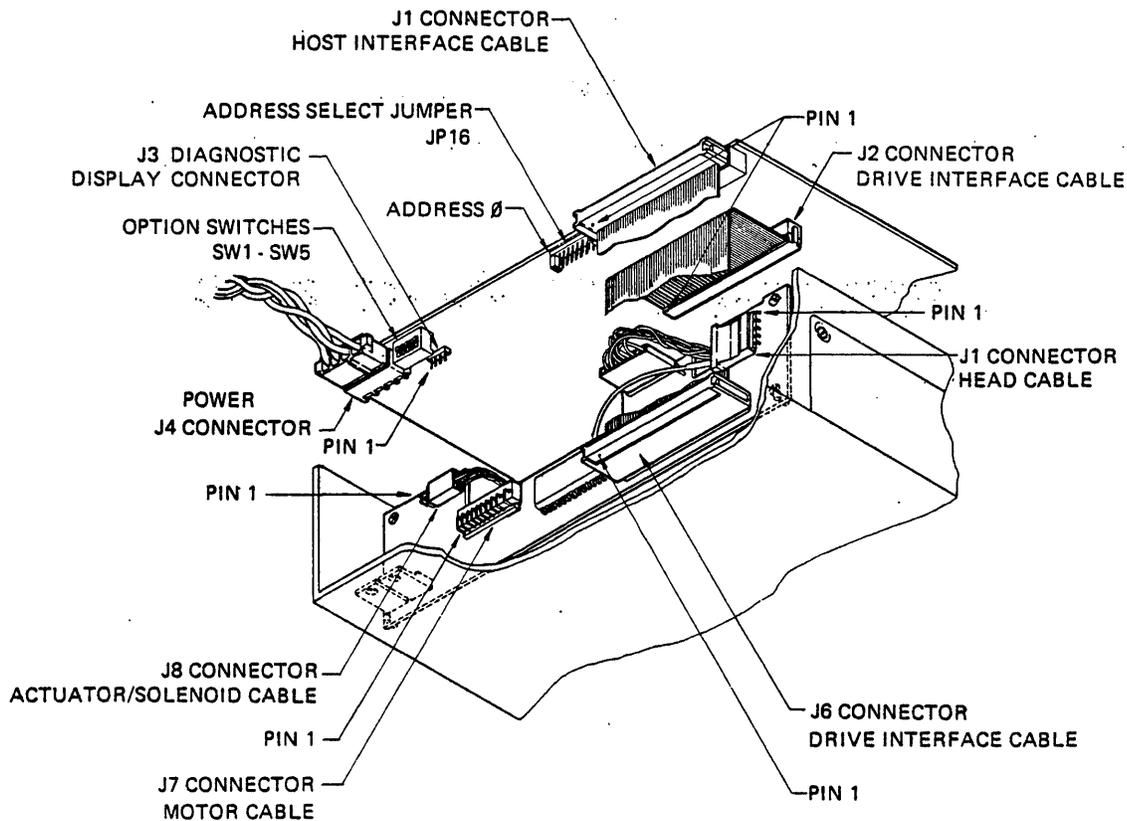


Figure 21. Printed Circuit Board and Main Cable Locations

### 3.4.2 Drive Interface Cable

The drive interface cable connects the controller to the interface board of the drive(s). Each successive drive is attached to the same cable by a 50 pin connector. The maximum recommended length of this cable from the controller to the last drive is 1.0 m (3.3 ft.). The connectors are keyed by plugging locations 34 and 43.

### 3.4.3 Power Cable

Power to the subsystem should be distributed radially with all return wires connected to a common ground at the power supply (Figure 23). Power supply grounds should be connected to a good earth ground, using as short a wire as possible. This wire should be at least 14 gage. Figure 24 shows the recommended grounding scheme. Where possible cable lengths should be 1.0 m (3.3 ft.) or less to minimize line drop. Recommended wire size is 16 gage. With power applied, dc voltage between any two grounds in the system should not exceed 0.06 volts.

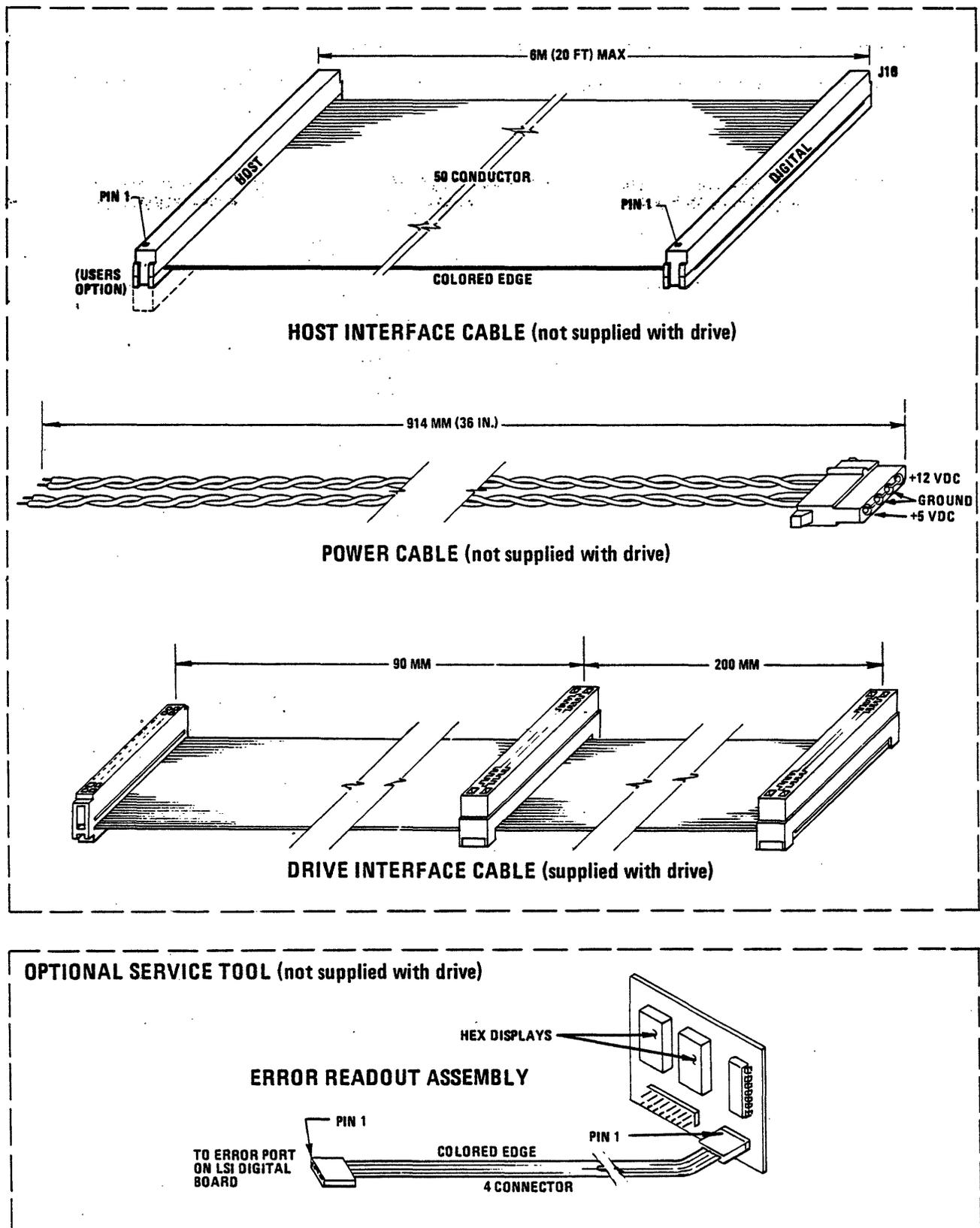
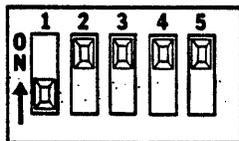
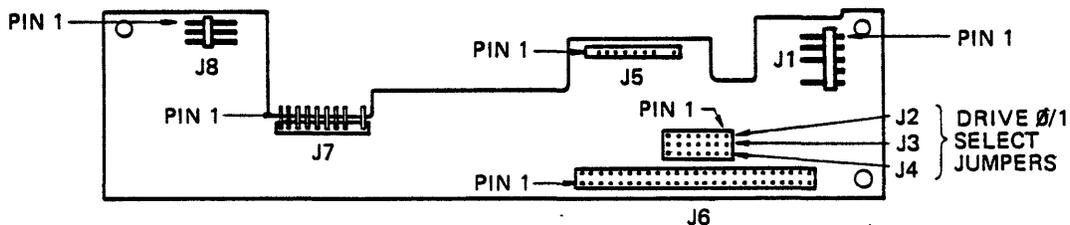
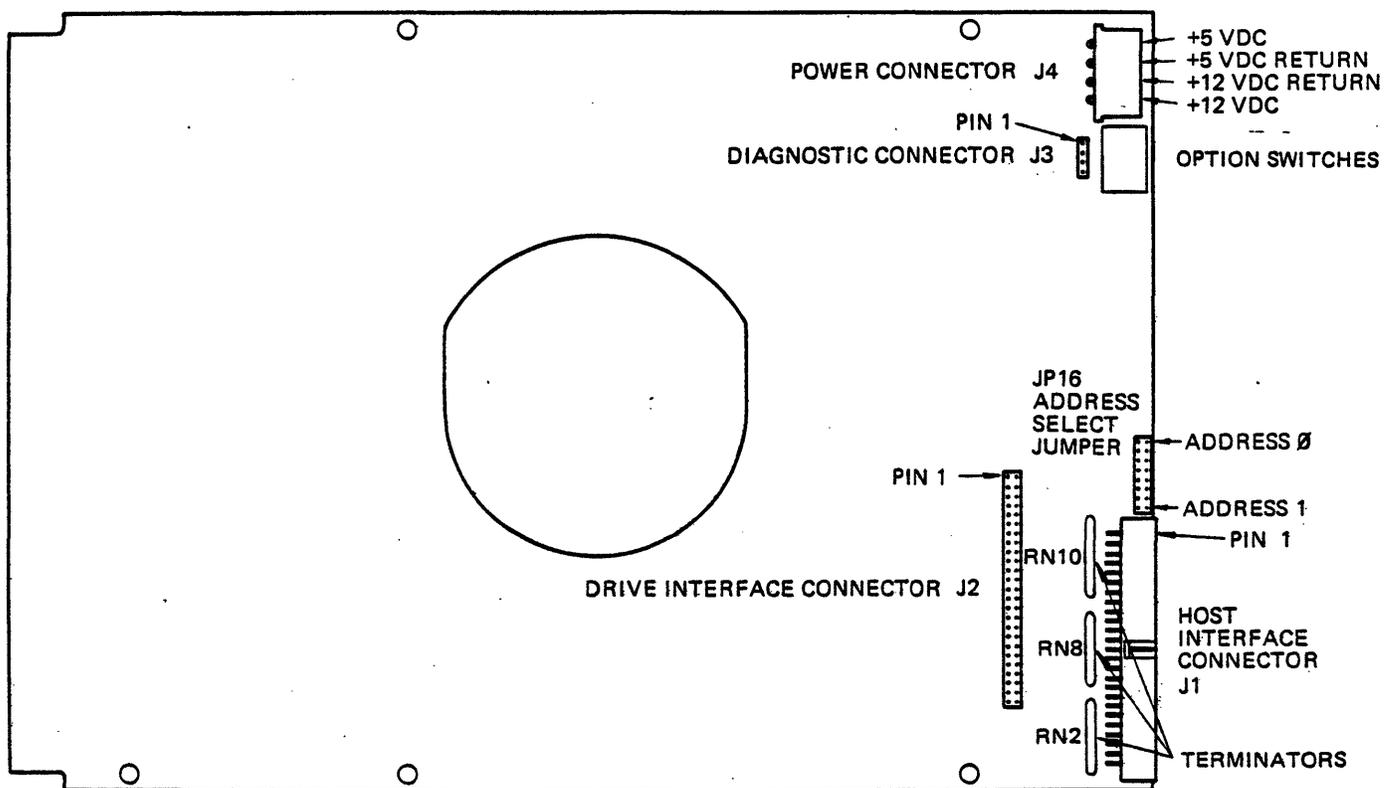


Figure 22. Cabling and Connector Requirements

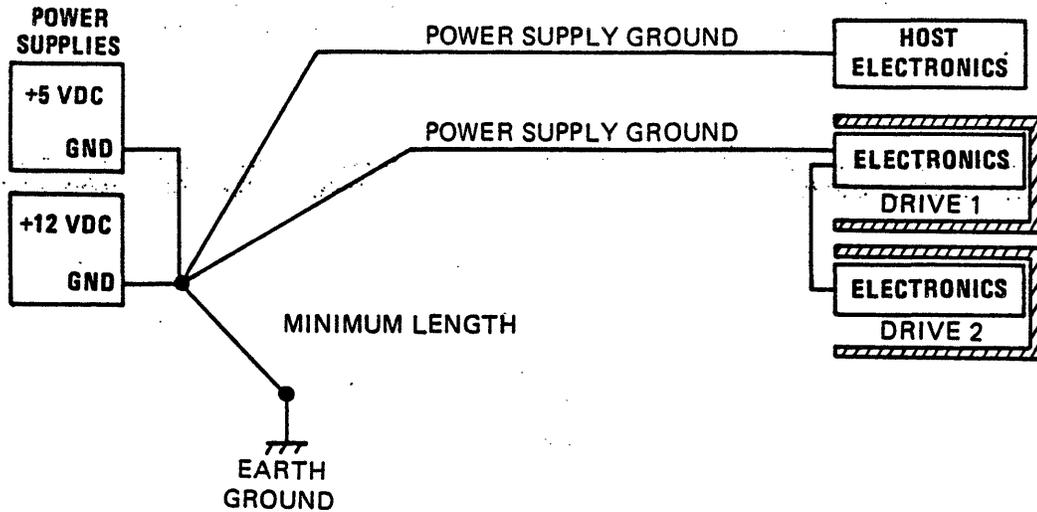


- SW1    OFF = MANUAL POWER-ON RESET  
          (MUST BE SWITCHED OFF FOR SUBSYSTEM TO OPERATE)
- SW2    OFF = PARITY CHECKING  
          ON  = NO PARITY CHECKING
- SW3    SW4
- OFF    OFF = RETRIES ENABLED WITHOUT STARTUP DIAGNOSTICS
- OFF    ON  = RETRIES DISABLED WITHOUT STARTUP DIAGNOSTICS
- ON     OFF = RETRIES ENABLED WITH STARTUP DIAGNOSTICS
- ON     ON  = REPEATING STARTUP DIAGNOSTICS
- SW5    OFF = 10.0 CODE ENABLED  
          ON  = 10.5 CODE ENABLED



(Actuator cables and jumpers identified in Figure 21)

Figure 23. Digital Controller Terminations and Address Options



#### GROUNDING INSTRUCTIONS

KEEP GROUND WIRES AS SHORT AS POSSIBLE.

- TIE ALL POWER SUPPLY GROUNDS TO A COMMON POINT AT THE POWER SUPPLY.
- CONNECT THE POWER SUPPLY GROUND AND THE CHASSIS GROUNDS TO A GOOD COMMON EARTH GROUND USING MINIMUM LENGTH WIRE.
- POWER TO MORE THAN ONE CONTROLLER SHOULD COME DIRECTLY FROM POWER SOURCE' NOT ANOTHER CONTROLLER.

Figure 24. Recommended Grounding

### 3.4.4 Diagnostic Error Display Port

A four pin error port at the diagnostic connector provides the user with an 8 bit error code corresponding to the hex error codes listed in Appendix A. Use of this port is especially helpful in identifying problems during interface development. Pin-out of the port is as follows.

<u>Pin No.</u>	<u>Output</u>
1	Ground
2	Clock
3	+5 vdc
4	Serial Data

If an error is discovered, it is clocked serially to the display port. A shift register IC is necessary to receive the bits for display. An optional diagnostic tool for use with the port to display error information (in hex format) is available from the manufacturer. Appendix B includes ordering information.

### **3.4.5 Drive Addressing**

Three rows of seven pins, each located just above the drive interface connector on the drive interface board (Figure 23), control the drive address selection. The seven position jumper block selects drive 0 if installed between the upper and middle rows of pins, and drive 1 if installed between the lower and middle rows of pins.

The drives can be addressed in any order but no two can have the same address.

### **3.4.6 Controller Addressing and Option Selection**

The eight position bus address shunt JP16 and five position DIP switch S1 on the controller board (Figure 24) must be set up correctly prior to subsystem operation. The shunt bank allows user definition of the controller address during device selection. Only one out of the eight positions should have a shunt in place, indicating which address line must be asserted during the selection sequence (subsystem address).

Dip switch S1 is used to enable or disable various options (Figure 23). These switches are sampled only following a power-on reset. Changing them with power already on may not have any effect.

Bus termination is provided by resistor packs RN1, RN2, and RN3 (Figure 23). If more than one device is connected to the SCSI bus, termination should be provided at the two physical ends of the bus. If the controller is not at either end, resistor packs RN1, RN2, and RN3 should be removed.

## 4.0 CONTROLLER OPTIONS

Subsystem hardware options are available for error correction codes (ECC) and arbitration. A description of the ECC follows; information on the arbitration is now in preparation.

### 4.1 ERROR CORRECTION CODE

The subsystem supports two levels of error correction hardware options: post-write CRC checking and error correction code (ECC). Both of these options involve some overhead that the user should be aware of.

Post-write CRC causes the subsystem to verify data on the disk after write. This verification ensures that the write operation was successful while the host still has the data available, in case any retries are required. After a command has been completed, or whenever the transfer must continue on the next track (whichever comes first), the drive verifies that all the sectors written on the track during this command are readable. The overhead for this operation is one additional revolution, or 40 msec. This overhead can be substantial for multiple single sector transfers on the same track.

The error correction code hardware option is a sophisticated system for data recovery if a read operation fails. A special sector (ECC sector) on each track, plus all the other sectors on the same track, are used to recreate the data from the defective sector. (The host should then rewrite the defective sector and flag it if necessary.) The ECC system involves no overhead for reading (unless it is needed to recover data) but it does require some additional time for writes. The following steps take place for each track during a write operation when ECC is selected. Overhead for each phase is described.

1. All sectors that are to be written during this command are read for use in constructing the ECC sector.

Overhead -- One revolution is needed to read all sectors that are not be be written. If all sectors on the track are to be written, this phase is eliminated.

2. Each sector is written as received and also added to those from Step 1 for constructing the ECC sector.

Overhead -- Same as for normal write operation.

3. The ECC sector for this track or command is written after the last sector.

Overhead -- No additional overhead.

4. Sectors written are checked for CRC validity.

Overhead -- One revolution is required to verify all updated sectors, including the ECC sector.

The total relative overhead of the ECC option depends upon the size of the transfers.

## 4.2 ARBITRATION

Information on this subsystem option is now in preparation and will be provided at a later date.

### 3.4 CABLES AND CONNECTORS

The following interconnections must be made after subsystem unpacking and prior to disk drive operation.

1. Provide an interface to the host.
2. Connect the controller and its resident drive to any additional drives.
3. Supply power to the subsystem.

The controller is resident within the first drive of a one or two drive subsystem. Connection to the host is made through a 50 conductor host interface cable to the controller (Figure 21). The controller is connected to its drive(s) by a 50 conductor drive interface cable in a daisy chain fashion. All necessary data and control signals and power for the second drive are included in the drive interface cable. Power is supplied to the subsystem via the controller by a four conductor cable.

The host interface and power cables are supplied by the user, which allows the cables to be custom fit for particular system configurations. The drive interface cable may be supplied by the user; however, since the controller board must be removed from the drive to make the connection and since testing of both the drive and controller as a subsystem takes place at the factory, the subsystem normally will be shipped with a drive interface cable installed. Each of these cables may be ordered from the manufacturer to fill general requirements.

Ordering information is presented in Appendix B. Detailed information about each of the cables is presented in this subsection. Figures 21 through 24 illustrate the cables and describe their application.

#### WARNING

The host interface cable and the drive interface cable both contain 50 conductors and use the same connector. Damage may occur if they are not connected properly. The drive interface cable on this product is not compatible with that of any previous products of the manufacturer, and connection of other types of drives to this connector will damage the subsystem.

#### 3.4.1 Host Interface Cable

The host interface connection is a 50 pin cable that carries all the signals, commands, and data between the host and the LSI controller. Section 2.0 of this manual includes a description of the interface. The maximum recommended length of this cable is 6 m (20 ft). A shielded cable is recommended if it is to be used outside a shielded enclosure.

## **APPENDIX A**

### **DIAGNOSTIC PORT ERROR CODES FOR THE 10/10.5 MEGABYTE, 8 INCH DISK STORAGE SUBSYSTEM WITH EXTENDED SCSI**

## INTRODUCTION

Error information for the 10/10.5 megabyte 8 inch disk storage subsystem is provided in this Appendix as subsystem Diagnostic Port Error Codes and their equivalent proposed SCSI error codes (Table A-1).

First, error codes are clocked serially to a shift register on the diagnostic display board (see subsection 3.3.4). This type of error code, known as the Diagnostic Port Error Code, is a one-byte hexadecimal (2 digit) number.

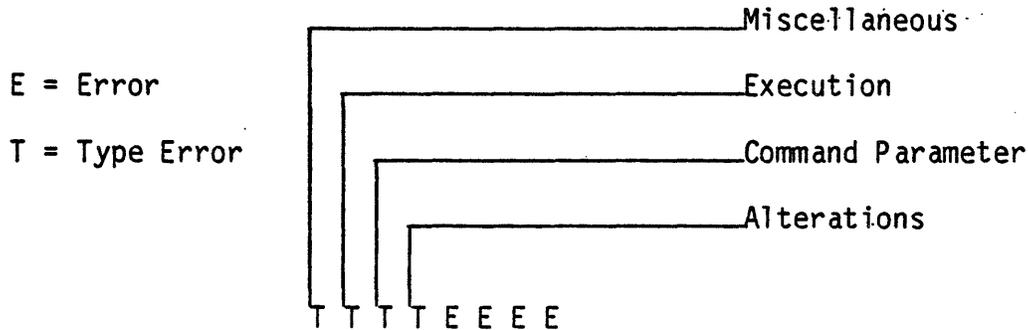
Second, error codes are available as a response to the REQUEST SENSE command. In this case, the error is defined by specifying both an error class and an error code. The error class groups together the errors related to a specific portion of the device. The code indicates a particular error in a given class. In addition, the SCSI EXTENDED SENSE format reports a Sense Key for each error. The Sense Key groups errors together by type, rather than by location in the subsystem. Definitions of the error classes and Sense Keys are included in the proposed ANSI standard, Small Computer System Interface.

Note that, according to the proposed SCSI standards, whenever media changes a check condition must be reported. The SCSI class and code values are zeroes, which would indicate no error, but the Sense Key and Diagnostic Port Error Code will indicate the media changed status. This means that on all power-ups and every time the load lever on the drive is opened and then closed the subsystem reports a check condition to the host after the next command since the media might have been changed. The command must be sent again for the operation to take place.

One other error report exists in which the error class and code are both zeroes: the INVALID REQUEST error. Do not assume that zeroes in the error class and code bits signify that no error has occurred, nor that the media was changed.

## DIAGNOSTIC PORT ERROR CODES

The diagnostic error port error codes presented in this Appendix are effective for the 10/10.5 megabyte, 8 inch disk storage drive subsystem. Structure of the error code is as follows.



Description of the errors and their possible causes are included in the following listing.

Code  
(Hex)    Type Error

00 = NORMAL COMPLETION -- No error was detected.

### Miscellaneous (High Priority) Errors

- 80 = CARTRIDGE WRITE PROTECT -- Caused by trying any write operation on a cartridge that is in the write protect mode.
- 82 = CARTRIDGE NOT LOADED -- Reported when the controller is unable to detect if the cartridge is inserted and the bezel closed.
- 83 = HARDWARE/DISK SYNC ERROR -- This error is an indication that the interrupt generated by the format sequencer is not happening or may not be happening in sync with the disk format.
- 84 = CANNOT READ Z-TRACKS -- An indication that either the controller hardware is unable to read data from the Z-tracks or that the information on the Z-tracks is invalid.
- 86 = SPIN UP FAIL -- An indication that the drive motor has failed to come up to speed within the allotted time.
- 89 = PARITY ERROR -- Will be reported if the controller detects a parity error on the host bus.
- \*8A = OVERRUN ON RECORD 1 -- Record 1 interface buffer either failed to empty or fill within six revolutions.

- \*8B = OVERRUN ON RECORD 2 -- Record 2 interface buffer either failed to empty or fill within six revolutions.
- 8C = MEDIA CHANGED -- Cartridge may have been changed since last access to drive.
- 8D = ECC WAS INVOKED -- Last I/O was completed successfully but ECC was invoked to recover data.
- 8F = NO OPTION -- Tried to invoke an ECC operation without the ECC/ARB hardware option. Can also occur when trying to format a cartridge ECC turned on. An ECC cartridge can be read without the hardware option, but cannot write.
- 90 = Not assigned.
- 91 = SERVO LOOP ERROR -- Failure to acquire track on drive selection. Could be preceded by an 83 error.
- 92 = DRIVE SELECTION ERROR -- Error in switching servo loop from one drive to another. May be preceded by a 91 error.
- 93 = FATAL SEEK ERROR -- Retries exhausted in trying to seek target track.
- 94 = RESEQUENCE ERROR -- Not able to read a sector ID when formatting.
- 95 = ID READ ERROR -- Failed to read ID on source track before seeking to target track.

#### Execution Errors

- 40 = SECTOR NOT FOUND -- Controller was unable to find the requested sector on the disk.
- 41 = SEEK FAIL -- Controller was unable to find the requested track after four tries.
- 42 = OUT OF SYNC -- The controller detected two consecutive missing sector marks during the operation.
- 43 = SECTOR MARK ERROR -- Controller was unable to read a sector mark during an ID write operation.

---

\*Errors 8A and 8B may be seen occasionally in the LED readout, yet not be reported to the host. This condition, though most likely to occur when the host's transfer rate is slow, can occur during any read or write operation. No data loss will occur.

- 44 = PES ERROR -- Indicates that the head may be too far off track to write this sector safely.
- 45 = DATA CRC ON RECORD 1 -- Controller detected a data CRC error on Record 1 of the sector being read.
- 46 = DATA CRC ON RECORD 2 -- Controller detected a data CRC error on Record 2 of the sector being read.
- 47 = DATA SYNC ON RECORD 1 -- Controller not able to read the SYNC mark on Record 1 of the requested sector.
- 48 = DATA SYNC ON RECORD 2 -- Controller not able to read the SYNC mark on Record 2 of the requested sector.
- 49 = PREWRITE CRC ON RECORD 1 -- The controller detected a data CRC error on Record 1 during prewrite CRC check during an ECC write operation.
- 4A = PREWRITE CRC ON RECORD 2 -- The controller detected a data CRC error on Record 2 during the prewrite CRC check during an ECC write operation.
- 4B = POST-WRITE CRC ON RECORD 1 -- The controller detected a CRC error on Record 1 of a sector that was written during this write operation.
- 4C = POST-WRITE CRC ON RECORD 2 -- The controller detected a CRC error on Record 2 of a sector that was written during this write operation.
- 4D = NON-RECOVERABLE ERROR ON RECORD 1 -- The controller has detected more than one record 1 data CRC error on this track during an ECC read.
- 4E = NON-RECOVERABLE ERROR ON RECORD 2 -- The controller has detected more than one record 2 data CRC error on this track during an ECC read.

#### Command Parameter Errors

- 20 = INVALID COMMAND -- The command passed to the controller by the host is not part of the controller command set.
- 21 = INVALID ADDRESS -- The address passed to the controller is out of the address range.
- 22 = INTERLEAVE BAD -- The specified interleave for a FORMAT UNIT command or FORMAT Z-TRACK subcommand was illegal.
- 25 = CARTRIDGE FULL -- A read or a write was attempted beyond the maximum logical address.
- 26 = INVALID REQUEST -- A parameter byte had invalid information.

## Alteration Errors

- 10 = NO SPARE SECTOR -- No remaining spare sectors are on the track.
- 11 = NO SPARE TRACK -- No remaining spare tracks are on the cartridge.
- 12 = WRITE ID ERROR -- Controller was unable to write an ID as requested.
- 13 = BAD TRACK FORMAT -- Track had excessive bad IDs. Controller could not determine which sector to flag.
- 14 = RESEQUENCE READ ERROR -- An ID read error was detected on a pre-write read pass prior to resequencing.
- 15 = TOO MANY FLAGGED IDs -- Resequence routine found more IDs flagged than spares available.
- 16 = RESEQUENCE WRITE ERROR -- An ID error was detected after resequencing.

## Startup Diagnostic Errors

- F0 = SEEK ERROR -- Missed one of 20 random seeks.
- F1 = CRC DETECTION ERROR -- Did not detect all of the prewritten CRC error sectors.
- F3 = WRITE BUFFER FAIL -- Wrote data when the buffers were empty.
- F4 = READ BUFFER FAIL -- Read data when the buffers were full.
- F5 = ALL ONES READ ERROR -- Had a data error on all attempts to read sectors factory-written with an all ones data pattern.
- F6 = STRESS READ ERROR -- Had a data error on all attempts to read sectors factory-written with a stress data pattern.
- F7 = INCREMENTING READ ERROR -- Had a data error on all attempts to read sectors factory-written with an incrementing data pattern.
- F8 = ALL ONES COMPARE ERROR -- Had a data error when the data read did not match the all ones data written at time of test.
- F9 = STRESS COMPARE ERROR -- Had a data error when the data read did not match the stress data written at time of test.
- FA = INCREMENTING COMPARE ERROR -- Same as stress compare error only with an incrementing data pattern.
- FB = ECC CIRCUITRY ERROR -- ECC circuitry not functioning properly.
- FC = SYNC CIRCUITRY ERROR -- Circuitry to detect ID and data sync marks is not functioning properly.

TABLE A-1  
ERROR CODES

Diagnostic Port Error Codes***		SCSI Equivalent			
No.	Description	Sense*		Error Codes	
		Key	Class*	No.	Description
00	NORMAL COMPLETION	0	0	0	NO SENSE
80	CARTRIDGE WRITE PROTECTED	7	1	7	WRITE PROTECTED
82	CARTRIDGE NOT LOADED	2	0	9	MEDIA NOT LOADED
83	HARDWARE/DISK SYNC ERROR	4	0	1	NO INDEX SIGNAL
84	CANNOT READ Z-TRACK	9	0	6	NO TRACK 0
86	SPINUP FAIL	4	0	4	DRIVE NOT READY
89	PARITY ERROR	4	2	3	VENDOR UNIQUE
8A	OVERRUN ON RECORD 1	4	1	B	DATA TRANSFER NOT COMPLETE
8B	OVERRUN ON RECORD 2	4	1	B	DATA TRANSFER NOT COMPLETE
8C	MEDIA CHANGED	6	0	0	NO SENSE
8D	ECC WAS INVOKED	1	1	8	CORRECTABLE DATA CHECK
8F	NO OPTION	9	1	C	NO ECC/ARB OPTION
40	SECTOR NOT FOUND	3	1	4	RECORD NOT FOUND
41	SEEK FAIL	4	1	5	SEEK ERROR
42	OUT OF SYNC	3	0	1	NO INDEX SIGNAL
43	SECTOR MARK ERROR	3	1	2	ID ADDRESS MARK NOT FOUND
44	PES ERROR	3	0	3	WRITE FAULT
45	DATA CRC ON RECORD 1	3	1	1	UNCORRECTABLE DATA ERROR
46	DATA CRC ON RECORD 2	3	1	1	UNCORRECTABLE DATA ERROR
47	DATA SYNC ON RECORD 1	3	1	3	DATA ADDRESS MARK NOT FOUND
48	DATA SYNC ON RECORD 2	3	1	3	DATA ADDRESS MARK NOT FOUND
49	PREWRITE CRC ON RECORD 1 (ECC)	9	1	C	VENDOR UNIQUE
4A	PREWRITE CRC ON RECORD 2 (ECC)	9	1	C	VENDOR UNIQUE
4B	POST-WRITE CRC ON RECORD 1 (ECC)	3	0	3	WRITE FAULT
4C	POST-WRITE CRC ON RECORD 2 (ECC)	3	0	3	WRITE FAULT
4D	NONRECOVERABLE ERROR ON RECORD 1 (ECC)	3	1	1	UNCORRECTABLE DATA ERROR
4E	NONRECOVERABLE ERROR ON RECORD 2 (ECC)	3	1	1	UNCORRECTABLE DATA ERROR
4F**	NONRECOVERABLE ERROR ON ECC SECTOR	9	1	D	VENDOR UNIQUE
20	INVALID COMMAND	5	2	0	INVALID COMMAND
21	INVALID ADDRESS	5	2	1	ILLEGAL BLOCK ADDRESS
22	INTERLEAVE BAD	5	1	A	INTERLEAVE ERROR
25	CARTRIDGE FULL	5	0	A	INSUFFICIENT CAPACITY
26	INVALID REQUEST	5	0	0	NO SENSE
10	NO SPARE SECTOR	3	0	A	INSUFFICIENT CAPACITY
11	NO SPARE TRACK	3	0	A	INSUFFICIENT CAPACITY
12-16	FLAG SECTOR FAILURE	9	1	E	VENDOR UNIQUE
01	ROM TEST FAILURE	-	-	-	] SEE SUBSECTION 3.3, TECHNICAL DESCRIPTION MANUAL, 00701300
02	RAM TEST FAILURE	-	-	-	
03	INTERFACE BUFFER TEST FAILURE	-	-	-	
91-95	SYNCHRONIZATION ERROR	9		C	VENDOR UNIQUE
FO-FC	DIAGNOSTICS FAILURE	A	3	O-C	DIAGNOSTIC ERROR

\* See ANSC X3T9.2 Proposed Standard, Small Computer System Interface.

\*\* Could be any one of the following errors: 40, 44, 47, 48, 4B through 4E. Code 4F is not actually seen on the LEDs.

\*\*\* See Diagnostic Port Error Codes listing in this Appendix.

## **APPENDIX B**

### **INTERCONNECT CABLE ORDERING INFORMATION**

Interface and power cables provide all the interconnection needed to interface the Alpha-10H/10.5H™ disk drive to its host and power supply. The cables are available from IOMEGA Corporation as a convenient aid for interconnection, especially during subsystem evaluation. Also available is a diagnostic tool (error readout assembly), which displays error code information directly from the LSI controller.

Table B-1 of this guide includes cable and connector specifications for users wishing to fabricate their own cable harnesses.

### AVAILABLE FROM THE MANUFACTURER

The following cables can be ordered directly from IOMEGA.

#### HOST INTERFACE CABLE

The host interface cable (Figure B-1) connects the digital controller board to the host adaptor. Consisting of a 50 conductor ribbon cable terminated at each end with a 50 pin IDC connector, it is available in three lengths: 1, 2, and 4 meters. Part numbers of the cables are:

<u>Length (m)</u>	<u>Part Number</u>
1	00116900
2	00112700
4	00112800

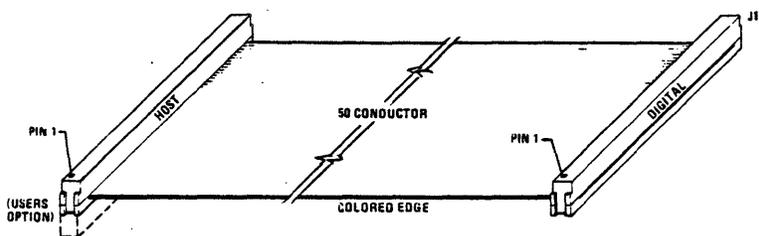


Figure B-1. Host Interface Cable

#### POWER CABLE (IOMEGA P/N 00216000)

Power is supplied to the drive through an 16 AWG, four conductor harness. Length of the harness (Figure B-2) is 36 inches with a connector at one end. The other end is left unterminated, allowing cutting and terminating as required. The power cable also will fit most ST506/706 controllers.

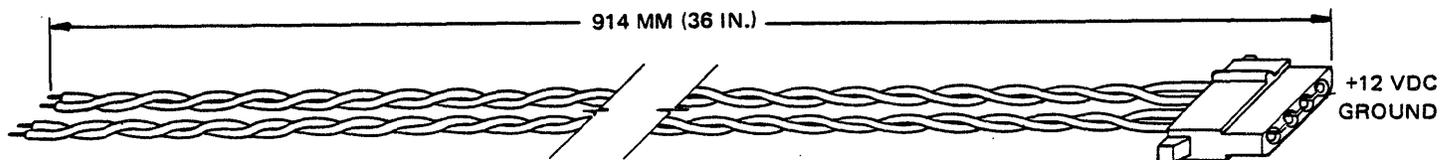


Figure B-2. Power Cable Harness

## ERROR READOUT ASSEMBLY (IOMEGA P/N 00714700)

The error readout assembly (P/N 00714700) which provides error code information on two hex displays (Figure B-3), includes both the IOMEGA unique cable and circuit board for displaying diagnostic information. It connects directly to the diagnostic port on the drive controller board.

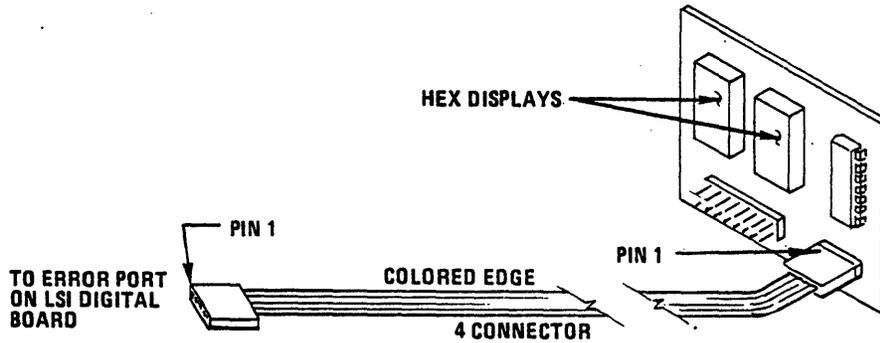


Figure B-3. Error Readout Assembly

## USER FABRICATED CABLE HARNESES

Table 1 shows the details for custom manufacturing the cable harnesses.

TABLE B-1  
CABLE CONNECTOR IDENTIFICATION

Cable	Location	Connector Number	Component					
			Connector			Cable		
			Type	Part Number		Type	Part Number	
				Molex	3M		Molex	3M
Host Interface Cable	Host to Controller	J1	50 Pin	4700 15-25-4505	3425-6000	50 Cond Flat 28 AWG	82-28-5750	3365/5
Drive Interface Cable	Controller to Drive Interface*	J2	50 Pin	4700 15-25-2505	3425-6000	50 Cond Flat 28 AWG	82-28-5750	3365/5
Power Cable	Power Supply to Controller	J4	4 Pin	1-480424-0	--	18 AWG 16/30 Twisted Pair	3075 (Alpha Wire)	--
Error Port Cable	LSI Digital Board	J3	4 Pin	--	--	4 Cond Flat 28 AWG	--	--

\* Pins 43 and 34 are clipped and plugged for keying