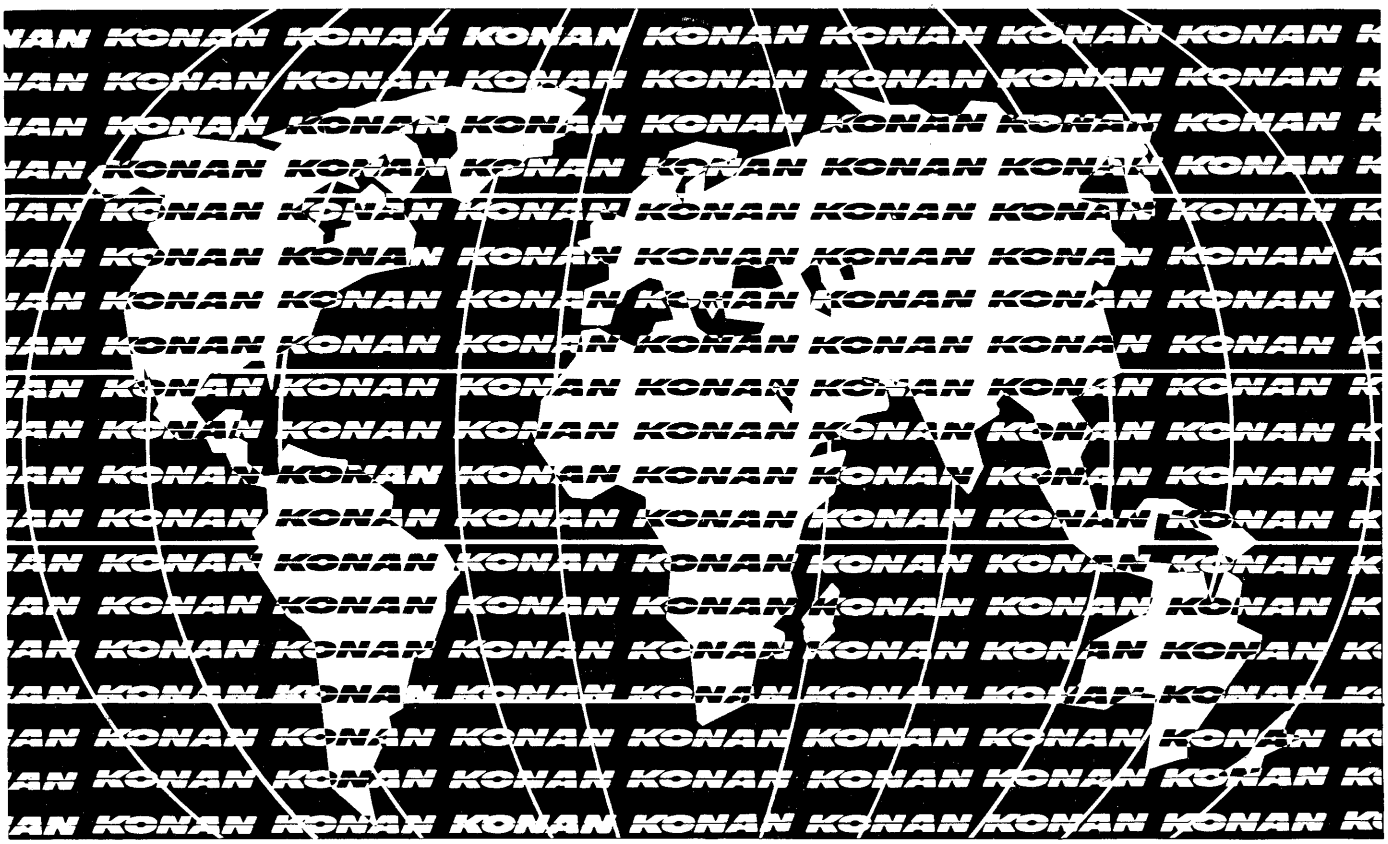


KONAN

THE WORLD IS UNDER OUR MASS STORAGE CONTROL

Konan Corporation, 1448 N. 27th Avenue, Phoenix, AZ 85009 • TWX/TELEX 9109511552
TOLL FREE ORDER LINE: 800-528-4563

DGC-100
O.E.M. REFERENCE MANUAL

Publication Date
11 February 1983

Publication No.
R-DGC-001-C

Warranty:

Subject to the conditions set forth below, KONAN will repair or replace, at its option, defective controllers and printed circuit board products (hereinafter referred to as "Product"), manufactured by KONAN. This warranty expires one year after the date of shipment from KONAN Corporation. A product shall be deemed defective only if it fails to perform to KONAN's published specifications.

If equipment is found to be defective during the warranty period, Buyer shall notify KONAN and request return authorization. The failed board should then be returned with the failure report attached, freight prepaid, to KONAN. The board will either be repaired or replaced, at KONAN's option, and returned to the customer, surface freight prepaid.

When buyer requests authorization from KONAN prior to the return of any board or equipment under the terms of this warranty, KONAN will promptly: (a) provide material return authorization tracer number(s) to be prominently displayed on all shipping containers containing the boards and/or equipment authorized for return, or (b) replace the affected parts or equipment under warranty without requiring their return by Buyer. This procedure is designed to help Konan Corporation provide you, the buyer, with high quality service. If your DGC-100 controller should require service, please follow this procedure exactly to ensure efficient service.

The above warranties are contingent upon proper use in the application for which equipment was intended and does not cover equipment which was modified without KONAN's approval or which was subjected to unusual physical or electrical abuse.

EXCEPT FOR THE EXPRESS WARRANTIES SET FORTH ABOVE, KONAN GRANTS NO OTHER WARRANTIES, EITHER EXPRESS OR IMPLIED, ON EQUIPMENT, INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS, AND THE STATED EXPRESS WARRANTY IS IN LIEU OF ALL LIABILITIES OR OBLIGATIONS OF SELLER FOR DAMAGES INCLUDING, BUT NOT LIMITED TO, CONSEQUENTIAL DAMAGES OCCURING OUT OF OR IN CONNECTION WITH THE USE OF OR PERFORMANCE OF KONAN'S PRODUCT.

Revision Sheet

Rev.	Release Date	Description of Revision
A	1981	Initial Release
B	Ø7/Ø7/82	Incoroporates description of functions
C	Ø2/15/83	New functionality

CONTENTS

CONTENTS

Section 1.Ø Introduction

1.1 Scope

1.2 Content

1.3 Product Description

1.4 Specifications

1.5 References

1.1 Scope:

The intent of this manual is to provide the user of the Konan DGC with all of the necessary data to integrate the product into their system.

1.2 Content:

The contents of this manual have been divided into six major sections. The six sections are as follows:

Section 1 - Introduction
Descibes the scope and content of the manual, and provides a generalized product description and specifications.

Section 2 - Installation
Describes the installation procedure, mounting and drive strapping.

Section 3 - Hardware Theory of Operation
Describes the DGC/disk drive interface.

Section 4 - Software Theory of Operation
Describes in detail the command set and general flow of command/parameter/data to and from DGC.

Section 5 - Maintenance
The Konan maintenance philosophy.

Section 6 - Appendix
This section contains additional information.

1.3 Product Description:

The Konan DGC is an intelligent 5-1/4" Winchester disk controller for the S-1ØØ Bus which meets the IEEE-696 specifications. The DGC can control up to two disk drives, with up to eight heads and 4Ø96 tracks. The command set for the DGC provides all of the required functions to interface the host computer to a standard 5 1/4" Winchester disk with minimum host software overhead.

1.4 Specifications:

Host Data Transfer (via S-100 Bus)
- 8-bit parallel
- 625K bytes per second maximum data rate

Disk Data Transfer
- modified frequency modulation
- pre-compensation 12 nsec
- 5 MHz data rate

Disk Control Capabilities
- 2 - units
- 8 - heads
- 4096 - track standard. The DGC will optionally address up to 32,000 tracks.

Cabling
- 34-pin disk control cable
- 20-pin disk data cable (drive 0)
- 20-pin disk data cable (drive 1)

Power Requirements
- +8 volts at 1.8 amps
- +16 volts at 0.1 amps

Board Dimensions
- 5" X 10"

Cooling

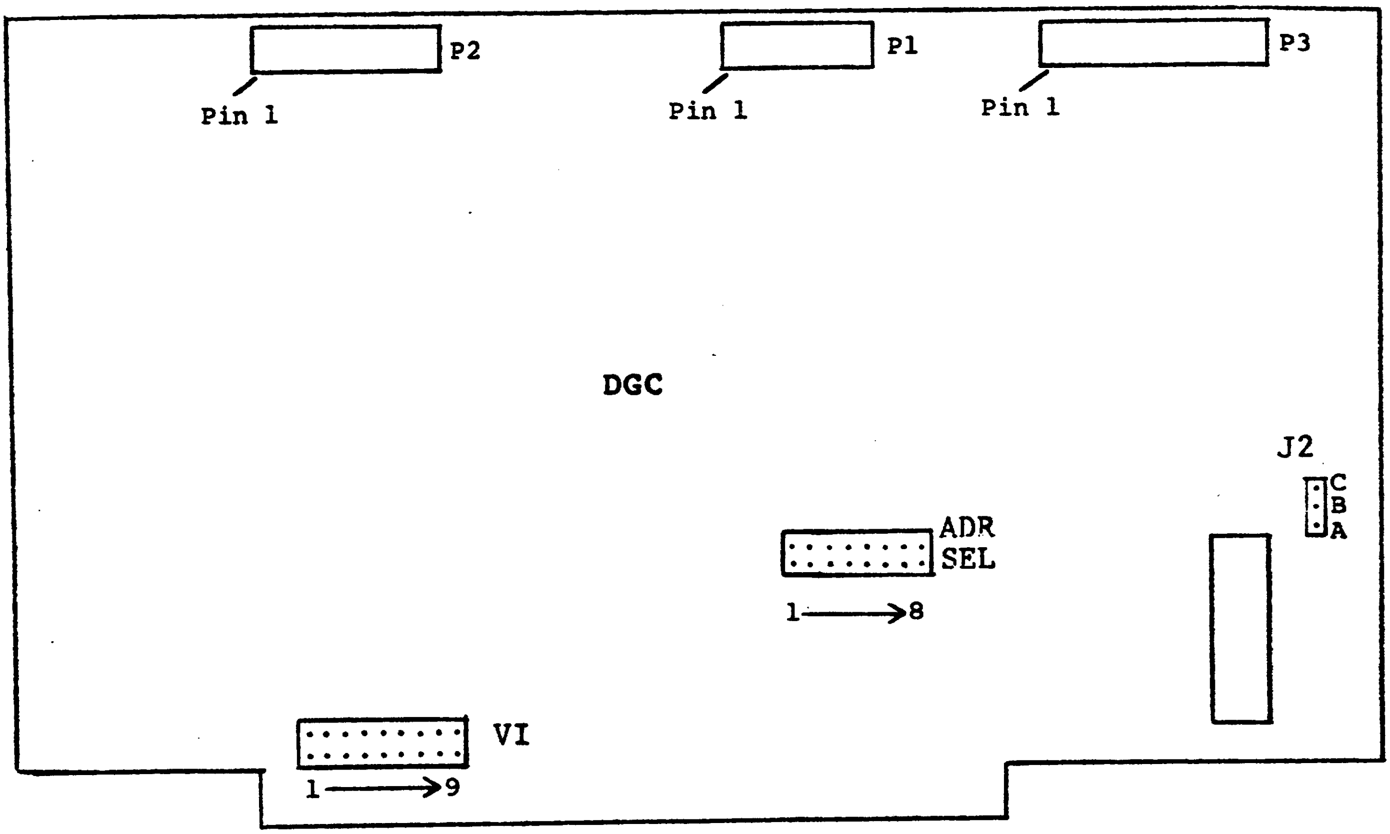
Forced cooling is suggested if the DGC-100 is enclosed in a restricted space.

1.5 References:

See operating manual of the particular disk to be interfaced to the DGC-100.

Section 2.0 Installation

2.1 Cables:



P1 20 pin Radial cable to Drive #0 - 3M# 3421-6000

P2 20 pin Radial cable to Drive #1 - 3M# 3421-6000

P3 34 pin Daisy chain cable - 3M# 3414-6000C (socket conn)
3M# 3463-0001 (edge conn)

2.2 Controller Strapping

VI 9 sets of jumper pins for interrupts (use only one jumper location)

POSITION	DESCRIPTION
1	$\overline{\text{VI0}}$
2	$\overline{\text{VI1}}$
3	$\overline{\text{VI2}}$
4	$\overline{\text{VI3}}$
5	$\overline{\text{VI4}}$
6	$\overline{\text{VI5}}$
7	$\overline{\text{VI6}}$
8	$\overline{\text{VI7}}$
9	$\overline{\text{INT}}$

ADR SEL 7 sets of jumper pins for I/O address selection. A jumper in position selects a Ø for that address line.

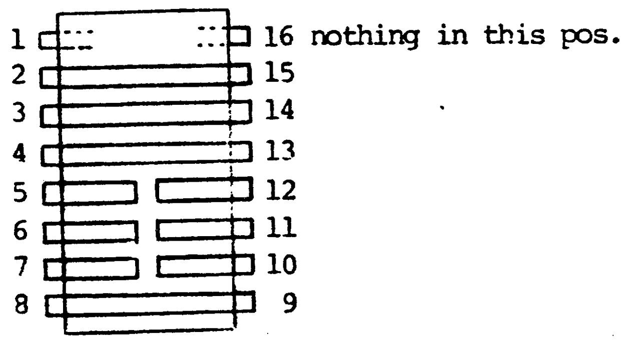
POSITION	DESCRIPTION
1	AØ
2	A1
3	A2
4	A3
5	A7
6	A6
7	A5
8	A4

J2 Selects either a 2716 or 2732 type EPROM in location U39. A jumper in the A-B position selects a 2732. A jumper in the B-C position selects a 2716.

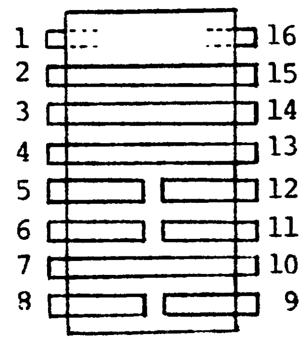
NOTE: The DGC as shipped is strapped for address 7D HEX. (i.e. jumpers #2 and #5 installed.

2.3 Drive Strapping

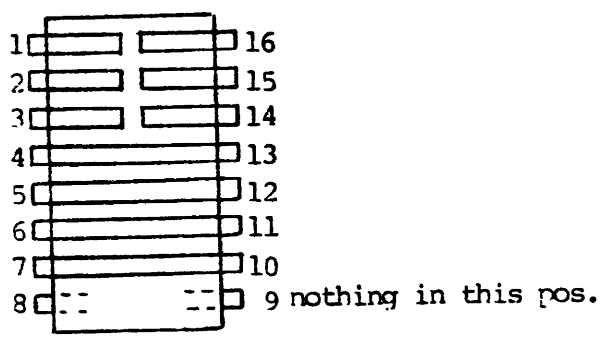
The drive must be strapped correctly to operate properly. Shown below is a strapping guide for some of the current disk drives. See the individual strapping guide for each manufacturer.



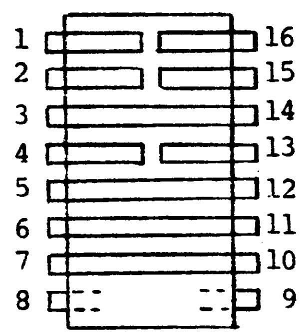
Seagate Technology
ST506 Drive #0 Strapping



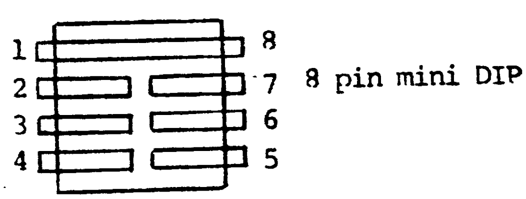
Seagate Technology
ST506 Drive #1 Strapping



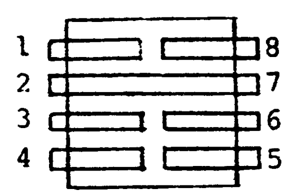
Texas Instruments
5¼" Drive #0 Strapping



Texas Instruments
5¼" Drive #1 Strapping



Rotating Memory Systems
RMS-500 Drive #0 Strapping



Rotating Memory Systems
RMS-500 Drive #1 Strapping

DISK DRIVE STRAPPING DIAGRAM
Figure 2.2

2.4 Drive Specifications

	SEAGATE ST-506	ROTATING MEMORIES RMS-512	COMPUTER MEMORIES CMS-5616
CAPACITY			
UNFORMATTED			
Per Drive	6.38	12.72	16.00
Per Surface	1.59	1.59	2.67
Per Track	10417	10417	10.4
FORMATTED			
Per Drive	5	10	12.6
Per Surface	1.25	1.25	2.1
Per Track	8192	8192	8.2
Per Sector	256	256	256
Sector/Track	32	32	32
TRANSFER RATE	5.0	5.0	5.0
ACCESS TIME			
Track to track	3ms	3ms	3ms
Average	170ms	70ms	105ms
Maximum	500ms	150ms	240ms
Settling time	15ms	15ms	17ms
LATENCY AVERAGE	8.33ms	8.33ms	8.3ms
FUNCTIONAL			
Rotational speed	3600	3600	3600
Recording density	7690	7700	8650
Flux density	7690	7700	8650
Track density	255	255	345
Cylinders	153	153	256
Tracks	612	1224	1536
Read/Write heads	4	8	6
Discs	2		3
Index	1	1	
RELIABILITY			
MTBF			
(POH typ. usage)	8000	8000	8000
P.M	none	none	none
MTTR (min.)	30	30	30
Component life	5 years	5 years	5 years

DRIVE SPECIFICATIONS (cont'd)

	SEAGATE ST-5Ø6	ROTATING MEMORIES RMS-512	COMPUTER MEMORIES CMS-5616
ERROR RATES			
Soft (Bits read)	$1/10^{10}$	$1/10^{10}$	$1/10^{10}$
Hard (Bits read)	$1/10^{12}$	$1/10^{12}$	$1/10^{12}$
Seek (Seeks)	$1/10^{6}$	$1/10^{6}$	$1/10^{6}$
REQUIREMENTS			
DC Voltage	+12VDC ±1Ø% 1.8A typical (4.5A start)	+12VDC ±1Ø% 1.3A typical (3.3A start)	+12VDC ±1Ø% 2.2A typical
	+5VDC ±5% .7A typical	+5VDC ±1Ø% .5A typical	+5VDC ±5% Ø.9A typical
AC Power	none req.	none req.	none req.
Ambient temp. range	5Ø° F to 115° F (1Ø C to 46 C)	5Ø° F to 115° F (1Ø C to 46 C)	5Ø° F to 115° F (1Ø C to 46 C)
Rel. Humidity range	8 to 8Ø%	8 to 8Ø%	8 to 8Ø%
Wet Bulb Max.	78° F non-cond	78° F non-cond	
Heat Diss.	3ØW(1Ø3 BTU/HR)	2ØW(66 BTU/HR)	31W(1Ø6 BTU/HR)

Section 3.Ø Hardware Theory of Operation

3.1 Disk/DGC Pin Out List

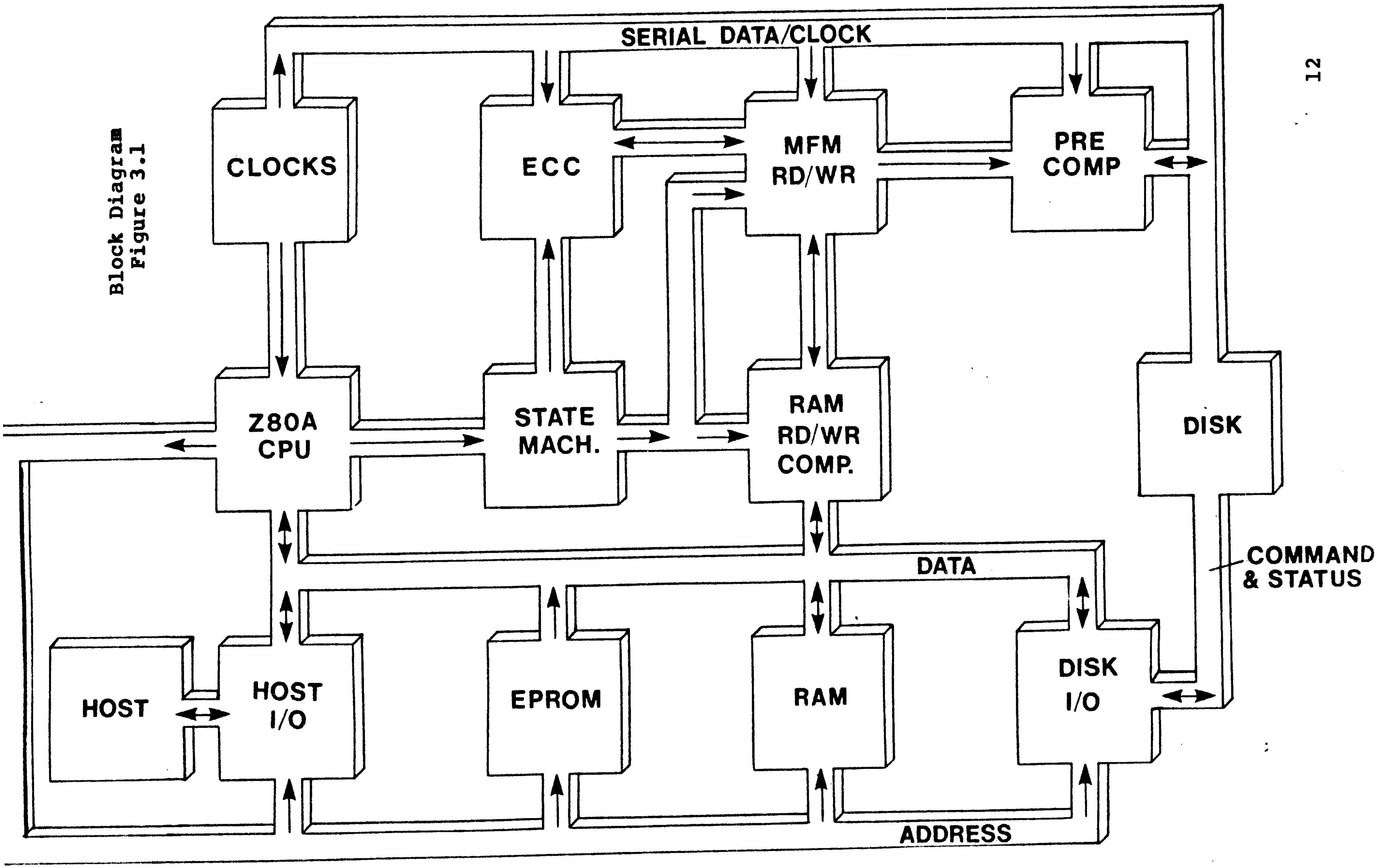
1	Drive Selected	2	GND
3	not connected	4	GND
5	not connected	6	GND
7	not connected	8	GND
9	not connected	1Ø	not connected
11	GND	12	GND
13	+MFM Write Data	14	-MFM Write Data
15	GND	16	GND
17	+MFM Read Data	18	-MFM Read Data
19	GND	2Ø	GND

DGC P1, P2 Disk Data Cable (Radial)

1	GND	2	Reduced Write Current
3	GND	4	Head Select Bit 2
5	GND	6	Write Gate
7	GND	8	Seek Complete
9	GND	1Ø	Track Ø
11	GND	12	Write Fault
13	GND	14	Head Select Bit Ø
15	GND	16	not connected
17	GND	18	Head Select Bit 1
19	GND	2Ø	Index
21	GND	22	Ready
23	GND	24	Step
25	GND	26	Drive Select Ø
27	GND	28	Drive Select 1
29	GND	3Ø	not connected
31	GND	32	not connected
33	GND	34	Direction In

DGC P3 Disk Control Cable (Daisy)

Block Diagram
Figure 3.1



Section 4.Ø Software Theory of Operation

4.1 Command Format

The commands have been divided into three major types which are described below. The high order nibble of the command byte contains the command type.

TYPE 0 COMMANDS - REQUIRE ONLY THE COMMAND BYTE TO BE ISSUED.
TYPE 2 COMMANDS - REQUIRE 8 BYTES TO BE TRANSFERRED.
TYPE 4 COMMANDS - REQUIRE SECTOR (256/512) BYTES TO BE TRANSFERRED.

Function	Command		Direction	Transfer
ABORT	01	HEX		NONE
INIT	02	"		NONE
INIT1	07	"		NONE
READ DISK	21	"	TO CNTRLR	8 BYTES
WRITE DISK	22	"	TO CNTRLR	8 BYTES
READ ID	23	"	TO HOST	8 BYTES
STATUS	24	"	TO HOST	8 BYTES
DRIVE STATUS	25	"	TO HOST	8 BYTES
FORMAT SPARE	26	"	TO CNTRLR	8 BYTES
FORMAT	27	"	TO CNTRLR	8 BYTES
SEEK	28	"	TO CNTRLR	8 BYTES
APPEND MAP	2A	"	TO CNTRLR	8 BYTES
READ BUFFER	41	"	TO HOST	EQUAL TO # OF BYTES IN SECTOR
WRITE BUFFER	42	"	TO CNTRLR	EQUAL TO # OF BYTES IN SECTOR

4.1.2 Address Format

In commands which include an 8 byte transfer from the host to the controller, unless otherwise specified follow the format below:

Byte #			
0	Unit Number	(0 or 1)	
1	Head Number	(0 --> 7)	
2	Track Low	(0 --> FF)	
3	Track High	(0 or 1)	
4	Sector	(0 --> F)	512 Byte Sectors
		or (0 --> 1F)	256 Byte Sectors
5	Reserved		
6	"		
7	"		

4.2 Command Sequence

In a typical command sequence, the command is issued using a simple handshake routine. Data/parameters are then transferred without any handshaking, making commands simple and fast. At the end of the transfer, a single byte of status is transmitted to the host. Following is a description of the flow chart of the command sequence. (Please refer to **COMMAND SEQUENCE**, Figure 4.1 on page 17).

On power up, the host should output a 00 to the DGC When a command is to be sent to the DGC, a subroutine with this sequence should be called.

1. Read the DGC port and wait for an "A0" hex byte. this indicates that the DGC is ready to receive a command.

2. Write the command byte to the DGC

3. Read the DGC port and wait for an "A1" hex byte. This indicates that the DGC has received the command which was just issued.

4. Write an "FF" hex byte to the DGC to allow it to execute the command.

5. Delay 50 micro-seconds. This allows the DGC time to set up in its internal DMA (Direct Memory Access) mode.

6. Do a transfer to/from the DGC if required.

7. Write an "FF" hex byte to the DGC

8. Delay 50us

9. Read the DGC and wait for an "FF" hex byte. This indicates the DGC is no longer in its internal DMA mode

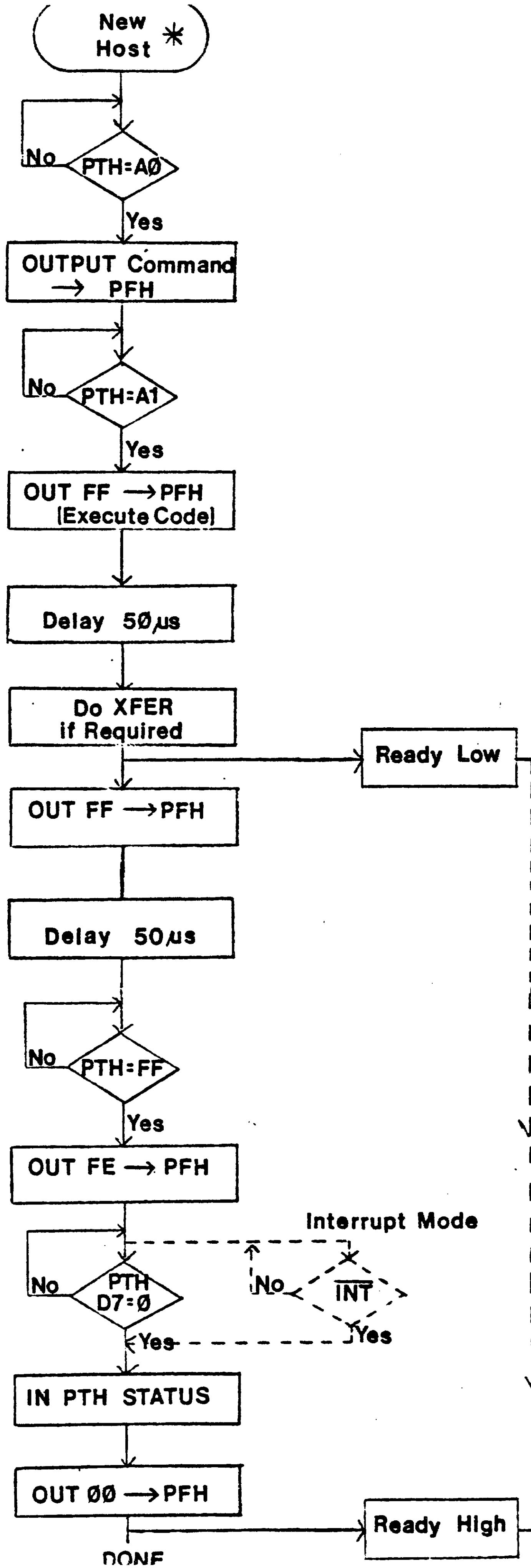
10. Write an "FE" hex byte to the DGC to indicate the host is ready for status.

11. Read the DGC and wait for data bit 7 (highest bit) to go low. When this occurs, the next byte read from the DGC will be the status byte.

12. Read the DGC to get the status byte.

13. Write a "00" hex byte to the DGC to indicate the status has been received, or the interrupt has been acknowledged.

COMMAND SEQUENCE
Figure 4.1



*Note: A ØØ Hex should be output → PFH on power-up.

PTH = To Host Port

PFH = From Host Port

The preceeding sequence is shown in two generalized routines, COMOUT (Command Out) and EXEC (Execute), written in 8Ø8Ø code below.

```
PTH      EQU     Ø7DH                        ;DGC READ PORT ADDRESS
PFH      EQU     Ø7DH                        ;DGC WRITE PORT ADDRESS


;THIS ROUTINE SENDS THE COMMAND IN REGISTER 'A' TO THE DGC

COMOUT:  MOV     B,A                         ;SAVE COMMAND (WAS IN 'A')
         XRA     A                           ;CLEAR DGC PORT (IN CASE IT
         OUT     PFH                         ;WASN'T ALREADY).
RDY1:    IN      PTH                         ;WAIT FOR THE DGC JR TO GO
         CPI     ØAØH                        ;READY.
         JNZ     RDY1
         MOV     A,B
         OUT     PFH                         ;SEND COMMAND
RDY2:    IN      PTH                         ;WAIT UNTIL THE DGC HAS IT
         CPI     ØA1H
         JNZ     RDY2
         MVI     A,ØFFH
         OUT     PFH                         ;SEND EXECUTE CODE
         MVI     A,18
RDY3:    DCR     A                           ;DELAY 5Ø MICRO-SECONDS
         JNZ     RDY3
         RET


;IF A DATA/PARAMETER TRANSFER IS REQUIRED FOR THIS COMMAND, DO IT NOW

EXEC:    MVI     A,ØFFH                      ;TRANSFER DONE
         OUT     PFH
         MVI     A,18
 EXO:    DCR     A
         JNZ     EXO
 EX1:    IN      PTH                         ;WAIT FOR DGC TO GET OUT OF
         CPI     ØFFH                        ;INTERNAL DMA MODE
         JNZ     EX1
         MVI     A,ØFEH                      ;SIGNAL THAT WE ARE READY FOR
         OUT     PFH                         ;STATUS
 EX2:    IN      PTH                         ;WAIT FOR STATUS BYTE TO GO READY
         ANI     8ØH
         JNZ     EX2
         IN      PTH                         ;GET STATUS
         MOV     B,A                         ;SAVE IT IN 'B'
         XRA     A
         OUT     PFH                         ;CLEAR THE DGC PORT
         RET
```

To show how to execute a simple series of commands with the DGC disk controller, the following routine reads Unit 0, Head 0, Track 0, Sector 0 from the disk and into the host's buffer. It uses the COMOUT and EXEC routines described above.

```
         MVI     A,21H           ;READ DISK COMMAND
         CALL    COMOUT
         XRA     A
         OUT     PFH             ;UNIT # 0
         OUT     PFH             ;HEAD # 0
         OUT     PFH             ;TRACK LOW = 0
         OUT     PFH             ;TRACK HIGH = 0
         OUT     PFH             ;SECTOR # 0
         OUT     PFH             ;RESERVED = 0
         OUT     PFH             ;RESERVED = 0
         OUT     PFH             ;RESERVED = 0
         CALL    EXEC            ;END COMMAND SEQUENCE

         LXI     H,1000H         ;LOAD ADDRESS
         MVI     A,41H           ;TO HOST DMA
         CALL    COMOUT          ;SEND IT
         LXI     B,200H          ;BC=NO.OF BYTES TO RETRIEVE (512)
RDDATA:  IN      PTH             ;GET DATA BYTE
         MOV     M,A             ;SAVE IN MEMORY
         INX     HL              ;INCREMENT MEMORY POINTER
         DCR     C               ;DECREMENT COUNT TILL DONE
         JNZ     RDDATA          ;DONE?
         DCR     B               ;DECREMENT LOW ORDER CNT
         JNZ     RDDATA          ;DONE?
         CALL    EXEC            ;END COMMAND SEQUENCE
         JMP     1000H           ;JUMP TO PROGRAM JUST
                                 ;LOADED FROM DISK
```

4.3 Status Byte

A single byte of status is provided by the DGC at the completion of each operation. If data bit six is low on status return, the operation was completed properly. If data bit six is high, a hard error occurred. The error codes are listed below.

ERROR CODE	TYPE		OPERATION
01	SOFT	HEADER	READ
03	SOFT	HEADER	WRITE
04	SOFT	DATA	READ
20	SOFT	DATA (CORRECTED)	READ
40	HARD	HEADER	READ
41	HARD	HEADER	READ ID
42	HARD	HEADER	WRITE
43	HARD	SEEK	SEEK
44	HARD	DATA	READ
45	HARD	WRITE PROTECTED	WRITE
46	HARD	WRITE FAULT	DRIVE SELECT
47	HARD	NOT READY	DRIVE SELECT
48	HARD	OUT OF SPARES	FORMAT
49	----	ILLEGAL COMMAND	COMMAND
4A	----	ACCESSED SPARE TRACK	READ/WRITE

```
D7   D6   D5   D4   D3   D2   D1   D0
!    !    !    !    !    !    !    !
!    !    !    !    !    !    !    !
!    !    !    !----!----!----!----!---------- ERROR CODE
!    !    !
!    !    !---------------------------------- CORRECTED DATA
!    !
!    !--------------------------------------- 0=OK  1=HARD ERROR
!
!-------------------------------------------- 0 INDICATES STATUS
                                                READY
```

4.4 Abort

Resets the controller to a power up state.

4.5 Read Buffer

The entire contents of the sector buffer (512/256 bytes) are transferred to the host.

4.6 Write Buffer

The entire contents of the sector buffer (512/256 bytes) are filled with the data transferred from the host.

4.7 Format

The format command can be used to format the entire disk, a complete surface, or a single track. Before sending a format command, the host system must first send a sector interlace list. NOTE: Format also assumes an Init command has been executed with the proper values. This is done with the write buffer command. The list begins with the first byte in the buffer data. The list's length is equal to the number of sectors on a track. The remainder of the write buffer data is zero filled. After transferring the interlace list using the write buffer command, the actual format command may be issued. The first parameter selects the unit . The unit number is followed by the head number. Valid head numbers are Ø - 7. To format more than one head with a single command, the head parameter byte can be modified to signal the head byte as a maximum value by setting the high order bit (D7) to a one. When D7 is a one for the head byte, the controller will format head zero through the maximum head number received from the host (starting with the max head). The third parameter byte in the format command is the track low byte. This is the low order portion of the track address. If it is desired to format more than one track (i.e., a surface or complete drive), this byte should equal the low order byte of the maximum track address. The fourth parameter byte is the high order track address. As in the low order track address byte, if a format drive or surface function is desired, this should be a maximum value. Valid high order track bytes are zero or one. If it is desired to format a complete surface, D7 of the high order track address (fourth parameter byte) should be set to a one. The fifth parameter byte is the number of sectors on a track - 1. The last three parameter bytes are zero. A typical format sequence follows.

Format Specifications:

```
  4 - HEADS
153 - TRACKS
 16 - SECTORS @ 512 BYTES/SECTOR
  1 - SECTOR INCREMENT VALUE
```

FILL 512 BYTE BUFFER AREA IN HOST WITH DATA. 16 SECTOR NUMBERS FOLLOWED BY 496 BYTES OF ZERO'S.

```
ØØ Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8 Ø9 ØA ØB ØC ØD ØE ØF
ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ
ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ
*                 *                 *                 *     512 BYTE DATA BUFFER
*                 *                 *                 *
*                 *                 *                 *
ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ ØØ
```

ISSUE A WRITE BUFFER COMMAND - 42 HEX

TRANSFER 512 BYTES

ISSUE A FORMAT COMMAND - 27 HEX

SEND 8 PARAMETER BYTES

```
ØØ HEX          FORMAT UNIT ZERO
83 HEX          FOMAT HEAD ZERO THROUGH 3
98 HEX          MAXIMUM TRACK NUMBER (LOW ORDER BYTE)
ØØ HEX          MAXIMUM TRACK NUMBER (HIGH ORDER BYTE)
ØF HEX          NUMBER OF SECTORS PER TRACK - 1
ØØ HEX          RESERVED
ØØ HEX          RESERVED
ØØ HEX          RESERVED
```

	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0
	H_2	H_1	H_0	S_4	S_3	S_2	S_1	S_0
*	$\overline{T_7}$/$\overline{T_B}$	$\overline{T_6}$/$\overline{T_A}$	$\overline{T_5}$/$\overline{T_9}$	$\overline{T_4}$/$\overline{T_4}$	$\overline{T_3}$	$\overline{T_2}$	$\overline{T_1}$	$\overline{T_0}$
	$\overline{T_8}$	$\overline{H_1}$	$\overline{H_0}$	$\overline{S_4}$	$\overline{S_3}$	$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$

If the currently selected head of the currently selected unit is positioned over a user track, the first four bytes returned from a Read ID command will be in the above form.

USER TRACK FORMAT
FIGURE 4.2A

	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	Physical Track Low
	T_8	1	0	1	1	H_2	H_1	H_0	Physical T_8, B_H and Head
*	$\overline{T_7}$/$\overline{T_B}$	$\overline{T_6}$/$\overline{T_A}$	$\overline{T_5}$/$\overline{T_9}$	$\overline{T_4}$/$\overline{T_4}$	$\overline{T_3}$	$\overline{T_2}$	$\overline{T_1}$	$\overline{T_0}$	Physical Track Low Not
	$\overline{T_8}$	1	0	1	1	$\overline{H_2}$	$\overline{H_1}$	$\overline{H_0}$	Physical T_8, B_H and Head Not

If the currently selected head of the currently selected unit is positioned over a spare track, the first four bytes returned from a Read ID command will be in the above form.

SPARE TRACK 58
FIGURE 4.2B

* Bit values following the slash are for tracks $\geq 512_{10}$

	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	New Track Low
	T_8	1	1	0	1	H_2	H_1	H_0	New T_8, D_H and New Head
*	$\overline{T_7}$/$\overline{T_B}$	$\overline{T_6}$/$\overline{T_A}$	$\overline{T_5}$/$\overline{T_9}$	$\overline{T_4}$/$\overline{T_4}$	$\overline{T_3}$	$\overline{T_2}$	$\overline{T_1}$	$\overline{T_0}$	New Track Low Not
	$\overline{T_8}$	1	1	0	1	$\overline{H_2}$	$\overline{H_1}$	$\overline{H_0}$	New $\overline{T_8}$, D_H and New Head Not
	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	Current Track Low
	H_2	H_1	H_0	S_4	S_3	S_2	S_1	S_0	Current Head/ Sector
*	$\overline{T_7}$/$\overline{T_B}$	$\overline{T_6}$/$\overline{T_A}$	$\overline{T_5}$/$\overline{T_9}$	$\overline{T_4}$/$\overline{T_4}$	$\overline{T_3}$	$\overline{T_2}$	$\overline{T_1}$	$\overline{T_0}$	Current Track Low Not
	$\overline{T_8}$	$\overline{H_1}$	$\overline{H_0}$	$\overline{S_4}$	$\overline{S_3}$	$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Current $\overline{T_8}$,$\overline{H_1}$,$\overline{H_0}$ and Sector Not

If the currently selected head of the currently selected unit is positioned over a bad track, the eight bytes returned from a Read ID command will be in the above form.

BAD TRACK FORMAT 68
FIGURE 4.2C

* Bit values following the slash are for tracks $\geq 512_{10}$

4.8 Read Disk

The read disk command causes the data in the sector addressed by the parameters following the command to be transferred to the sector buffer onboard the DGC. The data may then be transferred to the host by using the read buffer command. The eight byte transfer follows the address format described in Section 4.1.2.

4.9 Write Disk

The write disk command causes the data in the sector buffer to be transferred to the sector on the disk addressed by the parameters from the host. The eight-byte transfer follows the address format described in Section 4.1.2.

4.10 Format Spare

The format spare command follows the address format described in Section 4.1.2. The track of the specified unit and head will be formatted as a spare. The track address should be greater than the maximum user track address. This command need not be used if a format command is used with D7 of the head byte or D7 of the high order track byte set to a one.

4.11 Drive Status

The drive status command returns to the host the eight bytes below:

Byte #	Description
0	Drive 0 Status
1	Drive 1 Status
2	00
3	00
4	00
5	00
6	00
7	00

The drive status bytes are defined below:

```
D0   D1   D2   D3   D4   D5   D6   D7
I    I    I    I    I    I    I    I         _____________
I    I    I    I    I    I    I    I________ WRITE PROTECT
I    I    I    I    I    I    I              ______________
I    I    I    I    I    I    I_____________ DRIVE SELECTED
I    I    I    I    I    I
I    I    I    I    I    I__________________ USED INTERNALLY
I    I    I    I    I                        ___________
I    I    I    I    I_______________________ DRIVE READY
I    I    I    I                             _____
I    I    I    I____________________________ INDEX
I    I    I                                  ___________
I    I    I_________________________________ WRITE FAULT
I    I                                       _______
I    I______________________________________ TRACK 0
I                                            _____________
I___________________________________________ SEEK COMPLETE
```

4.12 Seek

Causes the heads on the specified unit to be moved to the track addressed in the eight-byte transfer. See Section 4.1.2.

4.13 Read I.D.

Reads the first header found on the current track of the last selected unit and head, and transfers this header data to the host. (See **HEADER FORMAT**, Figure 4.2 A,B and C).

4.14 Status

To be defined.

4.15 Append Map

A sector interlace pattern must be sent before append map (see Format, Section 4.7). The append map command requires an eight-byte transfer from the host, and follows the address format described in Section 4.1.2. The sector number is ignored. Upon receiving this command, the controller will search the addressed unit and head for a spare track. If none exists, an error code 48 will be returned to the host. If a spare is found, it will be reformatted as a user track. The bad track which was addressed in the eight-byte transfer will then be reformatted as bad with a pointer to the new user track. This command requires that the disk was previously formatted with mapping enabled, and a specified number of spares allotted at that time.

4.16 INIT

Upon power up, the DGC defaults to a standard set of drive control parameters. These parameters are listed below, along with the default values for power up. To change these parameters, the host must first do a write buffer command to the DGC with the list of bytes below starting at buffer address zero. The first 16 bytes transferred to the DGC are then the new parameter bytes with the remaining bytes zero filled. After the write buffer command, the parameters will now be in the DGC'S RAM buffer. Now an INIT command (single byte) must be issued to signal the DGC to move these values into the parameter area.

PRE-COMP SWITCH *	FFH
PRE-COMP LOW ORDER ADDRESS	20H
PRE-COMP HIGH ORDER ADDRESS	00H
REDUCE WRITE CURRENT SWITCH *	FFH
REDUCE WRITE CURRENT LOW ORDER ADDRESS	80H
REDUCE WRITE CURRENT HIGH ORDER ADDRESS	00H
STEP MODE (0=3ms,1=60us,2=FAST1,3=200us,4=FAST2)	00H
MAX TRACK LOW ORDER ADDRESS	98H
MAX TRACK HIGH ORDER ADDRESS	00H
SPARE-1 LOW ORDER ADDRESS	98H
SPARE-1 HIGH ORDER ADDRESS	00H
MAP SWITCH	FFH
RESERVED	00H
RESERVED	00H
RESERVED	00H
RESERVED	00H

* ALL SWITCHES: ON=0FFH, OFF=00H
FAST1 = SEAGATE FAST SEEK ALGORITHM
FAST2 = MINI SCRIBE FAST SEEK ALGORITHM

PRECOMP SWITCH: Byte 0
If this byte is 00, then all data is written to the disk with no pre-compensation added to the data. If this byte is FF Hex, all data to be written to the disk on track numbers less than the precomp address (see below) is written with no precompensation added to the data. All data to be written on track numbers greater than or equal to the precomp address will be written with ±12ns of shift in the data.

PRECOMP ADDRESS: Bytes 1 & 2
This is the two-byte address at which precompensation, if switched on, will start to be applied to data written to the disk. Track addresses less than precomp address will not receive precompensated data. Track addresses greater than or equal to precomp address will receive precompensated data if the precomp switch equals FF Hex. The low order precomp address byte is before the high order precomp address byte.

REDUCE WRITE CURRENT SWITCH: Byte 3
If this byte is 00, the reduce write current control line from the controller to the disk will never go active. If this byte is FF Hex, when accessing track number greater than or equal to the reduce write current address the reduce write current control line will be active to the disk.

REDUCE WRITE CURRENT ADDRESS: Bytes 4 & 4
This is the two-byte address at which the reduce write current control line, if switched on, will go active. Access to track numbers less than this address will result in the reduce write current control line going inactive.

STEP MODE: Byte 6
This byte sets the internal step mode of the controller. There are currently five step modes available. These are listed below, with their corresponding codes:

0	Standard 3ms Step Pulses
1	60us Step Pulses
2	Seagate Fast Seek Algorithm
3	200us Step Pulses

MAXIMUM TRACK ADDRESS: Bytes 7 & 8
This two-byte address is equal to the value of the last track on the disk.

MAXIMUM USER TRACK ADDRESS: Bytes 9 & 10
This two-byte address is equal to the value of the last user track on the disk (also equal to the address of the first spare track minus one).

MAP SWITCH: Byte 11
If this byte is 00, then the generation of spares, auto testing of the disk, and mapping of bad tracks during formatting of a unit, are disabled. If this byte is FF Hex, and a format command is issued with D7 of the head byte set to a one, then an automatic process of formatting user tracks, spare tracks, testing all user tracks and mapping any bad tracks to spare tracks is done. If D7 if head is not set and D7 of the High order track byte is set, then the spare tracks will be generated but no mapping will be done.

RESERVED: Bytes 12 Thru 15:
These bytes are reserved and their values (as well as the remainder of the buffer) should be 00.

LIST OF INIT PARAMETERS FOR VARIOUS DRIVES

Company	Model #	Max Head	Max Track	RWC	Precomp
Rodime	101	2	BF(191)	60(96)	0(0)
	102	4	BF(191)	60(96)	0(0)
	104	8	BF(191)	60(96)	0(0)
Miniscribe	1006	2	131(305)	98(153)	0(0)
	1012	4	131(305)	98(153)	0(0)
Texas Instruments	5-1/4	4	98(152)	40(64)	40(64)
Computer Memories	5205	2	FF(255)	OFF	OFF
		4	FF(255)	OFF	OFF
		6	FF(255)	OFF	OFF
Rotating Memory Systems	503	2	98(152)	4B(77)	4B(77)
		4	98(152)	4B(77)	4B(77)
		8	98(152)	4B(77)	4B(77)
Seagate Technology	506	4	95(152)	80(128)	20(32)

INIT1

The INIT command loads the desired parameters into the parameter area for both units. If the two units being controlled by the DGC-100 are different, then they may require different parameters. The INIT1 command is identical with the INIT command, except the parameters are loaded only into the unit #1 parameter area.

Section 5.Ø Maintenance, Returning Merchandise

5.1 Maintenance Philosophy

The DGC requires no preventative maintenance. The suggested method of repair is board replacement. If a board fails, it should be replaced with a good board and the faulty board returned to Konan for repair. All boards return for repair must have an RMA number. (See Section 5.2)

If a CP/M system is available, Konan will provide diagnostics to aid in determining if the DGC is operating properly.

5.2 Return Merchandise Authorization

Any merchandise being returned to Konan must have an RMA number. This number can be obtained by contacting the Konan Customer Service Department at (602) 269-2649.

Section 6.0 Diagnostics

6.1 Diagnostics

A CP/M floppy is available with diagnostics for the DGC It tests the DGC for correct data transfers, disk read, disk write, format, and header read functions.