

LOGIC SUMMARY - ALWAC III-E

This Logic Summary is addressed primarily to ALWAC trainees who wish to obtain a knowledge of the ALWAC III-E GENERAL PURPOSE DIGITAL COMPUTER.

This Logic Summary is not applicable in its entirety for each individual machine, but is intended to serve as a guide for the majority of ALWAC III-E Computers.

It would be appreciated if any errors, suggestions or additional information would be brought to the attention of the TRAINING BRANCH.

Revised by the TRAINING BRANCH 3 September 1958.

FLB/ic

TERMS FROM LOGIC TO CONTROL PANEL

1. Si
Ri
Ti (i = 1 through 8)

These terms either turn on or off the neon indicators in the S, R, and T registers on the control panel. The neons in the control panel are effectively tied in parallel to the neons on their corresponding flip flops.

2. F3, Mr, An, Bn, Dn, En, Vw, Wn, (Va Os' P33)

These terms come from the computer to the Register Selection Rotary Switch (ABDEWM) and are selected by the switch for oscilloscope synching and input Vw provides scope sync for all registers except for Main Memory (M). The term (Va Os' P33) provides scope sync for Main Memory observation. The terms An, Bn, Dn, En, Wn, and Mr are selected by the switch to provide vertical input to the scope for inspection of the A, B, D, E, Working Storage or Main Memory lines. F3 is also added to these latter terms to provide a pedestal on the scope sweep for easier observation of the word.

3. A2'

This term comes from the prime output of A2 flip flop. It goes to relay "O" in the control panel. When A2 flip flop is prime (indicating no block transfer alarm) relay "O" is de-energized, and the secondary of the buzzer transformer is open. When A2 flip flop is true, relay "O" is energized, completing buzzer circuit and sounding alarm.

4. A4'

This term comes from the prime output of A4 driver and operates in the manner described for A2', except that relay "P" is involved. A4 true means that the overflow is on and an arithmetic command is present in the "T" register. Under these circumstances the overflow alarm sounds. The computer remains in $\emptyset 1$ since Q3 will not come up while A4 is true.

$$Q3 = Ho (\emptyset 1 \text{ G } A2' \text{ A4}' \text{ P33})$$

TERMS FROM CONTROL PANEL TO LOGIC

1. Pti
Pri
Psi (i = 1 through 8)

By pushing the push button corresponding to a particular S, R or T neon indicator the associated flip flop may be either turned on or off.

This appears in the logic as:

$$Ti = Pti$$

$$Ti' = Pti'$$

2. Z trigger

Z' trigger

These terms appear in the logic as Pz and Pz'. Pz is triggered by the OVERFLOW ON punch switch and turns Z flip flop on if it is off.

Pz' is triggered by the OVERFLOW OFF punch switch and turns Z flip flop off if it is on.

The RESTORE position of the ALARM switch #2 is tied in parallel to the Z' trigger term so that Z flip flop is held prime.

3. Q2'

This term appears in the logic as PQ2. (Q2 = PQ2)

PQ2 comes up when the NORMAL - HOLD - SELECT switch is in the SELECT position.

4. Fo'

This term comes up when the NORMAL - HOLD - SELECT switch is in NORMAL position and is used in Q1 driver logic. Fo' allows normal sequencing.

5. Pgg

This term is associated with the ONE - STEP position of the NORMAL - STOP - ONE STEP switch. With this switch set to STOP position the computer cannot sequence out of $\phi 1$. Pgg turns Gg flip flop true in $\phi 1$. (Gg = Pgg). Gg flip flop is immediately turned off as the computer sequences into $\phi 2$. (Gg' = $\phi 1$ ' 0).

6. G

This term is associated with the NORMAL setting of the NORMAL-STOP-ONE STEP switch. As long as G is up (+15v) the computer will sequence normally.

7. Ho

This term will allow the computer to step through orders in normal sequence when the NORMAL-TEST-CLEAR switch is in TEST position. It is not necessary that the flexowriter be on.

8. Hof

The Hof term is a flexowriter term that comes to the control panel as well as to the logic directly. With the NORMAL-TEST-CLEAR switch in NORMAL position the Hof term is substituted for the Ho term and the computer is under control of the flexowriter.

Hof means flexowriter ON switch is in COMPUTE position.

9. S

This term is associated with the CLEAR position of the NORMAL-TEST-CLEAR switch. This term is "anded" with the clock in the logic cabinet and triggers several flip flops to call up MM channel 01 into WSI.

The term SC turns the following flip flops true.

T8 R1 ϕ 2 Yt

The term SC turns the following flip flops prime.

ϕ 0 ϕ 1 ϕ 3 ϕ 4 ϕ 5 ϕ 6 ϕ 7

S1 S2 S3 S4 S5 S6 S7 S8

R2 R3 R4 R5 R6 R7 R8

T1 T2 T3 T4 T5 T6 T7 E

Uk A2 Z Md Yp

10. Ss

This term is associated with the START position of the NORMAL-START switch. With a 1B command in the T register and the NORMAL-START switch in NORMAL position, the computer will not sequence out of ϕ 2.

$$Q3 = (T8' T7' T6' T5) T4 T3' \phi 2 P33 Uk$$

$$Uk = (T8' T7' T6' T5) T4 T3' T2 (\phi 2 P32 C) Ss$$

Ss then will allow the computer to transfer to the word designated in the R register.

11. SK1

This term is associated with Jump Switch #1.

In NORMAL position SK1 = 0v

In JUMP position SK1 = +15v

12. SK2

This term is identical to SK1 but is associated with Jump Switch #2.

13. Apr

This term is associated with the SILENCE position of Alarm Switch #1, and allows repeated block copying whenever an improper comparison is made.

$$Q3 = Apr Ut Q2 \phi 7 P33 Md' A2$$

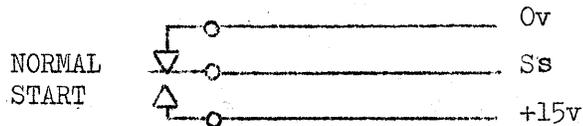
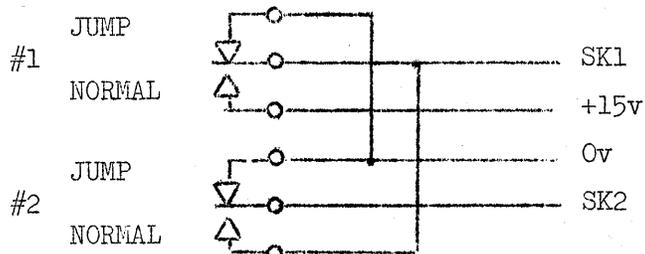
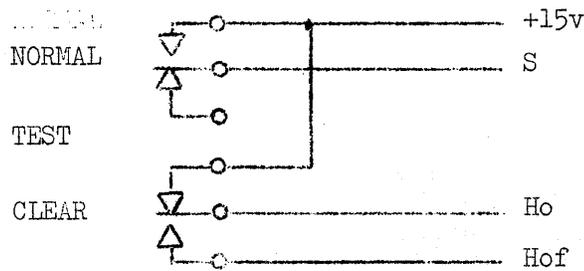
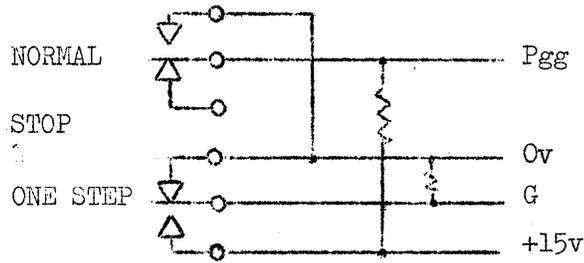
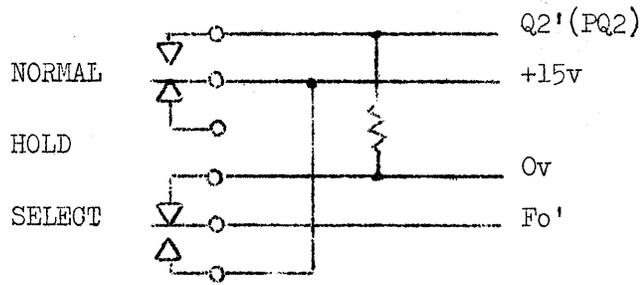
14. Ap2

This term is associated with the ~~RESTORE~~ position of Alarm Switch #1.

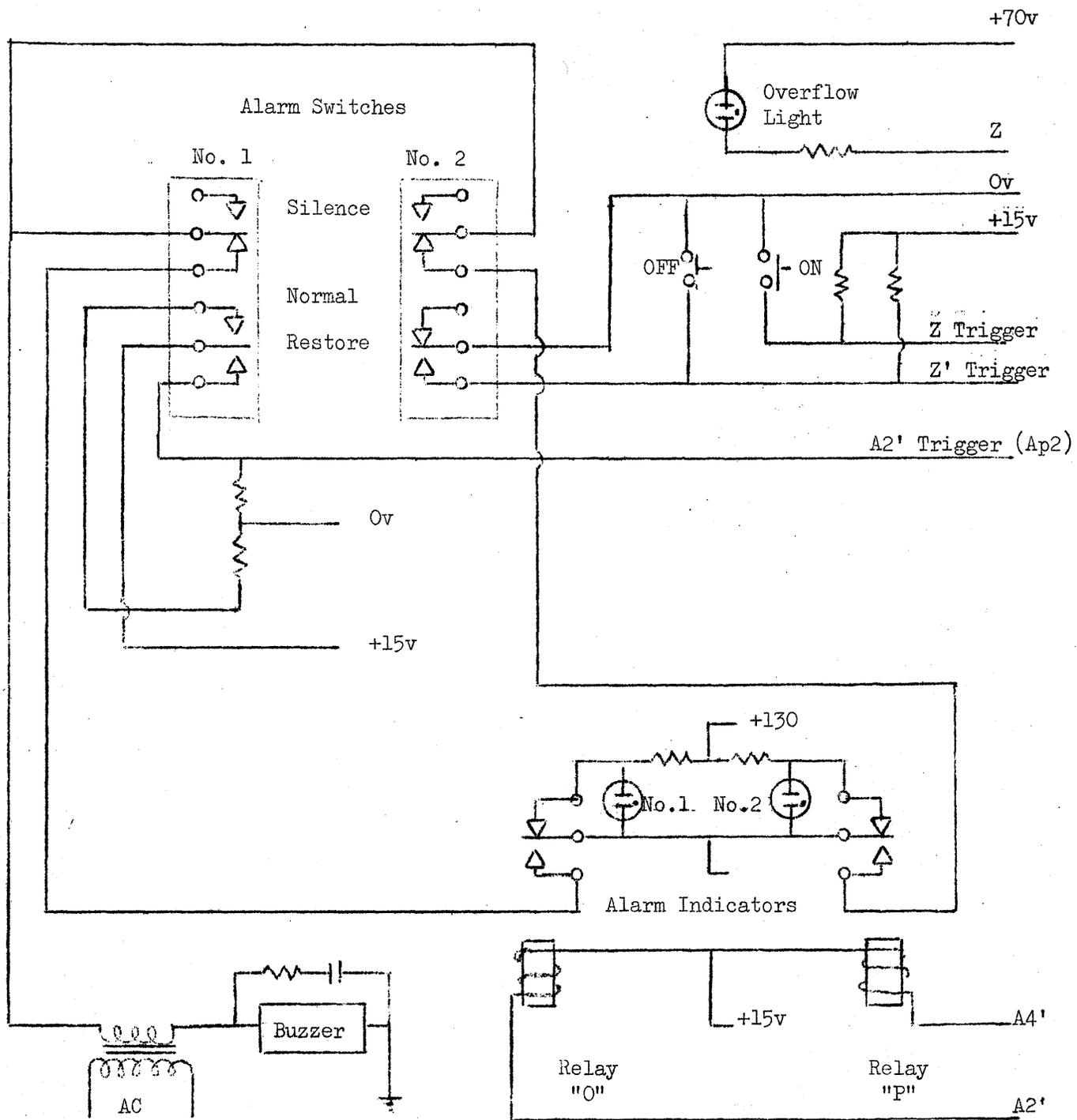
Ap2 turns A2 flip flop prime.

SWITCH POSITIONS AND THEIR LOGIC TERMS

1. Ap2 Restore position of Alarm #1 switch.
2. Apr Silence position of Alarm #1 switch.
3. Fo' Normal position of Normal-Hold-Select switch.
4. G Normal position of Normal-Stop-One Step switch.
5. Ho Test position of Normal-Test-Clear switch.
6. Hof Normal position of Normal-Test-Clear switch.
7. Pgg One-Step position of Normal-Stop-One Step switch.
8. PQ2 Select position of Normal-Hold-Select switch.
9. S Clear position of Normal-Test-Clear switch.
10. Sk1 Jump position of Jump #1 switch.
11. Sk2 Jump position of Jump #2 switch.
12. Ss Start position of Normal-Star' switch.



CONTROL PANEL SWITCHES



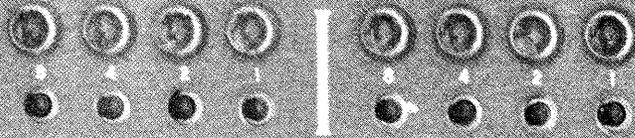
CONTROL PANEL SWITCHES

alwac III E

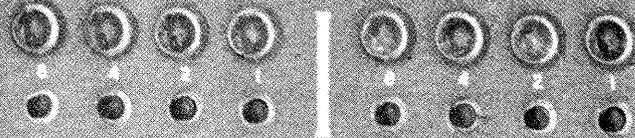
INSTRUCTION ADDRESS



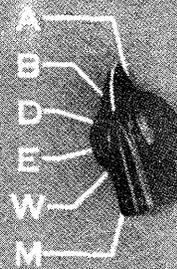
ADDRESS



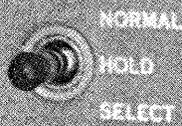
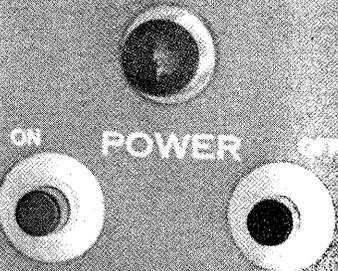
OPERATION



ALARMS



OVERFLOW



LOGISTICS RESEARCH LAB
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FUNCTIONS AND DEFINITIONS
OF ALWAC III-E PLUG-INS

In conjunction with this write up, refer to write up of "Terms to Control Panel".

Key:	DR	Driver
	FF	Flip Flop
	OS	One Shot
	PA	Pre-Amplifier for Selection Drivers
	RA	Read Amplifier
	WA	Write Amplifier
<u>Term</u>	<u>Ckt.</u>	
A2	FF	Used in conjunction with Block Transfer commands to indicate improper block copy. Used as protection against a Block Copy into Channel 01. "A2" prime, used in several equations for generating the Q3 driver term which is used for sequencing purposes. Refer also to "Terms To Control Panel" write up.
A4	DR	Alarm driver activated in "ø1" if a previous arithmetic operation generated an overflow, which is indicated by "Z" true during "ø1" time. Refer also to "Terms to Control Panel" write up.
Ab	FF	Follows "A" read amplifier in "A" recirculating line. Feeds Ae.
Ad	DR	Follows An during normal recirculation of "A" line. Controls information to "A" line depending upon command. Feeds Ar.
Ae	FF	Follows Ab. Feeds Ad during a right shift in "A" line. Feeds An during normal recirculation of "A" line. Feeds An during a left shift in "A" line. Feeds Q8 during certain copy operations. Used to check "early" time as compared to "now" time.
Al	FF	Follows An during a left shift in "A" line. Feeds Ad during a left shift in "A" line. Used to check "late" time as compared to "now" time.
An	FF	Follows Ae during normal recirculation or during a left shift of "A" line. Feeds Al during a left shift in "A" line. Used to indicate "now" time. Feeds Ad during normal recirculation of "A" line. Excluded during a right shift of "A" line. Used to output information from "A" line depending upon command. Used for oscilloscope vertical input when looking at the "A" line.

<u>Term</u>	<u>Ckt.</u>	
Ar	FF	Follows Ad. Feeds "A" write amplifier. Used to check "late" time as compared to "now" time.
Ar	RA	Follows output of "A" read head. Feeds Ab.
Aw	WA	Follows Ar FF. Feeds "A" write head to write information on the drum for "A" line.
B4	FF	Used for delay purposes during a "B5" order.
B5	FF	Used for delay purpose during a "B5" order.
	Note:	B4 and B5 used in conjunction with each other to count three drum revolutions.
Bb	FF	Follows "B" read amplifier in "B" recirculating line. Feeds Be.
Bd	DR	Follows Bn during normal recirculation of "B" line. Controls information to "B" line depending upon command. Feeds Br.
Be	FF	Follows Bb. Feeds Bd during a right shift in "B" line. Feeds Bn during normal recirculation of "B" line. Feeds Bn during a left shift in "B" line. Feeds QB during certain copy operations. Used to check "early" time as compared to "now" time.
Bl	FF	Follows Bn during a left shift in the "B" line. Feeds Bd during a left shift in "B" line. Used to check "late" time as compared to "now" time.
Bn	FF	Follows Be during normal recirculation or during a left shift of "B" line. Feeds Bl during a left shift in "B" line. Used to indicate "now" time. Feeds Bd during normal recirculation of the "B" line. Excluded during a right shift of the "B" line. Used to output information from "B" line depending upon command. Used for oscilloscope vertical input when looking at the "B" line.
Br	FF	Follows Bd. Feeds "B" write amplifier. Used to check "late" time as compared to "now" time.
Br	RA	Follows output of "B" read head. Feeds Bb.

<u>Term</u>	<u>Ckt.</u>	
Bw	WA	Follows Dr-FF. Feeds "B" write head to write information on the drum for "B" line.
Cd	DR	Amplifies, shapes and outputs clock pulses. The figure "C" is the clock pulse from the clock driver.
Cr	FF	Inter-lock during carriage return cycle. Timing delay in block transfer to allow Md relay to drop out, prior to reading back the written data for a comparison check.
Db	FF	Follows "D" read amplifier in "D" recirculating line. Feeds De.
Dd	DR	Follows Dn during normal recirculation of the "D" line, except during " ϕ_0 " look-up. Controls information to the "D" line depending upon command. Follows Dr during " ϕ_0 " look-up. During " ϕ_0 " 1st mode used in conjunction with other terms to modify incoming address going to "R" register. During " ϕ_0 " 2nd and 3rd modes used in conjunction with other terms to modify the address in "R" register while it recirculates when T1 is prime. During " ϕ_0 " 2nd and 3rd modes used to recirculate unmodified address from "R" register when T1 is true. Used in conjunction with other terms for counting operation during shift operations. Used in conjunction with other terms to generate a sum product, or difference depending upon command.
De	FF	Follows Db. Feeds Dn during normal recirculation of "D" line. Feeds Q8 during certain copy operations. Use to check "early" time as compared to "now" time.
Dn	FF	Follows De during normal recirculation of "D" line. Used to indicate "now" time. Feeds Dd during normal recirculation of "D" line, except during " ϕ_0 " when it feeds Dr. Used to output information from "D" line depending upon command. Used for oscilloscope vertical input when looking at the "D" line.
Dr	FF	Follows Dd during normal recirculation, except during " ϕ_0 " when it follows Dn. Feeds "D" write amplifier.
Dr	RA	Follows the output of "D" read head. Feeds Db.
Dw	WA	Follows Dr FF. Feeds "D" write head to write information on the drum for "D" line.
Eb	FF	Follows "E" read amplifier in "E" recirculating line. Feeds Ee.

<u>Term</u>	<u>Ckt.</u>	
Ee	FF	Follows Eb. Feeds En during normal recirculation of "E" line. Feeds Q8 during certain copy operations.
En	FF	Follows Ee during normal recirculation of "E" line. Feeds Er during normal recirculation of "E" line. Used to indicate "now" time. Used to output information from "E" line depending upon command. Used for oscilloscope vertical input when looking at "E" line.
Er	FF	Follows En during normal recirculation of "E" line. Controls information to "E" line depending upon command. Follows Ws driver during least significant half word time (LSH) 1st and 3rd modes of "00" look-up.
Er	RA	Follows the output of "E" read head. Feeds Eb.
Ew	WA	Follows Er FF. Feeds write head to write information on the drum for "E" line.
F1	FF	Used in "F" counter circuit to count down the "clock" by two.
F2	FF	Used in "F" counter circuit to count down the output of the F1 FF by two, except at Po time and P33 time.
F3	FF	Used in the "F" counter circuit to count down a word into quarters. Also used to distinguish between Po and P33 time. "F3" true: instruction portion of a word or Po time. "F3" prime: address portion of a word or P33 time.
F4	FF	Used in the "F" counter circuit to divide a whole word (34 bits) into half words. "F4" prime: Po thru P16 inclusively is the least significant half (LSH) word. "F4" true: P17 thru P33 inclusively is the most significant half (MSH) word.
F5	FF	Used in the "F" counter circuit. Used to indicate "word identification portion" of words on the "F" line. "F5" true: during P28, P29, P30, P31 and P33. "F5" prime: the remaining pulse times in a word.
F	FF	Used in the "F" counter circuit. Follows the Fb FF.
Fb	FF	Follows the "F" read amplifier. Feeds the "F" FF.
Fr	RA	Follows the output of "F" read head which in turn is following the permanently recorded "F" line on the drum.

<u>Term</u>	<u>Ckt.</u>	
Fr'	FF	Used to tell the computer the flexowriter is or is not busy. "Fr" prime: indicates flex is not busy (actually a true output). "Fr" true: indicates flex is busy (actually a prime output). Follows the Fr' DR.
Fr'	DR	Used in conjunction with the Fr' FF to tell the computer the flexowriter is or is not busy. Receives its information from the flexowriter.
Fw'	FF	Fw' means flexowriter is not busy. Follows the Fw' DR.
Fw'	DR	Triggers the Fw' FF. Receives its information from either the flexowriter, or the H.S.P. Tape Unit.
Go	OS	Used as an inter-lock signal to prevent outputs during a programmed carriage return.
G1-G6	OS	Operate the flexowriter punch and/or translator.
Gg	FF	Turned on by (Pgg) when the NORMAL-STOP-ONE STEP-SWITCH is moved from the STOP to the ONE STEP position. Allows computer to sequence one order at a time.
H1	FF	Follows He in "HI" recirculating line. Feeds H2.
H2	FF	Follows H1 during normal recirculation of "HI" line, except at P32 time when it follows He. Feeds H3 during normal recirculation of "HI" line. Used to output "one word" of information from "HI" line depending upon command. Used in conjunction with Mr to check "block transfers" into or out of "HI" line.
H3	FF	Follows H2 during normal recirculation of "HI" line. Follows Mr during "block transfers" into "HI" line. Follows Q8 during "one word" copies into "HI" line. Feeds Hw.
Hb	FF	Follows "H" read amplifier in "HI" recirculating line. Feeds He.
He	FF	Follows Hb. Feeds H1. Feeds Mp and Mo during a "block transfer" from "HI" line. (WSI)
Hr	RA	Follows output of "H" read head. Feeds Hb.
Hw	WA	Follows H3. Feeds "H" write head which writes information on the drum for "HI" recirculating line.

<u>Term</u>	<u>Ckt.</u>	
I2	FF	Follows Ib. Feeds I3 during normal recirculation of "HI" line. Used to output "one word" of information depending upon command.
I3I3	FF	Follows I2 during normal recirculation of "HI" line. Follows Q8 during "one word" copies into "HI" line. Feeds Iw.
Ib	FF	Follows Ir. Feeds I2.
Ir	RA	Follows output of "I" read head. Feeds Ib.
Iw	WA	Follows I3. Feeds "I" write head which writes information on the drum for the "HI" recirculating line.
J1	FF	Follows Je in "JK" recirculating line. Feeds J2.
J2	FF	Follows J1 during normal recirculation of "JK" line, except at P32 time when it follows Je. Feeds J3 during normal recirculation of "JK" line. Used to output "one word" of information from "JK" line depending upon command. Used in conjunction with Mr to check "block transfers" into or out of "JK" line.
J3	FF	Follows J2 during normal recirculation of "JK" line. Follows Mr during "block transfers" into "JK" line. Follows Q8 during "one word" copies into "JK" line. Feeds Jw.
Jb	FF	Follows "J" read amplifier in "JK" recirculating line. Feeds Je.
Je	FF	Follows Jb. Feeds J1. Feeds Mp and Mo during a "block transfer" from "JK" line. (WSII)
Jr	RA	Follows output of "J" read head. Feeds Jb.
Jw	WA	Follows J3. Feeds "J" write head which writes information on the drum for "JK" recirculating line.
K2	FF	Follows Kb. Feeds K3 during normal recirculation of "JK" line. Used to output "one word" of information depending upon command.
K3	FF	Follows K2 during normal recirculation of "JK" line. Follows Q8 during "one word" copies into "JK" line. Feeds Kw.

<u>Term</u>	<u>Ckt.</u>	
Kb	FF	Follows Kr. Feeds K2.
Kr	RA	Follows output of "K" read head. Feeds Kb.
Kw	WA	Follows K3. Feeds "K" write head which writes information on the drum for the "JK" recirculating line.
L1	FF	Follows Le in "LM" recirculating line. Feeds L2.
L2	FF	Follows L1 during normal recirculation of "LM" line, except at P32 time when it follows Le. Feeds L3 during normal recirculation of "LM" line. Used to output "one word" of information from "LM" line depending upon command. Used in conjunction with Mr to check "block transfers" into or out of "LM" line.
L3	FF	Follows L2 during normal recirculation of "LM" line. Follows Mr during "block transfers" into "LM" line. Follows Q8 during "one word" copies into "LM" line. Feeds Lw.
Lb	FF	Follows "L" read amplifier in the "LM" recirculating line. Feeds Le.
Le	FF	Follows Lb. Feeds L1. Feeds Mp and Mo during a "block transfer" from "LM" line. (WS III)
Lr	RA	Follows output of "L" read head. Feeds Lb.
Lw	WA	Follows L3. Feeds "L" write head which writes information on the drum for "LM" recirculating line.
M2	FF	Follows Mb. Feeds M3 during normal recirculation of "LM" line. Used to output "one word" of information depending upon command.
M3	FF	Follows M2 during normal recirculation of "LM" line. Follows Q8 during "one word" copies into "LM" line. Feeds Mw.
Mb	FF	Follows Mr. Feeds M2.
Md	FF	Controls the configuration of Md relay through Pa Md, for reading out of, or writing into Main Memory. "Block Transfers".
Me	FF	Drives memory write amplifier for "O's". Follows He, Je, Le or Ne depending upon command.

<u>Term</u>	<u>Ckt.</u>	
Mp	FF	Drives memory write amplifier for "l's". Follows He, Je, Le or Ne depending upon command used.
Mr	FF	Used in the Ferranti system for "block transfers" from MM to WS. Used to check the validity of block transfers between MM and WS. Used for oscilloscope vertical input when observing contents of "one word" in Main Memory.
Mr	RA	Follows M3. Feeds Mb.
Mw	WA	Follows M3. Feeds "M" write head which writes information on the drum for "LM" recirculating line.
N1	FF	Follows Ne in the "NO" recirculating line. Feeds N2.
N2	FF	Follows N1 during normal recirculation of "NO" line, except at P32 time when it follows Ne. Feeds N3 during normal recirculation of "NO" line, depending upon command. Used in conjunction with Mr to check "block transfers" into or out of "NO" line. Used to output "one word" of information depending upon command.
N3	FF	Follows N2 during normal recirculation of "NO" line. Follows Mr during "block transfers" into "NO" line. Follows Q8 during "one word" copies into "NO" line.
Nb	FF	Follows "N" read amplifier in "NO" recirculating line. Feeds Ne.
Ne	FF	Follows Nb. Feeds N1. Feeds Mp and Mo during a "block transfer" from "NO" line. (WS IV)
Nr	RA	Follows output of "N" read head. Feeds Nb.
Nw	WA	Follows N3. Feeds "N" write head which writes information on the drum for "NO" recirculating line.
O2	FF	Follows Ob. Feeds O3 during normal recirculation of "NO" line. Used to output "one word" of information depending upon the command.
O3	FF	Follows O2 during normal recirculation of "NO" line. Follows Q8 during "one word" copies into "NO" line. Feeds Ow.
Ob	FF	Follows Or. Feeds O2.

<u>Term</u>	<u>Ckt.</u>	
Or	RA	Follows output of "O" read head. Feeds Ob.
Ow	WA	Follows O3. Feeds "O" write head which writes information on the drum for "NO" recirculating line.
Po	FF	Used in the "F" counter circuit. "Po" true during Po time of a word. "Po" prime during the remaining 33 pulse times of a word. Basically a timing term, used to specifically exclude or work with the Po (sign) bit of a word. "First pulse of a word".
P1	FF	Used in the "F" counter circuit. "P1" true during P1 time of a word. "P1" prime during the remaining 33 pulse times of a word. Basically a timing term. "First pulse of the magnitude portion of a word".
P32	FF	Used in the "F" counter circuit. "P32" true during P32 time of a word. "P32" prime during the remaining 33 pulse times of a word. Basically a timing term. "Last pulse of the magnitude portion of a word."
P33	FF	Used in the "F" counter circuit. "P33" true during P33 time of a word. "P33" prime during the remaining 33 pulse times of a word. Basically a timing term. "Used to specifically exclude or work with the P33 (Overflow) bit of a word." "Thirty-fourth pulse of a word."
Pal-8	SD	Used to activate the MM selection drivers.
PaMd	DR	Used to activate Md relay to set either reading or writing conditions for Main Memory.
PaYd	DR	Interlock signal between Flexowriter and the computer that indicates the flexowriter is asking for inputs. Helps choose between inputs from the HSPTR or the flexowriter.
Q1	DR	During "Ø0" 1st and 3rd modes used to gate information to the LSH of the "E" line. During "Ø0" all modes used to condition subtractor circuitry. During "Ø0" 1st mode used to condition parallel transfer circuitry between the "T" and "R" registers. During "Ø0" all modes used to condition "serial" pump across" circuitry in the "T" and "R" register. (1 thru & FF's). During "Ø0" all modes used to gate information to the T8 and R8 FF's. During "Ø0" all modes used to condition the Q3 driver.
Q2	DR	Operate selection driver pre-amplifiers which in turn operate selection drivers that control the relays in the matrix.
Q3	DR	Advances "Ø" sequence counter, or resets it to Ø3 if the computer is in Ø7.

<u>Term</u>	<u>Ckt.</u>	
Q4	DR	Resets "Ø" sequence counter to "Ø0". Terminates the execution of commands. Used in conjunction with (Uk C) to cause a parallel transfer between the "R" and "S" register. Sets Va to prime configuration.
Q6	DR	Conditions copying equations during the execution of various commands.
Q7	DR	Conditions copying equations during the execution of various commands.
Q8	FF	Follows Ae, Be, De or Ee during certain copying operations depending upon command. Feeds H3, I3, J3, K3, L3, M3, N3 or O3 during some copying operations depending upon command and timing. Used during input commands for timing and delay purposes.
R1	FF	Compared with the P28 pulse on the "F" line during a data word look-up (Ø2).
R2	FF	Compared with the P29 pulse on the "F" line during a data word look-up (Ø2).
R3	FF	Compared with the P30 pulse on the "F" line during a data word look-up (Ø2).
R4	FF	Compared with the P31 pulse on the "F" line during a data word look-up (Ø2).
R5	FF	Compared with the P33 pulse on the "F" line during a data word look-up (Ø2).
R6	FF	Used in conjunction with R7 and Or to select the particular WS channel a data word is stored (Ø2).
R7	FF	Used in conjunction with R6 and Or to select the particular WS channel a data word is stored (Ø2).
R8	FF	Used for address purposes in conjunction with R1 thru R7 FF's. The "R" register determines a particular type of operation to be performed in conjunction with magnetic tape and input output commands.

NOTE: These FF's compose the address "R" register.
The "R" register has various functions according to the command used.
It contains the address of data to be used in conjunction with the execution of various commands.
It contains the address where data is to be stored when used with various commands.
It contains the number of shifts to be executed when used with shift commands.
It contains the second command to be executed when used in conjunction with "packed" commands.
It contains the number of characters to be taken in or outputted when used with input output commands.

<u>Term</u>	<u>Ckt.</u>	
		It contains the MM channel to which or from which information is to be copied when used with "block transfer" commands.
S1	FF	Compared with the P28 pulse on the "F" line during an instruction word look-up (ϕ_0).
S2	FF	Compared with the P29 pulse on the "F" line during an instruction word look-up (ϕ_0).
S3	FF	Compared with the P30 pulse on the "F" line during an instruction word look-up (ϕ_0).
S4	FF	Compared with the P31 pulse on the "F" line during an instruction word look-up (ϕ_0).
S5	FF	Compared with the P33 pulse on the "F" line during an instruction word look-up (ϕ_0).
S6	FF	Used in conjunction with S7 and Θ_s to select a particular WS channel an instruction word is stored (ϕ_0).
S7	FF	Used in conjunction with S6 and Θ_s to select a particular WS channel an instruction word is stored (ϕ_0).
S8	FF	Conditions circuitry to deal with a particular half of an instruction word. "S8" prime: indicates most significant half (MSH) word to be processed first. "S8" true: indicates least significant half (LSH) word to be processed first.
	NOTE:	These FF's compose the instruction address "S" register. The "S" register contains the address of the instruction word. When looking at a visual display of a word located in the main memory the "S" register contains the words relative location to the "F" line.
T1	FF	During " ϕ_0 " look-up 2nd and 3rd modes T1 will indicate whether a modified or unmodified address is to be used in conjunction with an order. "T1" prime: indicates a modified address to be used. "T1" true: indicates an unmodified address to be used.
T2-T8	FF	Contains after " ϕ_0 " time the order being executed. Contains during " ϕ_0 " look up 1st mode, before F4 time the unmodified incoming address.
	NOTE:	These FF's compose the operation "T" register.
Ua	FF	Used as a carry FF for Add, Binary round and Multiplication orders. Used as a borrow FF in Subtract and Division orders. Used in some orders to condition "Q4" DR for sequencing.

<u>Term</u>	<u>Ckt.</u>	
Ub	FF	Used as a coupling device between the "A" and "B" recirculating lines in Double Length Shifting, Multiply, Divide and Binary round orders. Holds least significant digit of intermediate product or dividend for Multiply or Divide orders.
Uc	FF	Used as carry FF during Multiply orders. Used for timing device in "ø" look-up. (Turned on at the fall of P24; off at P25) Used as a carry FF in an AB order.
Ud	FF	Used to make magnitude comparisons between the dividend and divisor in a Division order.
Ue	FF	Used as the borrow FF during "ø" lock up. Used as an interlock for output orders.
Uk	FF	Used to tell the computer to jump or not. "Uk" true: indicates a jump condition. "Uk" prime: indicates a no jump condition.
Um	FF	Used as a sequencing control in shifting orders.
Ur	FF	Makes final decision in whether to shift and subtract or merely shift during a Division order. "Ur" true: indicates shift and subtract. "Ur" prime: indicates shift only. Also Ur's configuration is inserted in the "B" line at P1 which in turn is generating the quotient in a Division order.
Us	FF	Used as a control in an Add or Subtract order according to the configuration of the signs. Used in some orders to condition "Q4" DR for sequencing.
Ut	FF	Used to determine whether an addition and a shift will take place or merely a shift operation during the Multiply command. "Ut" true: indicates an add and shift condition. "Ut" prime: indicates a shift only. Used for timing in block transfer commands.
Uv	FF	Used as a borrow FF during Divide orders.
Va	FF	Used for conditioning "Q1" Driver during "ø" look-up.
V _o	FF	Turns on at the fall of P33 time in words 10 thru 1F on the "F" line. (V _o P33) occurs once per drum revolution, at the fall of P33 of word "00" on the "F" line. Used for timing purposes during block transfer commands.
Vr	FF	Used in comparison check between the R1 thru R4 FF's with the P28 thru P31 bits on the "F" line. "Vr" true: indicates a matching condition between all of the bits on the "F" line and the R1 thru R4 FF's. "Vr" prime: indicates a mismatch during one of the particular bit times P28 thru P31 on the "F" line and R1 thru R4 FF's. If Vr is on at P33 time Vw will be turned on.

<u>Term</u>	<u>Ckt.</u>	
Vs	FF	Turned true at the fall of P24 every word time. Compares S1 thru S4 with the P28 thru P31 bits on the "F" line. "Vs" true: indicates proper match between the S1 thru S4 FF's and the P28 thru P31 bits on the "F" line. "Vs" prime: indicates a mismatch between one of the S1 thru S4 FF's and the P28 through P31 bits on the "F" line. If Vs is on at P33 time Va will be turned on.
Vw	FF	Used to condition copy equations during and after " ϕ 2" look-up. Used for timing purposes in the Multiply and Divide orders. Used for oscilloscope synching.
Wn	DR	Follows information in WS specified by the "R" register during " ϕ 2" look-up. Used for oscilloscope vertical input when observing one word in working storage.
Ws	DR	Follows information in WS specified by the "S" register during " ϕ 0" look-up.
Xl	FF	Used as the comparison FF during block transfer commands. "Xl" true: indicates a proper block copy. "Xl" prime: indicates an improper block copy.
Y1-Y6	FF	Intermediate storage between the flexowriter and the HSPTR and the "A" line during input/output commands. Multiplied by 10 during conversion orders.
Yp	FF	Used in conjunction with the punch relay in the flexowriter. "Yp" true: indicates a punching operation. "Yp" prime: indicates no punching operation.
Yt	FF	Used in conjunction with the type relay in the flexowriter. "Yt" true: indicates a typing operation. "Yt" prime: indicates no type operation.
Z	FF	Used for indicating overflow conditions in arithmetic commands. "Z" true: indicates an overflow condition present. "Z" prime: indicates no overflow condition present. Used for magnitude check between the "A" and "D" lines in Divide double length orders.
ϕ 0	FF	" ϕ 0" true: indicates the computer is looking up an instruction word.
ϕ 1	FF	" ϕ 1" true: indicates idling condition. During " ϕ 1" an alarming condition may occur if a previous arithmetic command has generated an overflow and another arithmetic command is now trying to be executed. During " ϕ 1" the "S" register counts its normal cycle.
ϕ 2	FF	" ϕ 2" true: indicates the computer may be looking up a data word indicated by address in the "R" register. Orders that do not involve a data look-up (ϕ 2) may be executed during this time.

<u>Term</u>	<u>Ckt.</u>	
$\phi_3-\phi_7$	FF	Various sequential states of the computer where certain functions are performed according to the order being executed.
Θ_r	FF	Determines from which half of a particular working storage line the data word is to be read from. Θ_r 's configuration depends upon the configuration of R5 and the P33 bit on the "F" line.
Θ_s	FF	Determines from which half of a particular WS line an instruction word is to be read. Its configuration depends upon the configuration of the S5 and the P33 bit on the "F" line. Turned prime at the fall of P32 every word time.

FLEXOWRITER TERMS

The computer logic provides input signals to the Flexowriter for certain operations.

- G1 through G6 One Shots provide signals to operate the translator or punch solenoids.
- Go one shot provides a delay signal to prevent type out during initial part of Flexowriter carriage return.
- Yd selection driver provides the signal to operate K401 in the Flexowriter. K401, when energized, provides power to the common side of SC contacts, and a ground path for the Reader cycle solenoid (LAC). K401 also turns on the Flexowriter ready light.
- Yt flip flop provides a signal to the Flexowriter relay for typing.
- Yp flip flop provides a signal to the Flexowriter relay for punching.

The Flexowriter, in turn, furnishes signals to the logical gates in the computer.

- S A + 15v signal to clear the computer for calling up N.M. Channel 01 to W.S. I (start routine).
- y1 through y6 are signals to set the computer "Y" flip flops. These signals come from either the RC or SC contacts and receive their voltage from the FLEXOWRITER I+ which is dropped and clamped to a 15 volt level in the Flexowriter filter unit before going to the logic gates.
- cr' a signal from flexowriter to denote whether the carriage is idle or returning. cr' goes to Cr' flip flop and is used as an interlock to keep flex from accepting outputs during a carriage return, tab, or back space. Go acts with this term to prevent outputs until cr' term comes up.
- fr' a signal originated in the Flexowriter to tell the computer it is busy reading. It normally rides at +15 v and drops to 0v during an RKC (read) or SC8 (power roller) cycle. In either case, the start of the signal is by mechanical contact closure and is adjustable. fr' is fed to Fr' Driver, which, in turn, triggers Fr' Flip Flop. The term Fr' (flip flop output) means that the Flexowriter is not busy reading.
- fw' a signal originated in the Flexowriter to tell the computer it is busy typing or punching. It normally rides at +15 v and drops to 0v during a TS (translator) or PCC (punch) cycle. In either case, the start of the signal is by mechanical contact closure and is adjustable. fw' is fed to Fw' Driver which, in turn, triggers Fw' flip flop. The term Fw' (flip flop output) means that the Flexowriter is not busy typing or punching.
- Hof this term is a logical +15 volt signal that tells the computer that the Flexowriter is on and the COMPUTE-OFF-FLEX Switch is in the COMPUTE position.
- I+ this is a rectified unfiltered +48 volts supply (as measured with a meter) that provides plate voltage for the one shot thyratons so that they may be extinguished. The I+ is used for the cr' term and is dropped and clamped to +15 volts through a 10K resistor on the Flexowriter filter unit.

"F" COUNTER EQUATIONS

$$\underline{F_1} = F' (F_1' C) + F_5 (F_1' C)$$

$$\underline{F_1}' = F_1 C$$

$$\underline{F_2} = F_2' (F_1 C) + P_{33} C$$

$$\underline{F_2}' = F_2 (F_1 C)$$

$$\underline{F_3} = F_3' (F C) + P_{33} C$$

$$\underline{F_3}' = F_3 (F_5' F C) + P_0 C$$

$$\underline{F_4} = F_4' F_3 (F C)$$

$$\underline{F_4}' = F_3' F_5 C$$

$$\underline{F_5} = F_5' (F_3 F_4 F_2 F_1' C) + F_4 (F_3' F_5')$$

$$\underline{F_5}' = F_5 (F_4 F_3 F_2 F_1' C) + P_{33} C$$

$$\underline{P_0} = F_5 F_3' C$$

$$\underline{P_0}' = P_0 C$$

$$\underline{P_1} = P_0 C$$

$$\underline{P_1}' = P_1 C$$

$$\underline{P_{32}} = F_5 (F_4 F_3 F_2 F_1' C)$$

$$\underline{P_{32}}' = P_{32} C$$

$$\underline{P_{33}} = F_4 (F_5' F_3' F C)$$

$$\underline{P_{33}}' = P_{33} C$$

"S" COUNTER EQUATIONS

$$\underline{S_1} = P_{S1} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 S_5 S_1' + (U K Q_4 C) R_1$$

$$\underline{S_1'} = P_{S1'} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 S_5 S_1 + (U K Q_4 C) R_1' + SC$$

$$\underline{S_2} = P_{S2} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 S_5 S_1 S_2' + (U K Q_4 C) R_2$$

$$\underline{S_2'} = P_{S2'} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 S_5 S_1 S_2 + (U K Q_4 C) R_2' + SC$$

$$\underline{S_3} = P_{S3} + F_0 \phi_1 Q_3 C S_8 S_3' + (U K Q_4 C) R_3$$

$$\underline{S_3'} = P_{S3'} + F_0 \phi_1 Q_3 C S_8 S_3 + (U K Q_4 C) R_3' + SC$$

$$\underline{S_4} = P_{S4} + F_0 \phi_1 Q_3 C S_8 S_3 S_4' + (U K Q_4 C) R_4$$

$$\underline{S_4'} = P_{S4'} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 + (U K Q_4 C) R_4' + SC$$

$$\underline{S_5} = P_{S5} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 S_5' + (U K Q_4 C) R_5$$

$$\underline{S_5'} = P_{S5'} + F_0 \phi_1 Q_3 C S_8 S_3 S_4 S_5 + (U K Q_4 C) R_5' + SC$$

$$\underline{S_6} = P_{S6} + (U K Q_4 C) R_6$$

$$\underline{S_6'} = P_{S6'} + (U K Q_4 C) R_6' + SC$$

$$\underline{S_7} = P_{S7} + (U K Q_4 C) R_7$$

$$\underline{S_7'} = P_{S7'} + (U K Q_4 C) R_7' + SC$$

$$\underline{S_8} = P_{S8} + F_0 \phi_1 Q_3 C S_8' + (U K Q_4 C) R_8$$

$$\underline{S_8'} = P_{S8'} + F_0 \phi_1 Q_3 C S_8 + (U K Q_4 C) R_8' + SC$$

" ϕ " Counter Equations

$$\begin{aligned}\phi_0 &= Q_4^C \\ \underline{\phi_0'} &= Q_3^C + SC\end{aligned}$$

$$\begin{aligned}\phi_1 &= \phi_0 Q_3^C \\ \underline{\phi_1'} &= \phi_1 Q_3^C + SC\end{aligned}$$

$$\begin{aligned}\phi_2 &= \phi_1 Q_3^C + SC \\ \underline{\phi_2'} &= \phi_2 Q_3^C + Q_4^C\end{aligned}$$

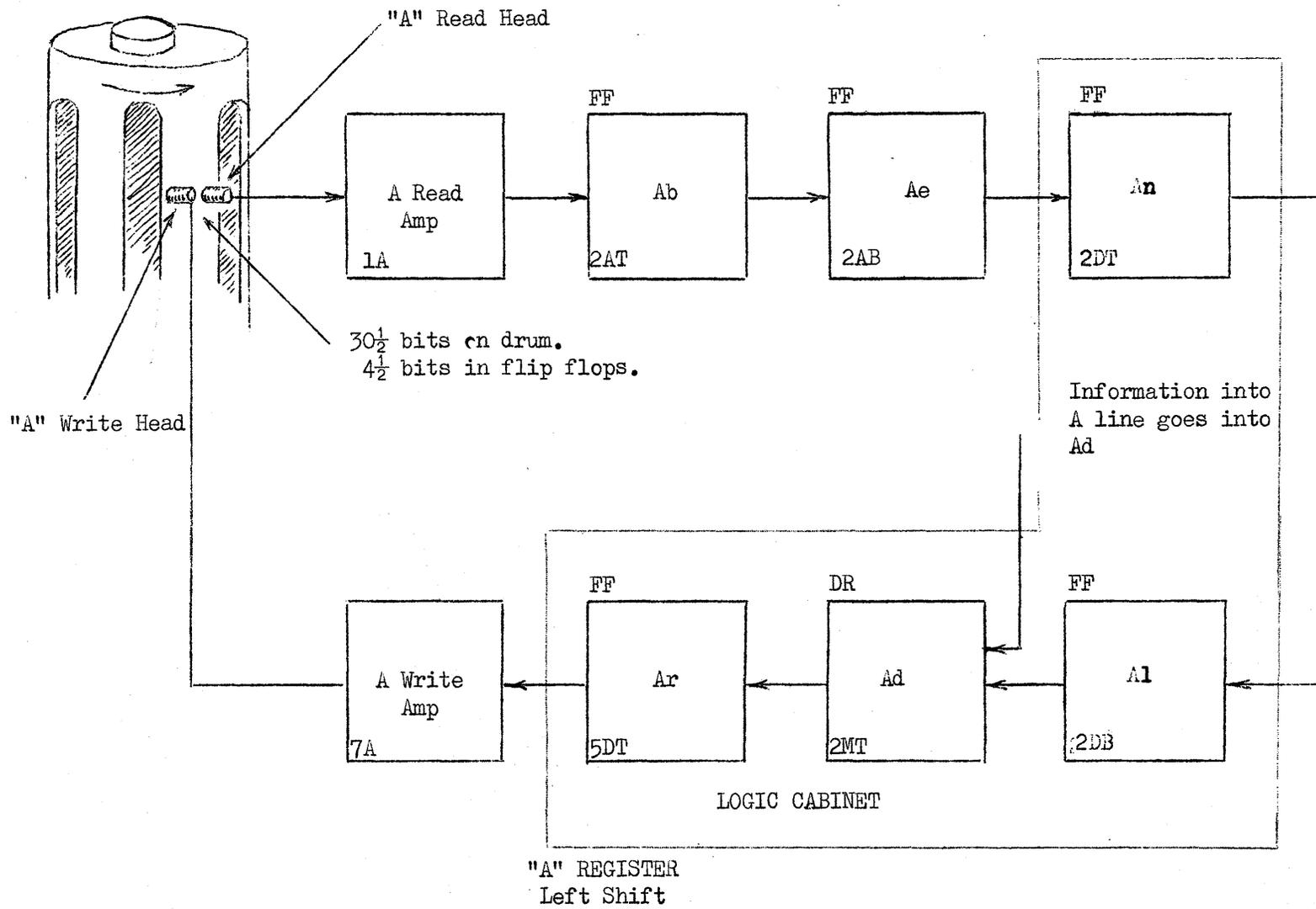
$$\begin{aligned}\phi_3 &= \phi_2 Q_3^C + \phi_7 Q_3^C \\ \underline{\phi_3'} &= \phi_3 Q_3^C + Q_4^C + SC\end{aligned}$$

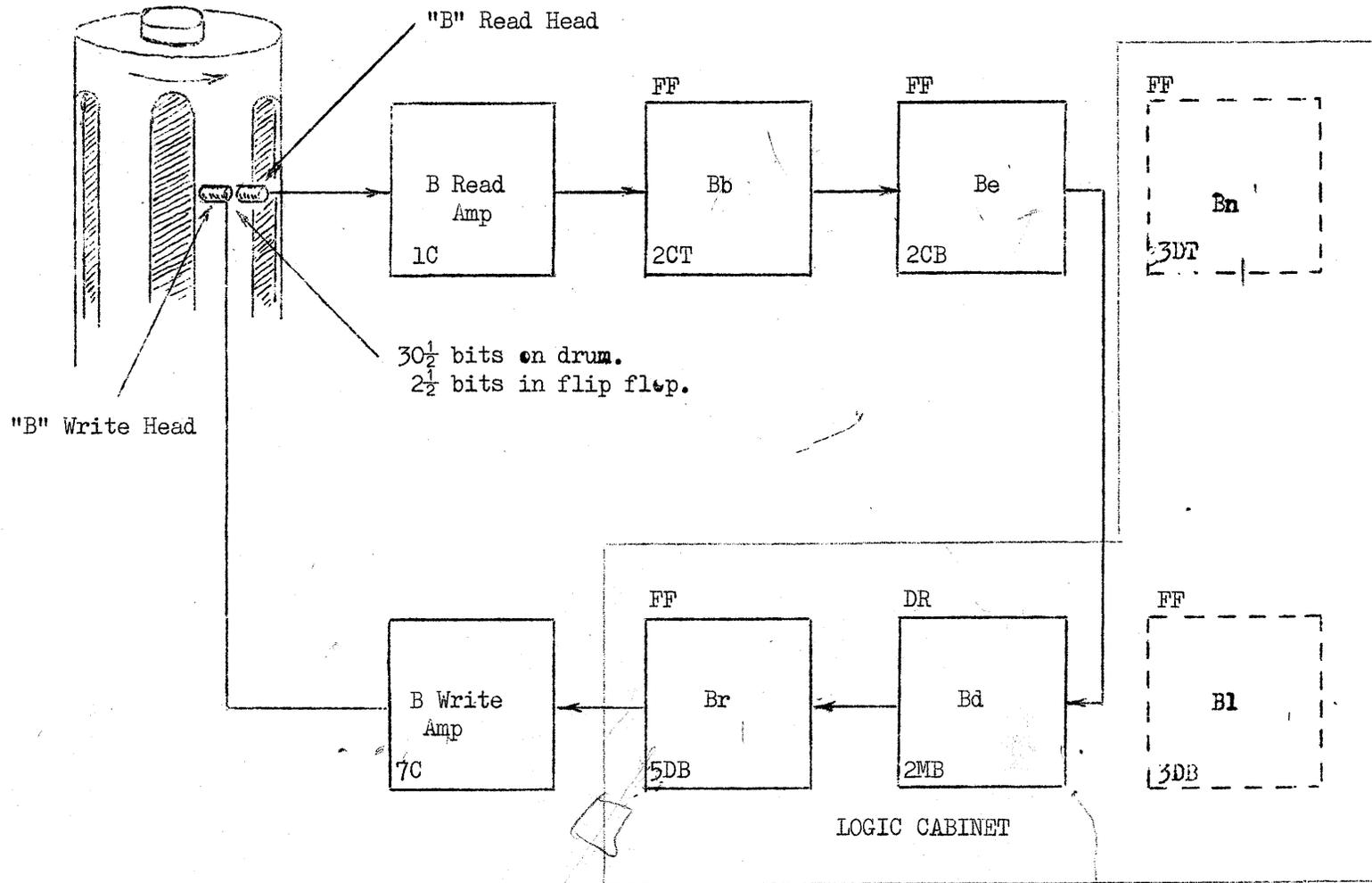
$$\begin{aligned}\phi_4 &= \phi_3 Q_3^C \\ \underline{\phi_4'} &= \phi_4 Q_3^C + Q_4^C + SC\end{aligned}$$

$$\begin{aligned}\phi_5 &= \phi_4 Q_3^C \\ \underline{\phi_5'} &= \phi_5 Q_3^C + Q_4^C + SC\end{aligned}$$

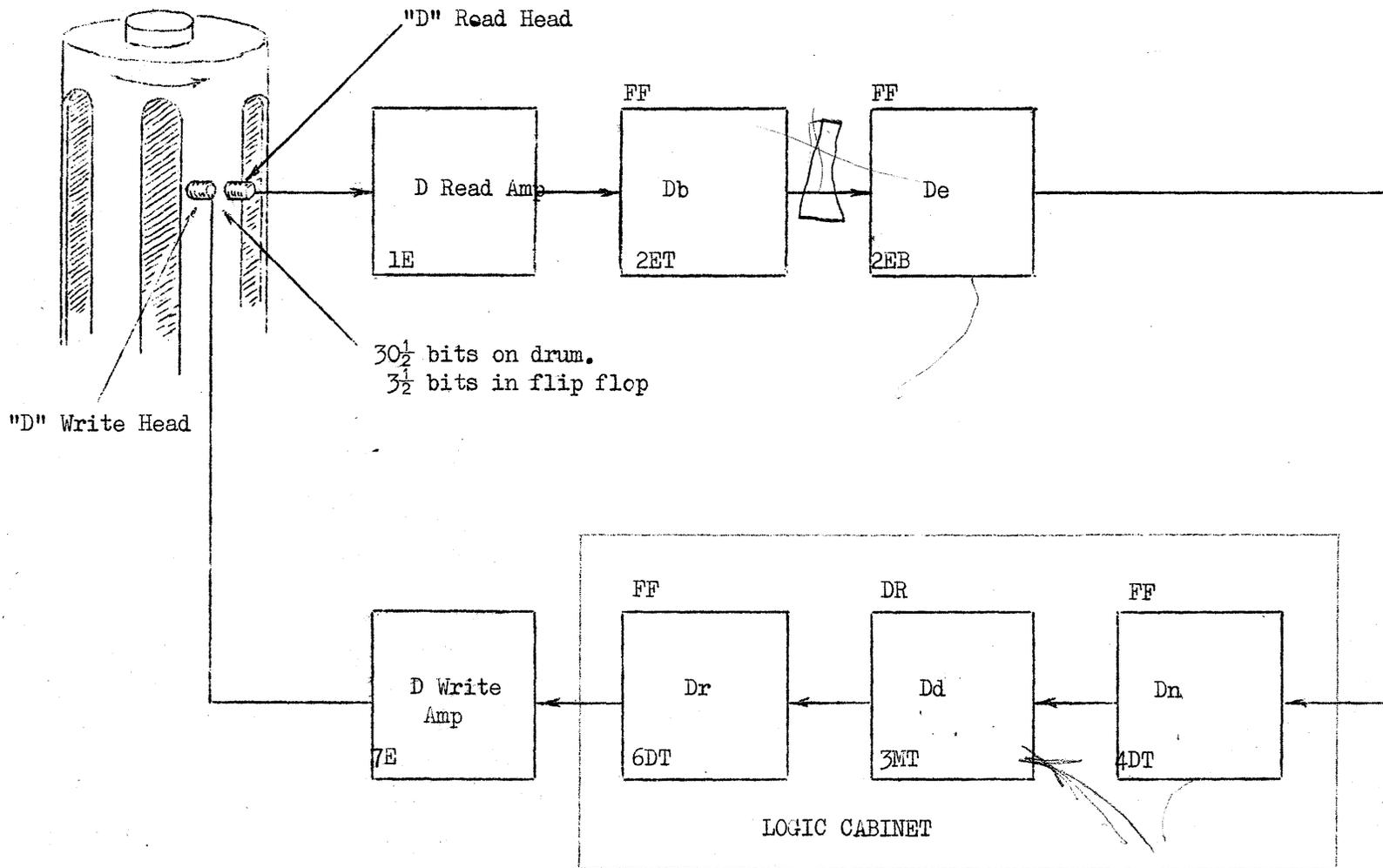
$$\begin{aligned}\phi_6 &= \phi_5 Q_3^C \\ \underline{\phi_6'} &= \phi_6 Q_3^C + Q_4^C + SC\end{aligned}$$

$$\begin{aligned}\phi_7 &= \phi_6 Q_3^C \\ \underline{\phi_7'} &= \phi_7 Q_3^C + Q_4^C + SC\end{aligned}$$

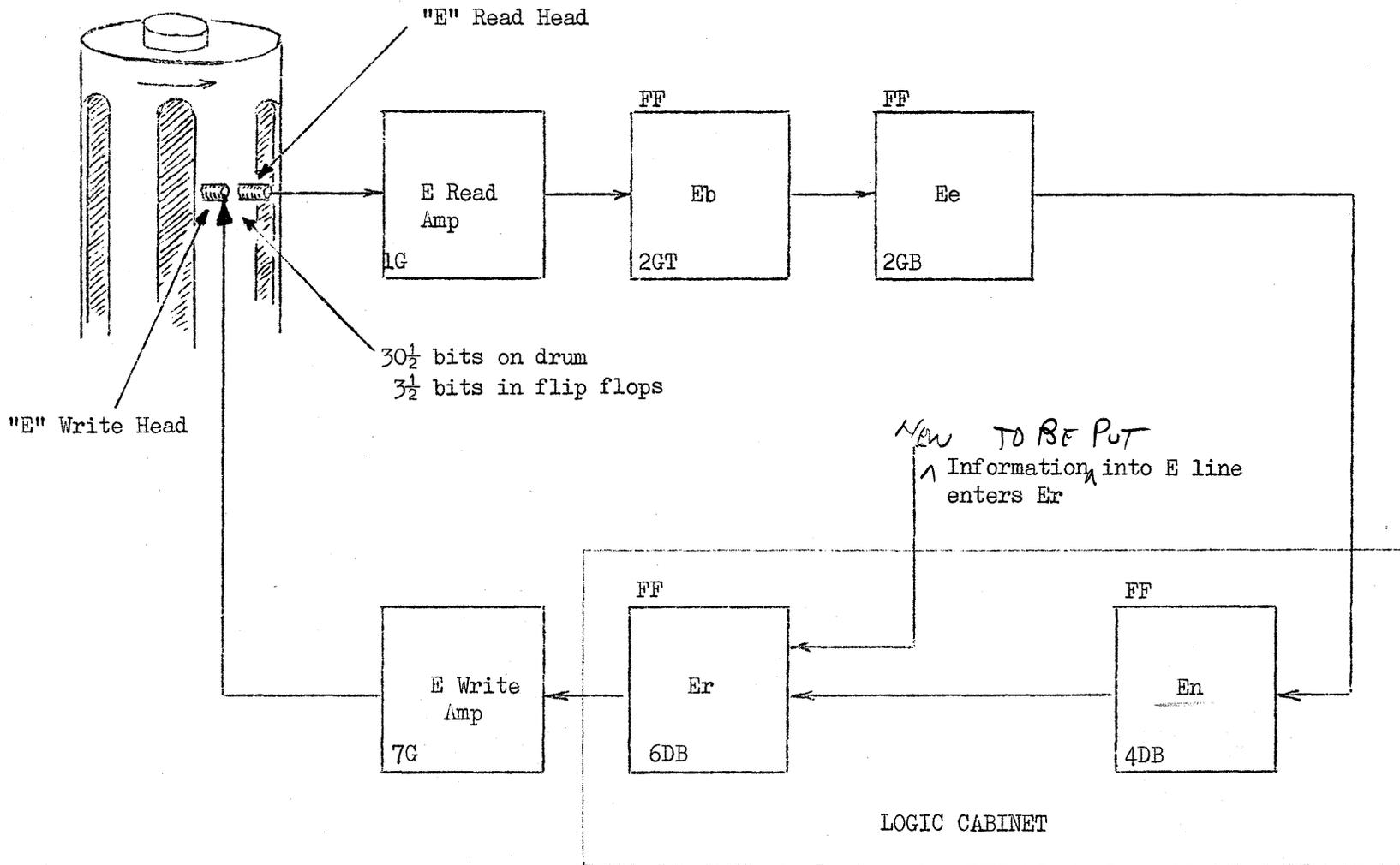




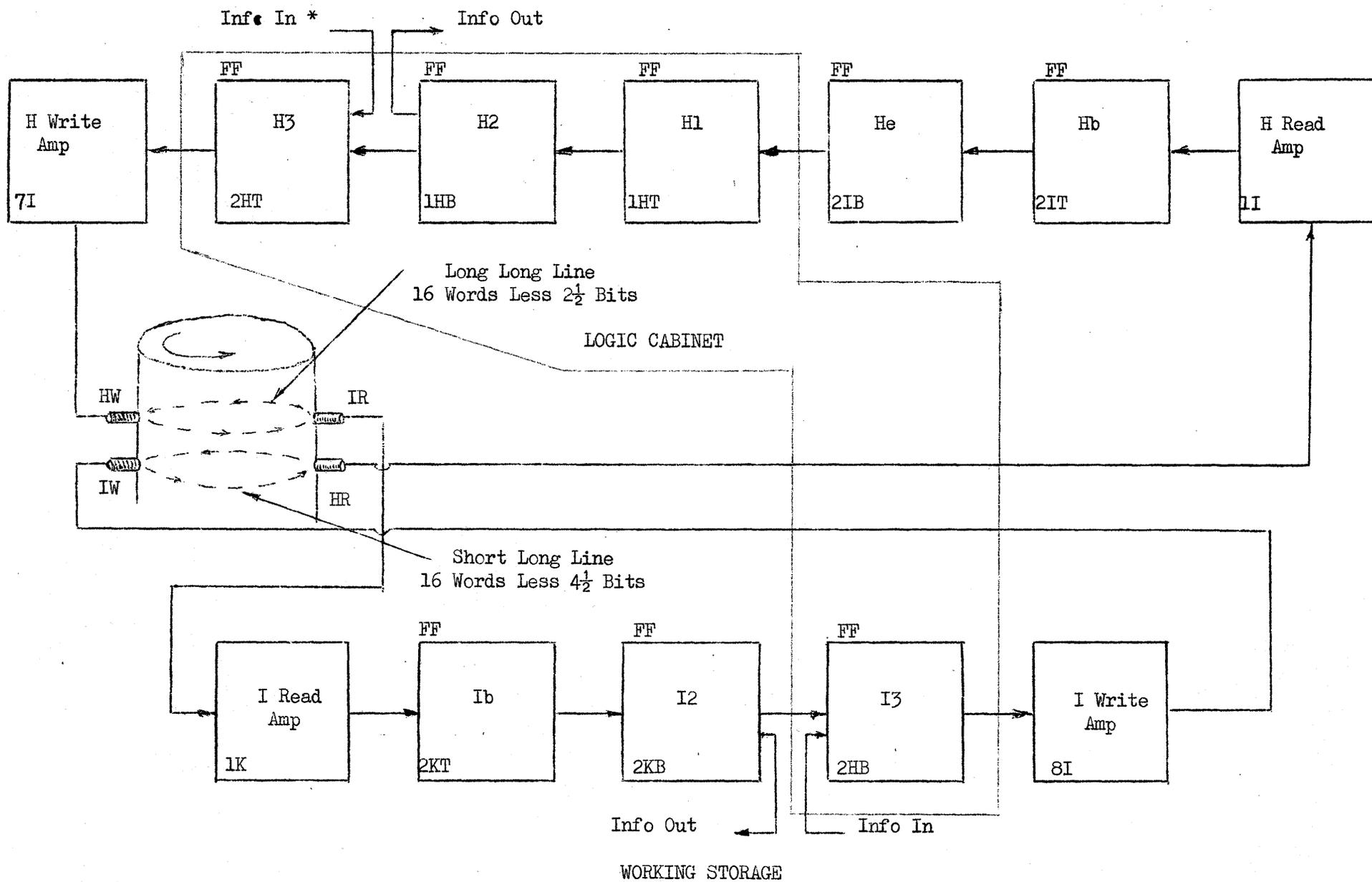
"B" REGISTER
Right Shift



"D" REGISTER
Normal Recirculation



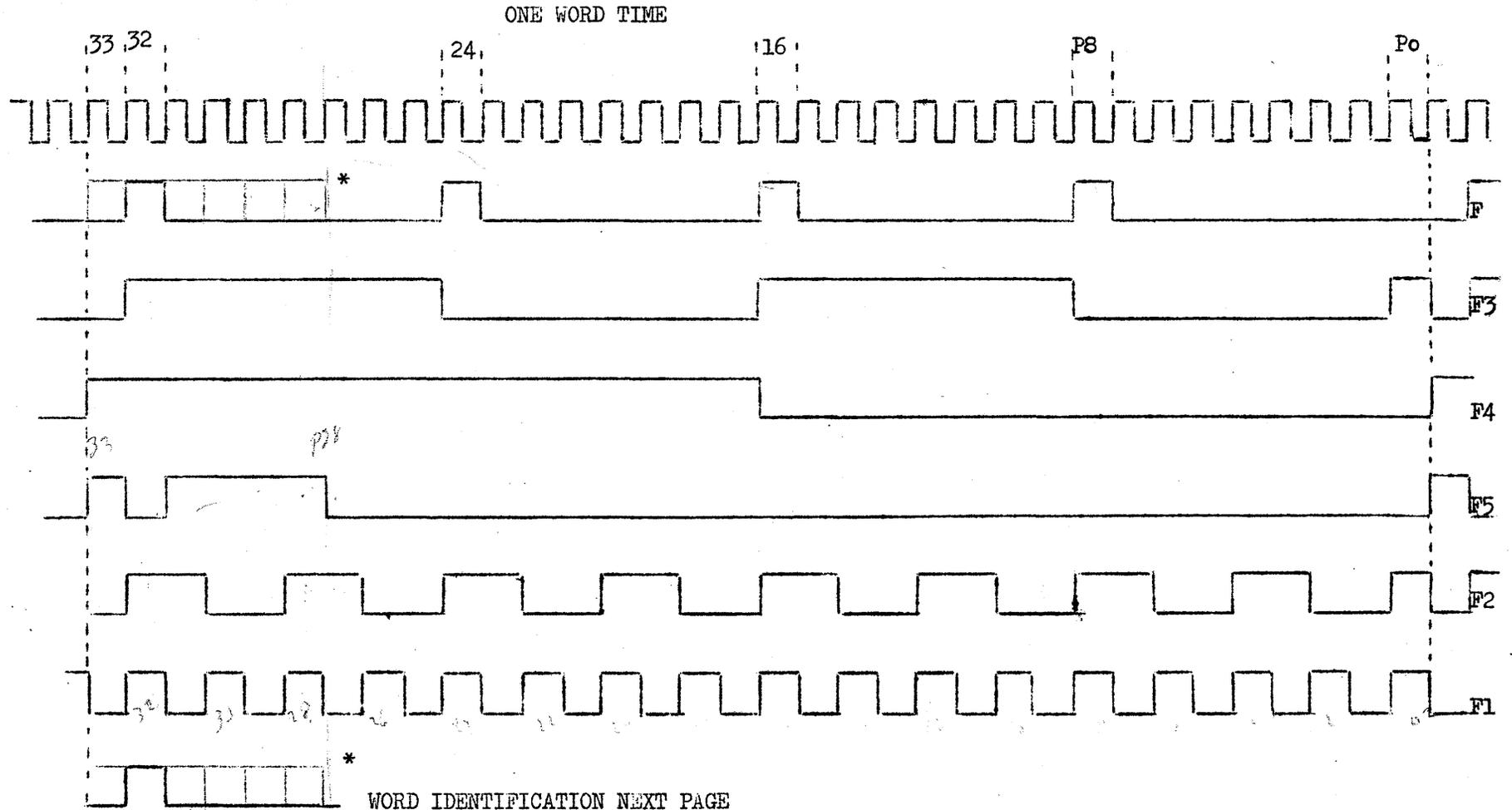
"E" REGISTER
Normal Recirculation



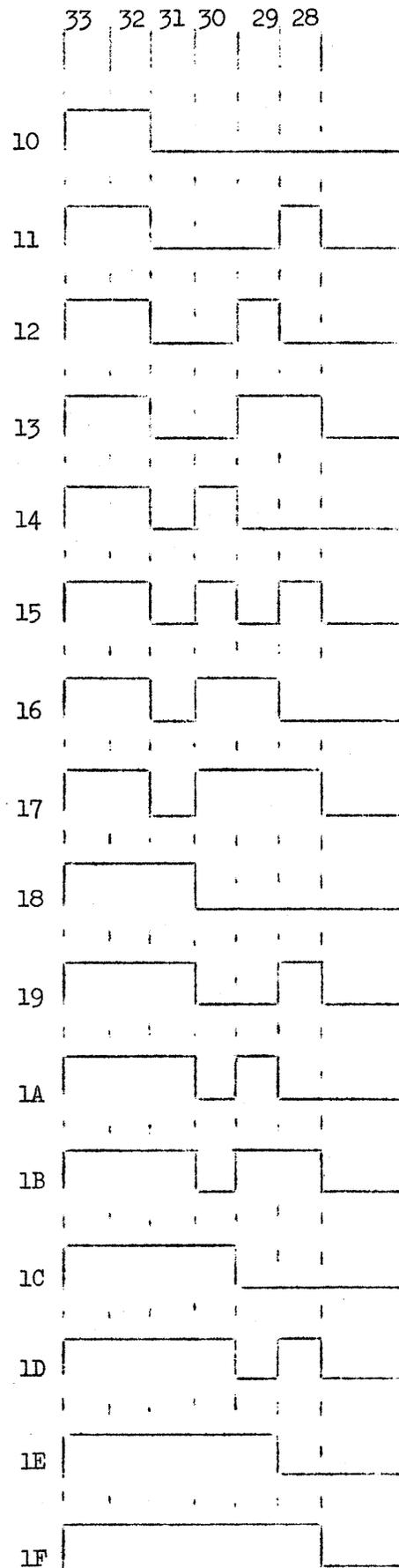
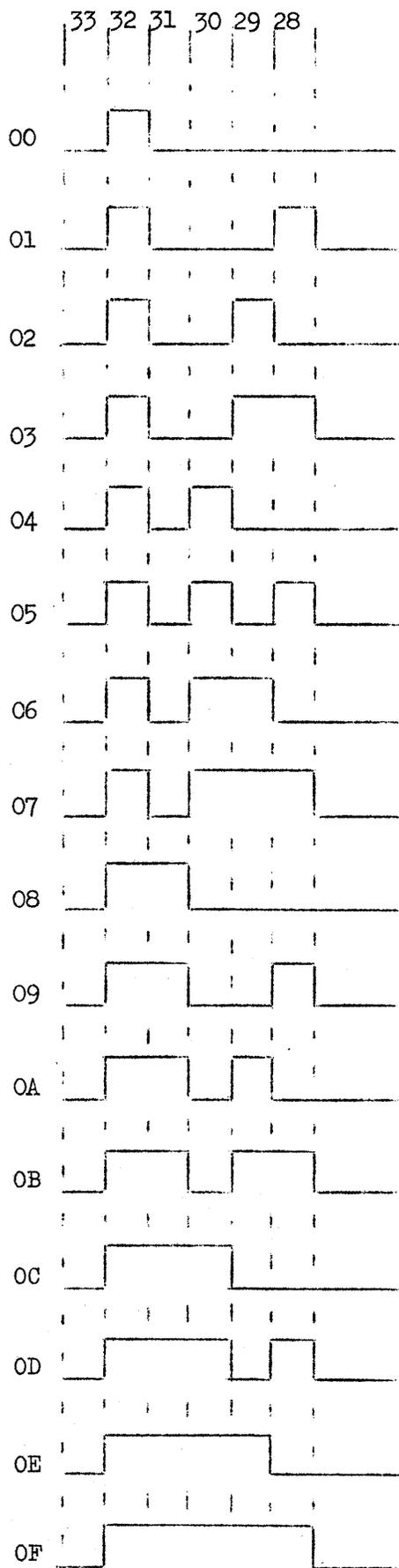
* Information into working storage lines in block transfers enter into H3, J3, L3 or N3 only.

TIMING CHART

← TIME



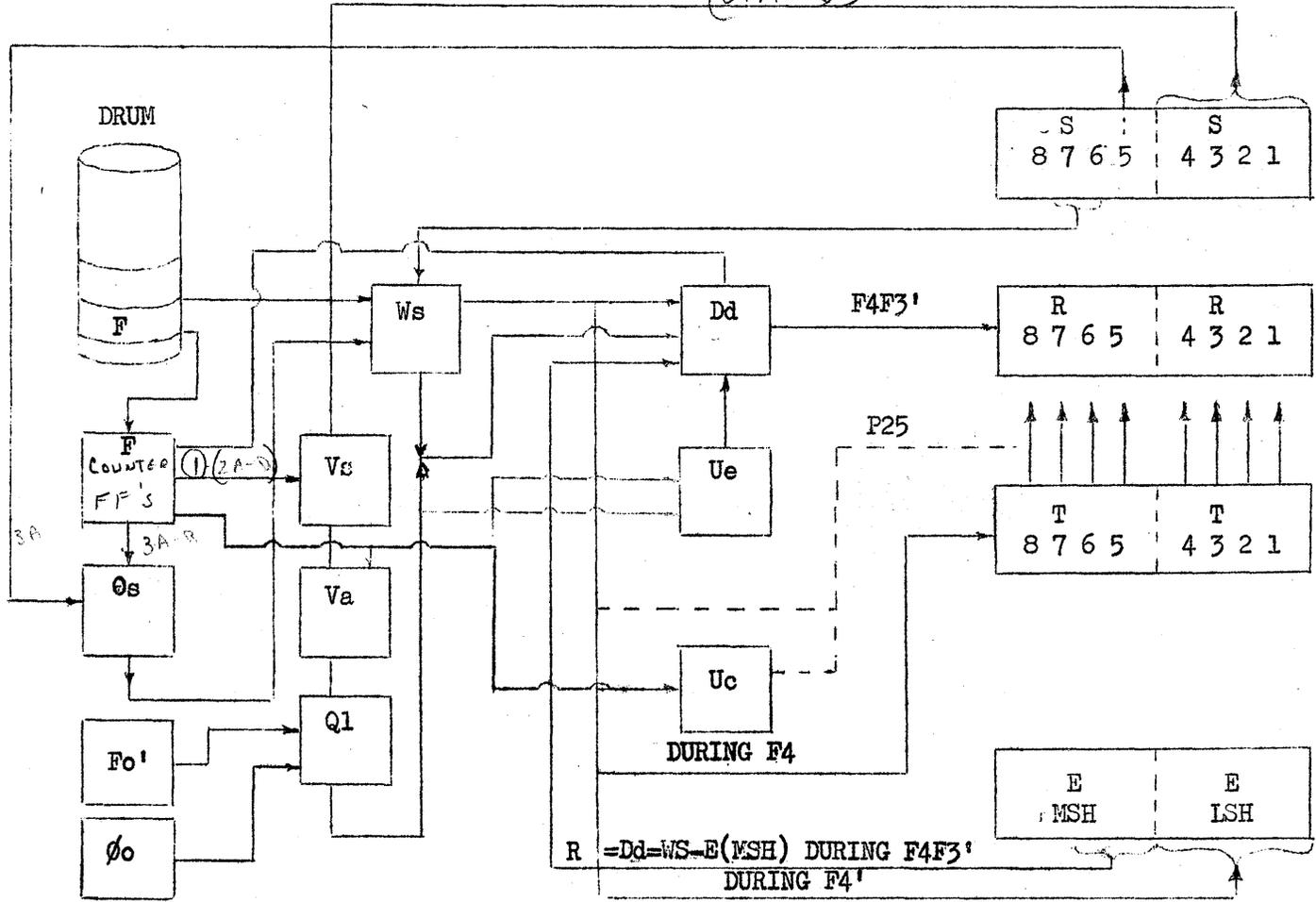
WORD IDENTIFICATION



"ø LOOK UP"

"S8 Uk" 1st Mode

(2A-D)



"S8 Uk" 2nd Mode

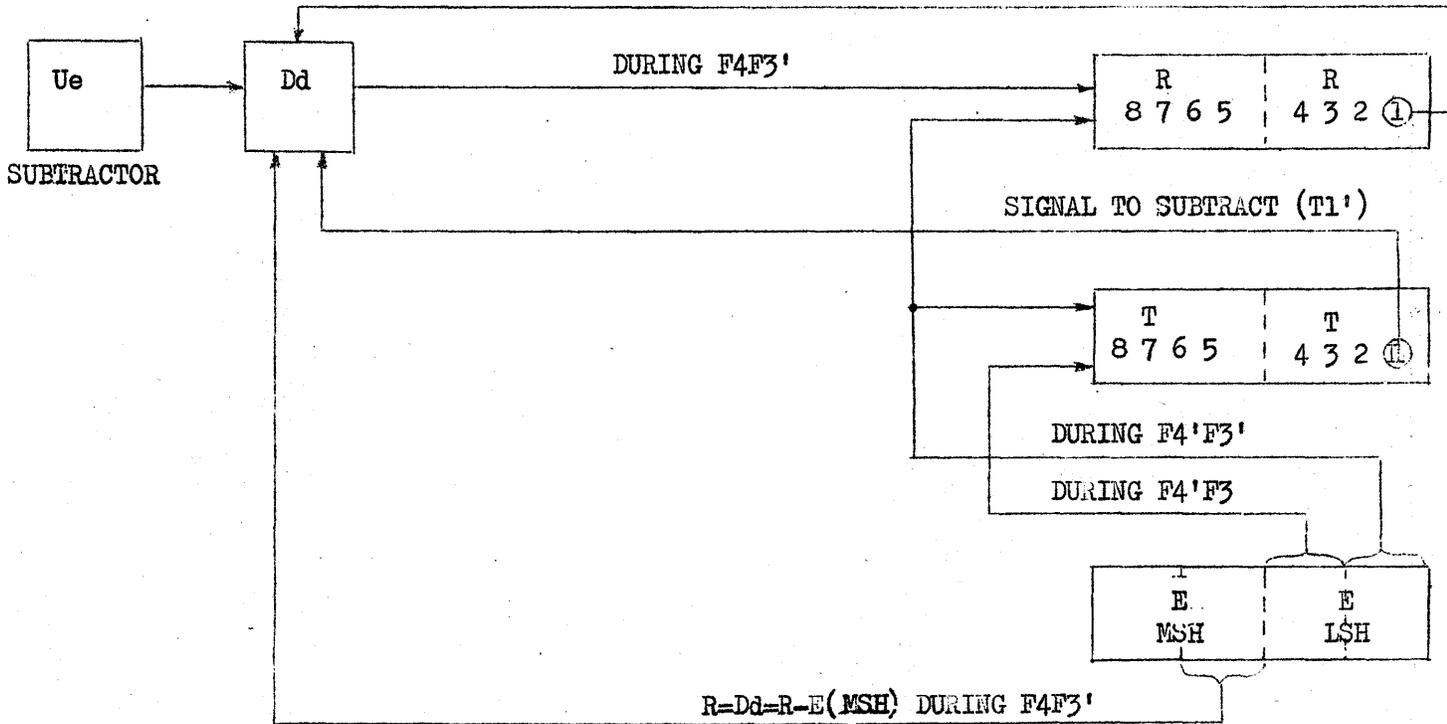


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" ϕ_0 " Look-up S8' UK' 1st. Mode

1. $V_s = F4 (F3' FC)$ 8BB5
2. (a) $V_{s'} = (F5 F2 F1 FC) S1' + (F5 F2 F1 F'C) S1$ 0BB5 0BB3
 (b) $+ (F5 F2' F1' FC) S2' P33' + (F5 F2' F1' F'C) S2 P33'$ 0BB15 0BB10
 (c) $+ (F5 F2' F1 FC) S3' + (F5 F2' F1 F'C) S3$ 1DD15 1DD11
 (d) $+ (F5 F2 F1' FC) S4' + (F5 F2 F1' F'C) S4$ 9BB7 9BB3
3. (a) $\underline{Q}_s = S5 (F' P33 C) + S5' (F' P33 C)$ 3B8 3B10
 (b) $\underline{Q}_{s'} = P32 C$ 3B6
4. (a) $\underline{W}_s = \left. \begin{array}{l} S7' S6' \overset{1-A}{Q_s'} H2 + S7' S6' \overset{3}{Q_s'} L2 \\ + S7' S6' \overset{1-B}{Q_s} I2 + S7' S6' \overset{3}{Q_s} L2 \\ + S7' S6' \overset{2-A}{Q_s'} J2 + S7' S6' \overset{4-A}{Q_s'} N2 \\ + S7' S6' \overset{2-B}{Q_s} K2 + S7' S6' \overset{4-B}{Q_s} O2 \end{array} \right\}$ 3J5 3J1
 (b) 4J13 4J9
 (c) 4J5 4J1
 (d) 5J13 5J9
5. (a) $\underline{V}_a = V_s P33 C$ 8BB13
 (b) $\underline{V}_{a'} = V_{s'} P33 C + U_k Q4 C$ — Jump 8BB11 3BB8
6. $\underline{Q}_1 = V_a F_0' \phi_0$ 2R24
7. (a) $\underline{E}_r = Q1' \phi_0 E_n C$ 7E8
 (b) $+ Q1 F4' W_s C$ 7YY14
 (c) $+ \phi_0 F4 E_n C$ 7YY10
 (d) $\underline{E}_{r'} = Q1' \phi_0 E_n' C$ 7E6
 (e) $+ Q1 F4' W_s' C$ 7YY2
 (f) $+ \phi_0 F4 E_n' C$ 7YY7
8. (a) $\underline{D}_r = \phi_0 D_n C$ 0B10
 (b) $\underline{D}_{r'} = \phi_0 D_n' C$ 0B7

Po - P32
 P17 - 24
 17-24

- 9. (a) $\underline{Dd} = (Q1 S8' F4 F3' P33')$ (Ws Ue En) 4YY16
- (b) + (") (Ws' Ue' En) 4YY12
- (c) + (") (Ws' Ue En') 4YY8
- (d) + (") (Ws Ue' En') 4YY4
- 10. (a) $\underline{Uc} = (")$ (Ws' En C) 2413
- (b) $\underline{Ue}' = (")$ (Ws En' C) 226
- (c) + (Q1 F4' F3' FC) 411
- 11. (a) $\underline{Uc} = \emptyset_0 F4 F3' FC$ 7EE5
- (b) $\underline{Uc}' = \emptyset_0 Uc C$ 2FF5
- 12. (a) $\underline{R8} = (Q1 F4 F3' P33')$ Fo' Dd C 7DD12
- (b) + Q1 Uc T8 Ws S8' Fo' C 6FF8
- (c) $\underline{R8}' = (Q1 F4 F3' P33')$ Fo' Dd' C 7DD10
- (d) + Q1 Uc T8' Ws S8' Fo' C 6FF6
- 13. (a) $\underline{Ri} = (Q1 F3' Fo')$ (Ri + 1) C (i = 1 thru 7 FFs)
- (b) + Q1 Uc Ti Ws S8' Fo' C
- (c) $\underline{Ri}' = (Q1 F3' Fo')$ (Ri' + 1) C
- (d) + Q1 Uc Ti' Ws S8' Fo' C
- 14. (a) $\underline{T8} = (Q1 Fo' F4 S8')$ Ws C 1FF3
- (b) $\underline{T8}' = (")$ Ws' C 2FF16
- 15. (a) $\underline{Ti} = Q1 Fo' (F4' + S8')$ (Ti + 1) C (i = 1 thru 7 FFs) 8U2
- (b) $\underline{Ti}' = Q1 Fo' (F4' + S8')$ (Ti' + 1) C 9U4
- 16. $\underline{Q3} = Q1 P32 + \emptyset_0 VA P32$ 2R5 867
- 17. $\underline{\emptyset_0}' = Q3 C$ 1U14
- 18. $\underline{\emptyset_1} = \emptyset_0 \Delta Q3 C$ 1U10
- 19. $\underline{Q3} = \emptyset_1 A2' A4' Ho G P33 + \emptyset_1 Gg P33$ OJ6 4R5
- 20. $\underline{\emptyset_1}' = \emptyset_1 Q3 C$ 1U3
- 21. $\underline{\emptyset_2} = \emptyset_1 Q3 C$ 1U3

DRIVERS: Ws, Q1, Dd and Q3. The remaining are FFs.

" ϕ " Look-up S8' UK' 1st. Mode

During ϕ S8' UK' the computer is seeking an instruction word, containing an order and address, that is located in one of the four working storage channels. The word's relative location to the "F" line is indicated by the configuration of the "S" register. To accomplish this "look-up" a comparison is made between the "S" register and the configuration of the "F" line.

In this mode of operation, the least significant half (LSH) of the 34 bit word is shifted into the LSH of the "E" line. The most significant half (MSH) is operated on and shifted into the "R" and "T" registers. P33 is excluded because Q1 goes prime at the fall of P32.

1. V_s is turned on at the fall of P24 every word time.
2. (a) The "S1" FF and "F" FF, (which is following the configuration of the "F" line) are compared at P28 time; if they are alike, V_s remains on; if they are different, V_s goes prime.
 - (b) The "S2" FF and "F" FF are compared at P29 time; if alike V_s remains on; if they are different V_s goes prime.
 - (c) The "S3" FF and "F" FF are compared at P30 time; if alike V_s remains on; if different V_s goes prime.
 - (d) The "S4" FF and "F" FF are compared at P31 time; if alike V_s remains on; if different V_s goes prime.

If "F" and "S" are alike for all four bits, V_s remains on at P33 and turns on V_a because there is no equation to turn V_s prime after P31.

"Refer to equation 5a".
3. The condition of Θ_s will determine from which half of the drum the word will be copied.
 - (a) If at P33 "S5" and "F" are opposite configurations, Θ_s will be turned on. If "S5" and "F" are alike Θ_s remains prime.
 - (b) Θ_s is turned prime at the fall of P32 every word time.

4. The various combinations of S7, S6 and Θ s will determine which FF Ws driver will follow.
5. (a) When Vs is on at P33 Va will be turned on. Va is a timing FF which signals that the word coming up is the one to be copied.
- (b) If Vs is prime Va remains prime and the computer knows the proper match has not been accomplished.
6. Q1 is a driver turned on at Po when Va is on and the NORMAL-HOLD-SELECT switch is in the NORMAL position (Fo') during ϕ_0 .
7. (a) This equation recirculates the "E" line normally before Q1 goes on by the En FF passing its ones to Er FF.
- (b) This equation feeds the ones being read out of the Ws driver to the Er FF after Q1 becomes true during the LSH word time.
- (c) This equation recirculates the "E" line normally during the MSH word time by passing the ones in the En FF to the Er FF.
- (d) This works in conjunction with the (7a) equation to pass the zeros.
- (e) This equation works in conjunction with the (b) equation to pass the zeros.
- (f) This equation works in conjunction with the (c) equation but passing the zeros.
8. (a) This equation recirculates the "D" line during the absence of the Dd in ϕ_0 by Dn FF passing its ones to the Dr FF.
- (b) This equation works in conjunction with the (a) equation but passes the zeros.
9. These equations (a.b.c.d) are used as a subtractor network to generate a modified address by subtracting the information passing thru the En FF from the information passing thru the Ws driver during the address portion ($F3'$) of the MSH word ($F4$) except for P33 time. The Ue FF is used as a borrow in these equations.
10. (a) Turns the borrow on.
- (b) Turns the borrow prime.
- (c) Turns the borrow prime before the subtraction starts.
11. Uc FF is used to pin-point P25 time.

- (a) Uc is turned on at the fall of P24 time.
 - (b) Uc is turned prime at the fall of P25 time.
12. (a) Q1 tells R8 (from P17 thru P24) if there is a one in the Dd take it.
- (b) Q1 tells R8, at P25 time, if Ws has a one accept the one in the T8.
 - (c) This equation works in conjunction with (a) but passes the zeros.
 - (d) This equation works in conjunction with (b) but passes the zeros.

The b and d equations are used if an unmodified address is desired as indicated by Ws containing a one at P25 time.

13. (a) This is used to serially pump across the ones in the "R" register.
- (b) This is used to parallel transfer in one pulse time, the ones in the "T" register if Ws has a one at P25 time.
 - (c) This is used to serially pump across the zeros in the "R" register.
 - (d) Same as (b) except to parallel transfer the zeros.

NOTE: (i = 1 thru 7)

14. (a) This tells T8 to follow Ws during F4 and follow the ones. 17-32
- (b) Same as (a) except to follow the zeros. 16
15. (a) This is used to serially pump across the ones in the "T" register.
- (b) Same as (a) except to serially pump across the zeros.
16. Turns on Q3 if Q1 is on at P32.
17. Turns off ϕ_0 when Q3 comes on.
18. Turns on ϕ_1 when Q3 comes on.
19. Turns on Q3 when in ϕ_1 and block transfer alarm is off (A2') overflow alarm is off (A4'), NORMAL-TEST-CLEAR switch in the NORMAL position (Ho), NORMAL-STOP-ONE STEP switch in the NORMAL position (G) at P33 time. The "or" equation takes care of sequencing when the NORMAL-STOP-ONE STEP switch is placed in the ONE STEP position. (Gg)
20. Turns ϕ_1 off when Q3 comes on.
21. Turns ϕ_2 on when Q3 comes on in ϕ_1 .

NOTE: Equations 16 thru 21 sequence the computer out of ϕ_0 and thru ϕ_1 into ϕ_2 .

- 1. (a) $V_a = P_0 S8 U_k' V_w' C$ 2R16
- (b) $V_a' = V_s' P33 C$ 83B11
- 2. $Q_1 = V_a F_0' \phi_0$ 2R24
- 3. (a) $R_8 = (Q_1 S8 F_4' F_3' U_k' F_0') E_n C$ 5FF16 ✓
- (b) $R_8' = (\quad) E_n' C$ 5FF6
- 4. (a) $R_i = (Q_1 F_3' F_0') (R_i + 1) C \quad (i = 1 \text{ thru } 7 \text{ FFs})$
- (b) $R_i' = (\quad) (R_i' + 1) C$
- 5. (a) $T_8 = (Q_1 F_0' F_4' P_0' U_k') E_n C$ 1FF6
- (b) $T_8' = (\quad) E_n' C$ 2FF10
- 6. (a) $T_i = Q_1 F_0' (F_4' + S8') (T_i + 1) C \quad (i = 1 \text{ thru } 7 \text{ FFs})$
- (b) $T_i' = Q_1 F_0' (F_4' + S8') (T_i' + 1) C$
- 7. (a) $D_r = \phi_0 D_n C$ 0B10
- (b) $D_r' = \phi_0 D_n' C$ 0B7
- 8. (a) $D_d = (Q_1 S8 F_4 F_3' P33') R_1 U_e E_n T_1'$ 5YY14
- (b) $+ (\quad) R_1' U_e' E_n T_1'$ 5YY10
- (c) $+ (\quad) R_1' U_e E_n' T_1'$ 5YY6
- (d) $+ (\quad) R_1 U_e' E_n' T_1'$ 5YY2
- (e) $+ (\quad) R_1 T_1' - ?$ 6YY2 ✓
- 9. (a) $U_e = (\quad) R_1' E_n C$ 2Z9
- (b) $U_e' = (\quad) R_1 E_n' C$ 3R16
- (c) $+ (Q_1 F_4' F_3' FC)$ 4I1
- 10. (a) $R_8 = (Q_1 F_4 F_3' P33') D_d F_0' C$ 7DD12
- (b) $R_8' = (\quad) D_d' F_0' C$ 7DD10
- 11. (a) $R_i = (Q_1 F_3' F_0') (R_i + 1) C \quad (i = 1 \text{ thru } 7 \text{ FFs})$
- (b) $R_i' = (\quad) (R_i' + 1) C$
- 12. $Q_3 = Q_1 P32$ 2R5
- 13. $\phi_0' = Q_3 C$ 1U14

Handwritten notes:

- 1-8 (ADDRESS)
- 17-24
- 17-24

- | | | | |
|-----|--|-----|------|
| 14. | $\underline{\phi 1} = \phi_0 Q3 C$ | | 1U10 |
| 15. | $\underline{Q3} = \phi 1 A2' A4' Ho G P33 + \phi 1 Gg P33$ | OJ6 | 4R5 |
| 16. | $\underline{\phi 1'} = \phi 1 Q3 C$ | | 1U3 |
| 17. | $\underline{\phi 2} = \phi 1 Q3 C$ | | 1U3 |

" ϕ_0 " S8 UK' 2nd. mode

In this mode of ϕ_0 , S8 UK' the computer does not have to locate the word in the MS channels because it has previously stored it in the LSH of the "E" line as a result of the 1st mode of ϕ_0 .

This mode of operation deals with shifting the instruction word located in the LSH of the "E" line, into the "R" and "T" registers and modifying the address if the instruction is modified.

1. (a) V_a goes true at P_0 time every word that V_w is prime, S8 true and UK prime (indicating no jump)
(b) V_a goes prime at P_{33} if V_s is prime.
2. Q1 is a driver turned on at P_0 when V_a is on and the NORMAL-HOLD-SELECT switch is in the NORMAL position (F_0') during ϕ_0 .
3. (a) Transfers the ones in the address portion of the LSH of the "E" line to the "R" register by the use of the R8 and En FFs.
(b) Same as (a), except transfers the zeros.
4. (a) Used to serially pump across the ones in the "R" register.
(b) Used to serially pump across the zeros in the "R" register.
5. (a) Transfers the ones, during F_4' time, from the LSH of the "E" line to the "T" register.
(b) Transfers the zeros, during F_4' time, from the LSH of the "E" line to the "T" register.
6. (a) Used to serially pump across the ones in the "T" register.
(b) Used to serially pump across the zeros in the "T" register.
7. (a) Recirculates the "D" line during the absence of the D_d in ϕ_0 by the D_n FF passing its ones to the D_r FF.
(b) Same as (a) but passes the zeros.
8. (a,b,c,d) equations form a subtractor, subtracting the information passing thru the E_n FF from the information passing thru the R_1 FF, providing the T_1 is prime. U_c is used as a borrow FF.
(c) This equation is used to recirculate the information in the "R" register by the use of the D_d during $F_4 F_3' P_{33}'$ if T_1 is true.
9. (a) Turns on borrow FF.
(b) Turns the borrow FF prime.
(c) Turns the borrow FF prime before the subtraction starts.

10. (a) Q1 tells R8, during F4 F3' P33' if there is a one in Dd take it.
(b) Same as (a), except passes the zeros.
11. (a) This is used to serially pump across the ones in the "R" register.
(b) Same as (a) but passes zeros.

Explanation for equations 12 thru 17 are the same as explanations for equations 16 thru 21 of "ø" 1st mode.

After equations 1 thru 4, page 1, are accomplished the following apply.

1. (a) $\underline{V_a} = V_s P33 C$ 8BB13
 (b) $\underline{V_a'} = U_k Q4 C + V_s' P33 C$ 3BB8 8BB11
2. $\underline{Q1} = V_a F_o' \phi_0$ 2R24
3. (a) $\underline{R8} = (Q1 S8 F4' F3' U_k F_o') W_s C$ 5FF13
 (b) $\underline{R8'} = (\quad) W_s' C$ 5FF3
4. (a) $\underline{R_i} = (Q1 F3' F_o') (R_i + 1) C$ (i = 1 thru 7 FFs)
 (b) $\underline{R_i'} = (\quad) (R_i' + 1) C$
5. (a) $\underline{T8} = (Q1 F_o' F4' P_o' U_k) W_s C$ 1FF9
 (b) $\underline{T8'} = (\quad) W_s' C$ 2FF13
6. (a) $\underline{T_i} = Q1 F_o' (F4' + S8') (T_i + 1) C$ (i = 1 thru 7 FFs)
 (b) $\underline{T_i'} = Q1 F_o' (F4' + S8') (T_i' + 1) C$
7. (a) $\underline{D_r} = \phi_0 D_n C$ OB10
 (b) $\underline{D_r'} = \phi_0 D_n' C$ OB7
8. (a) $\underline{D_d} = (Q1 S8 F4 F3' P33') R1 U_e E_n T1'$ 5YY14
 (b) $+ (\quad) R1' U_e' E_n T1'$ 5YY10
 (c) $+ (\quad) R1' U_e E_n' T1'$ 5YY6
 (d) $+ (\quad) R1 U_e' E_n' T1'$ 5YY2
 (e) $+ (\quad) R1 T1$ 6YY2
9. (a) $\underline{U_e} = (\quad) R1' E_n C$ 2Z9
 (b) $\underline{U_e'} = (\quad) R1 E_n' C$ 3R16
 (c) $+ Q1 F4' F3' F_C$ 4I1
10. (a) $\underline{R8} = (Q1 F4 F3' P33') D_d F_o' C$ 7DD12
 (b) $\underline{R8'} = (\quad) D_d' F_o' C$ 7DD10
11. (a) $\underline{R_i} = (Q1 F3' F_o') (R_i + 1) C$ (i = 1 thru 7 FFs)
 (b) $\underline{R_i'} = (\quad) (R_i' + 1) C$
12. $\underline{Q3} = Q1 P32$ 2R5
13. $\underline{\phi_0'} = Q3 C$ 1U14
14. $\underline{\phi_1} = \phi_0 Q3 C$ 1U10
15. $\underline{Q3} = \phi_1 A2' A4' H_o G P33 + \phi_1 G_g P33$ OJ6 4R5
16. $\underline{\phi_1'} = \phi_1 Q3 C$ 1U3
17. $\underline{\phi_2} = \phi_1 Q3 C$ 1U3

NOTE: During this mode of operation equations 7b and 7e, page 1, would be valid.

" ϕ_0 " S8 UK 3rd Mode

During " ϕ_0 " S8 UK the computer is seeking an instruction word containing an order and address that is located in one of the four working storage channels. The word's relative location to the "F" line is indicated by the configuration of the "S" register. To accomplish this "look-up" a comparison is made between the "S" register and the configuration of the "F" line.

In this mode of operation the LSH of the 34 bit word is going to be shifted into the "R" and "T" registers and operated on while the RSH will be disregarded.

NOTE: Equations 1, 2, 3 and 4 in mode one " ϕ_0 " operation are used before the first equation in this mode is used.

1. (a) When Vs is on at P33 Va will be turned on. Va is a timing FF which signals that the word coming up is the one to be copied.
 (b) If Vs is prime at P33 Va remains prime and the computer knows the proper match has not been made.
Uk 34 C has turned Va prime after ϕ_2 so the computer will perform the "look-up" by the use of equations 1, 2, 3 and 4 of mode one.
2. Q1 is a driver turned on at Po when Va is on and the NORMAL-HOLD-SELECT switch is in the NORMAL position (P_0') during ϕ_0 .
3. (a) Q1 tells R8 (from P1 thru P8) if there is a one in the Vs driver take it.
 (b) This equation works in conjunction with (a) but passes zeros.
4. (a) This is used to serially pump across the ones in the "R" register.
 (b) Same as (a) but passes zeros.
5. (a) Q1 tells T8 (from P1 thru P16) if there is a one in the Vs driver take it.
 (b) Same as (a) but passes zeros.

The explanations for equations 6 thru 17 are the same as the explanations for 6 thru 17 in " ϕ_0 " second mode.

"02" Look-up

1. (a) $\underline{Vr} = F4 (F3' FC)$ 8BB5
2. (a) $\underline{Vr}' = (F5 F2 F1 FC) R1' + (F5 F2 F1 F'C) R1$ 2DD16 2DD15
- (b) $+ (F5 F2' F1' FC) R2' P33' + (F5 F2' F1' F'C) R2 P33'$ 1DD5 2DD8
- (c) $+ (F5 F2' F1 FC) R3' + (F5 F2' F1 F'C) R3$ 2DD13 2DD11
- (d) $+ (F5 F2 F1' FC) R4' + (F5 F2 F1' F'C) R4$ 1DD9 1DD7
3. (a) $\underline{\Theta r} = R5 (P33 F'C) + R5' (P33 FC)$ 3B16 2B2
- (b) $\underline{\Theta r}' = R5 (P33 FC) + R5' (P33 F'C)$ 3B12 3B14
4. (a) $\underline{Wn} = R7' R6' \overset{\circ}{\Theta r}' \overset{0}{I-A} H2 + R7 R6' \overset{10}{\Theta r}' \overset{10}{III A} L2$ 1J13 1J8
- (b) $+ R7' R6' \overset{\circ}{\Theta r}' \overset{0}{I B} I2 + R7 R6' \overset{10}{\Theta r}' \overset{10}{III B} M2$ 1J3 2J14
- (c) $+ R7' R6 \overset{\circ}{\Theta r}' \overset{0}{II A} J2 + R7 R6 \overset{10}{\Theta r}' \overset{10}{IV A} N2$ 2J9 2J4
- (d) $+ R7' R6 \overset{\circ}{\Theta r}' \overset{0}{II B} K2 + R7 R6 \overset{10}{\Theta r}' \overset{10}{IV B} O2$ 3J15 3J10
5. (a) $\underline{Vw} = Vr P33 C$ 8BB9
- (b) $\underline{Vw}' = Vr' P33 C$ 8BB7

"Ø2" Look-up

In general, during "Ø2" the computer is seeking a data word that is located in one of the four working storage channels. The word's relative location to the "F" line is indicated by the configuration of the "R" register. To accomplish this "look-up", a comparison is made between the "R" register and the configuration of the "F" line.

The initial "Ø2" "look-up" is accomplished by equations 1 through 5 each time it is employed. The whole word, 34 bits, or the amount of the whole word that is copied, is dependent upon the particular command employing the "look-up".

1. Vr is turned on at the fall of P24 every word time.
2. (a) The "R1" FF and the "F" FF (which is following the configuration of the "F" line), are compared at P28 time; if they are alike, Vr remains on; if they are different, Vr goes prime.
 - (b) The "R2" FF and "F" FF are compared at P29 time; if alike Vr remains on; if they are different Vr goes prime.
 - (c) The "R3" FF and "F" FF are compared at P30 time; if alike Vr remains on; if different Vr goes prime.
 - (d) The "R4" FF and "F" FF are compared at P31 time; if alike Vr remains on; if they are different Vr goes prime.

If "F" and "R" are alike for all four bit times, Vr remains on at P33 and turns on Vw because there is no equation to turn Vr prime after P31.
"Refer to equation 5 a".
3. The conditions of Ør will determine from which half of the drum the word will be copied.
 - (a) If at P33 "R5" and "F" are opposite configurations, Ør will be turned on.
 - (b) If at P33 "R5" and "F" are alike, Ør will be turned prime.
4. Equations (a, b, c, d): The various configurations of R7, R6, and Ør will determine which FF Wn driver will follow.
5. (a) When Vr is on at P33, Vw will be turned on. Vw is a timing FF which signals that the word coming up is the one to be copied.
 - (b) If Vr is prime at P33, Vw remains prime and the computer knows the proper match has not been accomplished so it tries again.

NOTE: From this point on Wn driver will feed the information to the proper driver or FF selected by the particular order associated with this "look-up".

Orders beginning with 0, 2 or 3.

1. (a) $\underline{T1}' = T8' T7' T6 F0' \phi 2 P33 C$ 3U6
 (b) $+ T8' T7' T5' F0' \phi 2 P33 C$ 3U4
2. (a) $\underline{Ti} = (T8' T7' T6 F0' \phi 2 P33 C) Ri$ (i = 2 thru 8 FF's)
 (b) $+ (T8' T7' T5' F0' \phi 2 P33 C) Ri$
3. (a) $\underline{Ti}' = (T8' T7' T6 F0' \phi 2 P33 C) Ri'$
 (b) $+ (T8' T7' T5' F0' \phi 2 P33 C) Ri'$
4. (a) $\underline{Q4} = T8' T7' T6 T1' P33 \phi 2$ OP12
 (b) $+ T8' T7' T5' T1' P33 \phi 2$ OP9

DESCRIPTION:

These orders do not require an address, therefore, two can be "packed" into a half word. The computer recognizes this situation by the first order to be executed having been increased by one. In other words, the order placed in the order portion of the word has had a one added to it when it was programmed into the machine.

At the end of the first word time in $\phi 2$, by which time the execution of the first order would have taken place, the T1 FF will be true due to the above conditions. The Q4 driver could not be turned on because of equation 4a or 4b.

At P33 time in $\phi 2$, there will be a parallel transfer of the information in the "R" register to the "T" register (T2 thru T8 FF's) by equations 2a and 2b. The T1 FF will be turned prime by equations 1a or 1b.

After the execution of the second order in $\phi 2$ during the second word time, Q4 driver will be turned on due to equations 4a or 4b and the computer will sequence back to $\phi 0$.

02 Change Overflow Indicator

1. (a) $\underline{Z} = (T8' T7' T6' T5' T4' T3' T2) (P32 C) \phi 2 Z'$ 9DD6
 (b) $\underline{Z}' = (T8' T7' T6' T5' T4' T3' T2) (P32 C) \phi 2 Z$ 4Y9
2. (a) $\underline{Q4} = (T8' T7' T5') (\phi 2 P33) T1'$ OP9
 (b) $\underline{\phi 2}' = Q4 C$ 1U16
 (c) $\underline{\phi 0} = Q4 C$ 1U16

Q2 Change Overflow Indicator (Cont'd)

DESCRIPTION:

NOTE: "Z" is the overflow FF.

1. (a) At P32 with Q2 in the "T" register, if the Z FF is off, turn it on in $\phi 2$.
- (b) At P32 " " " " " " " " on, turn if off in $\phi 2$.
2. (a) At P33, turn Q4 on in $\phi 2$.
- (b)) Sequence out of $\phi 2$ to $\phi 0$.
- (c)

11 Transfer

1. (a) $\underline{Uk} = (T8' T7' T6' T5) (T4' T3') T2' (\phi 2 P33 C)$ 4Z15
- (b) $\underline{Q3} = (T8' T7' T6' T5) T4' \phi 2 P33$ 9EE16
- (c) $\underline{\phi 2'} = \phi 2 Q3 C$ 2U14
- (d) $\underline{\phi 3} = \phi 2 Q3 C$ 2U14
- (e) $\underline{Q4} = (T8' T7' T6') T5 \phi 3$ OP3
2. (a) $\underline{Si} = (Uk Q4 C) Ri$ (i = 1 thru 8 FF's)
- (b) $\underline{Si'} = (Uk Q4 C) Ri'$
- (c) $\underline{Va'} = Uk Q4 C$ 3BB8
3. (a) $\underline{\phi 3'} = Q4 C$ 1U16
- (b) $\underline{\phi 0} = Q4 C$ 1U16

DESCRIPTION:

NOTE: "Uk" is the jump FF and always turns prime at the fall of the clock in $\phi 1$ "UK" = $\phi 1 C$.

1. (a) At P33 with 11 in the "T" register, Uk is turned on in $\phi 2$.
- (b) Q3 driver is turned on at P33 in $\phi 2$.
- (c)) Sequences out of $\phi 2$ to $\phi 3$.
- (d)
- (e) Q4 driver turned on in $\phi 3$.

11 Transfer (Cont'd)

2. (a) Parallel transfer of the ones in the "R" register to the "S" register.
- (b) Same as (a) but zeros transferred.
- (c) Va is turned prime to start new ϕ_0 look-up.
3. (a) Sequencing equation out of ϕ_3 to ϕ_0 .
- (b) " " " " "

13 Transfer on Switch One

- 12 + 13
1. (a) $\underline{U_k} = (T_8' T_7' T_6' T_5) T_4' T_3' T_2 (\phi_2 P_{33} C) Sk 1$ 4Z11
 - (b) $\underline{Q_3} = (T_8' T_7' T_6' T_5) T_4' (\phi_2 P_{33})$ 9EE16
 - (c) $\underline{\phi_2'} = \phi_2 Q_3 C$ 2U14
 - (d) $\underline{\phi_3} = \phi_2 Q_3 C$ 2U14
 - (e) $\underline{Q_4} = (T_8' T_7' T_6') T_5 \phi_3$ OD3
 2. (a) $\underline{S_i} = (U_k Q_4 C) R_i$ (i = 1 thru 8 FF's)
 - (b) $\underline{S_i'} = (U_k Q_4 C) R_i'$
 - (c) $\underline{V_a'} = U_k Q_4 C$ 3BB8
 3. (a) $\underline{\phi_3'} = Q_4 C$ 1U16
 - (b) $\underline{\phi_0} = Q_4 C$ 1U16

DESCRIPTION:

1. (a) At P33 with 13 in the "T" register and jump switch #1 in the jump position, (Sk1) U_k is turned on in ϕ_2 .
- (b) Q_3 driver is turned on at P33 in ϕ_2 .
- (c)
- (d)) Sequences out of ϕ_2 to ϕ_3 .
- (e) Q_4 driver turned on in ϕ_3 .
2. (a) Parallel transfer of ones in the "R" register to the "S" register.
- (b) Same as (a) but zeros transferred.
- (c) Va is turned prime to start new ϕ_0 look-up.

13 Transfer on Switch One (Cont'd)

3. (a) Sequencing equations out of ϕ_3 to ϕ_0 .
 (b) " " " " "

15 Transfer on Switch Two

14 + 15

1. (a) $\underline{U_k} = (T_8' T_7' T_6' T_5) T_4' (T_3 T_2') (\phi_2 P_3 C) Sk_2$ 4Z5
 (b) $\underline{Q_3} = (T_8' T_7' T_6' T_5) T_4' (\phi_2 P_3)$ 9EE16
 (c) $\underline{\phi_2'} = \phi_2 Q_3 C$ 2U14
 (d) $\underline{\phi_3} = \phi_2 Q_3 C$ 2U14
 (e) $\underline{Q_4} = (T_8' T_7' T_6') T_5 \phi_3$ OP3
2. (a) $\underline{S_i} = (U_k Q_4 C) R_i$ (i = 1 thru 8 FF's)
 (b) $\underline{S_i'} = (U_k Q_4 C) R_i'$
 (c) $\underline{V_a'} = U_k Q_4 C$ 3BB8
3. (a) $\underline{\phi_3'} = Q_4 C$ 1U16
 (b) $\underline{\phi_0} = Q_4 C$ 1U16

DESCRIPTION:

Identical to the 13 order, except jump switch #2 in the jump position (Sk2).

17 Transfer on Index "Count-Down"

16 + 17

- 1. (a) \underline{Er} = (T8' T7' T6' T5 T4' T3 T2 \emptyset 2) (En' C) Ua OC6
- (b) + (" " " ") (En C) Ua' OC3
- (c) \underline{Er}' = (T8' T7' T6' T5 T4' T3 T2 \emptyset 2) (En C) Ua 2B12
- (d) + (" " " ") (En' C) Ua' 2B9

- 2. (a) \underline{Ua} = (T8' T7' T6' T5 T4' T3 T2) \emptyset 2 F4' F3 FC P14 6W4
- (b) \underline{Ua}' = (" " " ") \emptyset 2 (En C) F4 P17 P32 9W14
- (c) + P33 C 2C2

- 3. (a) \underline{Uc} = T8' T7' F4' F3 FC \emptyset 0' 0 to 3f p. 16 6FF16
- (b) \underline{Uc}' = T8' T7' Uc C - 10-17 2FF3
- (c) + P33 C 2C3

- 4. (a) \underline{Uk} = (T8' T7' T6' T5 T4' T3 T2) En' \emptyset 2 Uc C P17 5Z13
- (b) + (" " " ") En (F4 P33') (\emptyset 2 C) Uc' 5Z8
- (c) \underline{Uk}' = \emptyset 1 C 9B7

- 5. (a) $\underline{Q3}$ = (T8' T7' T6' T5) T4' (\emptyset 2 P33) 10-17 9EE16
- (b) $\underline{\emptyset 2}'$ = \emptyset 2 Q3 C 2U14
- (c) $\underline{\emptyset 3}$ = \emptyset 2 Q3 C 10-18 2U14
- (d) $\underline{Q4}$ = (T8' T7' T6') T5 \emptyset 3 OP3

- 6. (a) \underline{Si} = (Uk Q4 C) Ri (i = 1 thru 8 FF's)
- (b) \underline{Si}' = (Uk Q4 C) Ri'
- (c) \underline{Va}' = Uk Q4 C 3BB8

- 7. (a) $\underline{\emptyset 3}'$ = Q4 C 1U16
- (b) $\underline{\emptyset 0}$ = Q4 C 1U16

4 x 31
 1 L 2 3 -
 5 L 24 6 L 25 8 L 21 8 J 23 9 J 19
 7026
 6025
 0 C 17

17 Transfer on Index "Count-Down"

There are three functions taking place in this order:

1. The LSH of the "E" line is being recirculated normally.
2. The MSH (P17 thru P32) of the "E" line is being counted down by one.
3. The MSH of the "E" line is being checked to see if it is a one.

If after the subtraction of one, the MSH of the "E" line is a number equal to, or greater than, one, the address that is associated with the order and contained in the "R" register during ϕ_2 , is parallel transferred to the "S" register. The computer then sequences back to ϕ_0 and uses the address in the "S" register to locate the next instruction word.

If after the subtraction of one, the MSH of the "E" line equals zero, the computer sequences back to ϕ_0 but uses the address in the "S" register that has appeared due to the normal counting operation. (No parallel transfer from the "R" to "S")

The MSH of "E" line can have a value which will fit into one of the following categories:

- I Zero
- II Even, but greater than zero
- III Odd, but greater than one
- IV One

I If the value of the MSH of "E" line is zero, then the following operations take place during the MSH word time.

- (a) At the fall of P16 time, Ua FF is turned on by equation 2a and will remain on until the fall of P33 time. Equation 2b cannot turn Ua FF off as En is prime P17 thru P33 time.
- (b) At the fall of P16 time, Uc FF is turned on by equation 3a.
- (c) At the fall of P17 time, Uk FF is turned on by equation 4a. Uk FF will stay on for remaining pulse times.
- (d) At the fall of P17 time, Uc FF is turned off by equation 3b. Uc FF pin-pointed P17 time.
- (e) Due to Ua FF being on from P17 thru P33 time and the MSH of the "E" line having all zeros, equation 1a writes all ones in the MSH of the "E" line. Then the MSH "E" line has 1FFFF in it.
- (f) The computer will perform the "jump" because Uk was turned on at the fall of P17 and will remain in this loop until the MSH of "E" line is reduced to one.

17 Transfer on Index "Count-Down" (Cont'd)

II If the value of the MSH of "E" line is EVEN (and greater than zero), the following operations will take place during the MSH word time.

- (a) At the fall of P16 time, Ua FF is turned on by equation 2a.
- (b) At the fall of P16 time, Uc FF is turned on by equation 3a.
- (c) At the fall of P17 time, Uk FF is turned on by equation 4a. Uk FF will stay on for remaining pulse times.
- (d) At the fall of P17 time, Uc FF is turned off by equation 3b.
- (e) The value of the MSH of the "E" line will be reduced by one by equations 1a, 1b, 1c and 1d. Ua will be turned off by a bit between P17 thru P32 time by equation 2b; ~~the same bit which turned Uk on.~~ ?
- (f) The computer will execute the "jump" and remain in this loop until the MSH of the "E" line is reduced to one.

III If the value of the MSH of the "E" line is ODD (and greater than one), the following operations will take place during the MSH word time.

- (a) At the fall of P16 time, Ua FF is turned on by equation 2a.
- (b) At the fall of P16 time, Uc FF is turned on by equation 3a.
- (c) At the fall of P17 time, Uk is not turned on by equation 4a. $(E_n = 1)$?
- (d) From P18 thru P32 time, Uk will be turned on by ~~some~~ bit by equation 4b. ?
- (e) The value of the MSH of the "E" line is reduced by one by equations 1a, 1b, 1c and 1d. Ua will be turned off by the same bit which turned Uk on.
- (f) The computer will execute a "jump" and remain in this loop until the MSH of the "E" line is reduced to one.

IV If the value of the MSH of the "E" line is ONE, the following operations take place.

- (a) At the fall of P16 time, Ua FF is turned on by equation 2a.
- (b) At the fall of P16 time, Uc FF is turned on by equation 3a.
- (c) At the fall of P17 time, Uk FF is not turned on by equation 4a.
- (d) For the remaining pulse time, Uk is not turned on by equation 4b.
- (e) The value of the MSH of the "E" line is reduced from one to zero at the fall of P17 times.
- (f) The Uk FF was not turned on hence, the computer will not "jump" and will sequence out of the loop to the next address.

17 Transfer on Index "Count-Down" (Cont'd)

1. (a) Used to count down the MSH of "E" by putting out ones when Ua is true and En is prime.
 (b) Recirculates the ones in the LSH of "E" and also the remaining ones in the MSH of "E" during the subtraction process.
 (c) Used to count down the MSH of "E" by putting out zeros when Ua is true and En is true.
 (d) Recirculates the zeros in the LSH of "E" and also the remaining zeros in the MSH of "E" during the subtraction process.
2. (a) Ua is turned true at the fall of P16 time every word time in $\phi 2$.
 (b) Ua is turned prime any time there is a one in En during F4 $\phi 2$ time.
 (c) Ua is turned prime every P33 time.
3. (a) Uc is a timing FF that is turned on at the fall of P16 every word time and remains on for one pulse.
 (b) Uc is turned prime at the fall of P17 every word time.
 (c) Uc is turned prime at the fall of P17³³ every word time.
4. (a) Uk is the jump FF and is turned on at the fall of P17 time during $\phi 2$ if En contains a zero.
 (b) Uk is turned on any time from (P18 thru P32) in $\phi 2$ if En contains a one.
 (c) Uk is turned prime every $\phi 1$ time.
5. (a) Q3 driver is turned on during P33 and $\phi 2$ time with the 17 order in the "T" register.
 (b) $\phi 2$ is turned prime by $\phi 2$ Q3 and clock. "Sequencing"
 (c) $\phi 3$ is turned on by $\phi 2$ Q3 and clock. "Sequencing"
 (d) Q4 driver is turned on in $\phi 3$ with the 17 order in the "T" register.
6. (a) If Uk Q4 are on, the ones in the "R" register are parallel transferred to the "S" register.
 (b) Same as (a) but transfers the zeros.
 (c) Va is turned prime if Uk Q4 are on to start new $\phi 0$ "look-up".
7. (a) $\phi 3$ turned prime when Q4 is on. "Sequencing"
 (b) $\phi 0$ turned on when Q4 is on. "Sequencing".
 Computer then starts $\phi 0$ "look-up".

19 Transfer on Non-Zero

- 18, 19, 1a, 1d, P-P32*
1. (a) $\underline{U}_k = (T8' T7' T6' T5) T4 T2' \wedge n (P33' Po') (\phi 2 C)$ 3Z4
 - (b) $\underline{Q}_3 = (T8' T7' T6' T5) T4 T2' \phi 2 P33$ 9EE13
 - (c) $\underline{\phi 2}' = \phi 2 Q3 C$ 2U14
 - (d) $\underline{\phi 3} = \phi 2 Q3 C$ 2U14
 - (e) $\underline{Q}_4 = (T8' T7' T6') T5 \phi 3$ OP3

 2. (a) $\underline{S}_i = (Uk Q4 C) R_i$ (i = 1 thru 8 FFs)
 - (b) $\underline{S}_i' = (Uk Q4 C) R_i'$
 - (c) $\underline{V}_a' = Uk Q4 C$ 3BB8

 3. (a) $\underline{\phi 3}' = Q4 C$ 1U16
 - (b) $\underline{\phi 0} = Q4 C$ 1U16

DESCRIPTION:

1. (a) U_k will be turned on any time there is a one in $\wedge n$ from P1 thru P32 with a 19 order in the "T" during $\phi 2$.

Explanation for equations (1b thru 3b) are identical to the ones in an 11 order.

1B Halt and Transfer

- 1a, 1b*
1. (a) $\underline{U}_k = (T8' T7' T6' T5) (T4 T3') T2 S_s (\phi 2 P32 C)$ 4Y1
 - (b) $\underline{Q}_3 = (T8' T7' T6' T5) T4 T3' \phi 2 P33 Uk$ 9EE7

Equations and explanations from this point are identical to the 11 order (1c thru 3b)

DESCRIPTION:

1. (a) U_k will be turned on when there is a 1B order in the "T" register, the NORMAL-START switch is in the START position, (S_s), at P32 time during $\phi 2$.
- (b) Q_3 driver will be turned on at P33 time during $\phi 2$ with a 1B order in the "T" register.

1D Transfer on Less Than Zero

- 18, 19 1C, 1D*
- | | | | | | |
|----|-----|------------|---|---|-------|
| 1. | (a) | <u>Uk</u> | = | (T8' T7' T6' T5) T4 T2' An (P33' Po') (ϕ 2 C) | 3Z4 |
| | (b) | <u>Uk'</u> | = | (T8' T7' T6' T5) T4 (T3 T2') (ϕ 2 P33) (Ae C) | 5Z4 |
| | (c) | <u>Q3</u> | = | (T8' T7' T6' T5) T4 T2' ϕ 2 P33 | 9EE13 |

Equations and explanations from this point are identical to the 11 order (1c thru 3b).

DESCRIPTION:

If there is a number greater than zero in the "A" line and it is negative, parallel transfer the "R" to the "S" register. If not, sequence normally.

- | | | | |
|----|-----|-----------|---|
| 1. | (a) | Uk FF | will be turned on if An is true any time between P1 and P32 time, with a 1D order in the "T" register during ϕ 2. |
| | (b) | UK FF | will be turned off at P33 time if Ae (the sign bit position) is true, (indicating a plus sign) with a 1D in the "T" register during ϕ 2. |
| | (c) | Q3 driver | will be turned on at P33 time during ϕ 2 with a 1D order in the "T" register. |

1F Transfer on Overflow

- | | | | | | |
|----|-----|-----------|---|---|-------|
| 1. | (a) | <u>Uk</u> | = | (T8' T7' T6' T5) (T4 T2) (ϕ 2 P33 C) Z T3 | 5Z15 |
| | (b) | <u>Z'</u> | = | (T8' T7' T6') (T5 T4) T2 Z (ϕ 2 P33 C) | 5Y8 |
| | (c) | <u>Q3</u> | = | (T8' T7' T6' T5) (T4 T3) (ϕ 2 P33) | 9EE10 |

Equations and explanations from this point are identical to the 11 order (1c thru 3b).

DESCRIPTION:

NOTE: "Z" is the overflow FF.

- | | | | |
|----|-----|-----------|---|
| 1. | (a) | Uk FF | will be turned on at P33 time if the Z FF is on with a 1F order in the "T" register during ϕ 2. |
| | (b) | Z FF | will be turned prime at P33 time if the Z FF is on with a 1F order in the "T" register during ϕ 2. |
| | (c) | Q3 driver | will be turned on at P33 time with a 1F in the "T" register during ϕ 2. |

22 Round

If the computer sequences from $\phi 1$ to $\phi 2$, check page 21, the following is performed:

- | | | | | | |
|----|-----|-----------------------|---|--|------|
| 1. | (a) | $\underline{U_b}$ | = | B_d (P32 C) | 6Y15 |
| | (b) | $\underline{U_b}'$ | = | B_d' (P32 C) | 8Y15 |
| 2. | (a) | $\underline{U_a}$ | = | $(T_8' T_7' T_6 T_5' T_4')$ $\phi 2$ U_b (Po C) | 7W15 |
| | (b) | $\underline{U_a}'$ | = | (" ") $\phi 2$ (A_n' C) | 9W11 |
| | (c) | | + | P33 C | 2C2 |
| 3. | (a) | $\underline{A_d}$ | = | $(T_8' T_7' T_6 T_5' T_4' \phi 2)$ (A_n' U_a) T2 | 1L2 |
| | (b) | | + | (" ") (A_n U_a') T2 | 1L4 |
| 4. | | $\underline{Q_4}$ | = | $(T_8' T_7' T_6)$ ($\phi 2$ P33) T1' | OP12 |
| 5. | (a) | $\underline{\phi 2}'$ | = | Q4 C | 1U16 |
| | (b) | $\underline{\phi 0}$ | = | Q4 C | 1U16 |

DESCRIPTION:

If the P32 bit in the "B" line is a one, it will be added to the "A" line; if not, "A" is recirculated normally.

1. (a) U_b FF is turned on at P32 time if B_d has a one in it.
(b) U_b FF is turned off at P32 time if B_d has a zero in it.
2. (a) U_a FF is turned on at Po time if U_b is on.
(b) U_a FF is turned prime the first time A_n is prime during $\phi 2$. U_a stays prime then.
(c) U_a is turned prime at P33 every word time.
3. (a) A_d is turned on with a 22 order in the "T" register in $\phi 2$ when A_n is prime and U_a is true. "Adds the one to "A".
(b) A_d is turned on with a 22 order in the "T" register in $\phi 2$ when A_n is true and U_a is prime. Recirculates the "A" line normally. "Ad follows A_n ".
4. Q_4 driver is turned on at P33 time in $\phi 2$ with a 22 in the "T" register.
5. (a))
(b)) } Sequences the computer out of $\phi 2$ to $\phi 0$.

28 Clear A

- | | | | | | |
|----|--|-------------------|---|--|-----|
| 1. | | $\underline{A_d}$ | = | $(T_8' T_7' T_6 T_5' T_4 \phi 2)$ T2' Po | 3L7 |
|----|--|-------------------|---|--|-----|

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. A_d will go true at Po time with a 28 order in the "T" register during $\phi 2$. (Since there is no equation to recirculate "A" the duration of time from P1 thru P33, the "A" line will be filled with zeros including P33).

2C Set Sign Plus

1. (a) \underline{Ad} = $(T8' T7' T6 T5' T4 \emptyset 2) T2' Po$ 3L7
 (b) + (") $An T3 Po'$ 3L16

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. (a) \underline{Ad} will go true at Po time with a 2C order in the "T" register during $\emptyset 2$.
 (b) \underline{Ad} will go true from $P1$ thru $P33$ time every time An is true with a 2C order in the "T" register during $\emptyset 2$. "Normal Recirculation" " \underline{Ad} follows An ".

2E Change Sign

1. (a) \underline{Ad} = $(T8' T7' T6 T5' T4 \emptyset 2) An' T3 T2 Po$ 3L12
 (b) + (") $An T3 Po'$ 3L16

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. (a) \underline{Ad} will go true at Po time if An is prime with a 2E order in the "T" register during $\emptyset 2$. (Changes either a plus sign to minus or a minus sign to a plus)
 (b) \underline{Ad} will go true from $P1$ thru $P33$ time every time An is true with a 2E order in the "T" register during $\emptyset 2$. "Normal Recirculation" " \underline{Ad} follows An "

30 Exchange A and B

1. (a) \underline{Ad} = $(T8' T7' T6 T5 \emptyset 2) (T4' T3) Bn P33'$ 2L14
 (b) \underline{Bd} = $(T8' T7' T6 T5 \emptyset 2) (T4' T3') T2' An P33'$ 7J7

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. (a) \underline{Ad} will go true every time Bn is true from Po thru $P32$ time, excluding $P33$, with a 30 order in the "T" register during $\emptyset 2$. " \underline{Ad} follows Bn "
 (b) \underline{Bd} will go true every time An is true from Po thru $P32$ time, excluding $P33$, with a 30 order in the "T" register during $\emptyset 2$. " \underline{Bd} follows An "

32 Load A from B

1. (a) \underline{Ad} = $(T8' T7' T6 T5 \emptyset 2) T4' T3' Bn P33'$ 2L14
 (b) \underline{Bd} = $T8' T2 Bn$ 7J15

32 Load A from B (Cont'd.)

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. (a) Ad will go true every time Bn is true from Po thru P32 time, excluding P33, with a 32 order in the "T" register during ϕ_2 . "Ad follows Bn".
- (b) Bd will follow Bn (Po thru P33) with a 32 order in the "T" register.
"Normal recirculation"

34 Load A from E 2A9

1. (a) Ad = (T8' T7' T6 T5 T4' T3) ϕ_2 Po 2A11
- (b) Ad + (" " ") ϕ_2 An F4' OK4
- (c) + (" " ") ϕ_2 En P33' F4
2. (a) Er = T2' (En C) ϕ_0 ' 9C5
- (b) Er' = T2' (En' C) ϕ_0 ' 1B6

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. (a) Ad follows An for the LSH word time with a 34 order in the "T" register during ϕ_2 . "Normal Recirculation"
- (b) Ad follows En for the MSH word time excluding P33 with a 34 order in the "T" register during ϕ_2 . "Loading A from E"
2. (a) Recirculates the "E" line normally by En passing the ones to Er.
- (b) Same as (a) but passes the zeros.

Both equations will work as long as T2 is prime and ϕ_0 is prime, which means any other ϕ but ϕ_0 .

36 Exchange A and E

1. (a) Ad = (T8' T7' T6 T5 T4' T3) ϕ_2 Po 2A9
- (b) + (" " ") ϕ_2 An F4' 2A11
- (c) + (" " ") ϕ_2 En P33' F4 OK4
2. (a) Er = ϕ_0 ' F4' (En C) 7YY15
- (b) + (T8' T7' T6 T5 T4') (T3 T2) (An C) ϕ_2 F4 9C3
- (c) Er' = ϕ_0 ' F4' (En' C) 7YY4
- (d) + (T8' T7' T6 T5 T4') (T3 T2) (An' C) ϕ_2 F4 1B4

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

1. (a) Ad turns true at Po time with a 36 order in the "T" register during ϕ_2 .
- (b) Ad follows An for the LSH word time with a 36 order in the "T" register during ϕ_2 . "Normal Recirculation",
- (c) Ad follows En for the MSH word time excluding P33, with a 36 order in the "T" register during ϕ_2 .
2. (a) Er follows En (passing the ones) for the LSH word time in any ϕ but ϕ_0 .
(Recirculation of E during LSH word time)
- (b) Er follows An (passing the ones) for the MSH word time with a 36 order in the "T" register during ϕ_2 . (A to E)
- (c) Same as (a) but passing the zeros.
- (d) Same as (b) but passing the zeros.

38 Load A from D

1. (a) $\underline{Ad} = (T_8' T_7' T_6 T_5 \phi_2) T_4 T_3' D_n P_{33}'$ 2L10
- (b) $\underline{Dd} = T_2' D_n \phi_0'$ 5P2

Equations and explanations from this point are identical to the 22 order (4 thru 5b)

DESCRIPTION:

1. (a) Ad follows Dn from Po thru P32 excluding P33 with a 38 order in the "T" register during ϕ_2 .
- (b) Dd follows Dn (Po thru P33) with a 38 order in the "T" register and in any ϕ except ϕ_0 .

3A Exchange A and D

1. (a) $\underline{Ad} = (T_8' T_7' T_6 T_5 \phi_2) T_4 T_3' D_n P_{33}'$ 2L10
- (b) $\underline{Dd} = (T_8' T_7' T_6 T_5 \phi_2) (T_4 T_2) T_3' A_n$ 6P9

Equations and explanations from this point are identical to the 22 order (4 thru 5b)

DESCRIPTION:

1. (a) Ad follows Dn from Po thru P32 excluding P33 with a 3A order in the "T" register during ϕ_2 . At P33 time, Ad is prime.
- (b) Dd follows An from Po thru P33 with a 3A order in the "T" register during ϕ_2 .

NOTE: The P33 bit can be transferred from A to D but not from D to A.

3E Complement A

$$1. \quad \underline{Ad} = (T8' T7' T6 T5 \phi 2) T4 T3 An' P33' \quad 2L6$$

Equations and explanations from this point are identical to the 22 order (4 thru 5b).

DESCRIPTION:

1. Ad will go true everytime An is prime from Po thru P32 excluding P33 with a 3E order in the "T" register during $\phi 2$. Ad will go prime everytime An is true from Po thru P32. At P33 time, Ad will go prime regardless of the content of An.

41 Load B

After a " $\phi 2$ " look-up is accomplished, equations 1 thru 5b page 6, the following equations apply.

$$1. \quad \underline{Bd} = (T8' T6' T4') T7 T5' \phi 2 Vw Wn \quad 7I10$$

$$2. \quad (a) \quad \underline{Q4} = (T8' T7) (Vw P33 \phi 2) Ua' \quad 9010$$

$$(b) \quad + (\quad " \quad) (\quad " \quad) Us' \quad 907$$

$$(c) \quad \underline{\phi 2}' = Q4 C \quad 1U16$$

$$(d) \quad \underline{\phi 0} = Q4 C \quad 1U16$$

DESCRIPTION:

1. Bd driver follows Wn driver (Po thru P33) with a 41 order in the "T" register during $\phi 2$. "The Vw true in this equation indicates $\phi 2$ look-up has been accomplished and Wn is ready with the information."
2. (a) Q4 turns on during P33 time after the copying operation has taken place (Vw) with the "T" register in the proper configuration for this order during $\phi 2$ and with Ua prime.
 - (b) Same as 2a but if Us is prime.
 - (c) Sequencing equations out of $\phi 2$ to $\phi 0$.
 - (d)

After a "Ø2" look-up is accomplished, equations 1 thru 5b page 6, the following equations apply.

- | | | | | | | | |
|----|-----|-----------|---|---|-------|-----------------|------|
| 1. | (a) | $Q8$ | = | $T8' T7 T5' Ae C$ | | | 1G14 |
| | (b) | $Q8'$ | = | $T8' T7 T5' Ae' C$ | | | 1G4 |
| 2. | | $Q7$ | = | $(T8' T7 T5' T4 T3')(\phi_2 Vw)$ | | | 5T16 |
| 3. | (a) | $H3$ | = | $(R7' R6' \theta r') (Q7 \phi_2 C) Q8 + (R7 + R6 + \theta r') (Q7 \phi_2) (H2 C)$ | 5G13 | 6G6 | |
| | (b) | $H3'$ | = | $(") (") Q8' + (") (") (H2' C)$ | 7G14 | 8G15 | |
| | (c) | $I3$ | = | $(R7' R6' \theta r') (") Q8 + (R7 + R6 + \theta r') (") (I2 C)$ | 8G13 | 9G12 | |
| | (d) | $I3'$ | = | $(") (") Q8' + (") (") (I2' C)$ | 9G5 | 0G8 | |
| | (e) | $J3$ | = | $(R7' R6 \theta r') (") Q8 + (R7 + R6' + \theta r') (") (J2 C)$ | 1E6 | 2E3 | |
| | (f) | $J3'$ | = | $(") (") Q8' + (") (") (J2' C)$ | 3E11 | 3E2 | |
| | (g) | $K3$ | = | $(R7' R6 \theta r') (") Q8 + (R7 + R6' + \theta r') (") (K2 C)$ | 4E8 | 5E9 | |
| | (h) | $K3'$ | = | $(") (") Q8' + (") (") (K2' C)$ | 5E4 | 6E14 | |
| | (i) | $L3$ | = | $(R7 R6' \theta r') (") Q8 + (R7' + R6 + \theta r') (") (L2 C)$ | 7E10 | 8E5 | |
| | (j) | $L3'$ | = | $(") (") Q8' + (") (") (L2' C)$ | 9E2 | 0E8 | |
| | (k) | $M3$ | = | $(R7 R6' \theta r') (") Q8 + (R7' + R6 + \theta r') (") (M2 C)$ | 1C12 | 2C14 | |
| | (l) | $M3'$ | = | $(") (") Q8' + (") (") (M2' C)$ | 5A6 | 6A11 | |
| | (m) | $N3$ | = | $(R7 R6 \theta r') (") Q8 + (R7' + R6' + \theta r') (") (N2 C)$ | 8A2 | 0A14 | |
| | (n) | $N3'$ | = | $(") (") Q8' + (") (") (N2' C)$ | 0A9 | 1YY16 | |
| | (o) | $O3$ | = | $(R7 R6 \theta r') (") Q8 + (R7' + R6' + \theta r') (") (O2 C)$ | 1YY13 | 2YY14 | |
| | (p) | $O3'$ | = | $(") (") Q8' + (") (") (O2' C)$ | 2YY9 | 2YY3 | |
| 4. | (a) | $Q4$ | = | $(T8' T7) (Vw P33 \phi_2) Ua'$ | | | 9010 |
| | (b) | | + | $(") (") Us'$ | | | 907 |
| | (c) | ϕ_2' | = | $Q4 C$ | | | 1U16 |
| | (d) | ϕ_0 | = | $Q4 C$ | | | 1U16 |
| 5. | (a) | $Q7$ | = | $(T8' T7 T6' T5') T4 Q4$ | | | 5012 |
| | (b) | Uk | = | $Q7 Q4 Va Vw C$ | | | 1U8 |
| 6. | | Ad | = | $T6' An$ | | | 1L12 |

NOTE: There are also equations to recirculate the "WS" that is being copied into before Q7 turns true.

DESCRIPTIONS:

NOTE: "Q8" is a FF.

1. (a) Q8 FF turns true everytime Ae is true and with the proper setting in the "T" register. "Passes the ones"
- (b) This equation passes the zeros.
2. Q7 driver turns true when the proper word is selected (Vw) with the proper order in the "T" register during ϕ_2 . "Q7 remains on for one word time"
3. (a thru p) equations select the proper FF in the proper WS line that follows the Q8 FF.

NOTE: The "or" equations keep the non-selected working storages recirculating normally while information is being copied into the selected working storage.

4. (a) Q4 turns on during P33 time after the operation has taken place (Vw), with the "T" register in the proper configuration for this order during ϕ_2 and with Ua prime.
- (b) Same as (4a) but if Us is prime.
- (c)
- (d) } Sequencing equations out of ϕ_2 to ϕ_0 .
5. (a) Q7 driver turns on with the proper configuration in the "T" register and Q4.
- (b) Uk FF turns on when Q7 and Q4 are on and there is coincidence between the configuration of the "S" register and the "R" register as indicated by Va and Vw respectively.

6. Normal recirculation of "A" register.

NOTE: When there is a coincidence between the "S" and "R" registers, a situation arises whereby the command in MSH word (P17 thru P32) is to operate on (or modify) the LSH word which is stored in the "E" line. However, contents of "E" line cannot be changed directly. Therefore, the corresponding address (or location) in appropriate working storage is operated on or modified. Hence, the contents of the "E" line will differ from contents of its corresponding address in the appropriate working storage. This situation requires that the computer "jump" or transfer out of normal sequence and perform a mode III S8 Uk ϕ_0 look-up (page 5) in order to obtain the correct instruction word.

The coincidence between the "S" and "R" registers is only checked by the right hand character, therefore, there may not be full coincidence and no jump is needed, but the computer always prepares for it.

4D Store Address From A

After " $\emptyset 2$ " look-up is accomplished, equations 1 thru 5b page 6, the following equations apply.

1. (a) $Q8 = (T8' T7 T5') Ae C$ 1G14
- (b) $Q8' = (\quad " \quad) Ae' C$ 1G4
2. (a) $Q7 = (T8' T7 T6' T5' T3 T2' \emptyset 2 Vw) F4 F3' R8'$ 5T3
- (b) $+ (\quad " \quad " \quad " \quad) F4' F3' R8$ 6T12

Equations and explanations from this point are identical to the 49 order (3 thru 6).

DESCRIPTION:

1. (a) Q8 FF turns true everytime Ae is true and with the proper setting in the "T" register. "Passes the ones"
- (b) This equation passes the zeros.
2. (a) Q7 turns on during the address position of the MSH word time with the "T" register in the proper configuration after the word has been selected (Vw) during $\emptyset 2$. This happens if the "R" register contains a MSH word address as indicated by R8 prime. Q7 allows the copying operations to take place.
- (b) Same as (a) but Q7 turns on during the address portion of the LSH word time as indicated by the "R" register with R8 true.

4F Store Half-Word From A

After a " $\emptyset 2$ " look-up is accomplished, equations 1 thru 5b page 6, the following equations apply.

1. (a) $Q8 = (T8' T7 T5') Ae C$ 1G14
- (b) $Q8' = (\quad " \quad) Ae' C$ 1G4
2. (a) $Q7 = (T8' T7 T6' T5' T4 T2 \emptyset 2 Vw) F4 R8'$ 5T12
- (b) $+ (\quad " \quad " \quad " \quad) F4' Po' R8$ 5T9

Equations and explanations from this point are identical to the 49 order (3 thru 6).

DESCRIPTION:

1. (a) Q8 FF turns true everytime Ae is true and with the proper setting in the "T" register. "Passes the ones"
- (b) This equations passes the zeros.
2. (a) Q7 turns on during the MSH word time with the "T" register in the proper configuration after the word has been selected (Vw) during $\emptyset 2$. This happens if the "R" register contains a MSH word address indicated by R8 being prime. Q7 allows copying operation to take place.
- (b) Q7 turns on during the LSH word time excluding Po as indicated by (Po') with the "T" register in the proper configuration if the word has been selected (Vw) during $\emptyset 2$. This happens if the "R" register contains a LSH word address as indicated by R8 true.

Overflow Non-sequencing Situations from $\phi 1$ to $\phi 2$.

- | | | | | |
|----|-----|---|---------------------|------|
| 1. | (a) | $A4 = (T8 T7 T6 T5') (\phi 1 Z)$ | (Mult. & Divide) | 1R15 |
| | (b) | $+ (T8' T7 T6' T5 T4' T3') (\phi 1 Z)$ | (Compare Magnitude) | 1R10 |
| | (c) | $+ (T8' T7 T6 T5' T4') (\phi 1 Z)$ | (Add & Sub.) | 1R8 |
| | (d) | $+ (T8 T7' T6 T5 T4) (\phi 1 Z)$ | (Long Add & Sub.) | 1R5 |
| | (e) | $+ (T8' T7' T6 T5' T4') (\phi 1 Z)$ | (Round) | 2Y14 |
| | (f) | $+ (T8 T7' T6' T5 T4' T3' T2') (\phi 1 Z) (R8' R7 R6' R5') (Magnetic Tape)$ | | 9N13 |
| | (g) | $+ (R1 * R2 * R3 * R4 *) R8 (R7 \overline{A8}' + R7' \overline{A8}) \phi 1$ | (") | 9N12 |
| 2. | (a) | $Q3 = \phi 1 A2' A4' Ho G P33$ | (Automatic Control) | CJ6 |
| | (b) | $+ \phi 1 Gg P33$ | (Manual Control) | 4R5 |

DESCRIPTION:

Before any arithmetic command is performed, the overflow flip-flop (Z) must be off. If Z FF is on, an overflow condition is present from the preceding arithmetic command. The sequencing driver, Q3, does not turn on because A4 driver is true. A4 driver is true because Z is true. (See equations 1a to 1g and equation 2a). Q3 cannot be true when Z is true except in manual operation. The computer does not sequence from $\phi 1$ to $\phi 2$ during the present arithmetic command.

The following commands are affected by the above described conditions: 22, 51, 61, 63, 65, 67, BD, BF, E1, E3, E5, E7, E9, EB, ED, EF, and some magnetic tape commands.

51 Compare Magnitude

If the computer sequences from $\phi 1$ to $\phi 2$, check page 21. a " $\phi 2$ " look-up, page 6, is performed and the following equations apply.

- | | | | |
|----|-----|---|------|
| 1. | (a) | $Z = (T8' T7 T6' T5 T4' T2' \phi 2 Vw) (Po' P33') (An' C) Wn$ | 3Y16 |
| | (b) | $Z' = (" " " ") (") (An C) Wn'$ | 5Y15 |

Equations and explanations from this point are identical to the 41 order (2a thru 2d).

DESCRIPTION:

- (a) The Z FF turns on from P1 thru P32 time when An has a zero and Wn has a one with the "T" register in the proper configuration and the proper word selected (Vw) during $\phi 2$.
- (b) The Z FF turns off from P1 thru P32 time when An has a one and Wn has a zero with the "T" register in the proper configuration and the proper word selected (Vw) during $\phi 2$.

NOTE: The magnitude of the word in the "A" line and the selected word in WS are compared. If "A" is equal to, or greater than, "W", Z turns off and if "W" is larger, Z turns on. Each time "A" and "W" are alike, Z remains unchanged.

57 Load E

After a " ϕ^2 " look-up is accomplished, page 6, the following equations apply.

- | | | | | | |
|--------|------------------|-------------------|--|---|------|
| 1. (a) | \underline{Er} | = | $(T8' T7 T6' T5 T4' T3) (\phi^2 Vw) Wn C F4$ | OC15 | |
| | (b) | + | $\phi_0' F4' (En C)$ | 7YY10 | |
| | (c) | \underline{Er}' | = | $(T8' T7 T6' T5 T4' T3) (\phi^2 Vw) Wn' C F4$ | 2B16 |
| | (d) | + | $\phi_0' F4' (En' C)$ | 7YY4 | |

Equations and explanations from this point are identical to the 41 order (2a thru 2d).

DESCRIPTION:

1. (a) Er goes true everytime Wn is true from P17 thru P33 with a 57 order in the "T" register after the proper word is selected (Vw) during ϕ^2 .
- (b) Recirculates the ones in the LSH of "E" line in any ϕ but ϕ_0 .
- (c) Er goes prime everytime Wn' is prime from P17 thru P33 with a 57 order in the "T" register after the proper word is selected (Vw) during ϕ^2 .
- (d) Recirculates the zeros in the LSH of "E" line in any ϕ but ϕ_0 .

NOTE: Since there are no normal recirculation terms for the MSH of "E" line during ϕ^2 of this operation, the "E" line is cleared while the computer is trying to get Vw to turn on.

5B Load D

After a " ϕ^2 " look-up is accomplished, page 6, the following equations apply.

- | | | | | |
|----|------------------|---|-------------------------------------|------|
| 1. | \underline{Dd} | = | $(T8' T7 T6' T5 T4) (\phi^2 Vw) Wn$ | 6P13 |
|----|------------------|---|-------------------------------------|------|

Equations and explanations from this point are identical to the 41 order (2a thru 2d).

DESCRIPTION:

1. Dd follows Wn from Po thru P33 with a 5B order in the "T" register after the proper word is selected (Vw) during ϕ^2 .

61 Add

1. $\underline{Us}' = \phi 1 P33 C$ 1BB14

If the computer sequences from $\phi 1$ to $\phi 2$, check page 21. a " $\phi 2$ " look-up, page 6, is performed and the following equations apply.

2. (a) $\underline{Ad} = (T8' T7) (\phi 2 Vw') An$ 4L6
 (b) $+ (T8' T7 T6 T5' T4' T2' \phi 2 Vw) Wn Po$ 4L12
3. (a) $\underline{Us} = (T8' T7 T6 T5' T4' T3' Po Vw) Wn' (An C)$ 9Z3
 (b) $+ (" " " ") Wn (An'C)$ 0Z13
4. (a) $\underline{Ad} = (T8' T7 T6 T5' T4' \phi 2 Vw P33') Po' Ua An Wn$ 4L2
 (b) $+ (" " " ") Po' Ua An' Wn'$ 5L14
 (c) $+ (" " " ") Po' Ua' An Wn' \checkmark$ 5L9
 (d) $+ (" " " ") Po' Ua' An' Wn \checkmark$ 5L3
5. (a) $\underline{Ua} = (T8' T7 T6 T5' T4') (Po' P33' \underline{Us}' \phi 2 Vw) Wn (An C)$ 7W6
 (b) $+ (" ") (" \underline{Us} ") Wn' (An C) \checkmark$ 7W2
 (c) $\underline{Ua}' = (" ") (" \underline{Us}' ") Wn' (An'C)$ 9W7
 (d) $+ (" ") (" \underline{Us} ") Wn (An'C) \checkmark$ 9W3
 (e) $+ P33 C^3$ 2C2
6. $\underline{Ad} = (T8' T7 T6 T5' T4' \phi 2 Vw) Ua Us' P33$ 1FF16
7. $\underline{Z} = (T8' T7 T6 T5' T4' \phi 2 Vw) (Ua Us' P33 C)$ 3Y7
8. (a) $\underline{Q4} = (T8' T7) (Vw P33 \phi 2) Ua'$ 9010
 (b) $+ (") (") Us'$ 907
 (c) $\phi 2' = Q4 C$ 1U16
 (d) $\phi 0 = Q4 C$ 1U16
9. (a) $\underline{Q3} = (T8' T7) (\phi 2 Vw) P33 Ua Us$ 3R10
 (b) $\phi 2' = \phi 2 Q3 C$ 2U14
 (c) $\phi 3 = \phi 2 Q3 C$ 2U14
10. (a) $\underline{Ad} = (T8' T6 \phi 3) Ua' An' P33' \checkmark$ 6L10
 (b) $+ (") Ua An$ 6L13
 (c) $\underline{Ua} = \phi 2' (Po C)$ 8W5
 (d) $\underline{Ua}' = \phi 3 Po' Us (An C)$ 0W6
11. (a) $\underline{Q4} = T8' T7 \phi 3 P33$ 904
 (b) $\phi 3' = Q4 C$ 1U16
 (c) $\phi 0 = Q4 C$ 1U16

DESCRIPTION:

1. Us FF turns prime at the fall of P33 during $\phi 1$.
2. (a) Ad driver follows An with the "T" register in the order configuration before the proper word from WS is selected (Vw') during $\phi 2$. "Normal Recirculation"
 (b) Ad driver follows Wn at Po time (setting the sign) with a 6l order in the "T" register after the proper word is selected (Vw) during $\phi 2$.
3. (a) Us turns true if at Po time Wn is prime (-) and An is true (+) with a 6l order in the "T" register after the proper word is selected (Vw) during $\phi 2$.
 (b) Us turns true if at Po time Wn is true (+) and An is prime (-) with a 6l order in the "T" register after the proper word is selected (Vw) during $\phi 2$.

NOTE: The status of Us FF indicates whether an addition or subtraction is to be performed.

Us' = Add

Us = Subtract

4. (a thru d) equations are the logic for a "half-adder" which generates the "sum" or difference during magnitude portion of a word.
5. (a thru d) equations are the logic for another "half-adder" which generates a "carry" or "borrow" during addition or subtraction, respectively and is applicable during magnitude portion of a word.
 (e) Resets the Ua flip flop to prime at the fall of every P33 time.
6. Ad writes a one at P33 time and thus preserves the carry which may be generated during the P32 operation when performing an addition (Us').
7. The Z FF is turned on at P33 time if a carry is generated at P32 time when performing an addition (Us').
8. (a) During a subtraction (Us true) the Ua FF must be prime at P33 time or else the "difference" in the "A" register is erroneous.
 (b) Generates Q4 signal during normal addition.
 (c) }
 (d) } Sequences the computer from $\phi 2$ to $\phi 0$ if an addition or a valid subtraction has taken place.
9. (a) If the subtraction which has just been completed during $\phi 2$ time is erroneous, indicated by Ua true, generate a Q3 signal.
 (b) }
 (c) } Sequences computer from $\phi 2$ to $\phi 3$.
10. (a) Ua is prime at all Po times (equation 5e) hence the sign is changed from plus to minus or vice versa. From P2 thru P32 time the Ua FF status will vary according to the contents of the "A" register.
 (b) At P1 time the Ua FF is true (Equation 10c) Ad will then follow An.

10. (c) At any ϕ but $\phi 2$ at fall of P_0 time, turn U_a FF true.
(d) Permits U_a to be turned prime by the first "one" in the "A" register except at P_0 time.

NOTE: Equation 10a thru d rectify the erroneous subtraction which took place during $\phi 2$ by changing the sign, and performing a true complement on the magnitude portion of the "A" register.

True complement means changing all zeros to ones, all ones to zeros, and then adding one.

11. (a) Q_4 is needed to sequence out of $\phi 3$.
(b)
(c)) Sequence the computer from $\phi 3$ to $\phi 0$.

63 Add and Change Sign

Equations and explanations are identical to the 61 order except for the substitution of the following,

$$2. (b) \underline{Ad} = (T8' T7 T6 T5' T4' T2 \emptyset 2 Vw) Wn' Po \quad 4L16$$

DESCRIPTION:

2. (b) Ad turns on if at Po time Wn is prime, setting the sign positive. If at Po time Wn is true Ad writes a zero setting the sign minus, provided in both cases there is a 63 order in the "T" register after the proper word is selected (Vw) during $\emptyset 2$.

65 Subtract and Change Sign

Equations and explanations are identical to the 61 order except for the substitution of the following:

$$2. (b) \underline{Ad} = (T8' T7 T6 T5' T4' T2' \emptyset 2 Vw) Wn Po \quad 4L12$$

$$3. (a) \underline{Us} = (T8' T7 T6 T5' T4' T3 \emptyset 2 Vw) Wn An \quad 0Z10$$

$$(b) \quad + (\quad " \quad " \quad " \quad " \quad) Wn' An' \quad 0Z7$$

DESCRIPTION:

2. (b) Ad goes true if Wn is true at Po time, sets sign to positive, Ad writes a zero at Po time if Wn is prime, sets sign to minus.
3. (a) Us turns true if at Po time Wn and An are true.
 (b) Us turns true if at Po time Wn and An are prime.

NOTE: A subtraction will take place if the above 3a or 3b takes place.

67 Subtract

Equations and explanations are identical to the 65 order except for the substitution of the following:

$$2. (b) \underline{Ad} = (T8' T7 T6 T5' T4' T2 \emptyset 2 Vw) Wn' \textcircled{Po} \quad 4L16$$

DESCRIPTION:

2. (b) Ad turns on if at Po time Wn is prime, setting the sign positive. If at Po time Wn is true Ad writes a zero, setting the sign minus, provided in both cases there is a 67 order in the "T" register after the proper word is selected (Vw) during $\emptyset 2$.

69 Exchange A and W

This order is identical to the 49 order page 19, excluding equations 5a and 6, and including the equations that follow:

$$1. \quad \underline{Q6} = T8' T7 T6 T4 T3' \emptyset 2 Vw \quad 5T10$$

$$2. (a) \underline{Ad} = T8' P33' Q6 Wn \quad 6L7$$

$$(b) \quad + (T8' T7 T6 T4 \emptyset 2) Q6' An \quad 7L15$$

DESCRIPTION:

1. Q6 driver turns true after the proper word is selected (Vw) with the "T" register in the configuration for this order during $\phi 2$. Q6 remains true for one word time.
2. (a) Ad will follow Wn from Po thru P32, a zero is placed at P33 time, with the "T" register in the configuration for this order and with Q6 true.
 (b) Ad follows An while Q6 is prime with the "T" register in the proper configuration. "Recirculates the "A" line normally before Vw turns true".

6D Place Address in A

After $\phi 2$ look-up is accomplished, page 6, the following equations apply:

1. (a) $Q6 = (T8' T7 T6 T4 \phi 2 Vw) (T3 T2') R8' F4 F3' P33'$ 1T7
 (b) $+ (\quad " \quad) (\quad " \quad) R8 F4' F3'$ 1T2
2. (a) $Ad = (T8' T7 T6 T4 \phi 2) Q6' An$ 7L15
 (b) $+ T8' Q6 Wn P33'$ 6L7

Equations and explanations from this point are identical to the 41 order equations (2a thru 2d).

DESCRIPTION:

1. (a) Q6 turns on during the address portion of the MSH word time with the "T" register in the proper configuration after the word has been selected (Vw) during $\phi 2$. This happens if the "R" register contains a MSH word address as indicated by R8 prime.
 (b) Same as (a) but Q6 turns on during the address portion of the LSH word time as indicated by the "R" register with R8 true.
2. (a) Ad follows An during the time Q6 is prime which recirculates the portion of "A" not being copied into from Ws. This happens if there is the proper order in the "T" register during $\phi 2$.
 (b) Ad follows Wn during the time Q6 is true which copies in the information from WS. This happens if there is the proper order in the "T" register.

6F Place Half-word in A

After " $\phi 2$ " look-up is accomplished page 6, the following equations apply:

1. (a) $Q6 = (T8' T7 T6 T4 \phi 2 Vw) (T3 T2) R8' F4 P33'$ 2T12
 (b) $+ (\quad " \quad) (\quad " \quad) R8 F4' Po'$ 2T8

Equations and explanations from this point are identical to the 6D order.

DESCRIPTION:

1. (a) Q6 turns on during the MSH word time, excluding P33, with the "T" register in the proper configuration after the word has been selected (Vw) during $\phi 2$. This happens if the "R" register contains a MSH word address as indicated by R8 prime.
- (b) Same as (a) except during the LSH word time, excluding Po, as indicated by the "R" register with R8 true.

71 Extract with D Mask

After $\phi 2$ look-up is accomplished page 6, the following equations apply:

1. (a) $\underline{Ad} = (T8' T7 T6 T5 T4' T3' \phi 2 Vw) Wn Dn P33'$ 7L5
- (b) $+ (\quad " \quad " \quad " \quad) An Dn' P33'$ 8L15

Equations and explanations from this point are identical to the 41 order 2a thru 2d .

DESCRIPTION:

1. (a) Ad goes true when Wn and Dn are true from Po thru P32 time with a 71 order in the "T" register after the proper word is selected (Vw) during $\phi 2$. "Ad follows Wn when Dn is true".
- (b) Ad goes true when An is true and Dn is prime from Po thru P32 time with a 71 order in the "T" register after the proper word is selected (Vw) during $\phi 2$. "Ad follows An when Dn is prime".

75 Extract

After " $\phi 2$ " look-up is accomplished page 6, the following equations apply:

1. (a) $\underline{Ad} = (T8' T7 T6 T5 T4' \phi 2 Vw) T3 An Wn P33'$ 7L9

Equations and explanations from this point are identical to the 41 order (2a thru 2d).

DESCRIPTION:

1. (a) Ad goes true if An and Wn are true from Po thru P32 time with a 75 order in the "T" register after the proper word is selected (Vw) during $\phi 2$. "Ad follows An when Wn is true".

79 Load A from W

After a " $\phi 2$ " look-up is accomplished page 6, the following equations apply:

1. (a) $\underline{Q6} = T8' T7 T6 T4 T3' \phi 2 Vw$ 1T10
2. (a) $\underline{Ad} = (T8' T7 T6 T4 \phi 2) Q6' An$ 7L15
- (b) $+ T8' Q6 Wn P33'$ 6L7

Equations and explanations from this point are identical to the 41 order (2a thru 2d).

DESCRIPTION:

1. (a) Q6 driver turns true after the proper word is selected (Vw) with a 79 order in the "T" register during ϕ_2 . "Q6 is true for one word time".
2. (a) Ad follows An while Q6 is prime with a 79 order in the "T" register during ϕ_2 . "Recirculates the "A" line normally".
- (b) Ad follows Wn from Po thru P32 time when Q6 is true and there is a 79 order in the "T" register. "Copies "W" to "A".

81 Copy to Working Storage I

- | | | | |
|-----|--|-----------------------------|---------|
| 1. | $\underline{Md}' = \phi_1 C$ | <i>Read out of main mem</i> | 9B8 |
| 2. | (a) $\underline{Q2} = (T8 T7' T6' T5') \phi_0' \phi_1'$ | | 7T10 |
| | (b) + P _{Q2} | | J105-KK |
| 3. | $\underline{PAi} = (Q2' + Ri')$ | (i = 1 thru 8 pre-amps) | |
| 4. | (a) $\underline{Vo} = P33 F C$ | | 2B4 |
| | (b) $\underline{Vo}' = (F5 F C) P33'$ | | CY12 |
| 5. | (a) $\underline{Ut} = T7' Vo (P33 C)$ | | 7DD6 |
| | (b) $\underline{Ut}' = T7' Vo' (P33 C)$ | | 7DD3 |
| | (c) + T7' $\phi_6 (Q3 C)$ | | OY14 |
| 6. | (a) $\underline{Q3} = (A2' Ut Q2 F5 F2' F1) \phi_7' \phi_6' \phi_1'$ | | 6Q8 |
| | (b) $\phi_2' = \phi_2 Q3 C$ | | 2U14 |
| | (c) $\phi_3 = \phi_2 Q3 C$ | | 2U14 |
| | (d) $\phi_3' = \phi_3 Q3 C$ | | 2U12 |
| | (e) $\phi_4 = \phi_3 Q3 C$ | | 2U12 |
| | (f) $\phi_4' = \phi_4 Q3 C$ | | 2U8 |
| | (g) $\phi_5 = \phi_4 Q3 C$ | | 2U8 |
| 7. | $\underline{Q7} = Q2 T4' (\phi_5 + \phi_6)$ | | 6T8 |
| 8. | (a) $\underline{H3} = (Q7 \phi_2') (T3' T2' C) Mr$ | | 5G15 |
| | (b) $\underline{H3}' = (") (") Mr'$ | | 6G3 |
| 9. | (a) $\underline{Q3} = (A2' Ut Q2 F5 F2' F1) \phi_7' \phi_6' \phi_1'$ | | 6Q8 |
| | (b) $\phi_5' = \phi_5 Q3 C$ | | 2U6 |
| | (c) $\phi_6 = \phi_5 Q3 C$ | | 2U6 |
| | (d) $\underline{Q3} = (A2' Ut Q2 F5 F2' F1) \phi_6 T4'$ | | OP5 |
| | (e) $\phi_6' = \phi_6 Q3 C$ | | 2U4 |
| | (f) $\phi_7 = \phi_6 Q3 C$ | | 2U4 |
| 10. | (a) $\underline{X1} = P33 C$ | | 2C3 |
| | (b) $\underline{X1}' = H2 (T3' T2' C) (P33' Mr')$ | | 3C15 |
| | (c) + H2' (") (P33' Mr) | | 4C15 |

81 Copy to Working Storage I (Cont'd)

11. (a)	<u>A2</u> = T8 T7' T6' T5' ϕ 7 X1' C	5C4
	(b) <u>A2'</u> = Apr Ut Q2 ϕ 7 P33 Md' A2 C	4E12
	(c) + Ap2 C	6C11
	(d) + SC	6C9
12. (a)	<u>Q3</u> = Apr Ut Q2 ϕ 7 P33 Md' A2	4E13
	(b) ϕ 7' = ϕ 7 Q3 C	2U9
	(c) ϕ 3 = ϕ 7 Q3 C	2U10
13. (a)	<u>Q4</u> = Ut Q2 ϕ 7 P33 Md' A2'	9I12
	(b) ϕ 7' = Q4 C	1U16
	(c) ϕ 0 = Q4 C	1U16

DESCRIPTION:

- Md turns prime every ϕ 1 time.
- (a) Q2 driver turns true in any ϕ except ϕ 0 and ϕ 1, with the "T" register in the proper configuration.
(b) Q2 turns true when the NORMAL-HOLD-SELECT Switch is in the SELECT position (PQ2).
- When Q2 or Ri is prime PAi turns true. "i" indicates the 1 thru 8 FFs in the "R" register corresponding to the selection drivers used for controlling the relays in the matrix.

NOTE: Because of phase inversion in the circuitry when the PA is true the driver is false and the relay coil in the plate circuit of the driver is de-energized. If Q2 and Ri are both true, PA turns prime therefore the relay associated with the particular driver circuit will be energized.

- (a) Vo turns on at the fall of P33 every time there is a P33 bit in the "F" line (F). "Word 10 thru 1F".
(b) Vo turns prime from P28 to P31 (F5) anytime there is a bit in the "F" line (F) excluding P33. "Turns prime during word 10 thru 1F".

NOTE: Vo remains true from the fall of P33 time in word 1F until the fall of P28 time in word 01 in the "F" line.

- (a) Ut turns true if Vo is true at the fall of P33 time with the "T" register in the order configuration.
(b) Ut turns prime if Vo is prime at the fall of P33 time with the "T" register in the order configuration.
(c) Ut turns prime when Q3 is true and the "T" register is in the order configuration during ϕ 6.

81 Copy to Working Storage (Cont'd)

6. (a) Q3 driver turns true if the block transfer alarm is prime (A2'), Ut is true, Q2 is true at P30 time (F5 F2' F1) in any ϕ except $\phi 1$, $\phi 6$ or $\phi 7$. "Q3 driver is true for one pulse time P30 during word 01."

(b thru g) equation sequences the computer from $\phi 2$ to $\phi 5$. This takes one drum revolution per ϕ time because of the action of the Q3 driver and its terms.

7. Q7 turns true when Q2 is true with the "T" register in the proper order configuration during $\phi 5$ and $\phi 6$.

8. (a) H3 turns true every time Mr is true with Q7 true and the "T" register in the order configuration during $\phi 5$ and $\phi 6$. "H3 follows the ones from Mr".

(b) Same as 8a except H3 turns prime when Mr is prime. "H3 follows the zeros from Mr".

NOTE: Above 2 equations are the copying equations which take place for two drum revolutions $\phi 5$ and $\phi 6$.

9. (a) Q3 driver turns true for one pulse time at the fall of P30 time in word 01 if the other condition in the equations are met. "Sequences the computer from $\phi 5$ to $\phi 6$ while the copying operation is taking place".

(b) } Sequencing equation from $\phi 5$ to $\phi 6$
 (c) }

(d) Q3 turns true for one pulse time at the fall of P30 time in word 01 during $\phi 6$ if the other conditions in the equation are met.

(e) } Sequencing equations from $\phi 6$ to $\phi 7$
 (f) }

10. (a) X1 FF turns true at every P33 time.

(b) X1 turns prime every time H2 is true and Mr is prime from Po thru P32 and with the "T" register in the order configuration.

(c) Same as 10b except when H2 is prime and Mr is true.

NOTE: Comparing Equations.

11. (a) A2 turns true if X1 is prime and the "T" register in the order configuration during $\phi 7$.

"This indicates in conjunction with equations 10b and 10e that an improper block copy has been made".

(b) A2 turns prime if the ALARM SWITCH #1 is in the SILENCE position (Apr), Q2 is true, Ut is true, Md is prime, A2 is true during P33 time in $\phi 7$.

"With SW #1 in the SILENCE position and the remainder of the equation fulfilled the computer will try repeatedly to recopy the information correctly".

81 Copy to Working Storage I (Cont'd)

- (c) A2 turns prime if the ALARM SWITCH #1 is in the RESTORE position (Ap2).
"Computer will sequence to $\emptyset 0$ ".
- (d) A2 turns prime if the NORMAL-TEST-CLEAR SWITCH is in the CLEAR position (SC)
12. (a) Q3 turns true during P33 time if ALARM SWITCH #1 is in the SILENCE position, Ut is true, Q2 is true, Md is prime, A2 is true during $\emptyset 7$.
"Q3 will reset the computer to $\emptyset 3$ and the copying operation will be done repeatedly. When copying is accomplished correctly the computer goes to $\emptyset 0$."
- (b) } Sequences the computer to $\emptyset 3$.
(c) }
13. (a) Q4 driver turns true if a successful copy has been made as indicated by A2'.
(b) } Sequences the computer back to $\emptyset 0$.
(c) }

83 Copy to working Storage II

Equations and explanations identical to the 81 order except for the following substitutions:

8. (a) $\underline{J3} = (Q7 \emptyset 2') (T3' T2 C) Mr$ 1E10
(b) $\underline{J3}' = (") (") Mr'$ 3E16
10. (b) $\underline{X1}' = J2 (T3' T2 C) (P33' Mr')$ 3C12
(c) $+ J2' (") (P33' Mr)$ 4C14

85 Copy to Working Storage III

Equations and explanations identical to the 81 order except for the following substitutions:

8. (a) $\underline{L3} = (Q7 \emptyset 2') (T3 T2' C) Mr$ 7E12
(b) $\underline{L3}' = (") (") Mr'$ 9E4
10. (b) $\underline{X1}' = L2 (T3 T2' C) (P33' Mr')$ 3C9
(c) $+ L2' (") (P33' Mr)$ 4C11

87 Copy to Working Storage IV

Equations and explanations identical to the 81 order except for the following substitutions:

8. (a) $\underline{N3} = (Q7 \emptyset 2') (T3 T2 C) Mr$ 8A4
(b) $\underline{N3}' = (") (") Mr'$ 0A11

87 Copy to Working Storage IV (Cont'd)

10. (b) X1' = N2 (T3 T2 C) (P33' Mr')
(c) + N2' (") (P33' Mr)

306

408

89 Copy from Working Storage I

- | | | |
|---------|--|-------------------------|
| 1. | $\underline{Md}' = \phi_1 C$ | 9B8 |
| 2. (a) | $\underline{Q2} = (T8 T7' T6' T5' \phi_0' \phi_1')$ | 7T10 |
| | (b) $+ P Q_2$ | J105-KK |
| 3. | $\underline{PAi} = (Q2' + Ri')$ | (i = 1 thru 8 pre-amps) |
| 4. (a) | $\underline{Vo} = P33 F C$ | 2B4 |
| | (b) $\underline{Vo}' = (F5 F C) P33'$ | 3Y12 |
| 5. (a) | $\underline{Ut} = T7' Vo (P33 C)$ | 7DD6 |
| | (b) $\underline{Ut}' = T7' Vo' (P33 C)$ | 7DD3 |
| | (c) $+ T7' \phi_6 (Q3 C)$ | OY14 |
| 6. (a) | $\underline{Q3} = (A2' Ut Q2 F5 F2' F1) \phi_7' \phi_6' \phi_1'$ | 6Q8 |
| | (b) $\underline{\phi_2}' = \phi_2 Q3 C$ | 2U14 |
| | (c) $\underline{\phi_3} = \phi_2 Q3 C$ | 2U14 |
| 7. | $\underline{Md} = (T8 T7' T6' T5' T4) \phi_3 C$ | 9B12 |
| 8. (a) | $\underline{\phi_3}' = \phi_3 Q3 C$ | 2U12 |
| | (b) $\underline{\phi_4} = \phi_3 Q3 C$ | 2U12 |
| | (c) $\underline{\phi_4}' = \phi_4 Q3 C$ | 2U8 |
| | (d) $\underline{\phi_5} = \phi_4 Q3 C$ | 2U8 |
| 9. | $\underline{Cr}' = (A2' Ut Q2 F5 F2' F1) \phi_5 C$ | 3Z13 |
| 10. (a) | $\underline{Mp} = (T3' T2') (\phi_5 Md) Os He$ | 8F13 |
| | (b) $+ Mp' Os' (")$ | OE10 |
| | (c) $\underline{Mp}' = (T3' T2') (") Os He'$ | 8F16 |
| | (d) $+ Mp Os'$ | OE12 |
| | (e) $\underline{Mo} = (T3' T2') (\phi_5 Md) Os He'$ | 8F16 |
| | (f) $+ Mo' Os' (")$ | OE7 |
| | (g) $\underline{Mo}' = (T3' T2') (") Os He$ | 8F13 |
| | (h) $+ Mo Os'$ | OE14 |
| 11. (a) | $\underline{\phi_5}' = \phi_5 Q3 C$ | 2U6 |
| | (b) $\underline{\phi_6} = \phi_5 Q3 C$ | 2U6 |
| 12. | $\underline{Md}' = (T8 T7' T6' T5' T4) \phi_6 C$ | 9B10 |
| 13. (a) | $\underline{Cr} = T4 \phi_6 (A2' Ut Q2 F5 F2' F1) Cr' C$ | 3Z16 |
| | (b) $\underline{Cr}' = T4 \phi_6 (") Cr C$ | 3Z13 |
| 14. (a) | $\underline{Q3} = T4 \phi_6 (") Cr$ | 1015 |
| | (b) $\underline{\phi_6}' = \phi_6 Q3 C$ | 2U4 |
| | (c) $\underline{\phi_7} = \phi_6 Q3 C$ | 2U4 |

15. (a) X1 = P33 C 2C3
 (b) X1' = H2 (T3' T2' C) (P33' Mr') 3C15
 (c) + H2' (") (P33' Mr) 4C15
16. (a) A2 = T8 T7' T6' T5' ϕ 7 X1' C 5C4
 (b) A2' = Apr Ut Q2 ϕ 7 P33 Md' A2 C 4E12
 (c) + Ap2 C 6C11
 (d) + SC 6C9
17. (a) Q3 = Apr Ut Q2 ϕ 7 P33 Md' A2 4E13
 (b) ϕ 7' = ϕ 7 Q3 C 2U9
 (c) ϕ 3 = ϕ 7 Q3 C 2U9
18. (a) Q4 = Ut Q2 ϕ 7 P33 Md' A2' 9I12
 (b) ϕ 7' = Q4 C 1U16
 (c) ϕ o = Q4 C 1U16

DESCRIPRION:

Explanations for equations 1 thru 6c are identical to 81 order equations 1 thru 6c.

7. Md FF turns true in $\phi 3$ with proper setting in "T" register. Changes the "head" wires to the write amplifier by use of Md relay.
 8. (a thru d) equations sequence computer from $\phi 3$ to $\phi 5$ in conjunction with equation 6a.
 9. Cr FF turns prime in $\phi 5$ at P30 time if other terms are present. "Cr is used for delay purposes in later equations".
 10. (a thru h) refer to Ferranti system write up.
 11. (a) Sequencing from $\phi 5$ to $\phi 6$ in conjunction with equation 6a.
(b)
 12. Md FF turns prime during $\phi 6$ with proper setting in "T" register.
 13. (a) During $\phi 6$ at P30 time, other conditions being true, Cr turns true. "One drum revolution".
(b) During $\phi 6$ at P30 time, other condition being true, Cr turns prime. "Second drum revolution".
- NOTE: Equations 13a and b hold computer in $\phi 6$ for two drum revolutions to allow Md relay to drop out.
14. (a) Q3 turns true at P30 time during the second drum revolution in $\phi 6$, other conditions being true.
(b) Sequences computer from $\phi 6$ to $\phi 7$.
(c)
 15. Explanations from this point are identical to 81 order 10a thru 13c.

8B Copy from Working Storage II

Equations and explanations are identical to the 89 order except for the following substitutions:

- | | | | | | |
|-----|-----|--------------------|---|------------------------------------|------|
| 10. | (a) | \underline{M}_p | = | (T3' T2) (\emptyset 5 Md) Os Je | 8F2 |
| | (b) | | + | M_p' Os' (") | OE10 |
| | (c) | \underline{M}_p' | = | (T3' T2) (") Os Je' | 9F10 |
| | (d) | | + | M_p Os' | OE12 |
| | (e) | \underline{M}_o | = | (T3' T2) (") Os Je' | 7F4 |
| | (f) | | + | M_o' Os' (") | OE7 |
| | (g) | \underline{M}_o' | = | (T3' T2) (") Os Je | 7F4 |
| | (h) | | + | M_o Os' | OE14 |
| 15. | (b) | \underline{X}_1' | = | J2 (T3' T2 C) (P33' Mr') | 3C12 |
| | (c) | | + | J2' (") (P33' Mr) | 4C14 |

8D Copy from Working Storage III

Equations and explanations are identical to the 89 order except for the following substitutions:

- | | | | | | |
|-----|-----|--------------------|---|------------------------------------|------|
| 10. | (a) | \underline{M}_p | = | (T3 T2') (\emptyset 5 Md) Os Le | 8F7 |
| | (b) | | + | M_p' Os' (") | OE10 |
| | (c) | \underline{M}_p' | = | (T3 T2') (") Os Le' | 8F10 |
| | (d) | | + | M_p Os' | OE10 |
| | (e) | \underline{M}_o | = | (T3 T2') (") Os Le' | 8F10 |
| | (f) | | + | M_o' Os' (") | OE7 |
| | (g) | \underline{M}_o' | = | (T3 T2') (") Os Le | |
| | (h) | | + | M_o Os' (") | OE14 |
| 15. | (b) | \underline{X}_1' | = | L2 (T3 T2' C) (P33' Mr') | 3C9 |
| | (c) | | + | L2' (") (P33' Mr) | 4C11 |

8F Copy from Working Storage IV

Equations and explanations are identical to the 89 order except for the following substitutions:

- | | | | | | |
|-----|-----|--------------------|---|-----------------------------------|------|
| 10. | (a) | \underline{M}_p | = | (T3 T2) (\emptyset 5 Md) Os Ne | 9F16 |
| | (b) | | + | M_p' Os' (") | OE10 |
| | (c) | \underline{M}_p' | = | (T3 T2) (") Os Ne' | 9F13 |
| | (d) | | + | M_p Os' | OE12 |
| | (e) | \underline{M}_o | = | (T3 T2) (") Os Ne' | 9F13 |
| | (f) | | + | M_o' Os' (") | OE7 |

8F Copy from Working Storage IV (Cont'd)

- | | | |
|-----|--|------|
| | (g) <u>Mo'</u> = (T3 T2) (Ø5 Md) Os Ne | 9F16 |
| | (h) + Mo Os' | OE14 |
| 15. | (b) <u>X1'</u> = N2 (T3 T2 C) (P33' Mr') | 3C6 |
| | (c) + N2' (") (P33' Mr) | 4C8 |

99 Neither Type Nor Punch

- | | | |
|----|--|------|
| 1. | (a) <u>Yp'</u> = T8 T7' T6' T5 T4 T3' Ø2 C | 1A10 |
| | (b) + SC | 6C9 |
| 2. | <u>Yt'</u> = T8 T7' T6' T5 T4 T2' Ø2 C | 1A6 |
| 3. | (a) <u>Q3</u> = T8 T7' T6' T5 T4 Ø2 Vo P33 | 6O12 |
| | (b) <u>Ø2'</u> = Ø2 Q3 C | 2U14 |
| | (c) <u>Ø3</u> = Ø2 Q3 C | 2U14 |
| 4. | (a) <u>Q4</u> = T8 T7' T6' T5 T4 Ø3 Vo P33 | 8T8 |
| | (b) <u>Ø3'</u> = Q4 C | 1U16 |
| | (c) <u>Øo</u> = Q4 C | 1U16 |

DESCRIPTION:

1. (a) Yp FF turns prime with the proper setting in the "T" register during Ø2. "The punch relay in the flex de-energizes"
- (b) Pressing the NORMAL-TEST-CLEAR switch to the CLEAR position (SC) de-energizes the punch relay.
2. Yt FF turns prime with the proper setting in the "T" register during Ø2. "The type relay in the flex de-energizes."
3. (a) Q3 turns on during P33 in Ø2 when Vo is true with the proper setting in the "T" register.
- (b) Sequences the computer from Ø2 to Ø3.
- (c)
4. (a) Q4 turns true during P33 in Ø3 when Vo is true with the proper setting in the "T" register.
- (b) Sequences the computer from Ø3 to Øo.
- (c)

NOTE: This command allows one drum revolution (or longer) for the relays to drop out.

9B Type

- | | | | | | |
|----|-----|--------------------|---|--|------|
| 1. | (a) | \underline{Y}_p' | = | (T8 T7' T6' T5 T4 \emptyset 2 C) T3' | 1A10 |
| | (b) | | + | SC | 6C9 |
| 2. | (a) | \underline{Y}_t | = | (T8 T7' T6' T5 T4 \emptyset 2 C) T2 | 1A8 |
| | (b) | | + | SC | 6C9 |

Equations and explanations from this point are identical to the 99 order 3a thru 4c.

DESCRIPTION:

1. (a) Y_p turns prime with the proper setting in the "T" register during \emptyset 2.
- (b) Pressing the NORMAL-TEST-CLEAR switch to the CLEAR position (SC) turns Y_p prime.
2. (a) Y_t turns true with the proper setting in the "T" register during \emptyset 2.
- (b) Pressing the NORMAL-TEST-CLEAR switch to the CLEAR position (SC) turns Y_t true.

9D Punch

- | | | | | | |
|----|--|--------------------|---|---------------------------------------|------|
| 1. | | \underline{Y}_p | = | (T8 T7' T6' T5 T4 \emptyset 2 C) T3 | 1A12 |
| 2. | | \underline{Y}_t' | = | (" " ") T2' | 1A6 |

Equations and explanations from this point are identical to the 99 order 3a thru 4c.

DESCRIPTION:

1. Y_p turns true with the proper setting in the "T" register during \emptyset 2.
2. Y_t turns prime with the proper setting in the "T" register during \emptyset 2.

9F Both Type and Punch

- | | | | | | |
|----|-----|-------------------|---|---------------------------------------|------|
| 1. | | \underline{Y}_p | = | (T8 T7' T6' T5 T4 \emptyset 2 C) T3 | 1A12 |
| 2. | (a) | \underline{Y}_t | = | (" " ") T2 | 1A8 |
| | (b) | | + | SC | 6C9 |

Equations and explanations from this point are identical to the 99 order 3a thru 4c.

DESCRIPTION:

1. Y_p turns true with the proper setting in the "T" register during \emptyset 2.
2. (a) Y_t turns true with the proper setting in the "T" register during \emptyset 2.
- (b) Pressing the NORMAL-TEST-CLEAR switch to the CLEAR position turns Y_t true.

A1 Long Right Shift

- | | | | | | | |
|----|-----|----------------------------------|---|-------------------------------------|--|-------|
| 1. | (a) | <u>Ad</u> | = | (T8 T7' T6 T5' T4' $\emptyset 2$) | T2' Ae Po' P33' | 0L15 |
| | (b) | | + | (") | An Po | 1K13 |
| 2. | (a) | <u>Bd</u> | = | (T8 T7' T6 T5' T4' $\emptyset 2$) | (T3' T2') (Po' P32') Be | 1L13 |
| | (b) | | + | (") | P32 Ub | 1I9 |
| | (c) | | + | T8 $\emptyset 4'$ $\emptyset 5'$ | Po Bn | 9J14 |
| 3. | (a) | <u>Ub</u> | = | T7' An PlC | | 6Y13 |
| | (b) | <u>Ub'</u> | = | T7' An' PlC | | 8Y13 |
| 4. | (a) | <u>Um</u> | = | (T8 T7' T6 T5') | T4' (R6 + R5 + R4 + R3 + R2 + R1) P33C | 8EE9 |
| | (b) | <u>Um'</u> | = | (") | T4' (R6' R5' R4' R3' R2' R1') P33C | 8EE5 |
| 5. | (a) | <u>R1</u> | = | (T8 T7' T6 T5' $\emptyset 2$ P32 C) | R1' | 3DD12 |
| | (b) | <u>R1'</u> | = | (") | R1 | 3DD10 |
| | (c) | <u>R2</u> | = | (") | R1' R2' | 4DD10 |
| | (d) | <u>R2'</u> | = | (") | R1' R2 | 4DD8 |
| | (e) | <u>R3</u> | = | (") | R1' R2' R3' | 5DD14 |
| | (f) | <u>R3'</u> | = | (") | R1' R2' R3 | 5DD8 |
| | (g) | <u>R4</u> | = | (") | R1' R2' R3' R4' | 5DD2 |
| | (h) | <u>R4'</u> | = | (") | R1' R2' R3' R4 | 6DD16 |
| | (i) | <u>R5</u> | = | (") | R1' R2' R3' R4' R5' | 6DD14 |
| | (j) | <u>R5'</u> | = | (") | R1' R2' R3' R4' R5 | 6DD11 |
| | (k) | <u>R6'</u> | = | (") | R1' R2' R3' R4' R5' | 6DD13 |
| 6. | (a) | <u>Q4</u> | = | (T8 T7' T6 T5') | T4' $\emptyset 2$ Po Um' | 002 |
| | (b) | <u>$\emptyset 2'$</u> | = | Q4C | | 1U16 |
| | (c) | <u>$\emptyset 0$</u> | = | Q4C | | 1U16 |

DESCRIPTION:

1. (a) Ad follows Ae from P1 thru P32 time. "Shifting the P2 thru the P33 bits."
 (b) Ad follows An at Po time. "Recirculates the sign."
2. (a) Bd follow Be from P1 thru P33 time excluding P32 time. "Shifts the P2 thru the P32 bits also puts the Po bit in the P33 position."
 (b) Bd follows Ub at P32 time. "Transfers the P1 bit from "A" to the P32 position of "B"."
 (c) Bd follows Bn. "Recirculates the sign of "B"."
3. (a))
 (b)) Ub follows the configuration of An at P1 time.

NOTE: As the right shift operation takes place the P33 position of the "A" line is filled with zeroes.

4. (a) Um turns true whenever there is a true R1 thru R6 FF. "Indicates more shifting is to be performed."
 (b) Um turns prime when R1 thru R6 are prime. "Indicates shifting operations completed."
5. (a thru k) Equations used to count down the "R" register as each "word time" shift is completed.
6. (a) Q4 turns true when Um is prime and with other conditions fulfilled. "Um prime indicates the required number of shifts have been completed."
 (b))
 (c)) Sequence the computer from ϕ_2 to ϕ_0 .

A3 Long Left Shift

1. (a) Ad = (T8 T7' T6 T5' T4' ϕ_2) T2 A1 Po' P1' P33' 0L8
 (b) + (T8 T7' T6 T5' T4' ϕ_2) An Po 1K13
 (c) + (T8 T7' T6 T5' T4' ϕ_2) T3' T2 Ub P1 1K15
2. (a) Bd = (T8 T7' T6 T5' T4' ϕ_2) T3' T2 B1 Po' P1' P33' 1I5
 (b) + T8 ϕ_4' ϕ_5' Po Bn 9J14
3. (a) Ub = Bd P32C 6Y15
 (b) Ub' = Bd' P32C 8Y15

Equations and explanations from this point are identical to the A1 order 5 thru 6c.

DESCRIPTION:

1. (a) Ad follows A1 from P2 thru P32 time. "Shifting bits P1 thru P31 left."
 (b) Ad follows An at Po time. "Recirculates the sign of "A" line."
 (c) Ad follows Ub at P1 time. "Transfers the configuration of the P32 bit in the "B" line to the "A" line."
2. (a) Bd follows B1 from P2 thru P32 time. "Shifting bits P1 thru P31 left."
 (b) Bd follows Bn at Po time. "Recirculates the sign of "B" line."

NOTE: As the left shift operation takes place the P1 position of the "B" line is filled with zeroes.

3. (a) } Ub follows the configuration of Bd at P32 time.
 (b) }

A5 A Right Shift

1. (a) $\underline{Ad} = (T8 T7' T6 T5' T4' \emptyset 2) T2' Ae Po' P33'$ OL15
 (b) $+ (T8 T7' T6 T5' T4' \emptyset 2) An Po$ 1K13

Equations and explanations from this point are identical to the A1 order equations 4 thru 6c.

DESCRIPTION:

1. (a) Ad follows Ae from P1 thru P32 time. "Shifting the P2 thru P33 bits."
 (b) Ad follows An at Po time. "Recirculates the sign in the "A" line."

A7 A Left Shift

1. (a) $\underline{Ad} = (T8 T7' T6 T5' T4' \emptyset 2) T2 A1 Po' P1' P33'$ OL8
 (b) $+ (T8 T7' T6 T5' T4' \emptyset 2) An Po$ 1K13

Equations and explanations from this point are identical to the A1 order equations 4 thru 6c.

DESCRIPTION:

1. (a) Ad follows A1 from P2 thru P32 time. "Shifting the P1 thru P31 bits."
 (b) Ad follows An at Po time. "Recirculates the sign in the "A" line."

AB Shift and Count

1.	(a)	<u>Ad</u> = (T8 T7' T6 T4) ϕ 2 Bn Po	9L15
	(b)	+ (T8 T7' T6 T4 T3') ϕ 2 An Po'	8K13
2.		<u>Bd</u> = (") T2 ϕ 2 Bn	2I15
3.	(a)	<u>Ub</u> = Bd P32 C	6Y15
	(b)	<u>Ub'</u> = Bd' P32 C	8Y15
4.	(a)	<u>Um</u> = (T8 T7' T6 T4 T3' T2 Po' P33' ϕ 2) Ad C	7Z13
	(b)	+ (" ") Bd C	7Z16
	(c)	<u>Um'</u> = ϕ 2' ϕ 3' P32 C	7Z10
5.	(a)	<u>Q3</u> = (T8 T7' T6 T4 T3') ϕ 2 P32	4R9
	(b)	<u>ϕ2'</u> = ϕ 2 Q3 C	2U14
	(c)	<u>ϕ3</u> = ϕ 2 Q3 C	2U14
6.	(a)	<u>Ad</u> = (T8 T7' T6 T4 T3') T2 ϕ 2' An Po	9K16
	(b)	+ (") ϕ 3 Ub P1	2K14
	(c)	+ (") ϕ 3 A1 Po' P1' P33'	8K9
7.	(a)	<u>Bd</u> = T8 ϕ 4' ϕ 5' Bn Po	9J14
	(b)	+ (T8 T7' T6 T4 T3') T2 ϕ 3 B1 Po' P1' P33'	2I3
8.	(a)	<u>Uc</u> = (T8 T7' ϕ 0') Po C	8Y6
	(b)	<u>Uc'</u> = (") Dn' Po' C	9Y16
9.	(a)	<u>Dd</u> = (T8 T7' T6 T5' T4 ϕ 0' ϕ 1' ϕ 2') Po	8P14
	(b)	+ (" ") Dn' Uc	7P4
	(c)	+ (" ") Dn Uc'	8P15
10.	(a)	<u>Q4</u> = (T8 T7' T6 T4 T3' T2 ϕ 3 P33) Um'	8T2
	(b)	+ (" ") Ar	1U5
	(c)	<u>ϕ3'</u> = Q4 C	1U16
	(d)	<u>ϕ0</u> = Q4 C	1U16

DESCRIPTION:

1. (a) Ad follows Bn at Po time in ϕ 2. "Sets sign of "A" to same configuration of sign in "B"."
- (b) Ad follows An from P1 thru P33 time during ϕ 2. "Recirculates "A" line normally."
2. Bd follows Bn from Po thru P33 time during ϕ 2. "Recirculates "B" line normally."
3. (a)) Ub follows the configuration of Bd at P32 time.
- (b)

4. (a) Um turns true if Ad is true from P1 thru P32 time.
- (b) Um turns true if Bd is true from P1 thru P32 time.
- (c) Um turns prime at P32 time in every ϕ except $\phi 2$ and $\phi 3$.

NOTE: Um true causes the computer to perform or repeat shifting operation.

5. (a) Q3 turns true during P32 in $\phi 2$.
- (b) Sequences the computer from $\phi 2$ to $\phi 3$.
- (c)
6. (a) Ad follows An at Po in an ϕ except $\phi 2$. "Recirculates the sign of "A" normally."
- (b) Ad follows Ub at P1 time. "Transfers the configuration of the P32 bit in the "B" line to the "A" line."
- (c) Ad follows A1 from P2 thru P32 time. "Shifting bits P1 thru P31 left."
7. (a) Bd follows Bn at Po time in any ϕ except during $\phi 4$ and $\phi 5$. "Recirculates the sign."
- (b) Bd follows B1 from P2 thru P32 time. "Shifting bits P1 thru P31 left."
8. (a) Uc turns true at Po time in any ϕ except $\phi 0$.
- (b) Uc turns prime from P1 thru P33 time whenever Dn is prime in any ϕ but $\phi 0$

NOTE: Uc is used in conjunction with Dd to "count" the number of left shifts.

9. (a) Dd turns true at Po time during $\phi 3$. "Sets sign plus."
- (b) Used to add one to the "D" line each time a shift takes place.
-) Also recirculates the remainder of the "D" line.
- (c)

NOTE: Since there are no recirculation equations for the "D" line during $\phi 2$ with this order configuration in the "T" register, the "D" line is cleared and the sign set to minus.

10. (a) Q4 turns true during P33 time in $\phi 3$ if Um is prime.
- (b) Q4 turns true during P33 time in $\phi 3$ if Ar is true. "This equation stops the shifting action by checking to see if there is a "one" bit in the Ar FF. Ar contains the P32 bit at P33 time."
- (c)
-) Sequences the computer from $\phi 3$ to $\phi 0$.
- (d)

4. (a) Um turns true if Ad is true from P1 thru P32 time.
 (b) Um turns true if Bd is true from P1 thru P32 time.
 (c) Um turns prime at P32 time in every ϕ except $\phi 2$ and $\phi 3$.

NOTE: Um true causes the computer to perform or repeat shifting operation.

5. (a) Q3 turns true during P32 in $\phi 2$.
 (b) Sequences the computer from $\phi 2$ to $\phi 3$.
 (c)
6. (a) Ad follows An at Po in an ϕ except $\phi 2$. "Recirculates the sign of "A" normally."
 (b) Ad follows Ub at P1 time. "Transfers the configuration of the P32 bit in the "B" line to the "A" line."
 (c) Ad follows A1 from P2 thru P32 time. "Shifting bits P1 thru P31 left."
7. (a) Bd follows Bn at Po time in any ϕ except during $\phi 4$ and $\phi 5$. "Recirculates the sign."

(b) Bd follows B1 from P2 thru P32 time. "Shifting bits P1 thru P31 left."

8. (a) Uc turns true at Po time in any ϕ except $\phi 0$.
 (b) Uc turns prime from P1 thru P33 time whenever Dn is prime in any ϕ but $\phi 0$

NOTE: Uc is used in conjunction with Dd to "count" the number of left shifts.

9. (a) Dd turns true at Po time during $\phi 3$. "Sets sign plus."
 (b) Used to add one to the "D" line each time a shift takes place.
) Also recirculates the remainder of the "D" line.
 (c)

NOTE: Since there are no recirculation equations for the "D" line during $\phi 2$ with this order configuration in the "T" register, the "D" line is cleared and the sign set to minus.

10. (a) Q4 turns true during P33 time in $\phi 3$ if Um is prime.
 (b) Q4 turns true during P33 time in $\phi 3$ if Ar is true. "This equation stops the shifting action by checking to see if there is a "one" bit in the Ar FF. Ar contains the P32 bit at P33 time."
 (c)
) Sequences the computer from $\phi 3$ to $\phi 0$.
 (d)

B5 Load A from M

After a " $\emptyset 2$ " look-up is accomplished, page 6, the following equations apply.

- | | | |
|--------|---|------|
| 1. | <u>Q6</u> = (T8 T7' T6 T5 T4' T2' $\emptyset 2$ Vw) Or' (C1 C2 C3 C4 C5 C6) | 2T3 |
| 2. | <u>Ad</u> = T8 Q6 P33' Mr ← | 6L4 |
| 3. (a) | <u>Q4</u> = T8 T7' Q6 P33 | 7I2 |
| | (b) <u>$\emptyset 2'$</u> = Q4 C | 1U16 |
| | (c) <u>$\emptyset 0$</u> = Q4 C | 1U16 |

DESCRIPTION:

1. Q6 turns true after the proper word is selected (Vw) in $\emptyset 2$ when Or is prime.
2. Ad follows Mr from Po thru P32 time when Q6 is true.
3. (a) Q4 turns true during P33 when Q6 is true.
 - (b) } Sequences the computer from $\emptyset 2$ to $\emptyset 0$.
 - (c) }

1. $\underline{Us}' = \phi_1 P33 C$ 1BB14
 If the computer sequences from ϕ_1 to ϕ_2 , check page 21, a " ϕ_2 " look up, page 6, is performed and the following equations apply.
2. (a) $\underline{Ad} = (T8 T7' T6 T4) \phi_2 Po Bn$ 9L15
 (b) $+ (T8 T7' T6 T4 T3) \phi_2 Po' An$ 8L14
3. (a) $\underline{Bd} = T8 \phi_4' \phi_5' Po Bn$ 9J14
 (b) $+ (T8 T7' T6 T4 T3 \phi_2 Vw') Bn$ 9J15
4. (a) $\underline{Us} = (T8 T7' T6 T4 T3 T2' Po Vw) Wn Bn' C$ 1BB7
 (b) $+ (\quad " \quad) Wn' Bn C$ 1BB2
5. (a) $\underline{Bd} = (T8 T7' T6 T4 T3 \phi_2 Vw Po') Ua Bn Wn$ 8J15
 (b) $+ (\quad " \quad) Ua Bn' Wn'$ 8J13
 (c) $+ (\quad " \quad) Ua' Bn Wn'$ 8J9
 (d) $+ (\quad " \quad) Ua' Bn' Wn$ 8J5
6. (a) $\underline{Ua} = (T8 T7' T6 T4 T3) (Po' P33' Us' \phi_2 Vw) Wn Bn C$ 8W2
 (b) $+ (\quad " \quad) (" \quad " \quad Us \quad " \quad ") Wn Bn' C$ 8W9
 (c) $\underline{Ua}' = (\quad " \quad) (" \quad " \quad Us' \quad " \quad ") Wn' Bn' C$ 0W10
 (d) $+ (\quad " \quad) (" \quad " \quad Us \quad " \quad ") Wn' Bn C$ 0W15
 (e) $+ P33 C$ 2C2
7. (a) $\underline{Q3} = (T8 T7' T6 T4 T3) (\phi_2 Vw P33) Ua$ 3R2
 (b) $\phi_2' = \phi_2 Q3 C$ 2U14
 (c) $\phi_3 = \phi_2 Q3 C$ 2U14
8. (a) $\underline{Q4} = (T8 T7' T6 T4 T3) (\phi_2 Vw P33) Ua'$ 902
 (b) $\phi_2' = Q4 C$ 1U16
 (c) $\phi_0 = Q4 C$ 1U16
9. (a) $\underline{Ad} = (T8 T7' T6 T4 T3 \phi_3) Ua An' P33'$ 8L10
 (b) $+ (\quad " \quad) Ua' An P33'$ 8L6
 (c) $+ (\quad " \quad) Ua Us' P33$ 1K2
10. $\underline{Z}' = (\quad " \quad) Ua Us' P33 C$ 4Y6
11. (a) $\underline{Ua} = \phi_2' (Po C)$ 8W5
 (b) $\underline{Ua}' = \phi_3 Us Po' (An' C)$ 0W6
 (c) $+ \phi_3 Us' Po' (An' C)$ 0W2
12. $\underline{Bd} = (T8 T7' T6 T4 T3 \phi_3) Bn$ 0J14
13. (a) $\underline{Q3} = (\quad " \quad) Ua Us P33$ 4R13
 (b) $\phi_3' = \phi_3 Q3 C$ 2U12
 (c) $\phi_4 = \phi_3 Q3 C$ 2U12

14. (a) $\underline{Q4} = (T8 T7' T6 T4 T3 \emptyset3 P33) Us'$ 0013
 (b) $+ (\quad \quad \quad " \quad \quad \quad) Ua'$ 0010
 (c) $\underline{\emptyset3}' = Q4 C$ 1U16
 (d) $\underline{\emptyset c} = Q4 C$ 1U16
15. $\underline{Ad} = (T8 T7' T6 T4 T3 \emptyset4) An' P33'$ 8L2
16. (a) $\underline{Bd} = (\quad \quad \quad " \quad \quad \quad) Ua' Bn'$ 9J5
 (b) $+ (\quad \quad \quad " \quad \quad \quad) Ua Bn$ 9J9
17. (a) $\underline{Ua} = \emptyset2' (Po C)$ 8W5
 (b) $\underline{Ua}' = \emptyset4 Po' Bn C$ 9DD14
18. (a) $\underline{Q4} = (T8 T7' T6 T4 T3) \emptyset4 P33$ 007
 (b) $\underline{Q4}' = Q4' C$ 1U16
 (c) $\underline{\emptyset c} = Q4 C$ 1U16

DESCRIPTION:

1. Us FF turns prime at P33 time during $\phi 1$.
2. (a) Ad follows Bn at Po during $\phi 2$. "Sets the sign of "A" the same as the sign of "B".
(b) Ad follows An from P1 thru P33 time during $\phi 2$. "Recirculates the "A" line normally during $\phi 2$ ".
3. (a) Bd follows Bn at Po time in any ϕ but $\phi 4$, and $\phi 5$.
(b) Bd follows Bn during $\phi 2$ before the selected word (Vw').
4. (a) Us turns true if Wn is true (+) and Bn is prime (-) at Po time during $\phi 2$.
(b) Us turns true if Wn is prime (-) and Bn is true (+) at Po time during $\phi 2$.

NOTE: The status of Us FF indicates whether an addition or subtraction is to be performed.

Us' = Add

Us = Subtract

5. (a thru d) equations are the logic for a "half-adder" which generates the "sum" or "difference" during the magnitude portion of the words. (B register)
6. (a thru d) equations are the logic for another "half-adder" which generates a "carry" or "borrow" during addition or subtraction, respectively and is applicable during the magnitude portion of the words. (B register)
(e) Ua turns prime at every P33 time.
7. (a) Q3 turns true during P33 time if one of the three conditions that follow prevails. "Indication given by Ua true".
 1. A complete addition has not taken place and the computer must sequence into $\phi 3$ to continue operation.
 2. A complete subtraction has not taken place and the computer must sequence into $\phi 3$ to continue operation.
 3. An erroneous subtraction has taken place and the computer must sequence into the following ϕ 's to rectify this situation.
(b & c) Sequences the computer from $\phi 2$ to $\phi 3$.
8. (a) Q4 turns true during P33 time of $\phi 2$ if a complete addition or complete and valid subtraction has taken place.
(b & c) Sequences the computer from $\phi 2$ to $\phi 0$.
9. (a thru c) "Half-adder" used to generate a sum or difference in the "A" line. "Also recirculates the sign of "A" normally".
10. Equation will be discussed by instructor.

11. (a thru c) "Half-adder" used in conjunction with equations 9 to recirculate the sign of "A" and generate a carry or borrow during ϕ_3 .
12. Recirculates the "B" line normally during ϕ_3 .
13. (a) Q3 turns true during P33 of ϕ_3 to sequence the computer into ϕ_4 if an erroneous subtraction has taken place. "Indicated by Ua true Us true".
 - (b & c) Sequences the computer from ϕ_3 to ϕ_4 .
14. (a & b) Q4 turns true during P33 time of ϕ_3 if an addition has taken place (Us') or a valid subtraction (Ua').
 - (c & d) Sequences the computer from ϕ_3 to ϕ_0 .
15. Complements the contents of "A" during ϕ_4 excluding P33.
16. These equations are used to change the sign and perform a true complement (refer to 61 order for definition) on the erroneous subtraction.
17. (a) Same as 11 a
 - (b) Used in conjunction with 16 a & b.
18. (a thru c) Q4 turns true during P33 time and the computer sequences from ϕ_4 to ϕ_0 .

BF Subtract From B

Equations and explanations are identical to the BD order except for the following substitution:

4. (a) $\underline{U}_S = (T_8 T_7' T_6 T_4 T_3 T_2 P_0 V_w) W_n B_n C$ OZ2
 (b) $+ (\quad \quad \quad " \quad \quad \quad) W_n' B_n' C$ 1BB12

DESCRIPTION:

4. (a) U_S turns true if at P_0 time W_n and B_n are true. "Both signs plus".
 (b) U_S turns true if at P_0 time W_n and B_n are prime. "Both signs minus".

C3 Store E

1. (a) $\underline{Q}_8 = (T_8 T_7 T_6' T_5' T_4' T_3' T_2) E_e C$ 5G6
 (b) $\underline{Q}_8' = (\quad \quad \quad " \quad \quad \quad) E_e' C$ 9G6
 2. $\underline{Q}_7 = (T_8 T_7 T_6' T_5' T_4' T_3' \emptyset_2) F_4 V_w$ 5G11

Equations and explanations at this point are identical to the 49 order (3a thru 3p) page 19.

4. (a) $\underline{Q}_4 = (T_8 T_7 T_6' T_5') \emptyset_2 V_w P_{33}$ OJ4
 (b) $\underline{\emptyset}_2' = Q_4 C$ 1U16
 (c) $\underline{\emptyset}_0 = Q_4 C$ 1U16

DESCRIPTION:

1. (a) } Q_8 follows E_e when the "T" register is in a C3 configuration.
 (b) }
 2. Q_7 turns true during the MSH word time (F_4) of the selected word (V_w) during \emptyset_2 with the "T" register in a C3 configuration.
 4. (a) Q_4 turns true during P_{33} of the selected word (V_w) during \emptyset_2 .
 (b) } Sequences the computer from \emptyset_2 to \emptyset_0 .
 (c) }

C5 Store B

1. (a) $\underline{Q}_8 = (T_8 T_7 T_6' T_5' T_4' T_3 T_2') B_e C$ 1G11
 (b) $\underline{Q}_8' = (\quad \quad \quad " \quad \quad \quad) B_e' C$ 8G11
 2. $\underline{Q}_7 = T_8 T_7 T_6' T_5' T_4' T_3 \emptyset_2 V_w$ 6T11

Equations and explanations from this point are identical to the C3 order.

DESCRIPTION:

1. (a) } Q_8 follows B_e with the "T" register in a C5 configuration.
 (b) }
 2. Q_7 turns true from P_0 thru P_{33} during the selected word (V_w) in \emptyset_2 .

C7 Store D

Equations and explanations are identical to the C5 order, except for the following substitution.

- | | | |
|--------|---|-----|
| 1. (a) | $\underline{Q8} = (T8 T7 T6' T5' T4' T3 T2) De C$ | 1G7 |
| (b) | $\underline{Q8}' = (\quad \quad \quad " \quad \quad \quad) De' C$ | 8G7 |

DESCRIPTION:

- | | |
|--------|--|
| 1. (a) | } Q8 follows De with a C7 order in the "T" register. |
| (b) | |

D5 Sign Out

Equations and explanations are identical to the F5 order (To Flex or HSPTP) except for the following additions and substitutions.

- | | | | |
|-----|-----|---|------|
| 11. | (a) | $\underline{A_d} = T_6' A_n$ | 1L12 |
| | (b) | ----- | --- |
| 12. | (a) | ----- | --- |
| | (b) | $\underline{Y_1}' = (T_8 T_7 T_6' T_5 T_4' T_3 \phi_6 P_{33} C)$ | 5W14 |
| | (c) | $\underline{Y_2} = (\quad \quad \quad " \quad \quad \quad) Ae'$ | 5W8 |
| | (d) | $\underline{Y_2}' = (\quad \quad \quad " \quad \quad \quad) Ae$ | 5W10 |
| | (e) | $\underline{Y_3} = (\quad \quad \quad " \quad \quad \quad) Ae'$ | 5W8 |
| | (f) | $\underline{Y_3}' = (\quad \quad \quad " \quad \quad \quad) Ae$ | 5W10 |
| | (g) | $\underline{Y_4} = (\quad \quad \quad " \quad \quad \quad) Ae'$ | 5W8 |
| | (h) | $\underline{Y_4}' = (\quad \quad \quad " \quad \quad \quad) Ae$ | 5W10 |
| | (i) | $\underline{Y_5} = (\quad \quad \quad " \quad \quad \quad) Ae'$ | 5W8 |
| | (j) | $\underline{Y_5}' = (\quad \quad \quad " \quad \quad \quad) Ae$ | 5W10 |
| | (k) | ----- | --- |
| | (l) | $\underline{Y_6}' = (\quad \quad \quad " \quad \quad \quad)$ | 5W14 |

DESCRIPTION:

11. (a) Recirculates the "A" line in all ϕ 's.
 (b) -----
12. (a) -----
 (b & e) Y1 and Y6 are always set prime during ϕ_6 at P33 times. Insures no 1 or 6 punch.
12. (c thru j) At P33 the Y2 thru Y5 FF's are following the outputs of the Ae FF. At P33 time the sign bit is in Ae. If the sign is negative the Y2 thru 5 FF's are set true and when they fire the "one-shots" a 2 and 4 punch are made. (negative sign) If the sign is positive the Y2 thru Y5 FF's are set prime and when the "one-shots" are fired a 3 and 5 punch are made. (space)

DD Number Output

Equations and explanations are identical to the F5 order (Flex or HSFTP) except for the following substitutions and additions.

- | | | | | |
|---------|-----------|---|---------------------------------|------|
| 11. (a) | <u>Ad</u> | = | T6' An | 1L12 |
| 13. (a) | <u>Q3</u> | = | (T8 T7 T5 T4 T3) ϕ 6 F2 F1 | 505 |

DESCRIPTION:

11. (a) Recirculates the "A" line in all ϕ 's.
13. (a) In ϕ 6 Q3 comes up during P4 time and sequences the computer into ϕ 7 at the fall of P4.

NOTE:

In ϕ 7 Q3 cannot come up since T4 is true in a DD command. Therefore Q4 will come up in ϕ 7 to return the computer to ϕ 0 for look-up of the next command. Any information that may appear in R1 through R4 will be of no significance in the DD command.

E1 Multiply By D And Add A

If the computer sequences from ϕ_1 to ϕ_2 , check page 21, the computer performs the following:

1. $\underline{Ad} = (T8 T7 T5' \phi_2) T3' An$ 2K2
2. $\underline{Bd} = (\quad " \quad) Bn$ 4I14
3. (a) $\underline{Dd} = (\quad " \quad) Vw' Dn$ 6P6
 (b) $+ (\quad " \quad) Vw T2' Dn$ 7P15
4. (a) $\underline{Q3} = (T8 T7 T6 T5') \phi_2 Vw P33 (Z' + T4')$ 4R2
 (b) $\underline{\phi_2'} = \phi_2 Q3 C$ 2U14
 (c) $\underline{\phi_3} = \phi_2 Q3 C$ 2U14
5. (a) $\underline{Ut} = T7 Po Be C$ 2BB12
 (b) $\underline{Ut'} = T7 P32 C$ 2BB9
6. (a) $\underline{Ad} = (T8 T7 T5' T4' Ut \phi_0' \phi_1' \phi_2')(Po' P32') Ae De Uc$ 3K6
 (b) $+ (\quad " \quad)(\quad " \quad) Ae De' Uc'$ 3K2
 (c) $+ (\quad " \quad)(\quad " \quad) Ae' De Uc'$ 4K14
 (d) $+ (\quad " \quad)(\quad " \quad) Ae' De' Uc$ 4K10
 (e) $+ (\quad " \quad) P32 Uc$ 4K6
 (f) $+ (T8 T7 T5' T4' Ut' \phi_0' \phi_1' \phi_2')(Po' P32') Ae$ 5K10
7. (a) $\underline{Uc} = (T7 \phi_0' P33') Ae De C$ 8Y9
 (b) $\underline{Uc'} = T7 \phi_0' Ae' De' C$ 8Y4
 (c) $+ P33 C$ 2C3
8. (a) $\underline{Ub} = (T7 T4' P1) An Bn Dn' C$ 6Y9
 (b) $+ (\quad " \quad) An' Bn Dn C$ 6Y4
 (c) $+ (\quad " \quad) An Bn' C$ 7Y13
 (d) $\underline{Ub'} = (T7 T4' P1) An Bn Dn C$ 7Y10
 (e) $+ (\quad " \quad) An' Bn Dn' C$ 7Y6
 (f) $+ (\quad " \quad) An' Bn' C$ 7Y2
9. (a) $\underline{Bd} = T8 T7 \phi_5' Po Bn$ 5I16
 (b) $+ (T8 T7 T5' T4' \phi_0' \phi_1' \phi_2') (Po' P32') Be$ 3I13
 (c) $+ (\quad " \quad) P32 Ub$ 3I11
10. $\underline{Dd} = (T8 T7 T5') \phi_0' \phi_2' Dn P33'$ 7P11
11. (a) $\underline{Q3} = (\quad " \quad) \phi_0' \phi_1' \phi_2' Vw P33 + \phi_3 T8 T7 T6 T5' R8$ 6Q15
 (b) $\underline{\phi_3'} = \phi_3 Q3 C$ 2U12
 (c) $\underline{\phi_4} = \phi_3 Q3 C$ 2U12

12. (a) $\underline{Q3} = (T8 T7 T5') \phi_0' \phi_1' \phi_2' Vw P33$ 6Q15
 (b) $\underline{\phi_4'} = \phi_4 Q3 C$ 2U8
 (c) $\underline{\phi_5} = \phi_4 Q3 C$ 2U8
13. (a) $\underline{Ad} = (T8 T7 T5' T4' \phi_5) Bn Dn$ 4K2
 (b) $+ (\quad " \quad) Bn' Bn'$ 5K14
14. (a) $\underline{Bd} = (T8 T7 T5' \phi_5) Bn Dn$ 3I6
 (b) $+ (\quad " \quad) Bn' Dn'$ 3I3
15. (a) $\underline{Q4} = (\quad " \quad) Po$ 8T7
 (b) $\underline{\phi_5'} = Q4 C$ 1U16
 (c) $\underline{\phi_0} = Q4 C$ 1U16

DESCRIPTION:

1. Recirculates the "A" line during $\phi 2$.
2. Recirculates the "B" line during $\phi 2$.
3. (a & b) Recirculates the "D" line during $\phi 2$.
4. (a thru c) Q3 turns true during P33 time of $\phi 2$ and sequences the computer from $\phi 2$ to $\phi 3$
5. (a) Ut true indicates the LSB (Be at Po = P1 bit) in the multiplier is a "one", therefore, the operation will be shifting and adding.
 (b) Ut turns prime every P32 time with T7 true.

NOTE: If the "B" line doesn't contain a "one" at P1 time Ut remains prime and the operation will be of shifting only.

6. (a thru d) "Half-adder" that generates a sum (actually the product at the end of the entire operation). The addition takes place by using the early bits while a right shift is taking place in the "A" line.

(e) Used to record the carry (Uc) of one, if any, generate by the addition of the P32 bits.

(f) If no addition is to take place (Ut') this equation shifts the "A" line right only.

7. (a & b) "Half-adder" used to generate the carry during the add operation.

8. (a thru h) These equations are used to set the configuration of the Ub FF during this operation.

NOTE: Since the contents of "A" and "B" are shifted right, steps must be taken to preserve the sum of the P1 bits of "A" and "D". The Ub FF is used to store the sum of the P1 bits of "A" and "D" until P32 time. At P32 time, the content of Ub FF is transferred into the P32 position of the B line. The Ub FF stores the above sum from the fall of P1 time to the fall of P32 time. At the fall of P32 time, the Ub FF is set to conform with the content of the P32 position of the B line. The Ub FF contains this information until the fall of P1 time. However, this information is not used and consequently lost when the Ub FF is set once more with the sum of the P1 bits of "A" and "D" of the successive word time.

The P1 bit which is shifted out of the "B" line is lost but is of no further value and can be disregarded.

9. (a) Sign bit is recirculated normally.
(b) Magnitude portion of "B" is shifted right one place per word time.
(c) Contents of Ub FF transferred into P32 position of "B" from P1 of "A".
 10. Recirculates the multiplicand in "D" normally, no shifting.
 11. (a thru c) Sequencing from ϕ_3 to ϕ_4 .
 12. (a thru c) Sequencing from ϕ_4 to ϕ_5 .
 13. (a & b) Sign of A is **made** positive when Bn and Dn are alike.
 14. (a & b) Sign of B is made positive when Bn and Dn are alike.
 15. (a thru c) Sequence from ϕ_5 to ϕ_0 .
- NOTE: ϕ_5 is one pulse time in duration.

DESCRIPTION:

1. No equation in this order to recirculate "A", therefore, it is cleared during $\emptyset 2$.
2. Bd follows Bn. "Normal recirculation of the "B" line".
3. (a) Dd follows Dn with Vw prime. "Normal recirculation of "D" line before selected word".
(b) Dd follows Wn with Vw true. "Copies the multiplicand to the "D" line".

E9 Divide Double Length By D

If the computer sequences from $\phi 1$ to $\phi 2$, check page 21, the following is performed.

1. (a) \underline{Z} = (T8 T7 T5' T4 $\phi 2$ Vw)(Po C) 4Y15
- (b) + (") (Po' P33') Ad Dd' C 4Y13
- (c) \underline{Z}' = (") (") Ad' Dd C 5Y11
2. \underline{Ad} = (T8 T7 T5' $\phi 2$) T3' An 2K2
3. \underline{Bd} = (") Bn 4I14
4. (a) \underline{Dd} = (") Vw' Dn 6P6
- (b) + (") T2' Vw Dn 7F15
5. (a) \underline{Ud} = ($\phi 2$ P1) Ub C 1Z16
- (b) + (") Dd' C 2Z4
- (c) + ($\phi 2$ Po' P1' P32' P33') Ar Dd' C 1Z7
- ~~(d) + Br P32' C 1Z1~~
- (e) \underline{Ud}' = ($\phi 2$ P1) Ub' Dd C 1Z13
- (f) + ($\phi 2$ Po' P1' P32' P33') Ar' Dd C 1Z4
- ~~(g) + Br' P32 C 2Z15~~
6. (a) \underline{Ur} = ($\phi 2$ P32) Dd' Ud C 8Z14
- (b) + (") Ar Ud C 8Z12
- (c) + (") Ar Dd' C 8Z15
- (d) + Ad P32 C 7Z7
- (e) \underline{Ur}' = ($\phi 2$ P32) Ad' Ar' Dd C 9Z15
- (f) + (") Ad' Dd Ud' C 8Z2
- (g) + (") Ad' Ar' Ud' C 9Z12
7. (a) \underline{Ub} = Bd P32 C 6Y15
- (b) \underline{Ub}' = Bd' P32 C 8Y15
8. (a) $\underline{Q4}$ = (T8 T7 T5' T4) $\phi 2$ Vw P33 Z 6C12
- (b) $\underline{\phi 2}'$ = Q4 C 1U16
- (c) $\underline{\phi 0}$ = Q4 C 1U16
9. (a) $\underline{Q3}$ = (T8 T7 T6 T5') $\phi 2$ Vw P33 (Z' + T4') 4R2
- (b) $\underline{\phi 2}'$ = $\phi 2$ Q3 C 2U14
- (c) $\underline{\phi 3}$ = $\phi 2$ Q3 C 2U14
10. (a) \underline{Ad} = (T8 T7 T5' T4 $\phi 0'$ $\phi 1'$ $\phi 2'$ Po' P1' Ur) A1 Dn Uv 6K10
- (b) + (") A1' Dn' Uv 6K6
- (c) + (") A1' Dn Uv' 6K2
- (d) + (") A1 Dn' Uv' 7K14
- (e) + (T8 T7 T5' T4 $\phi 0'$ $\phi 1'$ $\phi 2'$) (Po' P1') Ur' A1 6K16

10. (f) + (T8 T7 T5' T4 ϕ_0' ϕ_1' ϕ_2') P1 Ur' Ub' 7K8
 (g) + (") P1 Ur Ub Dn' 7K4
 (h) + (") P1 Ur Ub' Dn 8K15
11. (a) Uv = Ub' Dn P1 C 2BB7
 (b) + A1' Dn (Po' P1') C 2EB4
 (c) Uv' = Po C 2BB28
 (d) + A1 Dn' P1' C 3BB16
12. (a) Bd = T8 T7 ϕ_5' Po Bn 5I16
 (b) + (T8 T7 T5' T4 ϕ_0' ϕ_1' ϕ_2') P1 Ur 5I7
 (c) + (")(Po' P1') B1 5I9
13. Dd = (T8 T7 T5' ϕ_0' ϕ_2') Dn P33' 7P11
14. (a) Ud = De' ϕ_2' Po C 1Z9
 (b) + Ad De' ϕ_2' Po' P32' P33' C 9Y5
 (c) + Br P32 C 1Z1
 (d) Ud' = Ad' De ϕ_2' Po' P32' P33' C 9Y2
 (e) + Br' P32 C 2Z15
15. (a) Ur = Ad P32 C 7Z7
 (b) + Ud ϕ_2' P32 C 8Z8
 (c) Ur' = Ad' Ud' ϕ_2' P32 C 8Z4
16. (a) Q3 = (T8 T7 T5' ϕ_0' ϕ_1' ϕ_2') Vw P33 6Q15
 (b) ϕ_3' = ϕ_3 Q3 C 2U12
 (c) ϕ_4 = ϕ_3 Q3 C 2U12
17. (a) Q3 = (T8 T7 T5' ϕ_0' ϕ_1' ϕ_2') Vw P33 6Q15
 (b) ϕ_4' = ϕ_4 Q3 C 2U8
 (c) ϕ_5 = ϕ_4 Q3 C 2U8
18. Ad = (T8 T7 T5' T4 ϕ_5) Bn 5K6
19. (a) Bd = (T8 T7 T5' ϕ_5) Bn Dn 3I6
 (b) + (") Bn' Dn' 3I3
20. Dd = (T8 T7 T5' ϕ_0' ϕ_2') Dn P33' 6Q15
21. (a) Q4 = (T8 T7 T5' ϕ_5) Po 8T7
 (b) ϕ_5' = Q4 C 1U16
 (c) ϕ_0 = Q4 C 1U16

DESCRIPTION:

To enable the student to grasp more easily the operation of the computer during the divide commands a short discussion of the philosophy employed during the execution follows:

1. As in all arithmetic commands in the ALMAC III-B, if the "Z" FF is on during $\phi 1$, due to an overflow generated by a previous arithmetic operation, the computer will stop. If the "Z" FF is not on during $\phi 1$, the computer sequences into $\phi 2$ to perform part of the divide operation.
2. Before the actual division operation is performed, by the use of the "Z" FF a check is made to determine whether the divisor, which is in the "D" line, is larger than the MSB of the dividend, which is in the "A" line. If the divisor is larger the computer will execute the command, if the divisor is equal to or smaller than the MSB of the dividend the command is not executed. The reason for the above is as follows: If the MSB of the dividend is equal to or larger than the divisor, the quotient that would be generated will be too large to be accommodated by the "B" line which is where it is to be placed.

Example: "Using the supposition of a one character recirculating line rather than an eight character recirculating line the principle is the same".

$$\begin{array}{r}
 17 \\
 5 \overline{) 89} \\
 \underline{5} \\
 39 \\
 \underline{35} \\
 4 \\
 \hline
 \hline
 \end{array}$$

- 5 - Divisor contained in the "D" line.
- 8 - MSB of the dividend contained in the "A" line.
- 9 - LSH of the dividend contained in the "B" line.
- 17 - Quotient generated and cannot be contained by the "B" line. "Remember the "B" line can accommodate only one character whereas the quotient generated contains two characters.
- 4 - Remainder generated and contained by the "A" line.

It can be seen readily that the computer is not able to cope with this situation therefore the division is not performed.

3. During the divide commands the computer has two alternatives, subtract and shift left, or merely shift left. ~~When~~ ^{IF DURING} subtraction takes place ~~is determined by considering~~ in the next word time, will the divisor be smaller than the shifted dividend. If the divisor can be subtracted a "one" is placed in the quotient and the subtraction and shift left take place simultaneously. If the divisor can not be subtracted from the present dividend a "zero" is placed in the quotient and ^{only} a shift left ~~only~~ takes place.
4. During $\phi 2$ (while the "Z" check, explained in #2, is taking place), the computer is also preparing to perform the divide operation if the divisor, in the case of the "Z" check proves to be larger than the MSB of the dividend. This checking operation between the divisor and the future dividend (shift anticipated) is accomplished by the use of the Ud and Ur FF's.
5. During $\phi 3$ and $\phi 4$ while the divide operation is taking place Ud and Ur are checking the divisor against the answer being generated to determine whether during the next word time there can be a subtraction and shift left or merely a shift left. "The checking is done during the present word time (dividend compared to right shifted divisor in anticipation of shift) to determine the operation during the next word time".
1. (a) Z turns true at the fall of Po.
 - (b) Z turns true when "A" is larger than "D"
 - (c) Z turns prime when "D" is larger than "A".

NOTE: When "A" and "D" are the same the "Z" FF is not effected.

2. Recirculates "A" line during $\phi 2$.
3. Recirculates "B" line during $\phi 2$.
4. (a & b) Recirculates the "D" line during $\phi 2$.
5. (a thru g) Comparing the magnitude of the P1 thru P31 bits of the dividend and divisor (shift anticipated).
6. (a thru g) Comparing the magnitude of the P32 bit of the dividend and divisor (shift anticipated) and considering Ud's state at this time.

Ur = Subtract and shift left.

Ur' = Shift left only.

- NOTE: Ur will contain the "one" or "zero" that is placed in the quotient at Po time.
7. (a) Ub is set according to Bd at P32 time. "Used later to shift the P32 bit of "B" to "A".
 8. (a thru c) If "Z" is true during P33 time, indicating the dividend is larger than the divisor, the divide is not performed, as explained in #2, and the computer sequences to ϕ_0 .
 9. (a thru c) If "Z" is prime during P33 time, indicating the dividend is smaller than the divisor, the computer sequences from ϕ_2 to ϕ_3 to begin the actual divide operation.
 10. (c thru d) "Half-adder" used to generate a difference when a subtraction takes place. Also shifts the "A" line left during the subtraction.
 - (e) Used to shift the "A" line left when no subtraction takes place.
 - (f) Shifts the P32 bit of "B" to the P1 position in the "A" line. "Shift left only".
 - (g & h) Subtract logic for the P1 bits of "A" and "D" line. "Subtract and shift left".
 11. (a thru d) "Half-adder" used to generate the borrow during the subtract and shift left operation.
 12. (a) Recirculates the sign of the "B" line.
 - (b) Ur inserts a "one" or "zero" into the LSB position of the "B" line every P1 time". Quotient.
 - (c) Shifts the "B" line left.
 13. Recirculates the "D" line.
 14. (a thru c) Used for same purpose as equations #5 only these operate during ϕ_3 and ϕ_4 .
 15. (a thru c) Used for same purpose as equations #6 only these operate during ϕ_3 and ϕ_4 .

16. (a thru c) Sequences the computer from ϕ_3 to ϕ_4 during the division operation. "Occurs after the first 16 word times in ϕ_3 .
17. (a thru c) Sequences the computer from ϕ_4 to ϕ_5 during the division operation. "Occurs after the first 16 word times in ϕ_4 .
18. Sets the sign of the "A" line to the sign of the "B" line.
19. (a & b) Sets the sign of the "B" line.
20. Recirculates the "D" line.
21. (a thru c) Sequences the computer from ϕ_5 to ϕ_0 . "In ϕ_5 for one pulse time.

EB Divide Double Length

Equations and explanations are identical to the E9 order except for the following substitution:

- 4. (a) $\underline{Dd} = (T8 T7 T5' \emptyset 2) Vw' Dn$ 6P6
- (b) + (") T6T2 Vw Wn 6P3

DESCRIPTION:

- 4. (a)
-) Recirculates the "D" line and copies the divisor from the "W" to "D".
- (b)

ED Divide By D

Equations and explanations are identical to the E9 order except for the following substitution:

- 2. - - - - -

DESCRIPTION:

- 2. No equation to recirculate "A" in " $\emptyset 2$ ", therefore, it is cleared.

EF Divide

Equations and explanations are identical to the E9 order except for the following substitution.

- 2. - - - - -

- 4. (a) $\underline{Dd} = (T8T7T5' \emptyset 2) Vw' Dn$ 6P6
- (b) + (") T6T2Vw Wn 6P3

DESCRIPTION:

- 2. No equation to recirculate "A" in " $\emptyset 2$ ", therefore, it is cleared.
- 4. (a)
-) Recirculates the "D" line and copies the divisor form "W" to "D"
- (b)

INPUT OUTPUT COMMANDS

In conjunction with the Input-Output command displayed by the "T" register, the configuration of the "R" register must be considered.

1. With R8 R7 setting in the "R" register:
 - (a) Information comes from the Flex... (R8).
 - (b) Decimal conversion takes place (R7).
2. With R8 R7' setting in the "R" register:
 - (a) Information comes from the Flex. (R8).
 - (b) Straight hexadecimal input (R7').
3. With R8' R7 setting in the "R" register:
 - (a) Information comes from the High Speed Paper Tape Reader if attached and on; otherwise the Flex (R8').
 - (b) Decimal conversion takes place (R7).
4. With R8' R7' setting in the "R" register:
 - (a) Information comes from the High Speed Paper Tape Reader if attached and on; otherwise the Flex. (R8').
 - (b) Straight hexadecimal input (R7').

F1 Hexadecimal Input (From Flex)

- 6Q2
- 2U14
- 2U14
- 9DD2
- 4N16
- 2U12
- 2U12
- 2W16
- 2W16
- 3Q11
- 2W16
- 3Q11
- 2W16
5. $\text{Payd} = T8' + T7' + T6' + T5' + T4 + T3 + (\phi3' \phi4') + Cr + Fr + Go + (R8' Sr)$
- 0EE20
- 4N9
- 8Q10
- 2U8
- 2U8
- 2W12
- 2W10
- 3W16
- 4W10
- 5W12
- 5W2
- 10 8. (a) $R1 = (T8 T7 T5 T4' \phi5 Q3 P32' C) R1'$ 3DD2
- (b) $R1' = (\quad " \quad) R1$ 4DD16
- (c) $R2 = (\quad " \quad) R2' R1'$ 4DD6
- (d) $R2' = (\quad " \quad) R2 R1'$ 4DD4
- (e) $R3 = (\quad " \quad) R3' R2' R1'$ 5DD10
- (f) $R3' = (\quad " \quad) R3 R2' R1'$ 5DD8
- 9 10. (a) $Q3 = (T8 T7 T6 T5 T3') \phi5 Fr' P33 (Y1' + Y2' + Y3 + Y4' + Y5 + Y6')$ 8Q6
- (b) $\phi5' = Q3 \phi5 C$ 2U6
- (c) $\phi6 = Q3 \phi5 C$ 2U6

11. (a) $\underline{Ad} = (T8 T7 T5) \phi 6' An$ 9K12
 (b) $+ (\quad " \quad) \phi 6 Po T4' An$ 9E16
 (c) $+ (T8 T7 T6 T5 T4') (\phi 6 Po' P33') Y1$ 9K9
12. (a) $\underline{Y1} = (T8 T7 T5 Po' P33') (T2' + T2 P1') (R7' \phi 6 C) Y2$ 1W8
 (b) $\underline{Y1}' = (\quad " \quad) (\quad " \quad) (\quad " \quad) Y2'$ 1W6
 (c) $\underline{Y2} = (\quad " \quad) (\quad " \quad) (\quad " \quad) Y3$ 2W8
 (d) $\underline{Y2}' = (\quad " \quad) (\quad " \quad) (\quad " \quad) Y3'$ 2W6
 (e) $\underline{Y3} = (\quad " \quad) (\quad " \quad) (\quad " \quad) Y4$ 3W14
 (f) $\underline{Y3}' = (\quad " \quad) (\quad " \quad) (\quad " \quad) Y4'$ 3W12
 (g) $\underline{Y4} = (T8 T7 T5 Po' P33' \phi 6 C) T2' R7' (T2' + T2 P1') An$ 3W6
 (h) $\underline{Y4}' = (\quad " \quad) T2' R7' (\quad " \quad) An'$ 4W8
13. (a) $\underline{Q3} = (T8 T7 T6 T5 T3') \phi 6 P32$ 5N8
 (b) $\underline{\phi 6}' = Q3 \phi 6 C$ 2U4
 (c) $\underline{\phi 7} = (\quad " \quad)$ 2U4
14. (a) $\underline{Q3} = T8 T7 T6 T5 T4' \phi 7 (R1 + R2 + R3) F2F1'$ 0Q11
 (b) $\underline{\phi 7}' = \phi 7 Q3 C$ 2U9
 (c) $\underline{\phi 3} = \phi 7 Q3 C$ 2U9
15. (a) $\underline{Q4} = T8 T7 T5 Q3' F2F1'$ 9I16
 (b) $\underline{\phi 7}' = Q4 C$ 1U16
 (c) $\underline{\phi 0} = Q4 C$ 1U16

DESCRIPTION:

1. (a thru c) Sequences the computer from $\phi 2$ to $\phi 3$. "In $\phi 2$ for one pulse time".
2. Q8 Turns prime $\phi 3$.
3. (a thru c) Sequences the computer from $\phi 3$ to $\phi 4$. "Q3 waits for Fr' (Flex Idle) and P33 time before sequencing to $\phi 4$ ".
4. (a thru f) "Y" FF are set to their relaxed configurations.
5. NOTE: Payd is a selection driver that operates a relay to turn on the Flexowriter "Ready" light. Since the selection driver inverts the signal it is required that the information to Payd be a "not" term. This says, "In $\phi 3$ or $\phi 4$, if the flex is not busy and not performing a carriage return, and Go One Shot is not being fired, then turn on the "Ready" light".
At this point the computer waits in $\phi 4$ for an input. When a Flex Key is struck or the reader y contacts are energized, Fr turns true
6. Q8 flip flop is turned true when any y contact is energized.
7. (a thru c) Q3 has been waiting for Q8, and now comes up at P33 time. Computer sequences out of $\phi 4$ into $\phi 5$ at the fall of P33.
8. (a thru f) The Y flip flops are set in parallel fashion from the y contacts on the Flexowriter at Po time.
9. (a thru f) The R register counts down one at Po time.
10. (a thru c) Computer waits until Flex has become idle (Fr'), and at the next P33 bit sequences into $\phi 6$.
11. (a) Ad follows An in all ϕ 's except $\phi 6$.
(b) In $\phi 6$ Ad follows An during Po time. "Recirculates the sign".
(c) Ad follows Y1 from P1 to P32 times. "The magnitude portion of the word".
12. (a thru h) From P1 through P32, Y1 follows Y2, Y2 follows Y3, Y3 follows Y4, Y4 follows An. The four Y flip flops are now inserted in the A line, lengthening the line by four bits. The new information in the "Y" flip flops is inserted in the four least significant bits of the A line. At P32 time the four most significant bits of A are now in the "Y" flip flops.
13. (a thru c) At P32 time Q3 comes up and the computer sequences to $\phi 7$ at the fall of P32. The new information is in the least significant four bits of A, and the four most significant bits of A have been left in the Y flip flops. A line is now recirculating.

14. (a thru c) If the R register has not been completely down, Q3 comes up at P3 time (F2F1') and the computer sequences back to ϕ_3 for next input at the fall of P3.

15. (a thru c) If the R register has been completely counted down, Q3 cannot come up, and Q4 comes up at P3 time, and computer sequences back to ϕ_0 .

F1 Hexadecimal Input (From High Speed Paper Tape Reader)

Equations and explanations are identical to the F1 (from Flex) except for the following substitution.

$$7. (a) Q3 = (T8 T7 T6 T5 T3') \phi 4 C (y1 + y2 + y3 + y4 + y5 + y6) P33 \bar{X}3 \quad 4N6$$

DESCRIPTION:

7. (a) Q3 turns on during P33 time in $\phi 4$ if $\bar{X}3$ is true indicating HSPT is connected and on.

NOTE: In the Flex logic the Q3 equation (7a) would not apply because Q8 could not be turned on due to no Fr term from Flex in equation 6.

F3 Alpha - Numerical Input

Equations and explanations are identical to F1 order (Flex or HSPTR) except for the following substitutions and additions.

$$\begin{aligned} 12. (g) \underline{Y4} &= (T8 T7 T5 Po' P33' \phi 6 C) (T2' + T2 P1') (T2 R7') Y5 && 3W3 \\ (h) \underline{Y4}' &= (\quad " \quad) (\quad " \quad) (\quad " \quad) Y5' && 4W5 \\ (i) \underline{Y5} &= (T8 T7 T5 T3' Po' P33' \phi 6 C) (T2' + T2 P1') R7' W6 && 5W4 \\ (j) \underline{Y5}' &= (\quad " \quad) (\quad " \quad) R7' Y6' && 5W6 \\ (k) \underline{Y6} &= (T8 T7 T5 Po' P33' \phi 6 C) (T2' + T2 P1') T2 An && 6W16 \\ (l) \underline{Y6}' &= (\quad " \quad) (\quad " \quad) T2 An' && 6W14 \end{aligned}$$

DESCRIPTION:

12. (g & h) Y4 now follows Y5 (not An as in the F1 order).
 (i & j) Y5 follows Y6.
 (k & l) Y6 follows An.

NOTE: This inserts six "Y" FFs in the "A" line instead of 4 as in the F1 order.

Ad follows Y1 at P1 time because of equation 11(c) in the F1 order. This is of no significance since the P1 bit is not used with alpha-numerical information. The status of Y1 flip flop is not affected because of this, and Ad starts following Y1 at P2 time (because of T2P1' in the Y equations). Similarly, information goes into Ad at P32 time from Y1 flip flop, but the P32 bit has no significance in alpha-numerical information since only bits P2 through P31 inclusive (total 30 bits) are used.

F5 Hexadecimal Output (to Flex)

- | | | | |
|-------|-----|---|-------|
| 1. | (a) | $Q3 = T8 T7 T5 \phi 2$ | 6Q2 |
| | (b) | $\phi 2' = Q3 \phi 2 C$ | 2U14 |
| | (c) | $\phi 3 = Q3 \phi 2 C$ | 2U14 |
| 2. | (a) | $Q3 = (T8 T7 T5 T3) \phi 3$ | 5N3 |
| | (b) | $\phi 3' = Q3 \phi 3 C$ | 2U12 |
| | (c) | $\phi 4 = Q3 \phi 3 C$ | 2U12 |
| 3. | (a) | $Y1' = (\phi 4 C)$ | 2W16 |
| | (b) | $Y2' = (")$ | 2W16 |
| | (c) | $Y3' = (") T3$ | 3Q5 |
| | (d) | $Y4' = (")$ | 2W16 |
| | (e) | $Y5' = (") T3$ | 3Q5 |
| | (f) | $Y6' = (")$ | 2W16 |
| 4. | | $Cr' = (T3) Go' (cr' C) T7$ | 8DD10 |
| 5. | | $Ue = G1' G2' G3' G4' G5' G6' Vo P32 T8 \phi 4 C$ | 5I1 |
| 6. | | $Fw'(DR) = fw' R8 Ue Hof Cr' (Vo P33)$ | |
| 7. | | $Fw'(PF) = Fw' C Po$ | OK16 |
| 8. | (a) | $Q3 = (T8 T7 T5 T3) \phi 4 Fw'$ | 0Q7 |
| | (b) | $\phi 4' = Q3 \phi 4 C$ | 2U8 |
| | (c) | $\phi 5 = Q3 \phi 4 C$ | 2U8 |
| 10 8. | (a) | $R1 = (T8 T7 T5 T4' \phi 5 Q3 P32' C) R1'$ | 3DD2 |
| | (b) | $R1' = (") R1$ | 4DD16 |
| | (c) | $R2 = (") R2' R1'$ | 4DD6 |
| | (d) | $R2' = (") R2 R1'$ | 4DD4 |
| | (e) | $R3 = (") R3' R2' R1'$ | 5DD10 |
| | (f) | $R3' = (") R3 R2' R1'$ | 5DD8 |
| 9 10. | (a) | $Q3 = T8 T7 T5 T3 \phi 5 Po$ | 501 |
| | (b) | $\phi 5' = Q3 \phi 5 C$ | 2U6 |
| | (c) | $\phi 6 = Q3 \phi 5 C$ | 2U6 |
| 11. | (a) | $Ad = (T8 T7 T5) \phi 6' An$ | 9K12 |
| | (b) | $+ (") \phi 6 Po' P33' Y1$ | 9E16 |
| | | | 9K9 |
| 12. | (a) | $Y1 = (T8 T7 T5 Po' P33' \phi 6 C) R7' Y2 (T2' + T2 P1')$ | 1W8 |
| | (b) | $Y1' = (") R7' Y2' (")$ | 1W6 |
| | (c) | $Y2 = (") R7' Y3 (")$ | 2W8 |
| | (d) | $Y2' = (") R7' Y3' (")$ | 2W6 |
| | (e) | $Y3 = (") R7' Y4 (")$ | 3W14 |
| | (f) | $Y3' = (") R7' Y4' (")$ | 3W12 |

- (g) $\underline{Y4}$ = (T8 T7 T5 Po' P33' ϕ 6 C) R7' An T2' (T2' + T2 P1') 3W6
- (h) $\underline{Y4'}$ = (") R7' An' T2' (") 4W8
13. (a) $\underline{Q3}$ = (T8 T7 T5 T4' T3) ϕ 6 P32 T6 T2' 9Q1
- (b) $\underline{\phi6'}$ = ϕ 6 Q3 C 2U4
- (c) $\underline{\phi7}$ = ϕ 6 Q3 C (new) 2U4
14. (a) $\underline{G1}$ = (T8 T7 T5 T3 ϕ 7 C F2 F1') Y1 $\gamma1'$ 2A3
- (b) $\underline{G2}$ = (") Y2 $\gamma2'$ 3A8
- (c) $\underline{G3}$ = (") Y3' $\gamma3'$ 3A4
- (d) $\underline{G4}$ = (") Y4 $\gamma4'$ 3A2
- (e) $\underline{G5}$ = (") Y5' $\gamma5'$ 4A16
- (f) $\underline{G6}$ = (") Y6 $\gamma6'$ 4A11
15. (a) $\underline{Q3}$ = (T8 T7 T5 T4') ϕ 7 (R1 + R2 + R3) F2F1' T6 0Q11
- (b) $\underline{\phi7'}$ = ϕ 7 Q3 C 2U9
- (c) $\underline{\phi3}$ = ϕ 7 Q3 C 2U9
16. (a) $\underline{Q4}$ = (T8 T7 T6) ϕ 7 F2F1' Q3' 9I16
- (b) $\underline{\phi7'}$ = Q4 C 1U16
- (c) $\underline{\phi0}$ = Q4 C 1U16

DESCRIPTION:

1. (a thru c) Sequences the computer from $\phi 2$ to $\phi 3$. "In $\phi 2$ for one pulse time".
2. (a thru c) Sequences the computer from $\phi 3$ to $\phi 4$. "In $\phi 3$ for one pulse time".
3. (a thru f) "Y" FF's are set prime.
4. Cr' indicates the flex is not in a carriage return cycle. "Go prime is an interlock signal to tell the computer the flex is ready to receive information and is not in a carriage return cycle".
5. Ue turns true when the "one-shots" have all been fired, indicated by Gi'. This happens at the fall of P32 of word "00" on the "F" line. "This term is used in a gate to sequence the computer".
6. Fw' DR turns true during P33 of word "00" on the "F" line if Ue is true, one-shots fired; Cr' carriage not in return cycle and Hof FLEX switch in COMPUTE position.
7. The Fw' FF is following the Fw' DR.
8. (a thru c) Q3 turns true to sequence the computer from $\phi 4$ to $\phi 5$.
9. (a thru c) "R" register counts down by "one" at the fall of Po during $\phi 5$.
"Counting number of characters outputed.
10. (a thru c) Q3 turns true during Po of $\phi 5$ to sequence the computer from $\phi 5$ to $\phi 6$.
11. (a) Recirculates the "A" line normally in all ϕ 's except $\phi 6$.
"
(b) Ad follows "Y1" from P1 thru P32 time during $\phi 6$. "Y" FF's are being loaded with the information from the "A" line.
12. (a thru h) Y1 follows Y2, Y2 follows Y3, Y3 follows Y4, and Y4 follows An from P1 thru P32 time during $\phi 6$.
13. (a thru c) Q3 turns true during P32 time in $\phi 6$ to sequence the computer from $\phi 6$ to $\phi 7$.
14. (a thru f) During $\phi 7$ the "one-shots" are fired according to the configuration of the "Y" FF's. "Pushing keys or punching tape in flex". This operation takes place in a parallel manner at P3 time.
15. (a thru c) Q3 turns true during P3 time in $\phi 7$ if the "R" register has not been counted down and the computer sequences from $\phi 7$ to $\phi 3$ to repeat the operation.
16. (a thru c) Q4 turns true during P3 time in $\phi 7$ if the "R" register is counted down and the computer sequences to $\phi 0$.

F5 Hexadecimal Output (to HSPT Punch)

Equations and explanations are identical to the F3 order (to Flex) except for the following substitutions.

- | | | |
|---------|---|------|
| 7. | $\underline{Fw'} (DR) = \overline{sw} R8' \overline{HSP}$ | OK14 |
| 15. (a) | $\underline{Q3} = (T8 T7 T6 T5 T4') \phi7 (R1 + R2 + R3) R8' F1 \overline{HSP}$ | 9Q3 |
| 16. (a) | $\underline{Q4} = (T8 T7 T5) \phi7 Q3' R8' F1 \overline{HSP}$ | 9I5 |

DESCRIPTION:

7. Fw' flip flop can come up without logic pertaining to Flexowriter status in order to allow Q3 to come up in $\phi4$. \overline{sw} is term from punch coming from sw cam switches on motor shaft.
15. (a) In $\phi7$ Q3 comes up during Po time if the "R" register is not counted down. This is to prevent the G1 through G6 shots from firing.
16. (a) If the R register has been counted down ($R1' R2' R3'$) Q3 cannot come up. Q4 comes up and sequences the computer back to $\phi0$ for look-up of next command.

F7 Alpha-Numerical Output

Equations and explanations are identical to the F5 order (Flex or HSPTP) except for the following substitutions and additions.

- | | | | | | |
|-----|-----|-------------------|---|---|------|
| 12. | (g) | $\underline{Y4}$ | = | (T8 T7 T5 Po' P33' ϕ 6 C)(T2' + T2 P1')(R7' T2) Y5 | 3W3 |
| | (h) | $\underline{Y4}'$ | = | (" ")(" ")(") Y5' | 4W5 |
| | (i) | $\underline{Y5}$ | = | (" ")(" ") R7' Y6 | 5W4 |
| | (j) | $\underline{Y5}'$ | = | (" ")(" ") R7' Y6' | 5W6 |
| | (k) | $\underline{Y6}$ | = | (" ")(" ")(R7' T2) An | 6W16 |
| | (l) | $\underline{Y6}'$ | = | (" ")(" ")(") An' | 6W14 |
| 13. | (a) | $\underline{Q3}$ | = | (T8 T7 T5 T4' T3 T2 ϕ 6)(F5 F2 F1') | 7T4 |
| 14. | (g) | \underline{Go} | = | (T8 T7 T5 T3) ϕ 7 C (Y6 Y5' Y4 Y3) | 3YY9 |

DESCRIPTION:

12. (g & h) Y4 now follows Y5 (not An as in the F5 order).
 (i & j) Y5 follows Y6..
 (k & l) Y6 follows An during P2 thru P31 time.

NOTE: This inserts six "Y" FFs in the "A" line instead of 4 as in the F5 order.

The "Po" bit is recirculated (equation 11b F5 order) and since there is no recirculation term for Ad at P1 time, P1 either remains "zero" or changes to zero. Neither the P1, P32 or P33 bits have any significance in alpha-numerical characters.

13. (a) At the fall of P31 in ϕ 6 the 6LS bits (P2 thru P7) of the "A" line are in the "Y" FFs, Q3 comes up to sequence the computer into ϕ 7.
14. (g) If the alpha-numerical information calls for a carriage return, Go is triggered at P32 time in ϕ 7. The computer sequences out of ϕ 7 before the G1 thru G6 "one shots" can be fired.

"CODE DELETE"

The following substitutions and additions apply during a code delete in a "F1" or "F3" order.

10.	(a)	$\underline{Q3}$	=	(T8 T7 T6 T5 T3')	$\phi 5$	Fr'	P32	(Y1 Y2 Y3' Y4 Y5' Y6)	8Q2
9	(b)	$\underline{\phi 5'}$	=	$\phi 5$	Q3	C			2U6
	(c)	$\underline{\phi 6}$	=	$\phi 5$	Q3	C			2U6
	(d)	$\underline{Q3}$	=	(T8 T7 T6 T5 T3')	$\phi 6$	P33			5N7
	(e)	$\underline{\phi 6'}$	=	$\phi 6$	Q3	C			2U4
	(f)	$\underline{\phi 7}$	=	$\phi 6$	Q3	C			2U4
	(g)	$\underline{Q3}$	=	(T8 T7 T6 T5 T4')	$\phi 7$	(Y1 Y2 Y3' Y4 Y5' Y6)			6I9
	(h)	$\underline{\phi 7'}$	=	$\phi 7$	Q3	C			2U10
	(i)	$\underline{\phi 3}$	=	$\phi 7$	Q3	C			2U10

DESCRIPTION:

During the execution of an input "Read" command either a F1 or F3 the computer will recognize and act accordingly on a "CODE DELETE".

10. (a thru c) Q3 turns true during P32 time, instead of P33 time, to sequence the computer from $\phi 5$ to $\phi 6$.
- (d thru f) Q3 turns true during P33 time to sequence the computer from $\phi 6$ to $\phi 7$.
- (g thru i) Q3 turns true during Po time to sequence the computer from $\phi 7$ to $\phi 3$.

NOTE: Due to the sequencing of the computer from $\phi 5$ to $\phi 3$ in a 3 pulse times the computer ignores the information in the "Y" flip flops and recycles to input the next character.

F9 Sign In

Equations and explanations are identical to the F1 order (From Flex or HSPTR) except for the following substitution.

- | | | |
|---------|---|-----|
| 11. (b) | <u>Ad</u> = (T8 T7 T6 T4) ϕ 6 Po Y4' | 2K6 |
| (c) | ----- | -- |

DESCRIPTION:

11. (b) Ad follows Y4' at Po time in ϕ 6.

NOTE: If Y4 were prime (which it would be if a space had been typed in), a one bit would be put into the "A" line at Po time, indicating a plus sign.

OR, if Y4 were true (which it would be if a "minus" had been typed in), no bit would be put into the "A" line at Po time indicating a minus sign.

- (c) Since there is no recirculation equation during the remainder of the one word time in ϕ 6, the "A" line is cleared.

MNEMONIC CODE

Alpha Code	Hex Code	Operation	Alpha Code	Hex Code	Operation
ACS	63	Add and Change Sign	MDA	E1	Multiply by D and Add
ADB	BD	Add to B	MPA	E3	Multiply and Add
ADD	61	Add	MPD	E5	Multiply by D
ALI	F3	Alphabetic Input	MPY	E7	Multiply
ALO	F7	Alphabetic Output	MTC	93	Magnetic Tape Copy
ALS	A7	A Left Shift	MTS	91	Magnetic Tape Status
ARS	A5	A Right Shift	MTX	95	Magnetic Tape Exchange
BTP	9F	Both Type and Punch	NOP	00	No Operation
CFA	89	Copy from Wk. St. I.	NMO	DD	Number Output
CFB	8B	Copy from Wk. St. II	NTP	99	Neither Type nor Punch
CFC	8D	Copy from Wk. St. III	PAA	6D	Place Address in A
CFD	8F	Copy from Wk. St. IV	PCD	97	Punch Cards
CLA	28	Clear A	PHA	6F	Place Half-word in A
CHS	2E	Change Sign	PNH	9D	Punch
COV	02	Change Overflow Ind.	RND	22	Round
COM	51	Compare Magnitude	SAA	4D	Store Address from A
CPL	3E	Complement	SAW	49	Store A
CTA	81	Copy to Wk. St. I.	SBB	BF	Subtract from B
CTB	83	Copy to Wk. St. II	SBW	C5	Store B
CTC	85	Copy to Wk. St. III	SCS	65	Subtract and Change Sign
CTD	87	Copy to Wk. St. IV	SCT	AB	Shift and Count
DDD	E9	Divide Double L by D	SDW	C7	Store D
DDW	EB	Divide Double Length	SEW	C3	Store E
DVD	ED	Divide by D	SHA	4F	Store Half-word from A
DVW	EF	Divide	SNI	F9	Sign Input
EXT	75	Extract	SNO	D5	Sign Output
EXD	71	Extract with D Mask	SSP	2C	Set Sign Plus
HTR	1B	Halt and Transfer	SUB	67	Subtract
HXI	F1	Hexadecimal Input	TLX	17	Transfer on Index
HXO	F5	Hexadecimal Output	TLZ	1D	Transfer on Less than Zero
LAB	32	Load A from B	TNZ	19	Transfer on Non-zero
LAD	38	Load A from D	TOV	1F	Transfer on Overflow
LAE	34	Load A from E	TRA	11	Transfer
LAM	B5	Load A from M	TSA	13	Transfer on Switch One
LAW	79	Load A	TSB	15	Transfer on Switch Two
LBW	41	Load B	TYP	9B	Type
LDW	5B	Load D	XAB	30	Exchange A and B
LEW	57	Load E	XAD	3A	Exchange A and D
LLS	A3	Long Left Shift	XAE	36	Exchange A and E
LRS	A1	Long Right Shift	XAW	69	Exchange A and W

MNEMONIC CODE

Hex Code	Alpha Code	Operation	Hex Code	Alpha Code	Operation
00	NOP	No Operation	91	MTS	Magnetic Tape Status
02	COV	Change Overflow Ind.	93	MTC	Magnetic Tape Copy
11	TRA	Transfer	95	MTX	Magnetic Tape Exchange
13	TSA	Transfer on Switch One	97	PCD	Punch Cards
15	TSB	Transfer on Switch Two	99	NTP	Neither Type nor Punch
17	TLX	Transfer on Index	9B	TYP	Type
19	TNZ	Transfer on Non-zero	9D	PNH	Punch
1B	HTR	Halt and Transfer	9F	BTP	Both Type and Punch
1D	TLZ	Transfer on Less than Zero			
1F	TOV	Transfer on Overflow	A1	IRS	Long Right Shift
			A3	LLS	Long Left Shift
22	RND	Round	A5	ARS	A Right Shift
28	CLA	Clear A	A7	ALS	A Left Shift
2C	SSP	Set Sign Plus	AB	SCT	Shift and Count
2E	CHS	Change Sign			
			B5	LAM	Load A from M
30	XAB	Exchange A and B	BD	ADB	Add to B
32	LAB	Load A from B	BF	SBB	Subtract from B
34	LAE	Load A from E			
36	XAW	Exchange A and E	C3	SEW	Store E
38	LAD	Load A from D	C5	SEW	Store B
3A	XAD	Exchange A and D	C7	SDW	Store D
3E	CPL	Complement (A)			
			D5	SNO	Sign Output
41	LBW	Load B	DD	NMO	Number Output
49	SAW	Store A			
4D	SAA	Store Address from A	E1	MDA	Multiply by D and Add
4F	SHA	Store Half-word from A	E3	MPA	Multiply and Add
			E5	MPD	Multiply by D
51	COM	Compare Magnitude	E7	MPY	Multiply
57	LEW	Load E	E9	DDD	Divide Double Length by D
5B	LDW	Load D	EB	DDW	Divide Double Length
			ED	DVD	Divide by D
61	ADD	Add	EF	DVW	Divide
63	ACS	Add and Change Sign			
65	SCS	Subtract and Change Sign	F1	HXI	Hexidecimal Input
67	SUB	Subtract	F3	ALI	Alphabetic Input
69	XAW	Exchange A and W	F5	HXO	Hexidecimal Output
6D	PAA	Place Address in A	F7	ALO	Alphabetic Output
6F	PHA	Place Half-word in A	F9	SNI	Sign Input
71	EXD	Extract with D mask			
75	EXT	Extract			
79	LAW	Load A			
81	CTA	Copy to Wk. St. I			
83	CTB	Copy to Wk. St. II			
85	CTC	Copy to Wk. St. III			
87	CTD	Copy to Wk. St. IV			
89	CFA	Copy from Wk. St. I			
8B	CFB	Copy from Wk. St. II			
8D	CFC	Copy from Wk. St. III			
8F	CFD	Copy from Wk. St. IV.			

STANDARD ALWAC III-E CODES

(1959 Compatible - Engineer's Copy)

.Hole No. 5 = Code Delete

<u>Tape</u>	<u>Flex</u>	<u>ALWAC</u>	<u>407</u>	<u>Cards</u>	<u>Tape</u>	<u>Flex</u>	<u>ALWAC</u>	<u>407</u>	<u>Cards</u>
7612.34	Space	00 00 00	Space		7612.3	* -	10 00 00	-	X
612.34	0 1	00 00 01	1	1	612.3	j J	10 00 01	J	X 1
7 12.34	" 2	00 00 10	2	2	7 12.3	k K	10 00 10	K	X 2
12.34	Δ 3	00 00 11	3	3	12.3	l L	10 00 11	L	X 3
76 2.34	Σ 4	00 01 00	4	4	76 2.3	m M	10 01 00	M	X 4
6 2.34	& 5	00 01 01	5	5	6 2.3	n N	10 01 01	N	X 5
7 2.34	+ 6	00 01 10	6	6	7 2.3	o O	10 01 10	O	X 6
2.34	? 7	00 01 11	7	7	2.3	p P	10 01 11	P	X 7
761 .34	= 8	00 10 00	8	8	761 .3	q Q	10 10 00	Q	X 8
61 .34	(9	00 10 01	9	9	61 .3	r R	10 10 01	R	X 9
7 1 .34	Stop Code	00 10 10	(9)	82	7 1 .3		10 10 10	(R)	X82
1 .34	(\$)	00 10 11	#	83	1 .3	# \$	10 10 11	\$	X83
76 .34	(%)	00 11 00	⊙	84	76 .3	(%)	10 11 00	*	X84
6 .34	Back Space	00 11 01	(⊙)	85	6 .3	Car. Ret.	10 11 01	(*)	X85
7 .34		00 11 10	(#)	86	7 .3		10 11 10	(\$)	X86
.34		00 11 11	(⊙)	87	.3	Upper Case	10 11 11	(*)	X87
7612. 4	(A)	01 00 00	&	Y	7612.) 0	11 00 00	0	0
612. 4	a A	01 00 01	A	Y 1	612.	: /	11 00 01	/	0 1
7 12. 4	b B	01 00 10	B	Y 2	7 12.	s S	11 00 10	S	0 2
12. 4	c C	01 00 11	C	Y 3	12.	t T	11 00 11	T	0 3
76 2. 4	d D	01 01 00	D	Y 4	76 2.	u U	11 01 00	U	0 4
6 2. 4	e E	01 01 01	E	Y 5	6 2.	v V	11 01 01	V	0 5
7 2. 4	f F	01 01 10	F	Y 6	7 2.	w W	11 01 10	W	0 6
2. 4	g G	01 01 11	G	Y 7	2.	x X	11 01 11	X	0 7
761 . 4	h H	01 10 00	H	Y 8	761 .	y Y	11 10 00	Y	0 8
61 . 4	i I	01 10 01	I	Y 9	61 .	z Z	11 10 01	Z	0 9
7 1 . 4		01 10 10	(I)	Y82	7 1 .		11 10 10	(Z)	082
1 . 4		01 10 11	.	Y83	1 .	,	11 10 11	,	083
76 . 4	(%)	01 11 00	⊙	Y84	76 .	⊙ %	11 11 00	%	084
6 . 4	Tab	01 11 01	(⊙)	Y85	6 .	Clear	11 11 01	(%)	085
7 . 4		01 11 10	(.)	Y86	7 .	Color Shift	11 11 10	(,)	086
. 4	Lower Case	01 11 11	(⊙)	Y87	.	Tape Feed	11 11 11	(%)	087

ALWAC III-E CODE CONVERSION

1956 code

FLEXOWRITER			ALWAC
PUNCH	PRINT	HEX	
3 5	Space	0	00 0000
1 .3 5	0 1	1	00 0001
2.3 5	" 2	2	00 0010
12.3 5	+ 3	3	00 0011
. 5	= 4	4	00 0100
1 . 5	% 5	5	00 0101
2. 5	? 6	6	00 0110
12. 5	! 7	7	00 0111
.345	Σ 8	8	00 1000
1 .345	(9	9	00 1001
2.345	A a	A	00 1010
12.345	B b	B	00 1011
. 45	C c	C	00 1100
1 . 45	D d	D	00 1101
2. 45	E e	E	00 1110
12. 45	F f	F	00 1111
.3	G g		01 0000
1 .3	H h		01 0001
2.3	I i		01 0010
	Tape Feed		01 0100
2. 4			01 1110
12. 4	J j		01 1111
6 .3 5	K k		10 0000
61 .3 5	L l		10 0001
6 2.3 5	M m		10 0010
612.3 5	N n		10 0011
6 . 5	O o		10 0100
61 . 5	P p		10 0101
6 2. 5	Q q		10 0110
612. 5	R r		10 0111
6 .345	Lower Case		10 1000
61 .345	Upper Case		10 1001
6 2.345	Color shift		10 1010
612.345	Code delete		10 1011
6 . 45	Tabulate		10 1100

08 Load B from E

- 1. \underline{Bd} = $\emptyset 2$ T8' T7' T6' T5' T4 T3' T2' F4 En 7I15
- 2. (a) $\underline{Q4}$ = (T8' T7' T5') ($\emptyset 2$ P33) T1' OP9
- (b) $\underline{\emptyset 2'}$ = Q4 C 1U16
- (c) $\underline{\emptyset o}$ = Q4 C 1U16

DESCRIPTION

- 1. Bd follows En during the MSH word time (F4). "Copies MSH of E to MSH of B. (The LSH of B including the sign is cleared.)"
- 2. (a) Q4 driver turns on during P33 time in $\emptyset 2$ if T1 is prime. "T1' used in packed commands."
- (b) Sequences the computer from $\emptyset 2$ to $\emptyset o$.
- (c)

0A Load D from E

- 1. \underline{Dd} = $\emptyset 2$ T8' T7' T6' T5' T4 T3' T2 F4 En 8P11
- 2. (a) $\underline{Q4}$ = (T8' T7' T5') ($\emptyset 2$ P33) T1' OP9
- (b) $\underline{\emptyset 2'}$ = Q4 C 1U16
- (c) $\underline{\emptyset o}$ = Q4 C 1U16

DESCRIPTION

- 1. Dd follows En during the MSH word time (F4). "Copies MSH of E to MSH of D. (The LSH of D including the sign is cleared.)"
- 2. (a) Q4 driver turns on during P33 time in $\emptyset 2$ if T1 is prime. "T1' used in packed commands."
- (b) Sequences the computer from $\emptyset 2$ to $\emptyset o$.
- (c)

OC Sign of A to B (B recirculates)

- | | | | |
|----|-----|--|-------|
| 1. | (a) | <u>Bd</u> = (T8' T7' T6' T5' T4 T3) ϕ 2 Po An | OFF16 |
| | (b) | + (T8' T7' T6' T5' T4 T3) T2' ϕ 2 Po' Bn | 5FF10 |
| 2. | (a) | <u>Q4</u> = (T8' T7' T5') (ϕ 2 P33) T1' | OP9 |
| | (b) | <u>ϕ2'</u> = Q4 C | 1U16 |
| | (c) | <u>ϕ0</u> = Q4 C | 1U16 |

DESCRIPTION:

1. (a) Bd follows An during Po in ϕ 2. "Transfers sign of "A" to "B".
- (b) Bd follows Bn the duration of the word time in ϕ 2. "Recirculates "B"
2. (a) Q4 driver turns on during P33 in ϕ 2.
- (b & c) Sequences the computer from ϕ 2 to ϕ 0.

OE Clear B and Sign of A to B

- | | | | |
|----|-----|---|-------|
| 1. | (a) | <u>Bd</u> = (T8' T7' T6' T5' T4 T3) ϕ 2 Po An | OFF16 |
| | (b) | + - - - - - - - - - - - - - - - - - | - - - |
| 2. | (a) | <u>Q4</u> = (T8' T7' T5') (ϕ 2 P33) T1' <i>in S #11</i> | OP9 |
| | (b) | <u>ϕ2'</u> = Q4 C | 1U16 |
| | (c) | <u>ϕ0</u> = Q4 C | 1U16 |

DESCRIPTION:

1. (a) Bd follows An during Po time in ϕ 2 with this order in the "T". "Copies sign of A."
- (b) No recirculation equations for the "B" line with this order in "T", therefore, the "B" line is cleared from P1 thru P33 time.
2. (a) Q4 turns on during P33 time in ϕ 2.
3. (b & c) Sequences the computer from ϕ 2 to ϕ 0.

NOTE: Bd = (T8' T3) Bn changed to Bd = (T8' T4' T2) Bn. This prevents recirculation of the "B" line in ϕ 2 during an OE order.

55 Load Index From Address

After a " $\phi 2$ " look-up is accomplished, Page 6,
the following equations apply.

- | | | | |
|----|-----|---|-------|
| 1. | (a) | $\underline{Er} = (T8'T7 T6'T5T4'T3)(T2+F3')(\phi 2 Vw)F4 Wn C$ | 0C15 |
| | (b) | $+ \phi o' F4' (En C)$ | 7YY10 |
| | (c) | $\underline{Er}' = (T8'T7T6'T5T4'T3)(T2'F3 + Wn')(\phi 2 Vw)F4 C$ | 2B16 |
| | (d) | $+ \phi o' F4' (En' C)$ | 7YY4 |
| 2. | (a) | $\underline{Q4} = (T8' T7) (Vw P33 \phi 2) Ua'$ | 9010 |
| | (b) | $+ (T8' T7) (Vw P33 \phi 2) Us'$ | 907 |
| | (c) | $\underline{\phi 2} = Q4 C$ | 1U16 |
| | (d) | $\underline{\phi o} = Q4 C$ | 1U16 |

DESCRIPTION:

1.
 - (a) Er follows Wn during the MSH address portion ($F4 F3'$) in $\phi 2$ with this order in the "T" register. "Passes the one's"
 - (b) Er follows En during the LSH in any ϕ but ϕo . "Passes the one's during the LSH word time for normal recirculation."
 - (c) Er' follows Wn' during the MSH address portion in $\phi 2$ with this order in the "T" register. "Passes the zero's also, clears the MSH instruction portion of the "E" line."
 - (d) Er' follows En' during the LSH in any ϕ but ϕo . "Passes the zero's during the LSH word time for normal recirculation."
2.
 - (a) $Q4$ turns on during $P33$ if Ua is prime.
 - (b) Same as (a) but if Us is prime.
 - (c & d) Sequences the computer from $\phi 2$ to ϕo .

81 Copy to Working Storage I

- | | | | |
|----|-----|---|---------------------|
| 1. | (a) | $\underline{Md}' = \phi_1 C$ | 9B8 |
| | (b) | + SC | 6C8 |
| 2. | | $\underline{Q2} = (T8 T7' T6' T5') \phi_0' \phi_1'$ | 7T10 |
| 3. | (a) | $\underline{C7}' = (C7 Q2 \phi_2) (Ri Vi' + Ri' Vi) C$ | --- |
| | (b) | $\underline{C7} = C7' P33 C$ | 5N30 |
| 4. | (a) | $\underline{Vi} = (C7' Q2 \phi_2) Ri C$ | (i = 1 thru 8 FF's) |
| | (b) | $\underline{Vi}' = (\quad " \quad) Ri' C$ | --- |
| 5. | (a) | $\underline{C1} = (C7 P33 C) C1'$ | 4N16 |
| | (b) | $\underline{C1}' = (\quad " \quad) C1 (C2' + C3' + C4' + C5' + C6')$ | 4N11 |
| | (c) | + C7' C | 4N2 |
| | (d) | $\underline{C2} = (C7 P33 C) C1 C2'$ | 5N16 |
| | (e) | $\underline{C2}' = (\quad " \quad) C1 C2 (C2' + C3' + C4' + C5' + C6')$ | 5N13 |
| | (f) | + C7' C | 4N2 |
| | (g) | $\underline{C3} = (C7 P33 C) C1 C2 C3'$ | 5N11 |
| | (h) | $\underline{C3}' = (\quad " \quad) C1 C2 C3 (C2' + C3' + C4' + C5' + C6')$ | 5N9 |
| | (i) | + C7' C | 4N2 |
| | (j) | $\underline{C4} = (C7 P33 C) C1 C2 C3 C4'$ | 5N2 |
| | (k) | $\underline{C4}' = (\quad " \quad) C1 C2 C3 C4 (C2' + C3' + C4' + C5' + C6')$ | 7L14 |
| | (l) | + C7' C | 4N2 |
| | (m) | $\underline{C5} = (C7 P33 C) C1 C2 C3 C4 C5'$ | 7L12 |
| | (n) | $\underline{C5}' = (\quad " \quad) C1 C2 C3 C4 C5 C6'$ | 7L10 |
| | (o) | + C7' C | 4N2 |
| | (p) | $\underline{C6} = (C7 P33 C) C1 C2 C3 C4 C5 C6'$ | 7L8 |
| | (q) | $\underline{C6}' = \phi_2 C7' C$ | 7L7 |
| 6. | (a) | $\underline{Uc} = \phi_0' T8 T7' Po C$ | 8Y6 |
| | (b) | $\underline{Uc}' = P33 C$ | 2G3 |
| | (c) | + SC | 9AA23 |
| 7. | (a) | $\underline{Q3} = \phi_2 T7' Q2 Uc$ | OM7 |
| | (b) | $\underline{\phi_2}' = \phi_2 Q3 C$ | 2U14 |
| | (c) | $\underline{\phi_3} = \phi_2 Q3 C$ | 2U14 |
| 8. | (a) | $\underline{Q3} = \phi_3 Q2$ | OM16 |
| | (b) | $\underline{\phi_3}' = \phi_3 Q3 C$ | 2U12 |
| | (c) | $\underline{\phi_4} = \phi_3 Q3 C$ | 2U12 |

- P30
9. $\underline{Q3} = \phi 4 (C1 C2 C3 C4 C5 C6) Q2 A2' F5 F2' F1$ 9N9
10. $\underline{C7}' = T7' C7 (\phi 4 + \phi 5) Q2 Q3 C$ 8N14
11. (a) $\underline{\phi 4}' = \phi 4 Q3 C$ 2U8
 (b) $\underline{\phi 5} = \phi 4 Q3 C$ 2U8
12. $\underline{Q7} = \phi 5 T7' T4' Q2$ 6T8
13. (a) $\underline{H3} = (\phi 2' Q7) (T3' T2' C) Mr$ 5G15
 (b) $\underline{H3}' = (") (") Mr'$ 6G3
14. $\underline{Q3} = \phi 5 (C1 C2 C3 C4 C5 C6) Q2 Md' P33$ 8YY12
15. $\underline{C7}' = T7' C7 (\phi 4 + \phi 5) Q2 Q3 C$ 8N14
16. (a) $\underline{\phi 5}' = \phi 5 Q3 C$ 2U6
 (b) $\underline{\phi 6} = \phi 5 Q3 C$ 2U6
17. (a) $\underline{Q3} = \phi 6 Q2 P33$ 1N3
 (b) $\underline{\phi 6}' = \phi 6 Q3 C$ 2U4
 (c) $\underline{\phi 7} = \phi 6 Q3 C$ 2U4
18. (a) $\underline{X1} = P33 C$ 2C3
 (b) $\underline{X1}' = H2 (T3' T2' C) (P33' Mr')$ 3C15
 (c) $+ H2' (T3' T2' C) (P33' Mr)$ 4C15
19. (a) $\underline{A2} = \phi 7 T8 T6' T5' X1' C$ 5C4
 (b) $\underline{A2}' = \phi 7 Apr Q2 A2 P33 C$ 4E12
 (c) $+ Ap2 C$ 6C11
 (d) $+ SC$ 609
20. (a) $\underline{Q3} = \phi 7 Apr Q2 A2 P33$ 4E13
 (b) $\underline{\phi 7}' = \phi 7 Q3 C$ 2U9
 (c) $\underline{\phi 3} = \phi 7 Q3 C$ 2U9
21. (a) $\underline{Q4} = \phi 7 (C1 C2 C3 C4 C5 C6) Q2 A2' X1 P33$ 9I12
 (b) $\underline{\phi 7}' = Q4 C$ 1U16
 (c) $\underline{\phi 0} = Q4 C$ 1U16

DESCRIPTION:

1. (a) Md FF turns prime in ϕ_1
 (b) Md FF turns prime when the NORMAL-TEST-CLEAR-SWITCH is moved to the CLEAR POSITION.
2. Q2 driver turns true during all ϕ 's except ϕ_0 and ϕ_1 .
3. (a) C7 FF turns true at P33 time with C7 prime. "One word time."
 (b) C7 FF turns prime if the "R" register and selection driver FF's (V1 thru V8) do not compare. "If a pre-select or previous block transfer command had preceded this block copy soon enough (minimum 2 drum revolutions) the "R" and "V" FF's would have compared and the "C" counter would be true.
4. (a & b) The selection driver FF's (V) are set by the "R" FF's "Parallel Transfer".
5. (a thru q) If the "C" counter FF's were all set prime by C7' C, at the next P33 time, they would begin the 64 word time count. At the end of 2 drum revolutions C1 thru C6 would be true. This allows time for the relays to set.
6. (a) Uc turns on at P0 time in any ϕ except ϕ_0 with T8 true and T7'.
 (b) Uc turns prime at P33 every word time.
 (c) Uc turns prime when the NORMAL-TEST-CLEAR SWITCH is in the CLEAR position.

NOTE:

These equations are used in conjunction with equation (7a) to keep the computer from being in two ϕ 's (ϕ_2 and ϕ_3) at the same time when the NORMAL-CLEAR SWITCH is in the CLEAR position. Uc prime equation (6c) keeps Q3 from turning on (7a), therefore, preventing ϕ_2 Q3 C which would put both the true and prime inputs to the ϕ_3 FF when the N-T-C SWITCH is in the CLEAR position and then released.

7. (a) Q3 turns on with T7 prime Q2 on in $\phi 2$ with Uc true.
(b & c) Sequences the computer from $\phi 2$ to $\phi 3$.
8. (a) Q3 turns on in $\phi 3$ with Q2 on.
(b & c) Sequences the computer from $\phi 3$ to $\phi 4$.
9. Q3 turns on during P30 time in $\phi 4$ with Q2 on after the "C" counter has counted 2 drum revolutions (C1 C2 C3 C4 C5 C6) and with no block copy alarm A2'.
10. C7 turns prime during $\phi 4$ or $\phi 5$ when C7, Q2 and Q3 are true and T7 prime. "Start of a 32 word count for transfer."
11. (a & b) Sequences the computer from $\phi 4$ to $\phi 5$.
12. Q7 turns true during $\phi 5$ with Q2 true and T7 and T4 prime. "Conditions copying equations."
13. (a & b) H3 FF follows Mr FF "transfer operation".
14. Q3 turns on during P33 time after a 32 word count for transfer (C1 C2 C3 C4 C5 C6) in $\phi 5$ with Q2 on and Md' indicating the reading configuration.
15. C7' turned prime in $\phi 5$. "Resets 'C' counter for 32 word count for checking."
16. (a & b) Sequences the computer from $\phi 5$ to $\phi 6$.
17. (a) Q3 turns true in $\phi 6$ with Q2 true.
(b & c) Sequences the computer from $\phi 6$ to $\phi 7$.
18. (a) X1 turns on at the fall of P33 every word time.
(b) X1 turns prime if there is a mis-match between H2 and Mr from Po thru P32 for 32 word time
19. (a) A2 turns on in $\phi 7$ if an improper block copy took place (X1').
(b) A2 turns prime if the ALARM SWITCH # 1 is in the SILENCE position (Apr) Q2 is true, A2 is true during P33 time in $\phi 7$. "With SW # 1 in the SILENCE position and the remainder of the equation fulfilled the computer will try repeatedly to recopy the information correctly."

19. (c) A2 turns prime if the ALARM SWITCH # 1 is in the RESTORE position (Ap2). "Computer will sequence to ϕ_0 ."
- (d) A2 turns prime if the NORMAL-TEST-CLEAR SWITCH is in the CLEAR position (SC).
20. (a) Q3 turns true during P33 time if ALARM SWITCH # 1 is in the SILENCE position, Q2 is true, A2 is true during ϕ_7 . "Q3 will reset the computer to ϕ_3 and the copying operation will be done repeatedly. When copying is accomplished correctly the computer goes to ϕ_0 ."
- (b & c) Sequences the computer to ϕ_3 .
21. (a) Q4 turns on during P33 time in ϕ_7 after the 32 word count (C1 C2 C3 C4 C5 C6) with Q2 on if X1 is true.
- Note: X1 in this equation takes care of an improper copy of the P32 bit in the last word of the block copy.
- (b & c) Sequences the computer from ϕ_7 to ϕ_0 .

83 Copy to Working Storage II

Equations and explanations identical to the 81 order, page A3, except for the following substitutions:

- | | | | |
|-----|-----|--|------|
| 13. | (a) | $\underline{J3} = (Q7 \phi 2')(T3' T2 C) Mr$ | 1E10 |
| | (b) | $\underline{J3}' = (Q7 \phi 2')(T3' T2 C) Mr'$ | 3E16 |
| 18. | (b) | $\underline{X1}' = J2 (T7' T3' T2 C) (P33' Mr')$ | 3C12 |
| | (c) | $+ J2' (T7' T3' T2 C) (P33' Mr)$ | 4C14 |

85 Copy to Working Storage III

Equations and explanations identical to the 81 order, page A3, except for the following substitutions:

- | | | | |
|-----|-----|---|------|
| 13. | (a) | $\underline{L3} = (Q7 \phi 2') (T3 T2' C) Mr$ | 7E12 |
| | (b) | $\underline{L3}' = (Q7 \phi 2') (T3 T2' C) Mr'$ | 9E4 |
| 18. | (b) | $\underline{X1}' = L2 (T3 T2' C) (P33' Mr')$ | 3C9 |
| | (c) | $+ L2' (T3 T2' C) (P33' Mr)$ | 4C11 |

87 Copy to Working Storage IV

Equations and explanations identical to the 81 order, page A3, except for the following substitutions:

- | | | | |
|-----|-----|--|------|
| 13. | (a) | $\underline{N3} = (Q7 \phi 2') (T3 T2 C) Mr$ | 8A4 |
| | (b) | $\underline{N3}' = (Q7 \phi 2') (T3 T2 C) Mr'$ | 0A11 |
| 18. | (b) | $\underline{X1}' = N2 (T3 T2 C) (P33' Mr')$ | 3C6 |
| | (c) | $+ N2' (T3 T2 C) (P33' Mr)$ | 4C8 |

89 Copy from Working Storage I

Equations and explanations are identical to the 81 order, page A3, except for the following substitutions:

- | | | | |
|-----|-----|--|------|
| 10. | (a) | $\underline{M4} = (T8 T7' T6' T5' T4) \phi 4 Q3 C$ | 9B12 |
| | (b) | $\underline{C7}' = T7' C7 (\phi 4 + \phi 5) Q2 Q3 C$ | 8N14 |
| 11. | (a) | $\underline{\phi 4}' = \phi 4 Q3 C$ | 2U12 |
| | (b) | $\underline{\phi 5} = \phi 4 Q3 C$ | 2U12 |

- | | | | |
|-----|-----|--|------|
| 12. | (a) | $\underline{M}_D = (T_3' T_2') (\phi_5 \text{ Md}) \text{ Os He}$ | 9F13 |
| | (b) | $+ M_p' \text{ Os}' (\phi_5 \text{ Md})$ | OE10 |
| | (c) | $\underline{M}_D' = (T_3' T_2') (\phi_5 \text{ Md}) \text{ Os He}'$ | 8F16 |
| | (d) | $+ M_p \text{ Os}'$ | OE12 |
| | (e) | $\underline{M}_O = (T_3' T_2') (\phi_5 \text{ Md}) \text{ Os He}'$ | 8F16 |
| | (f) | $+ M_o' \text{ Os}' (\phi_5 \text{ Md})$ | OE7 |
| | (g) | $\underline{M}_O' = (T_3' T_2') (\phi_5 \text{ Md}) \text{ Os He}$ | 8F13 |
| | (h) | $+ M_o \text{ Os}'$ | OE14 |
| 13. | | $\underline{M}_d' = (C_1 C_2 C_3 C_4 C_5 C_6) \phi_5 F_5 F_2' F_1 C$ | 8M5 |

DESCRIPTION:

10. (a) Md FF turns true at the fall of P30 time in ϕ_4 . "Sets writing conditions."
 (b) C7 turns prime during ϕ_4 or ϕ_5 when C7, Q2 and Q3 are true and T7 prime "Start of a 32 word count for transfer."
11. (a & b) Sequences the computer from ϕ_4 to ϕ_5 .
12. (a thru h) Refer to Ferranti System Write up.
13. Md turns prime at P30 time during ϕ_5 . "Sets reading conditions."

8B Copy from Working Storage II

Equations and explanations are identical to the 89 order, page A8, except for the following substitutions.

- | | | | |
|-----|-----|--|------|
| 12. | (a) | $\underline{M}_D = (T_3' T_2) (\phi_5 \text{ Md}) \text{ Os Je}$ | 8F2 |
| | (b) | $+ M_p' \text{ Os}' (\phi_5 \text{ Md})$ | OE10 |
| | (c) | $\underline{M}_D' = (T_3' T_2) (\phi_5 \text{ Md}) \text{ Os Je}'$ | 9F10 |
| | (d) | $+ M_p \text{ Os}'$ | OE12 |
| | (e) | $\underline{M}_O = (T_3' T_2) (\phi_5 \text{ Md}) \text{ Os Je}'$ | 7F4 |
| | (f) | $+ M_o' \text{ Os}' (\phi_5 \text{ Md})$ | OE7 |
| | (g) | $\underline{M}_O' = (T_3' T_2) (\phi_5 \text{ Md}) \text{ Os Je}$ | 7F4 |
| | (h) | $+ M_o \text{ Os}'$ | OE14 |
| 18. | (b) | $\underline{X}_1' = J_2(T_7' T_3' T_2) (P_{33}' M_r')$ | 3C12 |
| | (c) | $+ J_2' (T_7' T_3' T_2) (P_{33}' M_r)$ | 4C14 |

8D Copy from Working Storage III

Equations and explanations are identical to the 89 order,
page A8 except for the following substitutions:

12.	(a)	$\underline{M_p} = (T_3 T_2') (\phi_5 Md) Os Le$	8F7
	(b)	$+ M_p' Os' (\phi_5 Md)$	OE10
	(c)	$\underline{M_p}' = (T_3 T_2') (\phi_5 Md) Os Le'$	8F10
	(d)	$+ M_p Os'$	OE10
	(e)	$\underline{M_o} = (T_3 T_2') (\phi_5 Md) Os Le'$	8F10
	(f)	$+ M_o' Os' (\phi_5 Md)$	OE7
	(g)	$\underline{M_o}' = (T_3 T_2') (\phi_5 Md) Os Le$	8F10
	(h)	$+ M_o Os'$	OE14
18.	(b)	$\underline{X_1}' = L_2 (T_3 T_2' C) (P_{33}' Mr')$	3C9
	(c)	$+ L_2' (T_3 T_2' C) (P_{33}' Mr)$	4C11

8F Copy from Working Storage IV

Equations and explanations are identical to the 89 order,
page A8 except for the following substitutions:

12.	(a)	$\underline{M_p} = (T_3 T_2) (\phi_5 Md) Os Ne$	9F16
	(b)	$+ M_p' Os' (\phi_5 Md)$	OE10
	(c)	$\underline{M_p}' = (T_3 T_2) (\phi_5 Md) Os Ne'$	9F13
	(d)	$+ M_p Os'$	OE12
	(e)	$\underline{M_o} = (T_3 T_2) (\phi_5 Md) Os Ne'$	9F13
	(f)	$+ M_o' Os' (\phi_5 Md)$	OE7
	(g)	$\underline{M_o}' = (T_3 T_2) (\phi_5 Md) Os Ne$	9F16
	(h)	$+ M_o Os'$	OE14
18.	(b)	$\underline{X_1}' = N_2 (T_3 T_2 C) (P_{33}' Mr')$	3C6
	(c)	$+ N_2' (T_3 T_2 C) (P_{33}' Mr)$	4C8

C1 Store Index in Address

- | | | | |
|----|-----|--|------|
| 1. | (a) | $\underline{Q8} = (T8 T7 T6' T5' T4' T3') Ee C$ | 5G6 |
| | (b) | $\underline{Q8}' = (\quad " \quad) Ee' C$ | 9G6 |
| 2. | | $\underline{Q7} = (\quad " \quad) (T2 + F3') \phi 2 Vw F4$ | 5G11 |

Equations and explanations from this point are identical to the 49 order (3a thru 3p) Page 19.

- | | | | |
|----|-----|--|------|
| 4. | (a) | $\underline{Er} = T8 (En C \phi 0')$ | 9C13 |
| | (b) | $\underline{Er}' = T8 (En' C \phi 0')$ | 1B14 |
| 5. | (a) | $\underline{Q4} = (T8 T7 T6' T5') \phi 2 Vw P33$ | QJ4 |
| | (b) | $\underline{\phi 2}' = Q4 C$ | 1U16 |
| | (c) | $\underline{\phi 0} = Q4 C$ | 1U16 |

DESCRIPTION:

1. (a & b) Q8 FF follows Ee with a C1 order in the "T" register.
2. Q7 turns on during the MSH address portion of Vw.
4. (a) Recirculates the "E" line normally by passing the one's.
(b) Same as (a) but passes the zero's.
5. (a) Q4 turns on during P33 of the selected word (Vw) during $\phi 2$.
(b & c) Sequences the computer from $\phi 2$ to $\phi 0$.

C9 Pre-Select

- | | | | |
|----|-----|---|-------------------------|
| 1. | | $\underline{Q2} = \phi 2 (T8 T7 T6' T5' T4 T3' T2')$ | OM6 |
| 2. | (a) | $\underline{C7}' = (\phi 2 C7 Q2) (Ri Vi' + Ri' Vi) C$ | --- |
| | (b) | $\underline{C7} = C7' P33 C$ | 5N30 |
| 3. | (a) | $\underline{Vi} = (\phi 2 C7' Q2) Ri C$ | (i = 1 thru 8 FF's) --- |
| | (b) | $\underline{Vi}' = (\quad " \quad) Ri' C$ | --- |
| 4. | (a) | $\underline{C1} = (C7 P33 C) C1'$ | 4N16 |
| | (b) | $\underline{C1}' = (\quad " \quad) C1 (C2' + C3' + C4' + C5' + C6')$ | 4N11 |
| | (c) | $+ C7' C$ | 4N2 |

4.	(d) $\underline{C2} = (C7 P33 C) C1 C2'$	5N16
	(e) $\underline{C2}' = (C7 P33 C) C1C2 (C2' + C3' + C4' + C5' + C6')$	5N13
	(f) $+ C7' C$	4N2
	(g) $\underline{C3} = (C7 P33 C) C1 C2 C3'$	5N11
	(h) $\underline{C3}' = (C7 P33 C) C1C2C3 (C2' + C3' + C4' + C5' + C6')$	5N9
	(i) $+ C7' C$	4N2
	(j) $\underline{C4} = (C7 P33 C) C1 C2 C3 C4'$	5N2
	(k) $\underline{C4}' = (C7 P33 C) C1C2C3C4 (C2' + C3' + C4' + C5' + C6')$	7L14
	(l) $+ C7' C$	4N2
	(m) $\underline{C5} = (C7 P33 C) C1 C2 C3 C4 C5'$	7L12
	(n) $\underline{C5}' = (C7 P33 C) C1 C2 C3 C4 C5 C6'$	7L10
	(o) $+ C7' C$	4N2
	(p) $\underline{C6} = (C7 P33 C) C1 C2 C3 C4 C5 C6'$	7L8
	(q) $\underline{C6}' = C7' \phi 2 C$	7L7
5.	(a) $\underline{Q4} = T7 Q2 \phi 2 P33$	OEE16
	(b) $\phi 2' = Q4 C$	1U16
	(c) $\underline{\phi 0} = Q4 C$	1U16

DESCRIPTION:

This operation pre-selects a MM Channel for future use. Although only one Msec is required to set the selection flip flops (V1 through V8), 32 Msec are required for the selection relays to set. A 32 Msec interlock is used to prevent premature transfers due to a transfer command being given less than 32 Msec after a pre-select command. The logic is so written that nothing is lost except time if a premature block transfer command is given.

- Q2 turns true in $\phi 2$.
- If C7 is prime, it is turned true at the fall of the P33.
 - In $\phi 2$, whenever C7 is true, it is turned prime if the "V" register and the "R" register do not compare.
- In $\phi 2$ Vi follows Ri and Vi' follows Ri'. . Parallel transfer of the information in "R" flip flops to the "V" flip flops.

4. (a thru 1) C7 prime turns C1, C2, C3, C4, C5 and C6 prime.
 "C" counter begins counting up to 64. "Since each counter will count only at P33 time total count is 64 word times or two drum revolutions."
5. (a) Q4 comes up with Q2 in $\phi 2$ and sequences computer to $\phi 0$. "Computer has been in $\phi 2$ for one word time."

CB Store A in M (C9 order is a pre-requisite)

- | | | | |
|-----|---|----|-------|
| 1. | <u>Um</u> = (T8 T7 T6' T5' T4 T3' T2) $\phi 1$ Q3 C | NO | 8M9 |
| 2. | (a) <u>R1</u> = (Um $\phi 2$ P32 C) R1' | ok | 3DD12 |
| | (b) <u>R1'</u> = (Um $\phi 2$ P32 C) R1 | | 3DD10 |
| | (c) <u>R2</u> = (Um $\phi 2$ P32 C) R1' R2' | | 4DD10 |
| | (d) <u>R2'</u> = (Um $\phi 2$ P32 C) R1' R2 | | 4DD8 |
| | (e) <u>R3</u> = (Um $\phi 2$ P32 C) R1' R2' R3' | | 5DD14 |
| | (f) <u>R3'</u> = (Um $\phi 2$ P32 C) R1' R2' R3 | | 5DD12 |
| | (g) <u>R4</u> = (Um $\phi 2$ P32 C) R1' R2' R3' R4' | | 5DD2 |
| | (h) <u>R4'</u> = (Um $\phi 2$ P32 C) R1' R2' R3' R4 | | 6DD16 |
| | (i) <u>R5</u> = (Um $\phi 2$ P32 C) R1' R2' R3' R4' R5' | | 6DD14 |
| | (j) <u>R5'</u> = (Um $\phi 2$ P32 C) R1' R2' R3' R4' R5 | | 6DD11 |
| | (k) <u>R6'</u> = (Um $\phi 2$ P32 C) R1' R2' R3' R4' R5' | | 6DD13 |
| 3. | <u>Um'</u> = (T8 T7 T6' T5' T4 T3' T2)($\phi 2$ P32 C) | NO | 9M5 |
| 4. | <u>Vr'</u> = (" ") (") | NO | 9M5 |
| 5. | <u>A2</u> = (T8T7T6'T5'T4T3'T2)($\phi 2$ P32 C)(V1V2'V3'V4'V5'V6'V7'V8') | NO | 9YY10 |
| 6. | (a) <u>Q3</u> = (T8 T7 T6' T5' T4 T3' T2) $\phi 2$ P32 | NO | 6Q8 |
| | (b) <u>$\phi 2'$</u> = $\phi 2$ Q3 C | | 2U14 |
| | (c) <u>$\phi 3$</u> = $\phi 2$ Q3 C | | 2U14 |
| 7. | <u>Q3</u> = (T8T7T6'T5'T3'T2)A2' Vw Or' $\phi 3$ (C1C2C3C4C5C6)F5F2'F1 | NO | 2N14 |
| 8. | <u>Md</u> = (" ") $\phi 3$ Q3 C | NO | 8M10 |
| 9. | (a) <u>$\phi 3'$</u> = $\phi 3$ Q3 C | | 2U12 |
| | (b) <u>$\phi 4$</u> = $\phi 3$ Q3 C | | 2U12 |
| 10. | (a) <u>Mo</u> = ($\phi 4$ Md) Os' Mo' | | 9H6 |
| | (b) + ($\phi 4$ Md) Os Abl' | | 9H13 |
| | (c) <u>Mo'</u> = Os' Mo | | OE14 |
| | (d) + ($\phi 4$ Md) Os Abl | | 9H11 |
| | (e) <u>Mp</u> = ($\phi 4$ Md) Os' Mp' | | 9H4 |
| | (f) + ($\phi 4$ Md) Os Abl | | 9H10 |
| | (g) <u>Mp'</u> = Os' Mp | | OE12 |
| | (h) + ($\phi 4$ Md) Os Abl' | | 9H12 |

11.	$Q_2 = (T_8 T_7 T_6' T_5' T_4 T_3' T_2) \phi_0' \phi_1' \phi_2' \phi_3' \phi_6'$	1N7 No
12.	$Q_3 = (C_1 C_2 C_3 C_4 C_5 C_6) \phi_4 Q_2 A_2' F_5 F_2' F_1$	4N11 OK
13.	$M_d' = (T_8 T_7 T_6' T_5' T_4 T_3' T_2) \phi_4 Q_3 C$	9M15 No
14.	(a) $\phi_4' = \phi_4 Q_3 C$	2U8
	(b) $\phi_5 = \phi_4 Q_3 C$	2U8
15.	(a) $Q_3 = (C_1 C_2 C_3 C_4 C_5 C_6) \phi_5 Q_2 A_2' P_{33}$	9YY1
	(b) $\phi_5' = \phi_5 Q_3 C$	2U6
	(c) $\phi_6 = \phi_5 Q_3 C$	2U6
16.	(a) $Q_3 = (T_8 T_7 T_6' T_5' T_4 T_3' T_2) \phi_6 V_w \phi_r' P_{33}$	9B10 No
	(b) $\phi_6' = \phi_6 Q_3 C$	2U4
	(c) $\phi_7 = \phi_6 Q_3 C$	2U4
17.	(a) $X_1 = P_{33} C$	2C3
	(b) $X_1' = T_7 P_{33}' An' Mr C$	1N16 No
	(c) $+ T_7 P_{33}' An Mr' C$	1N10 No
18.	(a) $A_2 = (T_8 T_6' T_5') \phi_7 X_1' C$	5C4
	(b) $A_2' = Apr Q_2 \phi_7 A_2 P_{33} C$	4E12
	(c) $+ Ap_2 C$	6C11
	(d) $+ SC$	6C9
19.	(a) $Q_3 = Apr Q_2 A_2 \phi_7 P_{33}$	4E13
	(b) $\phi_7' = \phi_7 Q_3 C$	2U9
	(c) $\phi_3 = \phi_7 Q_3 C$	2U9
20.	(a) $Q_4 = (C_1 C_2 C_3 C_4 C_5 C_6) \phi_7 Q_2 A_2' X_1 P_{33}$	9I12 No
	(b) $\phi_7' = Q_4 C$	1U16
	(c) $\phi_0 = Q_4 C$	1U16

DESCRIPTION:

1. With a CB order in the "T" register U_m turns on at $\phi_1 Q_3 C$.
2. (a thru k) At the fall of P_{32} in ϕ_2 with U_m true the "R" register counts down by 1.
 Note: This will set the "R" register to the address of one word time previous to the one stipulated to be written into.
3. U_m turns prime at P_{32} in ϕ_2 .
4. V_r turns prime at P_{32} in ϕ_2 .
5. A_2 alarm turns true at P_{32} in ϕ_2 if the V flip flops are set to MM Channel 01. "Protects against a block copy into MM 01 where the start routine is stored."

6. (a) Q3 driver turns true during P32 time in $\phi 2$.
(b & c) Sequences the computer from $\phi 2$ to $\phi 3$.
7. Q3 driver turns true during P30 in $\phi 3$ if the "C" counter has counted up. "If the "C" counter has not counted up the computer waits in $\phi 3$ until it does.
8. Md turns true at the fall of P30 during the selected word time Vw in $\phi 3$. "Sets the circuitry to writing configuration.
9. (a & b) Sequences the computer from $\phi 3$ to $\phi 4$.
10. (a thru h) Refer to Ferranti system write up. "Mp and Mo flip flops accept information from Abl at P31 time. At P31 time Abl contains the P33 bit."
11. Q2 comes up during $\phi 4$. "Used in sequencing equations."
12. Q3 turns true during P30 of the selected word time Vw in $\phi 4$.
13. Md turns prime in $\phi 4$. "Sets circuitry to the read configuration."
14. (a & b) Sequences the computer from $\phi 4$ to $\phi 5$.
15. (a) Q3 turns on during P33 time in $\phi 5$.
(b & c) Sequences the computer from $\phi 5$ to $\phi 6$.
16. (a) Q3 turns true during P33 time in $\phi 6$ during the selected word time (Vw $\phi r'$)
(b & c) Sequences the computer from $\phi 6$ to $\phi 7$.
17. (a) X1 turns true at the fall of P33 every word time.
(b) X1 turns prime if there is a mis-match between An and Mr. Checking bit by bit.
(c) X1 turns prime if there is a mis-match between An and Mr. Checking bit by bit.
18. (a) A2 is turned true in $\phi 7$ if an improper copy has been made (X1').
(b) A2 turns prime if the ALARM SWITCH # 1 is in the SILENCE position (Apr), Q2 is true, A2 is true at P33 time in $\phi 7$. "Allows computer to sequence to repeat the block copy."

18. (c) A2 turns prime if ALARM SWITCH #1 is in the RESTORE position (Ap2). Computer will sequence to ϕ_0 and ignore poor copy.
- (d) A2 turns prime if the NORMAL-TEST-CLEAR SWITCH is in the CLEAR position (S).
19. (a) Q3 turns true during P33 time if the ALARM SWITCH #1 is in the SILENCE position and other conditions present.
- (b & c) Sequences the computer from ϕ_7 to ϕ_3 . Repeats copy operation.
20. (a) Q4 turns true during P33 in ϕ_7 if a proper copy was made (A2') and the "C" counters have counted.
- (b & c) Sequences the computer from ϕ_7 to ϕ_5 .

FLB/ic
3 September 1958