Concurrent Computer/Perkin-Elmer compatible

DR11-W DEC LINK MANUAL

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INCLUDES: INSTALLATION SPECIFICATION PROGRAMMING SPECIFICATION MAINTENANCE SPECIFICATION SCHEMATICS

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DR11-W DEC LINK

1. INTRODUCTION

Macrolink's DR11-W/DEC LINK provides a high-speed processor-to-processor communication path. The LINK is protocol compatible with the DEC DR11-W interface, and was developed to facilitate high-speed communications between the 3200 CPU and DEC family of computers. The LINK may also be used between two 3200 processors.

Macrolink provides an OS/32 driver package with the LINK modules. This is a comprehensive software package that allows two OS/32 users to communicate using standard system software (COPY32, etc). The LINK driver may be used as an outline to develop hardware specific drivers for DR11-W compatible devices. User-developed software does exist to connect 3200 series to DEC PDP-11 computers. Please contact Macrolink if you need additional assistance with your driver software.

The DR11-W LINK is contained on a 7" x 15" halfboard that may be installed in any available I/O slot of a 16-bit or 32-bit 3200 compatible computer, however it is advisable to install it on a selector channel bus. Two 40 conductor flat cables directly connect the LINK to its companion communication module in the remote computer. These cables may be up to 50 feet long.

Data may be transferred in a 16-bit half duplex format up to one megabyte per second (limited by the DR11-W interface). Either the local or remote computer may initiate an exchange, and error reporting status is provided to insure data integrity.

Macrolink also supplies a high-speed version of the LINK just for 3200 series applications. The High Speed 3200 Link offers extended cable length (over 1000 feet) and higher speed transfers.

1.1 Standard Operation

The LINK allows programmed or DMA data transfers between 3200 series and DEC computers. Transfers may be initiated in either direction by either computer. Both interfaces default to receive mode after initialization.

In word mode, data is passed between computers word by word, with each exchange transferred by interrupts or status bits. In block or DMA mode of operation, the data exchange is controlled by the DMA hardware of each computer.

Introduction (Continued)

1.2 Product Specifications

Accessible Registers Status

Command Data Buffer

Word Size 16-Bits Parallel

Operating Modes Word, DMA Block

Maximum Block Length Limited only by SELCH

Block Transfer Method Under SELCH control

Transfer Direction Bidirectional, Half-Duplex

Address Switch Selectable (Recommend X'60')

Inter-connection Cable 2 40-pin flat cables up to 50 ft. Pin

compatible DR11-W connectors

Transfer rate (Block Mode) 1 Megabyte per second

or limited by DR11-W

Loop-Back Capabilities Standard Cables or

test cable

Bus Load 1/2 unit load, maximum

Mechanical One standard 3200 Half-board

Installation Compatible with standard

Halfboard mounting kit.

Power 5VDC at 1 Amp

INSPECTION AND INSTALLATION

2.1 Packaging

The Macrolink DR11-W LINK is normally shipped with two 40-pin shielded ribbon cables 20 feet each in length. It is packed in accordance with commercial practices using antistatic packaging material to cushion the LINK during shipment.

2.2 Unpacking

Inspect the outside of the package for any signs of damage that may have caused damage to its contents. If the package has been damaged, make a record of the type and extent of damage.

If the LINK or cables have been damaged during shipment, request that the carrier's agent inspect the damage and file a claim with the carrier. Usually the claim must be filed within seven days after receipt of the package.

Open the package and remove all packing material. Check the package contents against the shipping invoice (packing list) normally attached to the outside of the shipping container. Inspect all parts carefully. Inspect the LINK board for any loose or broken parts. Inspect cable assemblies for broken connector housing or other damage.

Notify MACROLINK INC. of any discrepancies between invoice and received material or of any damage found during inspection within 10 days.

2.3 Return Material Authorization

To return a product for repair, you must obtain a Return Material Authorization (RMA) number from Macrolink. This number must be on the outside of the shipping container, or the shipment will be refused.

When requesting an RMA number, please have the following information ready:

- 1. Product name or part number.
- 2. Serial Number.
- 3. Failure description.

Shipping expenses to Macrolink must be paid by you. We will pay for standard shipment back to you for products under warranty. Macrolink products are normally covered by a 12 month limited warranty. Full details are in our Terms and Conditions.

2.4 Board Installation

The LINK is a halfboard and therefore must be strapped to a blank or active halfboard to be installed directly into the 3200 series processor. The LINK should be on the LEFT side of the chassis, when viewed from the front.

IMPORTANT

Prior to installing the LINK, make sure that the address and switch settings are correct. Refer to the instructions on switch settings in the following paragraphs.

The LINK should be supported by a Selector Channel (3200 SELCH or BSELCH) and therefore is installed below the Selector Channel board so the LINK will be on the SELCH private bus (connector "1" side). Locating the LINK under a Selector Channel board is not mandatory, but it is the only way to achieve maximum throughput. The Macrolink supplied software MUST be used with a SELCH.

2.5 RACKO/TACKO

The CPU backplane must have the RACKO/TACKO wire wrap jumper between pins 122-1 and 222-1 REMOVED at the slot location that is used for the MACROLINK LINK.

2.6 Interface Cables

The cable-to-board connectors are of the 3M polarized type. The connectors for the cables have cable-locking clips that are engaged to retain the female 3M connector on the cable.

IMPORTANT

It is easy to incorrectly exchange the LINK cables. When two Macrolink DR11-W LINK modules are interconnected, Pl of the first module should be connected to P2 of the second, P2 of the first to P1 of the second. Also insure that pin 1 of the cable is connected to pin 1 of the connector.

2.7 Device Address Selection

The device address is determined by the two switches (MSD and LSD) located along the right hand side of the board. The switch labeled MSD selects the Most Significant Digit of the device address, and the switch labeled LSD selects the Least Significant Digit. For example, to make a board respond to address X'60', set MSD to 6 and LSD to 0.

DR11-W LINK PROGRAMMING

3.1 Processor I/O Instructions

There are five types of processor I/O instructions used to communicate between the P-E LINK and the 3200 processor. These instructions are sent on a byte or halfword I/O basis.

- 1. SENSE STATUS (SS or SSR) Used to receive the status information from the LINK. This is a byte instruction.
- 2. OUTPUT COMMAND (OC or OCR) Generates control signals, selects the mode of operation and is used to initialize the SELCH.
- 3. WRITE HALFWORD (WH or WHR) Loads the LINK with a halfword of data. Also used to load the SELCH address registers.
- 4. READ HALFWORD (RH or RHR) Reads a halfword of data from the LINK.
- 5. ACKNOWLEDGE INTERRUPT (ACK or ACKR or AI or AIR) This activates the interrupt priority chain (RACKO/TACKO). It is used to find the address of the highest priority device that is currently interrupting (on 32-bit processors, this is done automatically, and these instructions are illegal).

3.2 Command Register

The command register contains 8 bits, (08-15). Refer to Figure 2.

DR11-W LINK COMMAND REGISTER FUNCTIONS

BITS:	8	9	10	11	12	13	14	15
	DISABLE	ENABLE	DATA/ CNTRL	CLEAR	FNCT3	FNCT2	FNCT1	GO

FIGURE 2.

Bits 08 and 09 are used to enable, disable and disarm the interrupt capability of the LINK. There are 4 possible combinations:

BIT 8	BIT 9	FUNCTION
0	0	No Change in interrupt function
1	0	Disable interrupts (queue interrupts)
0	1	Enable interrupts
1	1	Disarm interrupts

The other bits take on the following meanings:

Bit	Name	Function
10	DATA/ CONTROL	Set for DMA transfers Clear for interrupt driven transfers.
11	CLEAR	Clears DR11-W LINK controller logic.
12,13,14	FUNCTION REGISTER	FUNCTION Output of this 3 bit register is presented to the outside device as 3 general purpose control lines.
15	GO	Setting this bit causes a pulse to be issued on the GO H interface line. In data (DMA) mode, this bit causes the busy flag in the 3200 status word to clear if the controller has been selected as a transmitter by holding the C1H interface signal low.

For DR11W/VAX LINK applications, the function lines have special meanings. These are as follows:

Bit	Name	Function
12	BLOCK/BURST FNCT3	Set = Block mode Clear = burst mode (no meaning in this controller).
13	INTERRUPT FNCT2	Set to interrupt corresponding computer. This bit is pulsed by software to interrupt VAX computer.
14	DIRECTION FNCT1	Set = this controller is the receiving controller. Clear = this controller is the transmitting controller.

3.3 Status Register

The status register contains 8 bits, (08-15). Refer to Figure 3.

SERIES 3200 STATUS REGISTER

BITS	8	9	10	11	12	13	14	15
	ATTN	STAT A	STAT B	STAT C	BUSY	EXAMINE		DEVICE UNAVAILABLE

FIGURE 3.

Bit	Name	Function
15	DEVICE UNAVAILABLE	Set if either cable is not plugged in at both ends.
14	ЕОМ	Set following completion of a data transfer, or whenever a transfer is halted.
13	EXAMINE	Set whenever ATTN bit is set.
12	BUSY	Active in data mode only. Held set in control mode. Busy is set whenever data is not available to the 3200 computer. Busy is clear whenever this controller is ready to transfer data to the 3200 computer.
9,10,11	STATUS A,B,C	General purpose status input lines.
8	ATTENTION	This bit is latched set each time Attention input to the controller goes high. It is reset after it has been read by a 'read status' operation.

In DR11-W/VAX LINK applications, the STATUS lines are connected to the FUNCTION REGISTER of the other computer. STATUS C to FNCT1, STATUS B to FNCT2, and STATUS A to FNCT3.

They also have the following meanings:

Bit	Name	Function
9	BLOCK/BURST	The opposite computer is in the BLOCK/BURST mode.
10	INTERRUPT	This bit shows the condition of the opposite computer's FNCT line. Since this line is only pulsed, it should not be relied upon for valid status.
11	DIRECTION	This bit shows the opposite computer's operating mode (transmitter or receiver): Set = receiver, Clear = transmitter

3.4 Interrupts

3.4.1 LINK Interrupts

The LINK interrupts the processor only when the interrupts are enabled. Interrupts occur on the following conditions:

ATTN status sets
BUSY status resets
EOM status sets
DU status sets or resets

3.4.2 SELCH Interrupts

SELCH interrupts are always enabled. When the SELCH terminates a transfer and goes into the idle state, it generates an interrupt. For more information on SELCH programming, please refer to the SELCH programming manual that is appropriate for your type of SELCH.

SCHEMATIC DESCRIPTION

4.1 Introduction

The DR11-W LINK provides an interface between a 3200 series processor MUX bus and an external device with DR11-W protocol. This section will provide the user with an understanding of the operation of the LINK. It is suggested that Chapter 3 be read before reading this chapter. References are made to the schematics using a location designation format of XYZ, where X is the sheet number, YZ are page coordinates.

4.2 MUX Bus Interface

The MUX bus interface consists of the following items:

Address decoding Command decoding SYNC return Status/Address multiplexors RACKO TACKO Data Path

4.2.1 Address Decoding

U16, U20, U13, U36, U23, and the switches MSD and LSD (sheet 1) comprise the address decoding circuitry. When the address on the bus matches the setting of LSD and MSD, the output of U20 goes low. The signal ADRSO clocks the ADRS F/F (1A1) set. When the address on the bus does not match, the signal ADRSO clocks the ADRS F/F reset.

4.2.2 Command Decoding

The signal CMD0 (3C4) clocks the command register. Bits 08 and 09 are clocked into U8 (3B3) on the trailing edge of CMDG0. These 2 bits control the interrupt circuitry. Bits 10, 12, 13 and 14 are clocked into the F/F's U33 (4D2), U43 (4D2) and U27 (4D2). Bit 10 is the DMA mode bit and bit 12, 13 and 14 are the function bits. Bit 11 is anded with CMG1 to produce SINIT1 (3C1). Bit 15 is anded with CMG1 (4B2) and fires the GOPLS1 F/F on the trailing edge of CMG1.

4.2.3 Sync Return

U16 (3C3), U15 (3C2), U29 and U28 (3C2), and U1 (3C1) comprise the sync return circuitry. U16 and U15 are used to detect that one of the six control tags are active. When one of the control tags goes active, U15 pin 8 goes high. This fires the one-shot U29 and releases the reset on the F/F U28. When U29 times out, it clocks U29 set. This causes SYNO (3C1) to go active. When the control tag is removed, U15 pin 8 goes low reseting U29.

4.2.4 Status/Address Multiplexors

U17 (1C2) and U18 (1B2) comprise the status / address multiplexors. In the default mode they output the device address. When a status request operation is performed, SRG0 changes the select causing them to output the device status. When DRG1 goes active, their outputs are disabled (tri-stated) allowing the data to be placed on the bus.

4.2.5 RACKO/TACKO

The lower half of sheet 3 of the schematics contains the interrupt circuitry. When RACKO goes active, either TACKO (3B1) or ATSYNO (3B1) will go active. If the interrupt enable F/F U8 pin 9 (3B2) is set and the interrupt F/F U28 (3A2) is also set, RACKO will cause the U14-U9 latch (3B2) to reset (U9 pin 8 high) which will cause ATSYNO to go active. If either F/F is reset, the U14-U9 latch will set, causing TACKO to go active.

4.2.6 Data Path

The data path is 16 bits wide and is divided into 2 bytes, the Least Significant (LS) byte and the Most Significant (MS) byte. When transferring data from the CPU to the DR11-W bus, the LS byte goes from the 3200 MUX bus to the bus receivers (D4), to the DEC register (A2), to the output drivers (A1), and out the DR11-W bus. The MS byte goes from the 3200 MUX bus to the receivers (C4), to the DEC register (A2), to the output drivers (A1), and out the DR11-W bus. When transferring data from the DR11-W bus to the 3200 MUX bus, the data goes from the DR11-W bus, to the bus drivers (B3 and C3), and out the MUX bus.

The left side of sheet 1 contains the receivers for the least significant byte (LS byte) of the MUX bus, U4 and U5. The right side of sheet 1 contains the drivers for the LS byte, U11 and U12. U4 and U5 feed the data register on sheet 5 on the left side, where it gets clocked in by DAG1 and then sent out on the DR11W bus. U40 (2C2) and U13 (2B2) comprise the receivers for the MS byte of the MUX bus, which feed the data register on sheet 5. Data is received from the DR11W bus by the receivers U51 and U52 on sheet 6, which feeds the LS byte drivers on sheet 1 and the MS byte drivers on sheet 2 (U37 and U38).

4.3 DR11-W Interface

The DR11-W interface section of the module consists of the following:

Control Input Lines Control Output Lines Data lines

4.3.1 Control Input Lines

The control input lines are received by U53 (right side of sheet 4). STATA, STATB, STATC are sent to the status/address mux as status bits.

CYCREQA and CYCREQB are or'd together by U42 (4C3), passed through a positive edge detector formed by U32 and U39 (4C3), which after the delay of the detector,

clocks the busy F/F. This clock will reset PBUSY1 if the DMA mode F/F is set.

ATTN (4C4) feeds through inverter U46 and direct sets the first stage of the ATTN status register U21 (4C3). This register is a "read then reset" register. The purpose of this register is to hold the ATTN status until it is read by the host CPU. U21-5 when set, will remain set until a status request is made. The leading edge of the status request will clock it into the second stage where it is sent to the status / address mux. The trailing edge of SRG0 will cause the first stage to reset providing the ATTN input has become inactive. When U21-5 goes from reset to set its Q-not side feeds into a negative edge detector formed by U42 and U39 (4A3). The output of the detector feeds into the interrupt circuitry.

P1-CABLE and P2-CABLE are the open cable detect signals. If both of them are low, DEVAVO (4B3) goes active indicating that the device is available. DEVAVO is fed into the status / address mux and also into a universal edge detector. The output of this detector feeds into the interrupt circuitry, interrupting on either edge of DEVAVO.

4.3.2 Control Output Lines

The control output lines are driven by U50 (right side of sheet 4). FNCT1, FNCT2, and FNCT3 are derived from the FNCT command registers. ACLOFNCT2 is derived from the FMCT2 function register.

BUSY is high as long as the board is not in DMA mode. When the board is in DMA mode, it is the same as the PBUSY1 F/F.

GO is a high active pulse derived from the GO one-shot, which fires whenever the board receives a GO command.

READY is produced by F/F U23 (4B2). U23 is reset when a GO command is issued with DMA mode set, via U25-6 (4A3). It is set whenever the EOM status bit sets, indicating the end of a DMA type transfer.

4.3.3 Data Path

The data transmitters U55 and U54 (sheet 5) output the data held in the data register U48 and U47). The data receivers feed straight into the MS byte (sheet 2) and LS byte (sheet 1) MUX bus transmitters.

4.4 Link Mode Operation

When the LINK is connected to a DR11-W or another LINK it is said to be in "link" mode. In link mode the P1 cable of one LINK is connected to the P2 cable of the other LINK and vice-versa. This causes the following connections to occur:

Schematic Description (Continued)

STATA	to	FNCT3
STATB	to	FNCT2
STATC	to	FNCT1
CYCREQA	to	BUSY not
CYCREQB	to	GND
ATTN	to	FNCT2
P1-CABLE	to	GND
P2-CABLE	to	GND

These connections occur from one board to the other and vice-versa. Also FNCT1 is fed back to the same board's C1H line which determines if the board is in transmit mode or receive mode.

When FNCT2 is set it activates ACLOFNCT2H (4C1) which goes to the other board as ATTN, generating an interrupt.

DMA transfers are initiated by a command with DMA and GO set. If FNCT1 is clear this will cause C1H to be low which will cause U42-6 (4C2) to go low resetting the PBUSY1 F/F.

During transmit mode, FNCT1 is reset so the PBUSY1 F/F (4C2) will be reset by the go pulse. This will cause the SELCH to send a halfword of data to the board with the DAG0 pulse. The positive edge detector formed by U32 and U46 (4C3) will set the PBUSY1 F/F on the trailing edge causing a low active pulse to be sent out on the BUSY H' interface signal (4B1). This will cause the other board to respond in the same manner, causing the CYCREQB signal coming back into the board to pulse low. The positive edge detector formed by U32 and U39 (4C3) will generate a pulse which will reset the PBUSY1 F/F. This will cause the cycle to repeat itself for as many times as there are halfwords to be transmitted.

Receive mode works the same as transmit mode, with the exception that the PBUSY1 F/F does not get reset by the go pulse, because FNCT1 is set during receive mode. This causes the SELCH to wait for the the other board to send a halfword before reading it from the board.

The EOM1 F/F (4A4) detects when the CYCREQA - BUSY H' handshake stops. EOM1 is reset by INITO or GOPLSO. Every time PBUSY1 goes low it fires the one-shot U29 (4A4). When the PBUSY F/F stops toggling, the one-shot times out (approx. 100ms) and sets the EOM F/F.

. MAINTENANCE

5.1 Preventative Maintenance

There is no preventative maintenance required on the MACROLINK DR11-W /DEC LINK.

5.2 Diagnostics

The LINK TEST PROGRAM is used to perform diagnostics on the LINK. For information on how to use this program, please refer to the LINK TEST PROGRAM MANUAL.

5.3 Board Maintenance

IMPORTANT - Any repairs or modifications made to the board without MACROLINK's written approval voids any warranties express or implied. Also, product warranties do not apply to products subjected to unusual physical or electrical stress or improper installation.

When performing repairs on the board, it is important to familiarize yourself with the theory of operation in this manual, and the fault locating guide in the LINK TEST PROGRAM.













