GER-100 CRT CONTROLLER MANUAL NO. 10024M0-01-0



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Schematics and Drawings

Appendix B

GER-100 CRT CONTROLLER MANUAL NO. 10024M0-01-0



# 1.0 SPECIFICATIONS:

#### COMPONENTS:

- 1 terminal controller PCB: CTM-100, 1108.
- 1 power supply PCB: CTM-300-PS, 1109.
- 1 transformer: 230V or 115V primary, 7.5V and 28V secondary.
- 1 rack mountable enclosure: GER-100 FRAME, 5043.

#### VIDEO:

- RS-330 type composite video signal, 1 VPP when terminated by 75 .

### DISPLAY FORMAT:

- 24 x 80 light characters on a dark background
- Non-interlaced raster with a selectable 50 or 60 Hz refresh rate.
- Character cells 7 dots wide by 10 scan lines high.

Circuit Descripting

\$117 CAR COLOR

# CHARACTER SET:

- 96 uppercase and lowercase characters
- Characters are formed in a 5 x 9 dot matrix.

#### SERIAL COMMUNICATIONS INTERFACE:

- 20 mA current loop TTY compatible.
- Switch selected half or full duplex operation.
- -Input and output parity are separately selectable as odd, even, or no parity.
- One or two stop bits, switch selectable.
- 110, 300, 600, 1200, 2400, 4800, 9600, or 19.2K BAUD, switch selectable.

#### KEYBOARD INTERFACE:

- TTL compatible 7 bit paralled ASCII interface.
- Repeat key and Break key inputs.
- Positive going data and keyboard strobe.

# OPERATING MODES:

- Normal Text Mode (No scroll).
- Scroll Mode.
- Auto Line Feed Mode.
- Split Screen Mode.
- Two switch selectable command modes.
- Self Test Mode

#### CURSOR:

- Full character cell inverted video or underscore.
- Positioned by control characters.

# 1.0 SPECIFICATION (Cont'd):

#### SCREEN ERASE:

- All text is erased by  ${\rm OC}_{_{\rm H}}$ 

#### ENCLOSURE DIMENSIONS:

- Height: 3 3/8". Width: 17 in. Depth: 13"
- Mounts in standard 19" EIA RACK

#### POWER REQUIREMENTS:

- 1A @ 115 VAC
- 1.5A @ 220 VAC
- FUSE for

#### CONNECTORS:

- TTY connector Female DB 25
- Keyboard Connector Female DB 25
- Video B.N.C. connector.

#### 2.0 FUNCTIONAL DESCRIPTION:

The GER-100 consists of a 19" rack mountable chasis containing a computer terminal controller card and a power supply. The terminal controller is a firmware controlled microcomputor operating an alphanumeric video controller, a serial interface, and a keyboard interface. The GER-100 provides a three way interface between a host computer, a keyboard, and a video display as shown in figure 2-1.

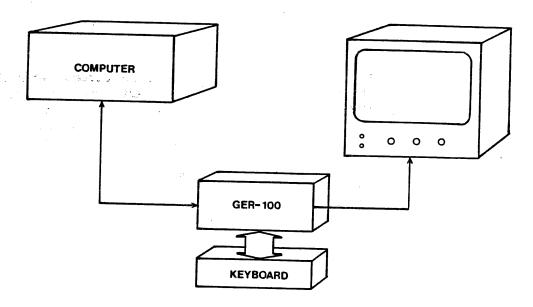


Figure 2.1 - GER-100 IN SYSTEM

#### 2.1 VIDEO INTERFACE:

#### 2.1.1 FORMAT:

The basic text format is 24 character rows by 80 character columns, and the characters, normally light on a dark background, are formed in character cells 7 dots wide by 10 scan lines high (see figure 2.2). The font of 96 uppercase and lowercase characters used, is shown in figure 2.3. The display, which uses a non-interlaced raster, can be switched to use either a 60 or 50 Hz refresh rate, making it compatible with both American and European systems.

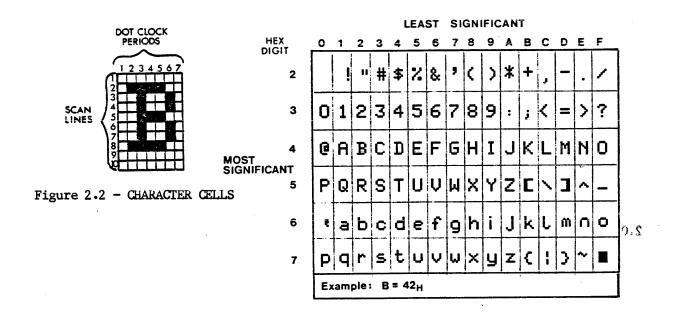


FIGURE 2.3 - CHARACTER FONT

### 2.1.2 TEXT MODES:

The GER-100 has three text modes: Normal, Scroll, and Split Screen. When the Normal Mode is used, the cursor's home position is in the upper left corner of text, and if it is moved down past the bottom line; it wraps around to the top line of text. In the Scroll Mode, the cursor's home position is the lower left corner of text, and when a line feed occurs, the entire text is scrolled up one line leaving the cursor in the new bottom line. The Split Screen mode divides the display into two independent horizontal sections, with the position of the dividing line determined by the user. The cursor will stay in one section or the other until it is moved across the boundary by a vertical tab instruction. Either section can be assigned the Normal Text Mode, or the top can be in the Normal Mode while the bottom is is the Scroll Mode.

#### 2.1.3 EDITING FEATURES:

The GER-100 has a comprehensive set of cursor, erase, and character attribute controls, which facilitate text editing.

The cursor can be selected as block or underscore and can be moved by a set of commands; including Home, Left, Right, Up, and Down instructions, as well as horizontal and Vertical Tab instructions, which move the cursor via XY coordinates. The horizontal coordinate can be given as two ASCII coded numbers or as one B.C.D. byte; the vertical coordinate can be given as two ASCII coded numbers or as a 5 bit binary number. An auto line feed mode can be selected, causing the cursor to automatically go to the next line every time there is a carriage return. Another editing feature allows the host computer to obtain the cursor position via the serial interface.

Erase instructions are provided, allowing the entire text to be erased, a single line of text to be erased, or text from cursor to end of line to be erased.

Portions of text can be assigned as inverse video, resulting in dark characters on a light background.

# 2.2 COMPUTER INTERFACE:

The GER-100 communicates with the host computer via a 20mA current loop serial interface, which can be configured by switches for several modes of operation. Input and output parity are separately selectable as even, odd, or no parity; and the user can choose one or two stop bits. Both full and half duplex operation are possible and the unit can be operated in on line or off line mode. The user can also select the baud rate which can be from 110 baud to 19.2K baud.

# 2.3 KEYBOARD INTERFACE:

Any standard TTL compatible ASCII keyboard using positive logic can be connected to the GER-100. In addition to the parallel ASCII inputs, the unit provides inputs for break and repeat keys as well as a +5V supply to power the keyboard.

#### 2.4 CONTROLS:

The various GER-100 functions are controlled by a series of programming straps and switches on the P.C.B. as well as by control characters originated by the keyboard or host computer.

Straps are used to select 50 Hz or 60 Hz operation and the cursor format (block or underscore). Switches program the serial interface parameters, scroll or normal text mode, auto line feed mode, and the command modes.

The GER-100's character font and response to control characters varies depending on which of two switch selectable command modes (A or B) is used; however, in general control characters control cursor positioning, erase functions, split screen mode, and character attribute assignment.

#### 3.0 OPERATING INSTRUCTIONS:

#### 3.1 SWITCHES AND STRAPS:

Functions which are not normally changed during actual operation are set by a series of switches and straps found on the terminal controller. The switches are in two dual in line packages; SWO and SW1, labelled as A8 and A24 respectively on the P.C. board. The straps are implemented using wire wrap pins numbered 1 through 18.

# 3.1.1 FULL DUPLEX/HALF DUPLEX MODE SWITCHES (4 - SW1):

When switch 4 of SWl is closed, the serial communications interface operates in Full Duplex Mode. Character codes generated by the keyboard are transmitted to the host computer, bypassing the display electronics, and the computer echoes each character back, writing it to the display. When 4-SWl is open, the serial interface operates in Half Duplex Mode, and data entered by the keyboard is sent to both the display and the host computer.

4 - SW1 open = HALF DUPLEX 4 - SW1 closed = FULL DUPLEX

# 3.1.2 SCROLL MODE SWITCH (5 - SW1):

When switch 5 of SW1 is open, the displayed text will scroll up one line if the cursor is in the bottom line and a line feed or cursor down command is received by the display electronics. The top line is lost from view, and a new blank line appears at the bottom. The cursor home position is in the lower left corner of the display.

When switch 5 of SWl is closed, the text is not scrolled, and the cursor reappears in the top line if it is moved down passed the bottom line. The cursor home position is in the upper left corner of the display.

5 - SW1 open = Scroll Mode 5 - SW1 closed = Normal Text Mode

#### 3.1.3 AUTO LINE FEED (1 - SW1):

When switch 1 of SWl is open, a line feed is executed every time there is a carriage return (CR). When 1-SWl is closed, line feeds are not automatically executed when there is a carriage return.

1 - SWl open = Automatic Line Feed
1 - SWl closed = Normal Line Feed

# 3.1.4 BAUD RATE SELECTION (1, 3, 4 - SWO):

Switches 1, 3, and 4 of SWO determine the baud rate used by the serial communications interface. Table 3.1 shows how the switches are set for the various baud rates.

SWITCHES	BAUD RATE						
SWITCHES	110	3 00	600	1200	2400	4800	9600
1 - SW0	0	1	0	1	0	1	0
4 - SW0	0	0	1	1	0	0	1
3 - SW0	0	0	0	0	1	1	1
	0 = S	WITCH CI	OSED	1 =	SWITCH	OPEN	

Table 3.1 - BAUD RATE SELECTION

## 3.1.5 PARITY ON/OFF (7 - SWO):

When switch 7 of SWO is open the serial communications interface adds parity bits to the outgoing data, and checks incoming data for parity. If this switch is closed, parity is ignored.

# 3.1.6 INPUT PARITY ON/OFF (7 - SW1):

When switch 7 of SWl is open and the PARITY ON/OFF switch is open, the GER-100 reacts to parity erors detected by the serial communications interface by ignoring the character with the error. When switch 7 of SWl is closed, parity errors are not detected.

# 3.1.7 EVEN/ODD PARITY (5 - SWO):

When switch 5 of SWO is closed, the serial communications interface uses even parity. When this switch is open, odd parity is used.

# 3.1.8 STOP BITS (6 - SWO):

When switch 6 of SWO is open, two stop bits are used. When this switch is closed, one stop bit is used.

# 3.1.9 BITS/CHARACTER (2, 8 - SWO):

As shown in the following table, switches 2 and 8 of SWO determine the number of bits per character used by the serial interface.

BITS/CHARACTER	5	6	7	8
8 - SW0	CLOSED	OPEN	CLOSED	OPEN
2 - SW0	CLOSED	CLOSED	OPEN	OPEN

# 3.1.10 ON LINE/OFF LINE (2 - SW1):

When switch 2 of SWl is closed, the GER-100 operates off-line. That is to say, the serial communications interface is disabled. When this switch is open, the serial communications interface is functional. Note that the GER-100 must be in off-line mode when the serial interface is not connected.

2 - SW1 closed = OFF LINE

2 - SW1 open = ON LINE

# 3.1.11 COMMAND SET A OR B (6 - SW1):

When switch 6 of SWl is closed Command Set A is functional. When switch 6 of SWl is open Command Set B is functional. Table 3.1 shows the basic differences between the to two command sets. A detailed description of control character commands, describing their use with respect to the command mode, is given in section 3.2.

	COMMAND MODE A	COMMAND MODE B
Character Font	64 Uppercase Characters (Lowercase Converted to Uppercase by Display)	96 Uppercase and Lowercase Characters
Character Attributes	No Character Attributes	Inverse Video
Erase Functions	Screen Erase	Screen Erase Plus Two Line Erase Functions.
Split Screen Mode	No Split Screen Mode	Split Screen Mode
Cursor Address Access	Cursor Address Can Not be Read	Cursor Address Can be Read
Cursor Address Notation	Binary and BCD Line & Column Numbers starting with Ø	ASCII Coded Line and Column Numbers Starting with 1

Table 3.1 - COMMAND MODE A Vs COMMAND MODE B

# 3.1.12 SELF TEST (3-SW1):

When switch 3 of SW1 is open, the GER-100 goes into the normal monitor program at start-up. When switch 3 of SW1 is closed, the GER-100 goes into a special self test program at start-up.

### 3.1.12 SELF TEST (3-SW1) (Cont'd):

The self test has three parts: the memory test, the PCl and display test, and the keyboard and switch test. It first runs the memory test, which takes about 20 seconds. The memory test first writes 00H into every location from 4000H through 477FH then reads each location writing the complement of the data back into the location. When it has done this for every location it increments the data and repeats the entire opeation, continuing until FFH has been written to every location. If there is an error, the alarm line is made active. Note that the data written to memory is automatically displayed.

The self test next runs the PCl and display test, which outputs codes OOF through FFH to the PCl. After each output the CPU does an input from the PCl and displays the data found there. If the serial interface is in full duplex mode or if the loop back connections in figure 3.1 are mode. The data that is output should return through the PCl and be displayed.

DB25	STRAP
23	
17	<b>←</b>
18	-
24	•
25	-
15	•

### LOOP-BACK

Disconnect the host computer from the serial interface and replace it with a male DB-25 connector strapped as shown.

Figure 3.1 - LOOP-BACK CONNECTOR

The third part of the self test is the keyboard and switch test which displays switch values plus the character font. If the user charges a switch position it will be reflected by a change in the display. The keyboard is tested by entering characters from the keyboard. As they are entered they will appear at the bottom of the screen and disappear from the font. The self test loops in this mode until power down.

# 3.1.13 50/60Hz (PINS 6, 12, 18):

When wire wrap pin 12 is strapped to pin 6, the display electronics are programmed to work with European systems (50 Hz). When wire wrap pin 12 is strapped to pin 18, the display electronics are programmed to work with American Systems (60 Hz).

$$6 - 12$$
 IN,  $18 - 12$  OUT =  $50$  Hz  $6 - 12$  OUT,  $18 - 12$  IN =  $60$  hz

# 1.1.14 BLOCK/UNDERSCORE CURSOR (PINS 3, 9, 15):

When wire wrap pin 9 is strapped to pin 3, the cursor covers the entire character cell. When wire wrap pin 9 is strapped to pin 15, the cursor underlines the character cell.

9 - 3 IN, 9 - 15 OUT = Block Cursor 9 - 3 OUT, 9 - 15 IN = Underscore Cursor (as-shipped)

# 3.2.0 USE OF CONTROL CHARACTERS:

Table 3.2 provides a quick reference for control character use; more detailed explanations of the control character functions are found in subsections 3.2.1 through 3.2.13. It must be remembered that there are two command modes (A and B) controlled by switch 6 of SW1 (see sec 3.1.11), and that some of the following commands can not be used in Command Mode A. It should also be noted that the cursor address notation varies with the command mode (see sec 3.2.6).

CTRL CONTROL				APPLICABLE
Control Notation	ASCII Notation	CODE	FUNCTION	COMMAND MODE
CTRL-A	so	Ø1 <sub>H</sub>	Home Cursor	A and B
CTRL-D	EOT	94н	End Inverse Field	B only
CTRL-F	ACK	<b>∮</b> 6н	Move Cursor Right	A and B
CTRL-G	BEL	Ø7 <sub>H</sub>	Enable Alarm	A and B
CTRL-J	LF	ØAH	Move Cursor Down	A and B
CTRL-K	VT	ØВн	Vertical Cursor Position Expects Input	A and B
CTRL-L	FF	ØСН	Erase Entire Screen , Cursor	A and B
CTRL-M	CR	ØDн	Carriage Return	A and B
CTRL-0	SI	ØFH	Output Cursor Address	B only
CTRL-P	DLE	1ØH	Horizontal Cursor Position Expect Input	A and B
CTRL-R	DC 2	12 <sub>H</sub>	Start Inverse Field	B only
CTRL-T	DC 2	14 <sub>H</sub>	Erase Entire Current Line	B only
CTRL-U	NAK	15 <sub>H</sub>	Move Cursor Left	A and B
CTRL-V	SYN	16 <sub>H</sub>	Split Screen Boundary	B only
CTRL-Z	SUB	1A <sub>H</sub>	Move Cursor Up	A and B
CTRL-1	GS	1D <sub>H</sub>	Disable Split Screen	B only
CTRL-^	RS	1E <sub>H</sub>	Erase to End of Line	B only
CTRL- +	٧s	1F <sub>H</sub>	Enable Split Screen	B only

Table 3.2 - CONTROL CHARACTER

#### 3.2.1 HOME CURSOR (CTRL -A):

When the GER-100 receives a CTRL-A character the cursor returns to its home position. Normally this is the upper left corner of text; however, in Scroll Mode it is the lower left corner of text. The Home Cursor command is identical in both command modes (A and B).

# 3.2.2 MOVE CURSOR RIGHT (CTRL -F):

When the GER-100 receives a CTRL-F, the cursor moves one space to the right. This command is the same in both command modes.

#### 3.2.3 MOVE CURSOR LEFT (CTRL -U):

When the GER-100 receives a CTRL-U, the cursor moves one space to the left. This command is the same in both command modes.

# 3.2.4 MOVE CURSOR UP (CTRL -Z):

When the GER-100 receives a CTRL-Z, the cursor moves up one line. If the cursor is in the top line it will wrap around to the bottom except when the GER-100 is in command mode B. In this case the entire text will scroll down when CTRL-Z is entered. In all other respects this command is the same in both command modes.

# 3.2.5 MOVE CURSOR DOWN (CTRL -J):

When the GER-100 receives a CTRL-J, the cursor moves down one line. This command is the same in both command modes.

# 3.2.6 CURSOR CONTROL BY COORDINATES (CTRL -K, CTRL -P):

The cursor can be moved from one position to another via a system of horizontal and vertical coordinates. A CTRL-K followed by a line number will move the cursor to that line. Similarly, a CTRL -P followed by a column number will move the cursor to that column. The form of these coordinates depends on the command mode.

When the GER-100 is in Command Mode A, the text rows are numbered 0 through 23, starting at the top of the display, and the columns are numbered 0 through 79 starting at the left of the display. The character following a CTRL-P is interpreted as a two digit binary coded decimal column number in the range 0 - 79. If the 4 LSBs are outside the BCD range (0 - 9), they are interpreted as zero; the most significant bit of the 4 MSBs is masked, preventing numbers higher that 7 (FH is interpreted as 7H etc). The vertical coordinate, in Command Mode A, is given as a 5 bit binary number formed by the 5 least significant bits of the character following CTRL-K. If the number is greater than 23, only the 4 LSBs are interpreted as the new vertical coordinate. In the special case where the vertical coordinate is 10H, it is also interpeted as CTRL-P and a column number must follow.

### 3.2.6 CURSOR CONTROL BY COORDINATES (CTRL-K, CTRL-P) (Cont'd):

When the GER-100 is in Command Mode B, the text rows are numbered 1 through 24 from the top of the display, and the text columns are numbered 1 through 80 from the left of the display. The horizontal and vertical coordinates are coded in the same way, each taking the form of two ASCII coded digits following CTRL-P or CTRL-K.

For example in Control Mode A the cursor would be moved to row 20 column 70 by entering the following:

In Control Mode B the same cursor position would be achieved by entering the following:

# 3.2.7 CARRIAGE RETURN (CTRL-M):

When the GER-100 receives a CTRL-M the cursor returns to the start of the current line. If the Auto Line Feed Mode is enabled (1-SW1), a line feed is executed as well. This command is the same in both command modes.

### 3.2.8 OUTPUT CURSOR ADDRESS (CTRL-0):

This command is only valid for Command Mode B. When the GER-100 receives a CTRL-O, it outputs the following 5 byte response on the serial interface:

```
Byte 1 - Preamble (OFH)
```

Byte 2 - MSB horizontal address in ASCII (range 0 - 8)

Byte 3 - LSB horizontal address in ASCII (range 0 - 9)

Byte 4 - MSB vertical address in ASCII (range 0 - 2)

Byte 5 - LSB vertical address in ASCII (range 0 - 9)

## 3.2.9 ERASE ENTIRE CURRENT LINE (CTRL-T):

This command is valid only for Command Mode B. When the GER-100 receives a CTRL-T, the line containing the cursor is completely erased.

# 3.2.10 ERASE TO END OF LINE (CTRL-):

This command is valid only for Command Mode B. When the GER-100 receives a CTRL-©, text is erased from the cursor to the end of the line it occupies.

#### 3.2.11 ERASE ENTIRE DISPLAY (CTRL-L):

When the GER-100 receives a CTRL-L, the entire display is erased and the cursor returns to its home position. This command is the same in both control modes.

#### 3.2.12 INVERSE VIDEO (CTRL-R, CTRL-D):

The Inverse Video commands can only be used in Command Mode B. Characters entered following a CTRL-R will have the inverted video character attribute. That is to say, the characters will be dark on a light background. Characters entered after a CTRL-D will have normal video.

# 3.2.13 SPLIT SCREEN MODE (CTRL-<, CTRL-V, CTRL-]):

The Split Screen Mode commands are valid only for Command Mode B. When the GER-100 receives a CTRL-< the display changes to Split Screen Mode: the screen is divided into two independent horizontal sections. If the display is in Normal Text Mode, both the bottom and the top sections will be normal. If, however, the display is in Scroll Mode (see sec. 3.1.2), the top section will be normal and the bottom section will be in Scroll Mode. The cursor stays in one section or the other until it is moved across the boundary by a CTRL-K (see sec 3.2.6).

The boundary between the upper and lower sections of text is set by entering a CTRL-V, followed by two ASCII coded digits which indicate the position of the top line of the bottom section (lines are numbered from 1 to 24 starting at the top of the display). Once this parameter has been set, it stays valid until changed by another CTRL-V command.

When the GER-100 receives a CTRL-] the Split Screen Mode is terminated.

#### 3.2.14 ALARM (CTRL-G):

When the GER-100 receives a CTRL-G, the alarm line produces a 400mS, +5V pulse which drives a 100mA Sonalert mounted on the back of the chasis. This command is the same for both command modes.

#### 4.0 INITIAL CHECKOUT:

This section provides a step by step procedure that can be followed to start up the GER-100 and familiarize the user with its various functions. The GER-100 is thoroughly tested at the factory and should work if this procedure is followed correctly; however, if there is a problem and the user is certain that all switches and connections are correct, he can refer to the trouble shooting guide in section 6.0.

- 1. Visually inspect the unit for any shipping damage.
- 2. Remove the top cover (6 screws) and set the two DIP programming switches as indicated in table 4.1. Note that SWO = A8 and SW1 = A24.

# 4.0 INITIAL CHECKOUT (Cont'd):

SWITCH	STATE	FUNCTION
1 - SWØ	*	BAUD RATE Ø (See sec 3.1.4)
2 - SWØ	OPEN	BITS PER CHARACTER 1
3 - SWØ	*	BAUD RATE 2 (See sec 3.1.4)
4 - SWØ	*	BAUD RATE 1 (See sec 3.1.4)
5 - SWØ	*	ODD/EVEN PARITY (See sec 3.1.7)
6 - SWØ	*	1 or 2 STOP BITS (See sec 3.1.8)
7 – SWØ	*	PARITY OR NO PARITY (See sec 3.1.5)
8 - SWØ	OPEN	BITS PER CHARACTER Ø
1 - SW1	OPEN	AUTO LINE FEED
2 - SW1	CLOSED	OFF LINE
3 - SW1	OPEN	NORMAL MONITOR
4 - SW1	OPEN	HALF DUPLEX
5 - SW1	OPEN	SCROLL MODE
6 - SW1	OPEN	COMMAND MODE B
7 - SW1	*	INPUT PARITY ON/OFF (See sec 3.1.6)
8 - SW1	DON'T CARE	

<sup>\*</sup> These switches control the serial interface, and their state depends on the conventions used by the serial interface of the host computer. For example, if the host computer uses even parity, 5 - SWØ must be closed. Refer to the sections indicated.

Table 4.1 - FIRST SWITCH CONFIGURATION FOR INITIAL CHECK-OUT

- 3. The board is strapped to be used with an American monitor (60Hz). If a European monitor (50Hz) is used, the strap between wire wrap pins 18 and 12 must be removed and wire wrap pin 12 must be strapped to wire wrap pin 6.
- 4. Connect the keyboard and the 20mA current loop serial interface. The GER-100's end of the 20mA current loop is passive and the current must be supplied by the host computer. An RS232C serial interface can be used in place of the current loop if the strap from wire wrap pin 23 is moved from pin 2 to pin 27 (see sec 7.0 for connections).

### 4.0 INITIAL CHECKOUT (Cont'd):

- 5. Connect a video monitor to the GER-100 via the BNC connector provided on the board. Note that direct drive monitors will not work.
- 6. Apply power. The GER-100 should now be operating in off line mode. That is to say, the serial communications interface is disabled and the keyboard is accessing the display directly. The display should be blank except for a flashing cursor in the lower left of the screen.
- 7. Enter some characters via the keyboard, checking that they are displayed correctly and that the cursor moves.
- 8. Press Carriage Return and check that the text scrolls up one line while the cursor moves to the left of the bottom line.
- 9. Try the control character commands described in section 3.2. They should all work except for Output Cursor Address which will only work in On-Line Mode.
- 10. Change to On-Line Mode by changing 2-SW1 to open, and if the host computer's serial interface is full duplex go to full duplex operation by changing 4-SW1 to closed.
- 11. Check that the serial interface is working correctly. If full duplex operation is being used, the appearance of typed characters on the display indicates that the host computer is receiving characters and echoing them back to the display. If half duplex operation is being used, the host computer will have to be programmed to write something on the display in response to data from the GER-100.
- 12. Change 5-SW1 to closed and check that the board operates correctly in normal Text Mode.
- 13. Have the host computer obtain the cursor address by using the CTRL-O command. As is, it will be given as ASCII coded digits with the horizontal position first (see sec 3.2.8).
- 14. Go to Command Mode A by closing switch 6 of SWl and check that the cursor addressing is as described in section 3.2.6.
- 15. Power down, disconnect the host computer from the serial interface and replace it with a male DB-25 connector wired as shown in figure 3.1. Close 3-SW1 and power up. The GER-100 should enter the self test mode. Referring to section 3.1.12 run through the self test.
- 16. Most of the boards functions have now been checked.

#### 5.0 CIRCUIT DESCRIPTION:

The GER-100's terminal controller PCB, the CTM-100, is basically a firmware programmed microcomputer containing a programmable serial interface and a programmable video controller. When power comes up, the firmware program initializes the serial interface and video controller, then directs their operation in accordance with on-board programming switches and straps, as well as control characters from the keyboard and host computer. The CPU writes text from the keyboard and host computer to a block of RAM which is continually being scanned and displayed by the video controller. This RAM plus another smaller block, used for the C.P.U.'s stack, is referred to as the Text Memory.

The CTM-100 is actually one specific configuration of a circuit designed to emulate different terminals by changing firmware, straps, and optional I.C.'s. For this reason some of the circuitry may seem more complicated than is necessary and optional circuits not used in the CTM-100 configuration may be found in the schematics.

Schematics are included at the back of this manual. These and the block diagram in figure 5.1 should be referred to while reading the rest of this section.

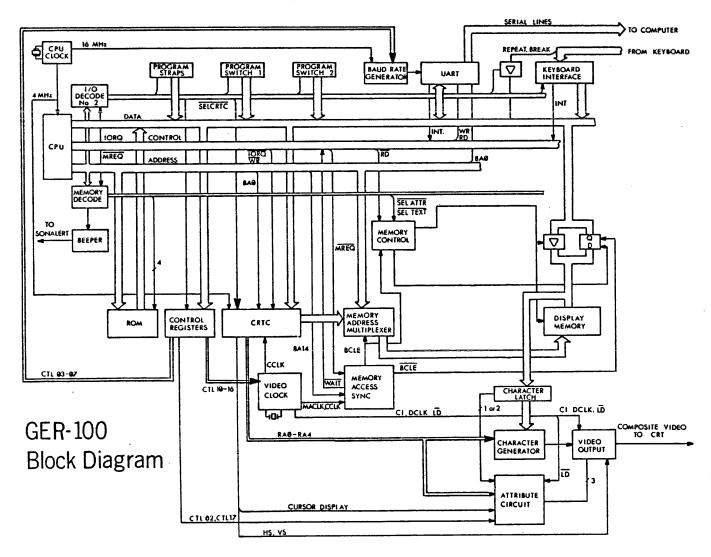


Figure 5.1 - BLOCK DIAGRAM OF GET-100

#### 5.1 ARCHITECTURE:

The CTM-100 uses a fairly orthodox architecture, with data moving between the CPU and its supporting circuits via a common data bus. The four most significant memory addresses are decoded in A4, which provides enabling signals for the various sections of ROM and RAM, and the alarm. All other constituent units are accessed by programmed I/O, with A3 decoding the I/O addresses.

The text memory, containing the displayed information plus the C.P.J.'s stack, can be accessed by both the CPU and the video controller, which is constantly refreshing the display. An arbitration circuit, described in section 5.6, assures that there are no memory contention problems.

# 5.2 PROGRAMMING SWITCHES AND STRAPS:

The board contains one set of wire wrap pin implemented programming straps (PINS 1-18) and two sets of DIP programming switched (SWO and SWI). The logical state of these straps and switches is read by the C.P.U. to determine part of the firmware program's operation. Only two of the 5 bits controlled by the programming straps, are used by the CTM-100 firmware: the remaining three are reserved for other configurations. The specific function of each strap and switch is given in section 3.1.

#### 5.3 KEYBOARD INTERFACE:

The keyboard interface consists of A71, A67 and part of A7. Parallel ASCII data is latched into A71 by the keyboard strobe, which also initiates an interrupt to the CPU by way of A69 and A34-6. The CPU uses a method described in the next subsection to determine that it is the keyboard that is interrupting, then inputs the data from that location. The keyboard's Repeat and Break key has a separate input, and it status is read at the same I/O location as the programming straps.

# 5.4 SERIAL INTERFACE:

The serial interface has two main parts: a programmable baud rate generator and a 8251A programmable communications interface (PCI). The baud rate generator is composed of A36, A66, and A67; and is programmed by CTL03 through CTL07 from Control Register Zero (A70). It uses 16 MHz from the system clock (A18) and provides the P.C.I. with 0, Txc, and Rxc. Once initialized, the P.C.I. (A69) converts parallel data from the CPU into serial data for the serial line and vice versa, adding and decoding the appropriate stop and parity bits. When it receives a character on the serial line, it interrupts the CPU via A34-6. The CPU then reads the PCI's status word to determine whether the interrupt comes from the PCI of the keyboard interface. It can do this because the keyboard strobe is fed into the status word via the PCI's DSR input. The status word also allows the CPU to discriminate between interrupts caused by errors and interrupts caused by valid data. Data sheets on the 8251A are found in section 8.

An optical interface (A83 and A84) is used to connect the PCI with the passive end of a 20mA current loop. An examination of the schematic will show that an RS232 line can be used instead of the current loop if the appropriate strap (47) is changed.

#### 5.5 VIDEO CONTROLLER:

The video controller is the largest of the CPU controlled sub units that make up the CTM-100. It is composed of an independent programmable clock, a programmable Cathode Ray tube controller I.C. (CRTC), a character generator, and a character attribute circuit.

#### 5.5.1 VIDEO CLOCK:

The video controller section has its own programmable clock designed to produce a variety of dot clock and character clock frequencies. The CTM-100 only uses one set of these frequencies; however, the programmable circuit is required so that firmware can establish the different formats that other versions of the basic emulator board may require. Figure 5.3 shows the video clock timing.

The video clock is composed of a crystal oscillator (A56) and three programmable dividers (A73, A74, and A75), arranged as shown in figure 5.2.

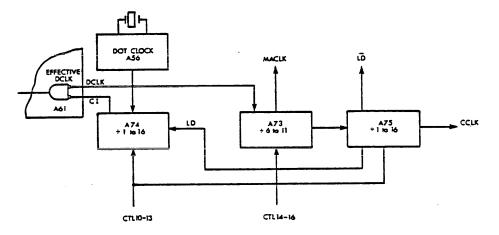
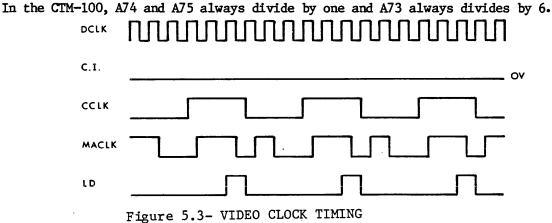


Figure 5.2 - VIDEO CLOCK

A clock inhibit signal (CI) is produced in A74 by dividing DCLK: the divide ratio is set by CTL10-13. This signal is used to inhibit the dot clk in the serial shift register (A61), producing a programmed effective dot clock frequency. A73 divides DCLK by a divider from 6 to 11, depending on CTL14-16, and A75 divides the resulting signal by the same ratio used in A74, to produce a character clock (CCLK) that is a submultiple of the effective dot clock frequency. It is A73 that sets the number of dots per character cell, and A73also produces the MACLK signal which is used in the memory contention circuit (see sec. 5.6). The load signal (LD/) generated by A75 synchronizes CI with CCLK, as well as performing synchonization functions in the video output section.



## 5.5.2 CRTC:

The most important I.C. in the video section is the programmable cathode ray tube controller (CRTC), because it is in this chip that the format is programmed. The CRTC (A39) refreshes the display, provides vertical and horizontal sync pulses at the proper times, and controlles the scroll and cursor functions. Data sheets on the CRTC are found in section 8; it should be kept in mind however that not all of the CRTC's possible functions are used by the CTM-100.

#### 5.5.3 CHARACTER GENERATION:

In order to refresh the display, the CRTC is continually scanning the Text Memory, addresing 8 bit character codes (7 bit ASCII code plus one attribute bit). When one of these codes is addressed, LD/ latches it into A62 where the first 7 bits are used to address a 16 byte block of video information in the character generator ROM (A60). The first 10 bytes of this block represent 10 horizontal sections of the character cell and they are individually addressed by RAO through RA3 from the CRTC, then loaded into the video shift register (A61) by LD. Once loaded they are shifted out to the video output section by the combination of DCLK and CI (effective dot clock).

The schematic shows RAO through RA3 going to A58 rather than A62. A60 is an optional I.C. used to produce multiple height characters in other versions of the basic emulator board. It is not installed in the CTM-100 and RAO through RA3 are strapped across the empty socket making connections with AO through A3 of A62 respectively.

#### 5.5.4 CHARACTER ATTRIBUTE GENERATION:

Although the emulator board provides for several character attributes, only inverse video is used by the CTM-100 version. It is enabled by bit 7 of the character code and implemented in the exclusive OR gate A64-8. A51 is used to synchronize attribute enable with the video information. Note that the inverted video circuit is also used to change the cursor signal from the CRTC into video information.

#### 5.5.5 VIDEO OUTPUT:

The video output section consists of a mixing circuit and a transistor driver for the composite video signal. Horizontal and vertical sync from the CRTC is mixed with TTL video from A89 then made available at a BNC connector. As can be seen on the schematic other signals are provided as well, but these are not used by the CTM-100.

#### 5.6 RAM CONTROL:

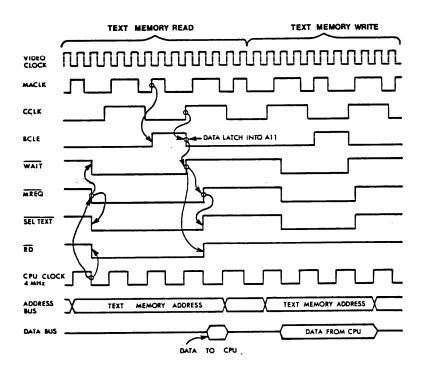
Before considering RAM control, it should be noted that not all of the RAM shown on the schematic is present in the CTM-100. The optional Attribute Memory (A28 and A29) and A30 of the Text Memory are not installed.

As previously mentioned, both the CPU and the CRTC can address the Text Memory. The CPU, which can both read and write RAM, does so to change text or to manipulate its stack. The CRTC can only read RAM, which it does to refresh the display. Memory access is organized so that there are no contention problems that would cause errors or display streaking.

### 5.6 RAM CONTROL (Cont'd):

Since display refresh is an on-going process, it takes precedence over CPU accesses, which are less frequent; and the three multiplexers, A25, A40, and A41, normally connect the RAM address lines to the CRTC. The CRTC accesses RAM only when CCLK is high, at which time the display data is placed in latch A62. Because this latch masks the character generator from RAM, the CPU can have RAM access whenever CCLK is low, without interfering with the display. The signal which gives RAM access to the CPU is BCLE, and it is produced by the two flip flops in A57 on the first rising edge of MACLK (A57-11) after MREQ is active, CCLK is low, and BA14 is high. If all of these conditions are not present when MREQ is generated, the CPU's wait line is pulled low until they are present. BCLE switches the RAM address multiplexers to the CPU and enables the control lines, RD and SELTEXT, that give the CPU data bus access to the RAM data. When the access is a memory read the trailing edge of BCLE latches the data from RAM onto the CPU data bus via A11.

Figure 5.4 shows the timing for typical read and write accesses of the text memory by the CPU. Note that the CPU's WR line is not used to control text memory: the fact that RD remains high during a memory write is used to gate data from the CPU to the RAM and to pull down the RAM W lines. It must be remembered that the CPU clock and the video clock are not synchronized and MREQ can fall anywhere with respect to CCLK.



NOTE: VIDEO CLOCK AND CPU CLOCK ARE NOT SYNCHRONIZED; THEIR RELATIONSHIP ABOVE IS ARBITRARY.

Figure 5.4 - TYPICAL TEXT MEMORY READ AND WRITE ACCESS BY CPU

# 6.0 TROUBLE SHOOTING:

Before attempting to trouble shoot this board, the circuit descripion in section 5 should be studied. The information contained therein plus the schematics at the back of this manual should be sufficient: however, a short list of possible problems along with their probable causes is provided in this section as supplementary trouble shooting information.

- 1. Problem: The display has no synchronization and is not stable. Some possible causes.
  - a) The CPU is not being reset at power-up.
  - b) The CPU clock is malfunctioning.
  - c) The CPU is not able to access the firmware.
  - d) The CPU is not able to initialize the CRTC.
  - e) The 50/60Hz strap is incorrect.
  - f) The video clock is malfunctioning.
  - g) V SYNC, H SYNC, DISPEN, or CCLK are missing or distorted.
- 2. Problem: The display can not be accessed at all.
  - a) The RAM is not being accessed.
  - b) The character generator is not being accessed.
  - c) The TTL video is missing.
- 3. Problem: The display can not be accessed from the keyboard.
  - a) The keyboard interface is malfunctioning.
- 4. Problem: The display can not be accessed from the host computer.
  - a) The serial interface is malfunctioning.
  - b) The programming switches controlling the serial interface are not set in a manner compatible with the serial interface format used by the host computer.
  - c) The break signal is being held low.
- 5. Problem: The characters in the display are not correct.
  - a) The character generator is malfunctioning.
  - b) The shift register A63 is bad.
  - c) The half/full duplex switch is incorrect.
  - d) DCLK or LD are incorrect.

#### 7.0 CONNECTORS:

#### 7.1 KEYBOARD CONNECTOR:

The GER-100 is connected to a keyboard via a female DB-25 connector mounted on the back of the chassis. Table 7-1 shows this connector's pin assignment and the corresponding pins on the PCB connector (J8) to which it is connected internally.

# 7.1 KEYBOARD CONNECTOR(Cont'd):

KEYBOARD CONNECTOR	J8 PCB	SIGNAL	KEYBOARD CONNECTOR	J8 PCB	SIGNAL
1	22	+5V	14	1	GND
2	24	+5∀	15	3	GND
3	16	KSTB	16	5	GND
4	2	B1KB	17	7	GND
5	4	B2KB	18	9	GND
6	6	в3кв	19	11	GND
7	8	B4KB	20	13	GND
8	10	в5кв	21	15	GND
9	12	в6КВ	22	17	GND
10	14	в7кв	23	19	GND
11	20	BREKEY	24	21	GND
12	-	N.C.	25	23	GND
13	-	N.C.			

TABLE 7-1 KEYBOARD CONNECTOR PIN ASSIGNMENT

# 7.2 TTY CONNECTOR:

The GER-100 is connected to a current loop serial interface via a female DB-25 connector mounted on the back of the chassis. Table 7-2 shows this connector's pin out plus the corresponding pin out of the PCB connector (J1) to which it is connected internally.

TTY CONNECTOR	J1 PCB	SIGNAL	TTY CONNECTOR	J1 PCB	SIGNAL
1	1	GND	14	N.C.	GND
2	-	N.C.	15	-	GND
3	-	N.C.	16	-	
4	_	N.C.	17	17	LIN+
5	-	N.C.	18	18	LIN-
6	-	N.C.	19	-	
7	7	GND	20	-	
8	-	N.C.	21		
9	-	N.C.	22	22	LBIAS
10	_	N.C.	23	-	N.C.
11	-	N.C.	24	24	LOUT+
12	-	N.C.	25	25	LOUT-
13	_	N.C.			

TABLE 7-2 SERIAL INTERFACE CONNECTOR

# 7.3 POWER SUPPLY CONNECTOR:

The terminal controller PCB is connected to the powersupply PCB by a 7 PIN header mounted on the controller PCP. The pin assignment is as shown in table 7-3.

PIN	CONNECTION
1	GND
2	+5V
3	+12V
4	GND
5	+5V
6	-12V
7	GND

TABLE 7-3 POWER CONNECTOR PIN OUT

# 7.4 VIDEO CONNECTOR:

A composite video signal for a CRT terminal is provided at a female BNC connector mounted on the back of the chassis.

# 8.0 DATA SHEETS:

Data sheets for the Hitachi HD 465055 CRTC are not available at this time. In their place we have included data sheets for a similar unit, the HD 46505R. These data sheets are preceded by a short explanation of the differences between the two I.C.'s

# 9.0 MAINTENANCE AND WARRANTY:

Matrox products are warranted against defects in materials and workmanship for a period of 180 days from date of delivery. We will repair or replace products which prove to be defective during the warranty period, provided they are returned to Matrox Electronic Systems Limited. No other warranty is expressed or implied. We are not liable for consequential damages.

# 10.0 ORDERING INFORMATION:

The GER-100 can be ordered directly from Matrox Electronic Systems Limisted or from its worldwide network of distributors.

# APPENDIX A, PARTS LIST:

COMPONENT	DESCRIPTION TRUNCATED	ENGINEERING . ORAWING NUMBER	QUANTITY PEP
#41 LITCK TWAISHERT	WASHER		
#4 NYLON WASHER	SEE HEADING		15.000
45 LOCK WASHER	WASHER		2.000
#5 TERMINAL EUG	16-14 WIRE TERMINAU LUG		9.003
CTM-100 AS	PCR ASSEMBLY FOR GER-100		1.000
ICT-406-5-T	DIP SOCKET 40 PIN		1.000
TMS2516	2K X 8 EPROM +5V 45UNS	99	2.500
09-74-1071	7 PIN HEADER #2373	<u>.</u>	1.000
1108-005-02	CTM-300 PC3 SUBASSEMBLY	1109-41-025	1.000
HJ4650559-1	CRT. CONTROLLER TO TOTAL	— "G"	1.000
ICT-246-S-T	2+ PIN SOCKET		1.000
J-309	FET TRANSISTOR	PP	1.000
?-90A	CPU	pp	1.305
0.C1UF	CERAMIC CAP 3439-050E-1	PP	3.600
(.1UF	C/C W/0.2 LS 3439-0508-1	çe	28.000
C.220F	CERAMIC CAP	वद	1.003
1.9K 0HM	PESISTOR	99	1.000
1k 3HM	PESISTOR	90	4•000
11,4148	SWITCHING DIODE 10M4	рр	3.005
15K OHM	RESISTOR	Þέ	1.000
1.jPF	CEPAMIC CAP 2222-638-10	99	1.000
100THMT TO T	RESISTOR	- q <del>a</del>	1.535
LUCK CHM	RESISTOR	ομ	1.000
19085	CERAMIC CAR 2222-639-53	99	3.300
same 🙀 s	• • • • • • • • • • • • • • • • • • •		

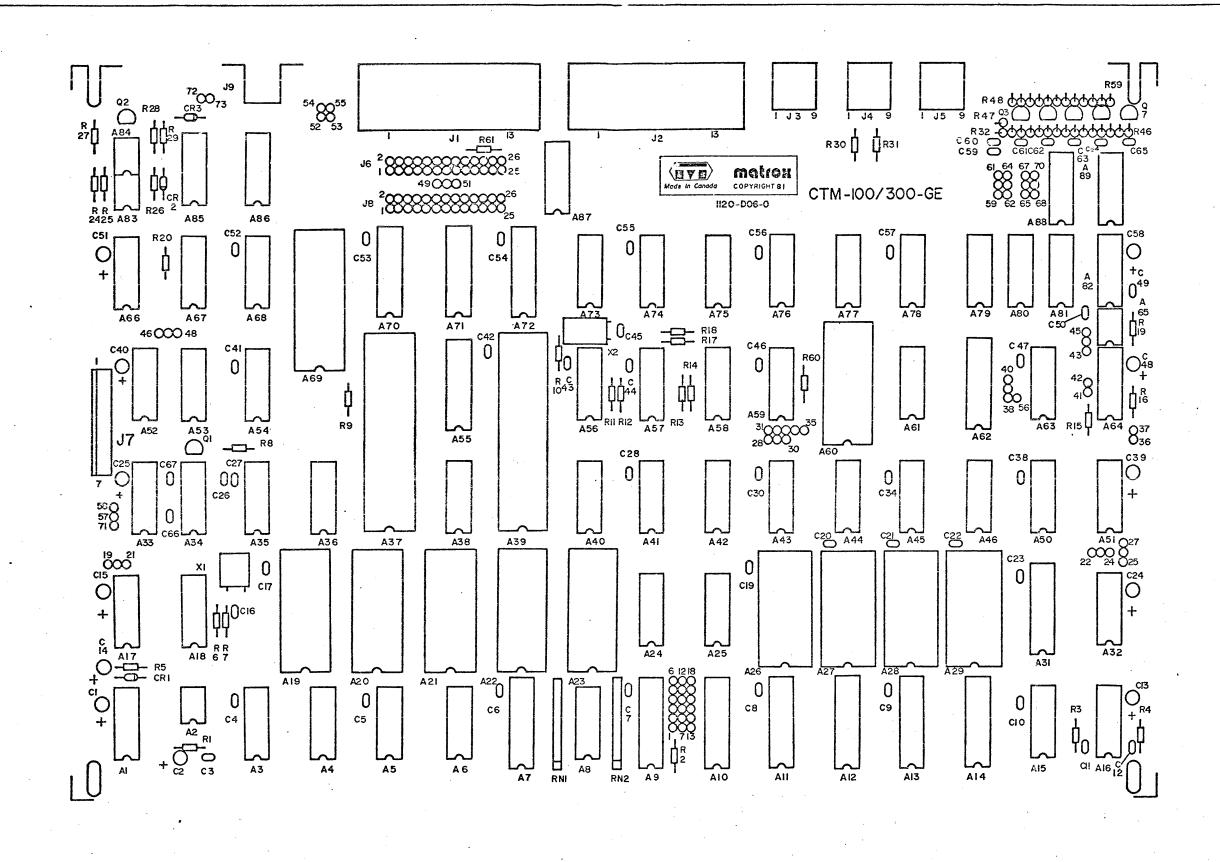
COMPONENT ITEM NO.	DESCRIPTION TRUNCATED	ENGINFERING . DRAWING NUMBER	QUANTITY PER
11.6566MHZ	X*TAL	- · · · · · · · · · · · · · · · · · · ·	1.600
1108-075-1	CTM+100/300 PCP LEVEL-1		1.000
12K OHM	RESISTOR	DР	1.000
15-25-1245	24 PIN SOCKET #340KT		
15-25-1285	25 PIN DIP SMCKET		1.000
15-25-1405	40 PIN DIP SOCKET		2.000
150PF	T CERAMIC CAP 2222-369-70	у	T.000
13.000MHZ	X. TAL	PΡ	1.076
19K OHW	RESISTOR		1.000
19978hM	TRESISTOR TO THE TOTAL		onc.T
2.2K OHM	RESISTOR	qc	7.000
2.295	CERAMIC CAP		1.603
2.7K 04M	RESISTOR		1.000
2 43904	NEW TRANSISTOR	Ģe	3.000
206584-1	25 PIN D TYPE RS-232 FEV	•	1.000
22UF T15V/12	DIP TANTALUM CAP W/C+Z L		11.000
2 <u>20 0</u> 8M	RESISTOR	<b>و</b> ٥	3.000
3505E	CERAMIC CAP 2222-630-03	) PP	1.305
27 TH: Y	RESISTOR TO THE TOTAL TO THE		<b>2.</b> 303
35 JHM	RESISTOR	ор	1.090
390K 084	RESISTOR		1.000
4.7K CHM	RESISTOR	<u> </u>	<b>5.</b> 000
4 ,25	OPTG COUPLER		2.000
43109-101-22?	10 SIP+ 9 X 2.2K RES-NE	PP	2.•∪∂∪
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COMPONEME ITEM NO•	DESCRIPTION TRUNCATED	ENGINEERING DRAWING NUMBER	O E P O LITY
470 DHM 1	RESISTOR	po	3.000
5.6K CHM	RESISTOR	الم ق	1.070
531220-1	TANDEM SPRING SHUNT		30 <b>.</b> 000
555	TIMER		27000
4.0P=	CERAMIC CAP 2222-638-09		1.000
65500-436	36 PIN WHW TERMINAL	φş	4.303
SSPF " " "	CERAMIC CAP "2222-638-40	٩٠	נמנ•ו
7+LS00	QUAD 2 INPUT NAND GATE		1.000
74LS02	DUAD 2 INPUT NOR GATE	ço	2.010
74US04	HEXTINVERTER		5.000
7-LS00	QUAD 2 INPUT AMD GATE	99	3.000
7+LS138	1 OF a DECIDER/DEMULTIPL	ρp	2.000
7-LSI37	104L 1 0F 4 NECOMER		1.000
7+L3163	RIMARY SYNCHRONOUS 4 BIT	٩٥	4.303
74L\$166	BBIT SHIFT REGISTER		1.600
74L3174	HEX TO FLTP FLOPT	797	2.000
7+LS20	DUAL 4 INPUT NAND GATE	op	1.000
7+LS21	DUAL 4 INPUT POSITIVE AN	çe	1.000
7+L5244	"OCTAL" PUFFER/LINE "DRIVER	- da	4.000
7-LS245	OCTAL BUS TRANSCRIVER		1.090
74LS273	OCTAL D TYPE FLIP FLOP	PP	3.000
7+L532***	10040 2 INPUT JR SATE	. د ه	77.000
7+L\$3+7	HEX RUS DRIVER	92	5.000
7465374	OCTAL O TYPE FLIP FLOP	s p	2.000

CUMPONENT ITEM NO.	DESCRIPTION TRUNCATED	ENGINEERING DRAWING NUMPER	PÉR PÉR
7-L5393	DUAL + SIT COUNTER	- حو	Z.000
7+L3399	OUAD 2 INPUT MULTIPLEXER	٩٩	1.000
7+L\$74	DUAL D TYPE +EDGE TRIGGE	ρp	4.000
74LS35	OUTD 2 INPUT EXCLUSIVE O	देव	1.003
7+500	STAD CRAN TURNI S CAUS		1.000
74574	DUAL D TYPE FLIP FLUP		1.000
7+157	TOUAD 2 INPUT MULTIPLEXER		<b>3.</b> 300
73 OHM	PESISTOR	55	1.000
2251 <u>0</u>	USART		1.000
31-010	SINC REMALE	64	1.000
3 DIO SWITCH	DIP SWITCH 3 ROCKERS		2.000
FIT 105 1/4 RK	HEAT SHRINK TURING		•C83
FIT 105 178 8K	HEAT SHRINK TUBING		•333
4T4 00	LITTLE FUSE HOLDER	PP	1.000
KT47	LUGS		3.010
LT-350	CABLE TIE 4 INCHES		17.000
LTA-100-TK3	SPST POWER SWITCH W/LIGH	ÇQ	1.000
45-8AR	SUCKET BAR FOR MODULES		•140
₽,.= <u>Z</u>	RRACKET FOR SONALERT BEE		C000-I
SAP-2	MALLORY SOMALERT BEEPER		1.000
05-50-0105	CRIMP TERM. #2478	FOR 09-50-3121	21.000
09-50-3071	7 SKTS HOUS'S #2139**	TREF 03500164 PP T	
1A FUSE-Fo	LITTLE FUSE FAST-9L0		1.000
1109-005	CTM-300 POWER SUPPLY ASS	1109-41-09	1.300

CUMPONENT Item no.	DESCRIPTION TRUNCATED	ENGINEERING DRAWING NUMPER	OBC DEC
15-25-4254	26 PIN HEADER #4730		1:000
17233	RELOEN LINE CORD 8*		1.000
20 GA WIRE-B	WIRE 20 GA COLOR-BLUE		•20s
SO GALMISE-BRU	HIRE ZO GA COLOR-BUACKT		• 525
20 GA VIRE-O	WIRE 20 GA COLOR-OPANGE		•203
20 GA WIRE-R	WIRE 20 GA COLOR-RED		• + 1 7
22 GATWIRE-BKT	WIRE 22 GA COUDR-BUACK		Z•5#3
22 GA WIRE-R	WIRE 22 GA COLOR-RED		2.533
31-010	RNC FEMALE	qq	1.50
3+3	SHPULDER WASHED		1.075
4/46 NUT	HEX NUT		5.000
4/40X1/2 PHMS	PAN HEAD MACHINE SCREW		5.000
4/40x3/3 FHMS	FUNT THEAD MACHINE SCREW		1.005
2MH4 8/6XC4/4	PAN HEAD MACHINE SCREW		9.000
4/45X7/15JS	JACKSCREW FOR DB-25 CONN		4.000
504 <del>2-0</del> 03177	REF WIRING DIAGRAM		1.000
5043-005	GER-100 FRAME		1.000
5045-005	GER-100 COVER		1.000
5046-005	GER-100 TRANSFORMER		
6/32 NUT	HEX MUT		2.000
62	STRAIN RELIEF		1.000
601	JUMPER		1.000
509-258	25 PIN FLAT CAPLS MOUNT	9p	1.305
64-21-023-212	MICA INSULATOR		1.603
<b>Marketin</b>	/ · · · · · · · · · · · · · · · · · · ·	Company of the control of the contro	Contract to a second district to the comment

CUMPORFUT ITEM NO.	DESCRIPTION TRUNCATED	ENGINEERING Drawing number	OUANTITY PER
69924 TT	TERMINAL BLOCK	· · · · · · · · · · · · · · · · · · ·	1.000
34-28-5726	26 CKTS F/CAPLE		• 3 3 3

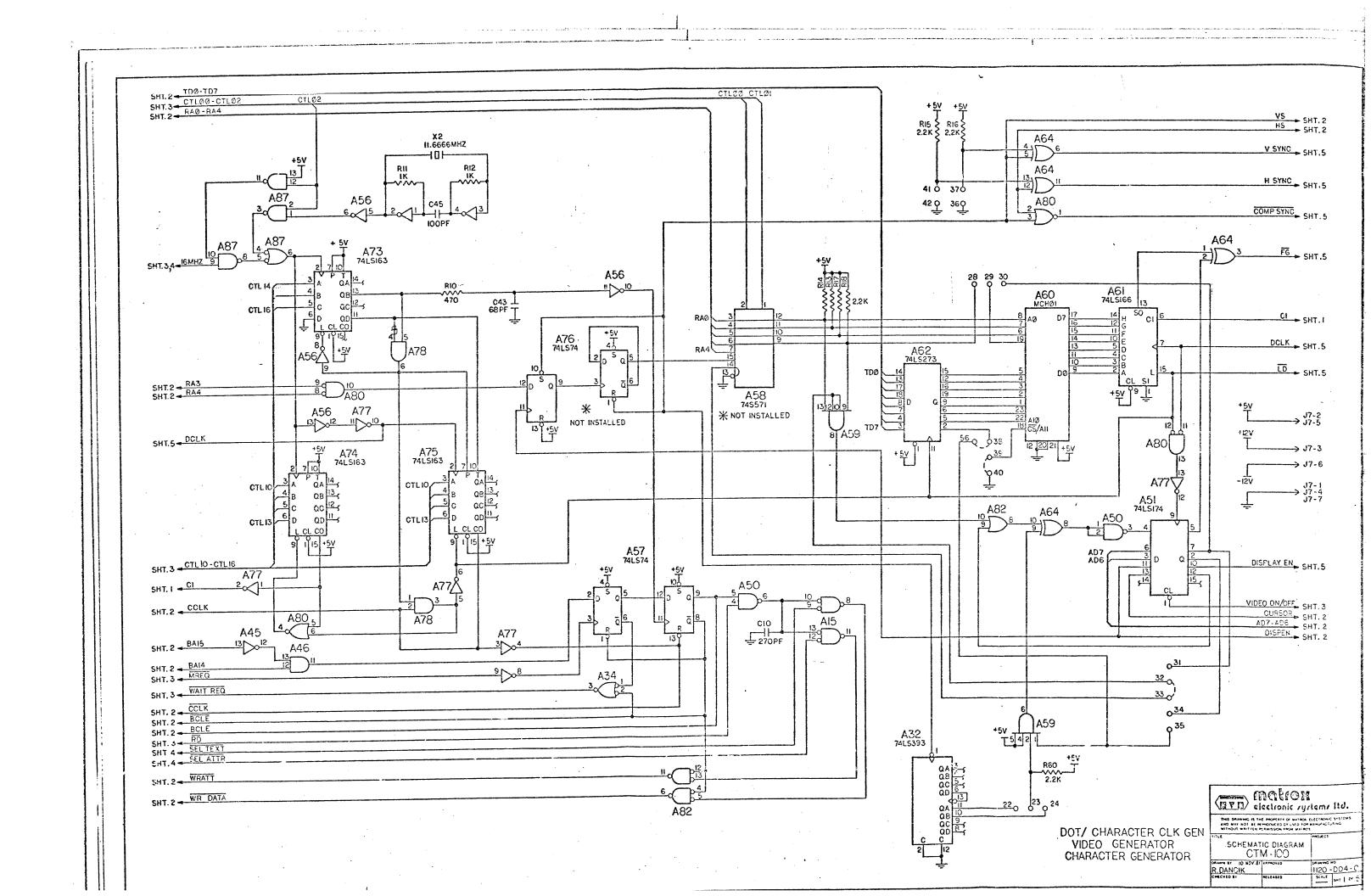


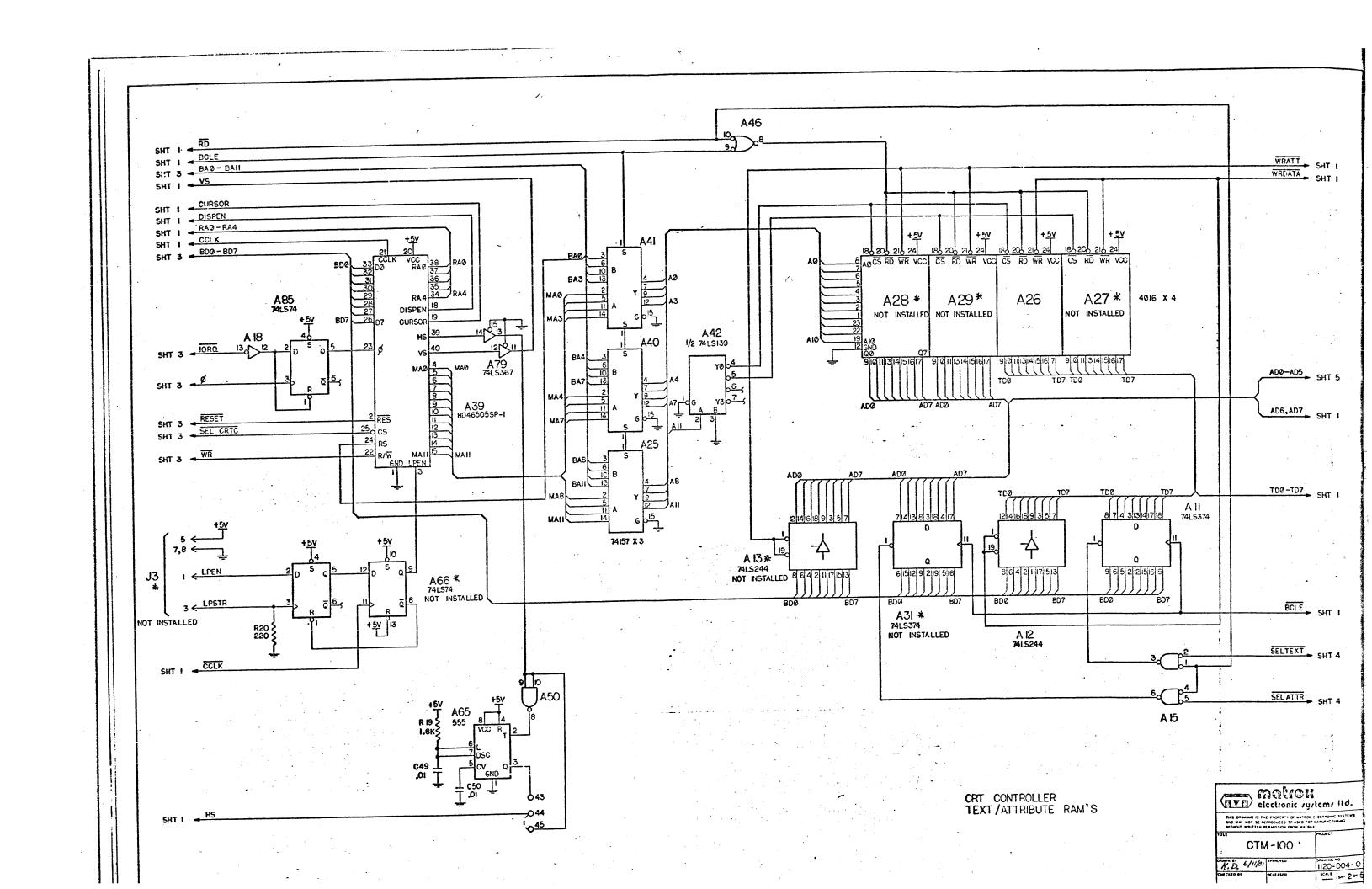
THE CTM-100 / 300-GE

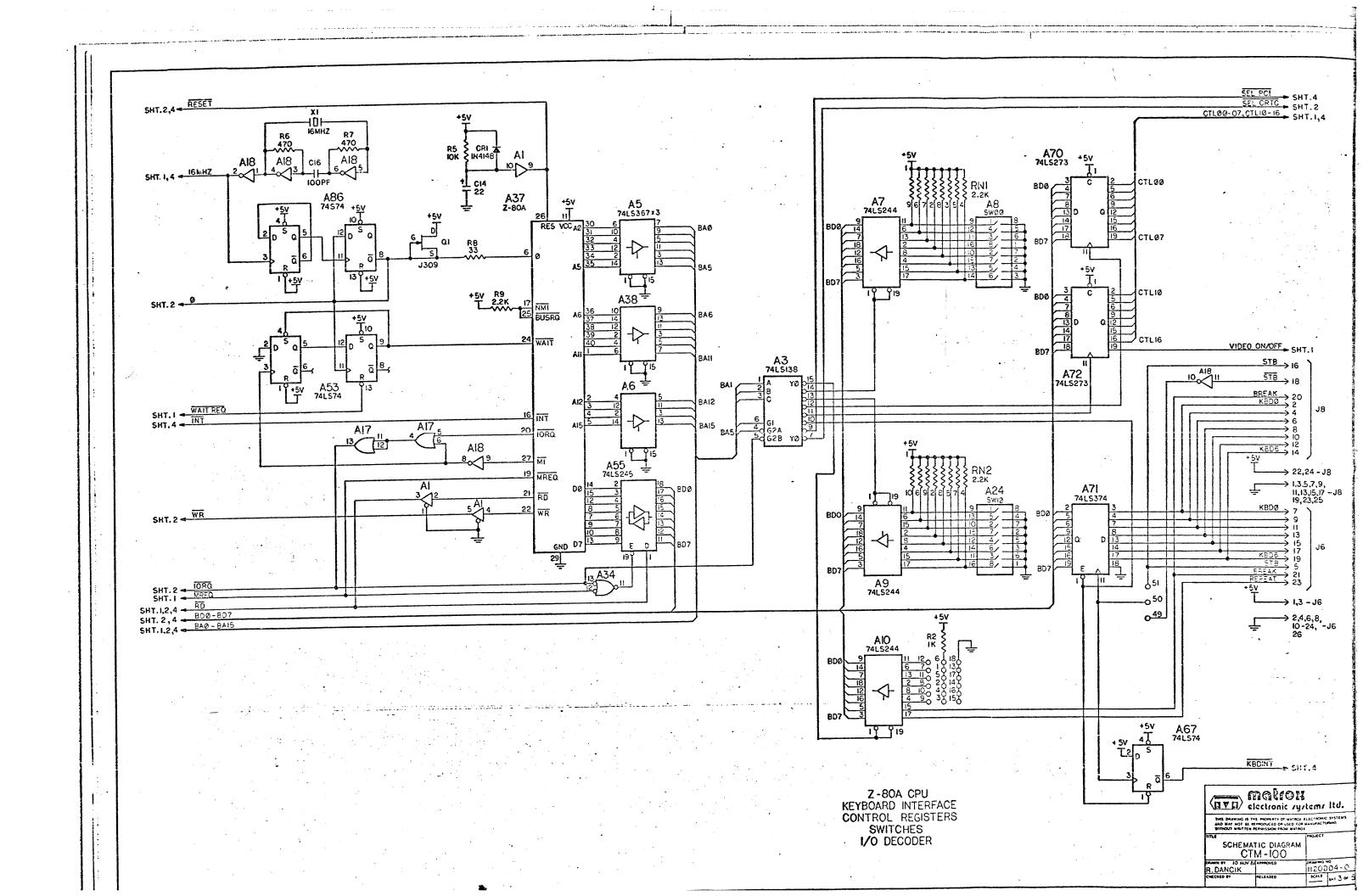
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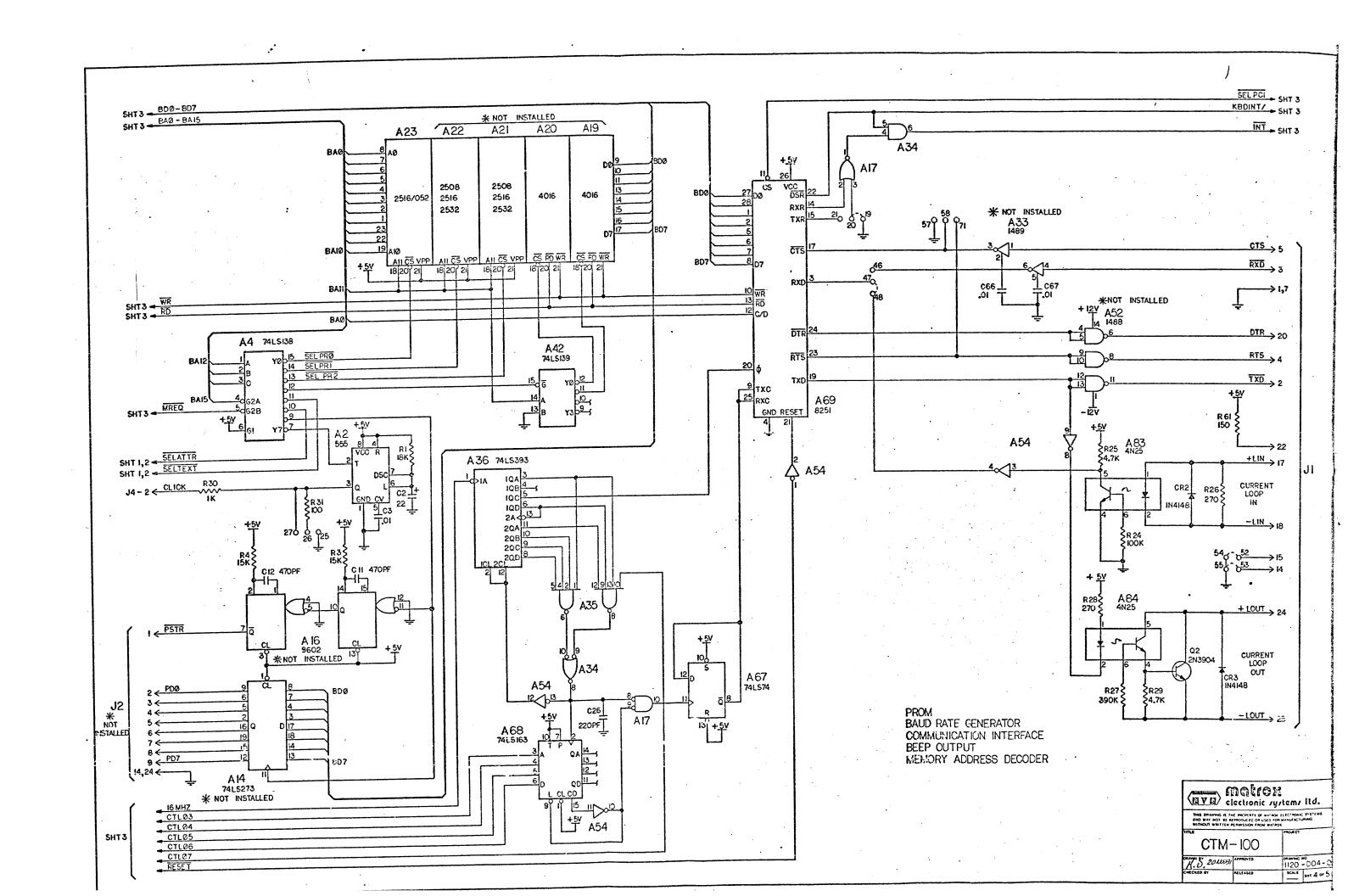
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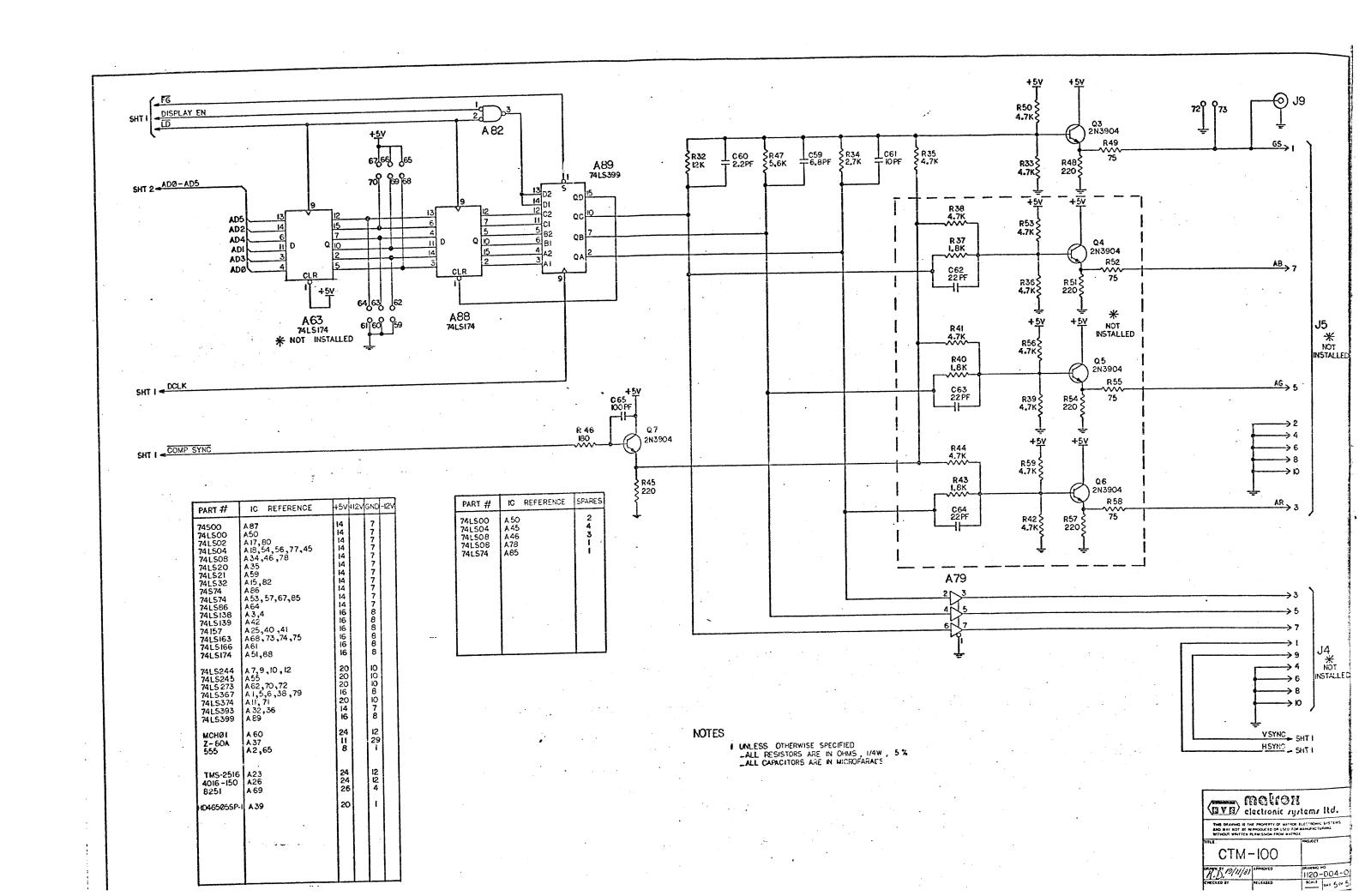
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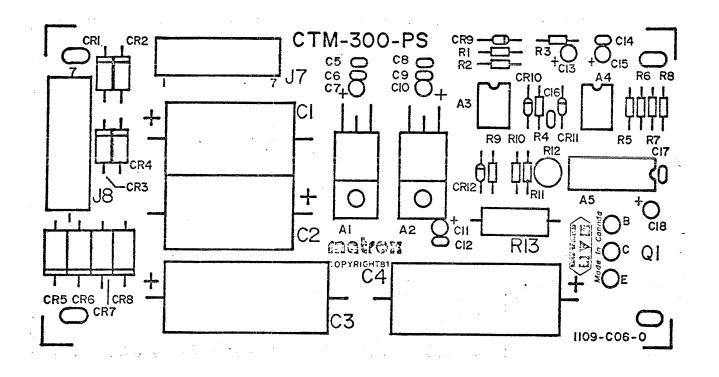










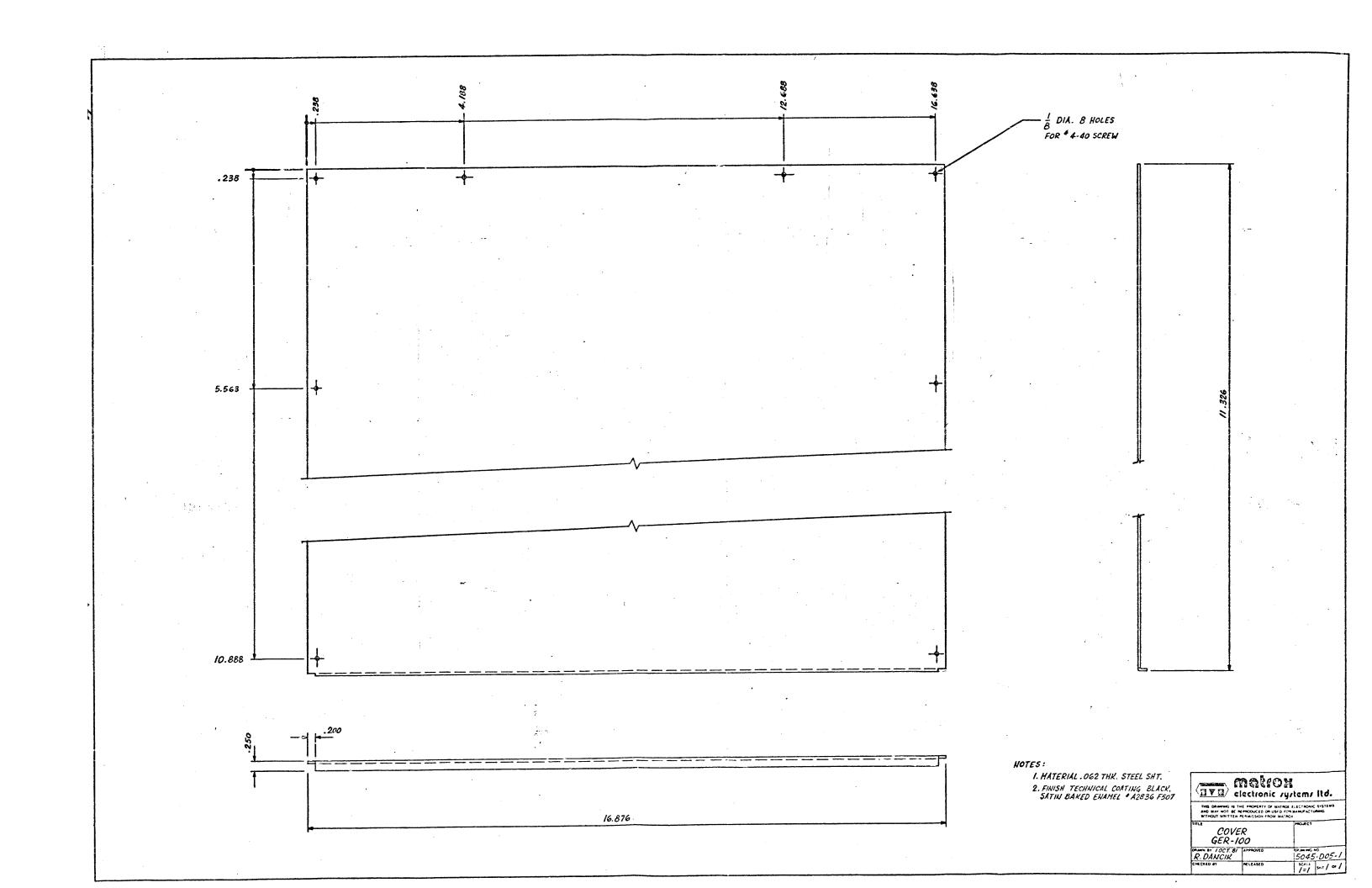


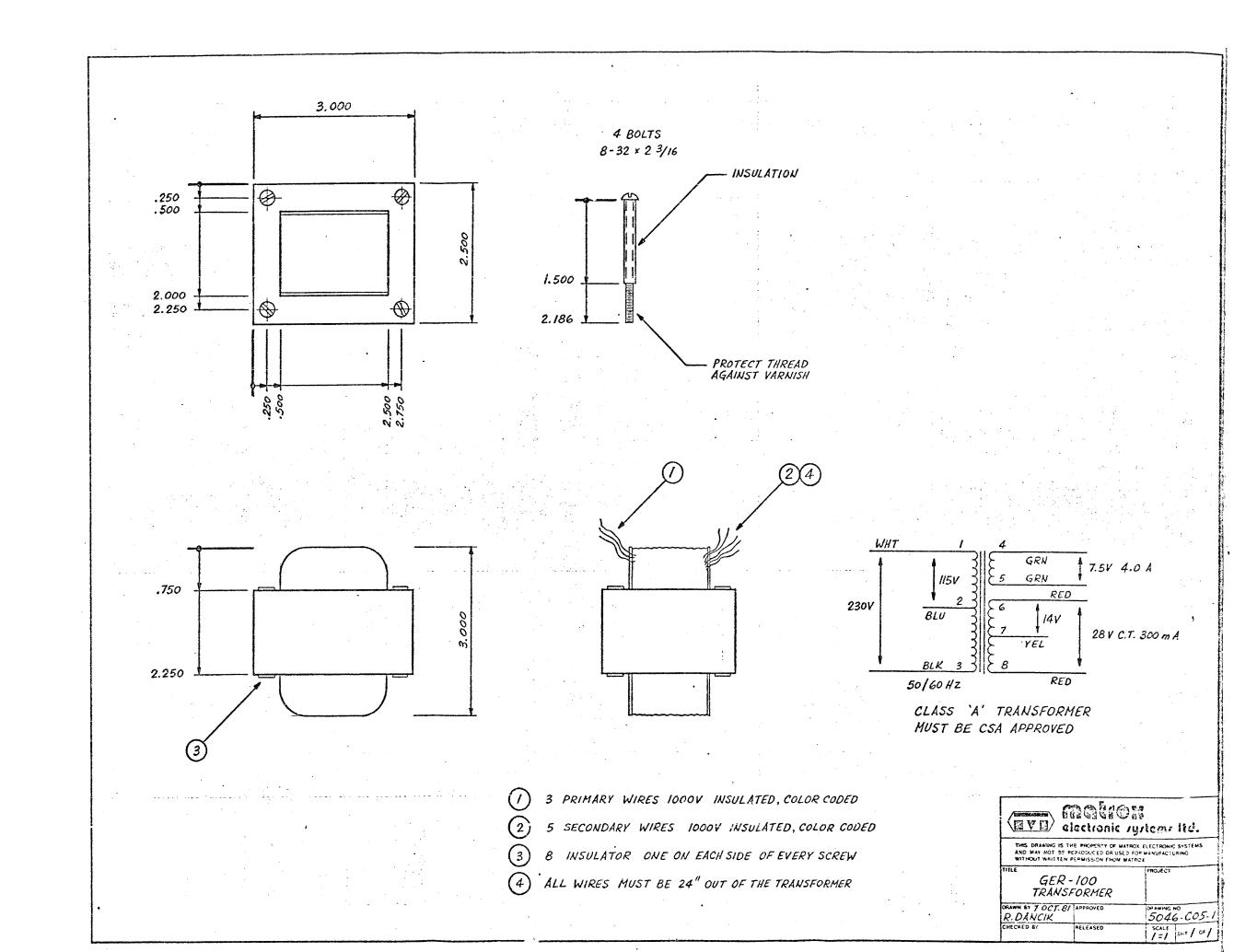


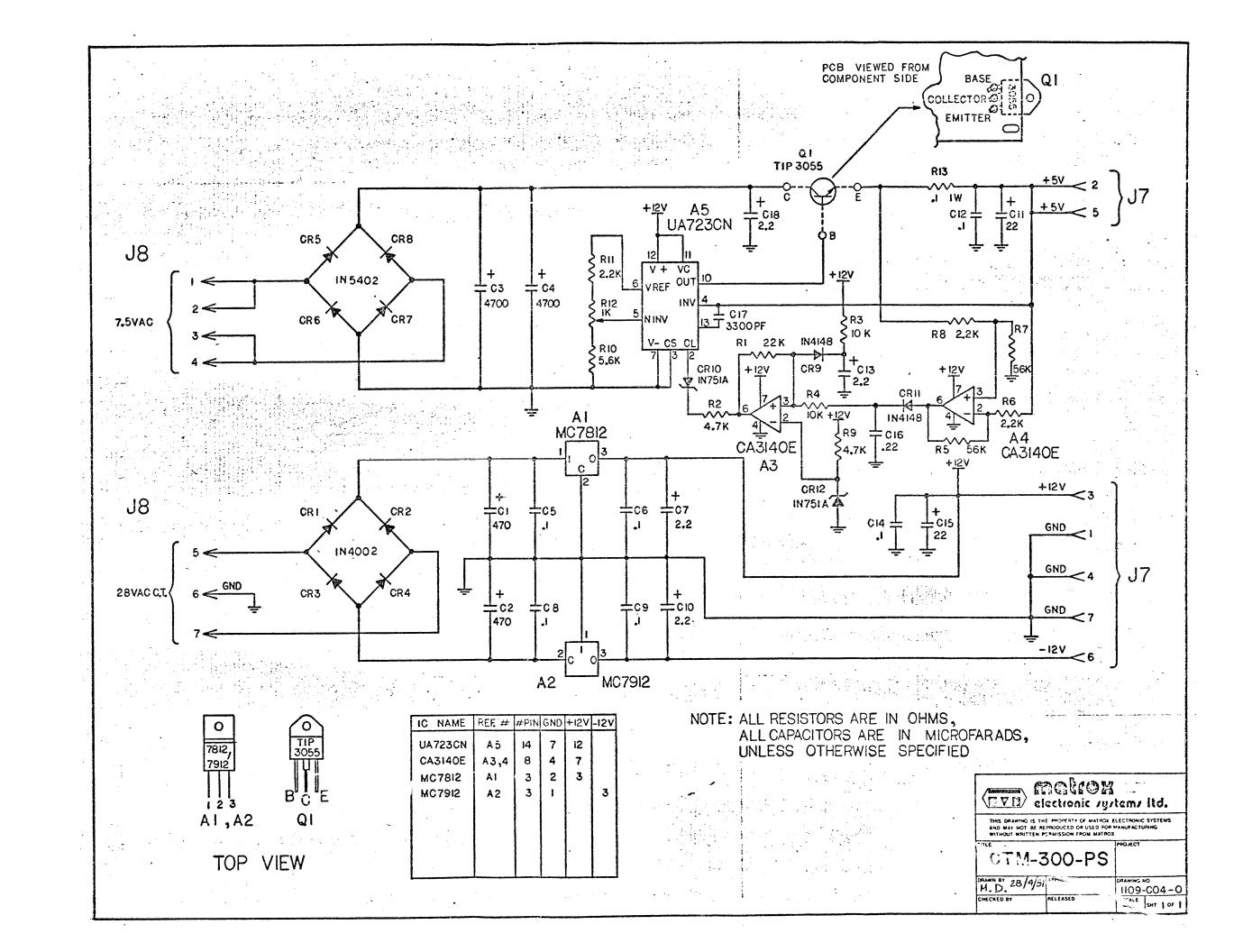
THIS DRAWING IS THE PROPERTY OF MATROX ELECTRONIC SYSTEMS AND MAY NOT BE REPRODUCED OR USED FOR MANUFACTURING WITHOUT WRITTEN PERMISSION FROM MATROX

TITLE		PROJECT
CTM	-300-PS	
DRAWN BY	APPROVED	DRAWING NO
	1	1109-005-0

SCALE SHT OF







# HD 46505R CRT CONTROLLER (CRTC) USERS MANUAL

HITACHI MICROCOMPUTER SYSTEM HMCS 6800



Symbol of Semiconductor Quality, Worldwide

#### 1. Abstract

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT

display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

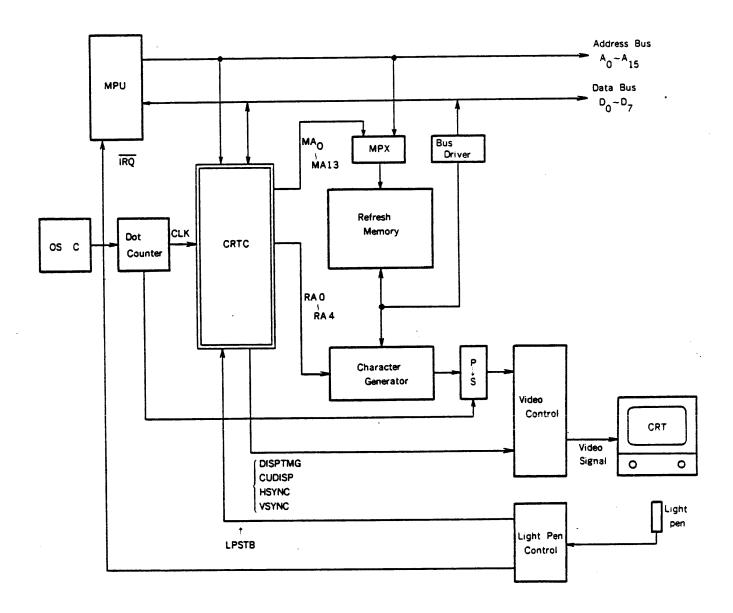


Fig. 1-1 Example of the CRTC Character Display System

### 2. Feature and Function

#### 2.1 Features of the CRTC

- Number of displayed characters on the screen, vertical dot format of one character, horizontal and verzical sync signal, display timing signal are programmable.
- (2) Line buffer-less refreshing.
- (3) 14-bit refresh memory address output. (16K words max. access)

- (4) Programmable interlace/Non-interlace scan mode.
- (5) Built-in cursor control function.
- (6) Programmable cursor height and its blink.
- (7) Built-in light pen detection function.
- (8) Paging and scrolling capability.
- (9) TTL compatible.
- (10) Single + 5V power supply.

### 2.2 Function of the CRTC

Fig.2-1 Function of the CRTC

İtem	Sub-item	Function	Remark
	Programmable screen format	Horizontal scan period  Vertical scan period(per.line)  Vertical scan period(fine adjustment)  Number of characters per line  Number of lines per screen  Number of rasters per line  Horizontal display position on CRT  Vertical display position on CRT  Pulse width of horizontal sync signal	Programmable per one character period Programmable perd one line period Programmable per one raster  Vertical dot number of one character + line space Programmble output timing of sync signal
Function of the CRTC	Programmable cursor display	Cursor display position on screen Cursor height Cursor blink and its Period	Built-in 14-bit cursor register  One choice between 16 fisld period and 32 fisld period
	Scan mode	Non-interlace mode Interlace mode Interlace sync and video mode	One choice
	Light pen	Built-in 14-bit light pen register	
	Refresh Memory Addressing	14-bit refresh memory address output	16K words max.refresh memory access
,	Programmable Start Address	Built-in programmable 14-bit start address register on refresh memory	Paging & scrolling
Structure of the CRTC LSI		Single + 5V power supply TTL compatible input/output Directly connected bus with the HMCS 6800 Family N-channel, Silicon-Gate E/D MOS Full static operation of internal logic 40 pin DIL package	
Application of the CRTC (Expansibility)		Character display  Limited(simple)graphic display  Full graphic display  Color display,blink of displayed characters  Cluster control	Alphanumeric, kanji & other characters Figure display(raster scan display)

#### 3. CRT Display System

#### 3.1 Principle of Raster Scan System

Raster scan system is the system where an electron beam, which is deflected according to a certain rule, hits

against the fluorescent screen of CRT and forms a frame. An ordinary CRT display device forms a frame by deflection of an electron beam by saw wave electric current (or voltage) like a common TV set. This system is shown in Fig. 3-1.

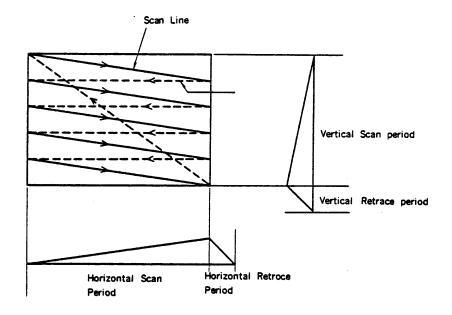
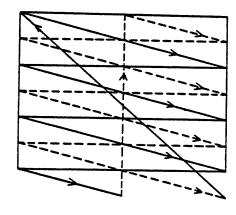


Fig. 3—1 Raster Scan System(Non-interlace)

One frame is composed both of horizontal scan from left to right and of vertical scan from top to bottom to move vertical position. Solid lines in Fig. 3-1 are called scan period (or display period), and broken lines are called retrace period. In this system, increase in frame number per sec enables to lessen its flickering. Increase in scan line per frame enables a high resolution. In an ordinary display device, frame number between 50 and 60 per sec is used. Besides the scan system shown in Fig. 3-1, there is another

scan system called interlace scan system, which is used for a TV set, etc. As shown in Fig. 3-2, each latter half scan is located in the middle of its former scans. Two-time vertical scans (odd and even number fields) form one frame. The CRTC is designed to be able to deal with the scan system (interlace mode) shown in Fig. 3-2 as well as the scan system shown in Fig. 3-1 (non-interlace mode).



Even Number Field(First)

---- Odd Number Field(Second)

Fig. 3—2 Raster Scan System(Interlace)

# 3.2 Principle of Character Display System

Principle of character display is shown in Fig. 3-3. In order to keep characters displayed on CRT screen, it is always necessary to repeat scans and refresh them. To do this, an ordinary CRT display device adopts a method that data to be displayed is stored in memory and screen is refreshed according to its contents. Here, the memory which stores data for display is called Refresh Memory. Data is written on Refresh Memory by data processing system including MPU. The data is written in ASCII code, so it cannot be displayed as characters. It is necessary to

convert the character code into the character pattern. The converter is called Character Generator. Fig. 3-4 shows the principle on which the character code is converted into the character pattern. Character Generator is a kind of ROM which generates the character pattern from the character code and the scan line number as address. Normally one dot period of characters is only several ten ns. To generate the character pattern, it is necessary to read the character dot per row or per column in parallel and to convert into serial. Now  $5 \times 7$ , or  $7 \times 9$  dot matrix format is widely used for display of alphanumeric.

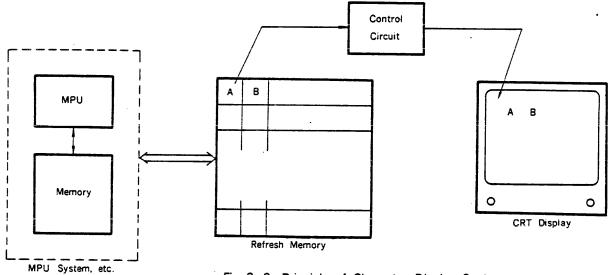


Fig. 3-3 Principle of Character Display System

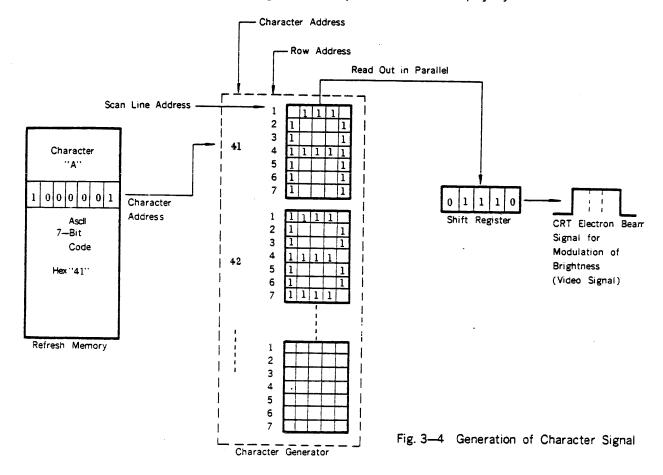


Fig. 3-5 shows an example of character patterns displayed on the screen. Being shown in Fig. 3-1, as an electron beam scans both horizontally and vertically on the screen, the data of refresh memory correspondent to its position of scanning is read out successively. Then the character

pattern of each scan line is generated according to the signal indicating position of the line. This video signal modulates an electron beam current to control brightness so as to display characters on the screen.

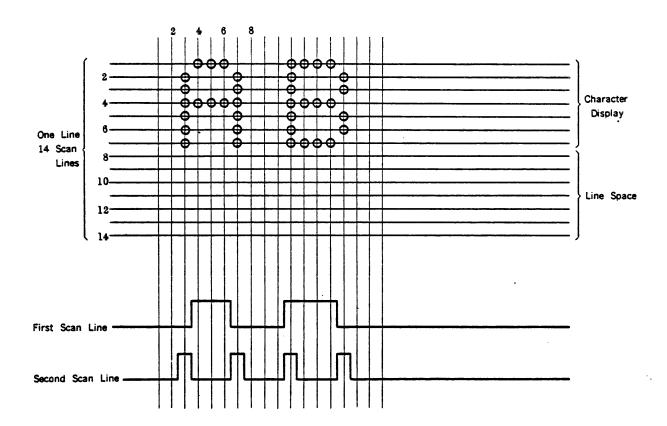


Fig. 3-5 Character Display on the Screen & Video Signal

#### 4. Structure of the CRTC

#### 4.1 Structure of the CRTC

As shown in Fig. 1-1, the CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate RA<sub>0</sub>~RA<sub>4</sub>, DISPTMG, HSYNC, and VSYNC. RA<sub>0</sub>~RA<sub>4</sub> are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit. Linear address generator generates

refresh memory address MA<sub>0</sub>~MA<sub>13</sub> to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16K words max are accessible. Moreover, the use of start address register enables paging and scrolling shown in Fig. 9-11 and 9.12. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

#### 4.2 Pin Assignment

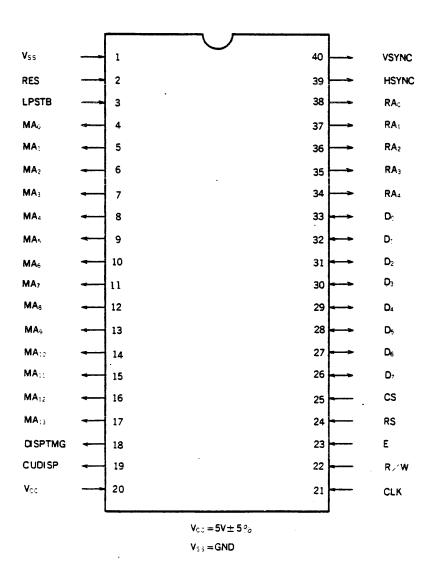


Fig. 4—1 Pin Assignment of the CRTC

# 4.3 Internal Block Diagram

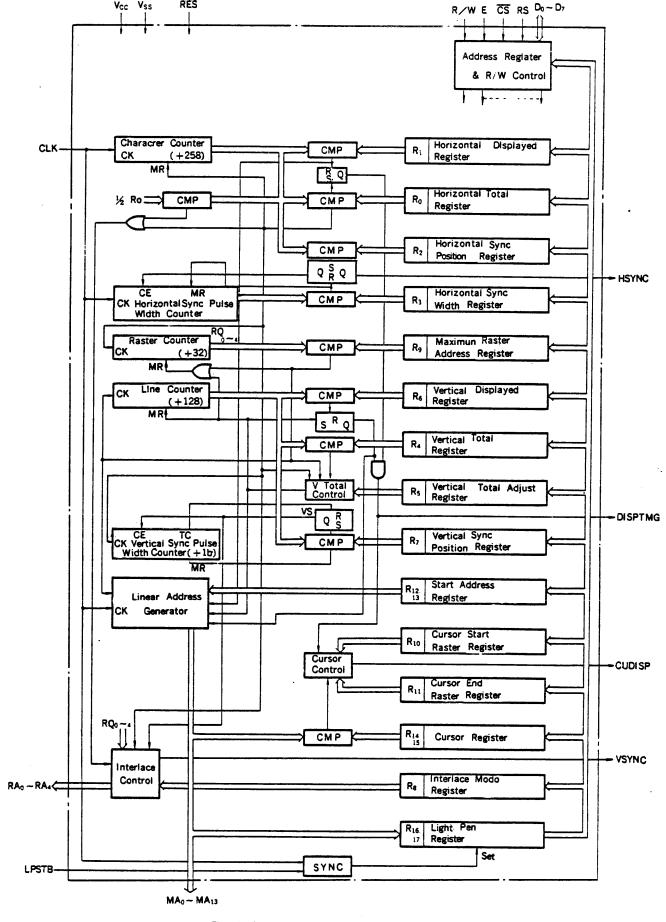


Fig. 4-2 Internal Block Diagram of the CRTC

#### 5. Function of Signal Line

As shown in Fig. 4-1, the CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

#### 5.1 Interface Signals to MPU

#### (1) Bi-directional Data Bus $(D_0 \sim D_7)$

Bi-directional data bus( $D_0 \sim D_7$ ) are used for data transfer between the CRTC and MPU. The data bus output are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

# (2) Read/Write (R/W)

R/W signal controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transferred to MPU. When R/W is at "Low" level, data of MPU is transferred to CRTC.

#### (3) Chip Select(CS)

Chip Select signal (CS) is used to address the CRTC. When CS is at "Low" level, it enables R/W operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA signal of MPU is at "High" level.

#### (4) Register Select(RS)

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bis  $(A_0)$  of MPU address bus.

#### (5) Enable(E)

Enable signal (E) is used as strobe signal in MPU R/W operation with the CRTC internal registers. This signal is normally a derivative of the HMCS6800 System  $\phi_2$  clock.

#### (6) Reset (RES)

Reset signal ( $\overline{RES}$ ) is an input signal used to reset the CRTC. When  $\overline{RES}$  is at "Low" level, it forces the CRTC into the following status.

- l. All the counters in the CRTC are cleared and the device stops the display operation.
- 2. All the outputs go down to "Low" level.
- 3. Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800 family LSIs in the following functions and has restrictions for usage.

- 1. RES signal has capability of reset function only when LPSTB is at "Low" level.
- After RES has gone down to "Low" level, output signals of MA<sub>0</sub>~MA<sub>13</sub> and RA<sub>0</sub>~RA<sub>4</sub>

- synchronize with CLK low level and go down to "Low" level. (At least, 1 cycle CLK signal is necessary for reset.)
- The CRTC starts the display operation immediately after RES signal goes high.

# 5.2 Interface Signals to CRT Display Device

#### (1) Character Clock(CLK)

CLK is a standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external high-speed dot timing logic.

#### (2) Horizontal Sync (HSYNC)

HSYNC is an active high level signal which provides horizontal synchronization for display device.

#### (3) Vertical Sync(VSYNC)

VSYNC is an active high level signal which provides vertical synchronization for display device. The pulse width is fixed at 16 horizontal scans (16H).

### (4) Display Timing(DISPTMG)

DISPTMG is an active high level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at high level.

# (5) Refresh Memory Address(MA<sub>0</sub>~MA<sub>13</sub>)

MA<sub>0</sub>~MA<sub>13</sub> are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enables 16K words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

# (6) Raster Address(RA<sub>0</sub>∼RA<sub>4</sub>)

RA<sub>0</sub>~RA<sub>4</sub> are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

# (7) Cursor Display(CUDISP)

CUDISP is an active high level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at low level. Normally this output is mixed with video signal and provided to the CRT display device.

#### (8) Light Pen Strobe(LPSTB)

LPSTB is an active high level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address  $(MA_0 \sim MA_{1\,3})$  which are shown in Fig.8-2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

### 6. Structure & Function of Internal Registers

### 6.1 Structure of Internal Registers

Table.6-1 Internal Registers of the CRTC

CS	RS	Α	ddre	55 F	legis	ster	Register	Register	Program	DEAD	WRITE				Dat	a Bi	t	·		1
	no	4	3	2	1	0	#	Name	Unit	READ	WANIE	7	6	5	4	3	2	1	0	
1	×	×	×	×	×	×	A		_	_	_						1			;
0	0	×	×	×	×	×	RR	Address Register	-	×	0									
0	1	0	0	0	0	0	Ro	Horizontal Total *7	character	×	0									•1
0	1	0	0	0	0	1	R <sub>1</sub>	Horizontal Displayed	,	×	0									
0	1	0	0	0	1	0	R <sub>2</sub>	Horizontal Sync +7 Position	,	×	0									
0	1	0	0	0	1	1	R <sub>3</sub>	Horizontal Sync Width	И	× .	0			$\setminus$						
0	1	0	0	1	0	0	R4	Vertical Total *7	line I	×	0									
0	1	0	0	1	0	1	R <sub>5</sub>	Vertcal Total Adjust	raster	×	0			1						*2
0	1	0	0	1	1	0	R <sub>6</sub>	Vertical Displayed	line	×	0									
0	1	0	0	1	1	1	R <sub>7</sub>	Vertical Sync *7 Position	,	×	0									
0	1	0	1	0	0	0	R <sub>8</sub>	Interlace Mode	_	×	0							٧	s	*3
0	1	0	1	0	0	1	R <sub>9</sub>	Maximum Raster *7 Address	raster	×	0									•4
o	1	0	1	0	1	0	R <sub>10</sub>	Cursor Start Raster	•	×	0		В	P						*5
0	1	0	1	0	1	1	Rıı	Cursor End Raster	•	×	0		$\setminus$							<b>*</b> 6
0	1	0	1	1	0	0	R <sub>12</sub>	Start Address(H)	_	×	0		/							,
0	1	0	1	1	0	1	R <sub>13</sub>	Start Address(L)	-	×	0									
0	1	0	1	1	1	0	R <sub>14</sub>	Cursor(H)	-	0	0	abla	$\setminus$							
0	1	0	1	1	1	1	R <sub>15</sub>	Cursor(L)	_	0	0		`							
0	1	1	0	0	0	0	R <sub>16</sub>	Light Pen(H)	_	0	×									
0	1	1	0	0	0	1	R <sub>17</sub>	Light Pen(L)		0	×		`							

NOTE: 1 When R<sub>8</sub> is 1 or 3 (Interlace Mode), programmed data must be odd.

- 2 When R<sub>8</sub> is 3, N/2 (N: total number of lines)
- 3 When S is 1, V specifies video mode. S specifies interlace sync mode.
- 4 When R<sub>8</sub> is 3, programmed data must be odd.
- 5 B specifies the cursor blink. P specifies the cursor blink period.

{	16 or 3	2 Field I	Period		1
(	light	dark	light	dark	period }

- 6 When R<sub>8</sub> is 3, the cursor start and the cursor end raster registers must be both even or both odd.
- 7 Programmed Value = Specified Value 1
  In the following explanation, for instance, total number of horizontal characters means "Specified Value"

# 6.2 Function of Internal Registers

#### (1) Address Register(AR)

This is a 5-bit register used to select 18 internal control registers  $(R_0 \sim R_{17})$ . Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to  $R_0 \sim R_{17}$  requires, first of all, to write the address of corresponding control register into this register. When RS and  $\overline{\text{CS}}$  are at low level, this register is selected.

#### (2) Horizontal Total Register(Ro)

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even. How to decide total number of characters is shown in 9.5.1.

#### (3) Horizontal Displayed Register(R<sub>1</sub>)

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

#### (4) Horizontal Sync Position Register(R2)

This is a register used to program horizontal sync position in unit of horizontal character time. Data is 8-bit and any number that is under the following condition (Horizontal Sync Position + Horizontal Pulse Width < Horizontal Total Characters) can be programmed. When H is character number of horizontal Sync Position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

# (5) Horizontal Sync Width Register(R<sub>3</sub>)

This is a register used to program horizontal sync pulse width from 1 to 15 in unit of horizontal character time. Note that when 0 is programmed, HSYNC is not provided.

#### (6) Vertical Total Register(R4)

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRTC. When N is total number of lines, (N-1) shall be programmed to this register. How to decide total number of lines is shown in 9.5.1.

# (7) Vertical Total Adjust Register(R<sub>5</sub>)

This is a register used to program the optimum number from 0 to 31 to adjust total number of rasters per frame. This register enables to decide the number of

vertical deflection frequency more strictly.

# (8) Vertical Displayed Register(R<sub>6</sub>)

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

# (9) Vertical Sync Position Register(R7)

This is a register used to program the vertical sync position on the screen in unit of horizontal character time. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, (V-1) shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

#### (10) Interlace Mode Register(R<sub>8</sub>)

This is a 2-bit register used to control the raster scan mode. (See Table.6-2)

Table.6-2 Interlace Mode

21	2°	Mode
0	0	Non-Interlace Mode
1	0	Non-Interlace Mode
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In interlace sync and video mode, the raster scan method is the same as that in interlace sync mode, but it is controlled to display different character pattern in two fields.

# (11) Maximum Raster Address Register (Rg)

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including spacing. When total number of rasters is RN, (RN-1) shall be programmed to this register. Moreover, when programmed value of  $R_8$  is "3", RN must be even.

#### (12) Cursor Start Raster Register(R<sub>10</sub>)

This is a register used to program the cursor start raster address by lower 5 bits  $(2^0 \sim 2^4)$  and the cursor display mode by higher 2 bits  $(2^5, 2^6)$ .

Table.6-3 Cursor Display Mode

26	25	Cursor Display Mode	
0	0	Non-Blink	
0	1	Cursor Non-Display	
1	0	Blink, 16 Field Period	
1	1	Blink, 32 Fiel dPeriod	

#### Blink Period

light	dark

16 or 32 Field Period

#### (13) Cursor End Raster Register (R11)

This is a register used to program the cursor end raster address. When programmed value of  $R_8$  is "3" (Interlace sync & video mode), both the cursor start raster register and the cursor end raster register must be even or odd.

### (14) Start Address Register (R<sub>12</sub>, R<sub>13</sub>)

These are used to program initial address of refresh memory to read out. Changing the contents of these registers dynamically enables paging and scrolling easily.

# (15) Cursor Register(R<sub>14</sub>,R<sub>15</sub>)

These are used to program the cursor display address and R/W operation from MPU is possible. When  $R_{14}$  is read, the higher 2 bits  $(2^6,2^7)$  are always "0".

### (16) Light Pen Register(R<sub>16</sub>,R<sub>17</sub>)

These are used to catch the detection address of light pen and only a read operation from MPU is possible. When  $R_{16}$  is read, the higher 2 bits  $(2^6, 2^7)$  are always "0". Its value needs to be corrected in software because there is time delay from address output of the CRTC to signal input to LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 8-2 needs to be taken into account.

### 7. Operation of the CRTC

### 7.1 Time Chart of CRT Interface Signals

The following example shows the display operation in

which values of Table. 7-1 are programmed to the CRTC internal registers. Fig. 7-1 shows the CRT screen format. Fig. 7-4 shows the time chart of signals output from the CRTC.

Table.7-1 Programmed Values into the Registers

Reg	Register Name	Value	Reg	Register Name	Value
R <sub>0</sub>	Horizotal Total	N <sub>ht</sub>	R,	Max. Raster Address	N <sub>r</sub>
R <sub>1</sub>	Horizontal Displayed	N <sub>hd</sub>	R <sub>10</sub>	Cursor Start Raster	
R <sub>2</sub>	Horizontal Sync Position	N <sub>hsp</sub>	R <sub>11</sub>	Cursor End Raster	i
R <sub>3</sub>	Horizontal Sync Width	N <sub>hsw</sub>	R <sub>12</sub>	Start Address(H)	0
R₄	Vertical Total	N <sub>vt</sub>	R <sub>13</sub>	Start Address(L)	0
R <sub>5</sub>	Vertical Total Adjust	N <sub>adj</sub>	R <sub>14</sub>	Cursor(H)	
R <sub>6</sub>	Vertical Displayed	N <sub>vd</sub>	R <sub>15</sub>	Cursor(L)	
R <sub>7</sub>	Vertical Sync Position	N <sub>vsp</sub>	R <sub>16</sub>	Light Pen(H)	
R <sub>8</sub>	Interlace Mode	•	R <sub>17</sub>	Light Pen(L)	

NOTE:  $N_{hd} < N_{ht}$  ,  $N_{vd} < N_{vt}$ 

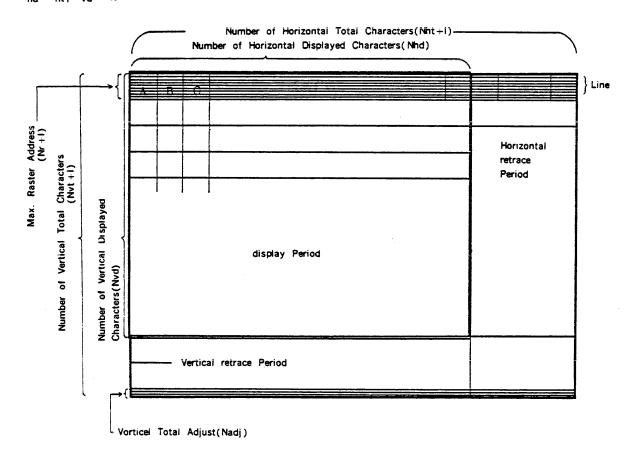
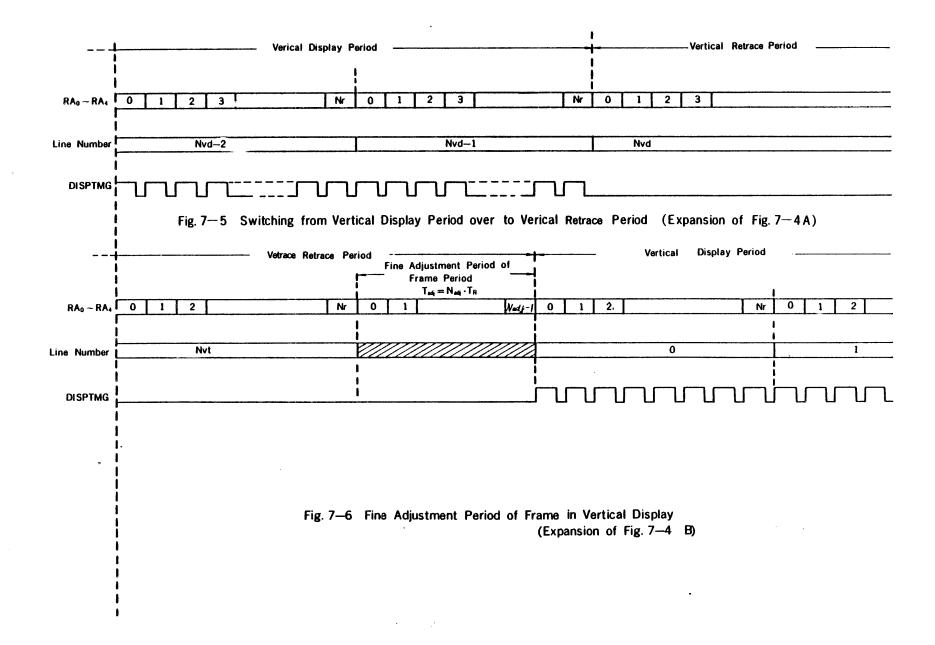


Fig. 7—1 CRT Screen Format



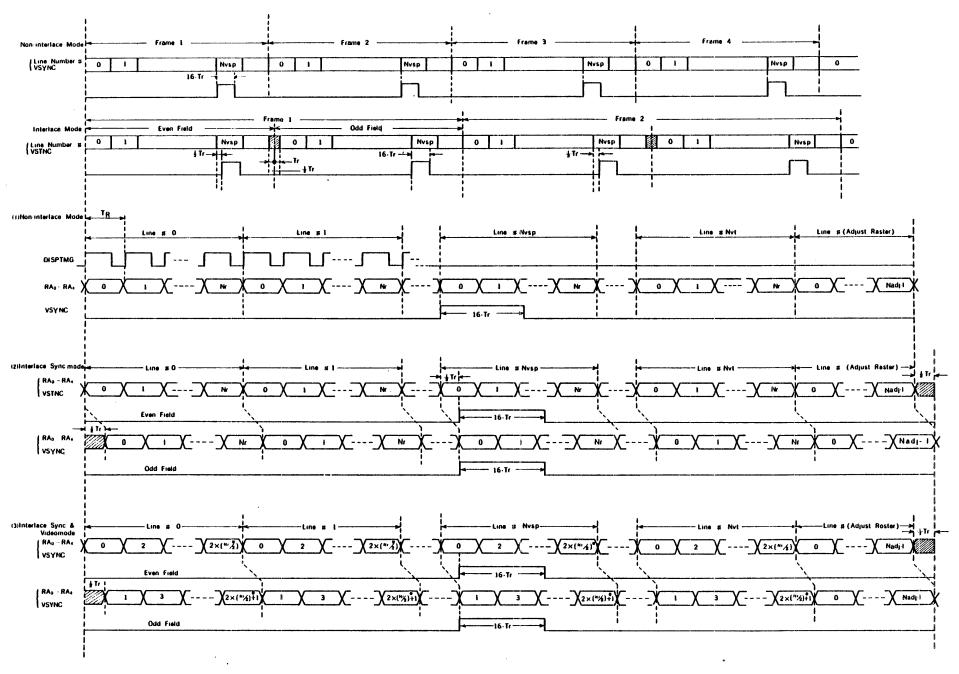
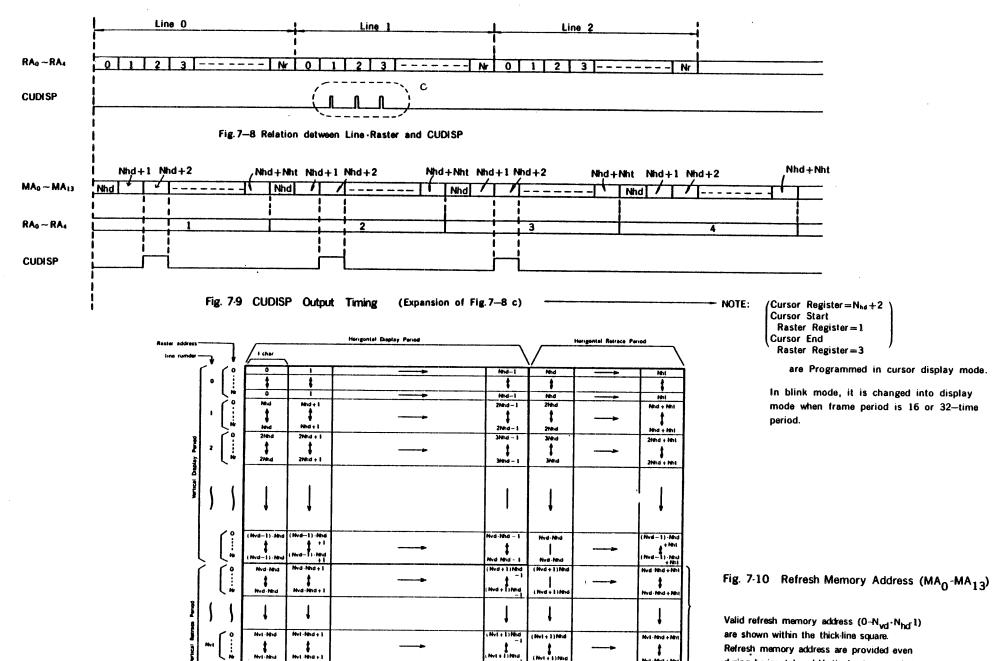


図 Fig. 7-7 Interlace Control

NOTE1 In interlace sync & video mode, maximum raster address(Nr))shall be odd
2 in interlace mode, Nht shall be odd



Nvl + 2) Nhd

(Not + 2) -Nhd

(Nvt + 1) - Hhd

Nvt - Nhd + Nn

(Nvi+1)Nhd A +Nhi

during horizontal and Vertical retrace period.

This is an example in the case where the programmed value of start address register is 0.

### 8. Electrical Characteristics of the CRTC

#### 8-1 Maximum Ratings

Table. 8-1 Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V <sub>cc</sub> *	$-0.3 \sim +7.0$	V
Input Voltage	V <sub>IN</sub> *	-0.3~+7.0	V
Operating Temperature Range	Ta	-20 ~+75	·c
Storage Temperature Range	Tstg	-55 ~+150	·c

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

\* With respect to Vss(SYSTEM GND)

8-2 Recommended Operating Conditions
Table. 8—2 Recommended Operating Conditions

Item	Symbol	min	typ	max	Unit
Supply Voltage	Vcc	4.75	5	5.25	V
	VIL	-0.3	_	0.8	V
Input Voltage	V <sub>IH</sub>	2.0	_	Vcc	V
Operating Temperature Range	Та	-20	25	75	·c

# 8-3 Electrical Characteristics

Table. 8—3 DC Characteristics

 $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_{a}=-20\sim +75$ °C

Item	Symbol	min	typ	max	Unit
Input High Voltage	ViH	2.0	1	$V_{CC}$	V
Input Low Voltage	Vil	-0.3	1	0.8	V
Input Leak Current	Im	_	1.0	2.5	μA
Three-State Input Current Vin=0.4~2.4V Vcc=5.25V	ITSI	_	2.0	10	μΑ
Output High Voltage $I_{LOAD} = -205 \mu A D_0 \sim D_7$ $I_{LOAD} = -100 \mu A$ All Other Outputs	V <sub>OH</sub>	2.4	_	_	v
Output Low Voltage ILOAD=1.6mA	VoL	_	_	0.4	v
Input Capacitance D <sub>0</sub> ~D <sub>7</sub> All Other Inputs	C <sub>IN</sub>		_	12.5 10.0	pF
Output Capacitance	Соит	_	_	10.0	pF
Power Dissipation	P <sub>D</sub>		600	1000	mW

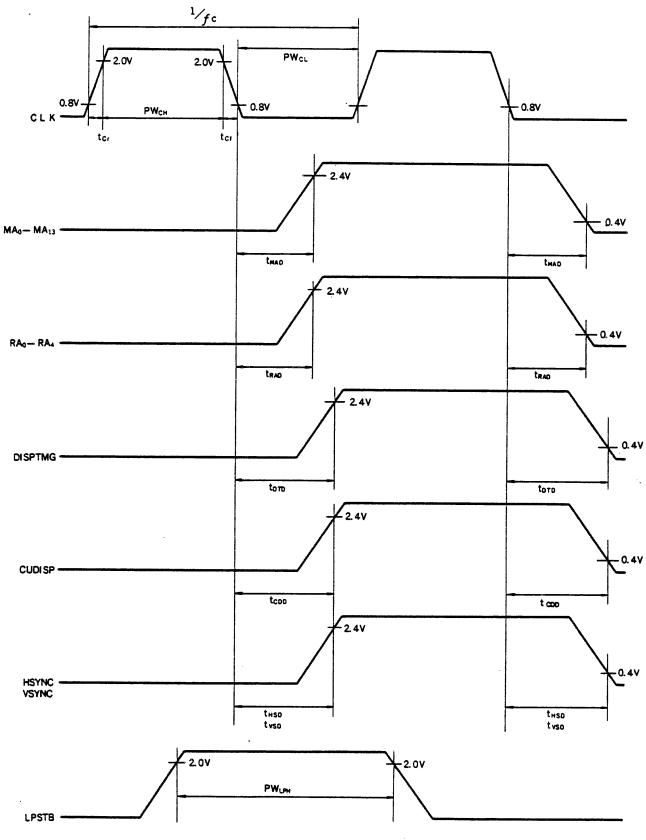
Table. 8-4 AC Characteristics

Item	Symble	min	typ	max	Unit
Clock Frequency	f <sub>c</sub>	_	_	3.0	MHz
Clock Pulse Width, Low	PW <sub>CL</sub>	150			ns
Clock Pulse Width, High	PW <sub>CH</sub>	150	_	_	ns
Rise and Fall Time For Clock Input	t <sub>CR</sub> t <sub>CF</sub>	_	_	15 15	ns
Memory Address Delay Time	t <sub>MAD</sub>	_	_	160	ns
Raster Address Delay . Time	t <sub>RAD</sub>	_	_	160	ns
Display Timing Delay Time	toro	_	_	250	ns
Horizontal Sync Delay Time	tHSD	_	_	250	ns
Vertical Sync Delay Time	tvsD	_	_	250	ns
Cursor Display Delay Time	tcdd	_	_	250	ns
Light Pen Strobe Pulse Width	PWLPH	80	_	_	ns
Light Pen Strobe Uncertain Time of Acceptance (Fig. 8-2)	t <sub>LPD1</sub>	_ _	_	80 10	ns

# 8-4 Bus Timing Characteristics

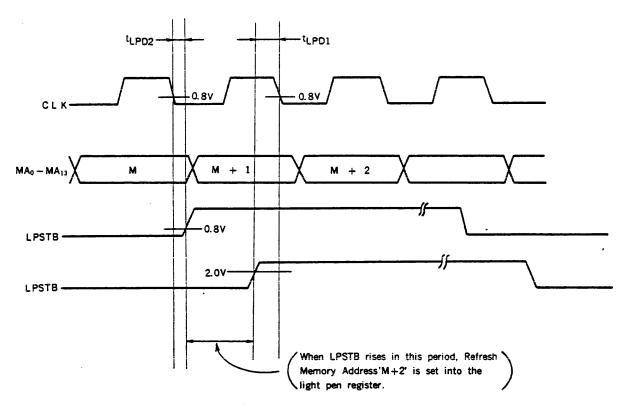
Table. 8-5 Read Sepuence

Item	Symbol	Test condi- tion	min	typ	max	Unit
Enable Cycle Time	t <sub>CYCE</sub>	-	1.0	_	_	μS
Enable Pulse Width ("High"level time)	PWEH	_	0.45	_	-	μs
Enable Pulse Width ("Low"level time)	· DW		0.40			-
Set Up Time ADDRESS-ENABLE	ias		140		_	ns
Data Delay Time	toor	_	_	_	320	ns
Data Hold Time	ţн	_	10	_	_	ns
Rise & Fall Time for Enable Input	ter/ter	_	_	_	25	ns
Address Hold Time	t <sub>AH</sub>	_	10		_	ns
Data Access Time	tacc	_	_	_	460	ns



This Figure shows the relation in time between CLK signal and each output signals. Output sequence is shown in Fig.  $7-4 \sim \text{Fig.} 7-9$ .

Fig. 8—1 Time Chart of the CRTC



 $\begin{array}{ll} \mathbf{f}_{\text{LPD1'}} & \mathbf{t}_{\text{LPD2}} & \text{LPSTB' s uncertain time} \\ & \text{of acceptance.} \end{array}$ 

Fig. 8—2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen register.

Table. 8-6 Write Sequence

ltem	Symbol	Test condi- tion	min	typ	max	Unit
Enable Cycle Time	tcyce	_	1.0	_	_	μs
Enable Pulse Width ("High"level time) Enable Pulse Width ("Low"level time)	PW <sub>EH</sub>	_	0.45 0.40	_	_	μs
Set Up Time	tas	_	140	_	_	ns
Data Set Up Time	tosw	_	195	_	_	ns
Data Hold Time	t <sub>H</sub>	_	10	_	_	ns
Rise & Fall Time for Enable Input	ter/ter	_	-	-	25	ns
Address Hold Time	t <sub>AH</sub>	-	10	<u> </u>	_	ns

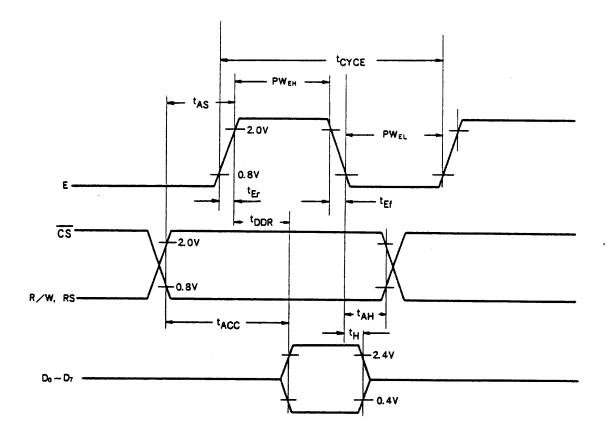


Fig. 8—3 Read Sequence

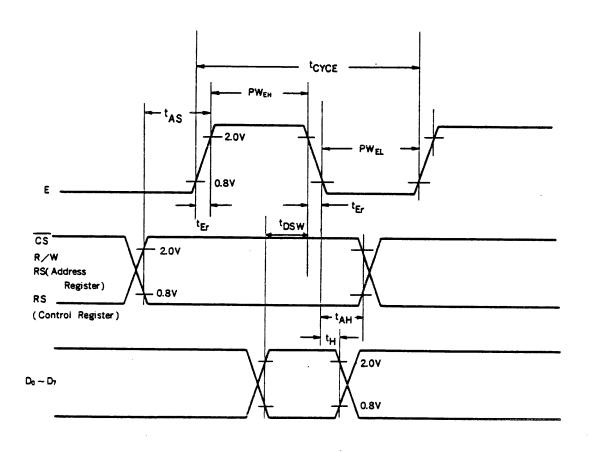


Fig. 8-4 Write Sequence

#### 9. How to Use the CRTC

#### 9-1 Interface to MPU

As shown in Fig. 9-1, the CRTC is connected with the standard bus of MPU to control the data transfer between them. The CRTC address is determined by  $\overline{CS}$  and RS, and the R/W operation is controlled by R/W and Enable signals. When  $\overline{CS}$  is "Low" and RS is also "Low", the CRTC address register is selected. When  $\overline{CS}$ 

is "Low" and RS is "High", one of 18 internal registers is selected.

 $\overline{RES}$  is the system reset signal. When  $\overline{RES}$  becomes "Low", the CRTC internal control logic is reset. But internal registers shown in Table. 6-1( $R_0 \sim R_{17}$ ) are not affecteb by  $\overline{RES}$  signal and remain unchanged.

The CRTC is designed so as to provide an interface to microcomputers, but adding some external circuits enables an interface to other data sources.

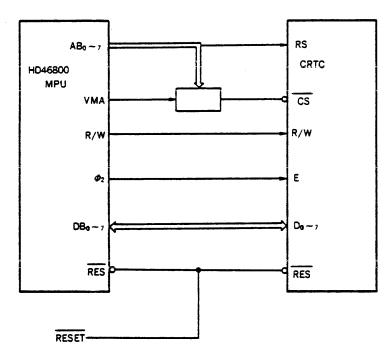


Fig. 9-1 Interface to MPU

#### 9-2 Dot Timing Generating Circuit

CRTC's CLK input (21 pin) is provided with CLK signal which defines horizontal character time period from the outside. This CLK signal is generated by dot counter shown in Fig. 9-2. Fig. 9-2 shows a example of circuit where horizontal dot number of the character

is "9". Fig. 9-3 shows the operation time chart of dot counter shown in Fig. 9-2. As this example shows explicitly, CLK signal is at "Low" level in the former half of horizontal character time and at "High" level in the latter half. It is necessary to be careful so as not to mistake this polarity.

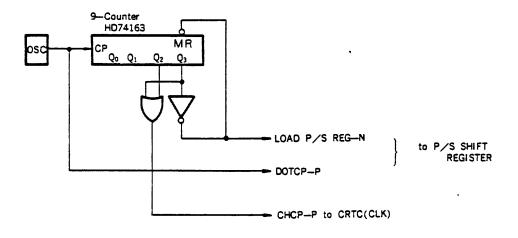


Fig. 9-2 Dot Counter

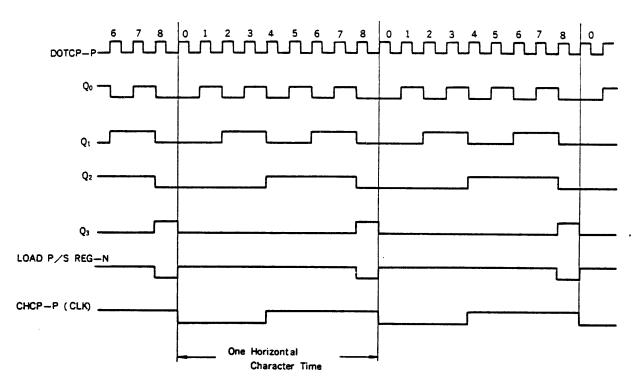


Fig. 9-3 Time Chart of Dot Counter

#### 9.3 Interface to Display Control Unit

Fig. 9-4 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit For refresh memory, 14 Memory Address line  $(0\sim16383)$  max are provided and for character generator, 5 Raster Address line  $(0\sim31)$  max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC signals are sent out. DISPTMG

signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

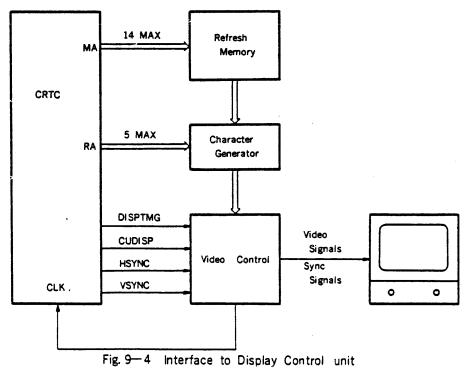
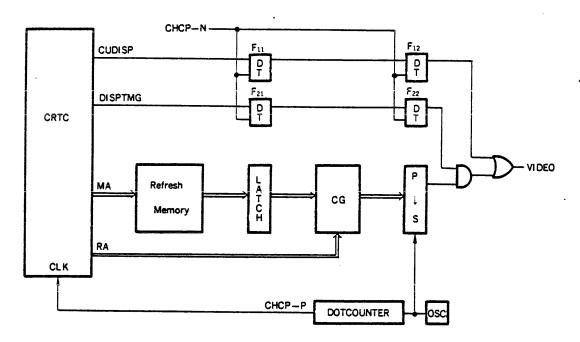


Fig. 9-5 shows more detailed block diagram of display control unit. This shows how to use DISPTMG and CUDISP signals. By delaying for one or two-character time, DISPTMG signal synchronizes with output timing of parallel-serial converter to control blanking of character video signal. By delaying for one or two-character time, CUDISP signal is mixed with character video signal. Whether delay time of DISPTMG and CUDISP signals should be one or two-character time, moreover, whether

LATCH register is necessary for output from refresh memory or not, are determined, as shown in Fig. 9-5, by the relations among one horizontal character time, delay time of Memory Address, access time of refresh memory, and access time of character generator.

For reference, time chart from refresh memory address MA to video signal in the case of two-character time delay is shown in Fig. 9-6.



Case	Aceess Time of RM and CG	LATCH	Fıı	F <sub>21</sub>	F <sub>12</sub>	F <sub>22</sub>
1	RM Access + CG Access >t <sub>CH</sub> -t <sub>MAD</sub>	N	N	N	N	N
2	RM Access + CG Access < t <sub>CH</sub> - t <sub>MAD</sub>	UN	N	N	UN	UN

[NOTE] N: Necessary

UN: Unnecessary

t<sub>CH</sub>: Cycle time of CHCP

t<sub>MAD</sub>: Delay time of MA

Fig. 9-5 Display Control unit

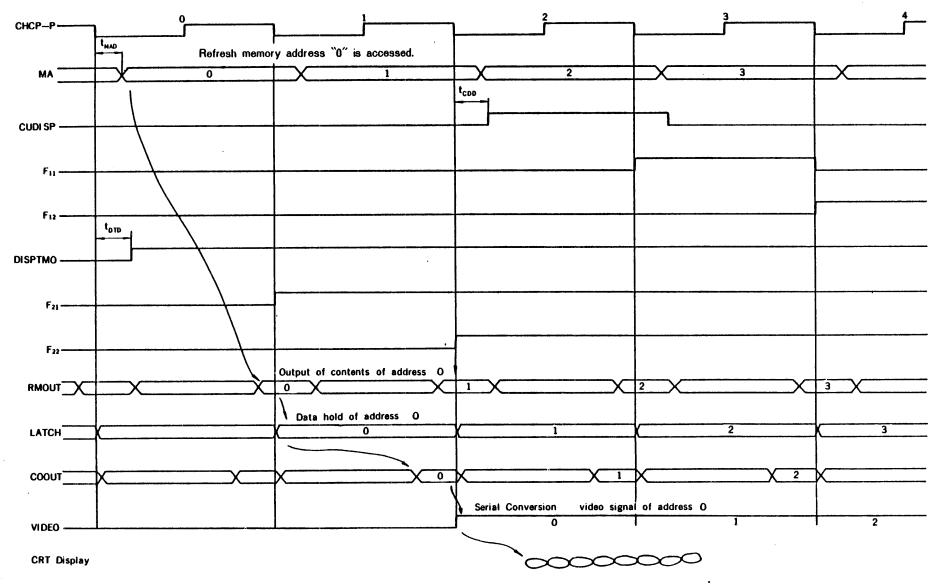


Fig. 9-6 Time Chart of Display Control unit

#### 9.4 Interface to CRT

To display video signals such as characters on the CRT, sync signals which drive the deflection circuit of CRT display unit and video signals which modulate brightness of an electron beam are needed. The ways in which these signals are interfaced are different according to the CRT display devices.

Fig. 9-7 shows four typical types of interfaces to CRT display unit. Fig. 9-7(A) shows the way in which HSYNC, VSYNC, and VIDEO signals are interfaced separately to

CRT display unit. Fig. 9-7(B) shows the way in the mixed signal of HSYNC and VSYNC signals EXCLUSIVE-OR GATE and VIDEO signal are interfaced to CRT display unit. Fig. 9-7(C) shows the way in which composite video signal of HSYNC, VSYNC, and VIDEO signals by Mixer is solely interfaced to CRT display unit. Fig. 9-7(D) shows the way in which composite video signal is modulated into high-fre quency signal by RF modulator and connected with antenna terminal of TV. This way is used in video game machines.

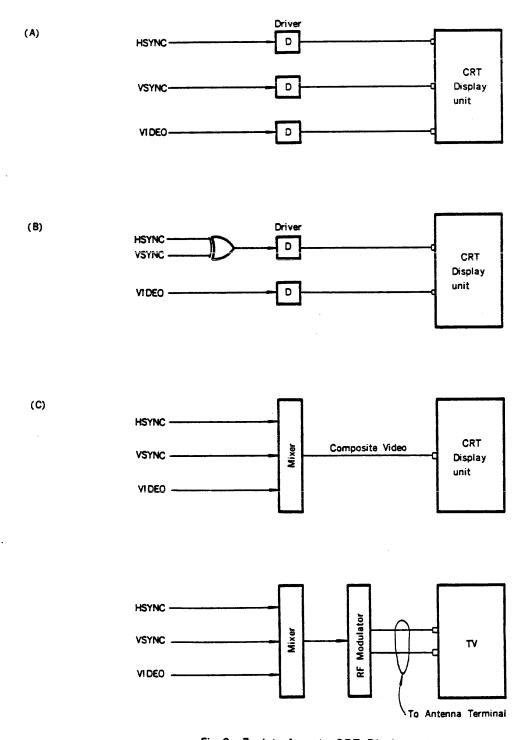


Fig. 9-7 Interface to CRT Display unit

#### 9.5 How to Decide Parameters Set on the CRTC

Tadle. 9-1 shows parameters which are necessary for CRT display. Some of them are decided by the specification of CRT display unit (Monitor) and others are decided by the display format on the screen. Moreover, CRTC internal registers which are related to setting these parameters are shown in this Table.

Table. 9-1 Parameters For CRT Display

Item	Specification of Monitor	Screen Format	CRTC Registers		
Dot Number of Characters (Horizontal)		0	External Circuits		
Dot Number of Characters (Vertical)		. 0	R,		
Number of Horizontal Total Characters	0		Ro		
Number of Horizontal Displayed Characters	Δ	0	Rı		
Horizontal Sync Position	0		R <sub>2</sub>		
Horizontal Sync Pulse Width	0		R <sub>3</sub>		
Number of Vertical Total Characters	0		R4		
Number of Vertical Displayed Characters	Δ	0	R <sub>6</sub>		
Vertical Sync Position	0		<b>R</b> 7		
Scan Mode		0	R <sub>s</sub>		
Cursor Display Method		0	R10, R11		
Start Address		0	R <sub>12</sub> , R <sub>13</sub>		
Cursor Address		0	R14, R15		

△·····Under the restriction of spcification of CRT display unit. (Monitor)

# 9.5.1 How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

#### (1) Number of Horizontal Total Characters

Horizontal deflection frequency  $f_b$  is given by specification of CRT display unit. Number of horizontal

Total characters is determined by the following equation. (Ref. 9.5-2(3))

$$f_h = \frac{1}{t_c(N_{ht}+1)}$$

where,

t<sub>c</sub>: Cycle Time of CLK (Character Clock)

 $N_{ht}$ : Programmed Value of Horizontal Total Register ( $R_0$ )

#### (2) Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation. (Ref. 9.5.2(4))

$$f_v = \frac{f_h}{R_t} = \frac{f_h}{(N_{vt} + 1)(N_r + 1) + N_{adj}}$$

where,

R<sub>t</sub>: Number of Total Rasters per frame (Including retrace period)

N<sub>vt</sub>: Programmed Value of Vertical Total Register (R<sub>4</sub>)

N<sub>r</sub>: Programmed Value of Maximum Raster Address Register (R<sub>9</sub>)

N<sub>adj</sub>: Programmed Value of Vertical Total Adjust Register (R<sub>5</sub>)

#### (3) Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to horizontal sync width register  $(R_3)$  in unit of horizontal character time.  $R_3$  is a 4-bit register, so programmed value can be selected within from 1 to 15.

#### (4) Horizontal Sync Position

As shown in Fig. 9-3, horizontal sync position is normally selected to be in the middle of horizontal blank period. But there are some cases where its optimum sync position is not located in the middle of horizontal blank period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

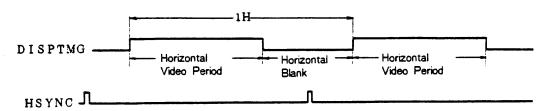


Fig. 9-8 Time Chart of HSYNC

#### (5) Vertical Sync Position

As shown in Fig. 9-9, vertical sync position is normally selected to be in the middle of vertical blank period. But there are some cases where its optimum sync position is not located in the middle of vertical blank

period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register  $(R_7)$  in unit of line period.

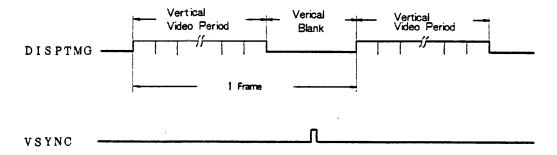


Fig. 9-9 Time chart of VSYNC

# 9-5-2 How to Decide Parameters Based on Screen Format

#### (1) Dot Number of Characters (Horizontal)

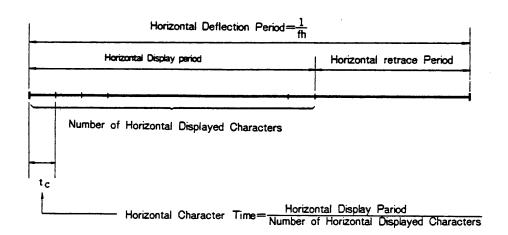
Dot number of characters (horizontal) is determined by character font and character space. More strictly, as shown in Fig. 9-2, dot number of characters (horizontal) N is determined by external N-counter.

#### (2) Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by character font and line space. Dot number of characters (vertical) is programmed to maximum raster address register ( $R_9$ ) of the CRTC. When  $N_r$  is programmed value of  $R_9$ , dot number of characters (vertical) is ( $N_r+1$ ).

# (3) Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R<sub>1</sub>) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, as Fig. 9-10 shows the access method of refresh memory, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.



#### (4) Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R<sub>6</sub>). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (R<sub>1</sub>) including vertical retrace period, CRT which is suitable for desired screen format should be selected. The relation between number of vertical displayed characters and number of total rasters per frame shown in 9-5-2(2) is shown in the following equation.

$$R_t = (N_{rt} + 1)(N_r + 1) + N_{adj}$$
 (Non Interlace Mode)  
Number of Vertical Total Characters = Number of

Vertical Displayed Characters (N<sub>vd</sub>) + Number of Characters during vertical retrace period

 $R_t = (N_{vt} + 1)(N_r + 1) + N_{adj} + 0.5$  (Interlace Mode) For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster  $(N_{adj})$  within specification of vertical deflection frequency.

# (5) Scan Mode

The CRTC can program three scan modes shown in Table. 9-2 to interlace mode register ( $R_4$ ). An example of character display in each scan mode is shown in Fig. 7-2.

Table. 9-2 Program of Scan Mode

21	20	Scan Mode	Main Usage
0	0	Non-Interlace	Normal Display of Characters & Figures
_		Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-Resolution CRT

[NOTE] In interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of lumine-scence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

#### (6) Cursor Display Method

Cursor start raster register and cursor end raster register ( $R_{10}$ ,  $R_{11}$ ) enable programming the display modes shown in Table 6-3 and display patterns shown in Fig. 7-3. Therefore, it is possible to change the method of cursor display dynamically according to the system

conditions as well as to realize the cursor display that meets the system requirements.

#### (7) Start Address

Start address registers ( $R_{12}$ ,  $R_{13}$ ) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

#### (8) Cursor Register

Cursor registers (R<sub>14</sub>, R<sub>15</sub>) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

# 9-6 Relation Between Number of Displayed Characters and Memory Address

Refresh memory address of the CRTC (MA<sub>0</sub>~MA<sub>13</sub>) is linear address which starts from the value of start address. It does not need the address conversion circuit in wide use that determines the address of refresh memory to read out by line address and row address and can be used without change.

Moreover, as start address registers ( $R_{12}$ ,  $R_{13}$ ) enable to change the initial address of refresh memory dynamically, paging and scrolling are easily possible.

Fig. 9-10 shows memory address in the case where start address is "0" and number of displayed characters is 640 (40 characters/line x 16 lines).

		L								Horiz		<u></u>	i	
_					Portzontal Orspray Fariou						ce Period	-		<del></del>
Raster	0	0	1	2 1		38 1 38	39 -39	40	41 ‡	42 ‡		62 -62	63 ‡	
Raster	11	0 40	1	42		78	39 79	40	81	42		$\overline{}$	63	
		40	41 41	1 42		78	79 79	80 1 80	‡ 81	82 \$ 82		102 102		
						118	119 119	120	121	122		142 1	143	
				•		118	119	120	121	122		142	143	<b>≨</b>
Raster	0	5 <b>6</b> 0	561 \$561 601	562 562	·	598	599 599 639	600	‡ 601	602		622 622 662	623	Vertical Display period
Raster		600 ‡				638	639	::0	1	t		t	t	
,,,,,,	••		641				679			642 682		662 702		<del></del> -
		640	1 641	642	-	l t	678	1 1	ı	t	-	t	703	
														Vertical Retrace
		720		722		758 1 758		7 <b>6</b> 0	7 <b>6</b> 1	762		782 1 782	783	period
V. Ad	g O	760	761	762		798	799 1	800 1	801 ‡	802		822	823	Ī
	4	760	761	762		798	799	800	801			822	823	$\perp$

Numb er of Horizontal Total Characters: 64 Number of Horizontal Displayed Characters: 40 Number of Vertical Total Characters: 18

Number of Vertical Displayed Characters: 16

Number of Rasters per line: 12 Vertical Total Adjust: 5

Start Address: 0

Fig. 9-10 Relation between Number of Displayed Characters and Memory Address

#### 9.7 How to Use Start Address

Start address controls the initial address of refresh memory to read out and gives an offset to refresh memory address within 14-bit.

Fig. 9-11 shows an example of paging to which start address is applied. In Fig. 9-11, there are refresh memories for 8 pages. Setting initial address of each page to start

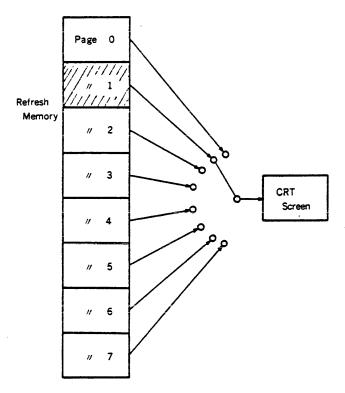


Fig. 9-11 Paging

# 9.8 How to Use Cursor Register

Cursor register is a register used to specify cursor display position on the screen and its contents are controlled by MPU. Cursor address is linear address and is itself refresh memory address of the character displayed in the cursor position.

In changing start address to  $\pm \Delta$  x for paging and scrolling, it is necessary to change cursor address to  $\pm \Delta$  x.

# 9.9 How to Use Light Pen Register

The CRTC adopts a 14-bit light pen register. When light pen detection pulse is added to LPSTB (3 pins), the values of memory address (MA<sub>0</sub>~MA<sub>13</sub>) are stored. As Light pen detection pulse is asynchronous with memory address timing, so its internal synchronization circuit makes the detection operation certain. The detection address involves the delay time of the system(from pulse output of light pen after a character is displayed on the screen and light pen detects it to LPSTB input of the CRTC), so its value needs to be corrected in software. Light pen detection address is itself refresh memory address. When cursor is moved to light pen detection position, the value corrected

address registers ( $R_{12}$ ,  $R_{13}$ ) enables to display an optional page in a moment.

Fig. 9-12 shows an example of scrolling to which start address is applied. In Fig. 9-12, changing start address periodically enables to move the data to be displayed for plural pages successively on the CRT screen.

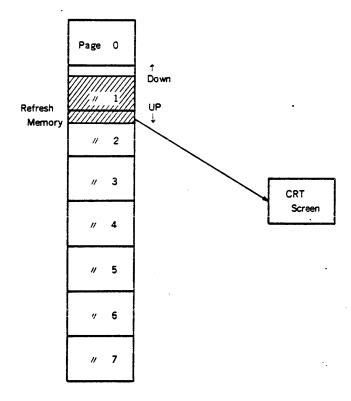


Fig. 9-12 Scrolling

in software is written into cursor register. When the character indicated by light pen is read out, the corrected value is used as refresh memory address to read out. As for frame address that light pen indicates, start address needs to be excluded from the corrected value because the corrected value is also modified with start adress.

Fig. 9-13 shows a typical example of light pen control circuit. As shown in Fig. 9-13, some external circuits enable to use light pen. There are some ways of interfacing between light pen and MPU. These are:

- (a) Interrupt Method
- (b) Program Scan Method

etc.

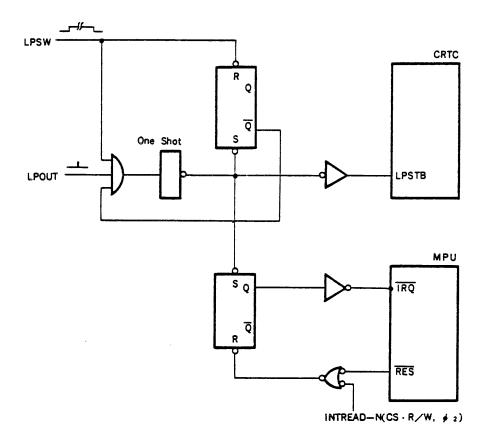


Fig. 9-13 Light Pen Control Circuit

Fig. 9-14 shows an interrupt method of interfacing. When light pen detects light, LPSTB signal and an interrupt signal  $\overline{1RQ}$  are respectively provided to the CRTC and MPU. Fig. 9-15 shows the program of this interrupt method.

Fig. 9-16 shows a program scan method of interfacing.

When LPSTB signal is provided to the CRTC, light pen sets up a detection FLAG. MPU reads out this FLAG periodically and when FLAG is "1", the contents of light pen register are read out, Table. 9-17 shows the program of this program scan method.

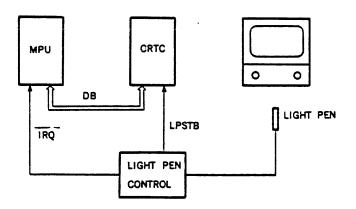


Fig. 9-14 Interfacing of Light Pen

INTERRUPT LDA A #16 LOAB LPH ADDRESS INTO ACCA STA A A0 STORE ACCA INTO ADDRESS REGISTER A0+1 LOAD LPH DATA LDA A INTO ACCA LDA B #17 LOAD LPL ADDRESS INTO ACCB STA B A0 STORE ACCB INTO ADDRESS REGISTER LDA B A0+1 LOAD LPL DATA INTO ACCB RTI RETURN FROM INTERRUPT

Fig. 9-15 Read Operation of Light Pen Register

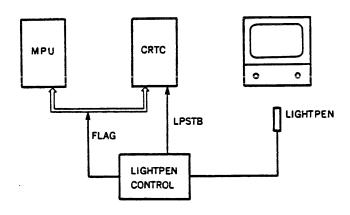


Fig. 9-16 Interfacing of Light Pen

LDA A LPFLAG LOAD LPFLAG INTO ACCA BIT BIT TEST TRY AGAIN IF LPPLAG=0 **BEQ** LOAD LPH ADDRESS INTO LDA A #16 **ACCA** STORE ACCA INTO ADDRESS STA A A0 REGISTER LOAD LPH DATA INTO ACCA LDA A A0+1 LDA B #17 LOAD LPL ADDRESS INTO **ACCB** STORE ACCB INTO ADDRESS STA B A0 REGISTER LOAD LPL DATA INTO ACCB LDA B A0+1LPFLAG CLEAR LPFLAG CLR

Fig. 9-17 Read Operation of Light Pen Register

#### 9.10 Access Method to Refresh Memory

For CRT display with the CRTC, refresh memory is accessed by CRTC's memory address (MA<sub>0</sub>~MA<sub>13</sub>) to refresh the screen periodically and also accessed by MPU in changing the contents to be displayed. As for access method by MPU, there are asynchronous access method that has no relation to the display condition and synchronous access method that avoids the display period. Fig. 9-18 shows an example of asynchronous access methods. In this case, MPU address specifies refresh memory address and the output of address multiplexer is switched over to address bus side. Therefore, a part of the screen may flash in a moment. Fig. 9-19 shows a program of asynchronous access method.

Fig. 9-20 shows an example of synchronous access methods. In this case, MPU reads out DISPTMG output of CRTC and only when DISPTMG is "Low" (horizontal and vertical retrace periods), refresh memory is accessed by MPU. In synchronous access method, there is no competition between MPU access and display access, the screen doesn't flash. Fig. 9-21 shows a program in this case.

Fig. 9-22 shows another example of synchronous access methods. In this case, a character time is devided into MPU access time and display access time. In MPU access, time MPU is synchronized by stretching MPU clock  $\phi_2$  by  $\overline{READY}$  signal till its access is finished. Fig. 9-23 shows a program of this case.

Moreover, as there are many other access methods including these typical examples, the most reasonable method should be selected according to each system.

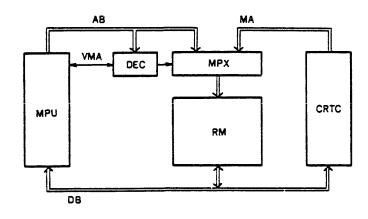


Fig. 9-18 Asynchronous Access to RM

STA A RM STORE ACCA INTO RM LOCATION

LDA A RM LOAD RM LOCATION INTO ACCA

Fig. 9-19 Program of Asynchronous Access to RM

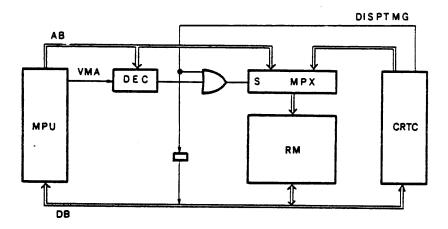


Fig. 9-20 Synchronous Access to RM (1)

LOAD DISPTMG INTO ACCA LDA A DT BIT TEST BIT A #1 **★**-5 TRY AGAIN IF DT=1 STORE ACCB INTO RM LOCATION RM STA B LDA A LOAD DISPTMG INTO ACCA DT BIT A #1 BIT TEST BEQ **\***−5 SKIP IF ACCA=0 RM LOAD RM LOCATION INTO ACCB LDA B

Fig. 9-21 Program of Synchronous Access to RM(1)

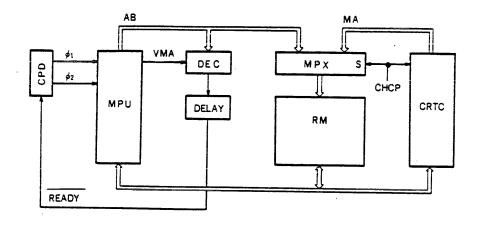


Fig. 9—22 Synchronous Access to RM (2)

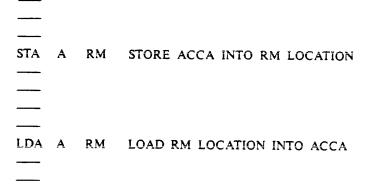


Fig. 9-23 Program of Synchronous Access to RM(2)

#### 10. Program of the CRTC

#### 10-1 READ WRITE Operation of Internal Registers

As shown in Table. 6-1, the CRTC has 18 internal registers and 1 address register that specifies address of these registers.

Therefore, READ WRITE operation of internal registers should be done through 2 steps in a pair.

STEP 1: Register address is written into address register by STORE command.

STEP 2: The contents of the specified register are read by LOAD command, or are written into the specified register by STORE command.

READ WRITE procedure of internal registers is shown in Fig. 10-1 and an example of its program is shown in Fig. 10-2.

When address register is accessed, it is necessary to assign address so that RS may be "Low"(pin 24). When an internal register is accessed, it is necessary to assign address so that RS may be "High".

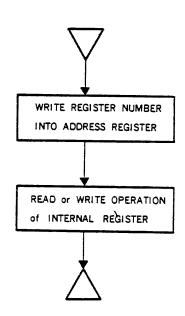


Fig. 10—1 READ/WRITE Procedure of Internal Register

LDA STA LDA	A A A	=15 Ao Ao-1	LOAD REGISTER NUMBER INTO ACCA STORE ACCA INTO ADDRESS REGISTER LOAD CURSOR LOWER BYTE INTO ACCA
LDA	Α	#15	LOAD REGISTER NUMBER INTO ACCA
STA	Α	Ao	STORE ACCA INTO ADDRESS REGISTER
LDA	A	DATA	LOAD WRITE DATA INTO ACCA
STA	Α	A <sub>0+1</sub>	STORE ACCA INTO CURSOR LOWER BYTE
			REGISTER

Fig.10-2 READ/WRITE Program of Internal Register

#### 10.2 Initializing Program of the CRTC

For desirable display control function of the CRTC, it is necessary to initialize 16 internal registers except

light pen register after the system power supply is established by power on.

Fig.10-3 shows a flow chart of initializing program and Fig.10-4 shows the program based on this flow chart. In this example, the number of program steps is decreased by looping the program, storing the initializing data in order of register address in a table.

Table.10-1 shows an example of initializing values for character display. In this case, there no paging and scrolling. So start address should be always "O". Cursor's initializing position shall be usually in home position, though it can be anywhere within valid memory address of system( $0\sim639$  in Table.10-1).

When cursor address is out of valid memory address, it is necessary to be careful because cursor display position is not guaranteed. Table. 10-3 and Table. 10-4 show an example of initializing values for full graphic display.

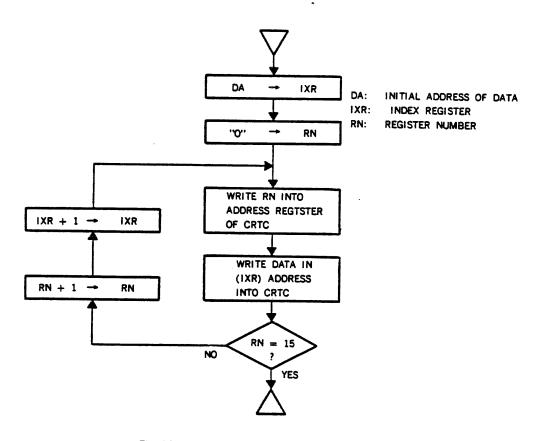


Fig. 10-3 Initializing Flow Chart of The CRTC

	LDX		#DA	LOAD DATA ADDRESS INTO INDEX		STA	В	A <sub>0+1</sub>	STORE ACCB INTO CRTC REGISTER
				REGISTER		CMP	Α	#15	
	CLR	A		CLEAR ACCA		BEQ		ILR <sub>2</sub>	BRANCH IF COMPLETE
ILRI	STA	A	A <sub>0</sub>	STORE REGISTER NUMBER INTO ADDRESS		INC	Α		INCREMENT ACCA
				REGISTER		INX			INCREMENT INDEX REGISTER
	LDA	В	0,X	LOAD INITAL DATA INTO ACCB		BRA		$ILR_i$	BRANCH TO ILRI
					ILR <sub>2</sub>				

Fig. 10-4 Initializing Program of the CRTC

Table.10-1 Specification of Character Display(Example)

Item	Specification
Scan Mode	Non-Interlace
Horizontal Deflection Frequency	15,625 KHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot (Horizontal x Vertical)	8 x 12
Number of Displayed Characters (Row x Line)	40 x 16
HSYNC Width	4 μs
Cursor Display	Raster 9~10, Blink:16Field Period
Paging, Scrolling	

Table.10-2 Initializing Values for Character Display

Register No.	Name	Initializing Value (Decimal)
R <sub>0</sub>	Horizontal Total	63
$R_1$	Horizontal Displayed	40
R <sub>2</sub>	Horizontal Sync Position	52
R <sub>3</sub>	Horizontal Sync Width	4
R <sub>4</sub>	Vertical Total	20
Rs	Vertical Total Adjust	8
R <sub>6</sub>	Vertical Displayed	16
R <sub>7</sub>	Vertical Sync Position	19
R <sub>8</sub>	Interlace Mode	0
R <sub>9</sub>	Maximum Raster Address	11
R <sub>10</sub>	Cursor Start Raster	73
R <sub>11</sub>	Cursor End Raster	10
R <sub>12</sub>	Start Address (H)	0
R <sub>13</sub>	Start Address (L)	0
R <sub>14</sub>	Cursor (H)	0
R <sub>15</sub>	Cursor (L)	0

Table.10-3 Specification of Full Graphic Display (Example)

Item	Specification
Scan Mode	Non-Interlace
Horizontal Deflection Frequency	15,625 KHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot (Horizontal x Vertical)	8 x 8
Number of Displayed Characters (Row x Line)	32 x 24
Number of Display Dot(Horizont- al x Vertical)	256 x 192
HSYNC Width	4 µš
Cursor Display	_
Paging, Scrolling	· <del>-</del>

Table.10-4 Initializing Values for Full Graphic Display

Register No.	Name	Initializing Value (Decimal)
R <sub>0</sub>	Horizontal Total	63
$R_1$	Horizontal Displayed	32
R <sub>2</sub>	Horizontal Sync Position	47
R <sub>3</sub>	Horizontal Sync Width	4
R <sub>4</sub>	Vertical Total	31
R <sub>5</sub>	Vertical Total Adjust	4
R <sub>6</sub>	Vertical Displayed	. 24
R <sub>7</sub>	Vertical Sync Position	28
R <sub>8</sub>	Interlace Mode	0
R <sub>9</sub>	Maximum Raster Address	7
R <sub>10</sub>	Cursor Start Raster	_
R <sub>11</sub>	Cursor End Raster	-
R <sub>12</sub>	Start Address (H)	0
R <sub>13</sub>	Start Address (L)	0
R <sub>14</sub>	Cursor (H)	_
R <sub>15</sub>	Cursor (L)	_

#### 10.3 Program of Paging

As shown in Fig.9-11, paging is to select a desired page from refresh memories for plural pages. Fig.10-5 shows a flow chart of paging. In this example, input for selecting a page is derived from page KEY. This is a very easy program where initial address of refresh memory corresponding to the selected page is set to start address register.

Then, as shown in 9.8, cursor address should be modified by the same number which start address is changed by.

#### Internal Registers of the CRTC

Regis	Name	Hexadecim -al			I	Data	а В	it			Range of
-ter No.		Programmed Values of AR	7	6	5	4	3	2	ı	0	Programme -d-Values
AR	Address Register	_	X	X	X	!	1				0~17
R₀	Horizontal Total	, 00					1				0~255
$R_1$	Horizontal Displayed	01					į				0~255 *
R <sub>2</sub>	Horizontal Sync Position	02									0~255 *
R <sub>3</sub>	Horizontal Sync Width	03	X	X	X	X					0~15
R <sub>4</sub>	Vertical Total	04	X				i				0~127
R <sub>5</sub>	VERTICAL Total Adjust	05	X	X	X						0~31
R <sub>6</sub>	Vertical Displayed	06	X					٠			0~127 *
R <sub>7.</sub>	Vertical Sync Position	07	X	1							0~127 *
R <sub>8</sub>	Interlace Mode	08	X	X	X	X	X	X	٧	S	0~3
R <sub>9</sub>	Maximum Raster Address	09	X	X	X	X					0~31
R <sub>10</sub>	Cursor Start Raster	0A	X	В	P						0~4 0~31 Bit *
Rii	Cursor End Raster	0B	X	X	X						0 31 *
R <sub>12</sub>	Start Address (H)	0C	X	X							0~
R <sub>13</sub>	Start Address (L)	0D		İ		:					16383
R <sub>14</sub>	Cursor (H)	0E	X	X							0~
R <sub>15</sub>	Cursor (L)	0F									16383
R16	Light Pen (H)	. 10	X	X							
R17	Light Pen (L)	11									177

<sup>\*</sup>These values shall be programmed according to restriction shown in next page.

#### Interlace Mode

V	S	M ode
0	0	Non-Interlace Mode
1	0	Non-interface Mode
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

#### Cursor Display

В	Р	Display Mode
0	0	Non-Blink
0	Ī	Non-Display
1	0	Blink, 16 Field Period
1	ı	Blink, 32 Field Period

Restriction On Programmed Values of the CRTC Programmed values of the CRTC internal registers shall be restricted like the followings:

- i)  $0 < N_{hd} < N_{ht} + 1 \le 256$
- ii)  $N_{ht}$ : Odd Number (in the case of interlace sync mode or interlace sync & video mode)
- iii)  $0 < N_{vd} < N_{vt} + 1 \le 128$
- $iV) N_{hsp} + N_{hsw} < N_{ht} + 1$
- $V) N_{vsp} \leq N_{vt}$
- Vi)  $0 \le N_{CSTART} \le N_{CEND} \le N_r$
- Vii) In the case of interlace sync & video mode, either of the followings shall be selected.
  - (1) Nostart, Noend : Even Number
  - (2) NCSTART, NCEND: Odd Number

Meaning of Symbols in i) ~ Vii).

Values of

Registers

Nht : (Number of Horizontal Total

Characters) - 1

N<sub>hd</sub>: Number of Horizontal Displayed

Characters

Programmed N<sub>vt</sub> : Number of Vertical Total

Characters) - 1

N<sub>vd</sub>: Number of Vertical Displayed
Characters

Nhsp: (Horizontal Sync Position) - 1

N<sub>vsp</sub>: (Vertical Sync Position) - 1

NCSTART: Cursor Start Raster Address

NCEND : Cursor End Raster Address

Nr : Maximum Raster Address

### **ABBREVIATIONS**

AB Address Bus

AR Address Register

CG Character Generator

CLĶ Clock

CMP Comparator

CRT Cathode Ray Tube

CRTC Cathode Ray Tube Controller

CUDISP Cursor Display

DB Data Bus

DEC Decoder

DISPTMG Display Timing

HSYNC Horizontal Synchronization

LPSTB Light Pen Strobe

MA Refresh Memory Address

MPU Micro Processor Unit

MPX Multiplexer

RA Raster Address

RM Refresh Memory

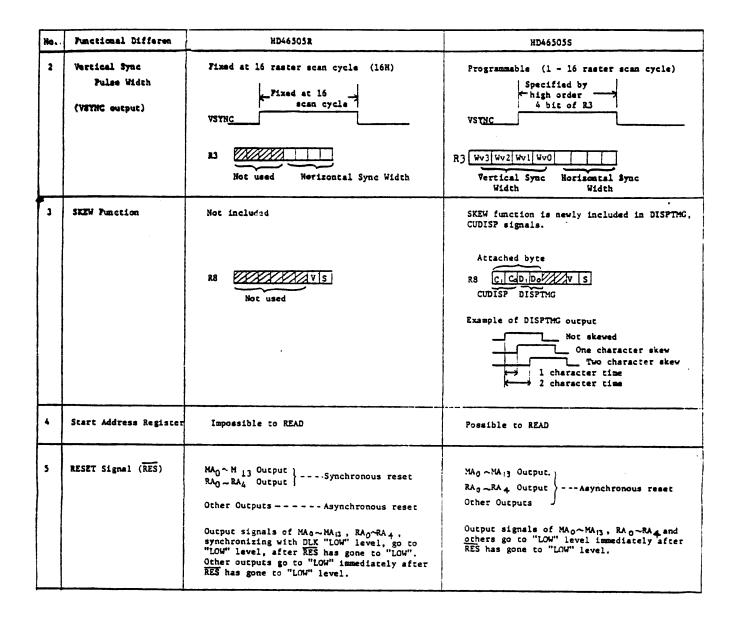
RS Register Select

VSYNC Vertical Synchronization

P→S Parallel-Serial Converter

Table of Functional Differences between HD46505R and HD46505S

No.	- Punctional Difference		HD46505R	#D46505s				
1	Interlace	Programming	Character line address	Character line address				
	Sync  & Video Hode Display	Method of number of vertical	Programming unit for number of vertical characters	1 unit for number of vertical				
		In HD46505R, number of characters is vertica-						
			iliustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure	lly programmed in unit of one line, as illustrated above. (Number of vertical fotal characters, Number of vertical displayed characters, Vertical Sync Position)  Example of above figure				
			Programmed number into Vertical Displayed Register = 5	Programmed number into Vertical Displayed Register = 10				
		Number of Taster per character	Only even number can be specified.	Both even number and odd number can be specified.  Character Character				
		line	Number of raster  Number of raster  Number of raster  Number of raster 10 scanline (specified)	0   line address   line address   2				
			Howerver, number which is programmed into register is caluculated as follows.  Programmed number (Nr)	When number of raster When number of raste per character line is per character line EVEN. is ODD.				
			<ul><li>(Number specified) - 1</li><li>.</li></ul>	Number of raster Number of raster = 10 scan line = 9 scan line (specified) (specified)				
			·	However, number which is programmed into register is caluculated as follows.  Programmed number (Nr)  = (Number specified) - 2				
	Cursor Display		Cursor is displayed in either EVEN field or ODD field.	Cursor is displayed in both EVEN field and ODD field.				
			2	EVEN number				
		-	2 - ○ ○ ○ ○ ○ ○ - 3 ← ODD number - ○ ○ ○ ○ ○ - 9 ← ODD number	2				
				0				



. Table of Characteristic Difference between HD46505R and HD46505S

No.	Characteristic Difference		HD46505R						
Ņ.	Characteristic Difference	Symbol	min	typ	ma x	min	typ	Max	Unit
1	Clock Cycle Time	teyee	330			270			ne
2	Clock Pulse Width "High"	PW <sub>CH</sub>	150	_		130			ns
3	Clock Pulse Width "Low"	PW <sub>CL</sub>	150			1 30			na
4	Rise and Fall Time for Clock Input	T <sub>CR</sub> ,T <sub>CF</sub>			15			20	ne
5	Horizontal Sync Delay Time	THSD			250			200	ns
6	Light Pen Strobe Pulse Width	PW <sub>LPH</sub>	80			60			ns
7	Light Pen Strobe Uncertain Time of	T <sub>LPD1</sub>			80			70	na -
	Acceptance	TLPD2			10			0	n.s

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our service to you are customer.						
NAME:	COMPANY:					
ADDRESS:	PHONE:					
DATE PRODUCT RECEIVED:	LOCAL MATROX REP:					
PRODUCT IDENTIFICATION  Each Matrox board or module has a paper label similar the right. Please fill in this box with the information of the silk screen one of our boards (as opposed to a module), please frank print it in the space provided to the right.  CUSTOM	on on the label.	TYPE : DATE : SER. NO. : CUST. : STS : A T B F S  Matrox Electronic Systems Ltd. MADE IN CANADA  WRITE SILK SCREEN DO6				
1. Did the product work when first tried?  UMES  NO	8.	What is your end product, and what stage of development is it at?				
2. Why did it not work?  Damaged in shipment Insufficient documentation Poor documentation Poor product design Don't know	9.	☐ Prototype ☐ In Production ☐ ☐  What is the product's software environment? (Monitor, operating system etc)				
3. Did you call Matrox for technical support?  YES  NO						
4. If yes, how do you rate our technical support?    Excellent   Good   Average   Poor	10.	What is the product's hardware environment? (CPU, Memory, Display Characteristics)				
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7. How did you find out about Matrox?  Magazine advertisement Trade Show Word of Mouth	11.	What additional products would you like to see Matrox develop?				



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NAME OF UNIT:
MODEL NO.(on silkscreen): SERIAL NO.(on label):
DATE UNIT RECEIVED: DATE UNIT FAILED: OR DEAD ON ARRIVAL [].
MEMORY BASE ADDRESS USED: I/O BASE ADDRESS USED:
PLEASE DESCRIBE THE SYSTEM THAT THE UNIT IS USED IN (CPU,BUS,MEMORY,ETC.):
UNIT CONFIGURATION (50 or 60 Hz, attributes used, display resolution selected, etc.):
FAULT IS CONSTANT [] FAULT IS INTERMITTENT [] PLEASE DESCRIBE THE FAULT:
THE FOLLOWING SPACE IS FOR FACTORY USE ONLY
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