

MLSI-KPV11

**POWER FAIL
DETECTOR/LTC MODULE**

**For use with DEC™ LSI-11™ Computers
INSTRUCTION MANUAL**

MDB SYSTEMS, INC.

MLSI-KPV11
POWER FAIL
DETECTOR/LTC MODULE

For use with DECTM LSI-11TM Computers
INSTRUCTION MANUAL



1995 North Batavia Street
Box 5508
Orange, CA 92267-0508
(714) 998-6900
TWX 910-593-1339

Document Part Number: 80040338
Document Revision Level: A
Product Revision Level: C

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The postage-prepaid READER'S COMMENTS page at the end of this instruction manual requests the user's critical evaluation to assist us in preparing future documentation.

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Price: \$10.00

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LIST OF DRAWINGS AND SCHEMATICS

NUMBER

- 44040338 SCHEMATIC DIAGRAM: MLSI-KPV11
45040338 ASSEMBLY DRAWING: MLSI-KPV11

INTRODUCTION

This is a preliminary technical manual for the MDB MLSI-KPV11 Power Fail Detect/LTC module to be used with Digital LSI-11 Q-bus computers.

PRODUCT DESCRIPTION

The MLSI-KPV11 is a dual-size Power Failure Detector/Line Time Clock module which is provided with removable/pluggable bus terminators. The bus terminators are 120 ohm impedance packs, which can be replaced with 220 ohm impedance packs or removed completely. The MLSI-KPV11 is furnished with 22-bit bus termination (BDAL0 - BDAL21).

The programmable Line Time Clock (LTC) feature is switch selectable to provide PDP-11/03, SMU, or KW11-L compatibility. The feature allows the user to enable or disable interrupts under program control. The MLSI-KPV11 has 4-level interrupt capabilities when used as a KW11-L compatible module. The DEC KPV11 has 1-level interrupt only. External clock capabilities are also provided.

The MLSI-KPV11 is functionally equivalent to the DEC KPV11-A, -B, and -C. The KPV11-A provides power failure detection and a Line Time Clock only; the KPV11-B provides power failure detection/LTC and 120 ohm bus termination; and the KPV11-C provides power failure detection/LTC and 220 ohm bus termination. However, the DEC modules have only 18-bit bus termination, whereas the MDB module terminates 22 bits.

The main differences between the MDB and DEC modules relate to the type of connectors on the modules, and the use of these connectors.

The DEC KPV11 utilizes three spade lugs for connection to a 24VAC source. The 24VAC source provides the 50 or 60 Hz reference for the Line Time Clock function and is the power fail monitor signal for the power sequence circuit.

The MDB MLSI-KPV11 utilizes a Molex-type connector for connection to the required 24VAC source. The output voltage source should come from a 24VAC center tap transformer and can be connected to J2 on the module. Since the MLSI-KPV11 utilizes a Molex-type connector, an existing DEC cable cannot be directly connected to the MDB module without first changing the connectors on the cable. A mating connector and pins for the MDB connector is supplied with each MLSI-KPV11 to allow the user to make the necessary modification.

The DEC KPV11 contains a berg connector that is used when the module is connected by a DEC cable to the DEC Console Control and Indicator Panel. The MDB module utilizes a different type of connector that is not compatible to the DEC cable. Moreover, the DEC Control Panel contains circuitry that is also on the MDB MLSI-KPV11. Therefore, the MDB module cannot be used with the DEC Control Panel.

A programmed shorting plug (MLSI-KPV-JMPR), inserted into the berg connector, is also provided with the MLSI-KPV11. This plug straps the board for circuits to function properly when a switch panel is not connected. When inserted, the DC ON circuitry is enabled and the LTC and HALT circuitry is disabled. Changing connections on the shorting plug can allow the LTC to be enabled.

INSTALLATION

The MLSI-KPV11 may be installed in the last slot of the backplane, or it may be installed in any slot after the last functioning module. If it is installed in the last slot of the backplane, Bus Grant Continuity Cards (MLSI-BGC) must be placed in the A or C portion only of all vacant (normal Q-bus wired) slots between the MLSI-KPV11 and the last functioning module. (Bus Grant Cards are not required in Slots 6-C and 7-C when an MLSI-BPA84-A type backplane/card guide is utilized, as standard Q-bus signals are not present on slots 6 C-D and 7 C-D.)

For additional information on the KPV11 module, refer to the DEC Memories and Peripherals Handbook, 1978-79.

JUMPER AND SWITCH SETTINGS

Select the appropriate interrupt level as follows:

TABLE 1
INTERRUPT LEVEL FOR LINE TIME CLOCK INTERRUPT

	5 J-H	3 J-H	6 J-H	4 J-H
LEVEL 4	•	○	○	○
LEVEL 5	•	•	○	○
LEVEL 6	•	○	•	○
LEVEL 7	•	○	•	•

• = Jumper Removed
○ = Jumper Installed

NOTE: The MLSI-KPV11 is factory configured for Interrupt Level 4.

The Interrupt Vector Address of the Line Time Clock Interrupt is 100_8 . This address cannot be changed.

The Device Address Switch Register (SWR) is 777570_8 .
The Device Address Line Time Clock Status (LKS) is 777546_8 .

The Device Address SWR and LKS cannot be changed.

Jumpers to enable or disable the Switch Register and Line Clock Status are as follows:

SWR OUT SWRO = 10 J-H

SWR IN SWRI = 12 J-H

LKS OUT LKSO = 13 J-H

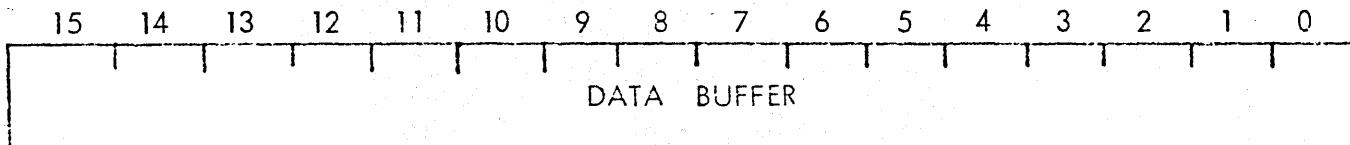
LKS IN LKSI = 11 J-H

The register is enabled when the jumper is installed.
The register is disabled when the jumper is removed.

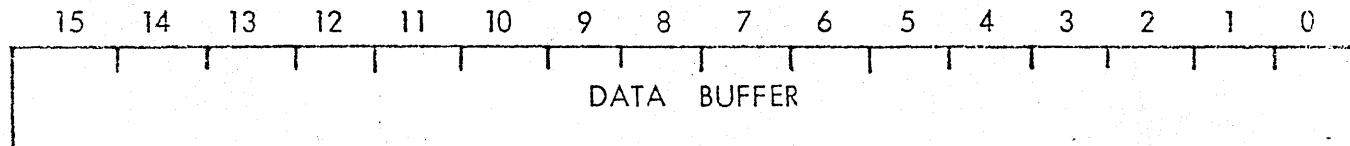
REGISTER ASSIGNMENTS

FIGURE 1
REGISTER ASSIGNMENTS

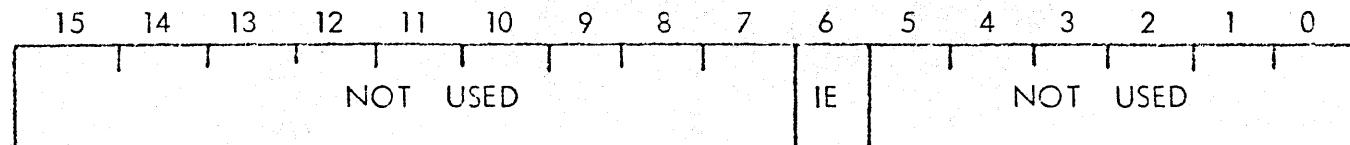
SWITCH REGISTER = SWR0 = 777570₈ WRITE ONLY



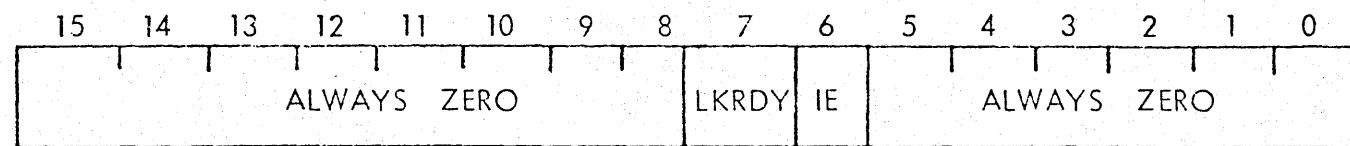
SWITCH REGISTER = SWR1 = 777570₈ READ ONLY



LINE CLOCK STATUS = LKSO = 777546₈ WRITE ONLY



LINE CLOCK STATUS = LKSI = 777546₈ READ ONLY



IE = LINE TIME CLOCK INTERRUPT ENABLE
LKRDY = LINE TIME CLOCK INTERRUPT READY

ADDITIONAL JUMPERS

Install additional jumpers on the MLSI-KPV11 for appropriate applications as specified in Table 2.

TABLE 2

ADDITIONAL JUMPERS

JUMPER	APPLICATION
1 J-H	Install to terminate BDMGOL
2 J-H	Install for EXTCLK 2
2 J-K	Install for EXTCLK 1
7 J-H	Install to terminate BDMGIL
8 J-H	Install to assert BSACKL when RPLY, SYNC, and BDMGI are asserted
9 J-H	Install if using LTC for clock
9 J-K	Install when using EXTCLK 1 or EXTCLK 2 for clock
14 J-H	Install to always enable clock
14 J-K	Install for DCON to enable ACOK
15 J-H	
15 L-K	Configured for desired outputs at Test Points PSON 1 and PSON 2 (For remote DC power on)
15 L-M	
16 L-M	Install to enable BEVNTL
16 J-K	Install to allow BEVNTL when LKIEN is set
16 J-H	Install to allow BEVNTL when LTC switch is enabled

PIN CONNECTIONS

Tables 3 and 4 list the Q-bus signals present on each pin of the P1 and P2 connectors. Figure 2 shows the strapping arrangement of the programmed shorting plug (MLSI-KPV-JMPR) which mates with the MLSI-KPV11 and allows the circuits on the board to function properly when a switch panel is not connected.

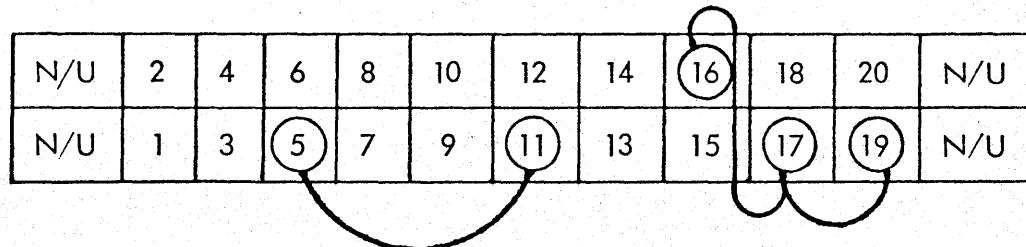
TABLE 3
P1 CONNECTIONS

PIN #	BUS SIGNAL
1	BPOKH
2	BEVNTL
3	SRUNL
4	EXTCLK 2
5	GND
6	DCOK
7	RUNLIT
8	N/C
9	BHALTL
10	BDCOKH
11	HALT OFF
12	HALT ON
13	+5VDC
14	HALT
15	LTC
16	GND
17	LTC OFF
18	LTC ON
19	DC ON
20	DC OFF

TABLE 4
P2 CONNECTIONS

PIN #	BUS SIGNAL
1	AC1
2	GND
3	GND
4	AC2

FIGURE 2
MLSI-KPV11 SHORTING PLUG (MLSI-KPV-JMPR)



MAINTENANCE

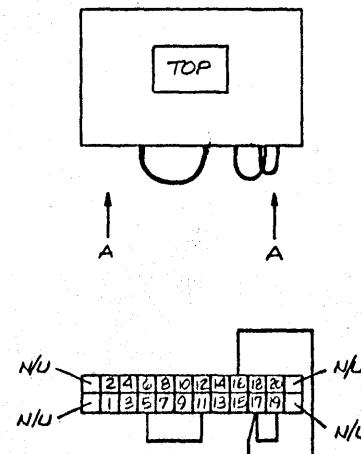
In the event of apparent malfunction, refer to the assembly drawings and logic diagrams contained in this manual. Check to be sure that connectors are seated properly.

Repair the module using appropriate skills, techniques, and materials. If you wish MDB Systems to repair the module, contact MDB Systems' Customer Service Department and request a Return Material Authorization (RMA). Once return authorization is granted, pack the module carefully, along with your best evaluation of trouble symptoms, and ship it, prepaid, to MDB Systems, Inc.

DRAWINGS

The following pages contain logic diagrams and assembly drawings useful in maintaining and repairing the module.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		A RELEASE TO PRODUCTION 3-9-82 Jm ECO NO. 1743		
		B ECO NO. 1912 5-11-82 Jm		
		C ECO NO. 2138 9-29-82		



NOTE:

1. THE PARTS LIST IS FOR REFERENCE ONLY
2. LABEL CONNECTOR "TOP" AS SHOWN

REF PARTS LIST			
ITEM NO	DESCRIPTION	PART NO	QTY
1	CONN, BERG 24 PIN	65043-025	1
2	CONTACTS	47745	5
3	WIRE, .26AWG, STRD/GRN		4'

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CITY NEED	FROM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION
			PARTS LIST		
			CONTRACT NO.	MDB SYSTEMS, INC.	
UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES TOLERANCES ARE .005 FRACTIONS DECIMALS ANGLES IN DEG SEC MATERIAL			APPROVALS	DATE	MLSI-KPV-JMPR
			DRAWN	J MCNEILLY 5-9-82	
FINISH			CHECKED	3-8	SIZE FSCM NO. C 51648
NEXT ASSY			ISSUED		DWG. NO. 50049200-000 C
USED ON			APPLICATION	DO NOT SCALE DRAWING	SCALE SHEET 1 OF 1

8

7

6

5

4

3

DWG. NO. 44040338 SH 1 REV C

1

REVISIONS			
ZONE	REV.	DESCRIPTION	DATE
A		ECO NO. 1191	8-81
B		ECO NO. 1404	11-9-81
B1		ECO NO. 1453	12-2-81
B2		ECO NO. 1470	12-10-81
B2		RELEASE TO PRODUCTION ECO NO. 1475	12-28-81
B3		ECO NO. 1754	3-10-82
B4		ECO NO. 1961	5-27-82
C		ECO NO. 2106	8-16-82
C		RELEASE TO PRODUCTION ECO NO. 2241	12-28-82

D

D

C

C

B

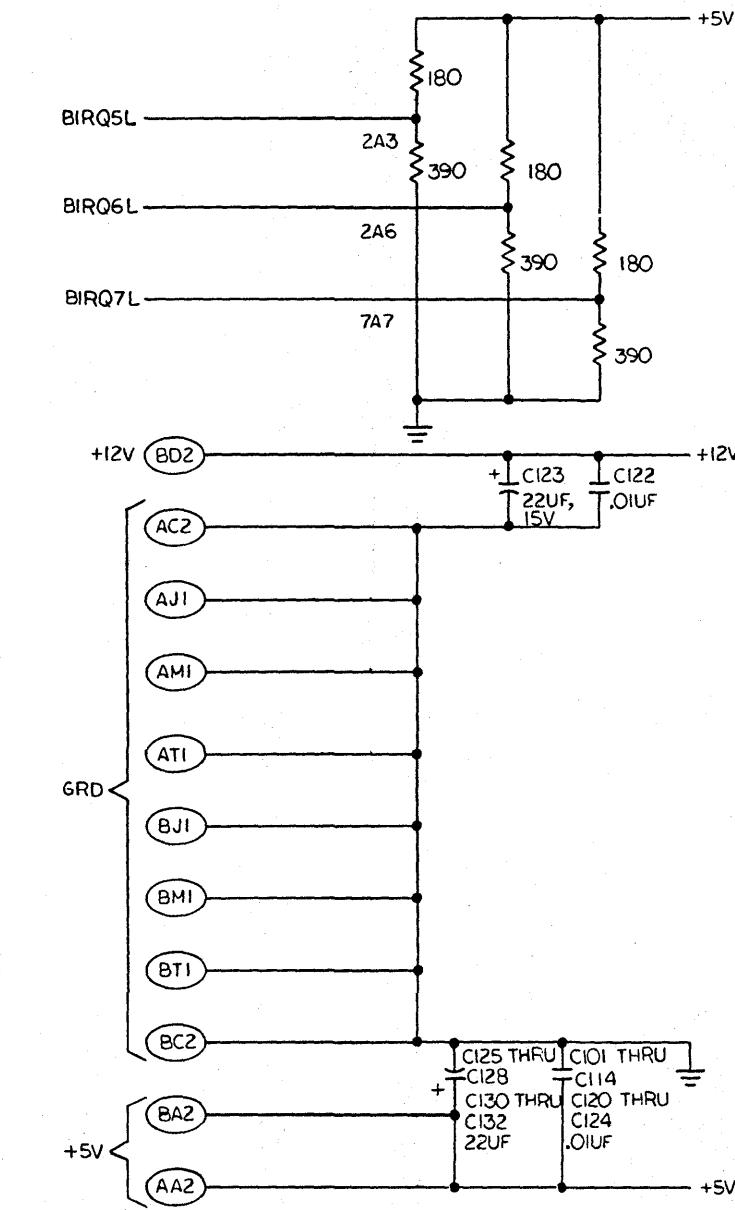
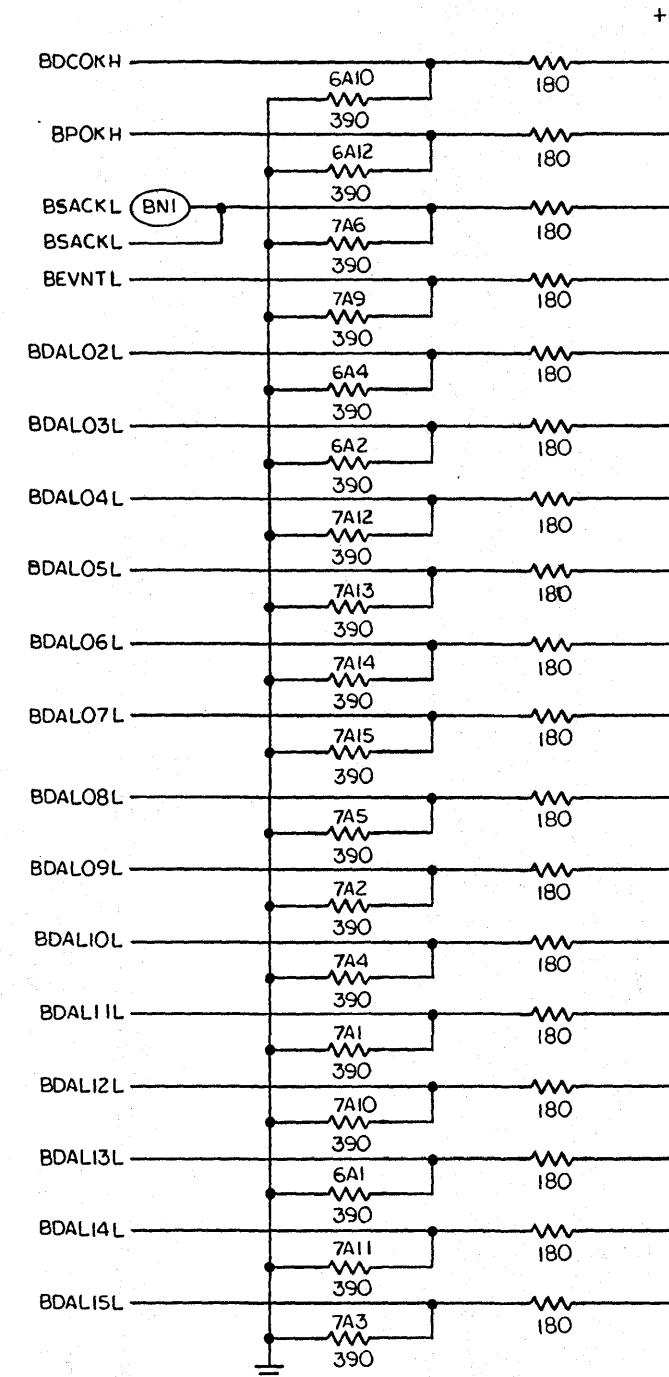
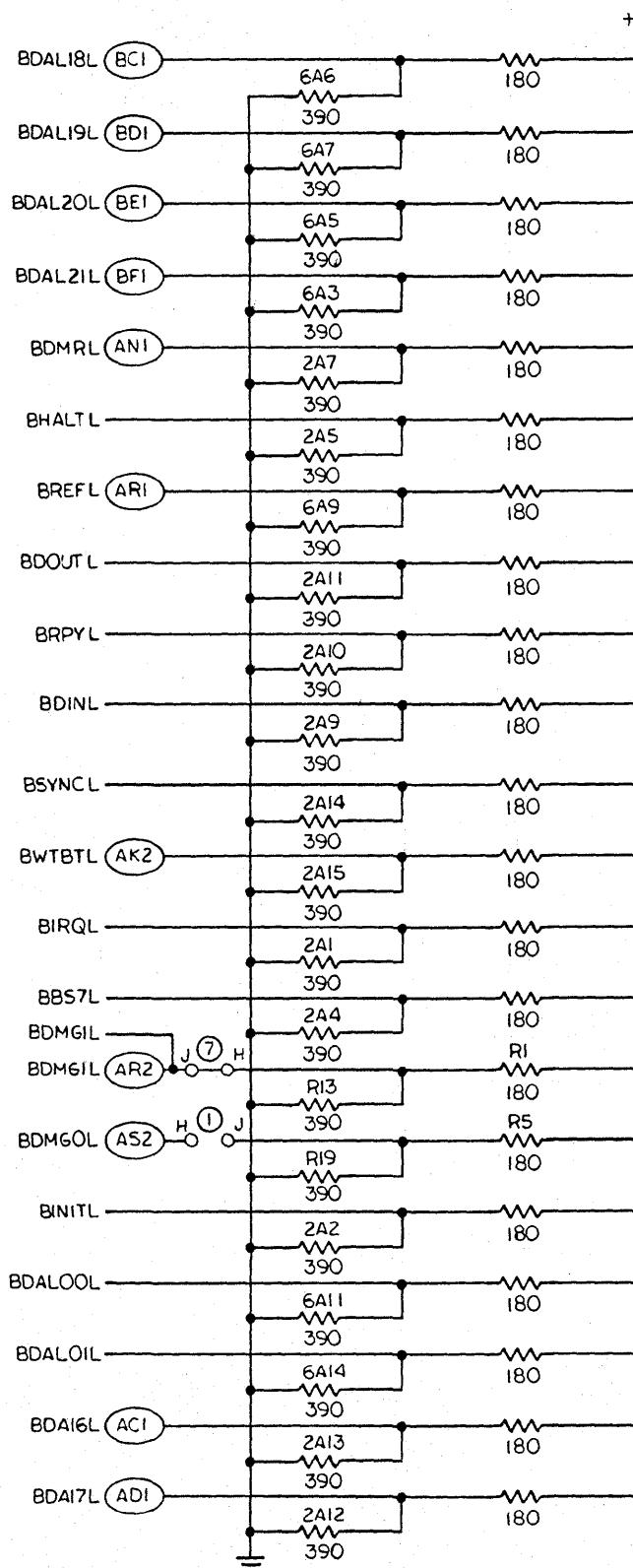
B

A

A

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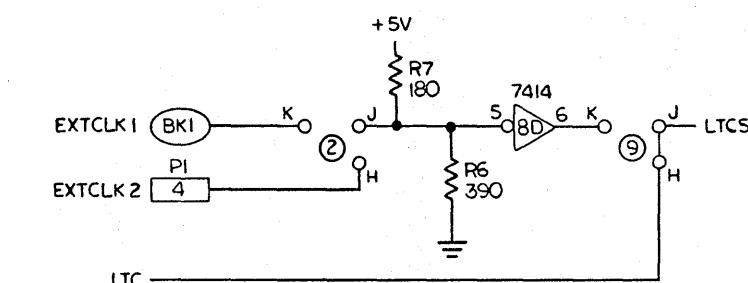
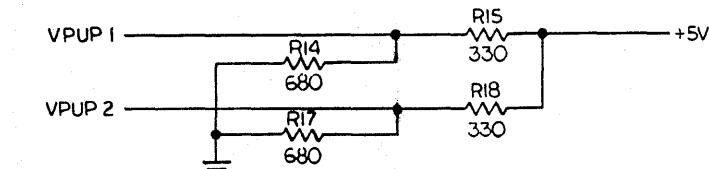
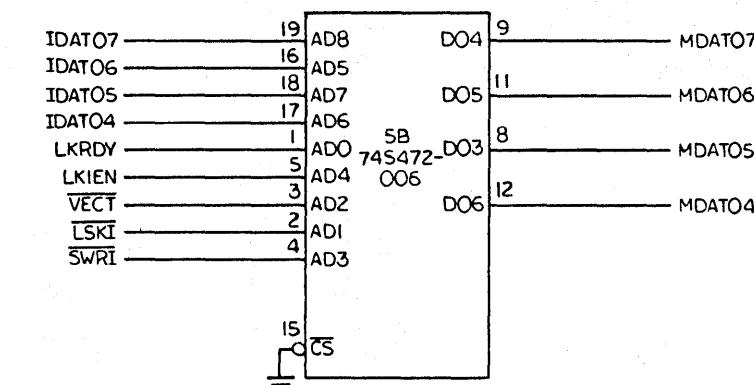
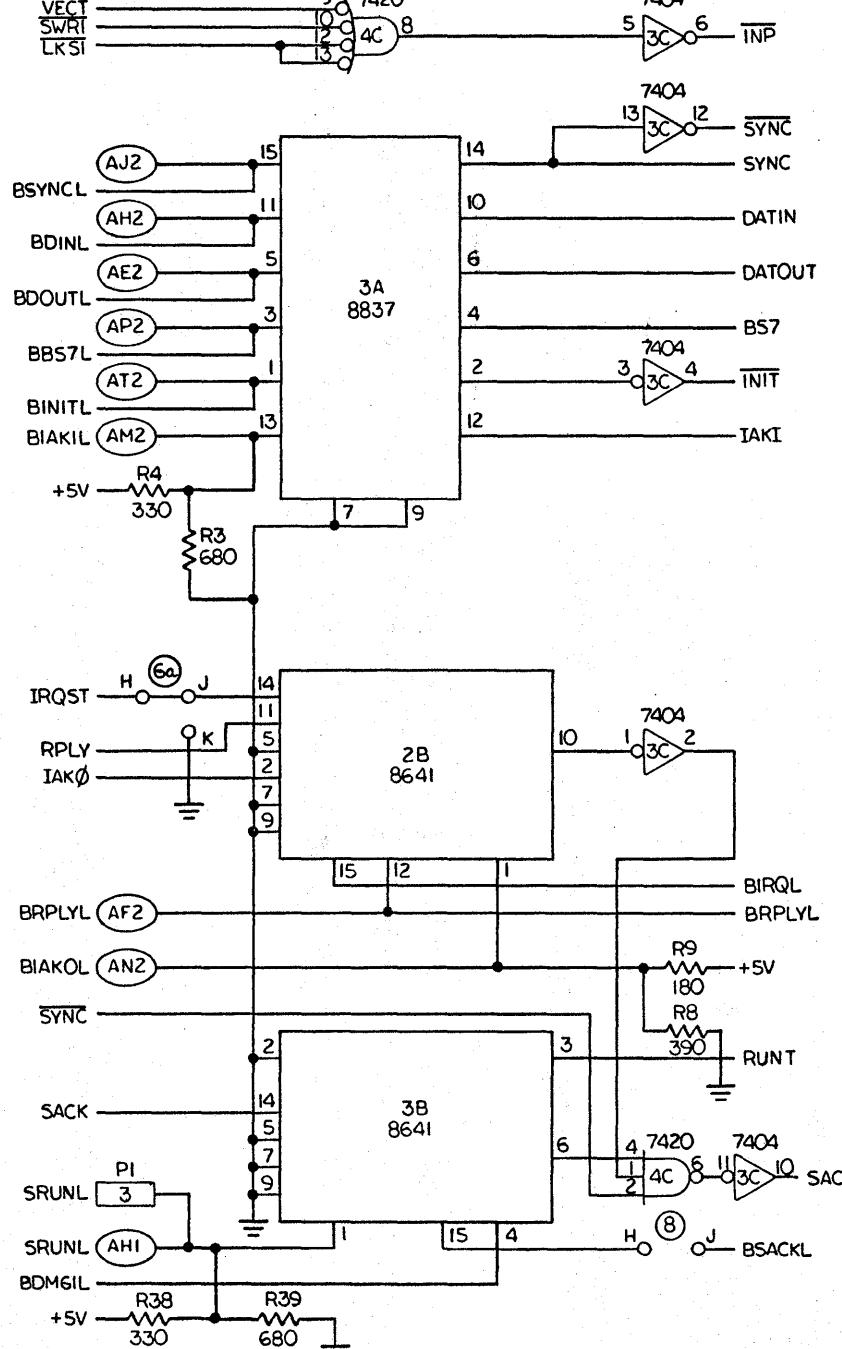
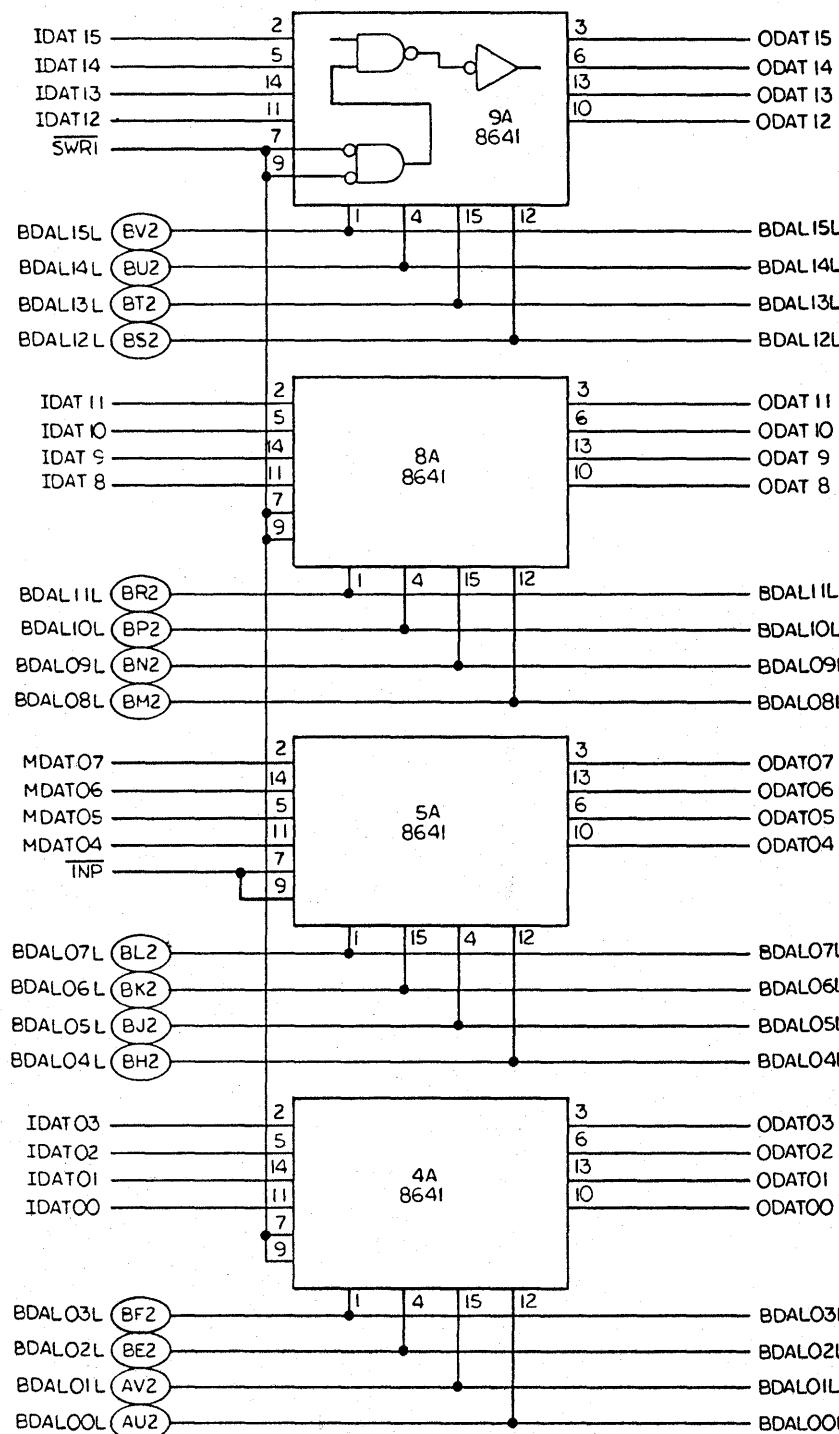
QTY REQ'D	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION
PARTS LIST					
			CONTRACT NO.		MDB SYSTEMS, INC.
					MLSI - KPVII
			APPROVALS	DATE	
			DRAWN JAY MCNEILLY	8-81	
			CHECKED		
			ISSUED <i>Jay</i>	8-81	SIZE FSCM NO. DWG. NO.
					D 51648 44040338 REV C
			SCALE		SHEET 1 OF 5



NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS VALUES ARE IN OHMS AND ARE 1/4 WATT

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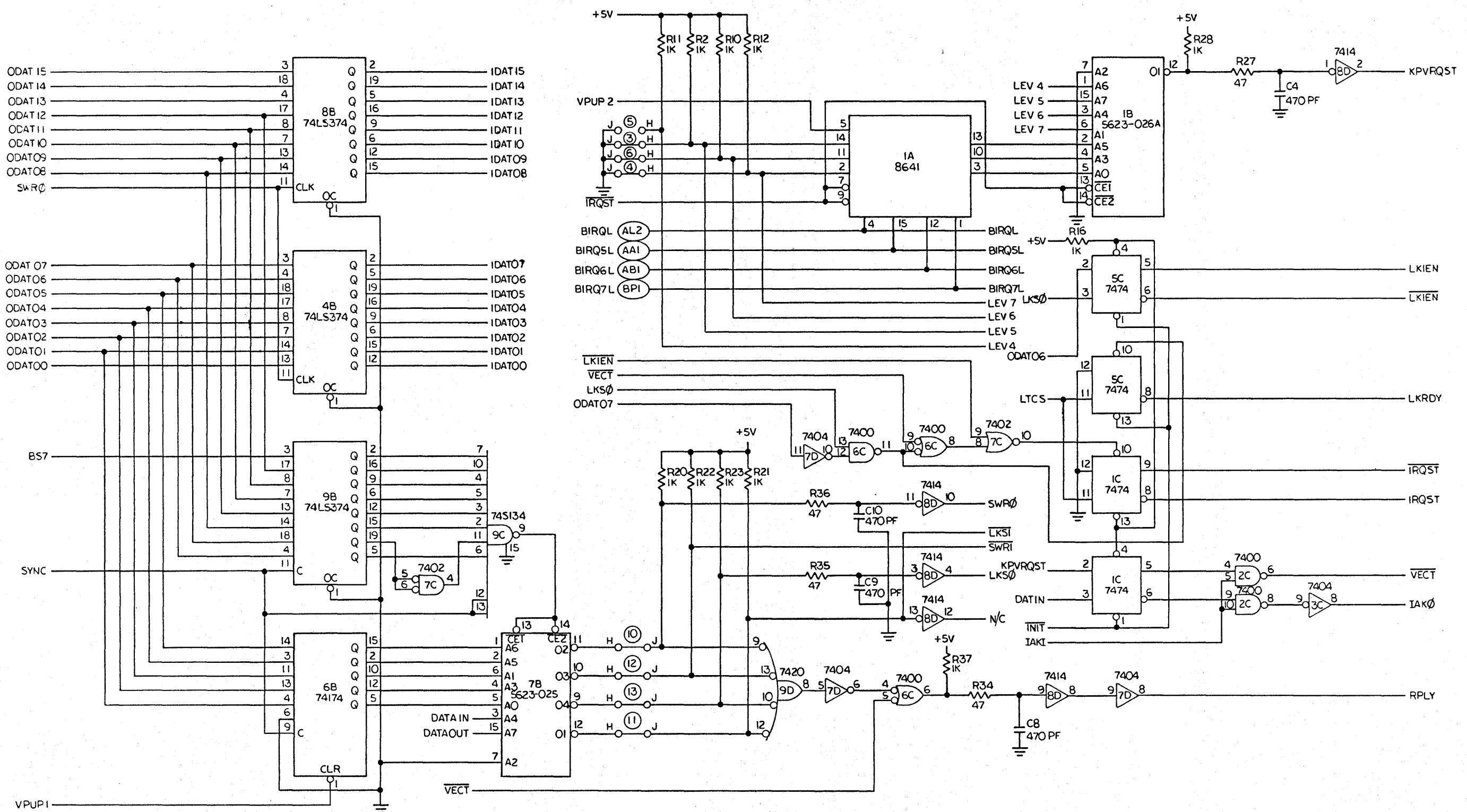
MDB SYSTEMS, INC.		SIZE FSCM NO.	DWG. NO.
DRAWN	J. MC.	D 51648	44040338
ISSUED	<i>[Signature]</i>	SCALE	REV C



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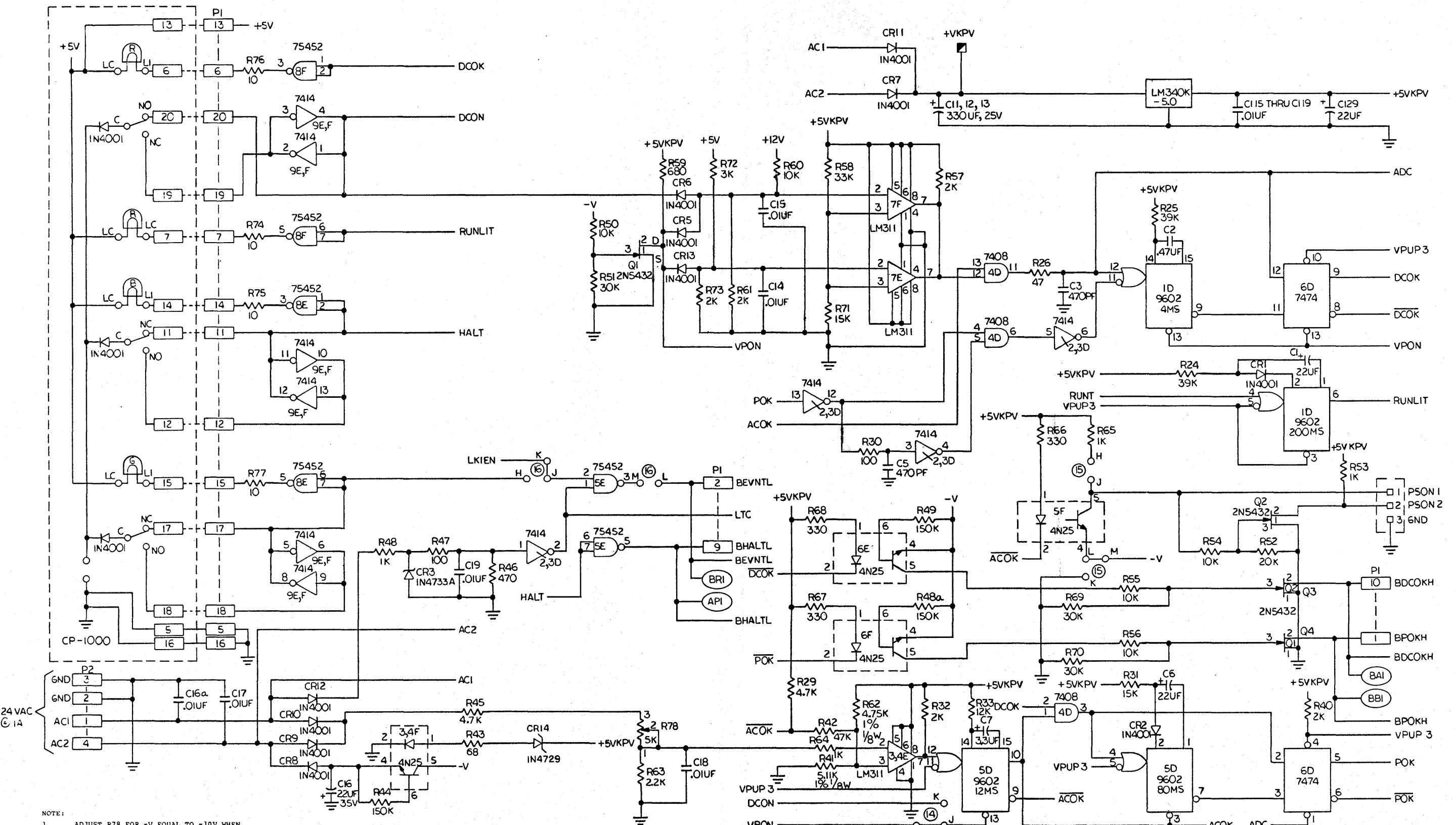
MDB SYSTEMS, INC.

SIZE FSCM NO. D 51648 DWG. NO. 44040338 REV C
DRAWN J. MC. ISSUED 2000 SCALE SHEET 3 OF 5



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DRAWN J. MC.	D	51648	44040338
ISSUED <i>[Signature]</i>	SCALE	REV C	
SHEET 4 OF 5			

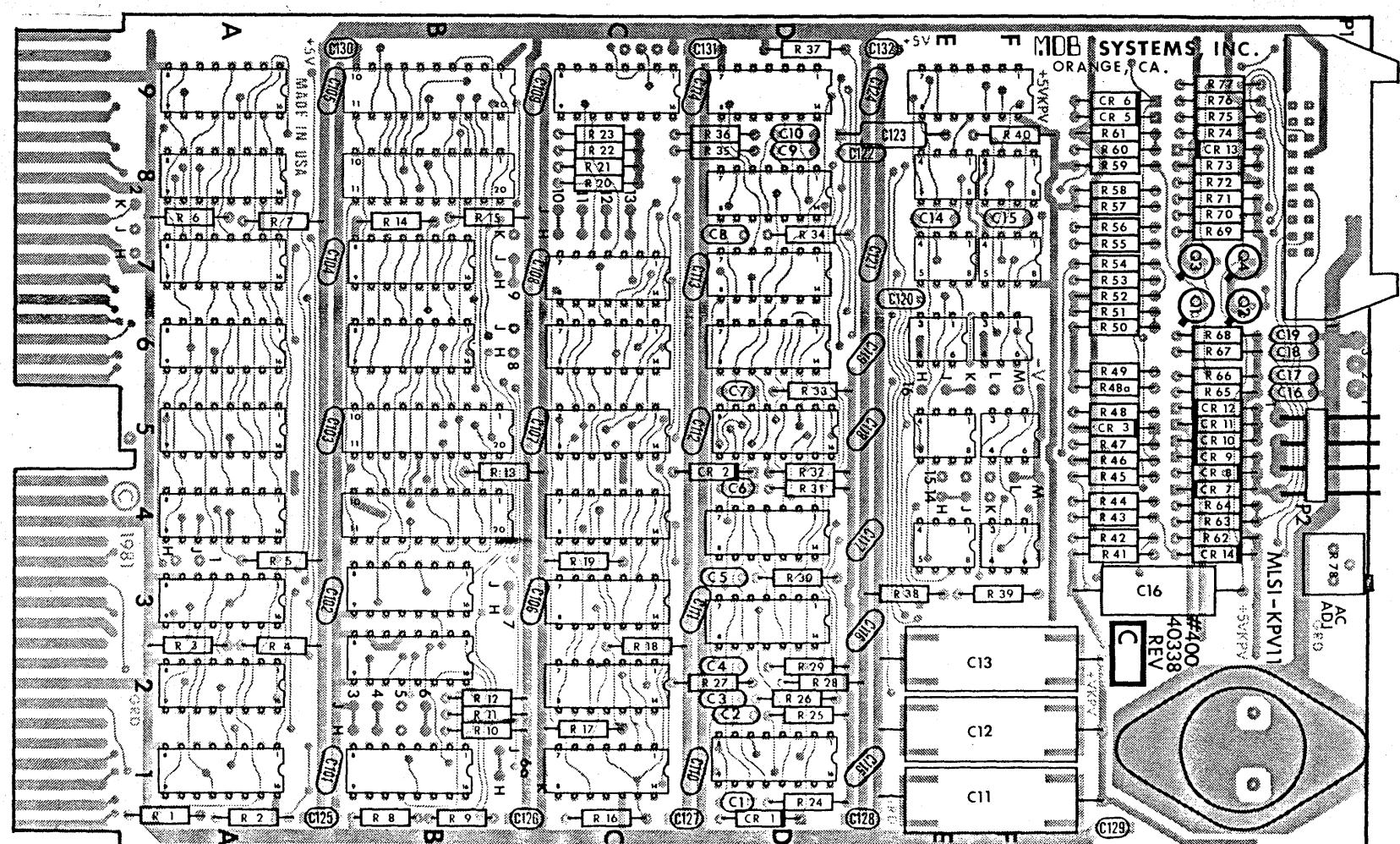


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DRAWN J. MC.
ISSUED 3m
SIZE FSCM NO. D 51648 DWG NO. 44040338 REV. C

SCALE SHEET 5 OF 5

MIDB SYSTEMS, INC.		SIZE	FSCM NO.	DWG. NO.	REV.
DRAWN			51648	45040338	
ISSUED		SCALE		SHEET 1 OF 1	C



MDB SYSTEMS, INC.
1995 North Batavia Street
Box 5508
Orange, California 92667-0508
(714) 998-6900
TWX: 910-593-1339