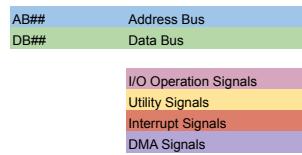


1	GND
3	+12V
5	+12V
7	-12V
9	DPIN
11	
13	+5V
15	MST
17	MACK
19	TYP1
21	PFD
23	AB08
25	AB10
27	GND
29	AB12
31	AB14
33	
35	STOP
37	MBIN
39	DB00
41	DB02
43	+5V
45	DB04
47	DB06
49	DB08
51	DB10
53	DB12
55	DB14
57	EXEC
59	GND
61	IOCL
63	CLK
65	IUR
67	IAR
69	RST
71	PLSE
73	+5V
75	AB03
77	AB05
79	AB07
81	AB01
83	PRIN
85	GND
2	GND
4	+12V
6	+12V
8	-12V
10	DPOT
12	
14	+5V
16	
18	RD
20	SLB
22	MDIS
24	AB09
26	AB11
28	GND
30	AB13
32	AB15
34	
36	SACK
38	MBOT
40	DB01
42	DB03
44	+5V
46	DB05
48	DB07
50	DB09
52	DB11
54	DB13
56	DB15
58	IN
60	GND
62	OUT
64	SER
66	IL1
68	IL2
70	IUA
72	ECHO
74	+5V
76	AB04
78	AB06
80	AB00
82	AB02
84	PROT
86	GND



Signal	Description	Direction
MBIN	Memory bank control in	
MBOT	Memory bank control out	
EXEC	Instruction is "Select" or "Select and Present"	P --> I
IN	Instruction is "Input"	P --> I
OUT	Instruction is "Output"	P --> I
PLSE	Interface strobe	P --> I
RST	Reset all interfaces	P/C --> I
CLK	1MHz timing reference	P --> I
TYP1	Type-1 processor installed	P --> I
SER	Interface controller status	P <-> I
IUR	Interrupt request	P <-> I
IOCL	Synchronize IUR into the processor	P --> I
PRIN	Interrupt priority in	I <-> I
PROT	Interrupt priority out	I <-> I
IUA	Interrupt acknowledge	P --> I
IAR	Interrupt address request	P --> I
ECHO	Transfer Complete	P --> I
IL1	Non-maskable interrupt (Vector 0002)	P <-> I
IL2	Non-maskable interrupt (Vector 0006)	P <-> I
DPIN	DMA priority in	I <-> I
DPOT	DMA priority out	I <-> I
STOP	Stop processor	P --> I
SACK	Stop acknowledge	P --> I
PFD	Power failure detected	PSU --> System
SLB	Select least-significant byte	P/I --> I/M
MST	Memory start	P/I --> M
RD	Read mode	P/I --> M
MACK	Memory acknowledge	P/I <-- M

All signals are active-low!