

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		1	PRELIMINARY	3/14/79	<i>Sbhe.</i>
		2	PRELIMINARY REVISED	3/29/79	<i>Sbhe.</i>
		A	PRODUCTION RELEASE ENQ411	10/30/79	<i>Sbhe.</i>

The information hereon is the property of MICROPOLIS CORPORATION. No portion of this data shall be released, disclosed, used, or duplicated for procurement or manufacturing purposes without specific written consent of MICROPOLIS.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC. DECIMALS ANGLES TIONS .XX .XXX ± ± ± ±	CONTRACT NO.		<h1>MICROPOLIS™</h1> <p>SPECIFICATION - 1220 SERIES RIGID DISK DRIVE SUBSYSTEMS</p>			
	DR BY	<i>Sbhe.</i>				
MATERIAL	CHK BY					
FINISH	APPROVED BY		SIZE	CODE IDENT NO.	DWG NO.	REV.
	<i>Sbhe. 3/14/79</i>		A		100292	A
DO NOT SCALE DRAWING			SCALE		SHEET 1 OF 40	

1.0 INTRODUCTION

This specification describes the Micropolis Model 1220/1200 series of fixed disk systems. These products are intended for mini or microcomputer applications which require medium capacity fixed disk storage at low cost.

Model 1220 consists of a Micropolis 8" fixed disk drive with an integral controller board, and is the minimum system configuration. The 1220 fits within the outline of a Shugart 8" flexible disk drive and requires the same D.C. supply voltages. The controller provides full data transfer and control facilities in six standard sectoring arrangements and can be easily attached to the host computer through a simple bus-oriented interface.

Model 1200 is an add-on module similar to the 1220 except that no controller is provided. Up to three 1200's may be added to the 1220.

These modules are available in three configurations depending on the number of data surfaces in use and offer the following formatted storage capacities:

TABLE 1

MODEL	DATA SURFACES PER DRIVE	DATA TRACKS PER SURFACE	1220/1200 FORMATTED CAPACITY (M BYTES)											
			PER DRIVE						PER SYSTEM					
			SECTOR LENGTH						SECTOR LENGTH					
			128	256	268	320	512	1024	128	256	268	320	512	1024
1221-1	1	580	4.90	6.24	6.22	6.68	7.13	7.13	19.6	24.9	24.9	26.7	28.5	28.5
1222-1	3	580	14.7	18.7	18.7	20.0	21.4	21.4	58.8	74.8	74.6	80.2	85.6	85.6
1223-1	5	580	24.5	31.2	31.1	33.4	35.6	35.6	98.0	125	124	134	143	143

In addition, the controller has select capability which allows two such systems to be attached to the host via a common interface cable.

2.0 FEATURES

- Buffered for asynchronous transfers between host and controller. Full error checking and error recovery procedures are automatically performed.
- Controller may be operated in a direct mode for synchronous transfers between the disk and host at disk speed. Error recovery procedures in direct mode are determined by the host.
- Error correction (ECC) option is provided to ensure high data integrity.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 2	OF

-- Six standard recording formats are available (others by special order):

66 Sectors @ 128 bytes
 42 Sectors @ 256 bytes
 40 Sectors @ 268 bytes
 36 Sectors @ 320 bytes
 24 Sectors @ 512 bytes
 12 Sectors @ 1024 bytes

-- Interfaces easily to the host via an 8-bit bi-directional bus and 9 control lines. The interface structure is suitable for use with either programmed I/O or DMA data transfers.

-- Provides capability to initialize the disk with a wide range of sector sequences to optimize thruput for specific applications.

-- Data transfers may be from one sector to a full track per command. Sectors are normally accessed in logical order. Special commands are also included which transfer a full track in physical sector order to facilitate loading/dumping the disk.

-- Overlap seek is provided. Seeks or read/write operations on the selected drive may be performed simultaneously with seeks on all other drives.

-- High thruput - In buffered mode, the buffer may be filled/unloaded at any rate up to disk speed (approximately $1\mu\text{s}/\text{byte}$). Since transfers are buffered, the host interface need not provide special logic to account for DMA latency for the first data request of each block. In direct mode, the host interface must provide for response to all data requests at disk speed.

-- Most media defects which appear during the life of the system can be eliminated under host control. One spare sector per track is provided for this purpose.

-- Host may verify the correct transmission of each byte of a command to the controller before the command is executed.

-- Cylinder accessing may be logical or physical.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 3	OF

3.0 GENERAL DESCRIPTION

Model 1220 consists of a 1200 series rigid disk drive and a controller board which is housed within the drive outline. These combine to form a flexible, low cost disk sub-system which can be easily attached to any computer system. Three additional 1200's can be attached to the 1220 for expanded storage capacity.

3.1 Disk Drive Mechanics

This consists of a die cast deck whose lower half is devoted to the recording heads, platters and the voice coil motor components. This lower half is sealed and air is circulated throughout the area by disk rotation induced flow. This flow is directed through a 0.3 micron absolute filter. The sealed area breathes to the outside via a similar filter.

There are no active electronic parts in the "clean" area and electrical connection is made between this area components and the electronics package via a PCB, which also seals the "clean" area from the rest of the casting.

3.2 Drive Motor

Rotational drive for the platters is provided by a direct coupled brushless D.C. motor. This combination provides a very low profile allowing 3 platters to be packaged in an envelope only 4.62" high. Switching information for the electronic commutator is supplied by 3 photo transistor/LED combinations attached to the motor control PCBA.

3.3 Positioner System

The positioner is a balanced swing arm mechanism supported on two pre-loaded bearings which reference to a stub shaft rigidly attached to the casting. The system is designed to accept between 2 and 4 arms depending on the model number. The voice coil is attached to the system on the opposite side of the bearings from the head and the whole mechanism is statically balanced. The magnet is of the short coil long magnet type and utilizes a Ferrite magnet. Position reference is made to tracks recorded on a dedicated surface on the platter nearest the deck. These tracks are recorded with position information in the "Modified Dabit" format.

3.4 Read/Write Head

This consists of a single gap slider assembly of the Winchester type with the slider surface modified to run at 3600rpm.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 4	OF

3.5 Electronics Package:

Three boards are associated with the basic drive mechanism:

- a) Preamplifier PCBA
- b) Motor Control PCBA
- c) Device Electronics PCBA

Figure 7 lists the basic drive interface signals. See Specification 100198 - 1200 Series Disk Drives, for a detailed description of the drive and drive interface signals.

3.6 Controller PCBA

This is a microprocessor-based controller which performs such functions as data formatting, encoding, decoding, sector buffering, error detection and recovery, and general housekeeping functions. It consists of a 8" x 14" board which resides in the 1220 drive assembly. Error correction is provided by an optional ECC board which attaches to the controller. D.C. power is drawn from the disk drive.

External connection is made through two edge connectors at the rear of the drive assembly:

- a) Host Interface, J101. (34 pin edge connector)

This attaches to the host system (and another 1220 in an expanded system). Signal and pin assignments for this interface are shown in Figure 8.

- b) Drive Interface, J102. (50 pin header)

This attaches to the drive interface connector, J1, and add-on 1220's, if any. Pin assignments are shown in Figure 7.

A detailed description of the host interface and controller operation is given in the following sections of this specification.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 5	OF

4.0 SPECIFICATION SUMMARY4.1 Disk Drives

Spindle Speed	3600 rpm
Speed Variation	±.5%
Latency	3.3 ms
Track Density	478 tpi
Available Tracks	580
Access Time	
Track-to-Track	4 ms
Average (1/3 stroke)	34 ms
Settling	8 ms
Data Surfaces	
1221-1	1
1222-1	3
1223-1	5
Media	200 mm oxide coated (IBM 3350 technology)

4.2 1220/1200 System

Sectoring Method	Hard
Number of Sectors	Six standard formats (See Table 1)
Encoding Method	EPM (modified 3PM).
Data Density (inner track)	8623 bpi
Flux Density (inner track)	5749 frpi
Transfer Rate	922 Kbytes/sec maximum
Formatted Capacity	See Table 1

4.3 Physical (each module)

Environmental

Ambient Temperature	10 - 40°C
Relative Humidity	10 - 80% non condensing

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 6	OF

Mechanical (See Figure 3)

Depth	14.25" (362 mm)
Width	8.55" (217 mm)
Height	4.62" (117 mm)
Weight	22 lbs. (10 KG).

4.4 Dissipation

Total dissipation including positioning:

1220	95 watts
1200	75 watts

4.5 Reliability (excluding error correction)

Soft Read Errors	1 in 10 ¹⁰
Hard Read Errors	1 in 10 ¹²
MTBF (Total Unit)	10,000 hrs.
MTBF "Clean" Area Components	25,000 hrs.

5.0 DC POWER REQUIREMENTS (each module)

DC power is supplied to each drive via a 10 pin AMP connector, J3. Pin assignments are shown in Figure 6. The mating connector is AMP 1-37159-0. The DC requirements are:

VOLTAGE	1220		1200	
	AVE	PEAK	AVE	PEAK
+24V ±5%	2.25A	4.5A (20 secs)	2.25A	4.5A (20 secs)
+ 5V ±5%	6.0A	6.0A	2.25A	2.25A
-12V ±5%	0.8A	0.8A	0.5A	0.5A

6.0 CONTROLS AND INDICATORS

None. When DC power is applied to the drive, power sense circuits in the drive and controller determine that all voltages are within limits. At this time the initial load sequence occurs which runs the spindle up to operating speed and positions the heads over cylinder 0. The controller initializes important flags and registers to a known state as described in Section 9.0.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 7	OF

7.0 DISK FORMAT

The 1220 controller makes use of the track/sector format shown in Figure 4. Tracks are divided into a number of sectors which contain a fixed blocklength of user data. The beginning of each sector is identified by a sector pulse from the disk drive. Each track contains one spare sector which at the time of initialization can be made to fall over a defective area of the track.

Sectors are divided into an address field, a data field, and a trailing gap area. Data is recorded most significant bit first where Bit 7 is the most significant and Bit 0 the least significant bit of each byte. The EPM encoding method provides an increased data packing density compared to MFM while maintaining the same decoding margins and reliability.

The suffix H indicates a hexadecimal value in the following description.

7.1.1 Address Field -- Contains a unique track/sector address and associated information. This field is written during initialize commands only.

Preamble ----- Synchronizes read circuits
 Address Mark ----- Identifies the beginning of an Address Field.
 The value contained in this byte indicates whether a defective sector has been spared on this track.
 = 77H Normal initialize, no defective sector. The spare sector resides at the end of the track.
 = 7DH Track has been initialized to eliminate a defective sector.

Byte 0 ----- Bits 0-2 Head Address (0-4)
 Byte 1 ----- Bits 0-7 Cylinder Address LSB } (0-579)
 Byte 2 ----- Bits 0-1 Cylinder Address MSB }
 Byte 3 ----- Bits 0-6 Logical Sector Address (0-65)
 CRC (2 bytes) ----- Cyclic Redundancy Check bytes.
 Computed from contents of the Address Mark and bytes 0-3 using the polynomial $X^{16} + X^{12} + X^5 + 1$

Postamble ----- Trailing guardband

Unused bits are zeroes.

7.1.2 Data Field -- Contains user data for transfer to/from the host system:

Preamble ----- Synchronizes read circuits
 Data Mark, 44H ----- Identifies beginning of a Data Field
 Data ----- n bytes of user data
 ECC (4 bytes) ----- Optional Error Correction Code computed from contents of Data Mark and User Data
 CRC (2 bytes) ----- CRC computed from contents of Data Mark and User Data using same polynomial as Address Field.
 Postamble ----- Trailing guardband

MICROPOLIS™

SIZE

A

CODE IDENT NO.

DWG NO.

100292

SCALE

SHEET 8 OF

7.1.3 GAP -- Provides tolerance for disk speed variation

Six standard arrangements of this format are available as shown in Figure 4. The required format is selected by appropriate jumper connections on the drive and controller and must be specified when ordering. An additional 1K bytes of RAM must be installed in the controller for operation with the 1K byte data format.

7.2 Sector Interleaving

A track can be initialized with the sectors in sequential order or in a number of interleaved patterns (Figure 5). When interleaved, consecutive logical sectors (as determined by byte 3 in the address field) are physically separated from each other by one or more other sectors. This provides a sector-to-sector latency which can be chosen to optimize the host system's processing time.

In addition, the physical position of sector 0 can be specified on a track-by-track basis. For instance, the user might format the disk surface with a specific interleaved pattern which rotates by equal increments as consecutive cylinders are accessed.

7.3 Sector Sparing

Tracks are normally initialized with the spare sector located at the end of the track. If one of the data sectors becomes defective the track can be re-initialized placing the spare sector over the defective area. The sector in error and all other sectors around to index are shifted right one place maintaining the interleaved pattern. Parameter Byte 6 in the Initialize commands specifies normal/spared mode and contains the logical address of the sector to be spared. Address Mark bytes contain 77H for a normal track or 7DH for a spared track.

A maximum of one sector per track may be spared. The user can determine if a given track has already been spared by accessing the contents of an Address Mark using the Read Header command.

7.4 Initialize Commands

Each data surface of the disk must be pre-recorded with the desired format before normal use. Three Initialize commands are provided for this purpose:

INITIALIZE TRACK ----- Writes entire length of current track (beginning and ending with index) using head, cylinder, sector sequencing and sparing information contained in the accompanying parameter bytes. Data fields contain the cylinder address in the first two bytes and EEH in the remaining data byte locations.

VERIFY FORMAT ----- Verifies that track is correctly initialized. Reads entire track and compares against initialize pattern.

MICROPOLIS™

SIZE

A

CODE IDENT NO.

DWG NO.

100292

SCALE

SHEET 9 OF

INIT and VFY ----- Combination of the two above commands.

A user utility program is required to initialize then verify each track on the disk with the desired format.

8.0 HOST INTERFACE

The host interface to the 1220 is made through a 34 pin edge connector, J101, located on the Controller PCBA. Pinouts, electrical characteristics, and timing requirements are shown in Figures 8-11.

All signals except CBUSY on the interface are low true (indicated by a /). However, in the remainder of this text reference will be made to the logical condition of each signal rather than it's electrical polarity. e.g. 0=false, 1=true.

The interface is structured around an 8 bit bi-directional bus and the three control signals WSTR, RSTR, and DATA. Information is output to either a control (command) or data port using WSTR, and input from a control (status) or data port using RSTR. DATA selects the port in use.

These exchanges are controlled by the host making use of handshake flags in the status byte. Most flags appear in both the status byte and on separate interface lines to allow flexibility in the method of attachment to the host system.

8.1 Interface Signals

- SEL ----- Selects the controller in one of two 1220/1200 systems attached to host interface. When selected, the controller responds to the bus control lines. The address is determined by jumpers W1, W2 on the controller PCBA.
- SEL = 0 Address 0, W1 installed
 = 1 Address 1, W2 installed
- ENABLE ----- Normally held true. When false (2 μ s min), the power-on sequence is invoked in all controllers (Section 9.0). Automatically initializes controller if there is no host power or if the cable is disconnected. May also be used for programmed reset.
- BUS \emptyset - BUS7 ----- Bi-directional tri-state bus which transfers (8 lines) information to/from the controller in parallel.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 10 OF

APPLICATION

REVISIONS

- WSTR ----- Write Strobe. When pulsed, one byte is output from the host to the controller. Contents of the bus are copied into an output buffer on the trailing edge of WSTR. The byte is interpreted as being either control (DATA=0) or data (DATA=1).
- RSTR ----- Read Strobe. When pulsed one byte is input from the controller to the host. When RSTR is true, the controller drives the bus with the contents of either the status register (DATA=0) or input buffer (DATA=1). RSTR must not be asserted while the host is driving the bus.
- DATA ----- Selects the control or data ports as described above.
- CBUSY/ ----- Controller Busy/. Cleared when a command is issued, set when the command is terminated. The polarity is chosen so that the controller appears busy to the host when the cable is disconnected.
- CBUSY/ = 0 Controller busy executing a command.
= 1 Controller not busy, a new command can be accepted.
- ATTN ----- Attention. Set true at the end of each command when CBUSY/ changes state. The host should respond by reading the TERMINATION STATUS byte which indicates the success or failure of the command. ATTN is cleared approximately 70 μ s after TERMINATION STATUS is read.
- DREQ ----- Data Request. This flag requests the transfer of each byte of user data to/from the controller. The direction of transfer is specified by OUT. The host must respond by writing/reading the required byte to the data port. Data must be transferred only in response to DREQ.
- In buffered mode the data transfer rate is determined by the host (0-922KHz). In direct mode transfers are synchronous with the disk, and each byte must be serviced in less than one byte-time. See Figure 11 for timing.
- OUT ----- Specifies the direction of data transfer.
- = 0 Controller to host (Class 2 commands)
= 1 Host to controller (Class 3 commands)

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 11 OF

8.2 Status Byte

This byte is accessed by reading from the control port. It contains controller status and handshake flags which co-ordinate the exchange of information with the host. The flags ORDY and IRDY are used during command initiation and termination only. DREQ and OUT control the transfer of user data.

- Bit 0 ----- Input Ready (IRDY).
 = 1 Input buffer contains a byte for the host. This may be a Command Verify, Termination Status, or Auxiliary Status byte. Set when input buffer is filled, cleared by reading from the data port.
 IRDY is not valid and should be ignored when CBUSY/=0.
 = 0 Input buffer empty.
- Bit 1 ----- Output Ready (ORDY).
 = 1 Host may output a Command, Parameter, or GO byte to the output buffer. Set when controller accepts previous byte, cleared by writing to the control or data port.
 ORDY is not valid and should be ignored when CBUSY/=0.
 = 0 Output buffer full.
- Bits 2,3 = 0
- Bit 4 CBUSY/ }
 Bit 5 DREQ }
 Bit 6 OUT } See Section 8.1
 Bit 7 ATTN }

8.3 Information Exchange

The following table summarizes the types of information exchanged between the controller and the host:

<u>DIRN</u>	<u>PORT</u>	<u>TYPE</u>	<u>QTY.</u>	<u>RELEVANT CONDITIONS</u>	
OUTPUT (WSTR)	CONTROL	COMMAND	1	CBUSY/,ORDY	
		DATA	CMD PARMS	6	CBUSY/,ORDY
			GO WRITE DATA	1 n	CBUSY/,ORDY CBUSY,DREQ,OUT
INPUT (RSTR)	CONTROL	STATUS	1	ALL	
		DATA	CMD VFY	0-7	CBUSY/,ORDY,IRDY
			READ DATA	n	CBUSY,DREQ,OUT/
			TERM STATUS AUX STATUS	1 0-7	CBUSY/,ATTN,IRDY CBUSY/,ATTN/,IRDY

MICROPOLIS™

SIZE

CODE IDENT NO.

DWG NO.

A

100292

SCALE

SHEET 12 OF

9.0 POWER-ON SEQUENCE

A d.c. reset is applied to the controller logic for a period of 500 ms after power-on, or when ENABLE/ is false. This forces CBUSY/=0, causing the controller to appear busy. When the reset is released the controller initializes important flags and registers to a known state. Approximately one second later, CBUSY/ is set and the controller is ready for use.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 13 OF

10.0 GENERAL OPERATION

A command is initiated by writing a command byte to the control port, followed by six parameter bytes and a GO byte to the data port. The command byte (Figure 12) specifies the type of command, while the parameter bytes (Figure 13) contain associated address information. The GO byte causes the command to be executed and may contain any value. All eight bytes must be transmitted to the controller even though some are not used in certain commands.

As each of the command and parameter bytes is transmitted, the controller copies the received value into the input buffer. If desired, the host may access and verify this byte before proceeding to the following byte. In this way the transmission of a command can be fully verified.

The command set is divided into three classes as follows:

Class 1 --- Non-data transfer

Class 2 --- Transfers from controller to host

Class 3 --- Transfers from host to controller

When the GO byte is received, the controller goes busy (CBUSY/ = 0) and proceeds to execute the command. Data transfers between the host/controller/disk now take place as required. Checks are performed on the validity of the command and parameter bytes, and on all data transfers to/from the disk.

The command is terminated in one of two ways:

- a) On successful completion of the command. For Class 2 and 3 commands this occurs when the required number of sectors have been transferred.
- b) When a fatal error condition has been detected.

In both cases a standard termination sequence occurs. First the controller drops busy (CBUSY/=1), sets ATTN, then places a Termination Status byte in the input buffer. Termination Status identifies any error condition or special event that may have occurred during the command. When ATTN true (or CBUSY/=1) is recognized, the host should respond by reading Termination Status from the data port using the command termination protocol shown in Figure 15. Reading Termination Status causes ATTN to be cleared. Execution of the command is now complete.

If desired, the host may also access one or more of the Auxiliary Status bytes which are placed in the input buffer following Termination Status. These provide detailed drive and controller status information and are usually reserved for diagnostic purposes.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 14 OF

A command will be accepted at any time the controller is not busy. The receipt of a command byte (i.e. write to control port while CBUSY/=1) conditions the controller to expect the transmission of a complete command, hence no special initialization is required when previous activity is unknown. For instance, if one of the command or parameter bytes fail to verify the host would simply retransmit the entire command beginning with the command byte.

The bus protocol taking place during command initiation and termination is shown in detail in Figures 14, 15, and 16.

11.0 COMMANDS (Figure 12)

11.1 Class 1 Commands

These commands do not involve host data transfers.

Bits 0,1 ----- 01H. Class 1 code.

Bits 2-4 ----- Command Code. See below.

Bit 5 ----- Not used.

Bit 6 ----- Seek (READ HDR, 3 INITIALIZE CMDS).
 = 1 -- A seek to the specified head/cylinder (track) occurs before the operation is performed.
 = 0 -- Operation performed on the current track.

Bit 7 ----- Retry Over-Ride (READ HDR, 3 INITIALIZE CMDS).
 = 1 -- Automatic error retry procedure disabled.
 = 0 -- Retry procedure enabled. (See Section 14.0)

CMD Code = 0 Drive Status

The specified drive is selected and drive status is reported in Aux. Status Byte 1.

= 1 Seek Only

A seek is initiated on the specified drive to the specified head/cylinder. The command is immediately terminated.

Overlapped seeks can be performed by repeated use of this command or in conjunction with commands having an implied seek. Any command can be overlapped with seeks previously initiated on other drives.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 15 OF

- = 2 Read Header
The Address Field in the first occurring sector is read and the contents are made available in Aux. Status bytes 3 thru 7.

This command may be used to determine whether a track has been spared, or to check that the expected track has been reached after a seek operation.
- = 3 Restore
The selected drive is restored to head 0, cylinder 0, and the drive cylinder address register is recalibrated.
- = 4 Initialize Track
See Section 7.4
- = 5 Verify Format
See Section 7.4. To ensure a good Initialize, retries should be disabled when using this command (bit 7=1).
- = 6 Initialize and Verify
Combination of Initialize Track and Verify Format. If retries are enabled a track failing to verify will be automatically re-written.
- = 7 Fault Reset
Resets fault latch in selected drive.

11.2 Class 2 Read Commands

These commands involve data transfers from the controller to the host. The four basic commands specified by bits 2,3 can be executed in a number of different modes depending on the value of bits 4-7.

Bits 0,1 ----- 02H. Class 2 code.

Bits 2,3 ----- Command Code. See below.

Bit 4 ----- Track. Selects logical or physical sector sequencing.

- = 0 Normal. Sectors are accessed in logical order. Parameter byte 4 contains the starting sector address and parameter byte 5 the number of sectors to be transferred.
- = 1 A complete track is transferred in physical order, beginning and ending with index. Parameter bytes 4,5 must contain the

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 16 OF

APPLICATION

REVISIONS

Initialize format pattern. Parameter byte 6 is not used. Useful for disk load/dump operations in direct mode.

- Bit 5 ----- Direct. Selects direct/buffered mode.
- = 0 Buffered Mode. All data transfers to/from the host take place through a sector buffer in the controller (0-922 Kbytes/sec). Buffered mode includes automatic error retries if bit 7=0.
 - = 1 Direct Mode. Data transfers takes place directly between the disk and host, and are synchronous with the disk (922 Kbytes/sec). Read data is also stored in the sector buffer for error correction purposes. Retries are not performed. The host must implement it's own error recovery procedures.
- Bit 6 ----- Seek.
- = 0 No implied seek.
 - = 1 Drive seeks to specified head/cylinder before data transfer.
- Bit 7 ----- Retry Over-Ride. (Buffered mode only).
- = 0 Automatic retry procedure enabled.
 - = 1 Retries disabled.
- CMD Code = 3 Normal Read. Disk read data is transferred to the host in the mode specified by bits 4-7. All error checks are enabled.
- = 2 Read with Address Check Over-ride. Same as normal read except that all checks on the address field are overridden except sector co-incidence. The overridden checks are head, cylinder, and CRC.
 - = 1 Read with Data Check Override. Same as normal read except that the data field checks (ECC and CRC) are overridden.
 - = 0 Correct. The contents of the sector buffer undergo a correction attempt and the result is transferred to the host. Success or failure is indicated in the Termination Status byte. This command is only valid immediately following an unsuccessful read in either Direct mode or Buffered mode with retries overridden, when the ECC option is installed.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 17 OF

11.3 Class 3 Write Commands

These commands involve data transfers from the host to the controller. They are divided into two groups, WRITE and VERIFY, depending on the state of bit 2 and can be executed in a number of different modes selected by bits 3-7.

Bits 0,1 ----- 11H. Class 3 code.

Bit 2 ----- Write. Selects WRITE or VERIFY command.
 = 1 WRITE command. Host data is transferred to the controller and is written onto the disk in the mode specified by bits 3-7. Automatic rewrites occur if bit 3 = 1 (buffered mode).
 = 0 VERIFY command. Host data is compared byte-for-byte against data read from the disk. This command is normally used directly after a WRITE command to verify that the data has been correctly recorded. Automatic rewrites occur if bit 3 = 1 (buffered mode).

Bit 3 ----- Read-After-Write.
 = 0 Normal WRITE or VERIFY.
 = 1 Buffered mode only (no effect Direct mode).
 For WRITE commands, an automatic read-after-write is performed as each sector is processed. If an error occurs, the sector is automatically rewritten using the contents of the sector buffer.

For VERIFY commands, a sector which fails to verify is automatically rewritten using the contents of the sector buffer.

Bit 4 ----- Track.

Bit 5 ----- Direct.

Bit 6 ----- Seek.

Bit 7 ----- Retry Override

} See Class 2 Commands.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 18 OF

12.0 PARAMETER BYTES (Figure 13).

The six parameter bytes contain address and control information associated with each command. All parameter bytes must be transmitted to the controller even though some may not be used. Unused bits should be zero.

PARAM BYTE 1 Bits 0,1 ---- Unit Address. Selects one of 4 disk drives.

Bits 2,3 ---- Not used.

Bits 4-7 ---- Head Address (0-4).

PARAM BYTE 2 Bits 0-7 ---- Cylinder Address, least significant 8 bits. } (0-579)
PARAM BYTE 3 Bits 0-2 ---- Cylinder Address, most significant 3 bits. }

Bits 3,4 ---- Zero.

Bit 5 ----- Not used.

Bit 6 ----- OFFSET+ } Offsets positioner either side of center track.
 Bit 7 ----- OFFSET- } Effective for Read Commands only in direct mode or buffered mode with retries disabled. Used in host error recovery procedures.

PARAM BYTE 4 Bits 0-7 ---- Normally contains the starting sector address. For track-oriented commands*it contains the physical address of logical sector 0.

PARAM BYTE 5 Bits 0-7 ---- Normally contains the number of sectors to be processed. For track-oriented commands*it contains the sector spacing code.

PARAM BYTE 6 Bits 0-7 ---- Normally not used. For INIT and INIT & VFY commands this byte determines the spare sector location as follows:

- = Illegal sector address (N thru 255).
Normal initialize, the spare is written at the end of the track. Address Marks contain 77H.
- = Legal sector address (0 thru N-1).
Spared mode. The spare is written where the specified logical sector would normally be. The replaced sector and the following sectors around to index are shifted right one place. Address marks contain 7DH.

* Track-oriented commands consist of the 3 INITIALIZE commands and Class 2 or 3 commands with the Track bit set (bit 4=1).

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 19 OF

13.0 TERMINATION/AUXILIARY STATUS

The Termination and Auxiliary Status bytes are made available by the controller at the end of each command. Termination Status is accessed by reading from the data port in response to ATTN true, using the command termination protocol. If desired, one or more of the Auxiliary Status bytes can then be accessed by further reads from the data port.

13.1 Termination Status Byte

Bits 0-3 of this byte contain an error code which identifies any error condition that may have occurred during the command. If zero, the command has been successfully completed; if non-zero, the code value indicates the reason for termination. Bits 4-7 contain other flags useful in error analysis.

Bits 0-3 ----- Error Code.

- = 0 No error.
- 1 Invalid command.
- 2 Invalid parameter byte.
- 3 Drive not ready.
- 4 Drive fault.
- 5 Illegal head or cylinder address.
- 6 Sector not found.
- 7 Data error.
- 8 Verify (compare) error.
- 9 Timeout error.
- A-F Not used.

Bit 4 ----- Temporary Positioner Error (sector not found cleared by restore).

Bit 5 ----- Temporary Write Fault (drive Fault occurred during write, was successfully cleared).

Bit 6 ----- Temporary Error (one or more retries performed).

Bit 7 ----- Corrected Error (data error successfully cleared by ECC correction).

Bits 4-7 = 0 if Error Code \neq 0.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 20 OF

13.2 Auxiliary Status

The Auxiliary Status bytes contain detailed drive and controller status relating to the last command. They are normally reserved for diagnostic purposes.

Auxiliary Byte 1	<u>Drive Status</u>	
	Bits 0,1,3,4	Undefined
	Bit 2	Not Ready
	Bit 5	Illegal Head or Cylinder Address
	Bit 6	Fault
	Bit 7	Seek Complete

Auxiliary Bytes 2-7 Command Echo

These bytes normally contain the command code and first 5 parameter bytes for the last command, except that the starting sector address (Aux. Byte 6) has been updated to indicate the last sector processed. Aux. Byte 6, therefore, indicates the failing sector address when an error termination occurs.

For a READ HEADER command:

Aux. Byte 2	= Command Code
Aux. Byte 3, bits 0-3	= Unit Address in command
Aux. Byte 3, bits 4-7	= Head Address read from header
Aux. Bytes 4-7	= Cylinder LSB, Cylinder MSB, Sector, and Address Mark bytes read from header, respectively

Following Aux. Status Byte 7, the controller will continue to fill the input buffer indefinitely. This information is not defined.

14.0 RETRY SEQUENCE

This feature is enabled or disabled by bit 7 in the command byte. In buffered mode, an automatic retry sequence is entered on a sector-by-sector basis when a disk error condition is detected. For data errors, three levels of retry are performed:

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 21 OF

Level 1 ----- If the ECC option is installed, a correction attempt is made on the contents of the sector buffer. If successful the corrected data is transmitted to the host.

Level 2 ----- The failing operation is repeated up to ten times. Level 1 retries are included.

Level 3 ----- The positioner is offset one way then the other from the track center. Level 1 and 2 retries are performed again.

For a sector not found condition, the positioner is restored and a re-seek takes place to the original track. A retry is then made.

If drive FAULT status is detected during write operations, a FAULT RESET is attempted. If successful, a retry is made.

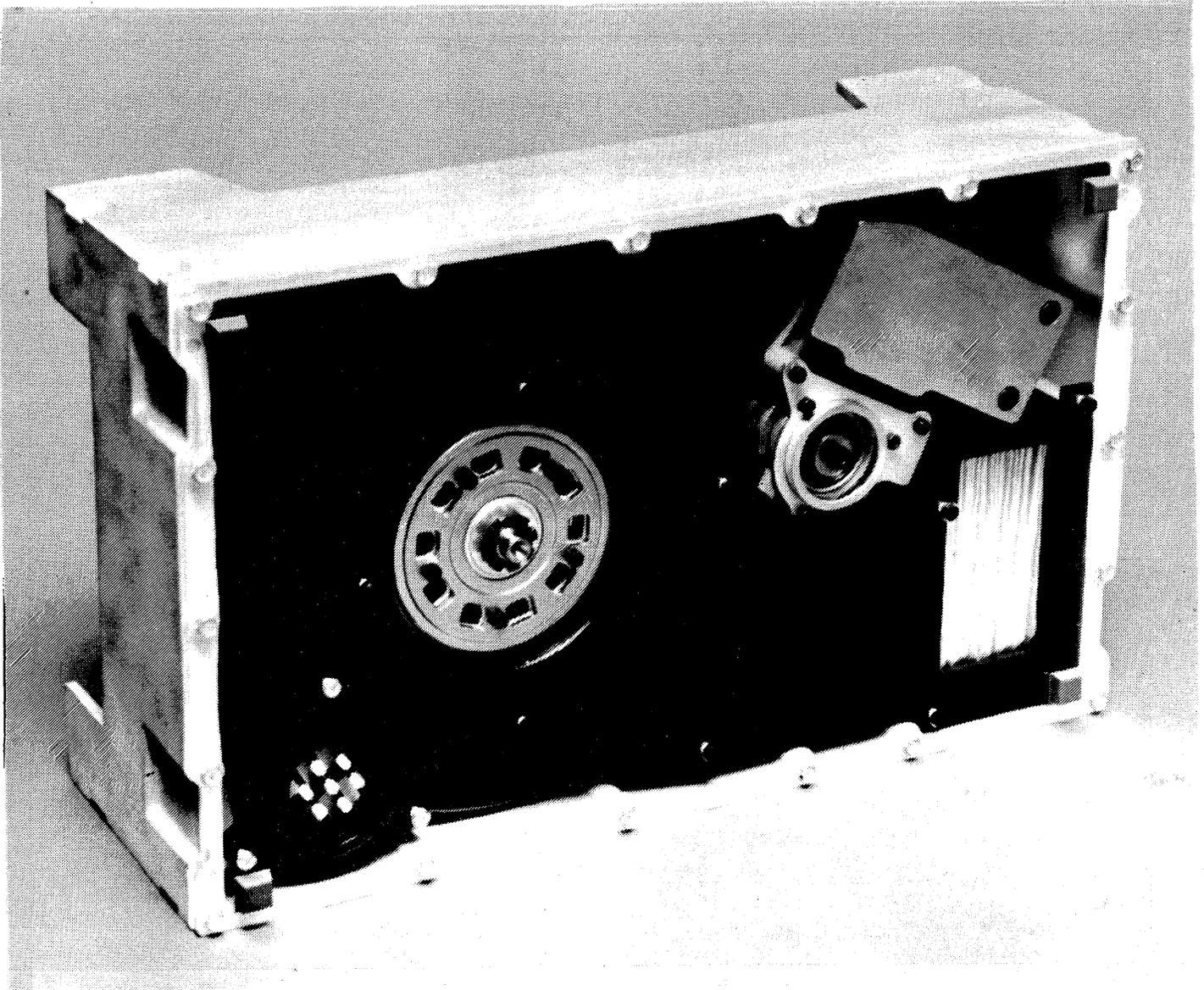
If all retries are unsuccessful, the command is aborted and an error termination occurs. The cause for termination is contained in the Termination Status byte.

15.0 HOST I/O PROTOCOL

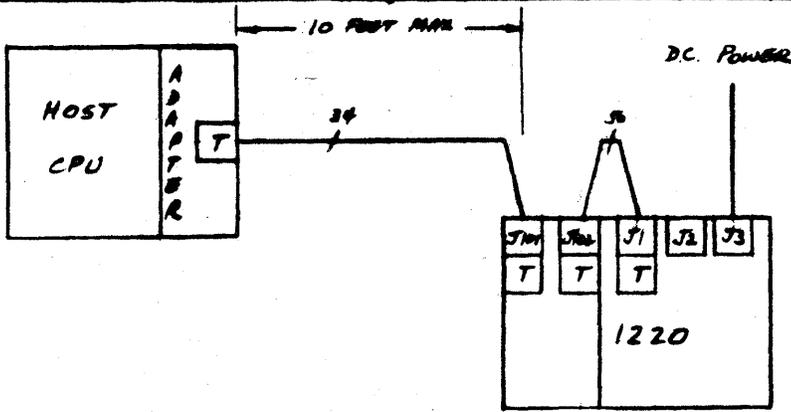
Figures 16a - 16c show the I/O bus protocol that must be performed by the host to successfully communicate with the controller. This may be implemented in any combination of hardware/software.

MICROPOLIS™

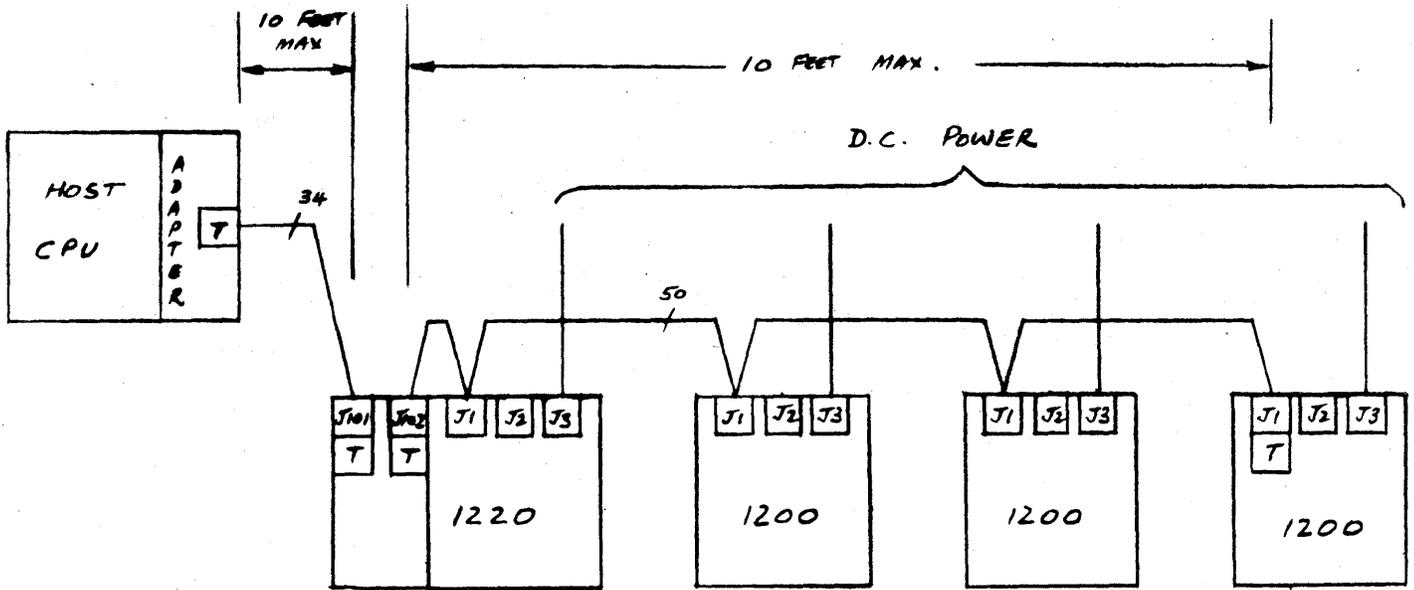
SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 22 OF

FIGURE 1. 1220/1200 MODULE.**MICROPOLIS™**

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 23 OF	



SINGLE DRIVE SYSTEM.



EXPANDED SYSTEM.

T = TERMINATION NETWORK INSTALLED.

FIGURE 2. SYSTEM CONFIGURATION.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292
SCALE	SHEET 24 OF	

APPLICATION

REVISIONS

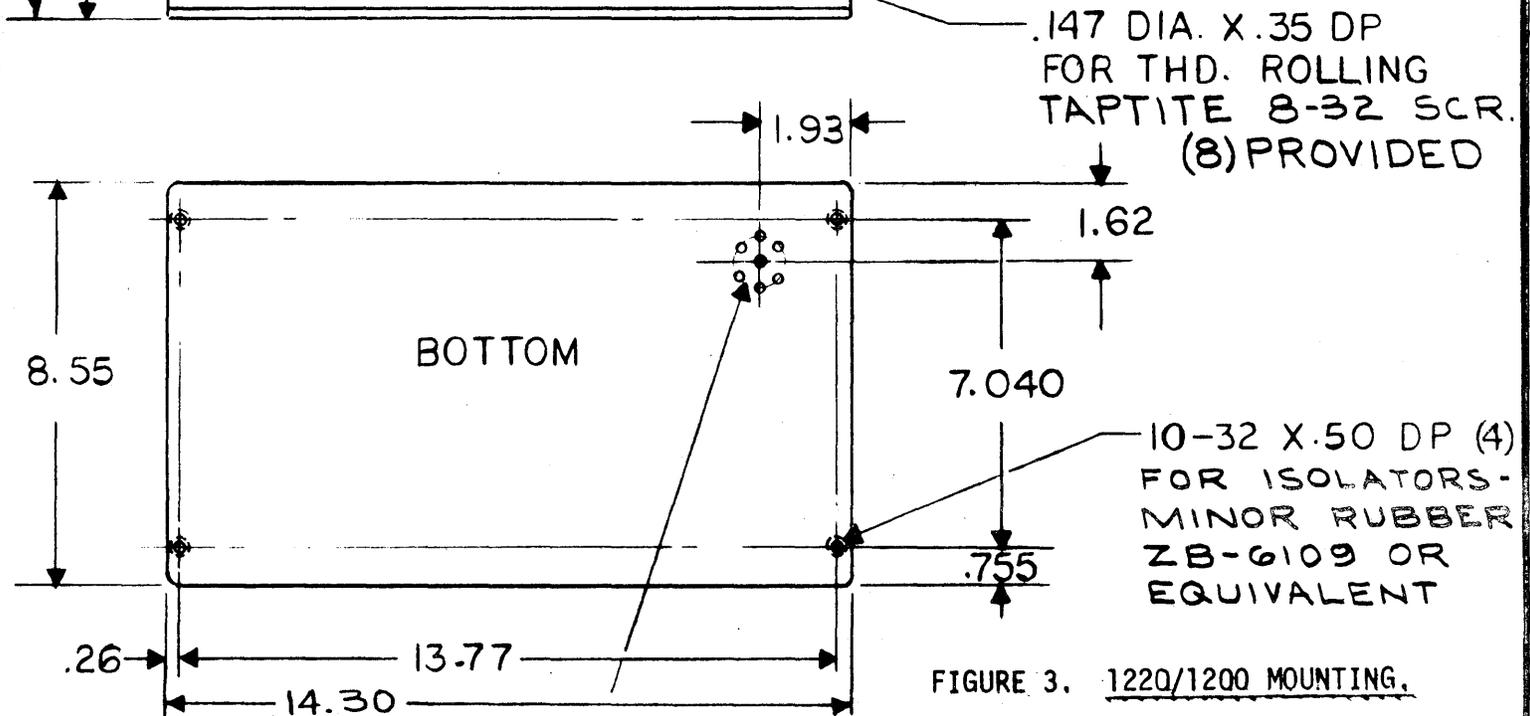
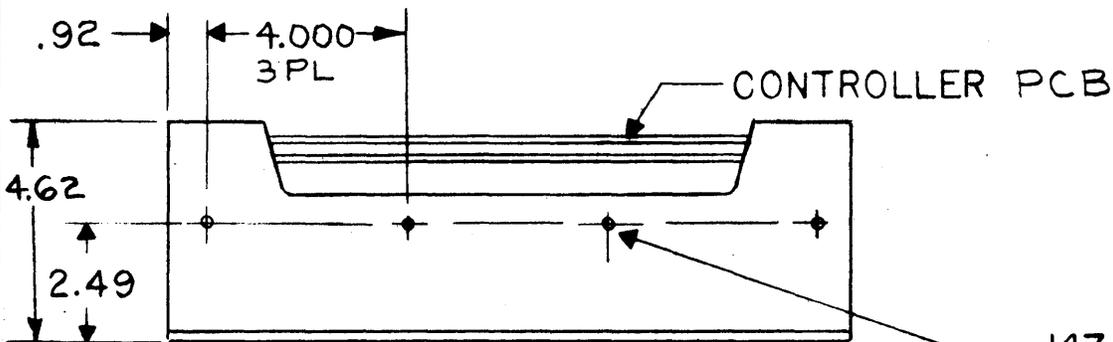
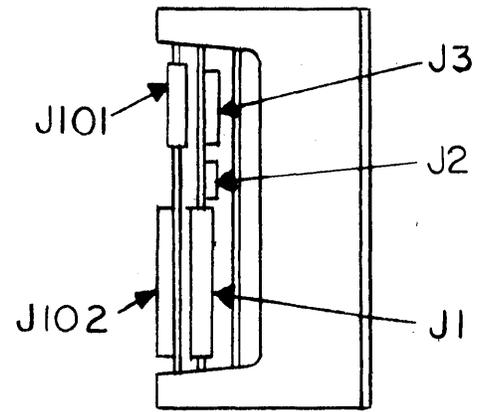
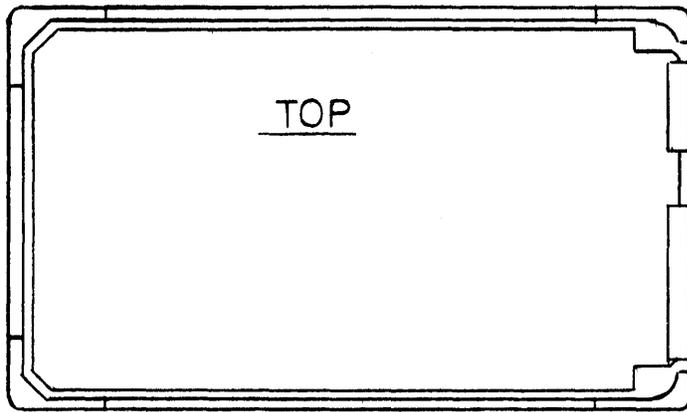


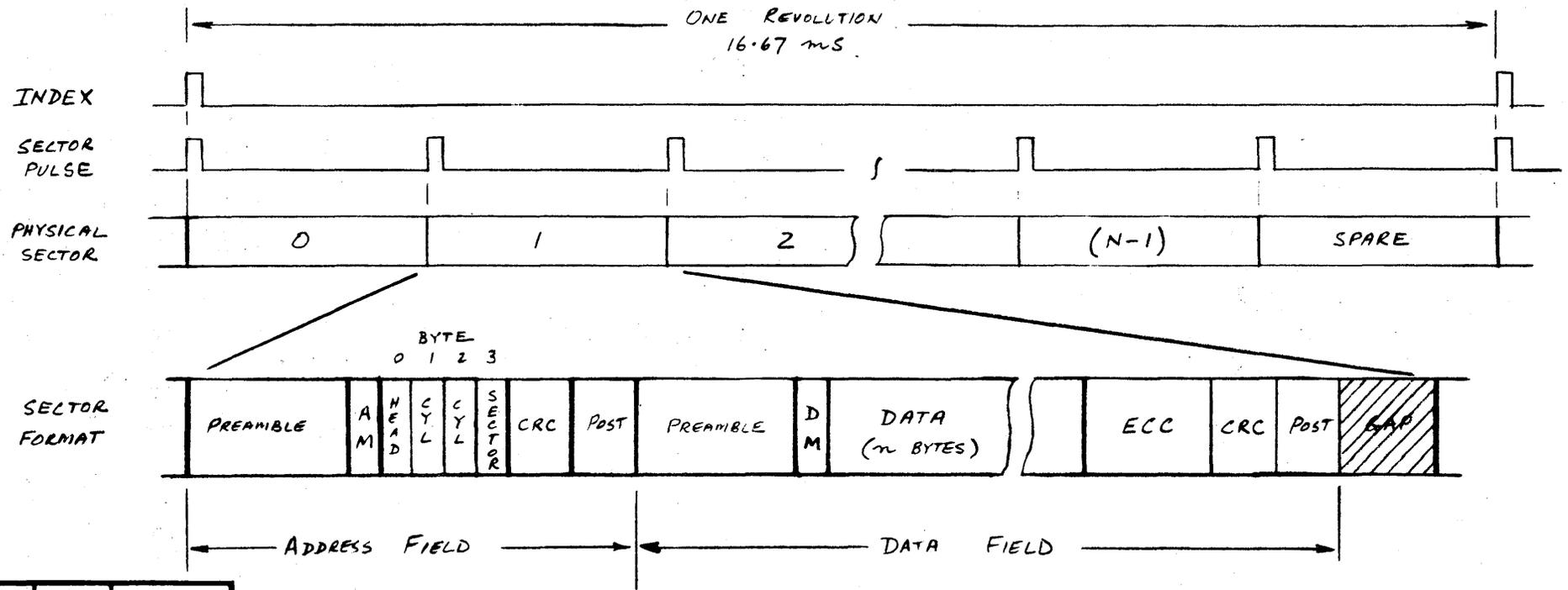
FIGURE 3. 1220/1200 MOUNTING.

1.0 DIA BREATHER HOLES DO NOT BLOCK

NOTE - BOTTOM-UP MOUNTING IS NOT PERMITTED.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292	
SCALE			SHEET 25 OF



SCALE	A	MICROPOLIS™	
SIZE	CODE IDENT NO.	DWG NO.	
	100292		
SHEET 26 OF			

STANDARD FORMATS

NUMBER OF SECTORS (N)	DATA BYTES PER SECTOR (n)	CAPACITY PER TRACK (KB)
66	128	8.4
42	256	10.8
40	268	10.7
36	320	11.5
24	512	12.3
12	1024	12.3

FIGURE 4. DISK FORMAT.

For Initialize Commands:

- a) Parameter Byte 4 specifies the physical address of logical sector 0.
- b) Parameter Byte 5 specifies the number of sectors occurring between consecutive logical sectors.
- c) Parameter Byte 6 selects normal/spared track and specifies the logical sector address to be spared.

EXAMPLE

12 Sector Format, Normal Initialize with Parameter Byte 4 = 0.

PARAMETER BYTE 5	PHYSICAL SECTOR POSITION												
	0	1	2	3	4	5	6	7	8	9	10	11	12
0	0	1	2	3	4	5	6	7	8	9	10	11	SP
1	0	6	1	7	2	8	3	9	4	10	5	11	SP
2	0	4	8	1	5	9	2	6	10	3	7	11	SP
3	0	3	6	9	1	4	7	10	2	5	8	11	SP
4	0	5	10	3	8	1	6	11	4	9	2	7	SP
5	0	2	4	6	8	10	1	3	5	7	9	11	SP
6	0	7	2	9	4	11	6	1	8	3	10	5	SP
7	0	3	6	9	2	5	8	11	1	4	7	10	SP
8	0	4	8	3	7	11	2	6	10	1	5	9	SP
9	0	6	5	11	4	10	3	9	2	8	1	7	SP
10	0	11	10	9	8	7	6	5	4	3	2	1	SP

FIGURE 5. INTERLEAVED SECTOR PATTERNS.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292	
SCALE		SHEET 27 OF	

APPLICATION

REVISIONS

<u>PIN</u>	<u>VOLTAGE</u>
1	+24V SENSE
2	GND SENSE
3	-12V SENSE
4	+5V SENSE
5	+5V RETURN
6	-12V RETURN
7	+5V
8	-12V
9	+24V RETURN
10	+24V

MATING CONNECTOR: AMP 1-87159-0

FIGURE 6. POWER CONNECTOR J3

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 28 OF	

J1/J102 CONNECTOR

<u>SIG</u>	<u>GND</u>	<u>NAME</u>	<u>DESCRIPTION</u>	<u>SOURCE</u>
2	1	(RESERVED)		-
3				-
5	4	R/W DATA +	Bi-directional Read/Write Data	C/D
6		R/W DATA -		
8	7	DS1/	Drive Select (encoded)	C
10	9	DS0/		
12	11	BUSEN/	Bus Strobe	C
14	13	BA1/	Bus Address (encoded)	C
16	15	BA0/		
18	17	ENABLE/	Bus Enable	C
20	19	(RESERVED)		-
22	21	BUS 7/	Data Bus	C
24	23	BUS 6/		
25		TV	Termination Voltage	C
26		TV		
28	27	BUS 5/	Data Bus	C
30	29	BUS 4/		
32	31	BUS 3/		
34	33	BUS 2/		
36	35	BUS 1/		
38	37	BUS 0/		
40	39	RDY/		
42	41	FLT/	Fault Status	D
44	43	ILADR/	Illegal Head/Cylinder Status	D
46	45	SKCMP/	Seek Complete Status	D
48	47	IDX/	Index Pulse	D
50	49	SECP/	Sector Pulse	D

Mating Connectors: J1 3M 3415-0001
J101 3M 3425-0000

Recommended Cable: 3M 3365/50

FIGURE 7. DRIVE INTERFACE J1/J102

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.
A		100292
SCALE		SHEET 29 OF

APPLICATION

REVISIONS

J101
CONNECTOR PIN

<u>SIG</u>	<u>GND</u>	<u>NAME</u>	<u>DESCRIPTION</u>	<u>SOURCE</u>	
2	1	BUS7/	(most significant)	H/C	
4	3	BUS6/		H/C	
6	5	BUS5/		H/C	
8	7	BUS4/		Bi- Directional	H/C
10	9	BUS3/		Data Bus	H/C
12	11	BUS2/			H/C
14	13	BUS1/			H/C
16	15	BUS0/	(least significant)	H/C	
18	17	ATTN/	Attention	C	
20	19	DATA/	Data/Control Select	H	
22	21	RSTR/	Read Strobe	H	
24	23	WSTR/	Write Strobe	H	
26	25	ENABLE/	Controller Enable	H	
28	27	SEL/	Controller Select	H	
30	29	CBUSY	Controller Busy	C	
32	31	DREQ/	Data Request	C	
34	33	OUT/	Direction of Data Transfer	C	

Mating Connector: 3M 3463-0001

Recommended Cable: 3M 3365/34

FIGURE 8. HOST INTERFACE, J101 -- PINOUTS

MICROPOLIS™

SIZE

CODE IDENT NO.

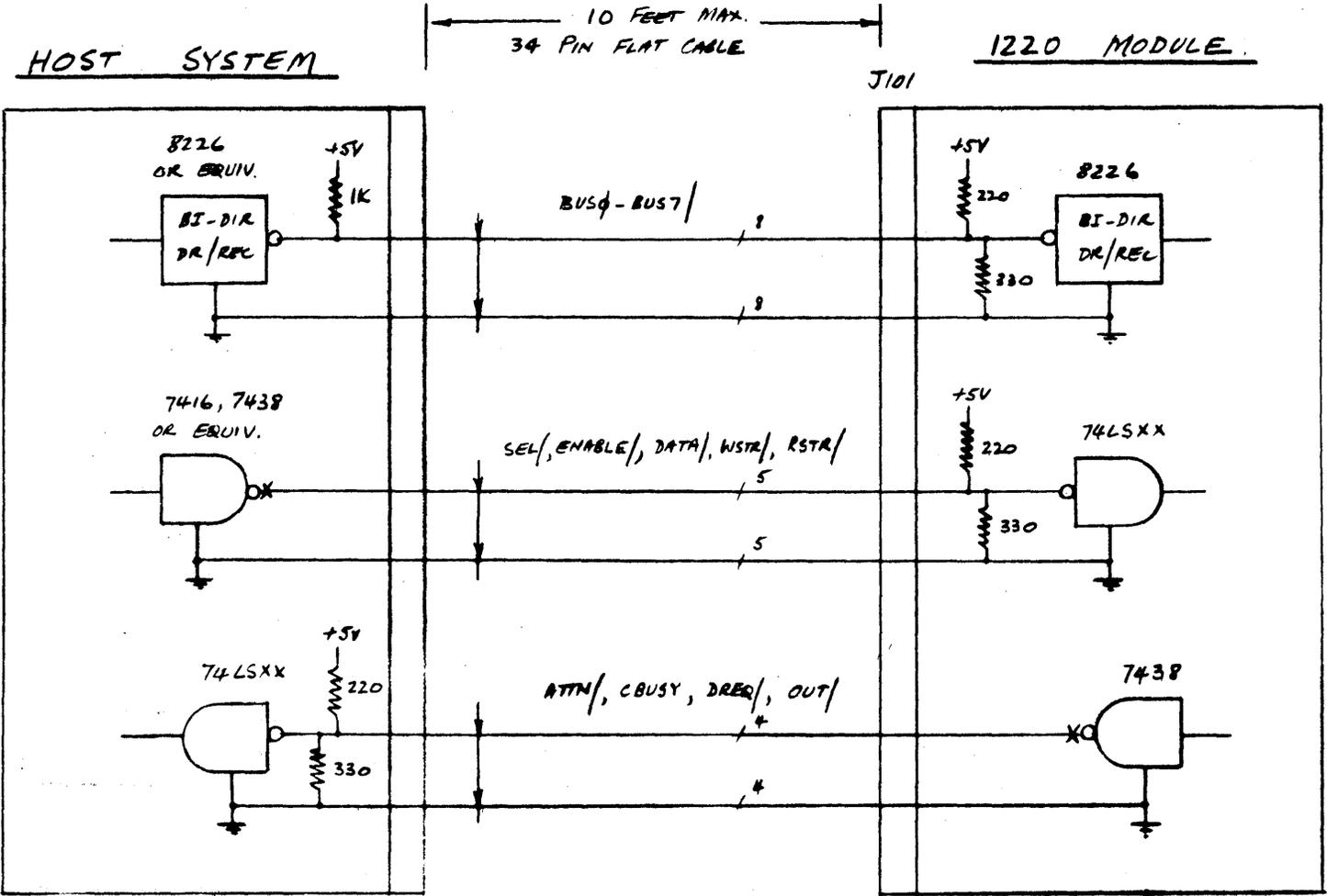
DWG NO.

A

100292

SCALE

SHEET 30 OF



- NOTES:**
1. ALL SIGNAL LINES (EXCEPT CBUSY) ARE LOW TRUE AT INTERFACE CONNECTOR AND HIGH TRUE INTO DRIVERS AND OUT OF RECEIVERS.
 2. INTERFACE SIGNAL LEVELS ARE LOW = 0-0.4V @25ma
HIGH = 2.5-5.0V @ 0ma
 3. HOST SHOULD PROVIDE 1K Ω PULLUPS ON BUS0/-BUS7/ AND 220/330 Ω TERMINATIONS ON ATTN/, CBUSY, DREQ/, OUT/.
 4. 220/330 Ω TERMINATORS ARE INSTALLED IN LAST 1220 MODULE ONLY.

FIGURE 9. HOST INTERFACE, J101 -- ELECTRICAL.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE			SHEET 31 OF

APPLICATION	REVISIONS
-------------	-----------

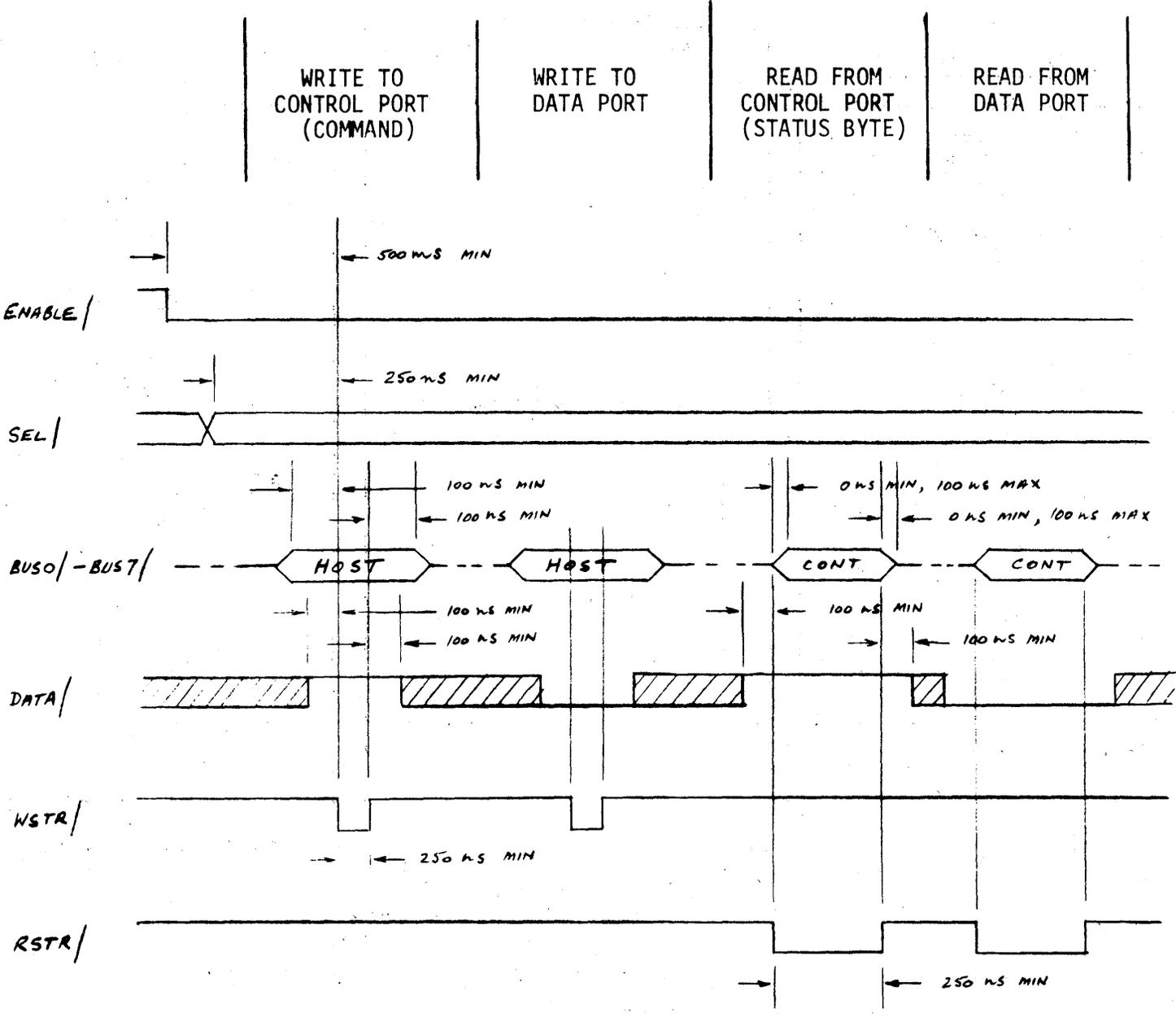


FIGURE 10. HOST INTERFACE, J101 -- BUS TIMING.

MICROPOLIS™			
SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 32 OF	

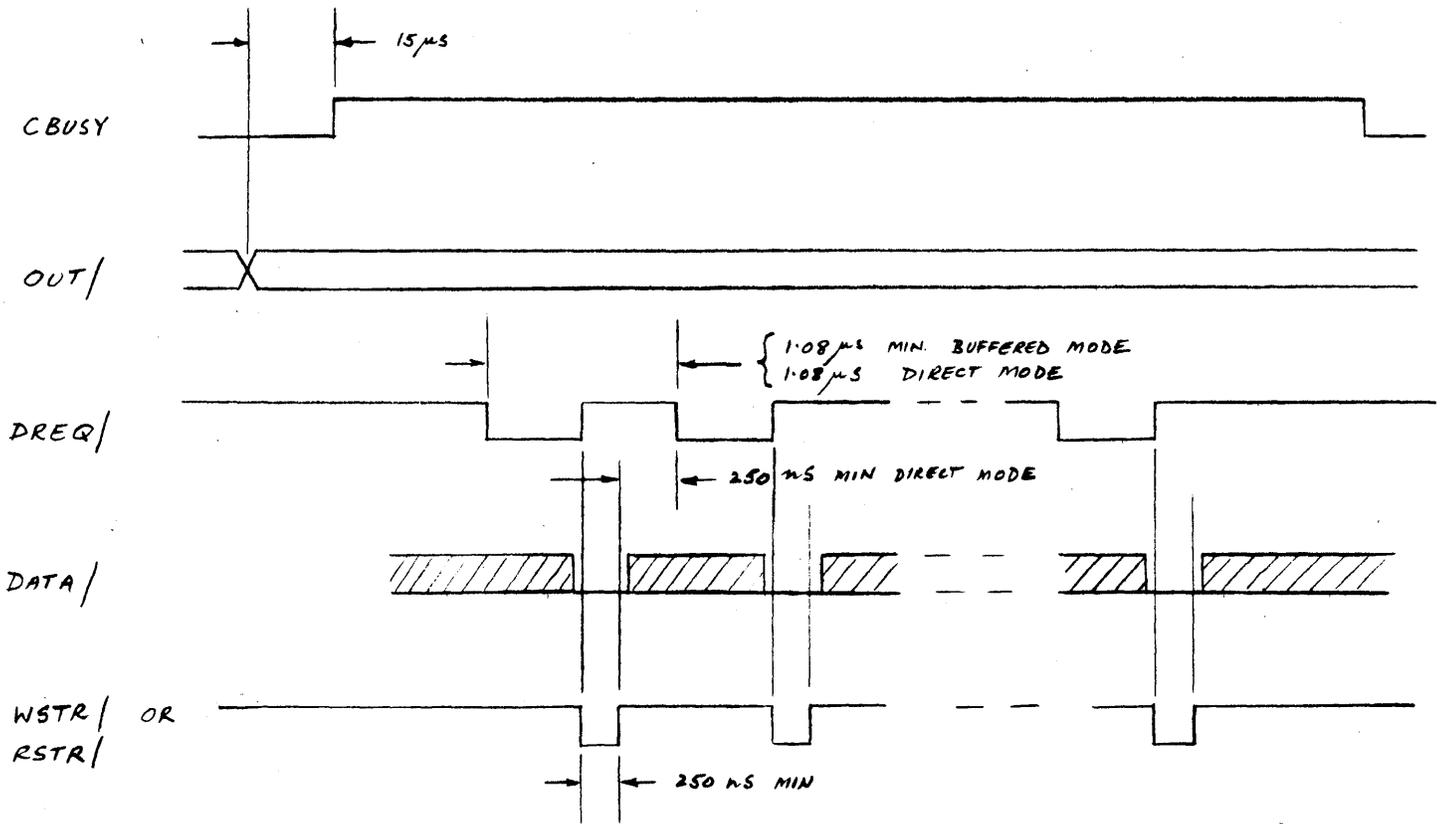
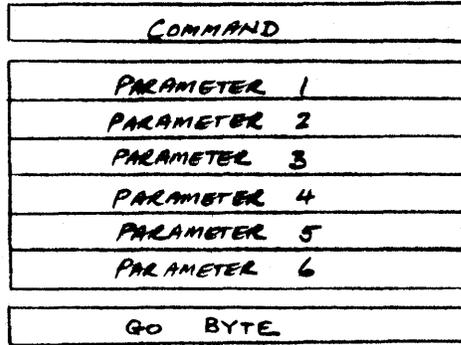


FIGURE 11. DATA BYTE TRANSFER TIMING.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292	
SCALE			SHEET 33 OF

CONTROL PORT



DATA PORT

COMMAND SEQUENCE

7	6	5	4	3	2	1	0
R	S		CMD			0	1
T	E						
O	E						

CLASS 1 COMMANDS

- CMD CODE = 0 DR. STATUS 4 INITIALIZE TRACK
 1 SEEK ONLY 5 VERIFY FORMAT
 2 READ HEADER 6 INIT & VFY
 3 RESTORE 7 FAULT RESET

7	6	5	4	3	2	1	0	
R	S	D	T	CMD			1	0
T	E	I	R					
O	E	R	A					

CLASS 2 COMMANDS

- CMD CODE = 0 CORRECT 2 READ WITH ACO
 1 READ WITH DCO 3 NORMAL READ

7	6	5	4	3	2	1	0
R	S	D	T	R	W	1	1
T	E	I	R	R	E		
O	E	R	A	A	E		

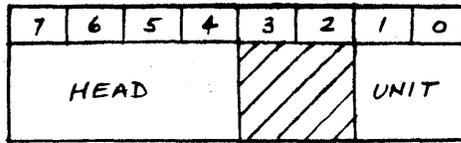
CLASS 3 COMMANDS

- WRITE = 0 VERIFY
 1 WRITE

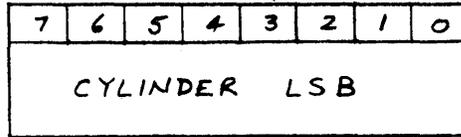
FIGURE 12. COMMAND BYTE CODING.

MICROPOLIS™

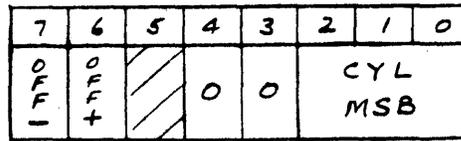
SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 34 OF	



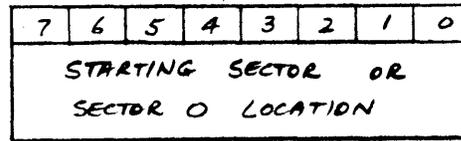
PARAMETER BYTE 1



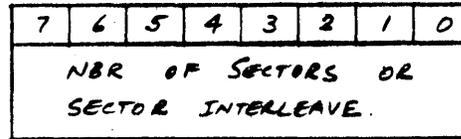
PARAMETER BYTE 2



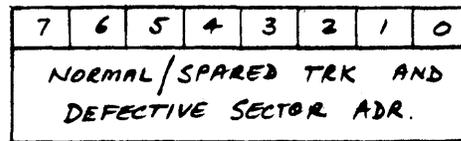
PARAMETER BYTE 3



PARAMETER BYTE 4



PARAMETER BYTE 5

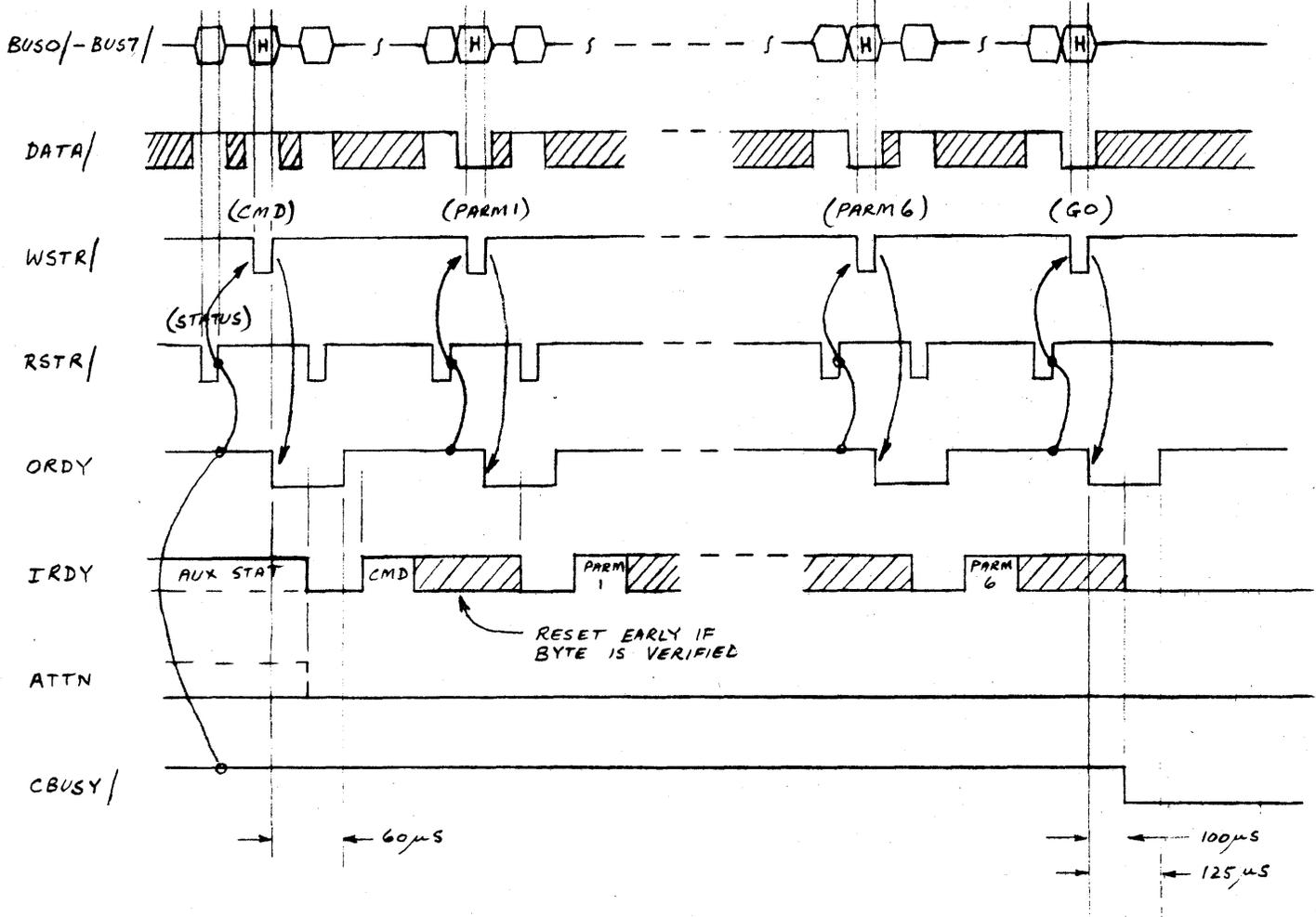


PARAMETER BYTE 6

FIGURE 13. PARAMETER BYTE CODING.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292	
SCALE		SHEET 35 OF	



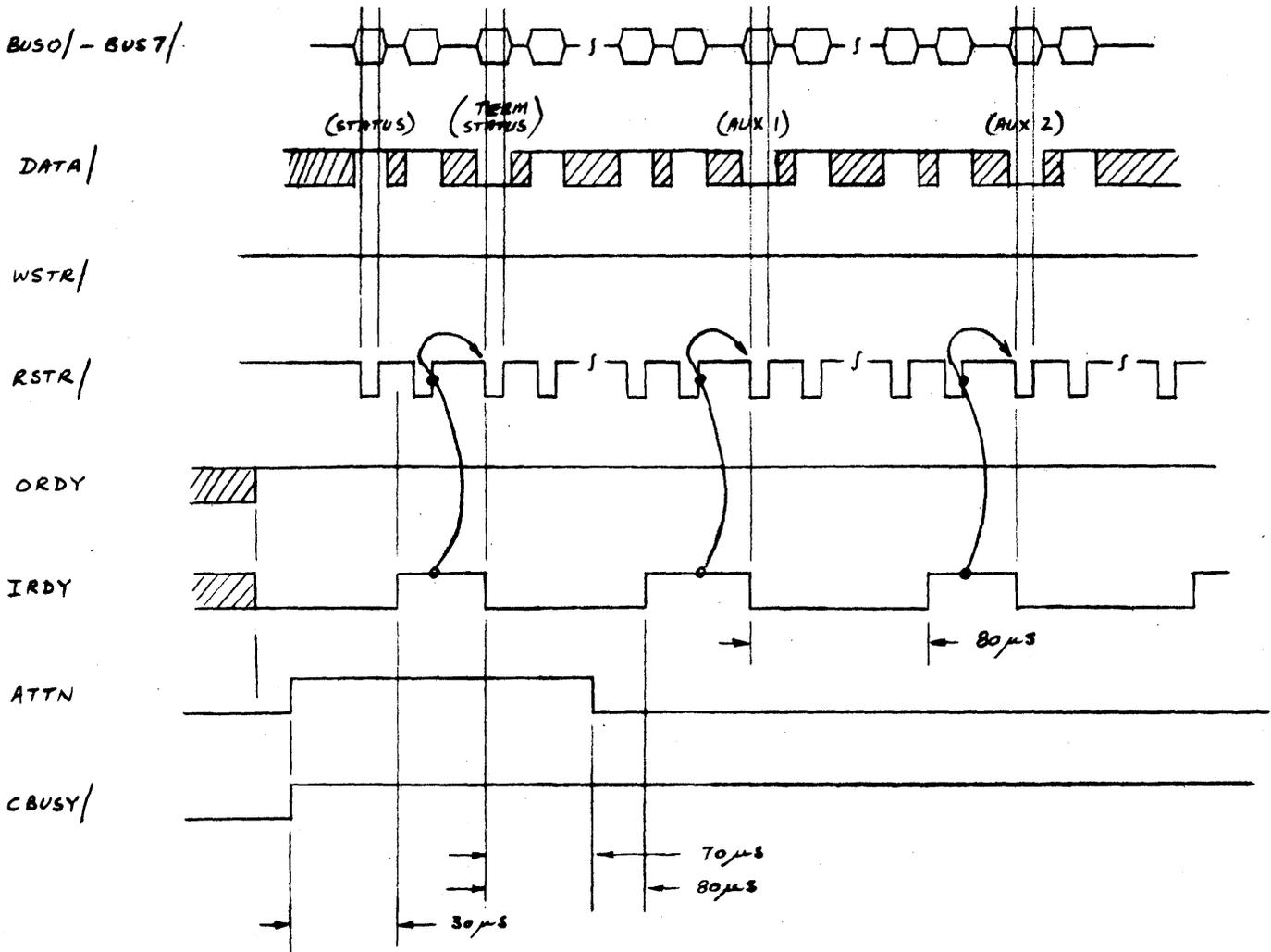
TIMES ARE APPROXIMATE.

COMMAND VERIFY PROTOCOL IS NOT SHOWN.

FIGURE 14. BUS PROTOCOL - COMMAND INITIATION.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292
SCALE	SHEET 36 OF	



TIMES ARE APPROXIMATE.

FIGURE 15. BUS PROTOCOL - COMMAND TERMINATION.

MICROPOLIS™

SIZE A	CODE IDENT NO.	DWG NO. 100292	
SCALE			SHEET 37 OF

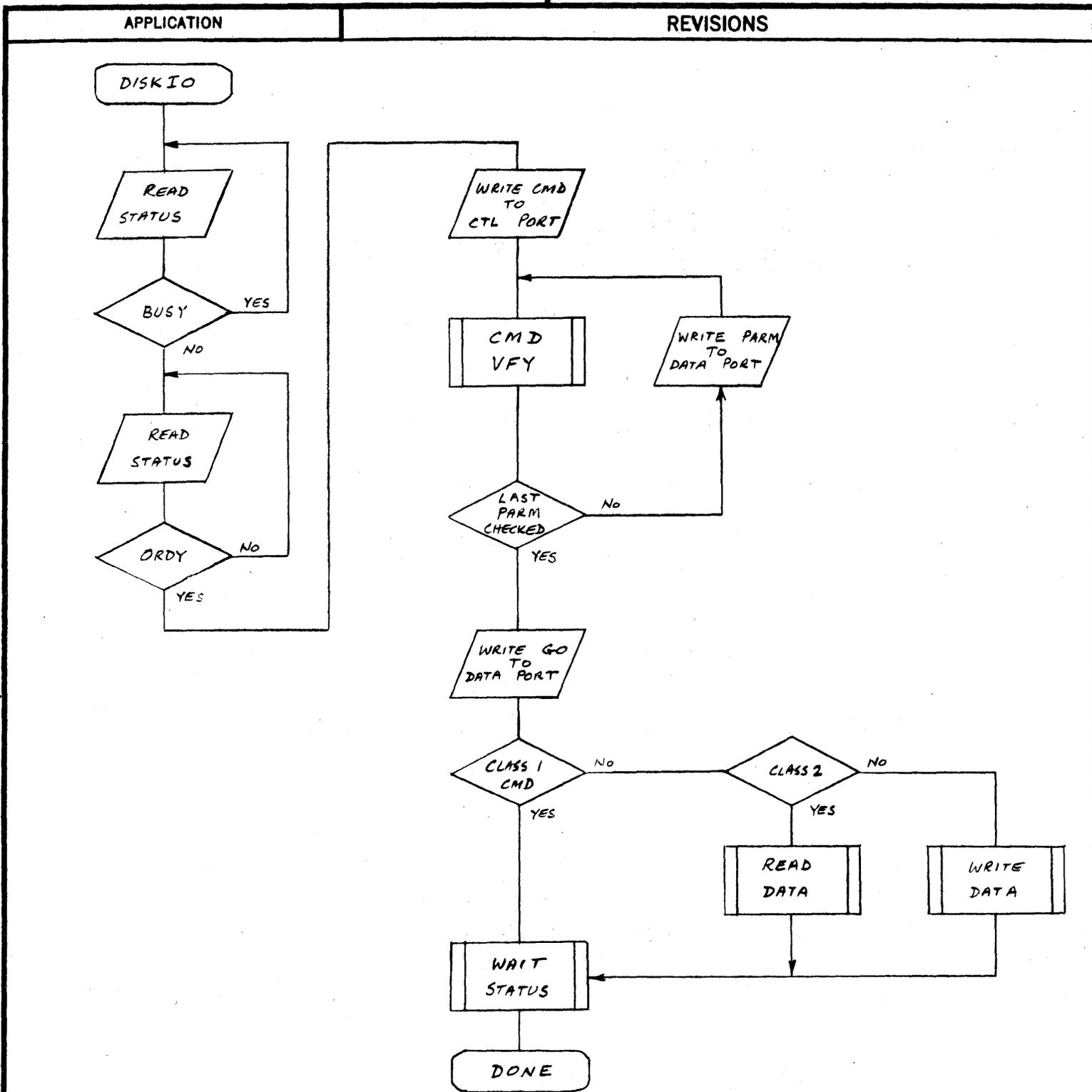


FIGURE 16a HOST IO PROTOCOL.

MICROPOLIS™			
SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 38 OF	

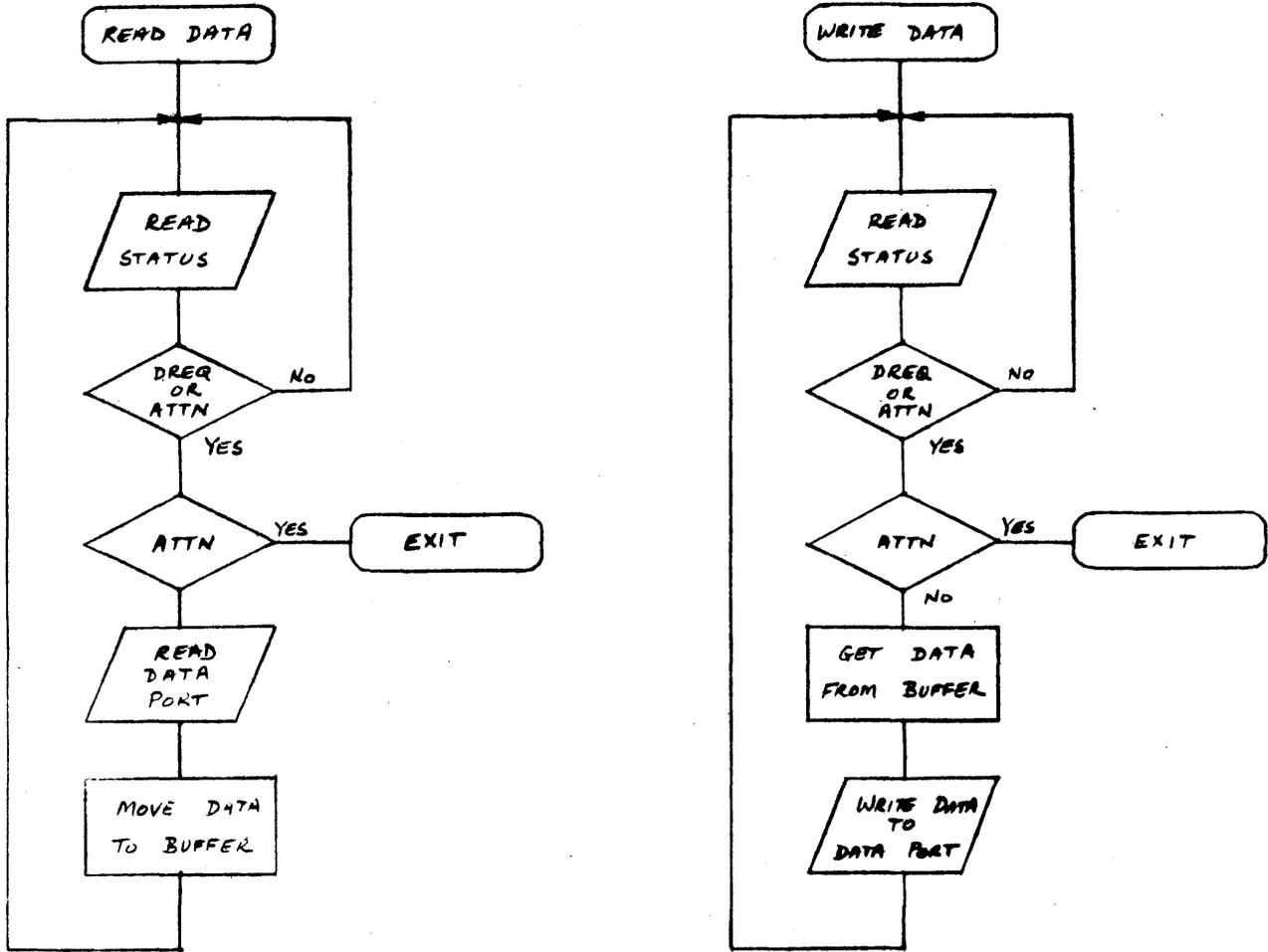


FIGURE 16b HOST IO PROTOCOL.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 39 OF	

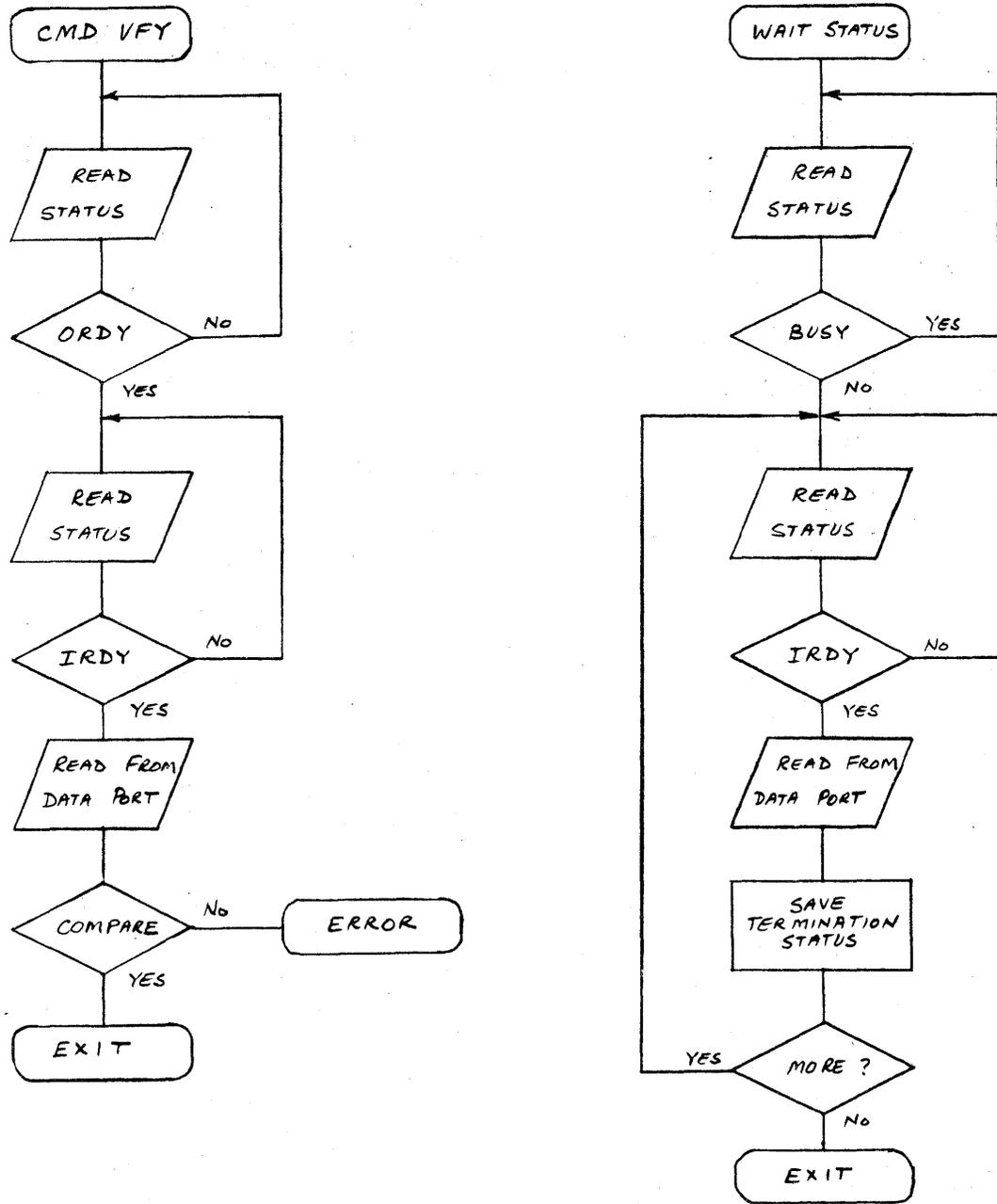


FIGURE 16c HOST IO PROTOCOL.

MICROPOLIS™

SIZE	CODE IDENT NO.	DWG NO.	
A		100292	
SCALE		SHEET 40 OF	