

**MICROPOLIS  
MAINTENANCE MANUAL  
FLOPPY DISK SUBSYSTEM**

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### GENERAL INFORMATION

#### 1.1 SCOPE OF MANUAL

This manual contains maintenance information on Floppy Disk Storage subsystem family, Model Numbers 1021 through 1057 manufactured by Micropolis, Canoga Park, California. The manual provides data to aid in maintaining the equipment. This includes some installation and operation instructions. For detailed information on installation and operation refer to the appropriate user's manual on the equipment. The manual consists of nine sections, as follows:

*Section 1, General Maintenance Information*, presents information that the user may find helpful, without requiring detailed technical involvement into the unit operation and structure. General information about maintenance philosophy, operator troubleshooting, maintenance, and service information are presented in this section.

*Section 2, Installation and Operation*, supplies information needed to install and operate the equipment. The section contains figures that specify the installation requirements for the subsystems, and text that informs the user on recommended wiring practices for the equipment as well as defines electrical connections peculiar to each type of subsystem configuration. Also included are instructions for reconfiguring the controller for special applications, and memory addresses.

*Section 3, Theory of Operation*, gives the maintenance personnel a detailed explanation of the internal function of the subsystem. The circuit theory is based on block diagrams and logic diagrams that show the functional elements of the unit. Each element operation is described, first in relation to other elements, then independently where its major components' use and purpose are described. Single and double drive operation is described individually to facilitate comprehension.

*Section 4, Tests and Adjustments*, offers a complete list of tests and adjustments that can be performed on the unit to check and ensure proper operation.

*Section 5, Troubleshooting*, lists the necessary procedures to fault-isolate the drive and its as-

sociated PCBA.

*Section 6, Parts Replacement*, defines the operations necessary to remove and replace components and subassemblies.

*Section 7, Parts Lists*, specify the location of all the parts referred to in the publication.

*Section 8, Micropolis Diagnostic*, describes the features and operation of the Micropolis Diagnostic program references in the manual.

*Section 9, Schematic and Assembly Drawings*, provide the detailed PCBA component locations, circuit diagrams, and electrical interconnections of the equipment.

#### 1.2 EQUIPMENT DESCRIPTION

Each model number is followed by either the notation MOD I or MOD II. These notations indicate whether the system operates at a track density of 48 Tracks Per Inch (TPI) (35 tracks total) or 100 TPI (77 tracks total) respectively. MOD I storage modules typically have a black disk load actuator, and MOD II modules have a blue disk load actuator. The models covered in this manual are described in Figure 1-1 and Table 1-1.

#### 1.3 INTERFACE CABLES

The standard Interface Cable A (1083-01) is 54" (137 cm) long and uses 34-wire flat cable with card edge connectors at each end. Pin 1 is indicated by a contrasting wire color along the appropriate edge. This cable is used to connect the controller directly to any single storage module (which can in turn contain one or two disk drives). When two or more storage modules are to be connected to the controller, the appropriate Daisy Chain cable must be used in place of the standard Cable A.

Daisy Chain Type	Model	Total Connectors	Total Storage Modules
B	1083-02	3	2
C	1083-03	4	3
D	1083-04	5	4

**TABLE 1-1. SUBSYSTEMS IDENTIFICATION**

Model No. (See Note 1)	Capacity Per Module Formatted	Tracks/ Inch	Single/Dual Module	With/Without Power Supply
1057(1037)	287 KB	48	Dual	With
1053(1033)Mod II	630 KB	100	Dual	With
1043(1023)Mod II	315 KB	100	Single	With
1042(1022)Mod I	143 KB	48	Single	With
1041(1021)Mod I	143 KB	48	Single	Without (See Note 2)
1041(1021)Mod II	315 KB	100	Single	Without (See Note 2)

**Note 1.** Models without parentheses are master modules used with a 1071 controller, and interface Cable A. All models in parentheses are add-on modules only.

**Note 2.** Includes power cable for connection to external power supply.  
Each model number is followed by either the notation Mod I or Mod II. These notations indicate whether the system operates at a track density of 48 tpi (35 tracks total) or 100 tpi (77 tracks total per drive).



**NOTE:** MOD I FEATURES A 48TPI CAPABILITY  
MOD II FEATURES A 100TPI CAPABILITY

**Figure 1-1. Micropolis Floppy Disk Subsystems**

The maximum number of storage modules that can be daisy chained to a single controller is four. This can be any combination of single and dual modules with the limitation that the total number of *drives* that can be daisy chained is four.

#### 1.4 IDENTIFICATION PLATE

An identification plate is located on the base chassis (bottom of unit). It shows model number, serial number, line voltage and fuse rating. Both model number and serial number should always be quoted in warranty correspondence.

#### WARNING

**This equipment is provided with a 3 pin power plug. The plug must be inserted in a 3 pin receptacle with the third pin connected to earth ground.**

**When replacing the fuse always use a fuse of the same type and rating. These are:**

Operating Voltage Range VAC RMS	Fuse Type	Ampere Rating	Voltage Rating	Littelfuse Part Number	Micropolis Part Number
100 to 125	3AG SLO-BLO	1.0	250	313001	626-0002-8
200 to 240	3AG SLO-BLO	0.5	250	313.500	626-0001-0

#### 1.5 SPECIFICATIONS

##### DRIVE PERFORMANCE

Capacity per drive (when used with 1071 controller)  
 MOD II: 315K bytes, formatted  
 MOD I: 143K bytes, formatted  
 Number of sectors: 16 (when used with 1071 controller)  
 Transfer rate: 250K bits/second

Average rotational latency time: 100 milliseconds (ms)

Access time  
 Track-to-track: 30 ms  
 Settling time: 10 ms

Head load time: 75 ms

Head positioner: stepper motor with lead-screw drive

Drive motor start time: 1 second

Rotational speed: 300 rpm

Recording density:  
 5248 bits per inch (BPI) MOD II  
 5162 bits per inch (BPI) MOD I

Recording mode: MFM

Track density  
 MOD II: 100 tracks per inch (TPI)  
 MOD I: 48 tracks per inch (TPI)

Surfaces used per diskette: 1

##### ENVIRONMENTAL

Operating temperature: 50° to 104°F, 10° to 40°C

Relative humidity: 20% to 80% (without condensation)

##### DRIVE RELIABILITY

MTBF	8000 hr/spindle
MTTR	0.5 hr
Media Life	3 x 10 <sup>6</sup> passes on single track
Head Life	10,000 hr
Soft Error Rate	1 in 10 <sup>9</sup>
Hard Error Rate	1 in 10 <sup>12</sup>
Seek Error Rate	1 in 10 <sup>6</sup>

## 1.6 PHYSICAL DESCRIPTION AND DIMENSIONS

### 1057/1037 DUAL DISK DRIVE MODULE

Height	8.0"	20.3 cm
Width	9.2"	23.4 cm
Depth	13.0"	33.0 cm
Weight	18 lb	8.2 Kg

Input Power requirements: 115/230V AC, 50/60 Hz.  
Standby 60 VA; Operating 78 VA.

### 1043/1023 AND 1042/1022 SINGLE DISK DRIVE MODULE

Height	4.0"	10.2 cm
Width	5.9"	15.0 cm
Depth	12.2"	31.0 cm
Weight	9.0 lb	4.1 Kg

Input Power requirements: 115/230V AC, 50/60 Hz.  
Standby 30 VA; Operating 45 VA.

### 1041/1021 SINGLE DISK DRIVE MODULE (WITHOUT POWER SUPPLY)

Height	4.0"	10.2 cm
Width	5.9"	15.0 cm
Depth	9.6"	24.3 cm
Weight	5.0 lb	2.3 Kg

Input Power requirements: +5V  $\pm 5\%$  regulated  
0.5A; +12V  $\pm 5\%$  regulated 1.15A.

### 1071 CONTROLLER

The MFM controller is a single printed circuit board, physically and electrically compatible with S-100 bus and 8080/Z80 microcomputers. It utilizes 16 sectors and 256 data bytes per track and will operate at either 2 or 4 MHz.

Height (not including the edge connector to the motherboard):

Height	5.0"	12.7 cm
Width	10.0"	25.4 cm

The edge connector for the interface cable is recessed to keep the overall height at 5.0" when the cable is connected.

## 1.7 MAINTENANCE PHILOSOPHY

Two important design considerations were incor-

porated into the entire Micropolis product line; freedom from mandatory preventive maintenance in normal use, and simplification of corrective maintenance actions. To the latter end all modules, whether dual or single, 48 TPI or 100 TPI, make use of similar drive mechanisms easily removed from their enclosures for service or replacement. The drive mechanism is modularized with readily replaceable modules or subassemblies requiring little or no adjustment.

### 1.7.1 End User Maintenance

The isolation and correction of faults within the module, or on the controller PCBA, requires sophisticated test equipment and moderate experience in the field of analog and digital troubleshooting. Unless you have been trained by Micropolis and have the necessary tools and equipment you should make no attempt to perform critical adjustments, tests, or replace components. If the checks on the following page do not isolate or correct the fault and you are not qualified to service the equipment, the subsystem should be returned to *the store from which it was purchased*.

### 1.7.2 Dealer Service Centers

Micropolis dealers receiving formal training on the theory of operation and maintenance of Micropolis subsystems, and possessing adequate test equipment and spare parts are designated as Micropolis Service Centers. These Service Centers are best able to provide high quality and timely warranty and nonwarranty service on Micropolis products. If you wish to obtain information on which dealers, in your area, are designated as Service Centers, or wish to obtain more information on becoming a Service Center, contact Micropolis Technical Marketing.

### 1.7.3 Repair Depot

Micropolis maintains a fully equipped repair depot which provides warranty and nonwarranty repairs and emergency spares support. Contact Micropolis Customer Service to obtain a Return Good Authorization (RGA) prior to returning any module or controller for repair.

## 1.8 PREVENTIVE MAINTENANCE

Your Micropolis disk memory system does not require preventive maintenance when used in a normal environment (dustfree 65° to 80°F ambience), 8

**END USER TROUBLESHOOTING CHART**

<b>Symptom</b>	<b>Probable Cause/Corrective Action</b>
On dual subsystem, displays do not light (with door open); on single subsystem motor does not turn and select light never lights.	1. No power to module. Check electrical outlet, check fuse in back of module, check serial number plate (bottom of module) for correct line voltage.
On dual module, displays go out when door is closed. On dual and single modules, select light never lights.	1. Interface cable is not plugged into controller. 2. Controller is not plugged into computer or computer is not turned on. 3. Computer power supply voltages are incorrect.
On dual and single module, drive is <i>always</i> selected.	1. Interface cable is upside down.
On dual and single modules, system cannot be booted (careful adherence to the procedure in the users manual has been followed).	1. Inadequate memory — the memory requirements for the high data transfer rates associated with the Micropolis subsystem may exceed the capabilities of the computer's memories. Substitute different manufacture of RAM in computer. 2. Bootstrap PROM address conflict. Remove all other controllers and/or refer to Section II on readdressing controller.
On dual and single subsystems, permanent I/O errors.	1. Inadequate memory (see above). 2. MPU (CPU) timing problems — there are many changes/improvements that have been made to various brands of microcomputers to improve operation with disk memory systems. Refer to Micropolis Product Support and/or the computer manufacturer to determine whether these changes have been incorporated in your system. 3. Drive module fault (substitute a known good module). 4. Controller fault — substitute a known good controller.
<b>NOTE:</b> This chart is intended only as a first level diagnostic aid. Section V contains a more thorough guide for qualified service personnel.	

hours/day or less power on/motor running and a head load cycle of 25% or less. If operating conditions exceed normal, then preventive maintenance as authorized in Table 1-2 should be performed.

Clean the magnetic head, using a lint-free cloth or cotton swab moistened with isopropyl alcohol or DuPont Freon TF. Wipe the head carefully to remove all accumulated oxide and dirt. Dry the head using a lint-free cloth.

**1.9 CLEANING AND LUBRICATION**

**1.9.1 Cleaning the Head**

**CAUTION**

ROUGH OR ABRASIVE CLOTH SHOULD NOT BE USED TO CLEAN THE MAGNETIC RECORDING HEAD. USE ONLY ISOPROPYL ALCOHOL OR DUPONT FREON TF. USE OF OTHER CLEANING SOLVENTS, SUCH AS CARBON TETRACHLORIDE, MAY DAMAGE THE HEAD LAMINATION ADHESIVE.

**NOTE**

The magnetic head must be cleaned after head load pad replacement.

**1.9.2 Lubrication of the Stepper Motor Lead Screw**

Prior to lubrication, the stepper motor shaft (lead screw) should be cleaned. Wipe the shaft with a lint-free cloth lightly moistened with isopropyl alcohol. Lubricate the lead screw and portion of the carriage

**TABLE 1-2. PREVENTIVE MAINTENANCE SCHEDULE UNDER SEVERE OPERATING CONDITIONS**

Maintenance Operation	Frequency	Time Required Hours	Manual Paragraph Reference
Replace Head Load Pad(s)	2000 hrs of diskette access	0.1	6.5
Clean Head(s)	2000 hrs of diskette access	0.1	1.9.1
Replace Drive Motor(s)	5000 hrs of motor operation	0.5	6.4
Lubricate Lead Screw(s)	2000 hrs of diskette access	0.1	1.9.2
Lubricate Latch Mechanism	Every 2 years or whenever latch operation becomes erratic	0.1	1.9.3

that rides on the platen by applying a liberal portion of Saunders Magnalube Micropolis P/N 732-0001-6 to these surfaces.

**CAUTION**

DO NOT CONTAMINATE MAGNETIC RECORDING HEAD OR HEAD PAD WITH LUBRICANT. DAMAGE TO THE RECORDING SURFACE CAN BE CAUSED BY LUBRICANT DEPOSITED ON THE MAGNETIC HEAD OR LOAD PAD BEING TRANSFERRED TO THE DISK.

**1.9.3 Lubrication of the Latch Mechanism**

To ensure smooth positive action of the door latch mechanism, apply a heavy coat of Saunders Magnalube Micropolis P/N 732-0001-6 to the entire latch mechanism.

**1.10 CORRECTIVE MAINTENANCE**

Corrective maintenance consists of isolating a malfunction first to the major assembly (i.e., power supply, drive electronics, drive mechanism, or controller), then to the defective or misadjusted component. The component is then replaced and the required adjustment and tests performed. The following sequence serves as a guide to making the most effective use of this manual.

- a. Isolating the malfunction to the correct assembly: See Section 5, Troubleshooting Chart.
- b. Isolating the malfunction to the correct com-

ponent or subassembly: See Section 5, Troubleshooting Tables 5-2 or 5-3.

- c. Understanding how the circuit, mechanical, or electrical component operates: See Section 3, Theory of Operation.
- d. Testing the circuit or mechanical component: See Section 4, Tests and Adjustments, Section 8, Micropolis diagnostic test program, Section 9, Schematics and Assembly Drawings.
- e. Ordering a part or subassembly: See Section 7, Parts List.
- f. Replacing the defective component or subassembly: See Section 6, Parts Replacement.
- g. Testing and/or adjusting the circuit/mechanism after replacing the part: See Section 4, Tests and Adjustments.

Before beginning major corrective maintenance activity it should be remembered that most computer system malfunctions which manifest themselves as inability to load a program, write or read, seek to a track, or perform other operations typically stem from nondisk system failures. The most common cause of such malfunctions are: insufficient memory, dirty memory board contacts, incorrect memory timing, conflicting PROM addresses, overloaded bus power supplies, and excessive bus noise. Prior to troubleshooting the disk module or controller, if possible, determine, by substitution of either the computer main frame, disk module or controller, whether the fault lies in the computer or in components of the disk subsystem.

## 1.11 TEST EQUIPMENT

The following test equipment is recommended for servicing Micropolis disk subsystems:

- a. Oscilloscope — Tektronix 453 or equivalent
- b. Digital Multimeter — Simpson 461 or equivalent
- c. Frequency Counter — 0 to 10 MHz (optional)
- d. S100 Microcomputer (Z80, 8080, or 8085) System with Keyboard/Display

## 1.12 HAND TOOLS AND SPECIAL SERVICE SUPPLIES

The following tools and special items are required for servicing Micropolis disk subsystems:

3/16 nut driver	XCELITE A6, or equivalent
1/4 nut driver	XCELITE 8, or equivalent
Screwdriver, Phillips #1	VACO P-1, or equivalent
Tweezers	Clause 231, or equivalent
7/64 hex driver	Hunter 12035, or equivalent
7/64 hex key, long handle	Jacks Industrial Supply, or equivalent
3/32 hex key	Jacks Industrial Supply, or equivalent
Spring hook set	National Camera S1390, or equivalent
1/4 combination wrench	Bonney 1158H, or equivalent
5/16 box wrench	Bonney 1160H, or equivalent
3/8 box wrench	Bonney 1161H, or equivalent
Pot screwdriver	Bouvus H-90, or equivalent
Spring scale	0-10 lbs
Cotton swabs	
Freon TF	
Grease, Magnalube (Saunders)	Micropolis P/N 732-0001
C.E. alignment diskette	Dysan 282
Standoff	Micropolis P/N 100100-02-3

## 1.13 ALIGNMENT DISKETTE

The alignment diskette, referenced in Section 4, Tests and Adjustments, is a Dysan P/N 282. The following tracks of this diskette are used:

MOD I, Track 1	Index/Photocell alignment
MOD II, Track 5	
MOD I, Track 16	Radial "cat's eye" alignment (also reference track for absolute track positioning (i.e., correct Tk 0 switch setting)
MOD II, Track 36	
MOD I, Track 35	Used in conjunction with tracks 1 (I) or 5 (II) for setting of
MOD II, Track 76	

azimuth (perpendicular head movement)

The specification for this diskette should be obtained from Dysan.

## CAUTION

CARE SHOULD BE EXERCISED NOT TO ERASE THE PRERECORDED ALIGNMENT TRACKS. DO NOT DEFEAT THE WRITE PROTECT FEATURE OF THE DISKETTE OR DRIVE. DO NOT INSTALL THE DISKETTE IN A DRIVE WITH A SUSPECTED WRITE LOGIC FAILURE. NEVER UNPLUG THE DRIVE'S HEAD CONNECTOR WITH ANY DISKETTE INSTALLED.

## 1.14 MICROPOLIS DIAGNOSTIC PROGRAM

Frequent mention is made in Section 4, Tests and Adjustments, to a Micropolis Diagnostic Program. While not mandatory, this software does simplify performing the tests and adjustments and eliminates the need for a tester/exerciser. Section 8 of this manual describes the features and use of this program. The diagnostic software is available on a configurable diskette for both MOD I and MOD II subsystems. Copies of the diagnostic software are available from Micropolis Technical Marketing.

## 1.15 SPARE PARTS

### 1.15.1 Routine

Section 7 details the number and kind of spare parts, component and subassembly, recommended for maintenance of Micropolis subsystems. A minimal level of recommended spares should be stocked if continual maintenance is performed on these products.

Routine orders for spare parts should be placed through order entry, *not* customer service. Order for routine spares will be treated and scheduled in the same manner as an order for subsystems, accessories, etc.

### 1.15.2 Emergency Spares

Emergency spares will be shipped within 24 hours and will not be discounted. Emergency spare orders should be placed with Customer Service.

### INSTALLATION AND OPERATION

#### 2.1 INTRODUCTION

This section provides information necessary for unit preparation for operation or repair. The section also supplies data on mounting, interface, addressing and source power considerations. Special hook-up instructions on multiple drive operation are also included.

The disk subsystem hardware consists of 1 to 4 disk storage modules, an associated interface cable and a controller printed circuit board. Installing the subsystem is accomplished by unpacking and visually inspecting the equipment, configuring the controller as necessary for your particular computer system, installing the controller in the S-100 bus and connecting the storage modules to the controller. A diskette may then be loaded into the disk drive. Hardware installation must be complete before system software configuration can begin.

#### 2.2 UNPACKING THE EQUIPMENT

The subsystems are shipped in a protective container which meets the National Safe Transit Specification (Project 1A, Category 1). The container is designed to minimize the possibility of damage during shipment.

The following procedure describes the recommended method for unpacking the elements of the subsystem.

- a. Place the shipping container on a flat work surface.
- b. Cut the sealing tape on the container top carefully; open the top flaps.
- c. Remove the User's Manual shipping box (12" X 12" X 2") and the controller box (12" X 6" X 1") and set aside. Not applicable to add-on units.
- d. For a Dual Disk Module Shipment, slide the Disk Module still supported by the 3" foam end pieces carefully out of the container. It will be necessary for the container to be held while this takes place.

For a Single Disk Module shipment, remove the module box from the outer shipping container. Cut open the tape sealing the top of the box, open the top flaps and carefully remove the Disk Module. For 1041/1021 Modules, the interface cable, power cable and optional regulator kit will be packed in the module box.

#### NOTE

Retain the packing materials in case it is necessary to return the equipment to the source or supplier. Do not attempt to ship the equipment except in the original packing.

#### 2.3 VISUAL CHECKOUT

Open the plastic bag enclosing the Disk Module and the controller box and inspect for shipping damage. If shipping damage is evident, call the origin of the shipment: typically, the dealer from whom the equipment was purchased or shipped (or Micropolis in the case of a direct factory sale).

#### NOTE

Do not return the damaged equipment until the shipping company inspector has reviewed the damage, since an insurance claim must be made by the receiving party.

Ensure that the model number on the identification plate is as ordered. If a Mod II (high capacity) drive was ordered check that the disk load actuator on the front of the drive is blue; for a Mod I the actuator is black. (May not be applicable on some models.)

#### 2.4 MOUNTING OF THE DRIVE MODULE

##### 2.4.1 All Modules Except 1021/1041

With the exception of the 1021/1041 all Micropolis Disk Subsystem modules are designed for desk top mounting. The following guidelines should be followed:

- a. Ensure that the louvered holes in the case are not obstructed.
- b. Do not exceed the rated ambient temperature of 50°–105°F.
- c. Do not place the module close to sources of strong electromagnetic or electrostatic fields (i.e., large transformers, CRTs, motors, etc.).
- d. Avoid excessively dirty or dusty areas.
- e. Avoid static discharging to any part of the system (use anti-static spray on carpets).
- f. Ensure that the line voltage is within specification *and* that the ground pin is actually connected to earth.

#### 2.4.2 Custom Mounting of the 1041/1021 Module

The 1041/1021 disk drive is enclosed in a protective sleeve with four rubber feet installed for desk-top use. The rubber feet may be peeled off for custom mounting, such as in the front panel of a computer main frame.

The following guidelines are recommended.

Refer to Figure 2-1.

- a. The drive may be mounted in any orientation except up-side down. If the drive is to be mounted bezel up, it should be ordered as such so that the disk eject system can be suitably adjusted.
- b. Use the recommended panel opening and insert the drive through the panel opening from the front.
- c. On no account should the mounting scheme rely on the plastic bezel for support.
- d. When mounting the drive with the width dimension (5.9") vertical, use the outside two screws (Ref. Figure 2-1.) on the appropriate side and two spacers to secure the drive to the base chassis.
- e. Spacers should be at least 0.5" outside diameter.

The screws should be of such a length as to not protrude more than 0.2" into the inside of the drive.

The holes in the chassis base to which the drive is mounted should have adequate clearance to take up tolerances. This precludes the use of flat head screws.

When mounting the drive with the width dimension (5.9") horizontal, use brackets made of 0.060 min. steel mounted to the chassis base to secure the drive in four places using the outside two screws on both sides (Ref. Figure 2-1).

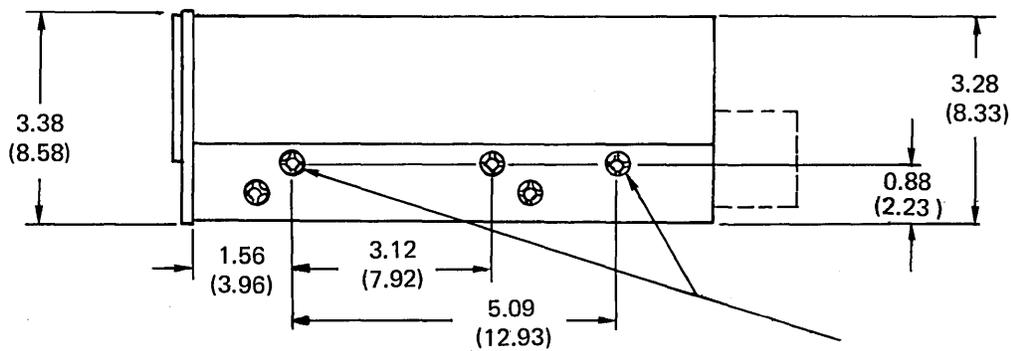
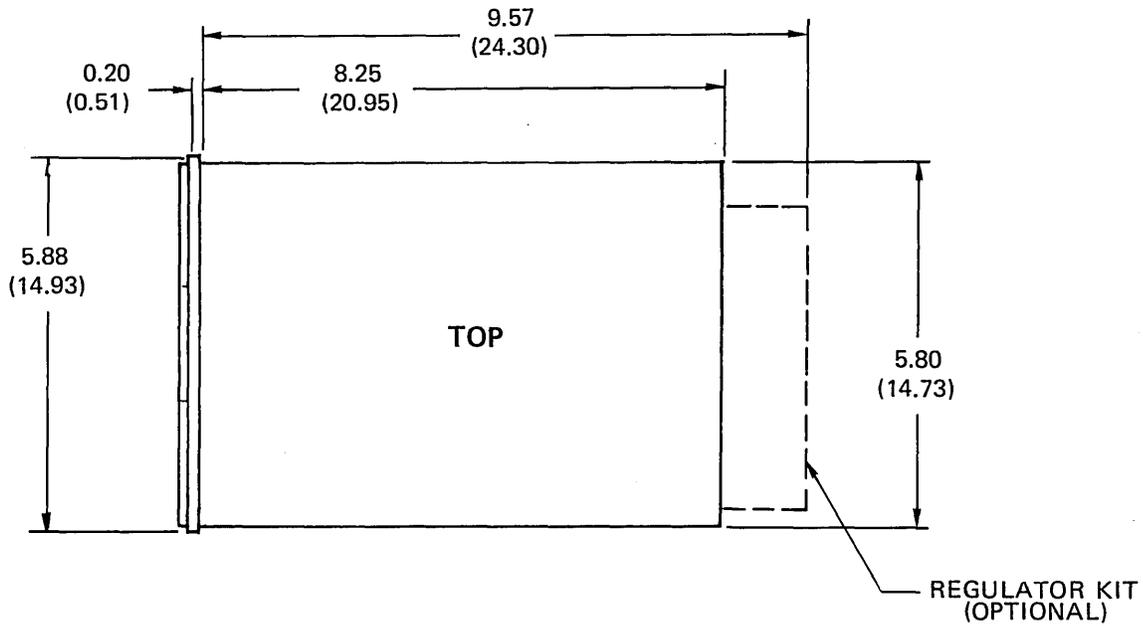
Holes in the brackets should have adequate clearance so that when all screws are tight, stress is not communicated to the drive.

## 2.5 CONTROLLER

### 2.5.1 Controller Interfacing

The disk controller board is accessed as a 1K block of memory using memory-mapped I/O. This addressing scheme leaves the full 256 standard I/O addresses for user devices. The controller is implemented as a "software controller"; most of the work required to access the disk is performed in software. The operation of the primitive read/write and timing loops depends upon instruction timing, which places the following restrictions on the system environment:

- a. RAM memory must be fast enough to operate without wait states. This implies 450 nsec or less access time with a 2-MHz system clock.
- b. If dynamic RAM is used, the overhead for refresh must not be more than 1 CPU clock cycle per 32 usecond period. The refresh logic must operate properly with approximately 18 usec/32 usec period spent in wait states. (The controller synchronizes disk transfers by asserting the PRDY line.)
- c. Interrupts are disabled during disk I/O operations.
- d. No cycle-stealing DMA devices may be in operation during disk I/O operations.
- e. The first 512 bytes of the 1K controller address space are allocated to the bootstrap, which is implemented in a 70 nsec ROM. The controller is mapped into the last 512 bytes.



6-32 HOLE. THREE PER SIDE. OUTSIDE TWO SCREWS ON EACH SIDE MAY BE REMOVED AND HOLES CAN BE USED FOR EXTERNAL MOUNTING.

SUGGESTED PANEL OPENING:

5.825  $\begin{matrix} +0.010 \\ -0.005 \end{matrix}$  BY 3.305  $\begin{matrix} +0.010 \\ -0.005 \end{matrix}$  INCHES

14.795  $\begin{matrix} +0.025 \\ -0.012 \end{matrix}$  BY 8.395  $\begin{matrix} +0.025 \\ -0.012 \end{matrix}$  CM

INCHES  
(CM)

Figure 2-1. 1021/1041 Module Outline Drawing

## 2.5.2 Controller Configuration

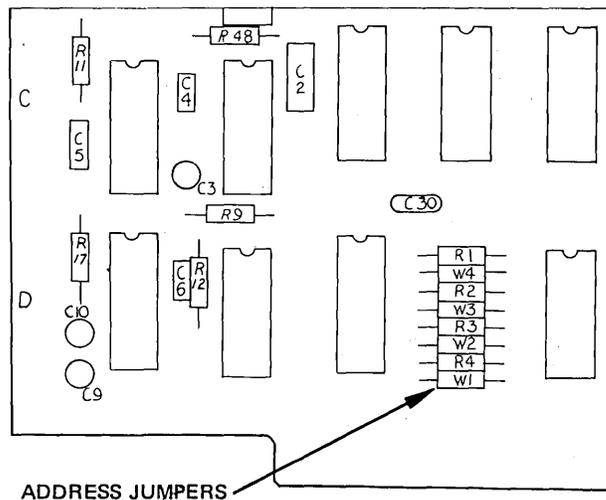
The Micropolis disk controller is normally configured to operate at a base address of F400H with a 2 MHz processor. Ensure that there is no other memory in the system that conflicts with the 1K space beginning at F400H.

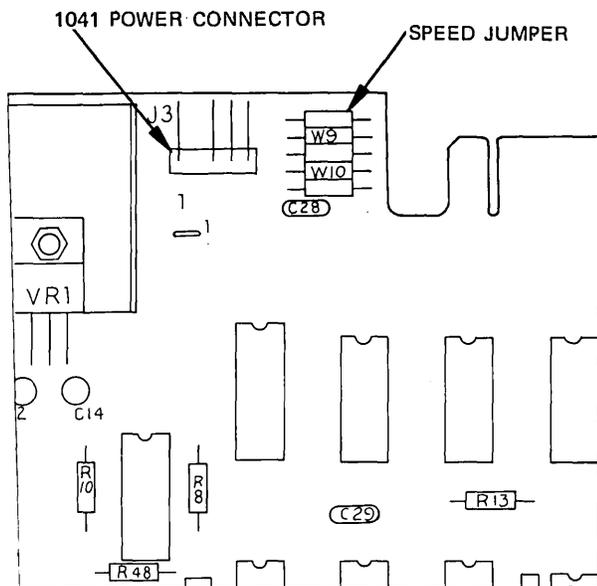
## 2.5.3 Changing the Controller Base Address

If the controller base address requires changing, the controller may be jumpered for a base address at any 1K boundary from C000H to FC00H by performing the following procedure.

- Referring to Figure 2-2, locate the address jumpers W1 through W4. (The controller is shipped with W3 only installed.)
- Referring to Table 2-1, determine the jumpers required for the desired base address. Install the required jumpers using a short length of insulated wire.

- Solder in the new jumper(s) using a 25-30 watt soldering iron and resin-core solder.





**Figure 2-3. Controller Processor Speed Jumper and 1041 Power Connector Location**

W9. Install jumper W9 using a small length of insulated wire and solder in place using a 25-30 watt soldering iron and rosin core solder.

A significant throughput advantage may be realized by operating the disk subsystem with a 3 MHz 8085 or 4 MHz Z80 processor. However, two important notes apply to this type of operation.

- a. System integrity is critical at higher clock rates, particularly 4 MHz. Bus noise in an S-100 bus system which is not specifically designed for 4 MHz operation may reach unacceptable levels when a 4 MHz ZPU is used. To obtain best performance, it is suggested that the user place the Micropolis disk controller as close as possible to the CPU board, preferably the next slot.
- b. Memory speed is extremely critical. Some "250 nsec" memories may not operate at 4 MHz because of logic delays which degrade the theoretical access time such that the access requirements of M1 cycles are not met. These marginal memory boards may be used if your processor is capable of inserting a wait state in an M1 cycle.

#### 2.5.4 Installing the Controller and Interface Cable

Refer to the 1040/1050 Series Floppy Disk Sub-

systems User's Manual, Installation Section for information on installing the controller and connecting the disk drive(s) to it.

## 2.6 MULTI-MODULE DISK SUBSYSTEMS

A Micropolis 1040/1050 series flexible disk subsystem may be expanded to a multi-module system including up to four disk drive units. The following paragraphs provide the technical information necessary to configure a multi-module system.

### 2.6.1 Daisy Chaining Modules

A multi-module system consists of two or more modules connected to the controller with a "Daisy-Chain" interface cable. Typical multiple module systems are illustrated in Figure 2-4.

The module interface consists of a set of common input/output lines and 4 disk select lines. These lines are applied to all modules cabled together. Address comparison logic in each module determines which disk select line will enable the module to respond to the I/O lines. A single module may be jumpered to respond to one of the addresses 0, 1, 2 or 3. A dual module may be jumpered to respond to a pair of addresses, either 0 and 1 or 2 and 3. In a multi-module system, no two modules may be jumpered to respond to the same select line. This requirement for unique addressing restricts the possible configurations to systems consisting of:

- a. Two dual modules
- b. A dual module and one or two single modules
- c. Up to four single modules

In a Daisy-Chained system a distinction is made between a Master module and Add-on modules. The module shipped with a 1040/1050 series subsystem is a master module. A master module contains a resistor network for terminating the interface lines and is jumpered to respond to drive address 0 (0 and 1 in dual module). A module purchased separately as an add-on module does not contain terminators. A single add-on will be jumpered to respond to address 1. A dual add-on will be jumpered to respond to addresses 2 and 3.

The following Daisy-Chain interface cables are available from Micropolis:

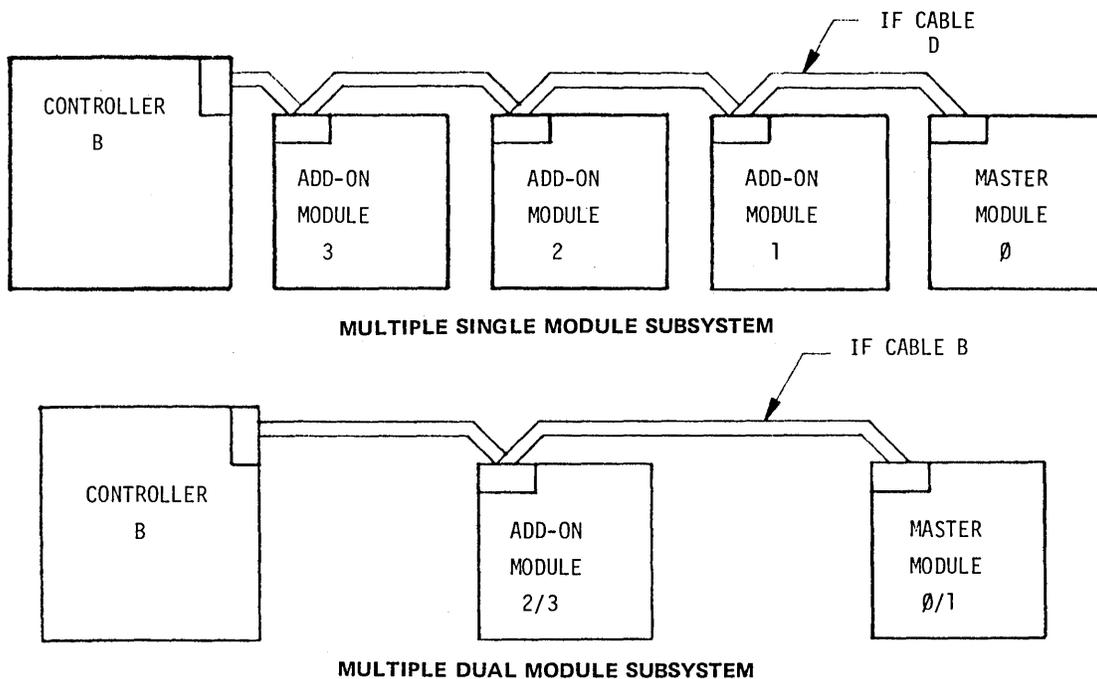


Figure 2-4. Daisy Chain Configuration

Model #	Description
1083-02	Interface Cable B — Used with two modules
1083-03	Interface Cable C — Used with three modules
1083-04	Interface Cable D — Used with four modules

### 2.7.1 Converting a Single Module

The special equipment required to perform the conversion consists of:

- Small flat blade screwdriver
- 1/4" hexdriver
- Phillips type screwdriver

## 2.7 MULTI-MODULE SYSTEM INSTALLATION (READDRESSING MODULE)

A multi-module system requires a master module, a Daisy Chain interface cable, and one or more add-on modules. Add-on modules jumpered for the standard add-on addresses may be purchased from Micropolis or a master module can be converted to an add-on by the procedures given below. These paragraphs also include procedures for re-jumpering the drive selection logic if required to provide unique addressing for all modules in a system.

Remove the cable A supplied with each module. (Remove cover from single modules other than 1041/1021 series.) Connect modules to controller with a Daisy-Chain interface cable as illustrated in Figure 2-4. The master module must be connected to the last connector on the cable, i.e., the furthest from the controller end of the cable, to provide proper termination of the interface.

This paragraph contains the procedure for converting a single master module to an add-on module and for jumpering the drive selections logic.

- a. Remove the screws securing the module cover. Carefully remove the cover by lifting the rear of cover slightly and sliding cover to rear of module. Figure 2-5 illustrates the mounting of the drive electronics PCBA in the single module and the interconnecting cables.
- b. Converting a master module to an add-on involves removing the terminator pack and re-

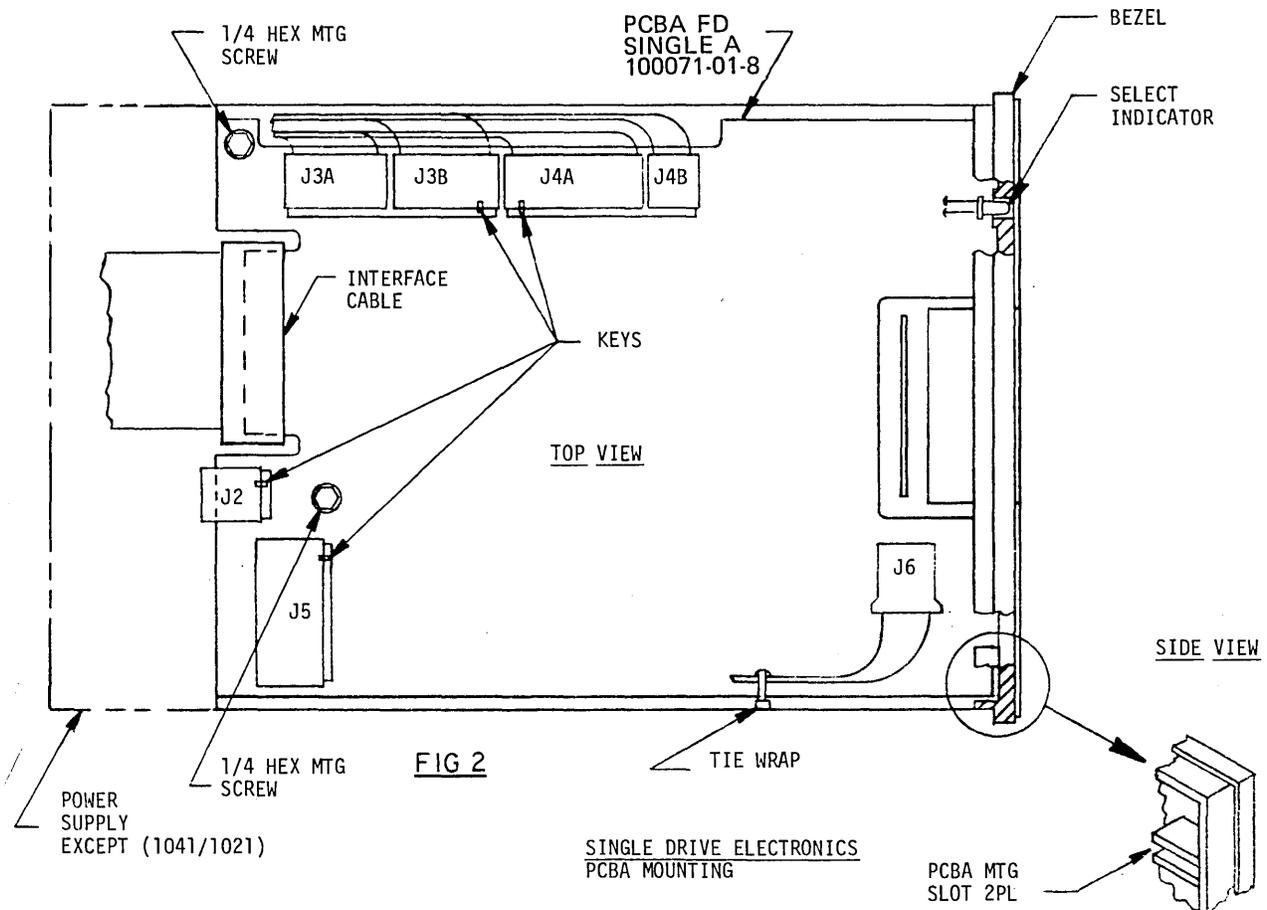


Figure 2-5. PCBA Mounting on Single Drive Electronics

jumpering for an address other than zero. Remove the terminator pack as follows:

1. Locate the terminator resistor pack, U15 (Ref. Figure 2-6.) (U17 in Single B)
2. With a small flat blade screwdriver, carefully pry the pack from its socket.

c. Change module address as follows:

1. Locate address jumpers W1 through W4 (Ref. Figure 2-6). A master module is supplied with W1 installed. An add-on module purchased from Micropolis is supplied with W2 installed. *Only one* of the jumpers W1-W4 may be installed in a PCBA.
2. Remove the jumper platform installed in the socket. Reinstall the jumper platform after jumpering, as follows to obtain the desired drive address:

Drive Address	W1	W2	W3	W4
0	X	Open	Open	Open
1	Open	X	Open	Open
2	Open	Open	X	Open
3	Open	Open	Open	X

- d. Reinstall the module cover carefully, ensuring none of the cables are trapped between the cover and the module chassis and that an insulated adhesive strip is preventing the select jumpers from shorting to the case. Install the cover screws.

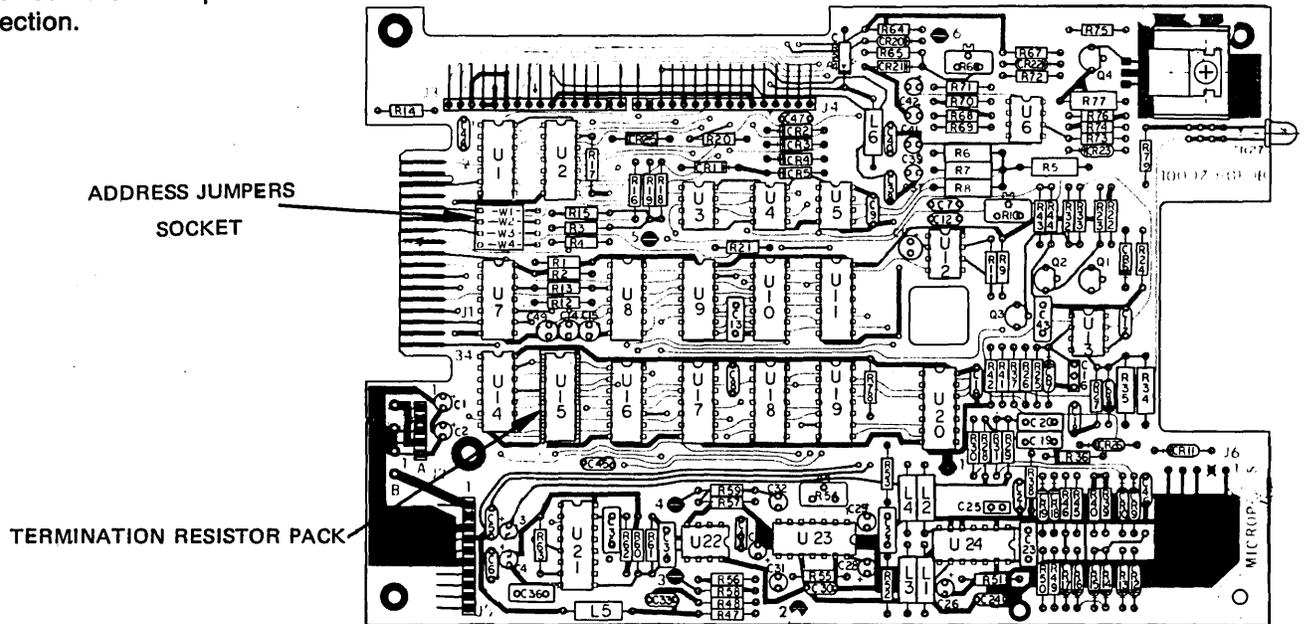
### 2.7.2 Converting a Dual Module

Converting a dual master module to an add-on module requires both changing the address selection jumpers and numerous resistors associated with the unit number LED displays.

This procedure is only recommended when it is impractical to purchase an add-on module (Model number 1033).

**NOTE**

On earlier drives a "zero ohm" jumper was soldered in place for address selection.



NOTE: FD Single B has similar layout.

**Figure 2-6. FD Single A Components Location**

Low-wattage soldering iron and rosin core solder

Pliers

¼" hexdriver

Phillips type screwdriver

¼ watt 270Ω resistors (as required)

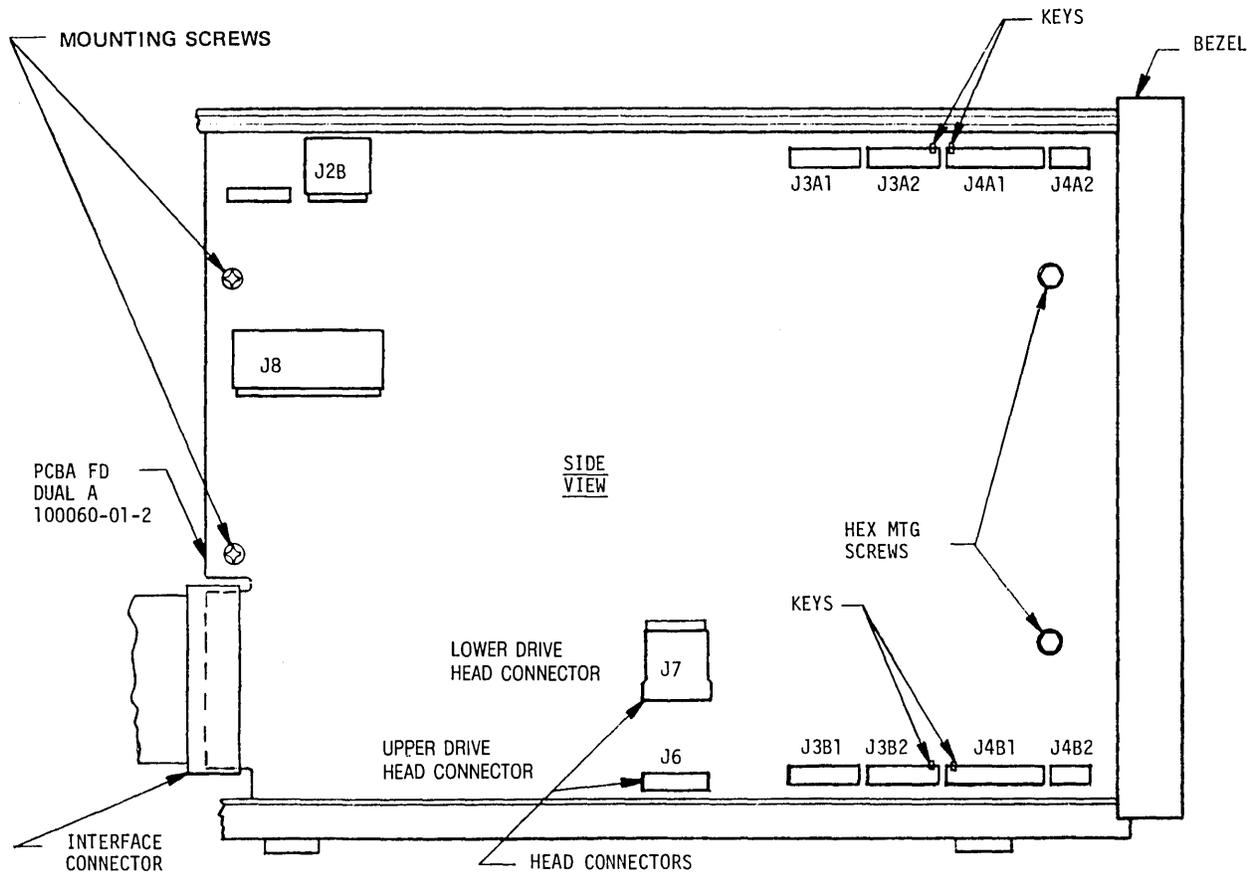
- a. Remove the 6 screws securing the module cover. Slide the cover to the rear of the module to remove. Figure 2-7 illustrates the mounting of the drive electronics PCBA in the dual module and the interconnecting cables.
- b. Modify the PCBA by removing it from the module as follows:
  1. Place a small strip of masking tape on each cable connector and mark with the cable designations shown in Figure 2-7. This will facilitate reassembly after the PCBA is modified.

2. Grasp the head connectors (J6 and J7) and remove.

**CAUTION**

DO NOT ATTEMPT TO REMOVE THE HEAD CONNECTORS BY PULLING ON THE HEAD CABLES — THE WIRES ARE VERY FRAGILE.

3. Disconnect all the interconnecting cables and the interface connector from the PCBA.
4. Remove the four PBA mounting screws. Maneuver the PCBA to the rear and side of the module and lift it out through the side.
- c. Place the PCBA on a clean, flat work surface. Refer to Figures 2-8 and 2-9 for location of components on the PCBA.



**Figure 2-7. Dual Electronics PCBA Mounting**

- d. Conversion of a master module to an add-on module consists of removing the terminating resistors, rejumping the drive select for address 2 and 3, and changing the drive address indicators to display addresses 2 and 3.
- e. Remove the terminating resistors as follows:
  1. Locate the terminating resistors R1-R6.
  2. Carefully unsolder resistors R1-R6 and remove.
- f. Rejump the drive select as follows:
  1. Locate address jumpers W1-W4. A master module has W1 and W2 installed.
  2. Carefully unsolder and remove W1 and W2. Reinstall jumpers (or short lengths of insulated wire) in W3 and W4 and solder in place.
- g. Readdress the displays as follows:
  1. Locate the resistors R69 thru R78 and R108 thru R117 in Figure 2-9.
  2. Remove/install 270  $\Omega$  resistors per Table 2-2 for add-on configuration.
- h. Clean the flux from the board with alcohol.
- i. Carefully maneuver the PCBA into the side of the module. Ensure there are no cables trapped behind the board. Install the four

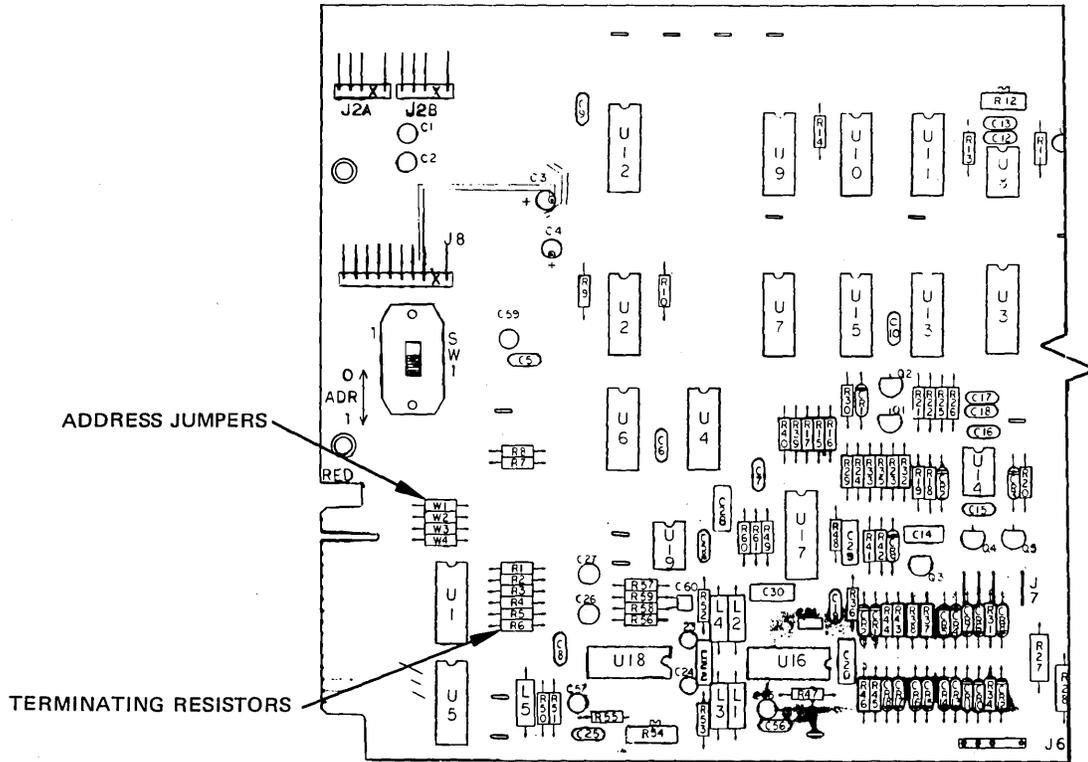


Figure 2-8. Address Jumpers and Terminating Resistors on FD Dual A

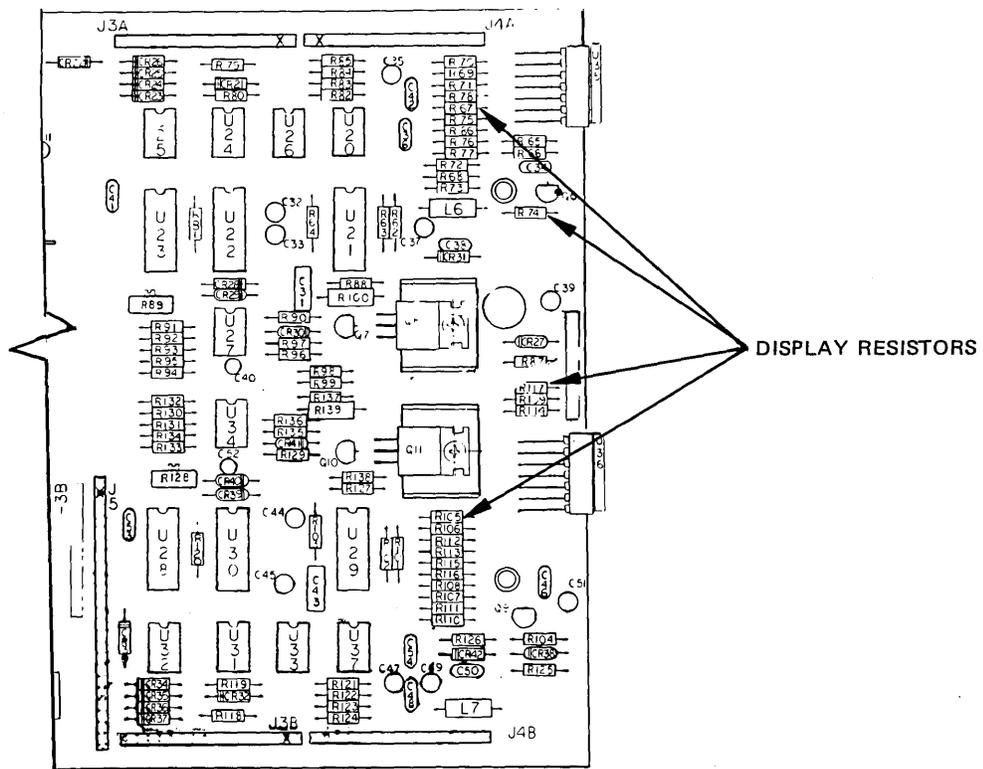


Figure 2-9. FD Dual A Display Resistors

**TABLE 2-2. DISPLAY CONTROL RESISTORS —  
FD DUAL A**

RESISTOR	[ADDR 0/1] MASTER	[ADDR 2/3] ADD-ON
R 69	270 Ω	Open
R 70	Open	270 Ω
R 71	270	270
R 72	270	Open
R 73	270	Open
R 74	Open	270
R 75	270	270
R 76	270	Open
R 77	Open	270
R 78	Open	270
R108	270	Open
R109	Open	270
R110	270	270
R111	270	Open
R112	270	Open
R113	Open	270
R114	270	270
R115	270	Open
R116	Open	270
R117	Open	270

Note: All resistors 270 ohm.(Ω)

PCBA mounting screws per Figure 2-7.

- j. Reinstall all connectors.
- k. Reinstall the module cover by carefully sliding it forward from the rear of the module. Ensure no cables are trapped between the cover and the module chassis. Secure the cover with the six screws.

**2.8 APPLYING DC POWER (MODEL 1041/1021 ONLY)**

Model 1041/1021 modules do not include power supplies thereby requiring the user to supply DC power. The user may provide regulated power directly or may provide unregulated voltages to modules equipped with the optional regulator kit, Model 1091-01.

**2.8.1 Regulated DC**

Regulated DC voltages are applied to J5 of the drive electronics board (refer to Figure 2-10 for location of J5) as follows:

J5 Pin	Voltage	Current Requirements	Wire Color*
7	+5V DC ±5%	0.5 AMP	Violet
6	+5V Return		Blue
4	+12V DC ±5%	1.15 AMP	Yellow
3	+12V Return		Orange
*Wire color refers to power cable supplied with 1041/1021 drive.			

+5 Return and +12 Return must be connected together at the power supply. The drive chassis must be connected to the computer chassis or directly to earth ground.

**2.8.2 Unregulated DC**

Unregulated DC power may be applied to modules equipped with the optional regulator kit Model 1091-01. Each regulator kit provides regulated DC power for one 1041 or 1021 module. Install the kit as follows:

Install the heatsink assembly on the rear of the protective sleeve using the hardware provided. Plug the connector from the heatsink onto J5 of the drive electronics board (see Figure 2-10 for location of J5).

Unregulated DC power is applied to J2 of the drive electronics board (see Figure 2-10 for location of J2) as follows:

J2 Pin	Voltage	Current Requirements	Wire Color*
1	+16V Unregulated (+15 to +17)	1.15 AMP	Brown
2	Key		
3	+16V Return		Orange
4	+8V Unregulated (+8 to +10)	0.5 AMP	Yellow
5	+8 Return		Green
*Wire color refers to the 4 wire power cable supplied with the regulator kit.			

Unregulated DC may be obtained from an S-100 bus computer by connecting the 4 wire power cable supplied with the regulator kit between J2 of the drive electronics board and J3 on the Controller

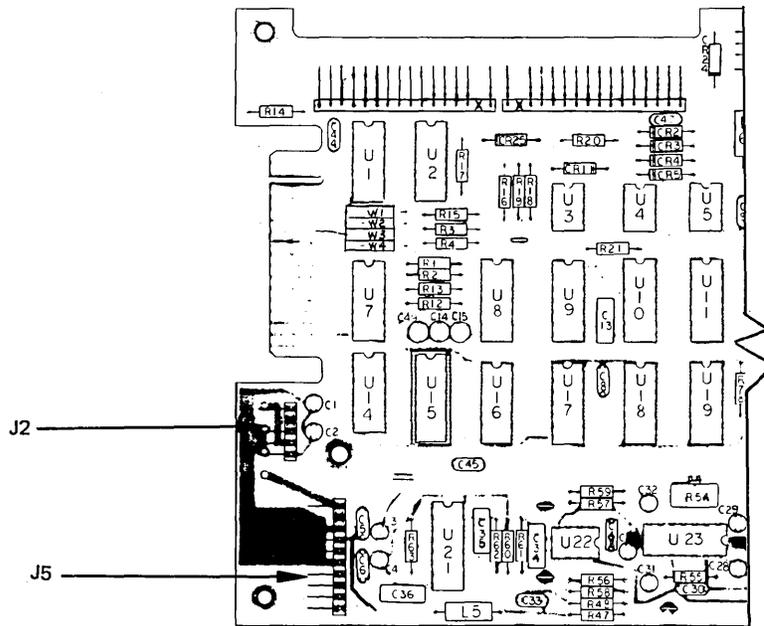


Figure 2-10. Model 1041/1021 Power Connectors

board. A maximum of one drive may be powered by the controller in this manner. It is suggested that multi-drive systems be powered directly by a separate power supply. Dual power supplies providing +5 and +12 regulated are commercially available from several manufacturers.

## 2.9 LINE VOLTAGE CONVERSION PROCEDURE

The 1020, 30, 40, and 50 series Floppy Disk subsystems are capable of operating at nominal line voltage of 100, 117, 200, 210 and 240 volts, 50 or 60 Hz. Conversion from one voltage to another is accomplished by rewiring of the power transformers primary to line connections. Connections to the transformer are by "Faston" terminals. The following procedure details changing of the subsystems operating line voltage.

### NOTE

There are no changes required to convert between 50 and 60 Hz operation.

### 2.9.1 Conversion Kit

A line voltage conversion kit P/N 100113-01 is available from Micropolis at a nominal charge which

contains jumpers, fuses and the tie wraps to convert one subsystem between the lower line voltage group (100V/117V) and the higher line voltage group (200/220/240V). Unless you have access to "Faston" terminals and the appropriate crimping tool this kit is recommended. Conversion within the two groups is accomplished by using existing jumpers.

### 2.9.2 Special Tools and Parts

#### NOTE

These parts are not required if the line voltage conversion kit is purchased.

Use the following tools and parts for conversion from 100/117 to 200/220/240 volts:

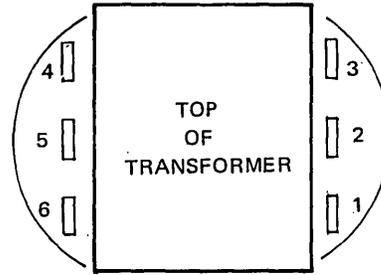
- 6 ea. 1/4 inch "Faston" insulated terminals
- 36 inches 20 AGW or larger hookup wire
- 3 small tie wraps
- "Faston" crimping tool
- wire strippers

**2.9.3 Procedure**

Lugs layout pattern is illustrated below:

**CAUTION**

HIGH VOLTAGE — ENSURE THAT THE LINE CORD IS DISCONNECTED FROM THE LINE BEFORE TOUCHING ANY PART OF THE POWER SUPPLY CIRCUITRY.



- a. With the subsystem placed right side up, locate the wires connecting the transformers primary to the fuse holder and the power switch. The transformer's primary connections consist of 6 lugs on the top of the transformer.

- b. Subsystems are normally shipped with the transformer primary connected for 117V operation. For operation at other voltages, refer to the chart below.

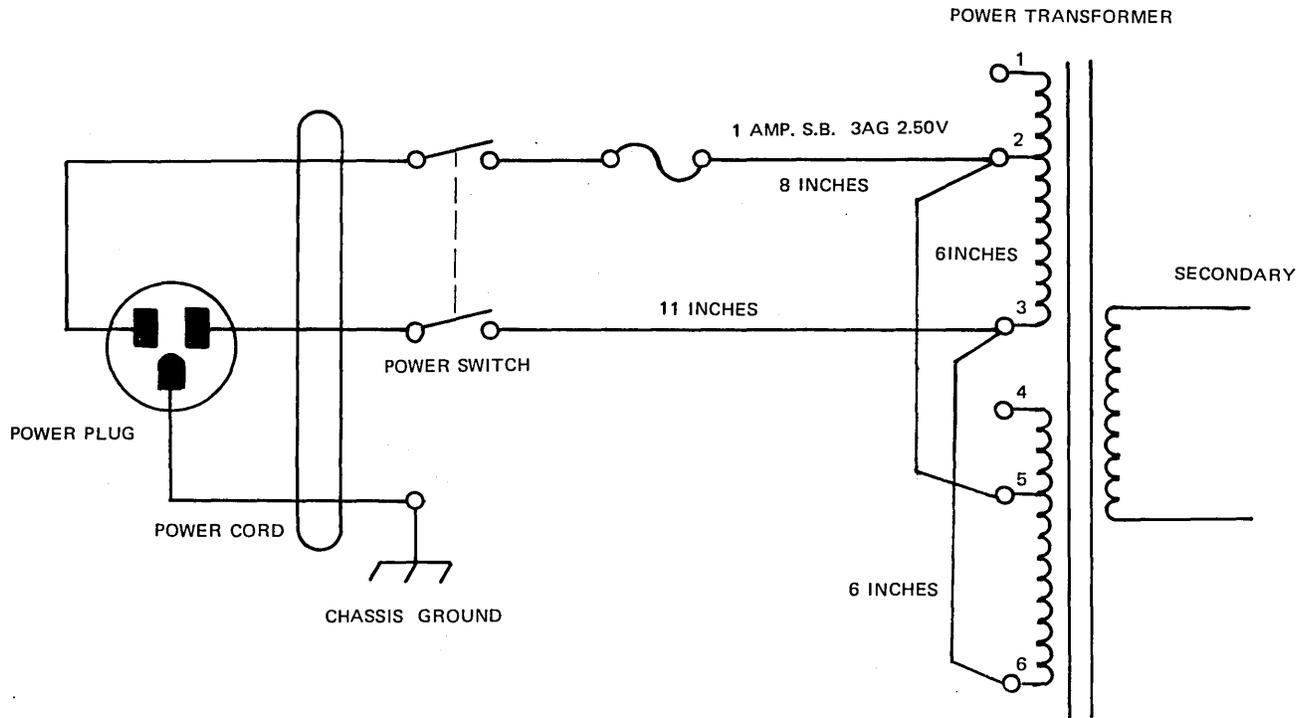
AC Volts	Freq.	Primary Connections			Fuse
		Line	Neut	Link	
100V AC	50/60 Hz	2	3	2 to 5, 3 to 6	1.0A SB
117V AC	50/60 Hz	1	3	1 to 4, 3 to 6	1.0A SB
200V AC	50/60 Hz	2	6	3 to 5	0.5A SB
220V AC	50/60 Hz	1	6	3 to 5	0.5A SB
240V AC	50/60 Hz	1	6	3 to 4	0.5A SB

- c. To change from one voltage to another, determine the jumper requirements from Figure 2-12 through Figure 2-15 and construct a new jumper set (preassembled jumpers contained in kit).
- d. Cut tie wraps securing wires between fuse holder, power switch and transformer. Remove all wires connected to transformers lugs.
- e. Connect leads as shown in appropriate figure. Ensure that unused lugs are insulated using spare terminals.

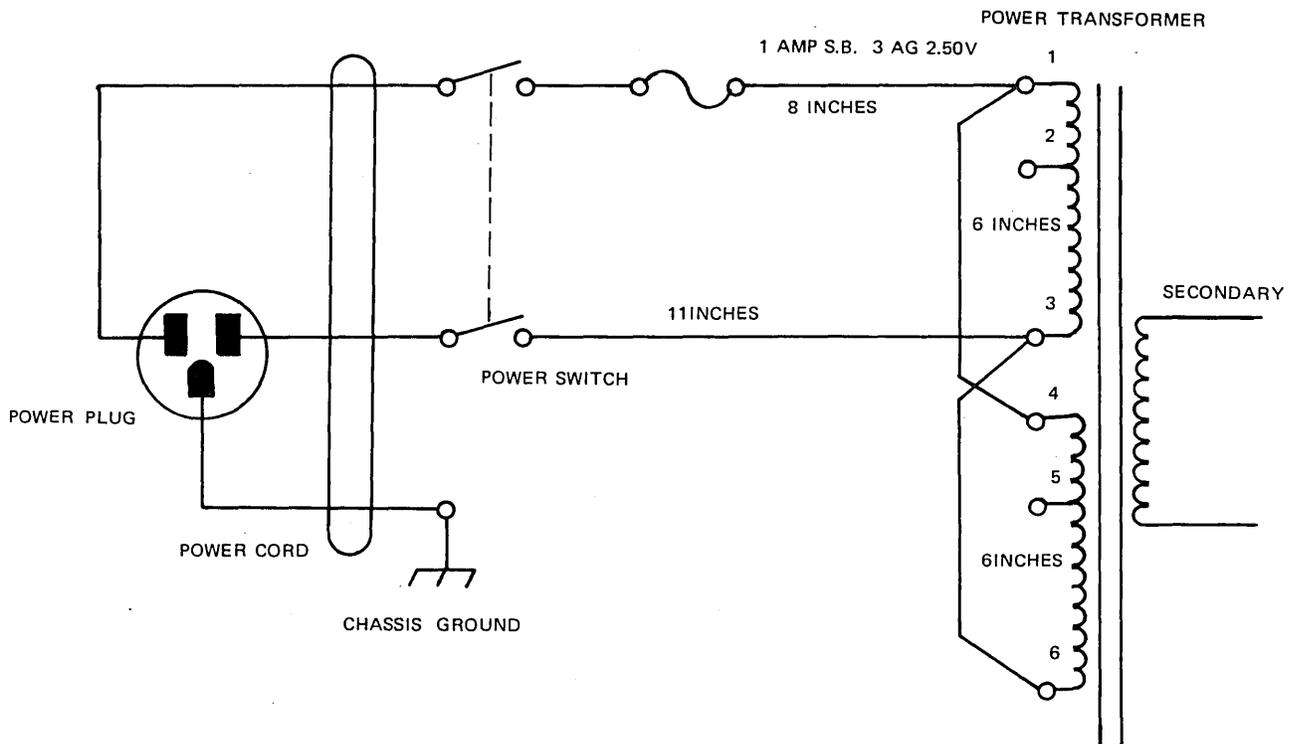
- f. Install new tie wraps as required.
- g. Replace line fuse with one of correct sizes as shown in appropriate figure.
- h. Check for normal operation of the subsystem. If fuse should fail after conversion, recheck wiring before reapplying power.

**2.9.4 Documentation/ID Label Change**

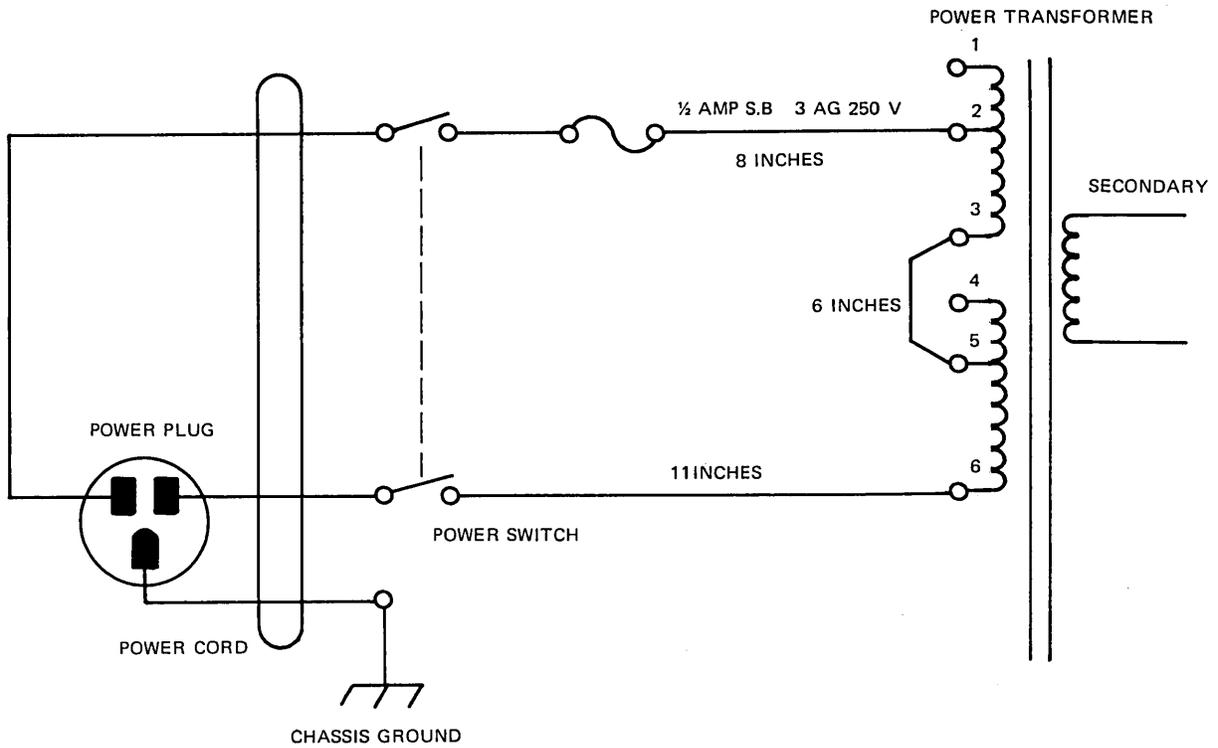
Indicate on the ID label, using suitable ink or a metal scribe, the correct line voltage and fuse size.



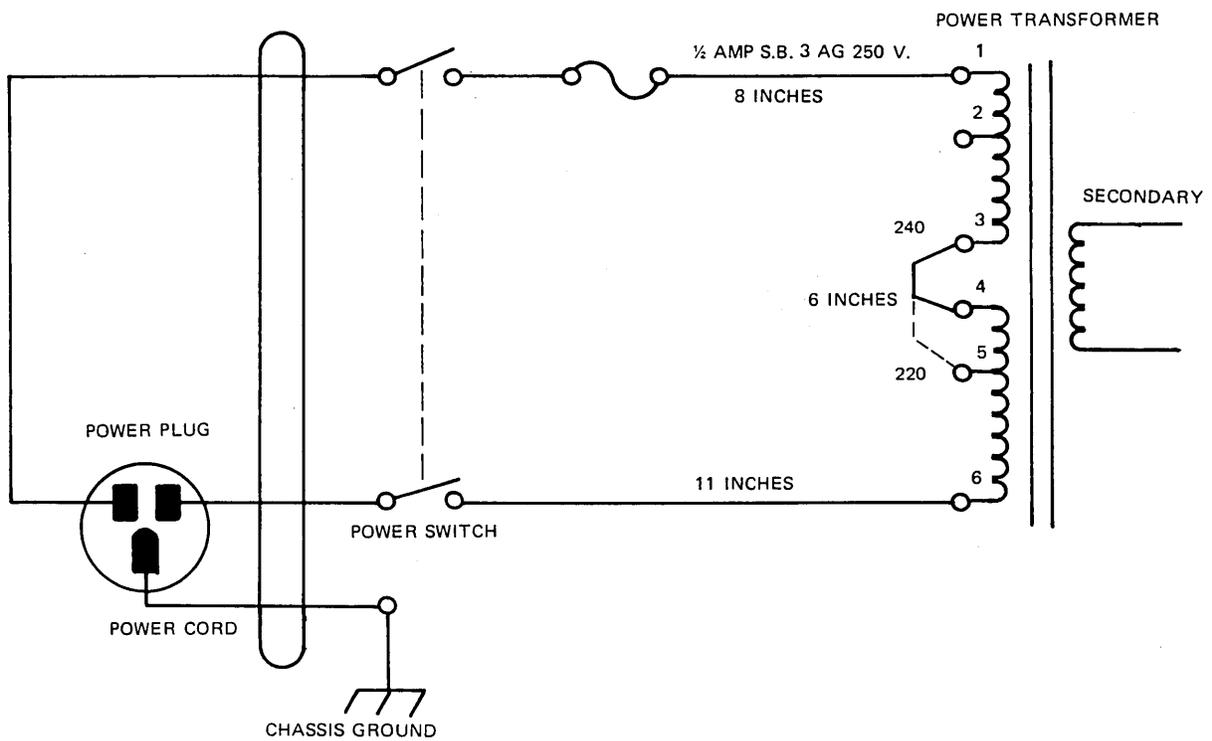
**Figure 2-11. Jumpers Required for 100V 50/60 Hz Power Source**



**Figure 2-12. Jumpers Required for 117V 50/60 Hz Power Source**



**Figure 2-13. Jumpers Required for 200V 50/60 Hz Power Source**



**Figure 2-14. Jumpers Required for 220/240V 50/60 Hz Power Source**

### THEORY OF OPERATION

#### 3.1 INTRODUCTION

This section identifies the components that comprise the different subsystems.

The theory of operation of each of the components is then described in detail.

#### 3.2 ORGANIZATION OF THE SUBSYSTEM

##### 3.2.1 Subsystem Description

Each subsystem comprises:

- a. A master storage module.
- b. A single printed circuit board controller designed to be physically and electrically compatible with an S-100 bus, 8080/Z80 based microcomputer, inserted in the host computer.
- c. An optional add-on storage module identical to the master storage module except for the unit address and the deletion of interface cable terminators. Add-on modules can be daisy-chained to the master modules using a daisy chain cable (see Section 2).
- d. A software package together with the appropriate user documentation. Description of the software is not within the scope of the Maintenance Manual and is fully documented in the User's Manual Part No. 100089-01.

##### 3.2.2 Module Description

###### *Dual Module with Power Supply (1053/1033)*

This equipment includes:

- a. Two disk drive mechanisms (48TPI or 100TPI, see Para. 3.6).
- b. A dual-drive board assembly, designated as Dual A PCBA.
- c. An enclosure, designated Enclosure B, that

houses a power supply, the two drives, and the Dual A PCBA.

###### *Single Module with Power Supply (1043/1023, 1042/1022)*

This equipment includes:

- a. One disk drive mechanism (48TPI or 100TPI, see Para. 3.6).
- b. A single-drive board assembly, designated Single A PCBA, or Single B PCBA.
- c. An enclosure, designated as Enclosure A, that houses a power supply, the drive, and the PCBA.

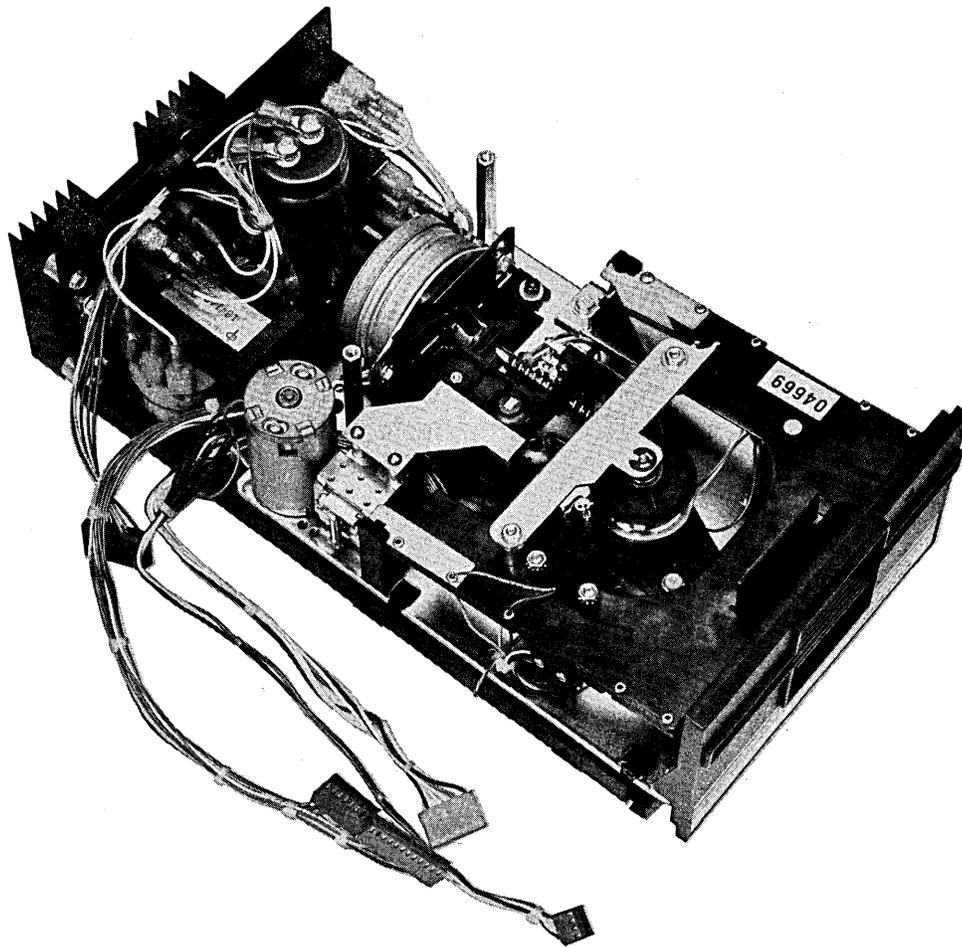
###### *Single Module Without Power Supply (1041, 1021)*

This equipment includes:

- a. One disk drive mechanism (48TPI or 100TPI, see Para. 3.2.2).
- b. A Single A PCBA, or Single B PCBA.
- c. A sleeve enclosure, which houses the drive and PCBA.
- d. An optional regulator kit (Model 1091-01) is available which mounts in the rear of the enclosure and which provides regulated power supplies from an external unregulated power.

#### 3.3 ENCLOSURE A POWER SUPPLY

Figure 3-1 shows the layout of the power supply components. Refer to Section 9, Schematic Diagram 100154. The power supply is a conventional full wave bridge rectifier power supply. Capacitor input filter C2 is supplied by a transformer T1 and bridge rectifier BR1. C1 acts to suppress transients due to rectifier switching. Different nominal line voltages are accommodated by changing the transformer connections according to Paragraph 2-9. Paragraph 2.9 also shows the appropriate fuse required. Unregulated DC power is supplied to Pin 1 of P2A and via a 7.5-ohm power resistor R1 to Pin 4 of P2A.



**Figure 3-1. Enclosure A, Power Supply Components**

A regulator package consisting of VR1 (7812) and VR2 (7805) is mounted to a heat sink on the rear of the enclosure. These regulators are connected to P5, P2A and P5 plug into the PCBA which provides the appropriate interconnections to yield the required regulated supplies. The 7.5-ohm resistor R1 reduces the power dissipated by the 5V regulator.

### **3.4 ENCLOSURE B POWER SUPPLY**

Figure 3-2 shows the layout of the power supply components. Refer to Section 9, Schematic Diagram 100155. Circuit description is identical with that of Enclosure A (Para. 3.3) with the exception that an extra 7812 regulator (UR3) is provided to generate the 12V supply for the second drive in the dual unit and R1 is 7.5  $\Omega$  because of increased current drawn from the +5V supply. The interconnection between P2A and P8 is provided on the Dual A PCBA.

### **3.5 REGULATOR 1091-01**

The schematic and operation of the optional regulator is identical with the regulators used in Enclosure A.

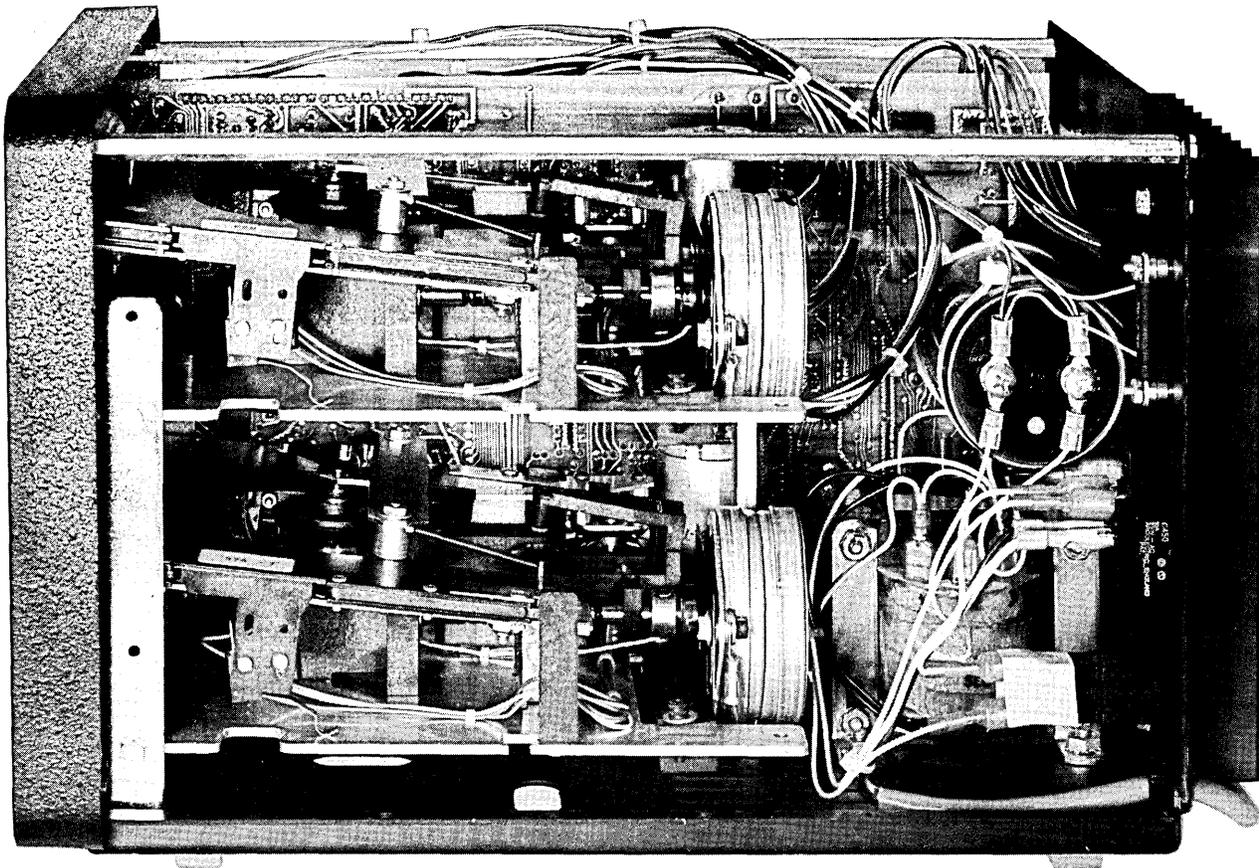
### **3.6 DRIVE MECHANISM FUNCTIONAL DESCRIPTION**

All drive mechanisms use the same mechanical elements except:

- a. The lead screw has a pitch of 8.33 threads per inch for the 100TPI drive (MOD II) versus 4 threads/inch for the 48TPI (MOD I) drives.
- b. A different magnetic head is used for 100TPI (MOD II) drives having narrower read/write (R/W) and erase widths than the 48TPI (MOD I) drives.

The drive mechanism shown in Figure 3-3 consists of:

- A spindle drive system.
- Positioner control mechanism.
- Read/write and tunnel erase head assembly.
- Head load mechanism.
- Interlocks.
- Index transducer.
- Receiver and clamp assembly.



**Figure 3-2. Enclosure B, Power Supply Components**

### **3.6.1 Spindle Drive System**

The spindle is driven from an integral DC motor/AC tachometer which provides a closed-loop velocity servo via a belt which yields an 8:1 speed reduction from motor to spindle. When the drive door is closed, a spring-loaded clamp attached to the receiver assembly lowers and forces the diskette over a precision cone on the spindle assembly. The cone profile is such as to provide an interference fit allowing the diskette to be centered on the spindle. Centering is promoted by the rotation of the spindle during the diskette clamping process. The door switch is adjusted so that the spindle begins to rotate before the diskette is clamped to the spindle.

### **3.6.2 Positioner Control Mechanism**

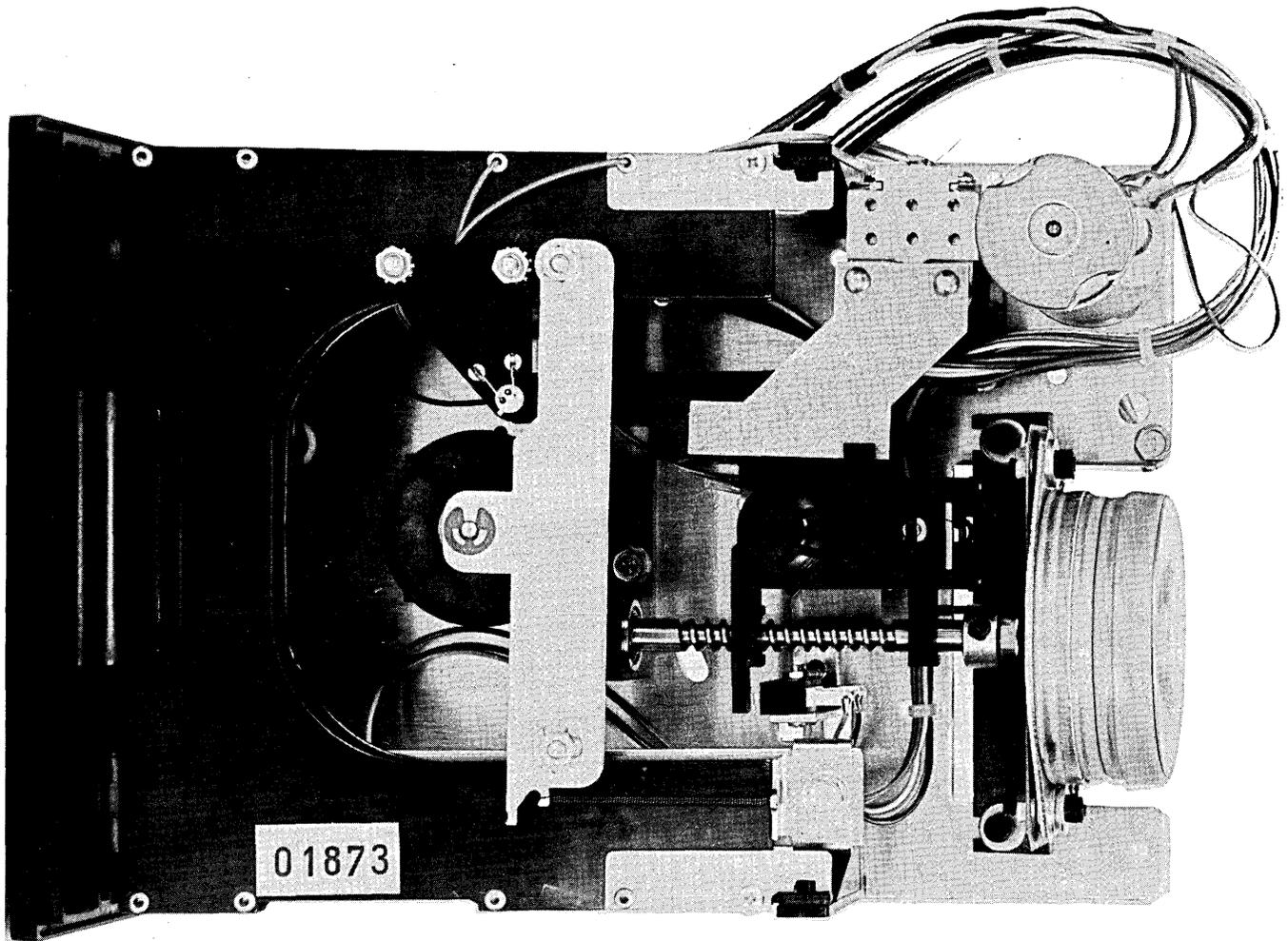
The head carriage assembly is positioned by a four-phase permanent magnet stepper motor via a ground stainless steel lead screw and single point steel follower. The positioner control and lead screw are preloaded against a bearing in the spindle housing by a flexure spring. This referencing technique substantially removes the base plate from the ther-

mal expansion and mechanical stability loops.

The lead screw pitch is chosen so that 4 "ministeps" are taken to move one track. This reduces by 4 to 1 the effects of stepper motor accuracy and hysteresis effects caused by friction. Sequencing of the phases is organized by the control electronics (see Para. 3.8.5). A track zero switch is mounted to the deck such that an extension of the head carriage activates the switch between tracks 0 and 1. A mechanical stop is provided which prevents the carriage from moving behind the track zero position.

### **3.6.3 Head Carriage Assembly**

The head consists of a ferrite R/W element and two tunnel erase elements mounted in a barium titanate slider. The head is mounted in a carriage assembly which is supported by and driven from the lead screw via a steel follower and also referenced to the platen. When the drive is selected, the head load solenoid is energized allowing the load arm and pressure pad to force the diskette into contact with the head with a load of 15 to 18 grams. A foam rubber pad on the solenoid arm ensures the diskette



**Figure 3-3. Typical Drive Mechanism**

jacket is loaded against the platen surface. In this way an accurate relationship is established between the diskette and the head surface yielding a controlled penetration. When the head load solenoid is deenergized, the diskette has little or no contact with the head.

#### **3.6.4 Interlocks**

The interlocks consist of two electrical switch interlocks and a mechanical interlock.

The door open switch is an interlock that deenergizes the drive motor and causes loss of the Ready indicator when the door is open. The switch is adjusted to close as soon as the receiver assembly is lowered so that the motor is rotating before the disk-

ette is actually clamped to the spindle.

The write protect switch senses the presence or absence of a notch in the diskette for write protect. The normal write protect convention requires that the diskette is write-protected if there is a tab on the diskette which keeps the switch contact from entering the notch.

The mechanical interlock is a mechanism associated with the diskette ejector that prevents the door from closing if no diskette has been loaded into the drive receiver assembly. It also ejects the diskette when the door handle is lifted after the door is opened.

### 3.6.5 Index Transducer

Scotchflex P/N 3463-0001 or equivalent

Index (sector) information is sensed by a combination of a LED mounted to the receiver assembly and a photo-cell mounted in the platen. Index to data adjustment is provided by moving the platen assembly.

Table 3-1 lists each interface line and Figure 3-4 provides a summary of the electrical characteristics of the interface. Figure 3-5 illustrates the general timing requirements.

### 3.7 DRIVE ELECTRICAL INTERFACE

Signal connector J1 provides the interface between the disk drive module and the host controller. This is a 34 pin edge connector located on the drive electronics PCB assembly. A total of 4 drives can be daisy chained on this interface.

Termination resistors for the input lines are provided on the drive electronics PCB assembly. They should be installed in the last module only. The interface consists of 10 input lines and 5 output lines. All lines are low true with the following logic levels:

True =Logic Zero = 0 — 0.4V

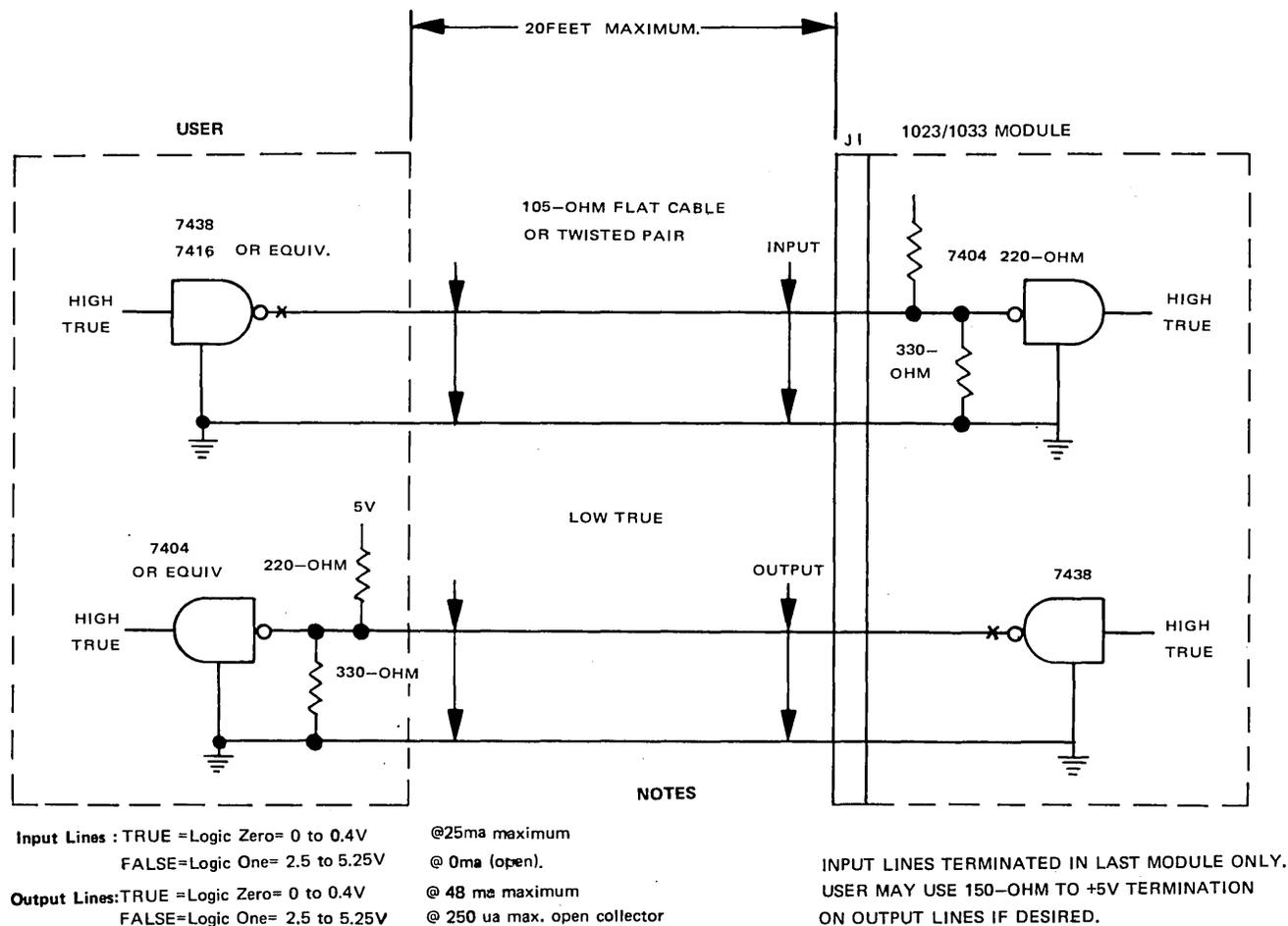
Either flat cable or twisted pair may be used with a maximum cable length of 20 feet. The mating connectors are:

False =Logic One = 2.5 — 5.25V

**TABLE 3-1. SIGNAL INTERFACE - J1**

J1 Connector Pin		Name	Description	Signal Direction
Signal	Gnd			
2	1	HDL	Head Load	IN
4	3	—	Spare	—
6	5	RDY	Ready	OUT
8	7	SECP	Sector/Index Pulse	OUT
10	9	DS1	Drive Select 1	IN
12	11	DS2	Drive Select 2	IN
14	13	DS3	Drive Select 3	IN
16	15	MTRN	Drive Motor On	IN
18	17	DIRN	Step Direction	IN
20	19	STEP	Step Command	IN
22	21	WDA	Write Data	IN
24	23	WRT	Write Gate	IN
26	25	TRK0	Track 0	OUT
28	27	WPT	Write Protect	OUT
30	29	RDA	Read Data	OUT
32	31	HSLT	Head Select	IN
34	33	DS4	Drive Select 4	IN

**NOTE:** J1 Mating Connector: Scotchflex P/N 3463-001 or equivalent.



**Figure 3-4. Signal Interface Characteristics**

**3.8 SINGLE A DRIVE (P/N 100072) PCBA, GENERAL FUNCTIONAL DESCRIPTION**

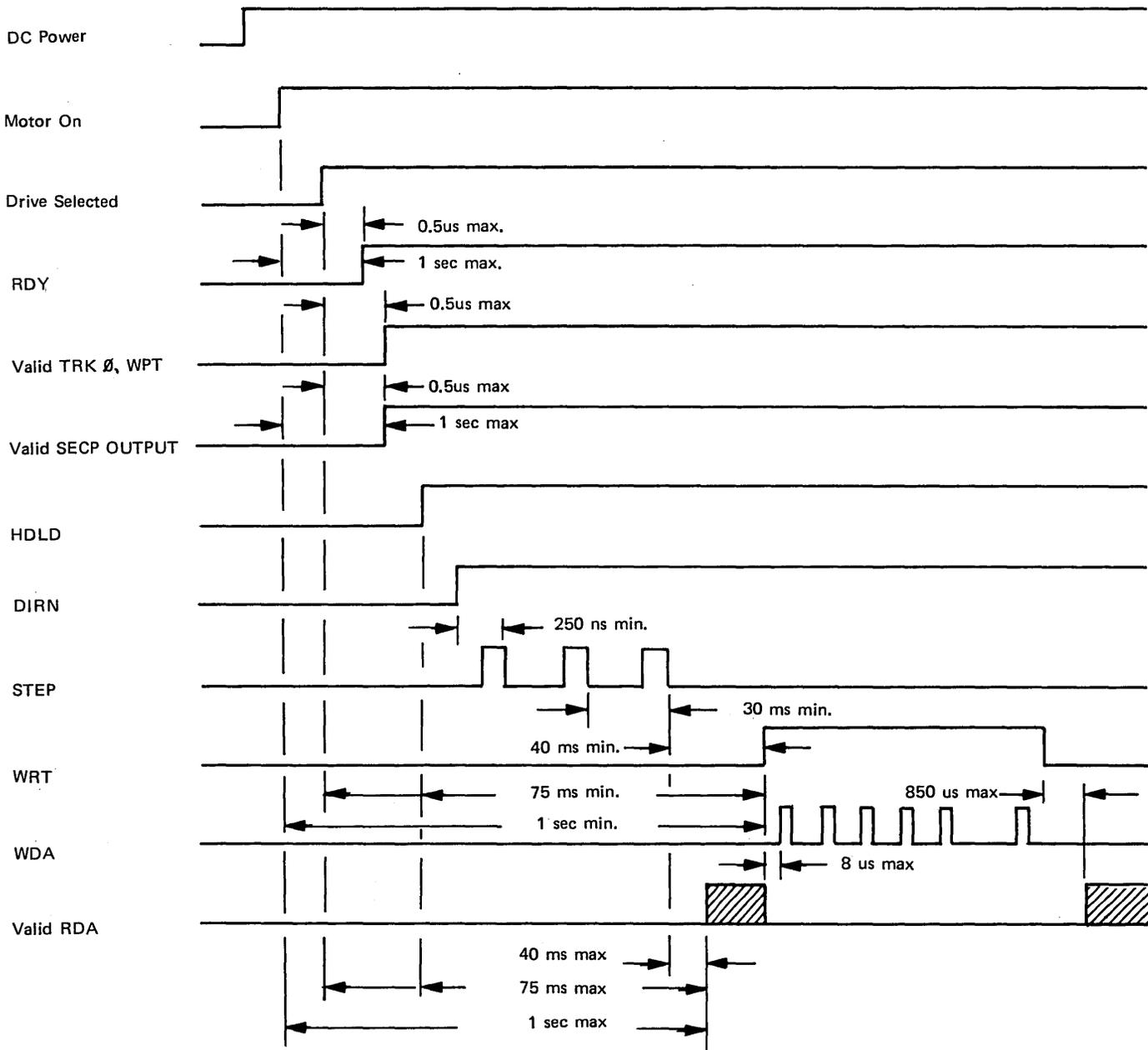
This PCBA provides the circuits necessary to read and write data on the diskette in the drive assembly. The board communicates with the interface through a 34 pin edge connector and with the disk drive through a number of molex connectors. Figure 3-6 illustrates the functional elements contained on the PCBA.

The board functional description consists of a detailed explanation of the following functional elements: interface circuits, motor control circuits, read and write circuits, positioner control circuits, and miscellaneous circuits such as switches, transducers and head load solenoid circuits. Although the circuit descriptions are supported by simplified drawings, the detailed circuit elements are shown in the schematic and logic drawings located in Section 9. These drawings are referenced by sheet and drawing number whenever appropriate.

**3.8.1 Interface Circuits (Ref. Sheet 2 of Dwg 100072)**

The interface circuits consist of receivers, terminators, transmitters, and select logic. The incoming signals are terminated with a 220/330 ohm terminator pack U15. A jumper in one of the positions W1, W2, W3 and W4 causes the drive selection logic to respond to one of the drive select input lines DS1 through DS4. The appropriate select line is terminated by R1 and received by U16-2. The select signal gates the output signals directly via transmitters U1 and indirectly in the case of the read data signal on U16-12 (Sheet 7 of Dwg 100072). It also drives a LED panel indicator through driver U20-4 which shows when the drive has been selected.

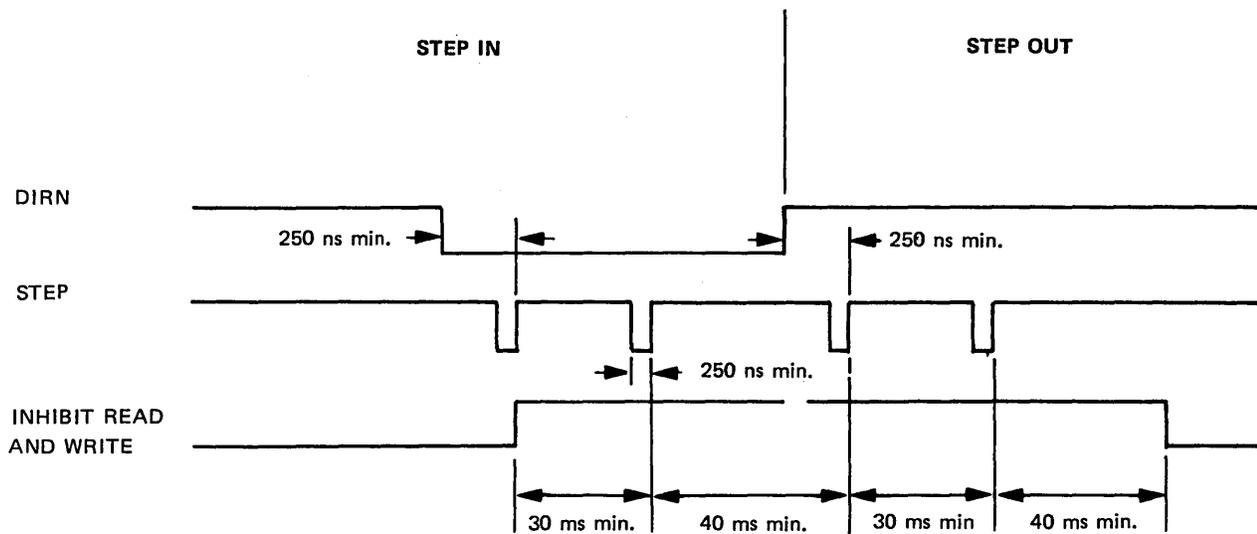
Versions of the board determine terminator and address response configurations. A master unit is configured with terminators and with W1 inserted. Add-on units are configured to be placed at an intermediate point on a daisy chain and have terminators removed and W2 inserted. (W3 and W4 could be inserted.)



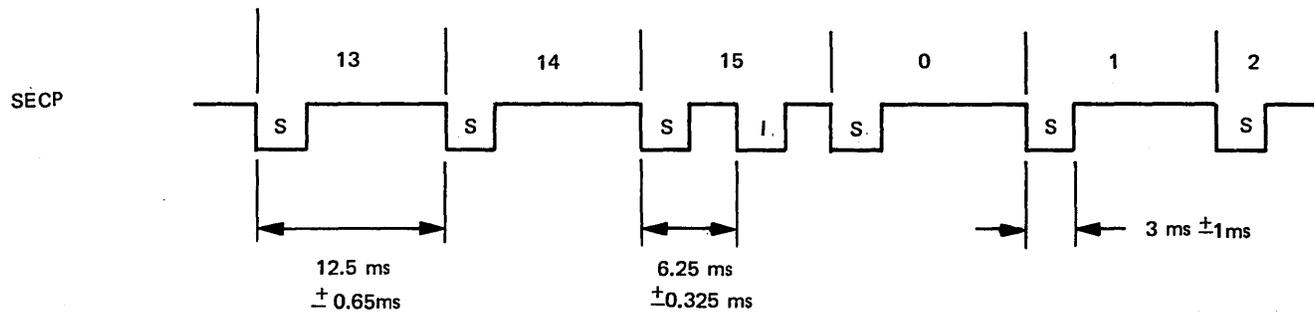
**a. Major Signal Timing**

**NOTE: ALL WAVEFORMS SHOWN ARE HIGH TRUE**

**Figure 3-5. General timing Diagram for a Micropolis Floppy Disk Subsystem**



**b. Positioner Control General Timing**



**c. Sector/Index General Timing**

**Figure 3-5. General Timing Diagram for a Micropolls Floppy Disk Subsystem (Cont'd)**

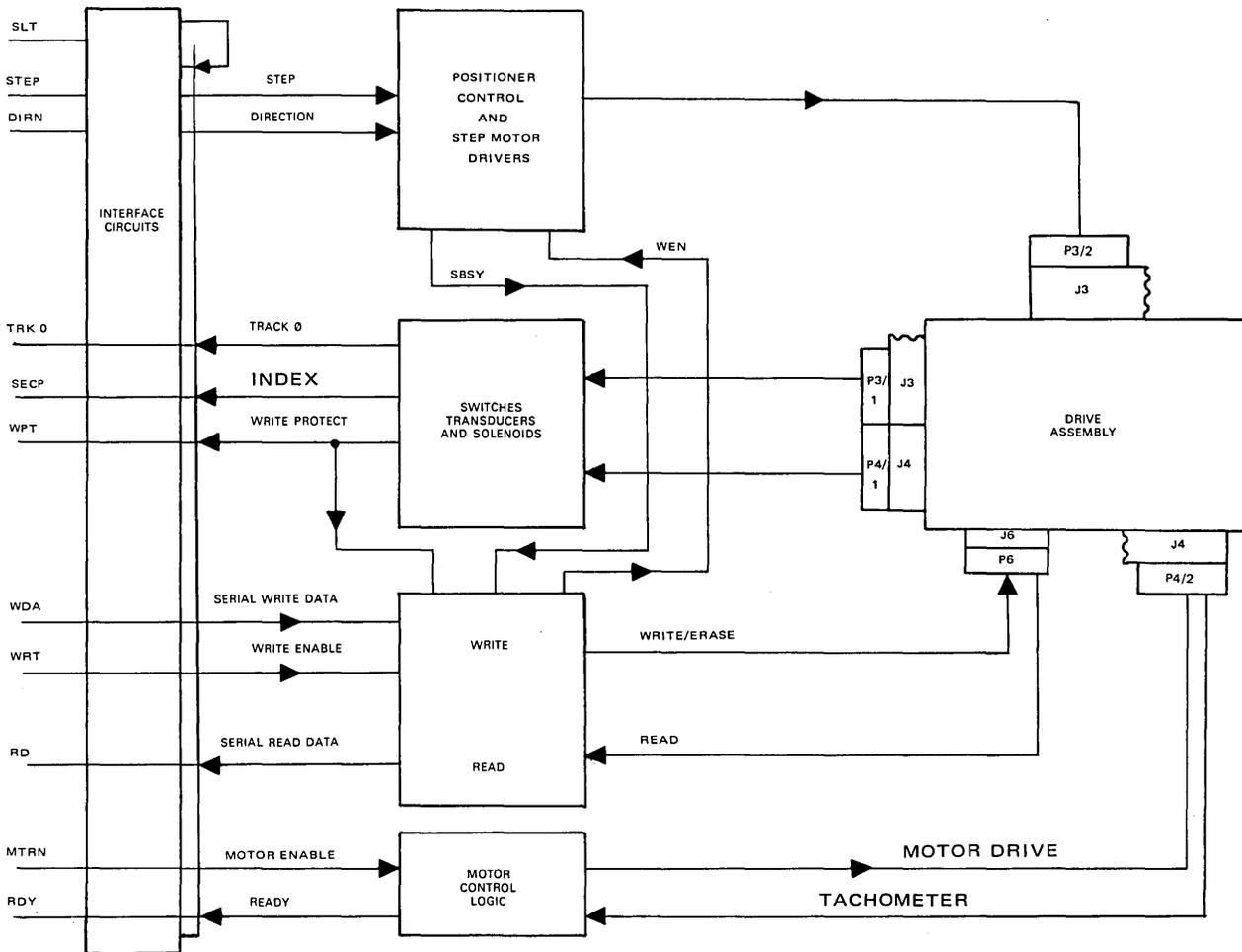


Figure 3-6. Single Drive Block Diagram

### 3.8.2 Motor Control (Ref. Sheet 8 of Dwg 100072)

The motor control circuit is a closed loop servo, controlling the spindle drive system. The spindle drive consists of a DC motor and AC tachometer mounted on a common shaft. The DC motor shaft rotation is converted by the tachometer to an AC signal whose amplitude is proportional to the speed of the motor. This feedback signal is rectified and filtered to produce an equivalent DC signal. An operational amplifier compares the feedback signal with a reference level generated on the PCBA. The net output from the operational amplifier drives a power amplifier which in turn powers the DC motor. Figure 3-7 illustrates the circuit.

#### Rectifier and Filtering Circuits

The output of the AC tachometer is received at J4-14 and J4-15. Diode CR20 and resistor R64 form a half-wave rectifier whose output is filtered by capacitor

C41. The output of this circuit is connected into the next stage through resistor R68.

#### Comparator and Reference Circuits

Operational amplifier U6 compares the output of the rectifier circuits with a reference level generated by R66 and associated components. The reference voltage is developed by a voltage divider network composed of resistor R65 and zener diode CR21. Potentiometer R66 is connected across the constant voltage source CR21 and in series with temperature compensating diode CR22 and resistor R67. The effect of this network is to produce a temperature compensated adjustable reference level at input U6-3. Resistors R70, R72 form the feedback loop with a DC gain of 36 while resistor R71 and C42 form a filter network that stabilizes the feedback loop. The output of U6 feeds the power amplifier drivers through DC coupling network R73, R74.

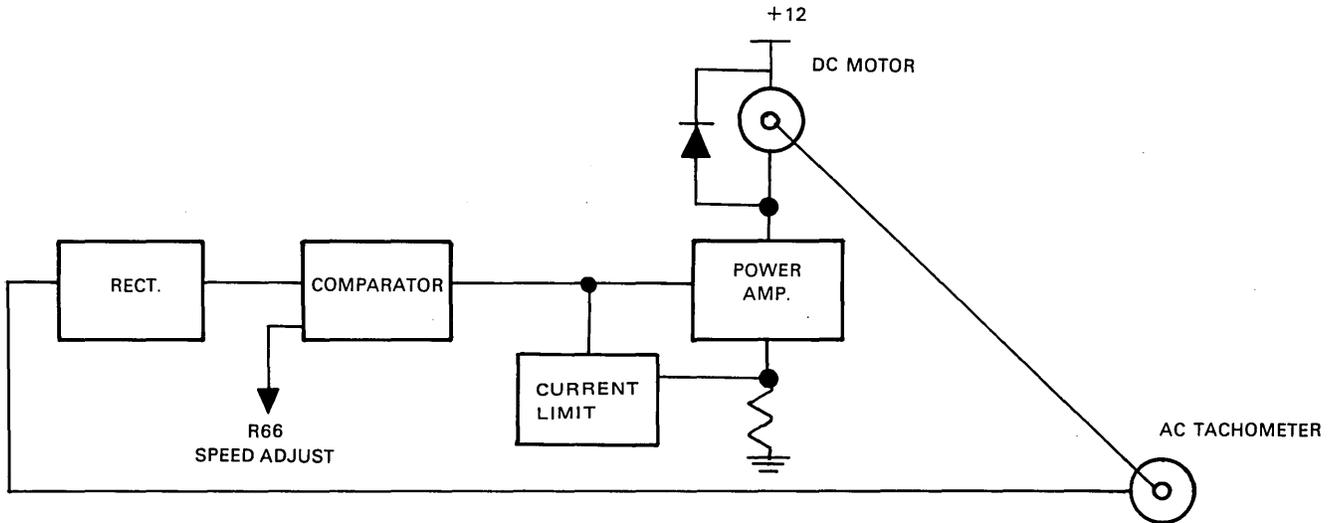


Figure 3-7. Single Drive Motor Control Circuits, Block Diagram

### Power Amplifier Circuits

The power amplifier circuits consist of Darlington pair transistor Q5, current limiter circuit Q4, and associated components. The power amplifier driver Q5 operation is controlled by the state of the MOT signal. This signal is coupled into the base of Q5 by diode CR23.

When MOT is low CR23 conducts, and the base of Q5 goes to 0.8V, cutting off Q5. When MOT goes high CR23 is cut off allowing the base of Q5 to attain its operational value (approx. 1.4V). Resistors R77, R75, R76, and Q4 form a feedback circuit that reduces the current surge caused by motor startup. When the motor-on command is received, transistor Q5 goes into saturation and collector current would normally rise to a larger value since the motor is still stationary. However, current feedback network Q4 and components will limit this initial surge to a maximum of 0.8 amp. Resistor R77 provides a convenient point to monitor the motor current. Diode CR24 protects Q5 from inductive kickback caused by commutation. L6, C37, C38, C39, and C40 are filters used to prevent high frequency transients generated by the motor from propagating into the unit electronics through the power supply.

### 3.8.3 Read Circuits Description (Ref. Sheet 7 of Dwg 100072)

These circuits process the low level information from the read head during the read cycle, reshaping it into a digital pulse stream. Figure 3-8 illustrates the functional components described in this paragraph. The

+12V supply to the elements in these circuits is filtered through L5 to provide additional noise isolation. Voltage divider R47, R48, and filter capacitor C22, develop a reference voltage (V1) of approximately 6V used in the read circuits discussed below.

### Input Clamp

The low level signal (approx. 1.5 mV pp) from the read head is fed to differentiator U24. Input diodes CR18, CR19 constitute a clamp circuit that prevent transients generated by the write cycle from breaking through into the read circuits. The junction of diodes CR18, CR19 at V2 is held at approximately +6.7V. This voltage is generated in a voltage divider R37, R36, and R38 (refer to the discussion on PSEN generation in Para. 3.8.4).

### Differentiator

The differentiator consists of U24 and its associated components. This element functions as a peak detector that generates the signal illustrated in the timing diagram of Figure 3-9, which shows the read waveforms for a sequence of "1's." Thus the output of U24 crosses the zero-base line each time a peak is detected on the input signal. Capacitor C25 yields the required 6 dB per octave rising characteristic of a differentiator. Resistor R51 terminates this characteristic at 250 kHz. This stage has an approximate gain of 40 at 125 kHz.

### Filter Circuits

The balanced output of U24 at pins 7 and 8 is fed into

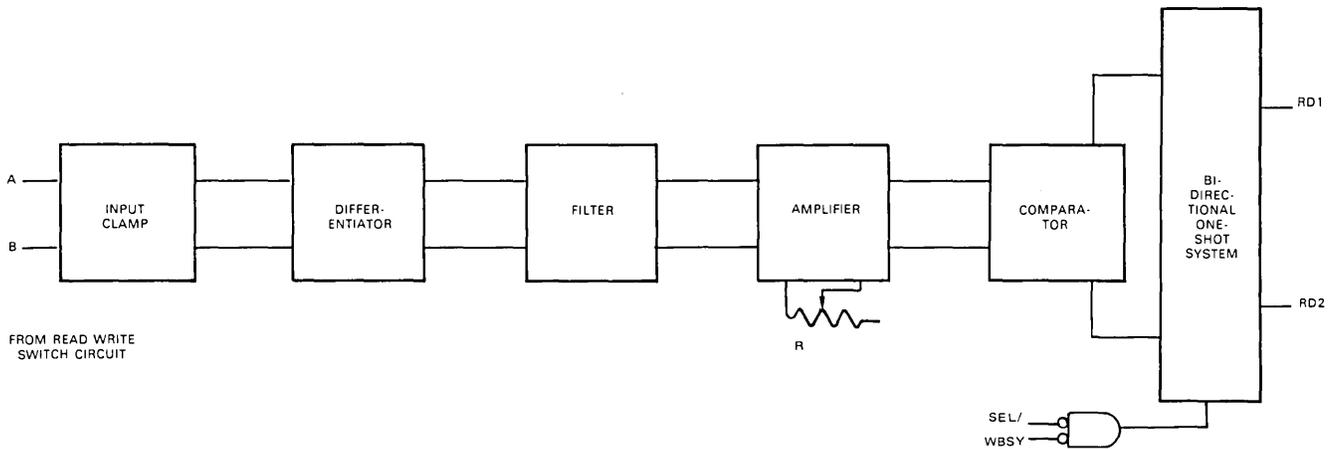


Figure 3-8. Single A Drive Read Circuits, Block Diagram

an LCR filter whose characteristics are such that a phase shift as a function of frequency is the linear function required for true reproduction of the magnetic recording signal. R52 and R53 and V1 maintain the read signal at the center of U23's linear range.

#### Amplifier Circuit

The amplifier circuit consists of U23 and resistors R54 and R55. The gain of this stage is approximately 50 and can be adjusted by R54. The balanced output of this amplifier is AC coupled into a comparator by capacitors C31, C32. Resistors R56 and R57 center the output signal from U23 at reference V1 potential.

#### Comparator Circuit

The output of the amplifier is processed by low pass filter network R58, R59, C48, thus providing additional noise rejection for this stage. Comparator U22 converts the essentially sinusoidal wave shape input into a square wave. Figure 3-9 shows this waveform conversion and timing. Capacitor C34 and resistor R61 provide a delay for the output of U22. This compensates for the inherently longer turn-on delay of U22, thus providing a symmetrical square wave to the next stage.

#### Bidirectional One-Shot System Circuits

The output of the comparator at pin 7 is connected into the input of dual one-shot U21. These elements are connected so that they each produce a pulse of fixed width corresponding to the positive and the negative edges respectively of the input waveform. Resistor R62 and capacitor C35 control one-shot

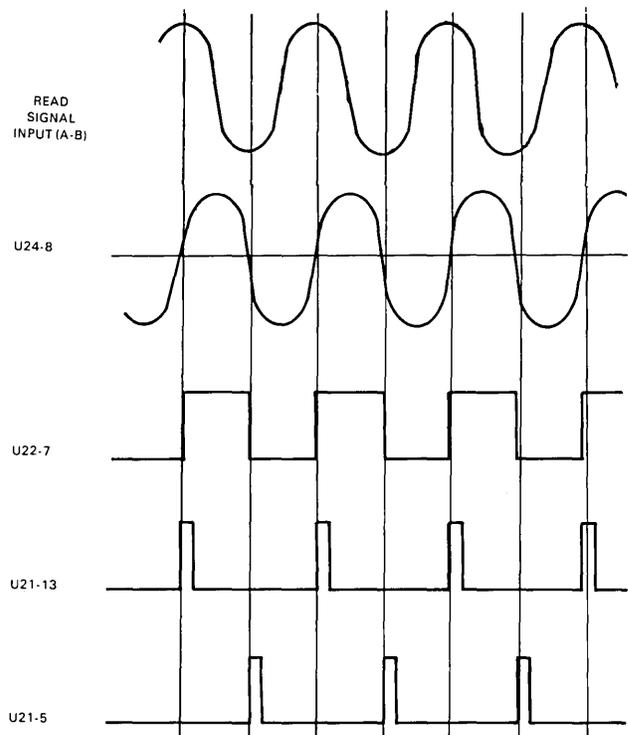


Figure 3-9. Single A Drive Read Circuits, Timing Diagram

U21-13 pulse width, while resistor R63 and capacitor C36 perform that function for U21-5. These two signals are ORed together in the interface circuits described in Para. 3.8.1. The bidirectional one-shot is reset by U16-3. If the unit is not selected, SEL is high causing U16-3 to go low, resetting U21. Similarly if the unit is in the write mode, WBSY is also high, causing U21 to reset. This logic prevents noise signals from being transmitted to the interface circuits whenever the unit is in the write mode, or the drive is not selected.

### 3.8.4 Write Circuits Description (Ref. Sheet 6 of Dwg 100072)

These circuits consist of a power supply enable (PSEN) circuit, write current control logic, write current drivers, an erase current driver, the read/write switch, and a write power control circuit. Figure 3-10 illustrates these circuits.

#### Power Supply Enable (PSEN) Circuits

The power supply enable circuits (PSEN) allows the write current to flow only when the power supply voltages (+5V and +12V) are within operational tolerances. This prevents writing on the diskette during power-up or power-down sequences of the disk drive, or accidental power loss to the unit. The PSEN circuit consists of transistors Q1, Q2, and associated components. Initially, as +5V power rises to operational level, transistor Q1 conducts as soon as the base voltage exceeds zener CR6 voltage, plus the emitter base drop of Q1, or about 3.4V. When Q1 collector current is sufficient to drop 0.7V across R23, transistor Q2 conducts, providing +12V to the remaining circuits if the +12V power is present. At the same time, voltage divider R43, R44 generates a high power-on indicator PSEN, the true state of this

logic signal. The +12V is also divided by R36, R37, and R38. Voltage dividers R36 and R37 produce about +6.7V, which is used in the input clamp of the read circuits (see Para. 3.8.3). Divider R38, R36 also develops approximately +6V. This voltage feeds the center tap of the R/W head and provides the correct bias for U24 in the read mode.

#### Write Control Logic

The write control logic provides the processing circuits necessary to gate and control the write circuits. The write control logic consists of elements U18, U10, U20, and U9. This logic controls the operation of the write current driver, the erase current driver, and the write busy (WBSY) generator. The write control signal for these circuits is generated by four external logic signals gated by U18 and U10. When WRT/ is low (TRUE) write protect (WPTSW) is low (FALSE) and the stepper or (SBSY) is low (FALSE), U18-8 is high enabling gate U10-8. If the unit is selected, SEL is high and U10-8 goes low. This condition is coupled to the base of Q3 via U20-2 generating the write busy (WBSY) signal.

As U10-8 goes low, inverter U9-10 releases the set and clear direct inputs on U19, at pins 10 and 13.

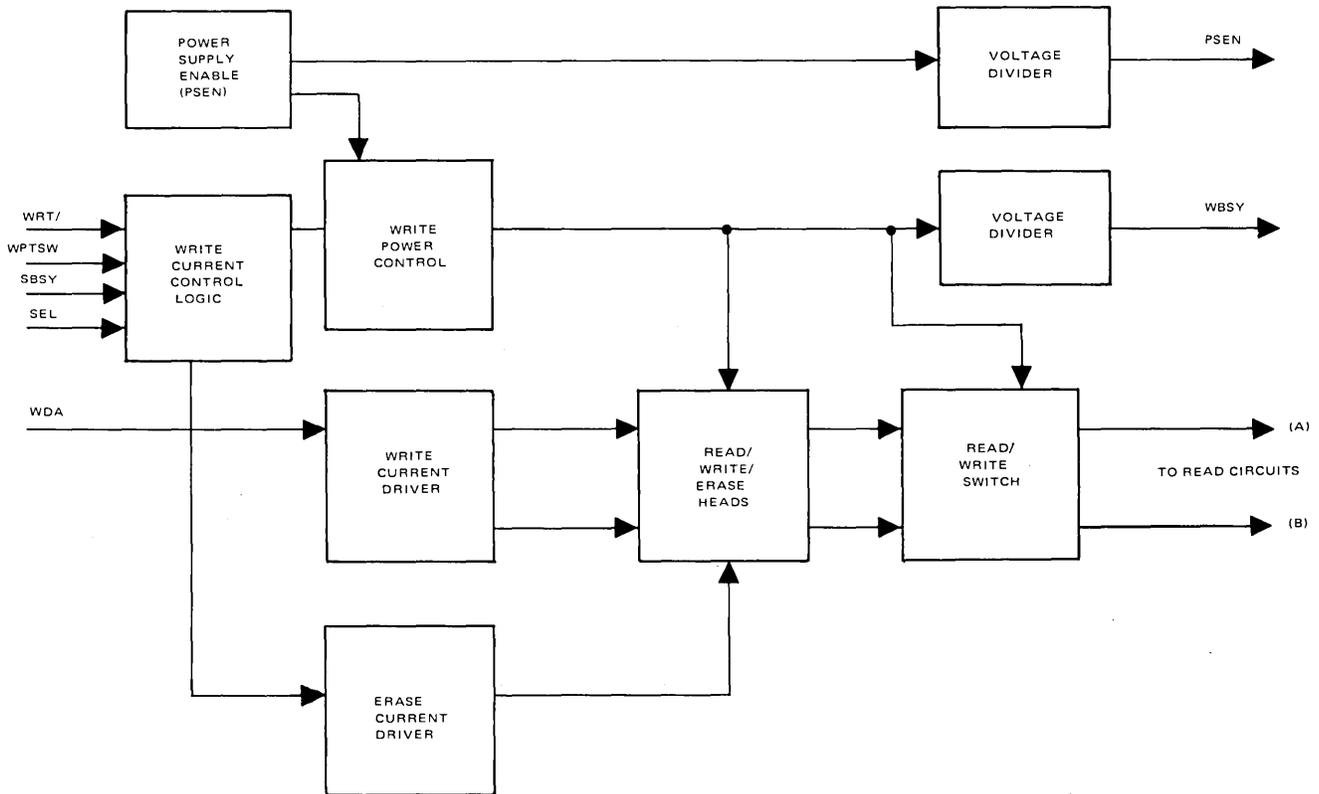


Figure 3-10. Single A Drive Write Circuits, Block Diagram

This condition enables this element to respond to the state of write data, WDA input. The low state of U10-8 also enables the erase current generator through U9-10 and U20-12. Note that when U19 pins 10 and 13 were both held low, pins 8 and 9 of U19 were both in a high state.

#### *Write Current Driver*

When the write control logic removes the set and clear direct inputs to the write flip-flop U19, write data (WDA) pulses from the interface can be processed by the write current driver circuit. The flip-flop is connected in such a manner that each time a write pulse occurs, the flip-flop toggles on the trailing edge of that pulse. The two complementary outputs of U19 are coupled by power drivers into the read/write head through resistors R30 and R31. As the flip-flop toggles, power drivers U20-10 and U20-8 are energized sequentially, thus alternately driving a current through both halves of the read/write head. Diodes CR9 and CR10 are used to isolate the write circuits from the head during the read operation, to increase noise immunity. Resistors R28, R29 ensure that CR9, CR10 are back biased when the write operation is concluded.

#### *Erase Current Driver*

Resistors R25, R26, diode CR7, and capacitors C16 and U13 combine the functions of an erase current driver with a delay generator that generates two different delays from the leading edge and the trailing edge of the input waveform. This causes the erase current to be switched on approximately 400  $\mu$ s after the write control signal has been activated, and off 800  $\mu$ s after the control signal is removed to accommodate the time delay between head write gap and erase gap using a tunnel erase head. When the circuits are not in the write mode, U20-12 is low and the output of erase driver U13-3 is high. When the write operation is initiated, U20-12 goes high. Driver U13 output now does not follow the change of state until delay network R26, C16 times out (approximately 400  $\mu$ s). At this time, U13 senses the high state of U20-12 and U13-3 goes low. This condition causes the erase current to flow from the center tap of the head through the erase winding and diode CR11. This current is defined by the values of R34 and R35.

At the conclusion of the write operation U20-12 goes low. Again U13 output does not follow this state until a new delay circuit, resistor R25 and C16, times out (approximately 800  $\mu$ s). At the end of that period

U13-3 goes high, and the erase current stops flowing. Diode CR8 absorbs the inductive emf when head winding current stops.

#### *Read Write Switch Circuits*

The read write switch consists of diodes CR12 through CR17, and resistors R39, R40, R45, R46. The function of this switch is to isolate the read circuit from the considerable voltage excursions which occur when a write operation is in effect, and to allow the read circuits to access the head when the read mode is selected.

When the write command occurs and Q3 conducts, CR14, CR15 anodes go to about 11.5V. Thus all the cathode junctions of diodes CR12 through CR17 are at about 11V. Since the anodes of diodes CR16 and CR17 cannot rise above the 6.7V clamp in the read circuits (Para. 3.8.3), CR16 and CR17 are back biased and the read circuits are effectively isolated from the read/write head. When the read mode is selected, Q3 is cut off, since the WRT/ signal is high at U18-9. Under these conditions, the circuit stabilizes with CR14 and CR15 cut off and diodes CR12, CR13, CR16, and CR17 conducting. The anodes of CR12 and CR13 are at approximately +6V since they are connected through the low impedance head to voltage divider R36, R38. Approximately 0.25 mA is supplied through resistors R45, R46, and diodes CR16, CR17. About 0.5 mA is drawn through R39, R40. Thus each of the four diodes have approximately 0.25 mA of current flowing through them. In this way, the diode bridge provides a low impedance path for the head signal to differentiator U24.

In this way, the diode bridge provides a low impedance path for the head signal to differentiator U24.

#### **3.8.5 Positioner Control (Ref. Sheet 3 of Dwg 100072)**

The positioner control circuits shown in Figure 3-11 generate signals which cause the stepper motor to move the head from track to track in response to a step command. Four sequential signals designated phase 1 ( $\phi$ 1), phase 2 ( $\phi$ 2), phase 3 ( $\phi$ 3), phase 4 ( $\phi$ 4) are sent to the stepper motor drive circuits to cause track-to-track positioning. Initially the system is in the hold-state with  $\phi$ 4 on. If a step-out command is received, the signal sequence  $\phi$ 3,  $\phi$ 2,  $\phi$ 1,  $\phi$ 4 is generated. If a step-in command is received, the signal sequence  $\phi$ 1,  $\phi$ 2,  $\phi$ 3,  $\phi$ 4 is generated.



Diodes CR2, CR3, CR4, and CR5 in conjunction with zener diode CR1 limit the turnoff transient to +20V. Referring to Figure 3-12, it can be seen that the step sequence is complete at the end of the SBSY (approximately 23 ms). If after a further 12 ms, i.e. after a total of 35 ms after a step pulse, a further step command has not been received, hold driver U5-5 is deenergized via the delay circuit U7-10, U8-6, R3, and C49. A hold current of about half the original value is then supplied via U5-3 and resistors R5, R6, R7, R8. This scheme allows a system and motor power reduction in the standby mode.

### 3.8.6 Switches, Transducer, and Head Load Solenoid Circuits (Ref. Sheets 4 and 5 of Dwg 100072)

These circuits perform several functions:

- a. Debounce the drive switches and reshape the index transducer output
- b. Energize the head load solenoid
- c. Generate the drive ready (RDY) status signal

*Switch Debouncer and Index Transducer Reshaper* (Ref. Sheet 5 of Dwg. 100072)

The door switch and Track 0 switch contacts are fed to latched gates U2 to eliminate contact bounce.

The index transducer (photo transistor) output is fed to Schmitt trigger U8-13. The output U8-12 is the sector pulse SECP which in turn feeds interface transmitter U1-9. Output U8-10 provides hysteresis thus preventing the circuit from responding to small discontinuities in the waveform.

*Head Load Solenoid Driver* (Ref. Sheet 4 of Dwg. 100072)

The head load solenoid is energized whenever the drive is selected or the HDLD signal is true. This latter mode allows the head to remain loaded even when the drive is deselected — for example, to avoid incurring a head load time in overlap operations.

Whenever the SEL/ or HDLD/ signal is low, the output of U10-11 goes high. This energizes the head load solenoid driver U3-3 provided that the motor is enabled (MTRN/low), PSEN is high, and the drive door is closed (DOOR/low).

### *Drive Ready Signal*

When the MTRN, PSEN, and DOOR signals become true, the 1½ second delay circuit U7-12, R12, C14, C15, and U8-4 is enabled. At the termination of this delay the drive read (RDY) signal is generated. This delay allows the drive motor to reach operational speed.

## 3.9 SINGLE B DRIVE (P/N 100164) PCBA, GENERAL FUNCTIONAL DESCRIPTION

This PCBA is similar to the Single A (P/N 100072) PCBA that it replaces. Three additional features are included:

- a. Optional circuits to accommodate a double headed positioner
- b. Automatic drive motor turn-on for 2 seconds to seat diskette
- c. Digital noise filtering

The Single B PCBA is compatible with the older Single A PCBA and may be used to replace this PCBA. The interface, interconnections and power requirements are essentially unchanged.

This PCBA provides the circuits necessary to read and write data on the diskette in the drive assembly. The board communicates with the interface through a 34 pin edge connector and with the disk drive through a number of molex connectors. Figure 3-6 illustrates the functional elements contained on the PCBA.

The board functional description consists of a detailed explanation of the following functional elements: interface circuits, motor control circuits, read and write circuits, positioner control circuits, and miscellaneous circuits such as switches, transducers and head load solenoid circuits. Although the circuit descriptions are supported by simplified drawings, the detailed circuit elements are shown in the schematic and logic drawings located in Section 9. These drawings are referenced by sheet and drawing number whenever appropriate.

### 3.9.1 Interface Circuits (Ref. Sheet 2 of Dwg 100164)

The interface circuits consist of receivers, terminators, transmitters, and select logic. The incoming signals are terminated with a 220/330 ohm ter-

minator pack U17. A jumper in one of the positions W1, W2, W3 and W4 causes the drive selection logic to respond to one of the drive select input lines DS1 through DS4. The appropriate select line is terminated by RN1 and received by U10-2. The select signal gates the output signals directly via transmitters U1 and indirectly in the case of the read data signal on U25-5 (Sheet 7 of Dwg 100164). It also drives a LED panel indicator through driver U9-4 which shows when the drive has been selected. Complements of a number of input signals are developed on this sheet.

Versions of the board determine terminator and address response configurations. A master unit is configured with terminators and with W1 inserted. Add-on units are configured to be placed at an intermediate point on a daisy chain and have terminators removed and W2 inserted. (W3 and W4 could be inserted.)

### **3.9.2 Motor Control** (Ref. Sheet 8 of Dwg 100164)

The motor control circuit is a closed loop servo, controlling the spindle drive system. The spindle drive consists of a DC motor and AC tachometer mounted on a common shaft. The DC motor shaft rotation is converted by the tachometer to an AC signal whose amplitude is proportional to the speed of the motor. This feedback signal is rectified and filtered to produce an equivalent DC signal. An operational amplifier compares the feedback signal with a reference level generated on the PCBA. The net output from the operational amplifier drives a power amplifier which in turn powers the DC motor. Figure 3-7 illustrates the circuit.

#### *Rectifier and Filtering Circuits*

The output of the AC tachometer is received at J4-14 and J4-15. Diode CR30 and resistor R70 form a half-wave rectifier whose output is filtered by capacitor C44. The output of this circuit is connected to the operational amplifier through resistor R74.

#### *Comparator and Reference Circuits*

Operational amplifier U7 compares the output of the rectifier circuits with a reference level established by R72 and associated components. The reference voltage is developed by a voltage divider network composed of resistor R71 and zener diode CR31. Potentiometer R72 is connected across the constant voltage source CR31 and in series with temperature

compensating diode CR32 and resistor R73. The effect of this network is to produce a temperature compensated adjustable reference level at input U7-3. Resistors R76, R78 form the feedback loop with a DC gain of 36. The output of U7 feeds the power amplifier drivers through DC coupling network R79, R80.

#### *Power Amplifier Circuits*

The power amplifier circuits consist of Darlington pair transistor Q7, current limiter circuit Q6, and associated components. The power amplifier driver Q7 operation is controlled by the state of the MOT signal. This signal is coupled into the base of Q7 by diode CR33.

When MOT is low CR33 conducts, and the base of Q7 goes to 0.8V, cutting off Q7. When MOT goes high CR33 is cut off allowing the base of Q7 to attain its operational value (approx. 1.4V). Resistors R83, R81, R82, and Q6 form a feedback circuit that reduces the current surge caused by motor startup. When the motor-on command is received, transistor Q7 goes into saturation and the collector current would normally rise to a large value since the motor is still stationary. However, current feedback network Q6 and components will limit this initial surge to a maximum of 0.8 amp. Resistor R83 provides a convenient point to monitor the motor current. Diode CR34 protects Q7 from inductive kickback caused by commutation. L6, C40, C41, C42, and C43 are filters used to prevent high frequency transients generated by the motor from propagating into the unit electronics through the power supply.

### **3.9.3 Read Circuits Description** (Ref. Sheet 7 of Dwg 100164)

These circuits process the low level information from the read head during the read cycle, reshaping it into a digital pulse stream. Figure 3-8 illustrates the functional components described in this paragraph. The +12V supply to the elements in these circuits is filtered through L5 to provide additional noise isolation. Voltage divider R54, R55, and filter capacitor C24, develop a reference voltage (V1) used in the read circuits discussed below.

#### *Input Clamp*

The low level signal (approx. 1.5 mV pp) from the read head is fed to differentiator U28. Input diodes

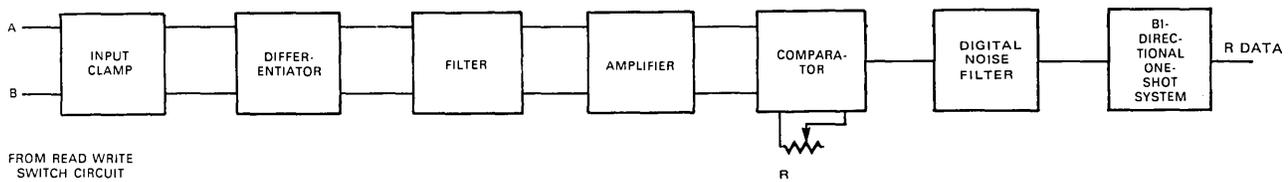


Figure 3-13. Single B Drive Read Circuits, Block Diagram

CR28, CR29 constitute a clamp circuit that prevent transients generated by the write cycle from breaking through into the read circuits. The junction of diodes CR28, CR29 at V2 is held at approximately +6.7V. This voltage is generated in a voltage divider R41, R42, R43 (refer to the discussion on PSEN generation in Para. 3.9.4).

#### Differentiator

The differentiator consists of U28 and its associated components. This element functions as a peak detector that generates the signal illustrated in the timing diagram of Figure 3-14, which shows the read waveforms for a sequence of "1's." Thus the output of U28 crosses the zero-base line each time a peak is detected on the input signal. Capacitor C25 yields the required 6 dB per octave using characteristic of a differentiator. Resistor R56 terminates this characteristic at 250 kHz. This stage has an approximate gain of 40 at 125 kHz. V1 maintains the DC level of read signal at the center of the operating range of U27 and U28.

#### Filter Circuits

The balanced output of U28 at pins 7 and 8 is fed into an LCR filter whose characteristics are such that a phase shift as a function of frequency is the linear function required for true reproduction of the magnetic recording signal.

#### Amplifier Circuit

The amplifier circuit consists of U27 and resistors R59 and R60. The gain of this stage is approximately 50 and can be adjusted by R59. The balanced output

of this amplifier is AC coupled into a comparator by capacitors C32, C33, and resistors R63, R64.

#### Comparator Circuit

The output of the amplifier is processed by low pass filter network R63, R64, C35, thus providing additional noise rejection for this stage. Comparator U26 converts the essentially sinusoidal wave shape input into a square wave. Figure 3-14 shows this waveform conversion and timing.

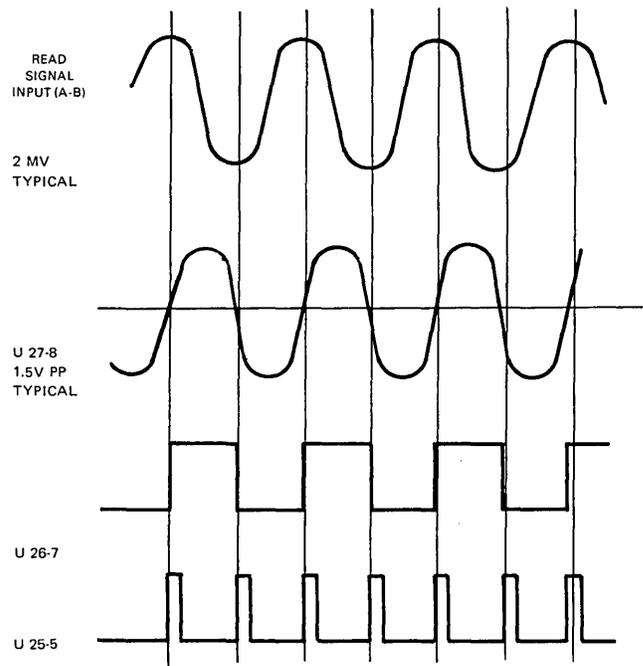


Figure 3-14. Single B Drive Read Circuits, Timing Diagram

### Digital Noise Filter Circuit

The output of comparator U26 is connected to one-shot U25-13 via an exclusive "OR" gate U24-6 and to flip-flop U23-9. These three logic elements and their associated components form a digital noise filter whose function is to reject short duration pulse type noise. The filter will reject noise pulses of a duration of less than 3 us (approx.) in an MFM version of the PCBA and less than 1.3 us in a GCR version.

Since U24-6 is an exclusive "OR" gate, a short duration high going pulse will be generated at U24-6 for every change in state of U26-7. This is due to the delay at U24 pin 5 created by R66 and C36. U25-13 will therefore fire for every transition. R67 and C37 determine the one-shot pulse width. U23-9 pin 11 will clock at the end of 3us (1.3us for GCR); and if the change in state which fired U25-13 is still present at U23 pin 12, then U23 pin 9 will assume the same state. U23 pin 12 will not change in less than 3 us (1.3 for GCR) for normal data transition. U23-9 will not change state for a short duration noise pulse, occurring at U26-7, since by the time the clock edge gen-

erated by the noise pulse is available at U23-11, the enable input at U23-12 is false.

### Bidirectional One-Shot

Operation of exclusive "OR" gate U24-8 is identical to that described for U24-6. Every change in state of U23-9 (every data transition) will cause a high-going pulse to be generated by 24-8. Element U24-5, a 0.9 us one-shot will fire for all transitions generating R DATA (see Figure 3-14). R69 and C39 determine the one-shot pulse width. U20 holds U25 reset whenever the drive is not selected or is in a write mode. This prevents noise from being transmitted to the interface.

### 3.9.4 Write Circuits Description (Ref. Sheet 6 of Dwg 100164)

These circuits consist of a power supply enable (PSEN) circuit, a head select circuit, write current control logic, write current drivers, an erase current driver, the read/write switch, a write power control circuit. Figure 3-15 illustrates these circuits.

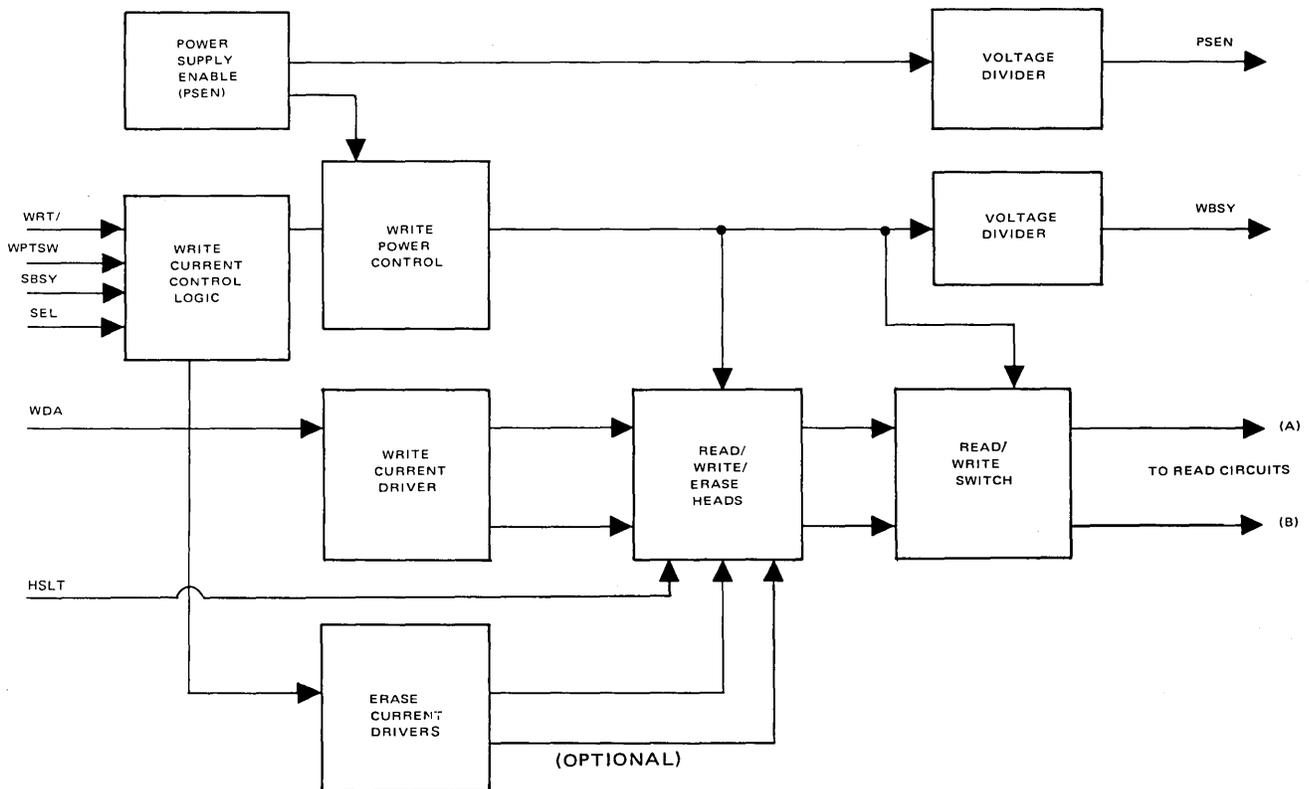


Figure 3-15. Single B Drive Write Circuits, Block Diagram

### *Power Supply Enable (PSEN) Circuits*

The power supply enable circuits (PSEN) allows the write current to flow only when the power supply voltages (+5V and +12V) are within operational tolerances. This prevents writing on the diskette during power-up or power-down sequences of the disk drive, or accidental power loss to the unit. The PSEN circuit consists of transistors Q1, Q2, and associated components. Initially, as +5V power rises to operational level, transistor Q1 conducts as soon as the base voltage exceeds zener CR8 voltage, plus the emitter base drop of Q1, or about 3.4V. When Q1 collector current is sufficient to drop 0.7V across R19, transistor Q2 conducts, providing +12V to the remaining circuits if the +12V power is present. At the same time, voltage divider R50, R51 generates a high logic level PSEN, enabling the positioner and head load circuitry. The +12V is also divided by R41, R42, and R43. These dividers produce about +6V, which is used in the input clamp of the read circuits (see Para. 3.9.3) and feeds the center tap of the R/W head, providing the correct bias for U28 in the read mode.

### *Head Select Circuit*

The 100164 (Single B) PCBA is used in both single and double head drive mechanisms. Enclosed within the dotted line on sheet 6 is the write current supply (Q5) upper R/W/E erase head (J8) and the erase timer/current driver (U8). These components are absent on single sided versions of the PCBA.

The head selection levels HSLT and HSLT/, from sheet 2, are applied to U14-3 and U14-5 to enable respectively the lower or upper head erase drivers and to U22-10 and U22-8. If the lower (normal) head is selected, U22-10 will be low turning on Q4. Q5 in turn will be turned off by HSLT/ being high. Write current from Q3 or read bias from R41, R42 and R43 will therefore be coupled to the correct head.

### *Write Control Logic*

The write control logic provides the processing circuits necessary to gate and control the write circuits. The write control logic consists of elements U18, U20, U22, and U24. This logic controls the operation of the write current drivers, the erase current driver(s), and the write busy (WBSY) generator. The write control signal for these circuits is generated by four external logic signals gated by U18 and U20. When WRT/ is low (TRUE) write protect (WPT) is low (FALSE) and the stepper or (SBSY) is low (FALSE),

U20-12 is high, enabling gate U18-13. If the unit is selected, SEL is high and U18-11 goes low. This condition is coupled to the base of Q3 via U22-6 generating the write busy (WBSY) signal.

As U18-11 goes low, exclusive "OR" gate U24-11 goes high, releasing the set and clear direct inputs on U21 at pins 10 and 13.

This condition enables this element to respond to the state of write data, WDA input. The low state of U18-11 also enables the erase current generators through U24-11, U14-3 and U14-5.

### *Write Current Driver*

When the write control logic removes the set and clear direct inputs to the write flip-flop U21, write data (WDA) pulses from the interface can be processed by the write current driver circuit. When both set and clear were low, both outputs were in a high state. The flip-flop is connected in such a manner that each time a write pulse occurs, the flip-flop toggles on the trailing edge of that pulse. The two complementary outputs of U21 are coupled by power drivers into the read/write head through resistors R31 and R32. As the flip-flop toggles power drivers U22-2 and U22-12 are energized sequentially, thus alternately driving a current through both halves of the read/write head. Diodes CR14 and CR15 are used to isolate the write circuits from the head during the read operation, to increase noise immunity. Resistors R27, R28 ensure that CR14, CR15 are back biased when the write operation is concluded.

### *Erase Current Driver*

Resistors R21, R22, diode CR9, and capacitor C10 and U15 combine the functions of an erase current driver with a delay generator that generates two different delays from the leading edge and the trailing edge of the input waveform to compensate for the distance between R/W base gap and the tunnel erase gaps. This causes the erase current to be switched on approximately 400 us after the write control signal has been activated, and off 800 us after the control signal is removed. When the circuits are not in the write mode, U14-3 is low and the output of erase driver U15-3 is high. When the write operation is initiated, U14-3 goes high. Driver U15 output does not follow the change of state until delay network R21 and C10 times out (approximately 400 us). At this time, U15 senses the high state of U14-3 and U15-3 goes low. This condition causes the erase current to

flow from the center tap of the head through the erase winding and diode CR18. This current is defined by the value of R35.

At the conclusion of the write operation U14-3 goes low. Again U15 output does not follow this state until a new delay circuit, resistor R22 and C16, times out (approximately 800 us). At the end of that period U15-3 goes high, and the erase current stops flowing. Diode CR8 absorbs the inductive emf when head winding current stops.

The operation of the U8 and the associated circuitry within the dashes lines is identical to that described above. This circuitry is only present on double head drives. Jumper W9 is required on single headed versions of the PCBA to prevent Q3 from switching to a read mode prior to the conclusion of the erase operation.

#### *Read Write Switch Circuits*

The read write switch consists of diodes CR16, CR17, CR19, CR20 and CR22 through CR27, and resistors R44, R45, R48, R49. The function of this switch is to isolate the read circuit from the considerable voltage excursions which occur when a write operation is in effect, and to allow the read circuits to access the head when the read mode is selected.

When the write command occurs and Q3 conducts, CR24, CR25 anodes go to about 11.5V. Thus all the cathode junctions of diodes CR22, CR23, CR26 and CR27 are at about 11V. Since the anodes of diodes CR26 and CR27 cannot rise above the 6.7V clamp in the read circuits (Para. 3.9.3), CR26 and CR27 are back biased and the read circuits are effectively isolated from the read/write head. When the read mode is selected, Q3 is cut off, since the WRT/ signal is high at U20-1. Under these conditions, the circuit stabilizes with CR24 and CR25 cut off and diodes CR22, CR23, CR26, and CR27 conducting. The anodes of CR22 and CR23 are at approximately +6V as established by the voltage drivers consisting of R41, R42 and R43 Q4 (or Q5) and R37. (Q3 is turned off.) Approximately 0.25 mA is supplied through resistors R48, R49, and diodes CR26, CR27. About 0.5 mA is drawn through R44, R45. Thus each of the four diodes have approximately 0.25 mA of current flowing through them.

In this way, the diode bridge provides a low impedance path for the head signal to differentiator U28.

#### **3.9.5 Positioner Control (Ref. Sheet 3 of Dwg 100164)**

The positioner control circuits shown in Figure 3-11 generate signals which cause the stepper motor to move the head from track to track in response to a step command. Four sequential signals designated phase 1 ( $\phi 1$ ), phase 2 ( $\phi 2$ ), phase 3 ( $\phi 3$ ), phase 4 ( $\phi 4$ ) are sent to the stepper motor drive circuits to cause track-to-track positioning. Initially the system is in the hold-state with  $\phi 4$  on. If a step-out command is received, the signal sequence  $\phi 3$ ,  $\phi 2$ ,  $\phi 1$ ,  $\phi 4$  is generated. If a step-in command is received, the signal sequence  $\phi 1$ ,  $\phi 2$ ,  $\phi 3$ ,  $\phi 4$  is generated.

The positioner control circuits consist of a gated NE555 oscillator U6, a LS51 dual and/or gate U19, which is used as a multiplexer and three LS74 flip-flops, U13-9, U13-5 U21-5, which comprise the sequencer. For ease in understanding these flip-flops have been designated S1, S2, and S3 respectively. Figure 3-12 is a timing diagram showing operation of the positioner control. Initially the oscillator is held clear and the flip-flops are reset. When a step pulse occurs and the drive is selected, and not writing, a positive going pulse is generated at U11-10. The trailing edge of this pulse sets flip-flop U13-9 so that:

- a. The hold driver U5 is deenergized.
- b. The SBSY line is set high thereby starting the NE555 oscillator and inhibiting writing operations via U18-8 for the duration of the stepping cycle.

The oscillator output then sets U13-5 and U21-5 in turn. The outputs from the sequence logic are fed to the multiplexer. The polarity of the direction signal DIRN conditions the multiplexer to generate the appropriate waveform sequence. This in turn is fed to the driver circuits U4-3, U3-3, U4-5, U5-3, and U5-5 causing the stepper motor to step-in (DIRN low) or step-out (DIRN high).

Diodes CR3, CR4, CR5, and CR6 in conjunction with zener diode CR2 limit the turnoff transient to +20V. Referring to Figure 3-12, it can be seen that the step sequence is complete at the end of the SBSY (approximately 23 ms). If after a further 12 ms, i.e. after a total of 35 ms after a step pulse, a further step command has not been received, hold driver U5-3 is deenergized via the delay circuit U9-12, U10-8, R6, and C33. A hold current of about half the original value is then supplied via U5-5 and resistors R7, R8, R9, R10. This scheme allows a system and motor power reduction in the standby mode.

### 3.9.6 Switches, Transducer, and Head Load Solenoid Circuits (Ref. Sheets 4 and 5 of Dwg 100164)

These circuits perform several functions:

- a. Debounce the drive switches and reshape the index transducer output
- b. Energize the head load solenoid
- c. Generate the drive ready (RDY) status signal

*Switch Debouncer and Index Transducer Reshaper* (Ref. Sheet 5 of Dwg 100164)

The door switch Track 0 switch and write protect switch contacts are fed to latched gates U2 to eliminate contact bounce.

The index transducer (photo transistor) output is fed to Schmitt trigger U10-4. The output U10-10 is the index/sector pulse SECP which in turn feeds interface transmitter U1-8 (Sheet 2). Output U10-10 provides hysteresis thus preventing the circuit from responding to small discontinuities in the waveform.

*Head Load Solenoid Driver* (Ref. Sheet 4 of Dwg 100164)

The head load solenoid is energized whenever the drive is selected or the HDLD signal is true. This latter mode allows the head to remain loaded even when the drive is deselected — for example, to avoid incurring a head long time in overlap operations since as drive to drive disk copying.

Whenever the SEL/ or HDLD/ signal is low, the output of U12-11 goes high. This energizes the head load solenoid driver U3-5 provided that the motor is enabled (MTRN/low), PSEN is high, and the drive door is closed (DOOR/low).

#### *Drive Ready Signal*

When the MTRN, PSEN, and DOOR signals become true the 1½ second delay circuit U9-2, R12, R14, C7, C8 and U10-6 is enabled. At the termination of this delay the drive read (RDY) signal is generated. This delay allows the drive motor to reach operational speed.

#### *Drive Motor Initialization*

To insure registration of the media whenever a diskette is inserted into the drive, the drive motor is automatically turned on for 1½ seconds, indepen-

dent of the state of MTRN. The delay circuit consisting of U9-10, R11, R13, C5, C6 and U10-2 generate a high MOT for 1½ seconds after DOOR/ goes low.

### 3.10 DUAL DRIVE PCBA GENERAL FUNCTIONAL DESCRIPTION

Functional organization of the Dual A PCBA is shown in Figure 3-13. The system consists of read/write circuits, drive motor control, positioner control logic, head load solenoid driver, switch and transducer processing circuits, multiplexing circuits to deal with the two drives, and interface and terminator circuits.

#### 3.10.1 Interface Circuits (Ref. Sheet 2 of Dwg 100061)

Selection of either of the two drives is accomplished through the interface. The interface circuits consist of receivers, terminators, transmitters, and select logic. Incoming signals are terminated by 150 ohm resistors R1 through R6. A jumper pair W1 and W2 or W3 and W4 cause the drive selection logic to respond to one of the drive select input line pairs DS1 and DS2 or DS3 and DS4. The appropriate select line pair is routed via switch SW1 to terminators R7 and R8 and receivers U2-5 and U2-2. The outputs of these receivers generate the upper and lower drive select signals SELA and SELB and are OR'd by gate U2-13 to generate a module select signal. Multiplexer U3 combines the functions of multiplexing output signals from the two drives and gating them to the interface transmitters U5.

Versions of the board determine terminator and address response configurations. A master unit is configured with terminators and displays showing '0' and '1.' An add-on unit is configured to be placed at an intermediate point on a daisy chain and has the terminators removed and the displays showing '2' and '3.'

Switch SW1 serves to interchange the addresses to which upper and lower drives respond. Normally with the switch UP, the upper drive responds to address '0' and the lower to '1' for a master unit. With the switch DOWN the upper drive responds to address '1' and the lower to '0.' For add-on units '0' and '1' are replaced by '2' and '3.'

The READY sector pulse, track zero, and write protect status signals from both drives are fed to the LS157 multiplexer. Selection of a drive causes either SELA or SELB to be asserted, gating the status signals from the corresponding drive (A or B) to the interface.

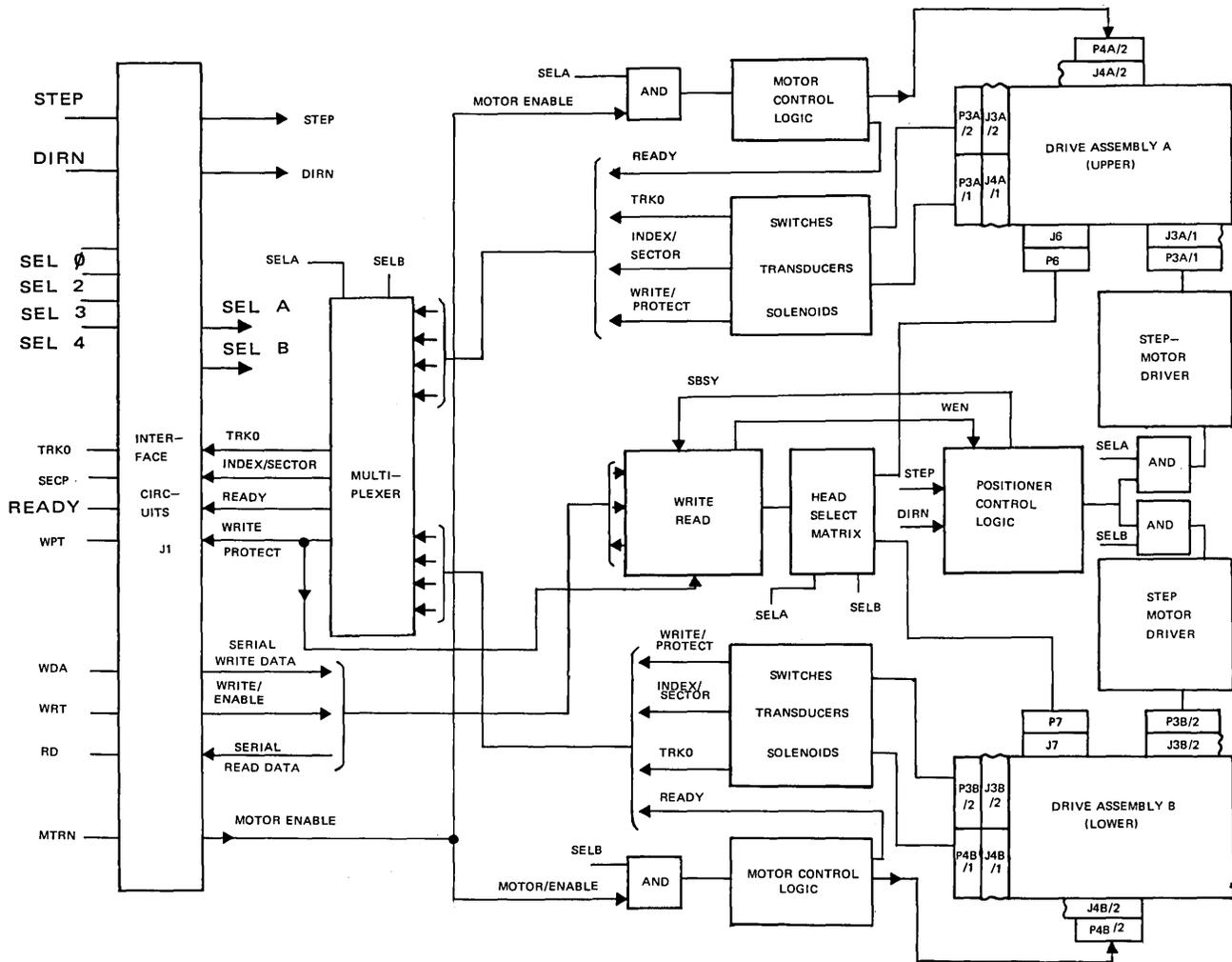


Figure 3-16. Dual Drive, Block Diagram

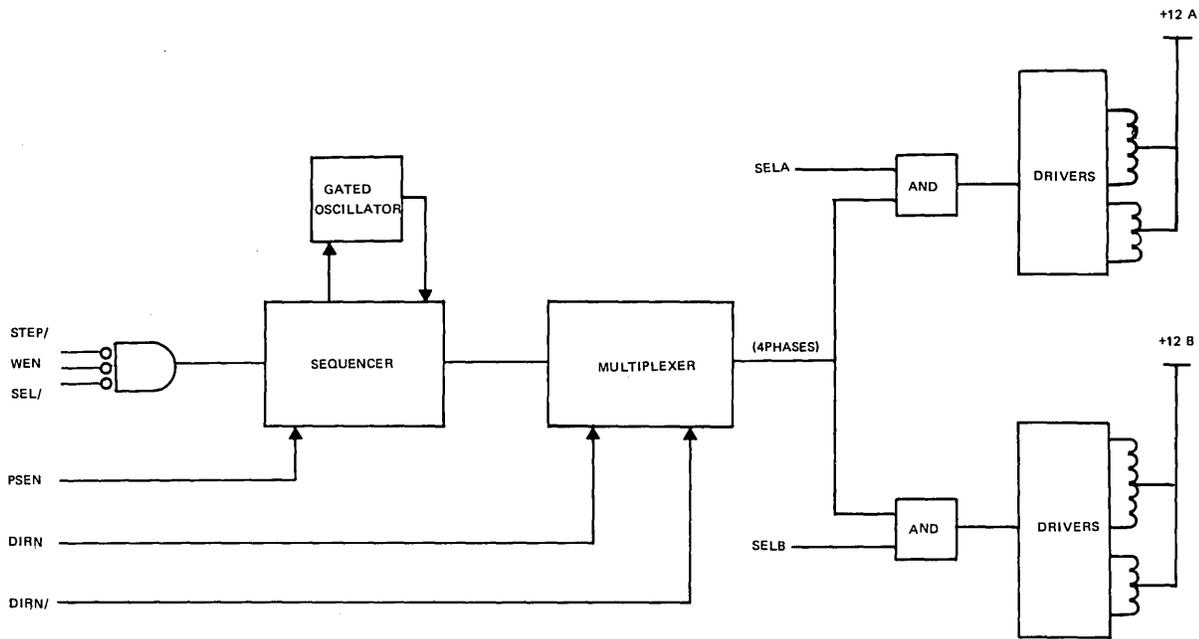
### 3.10.2 Positioner Control (Ref. Sheet 3 of Dwg 100061)

The positioner control generates signals causing the stepper motor to move the head from track to track in response to the step command. Figure 3-14 illustrates the circuit components relationship. Four sequential signals, designated phase 1 ( $\phi 1$ ), phase 2 ( $\phi 2$ ), phase 3 ( $\phi 3$ ), phase 4 ( $\phi 4$ ) are sent to the stepper motor to cause track-to-track positioning. Initially the system is in the hold state with  $\phi 4$  on. If a step-out command is received, the signal sequence  $\phi 3, \phi 2, \phi 1, \phi 4$  is generated. Conversely, the positioner control generates the signal sequence  $\phi 1, \phi 2, \phi 3, \phi 4$  if a step-in command is received. The positioner control circuits consist of a gated NE555 oscillator U8, an LS157 multiplexer, and three LS74 flip-flops (U10-5, U10-9, U11-5 and S1, S2, S3 respectively). Figure 3-12, timing diagram, shows operation of the positioner control. Initially, the oscillator is held clear and the flip-flops are reset. When the first step pulse

occurs, with the drive selected and not writing, S1 goes high, serving to (1) generate a low at U9-10, causing the S1 high to be gated to the  $\phi 4$  line, removing the hold to the stepper motor, and (2) set the SPSY line high, starting the NE555 oscillator and inhibiting writing operations via U4-10 (Ref. Sheet 4 of Dwg 100061) for the duration of the stepping cycle.

The polarity of the direction signal (DIRN/) now conditions the multiplexer to generate either the  $\phi 1, \phi 2, \phi 3, \phi 4$ , or the  $\phi 3, \phi 2, \phi 1, \phi 4$  sequence, as shown in the timing diagram. DIRN/ low causes step in, and DIRN/ high causes step out.

Position control signals ( $\phi 1, \phi 2, \phi 3, \phi 4$ ) are fed to each drive and gated by the drive select signal (SELA or SELB) to energize the stepper motor coils in sequence for track-to-track positioning. Diodes CR23, 24, 25, 26 suppress counter EMF when coils are deenergized. Zener CR22 provides a reference voltage to shorten the switch-off transient.



**Figure 3-17. Dual Drive Positioner Control Circuits, Block Diagram**

### 3.10.3 Switches, Transducer, and Head Load Solenoid Circuits (Ref. Sheets 7 and 9 of Dwg 100061)

These circuits perform several functions related to the drive mechanism:

- a. Debounces the drive switches and reshapes the pulses from the index transducer
- b. Energizes the head load solenoid
- c. Provides drive current for the stepper motor
- d. Generates the drive read status signal
- e. Drives the front panel L.E.D.'s

Sheets 7 and 9 of Dwg 100061 show the circuits for Drives A and B, respectively. Since the interfaces are essentially identical, only the Drive A interface will be discussed.

#### *Drive Switch Debounce and Index Pulse Reshape*

The door switch and track 0 switch closures are fed to latched gates (U21) to eliminate contact bounce. The index and sector pulses from the sector/index transducer (a photo transistor) is fed to Schmitt trigger U22-3 which generates the index/sector (SECP) pulse. U22-6 provides positive feedback to produce hysteresis, thus preventing the circuit from

responding to small discontinuities in the waveform.

#### *Head Load Solenoid Driver*

When the drive is selected (SELA) or a head load command (HLD) is received, a low appears at U23-5. If the motor is enabled (MTRN high), power supply voltage is within tolerance (PSEN high), and the diskette door is closed (MOTA high), U23-4 goes high, causing power NAND gate U24-5 to energize the head load solenoid. CR21 suppresses back EMF when the solenoid is deenergized. Use of the HLD signal allows the head to remain loaded even when the drive is deselected for example, to avoid incurring a head load time in overlap operation.

#### *Drive Ready Signal*

When the MTRN, PSEN, and DOORA/ signals become true, a 1½-second delay network (consisting of R63, R64, C32, C33) is enabled. At the termination of the delay the drive ready (RDY) signal is generated and fed to the drives interface. The delay provides for the motor to come up to speed before the drive is used to read or write information.

#### *Front Panel L.E.D. Display*

The display consists of the drive selected and write protect indicators together with an address indicator which displays the address to which the drive will respond. In the case of a master drive the addresses

are 0 and 1 or 1 and 0 as determined by switch SW1. In the case of an add-on drive the addresses are 2 and 3 or 3 and 2 as determined by the switch. See Table II of Sheet 1 to determine which resistors (R69-R78) should be present.

In the quiescent state with power on and the door open, U23-8 is high so that U23-10 is low. Q6 is therefore on and the display illuminates. If the MTRN is true and the door is closed, U23-8 goes low, Q6 is turned off, and the display goes out. At the end of the 1½ second ready delay U23-9 goes high and the display is illuminated again showing that the drive is ready.

### 3.10.4 Spindle Motor Control Circuit (Ref. Sheets 8 and 10 of Dwg 100061)

The spindle motor control circuits for both drives are identical. Therefore, only the circuit for drive A will be described. The circuit is illustrated in Figure 3-7. The motor control circuit is a closed loop servo controlling the spindle drive system. The spindle drive consists of a DC motor and AC tachometer mounted on a common shaft. The DC motor shaft rotation is converted by the tachometer to an AC signal whose amplitude is proportional to the speed of the motor. This feedback signal is rectified and filtered to produce an equivalent DC signal. An operational amplifier compares the feedback signal with a reference level generated on the PCBA. The net output from the operational amplifier drives a power amplifier which in turn powers the DC motor.

#### *Rectifier and Filtering Circuits*

The output of the AC tachometer is received at J4A-14 and J4A-15. Diode CR27 and resistor R87 form a half-wave rectifier whose output is filtered by capacitor C39. The output of this circuit is connected into the next stage through R91.

#### *Comparator and Reference Circuits*

Operational amplifier U27 compares the output of the rectifier circuits with a reference level generated by R89 and associated components. The reference voltage is developed by a voltage divider network composed of resistor R88 and zener diode CR28. Potentiometer R89 is connected across the constant voltage source CR28 and in series with temperature compensating diode CR29 and resistor R90. The effect of this network is to produce a temperature compensated adjustable reference level via R92 at input U27-3. Resistors R93, R95 form the feedback loop which defines an operational amplifier DC gain

of 36, while R94 and C40 form a filter network that stabilizes the feedback loop. The output of U27 feeds the power amplifier drivers through DC coupling network R96, R97.

#### *Power Amplifier Circuits*

The power amplifier circuits consist of Darlington transistor pair Q8 and current limiter circuit Q7 and associated components. The power amplifier driver Q8 operation is controlled by the state of the MOTA signal. This signal is coupled into the base of Q8 by diode CR30.

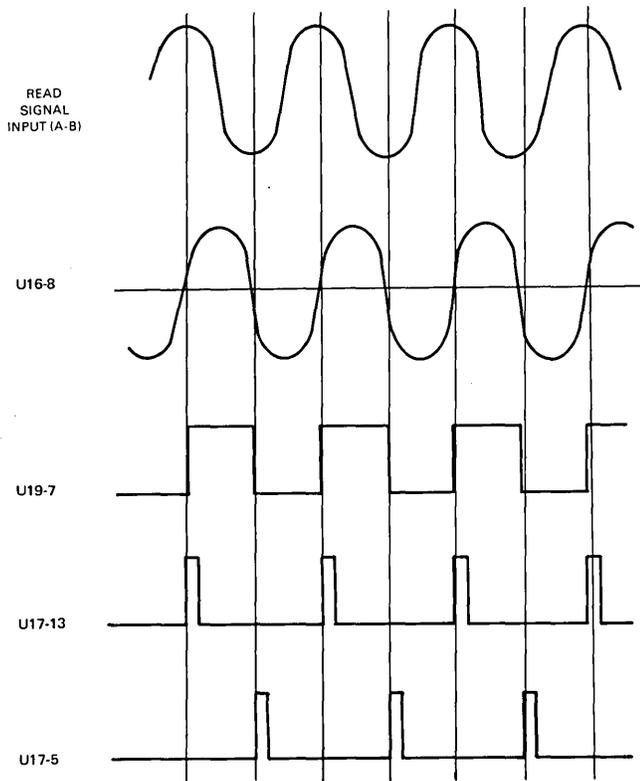
When MOTA is low, CR30 conducts, and the base of Q8 is at 0.8V, cutting off Q8. When MOTA goes high, CR30 is cut off, allowing the base of Q8 to attain its operational value (approx. 1.4V). Resistors R98, R99, R100, and Q7 form a feedback circuit that reduces the current surge caused by motor startup. When the motor-on command is received, transistor Q8 goes into saturation and collector current would normally rise to a large value since the motor is still stationary. However, current feedback network Q7 and components limit this initial surge to a maximum of 0.8 amp. This network effectively reduces current surges in the power supply caused by drive startup. R100 provides a convenient point to monitor the motor current. Diode CR31 protects Q8 from inductive kickbacks caused by commutation. L6, C35, C36, C37, C38 are filters used to prevent high frequency transients generated by the motor from propagating into the unit electronics through the power supply.

### 3.10.5 Read Circuits (Ref. Sheet 5 of Dwg 100061)

The read circuits process the low level information from the read head during the read cycle, reshaping it into a digital pulse stream. Figure 3-8 shows the functional components described in this paragraph while Figure 3-18 illustrates the read circuits timing. The +12V supply to the elements in these circuits is filtered through L5 to provide additional noise isolation. Voltage divider R50, R51 and filter capacitor C57 develop a reference voltage (V1) used in the read circuits discussed below.

#### *Input Clamp*

The low level signal (approx. 1.5 mV pp) from the read head is fed to differentiator U16. Input diodes CR20, CR19 constitute a clamp circuit that prevent



**Figure 3-18. Dual Drive Read Circuits, Timing Diagram**

transients generated by the write cycle from breaking through into the read circuits. The junction of diodes CR19 at V2 is held at approximately +6.7 volts. This voltage is generated in the write circuits (see Para. 3.9.4).

#### *Differentiator*

The differentiator consists of U16 and its associated components. This element functions as a peak detector that generates the signal illustrated in the timing diagram of Figure 3-18, which shows the read waveforms for a series of 1's. Thus the output of U16 crosses the zero-base line each time a peak is detected on the input signal. Capacitor C21 yields the required 6 dB per octave rising characteristic of a differentiator. Resistor R47 terminates this characteristic at 250 kHz. This stage has an approximate gain of 40 at 125 kHz.

#### *Filter Circuits*

The balanced output of U16 at pins 7 and 8 is fed into an LCR filter whose characteristics are such that a phase shift as a function of frequency is the linear function required for true reproduction of the

magnetic recording signal. R52 and R53 in conjunction with V1 maintain the read signal in the center of U16 and U18 linear range.

#### *Amplifier Circuit*

The amplifier circuit consists of U18 and resistors R54 and R55. The gain of this stage is approximately 30, and can be adjusted by R54. The balanced output of this amplifier is AC coupled into a comparator by capacitors C26, C27. Resistors R56, R57 and U1 maintain U18's output at the center of its operating range.

#### *Comparator Circuit*

The output of the amplifier is processed by low pass filter network R58, R59, C60, thus providing additional noise rejection for this stage. Comparator U19 converts the essentially sinusoidal wave shape input into a square-wave. Figure 3-18 shows this waveform conversion and timing. Capacitor C28 and resistor R61 provide a turnoff delay for the output of U19. This compensates for the inherently longer turn-on delay of U19, thus providing a symmetrical square wave to the next stage.

#### *Bidirectional One-Shot System Circuits*

The output of the comparator at pin 7 is connected into the input of dual one-shot U17. These elements are such that each produces a pulse of fixed width whose leading edge corresponds to the positive and negative edges respectively of the input waveform. Resistor R48 and capacitor C29 control one-shot U17-13 pulse width, while resistor R49 and capacitor C30 perform that function for U17-5. These two signals are ORed together in the controller interface. The bidirectional one-shots are reset by U6-8. If the unit is not selected, SEL/ is high, causing U6-8 to go low, resetting U17. Similarly if the unit is in the write mode, WBSY is also high, causing U17 to reset. This logic prevents noise signals from being transmitted to the interface circuits whenever the unit is in the write mode, or the drive is not selected.

#### **3.10.6 Write Circuits (Ref. Sheet 4 of Dwg 100061)**

These circuits consist of a power supply enable (PSEN) circuit, write current control logic, write current drivers, an erase current driver, and the read/write switch. Figure 3-19 illustrates the functional components of this circuit.

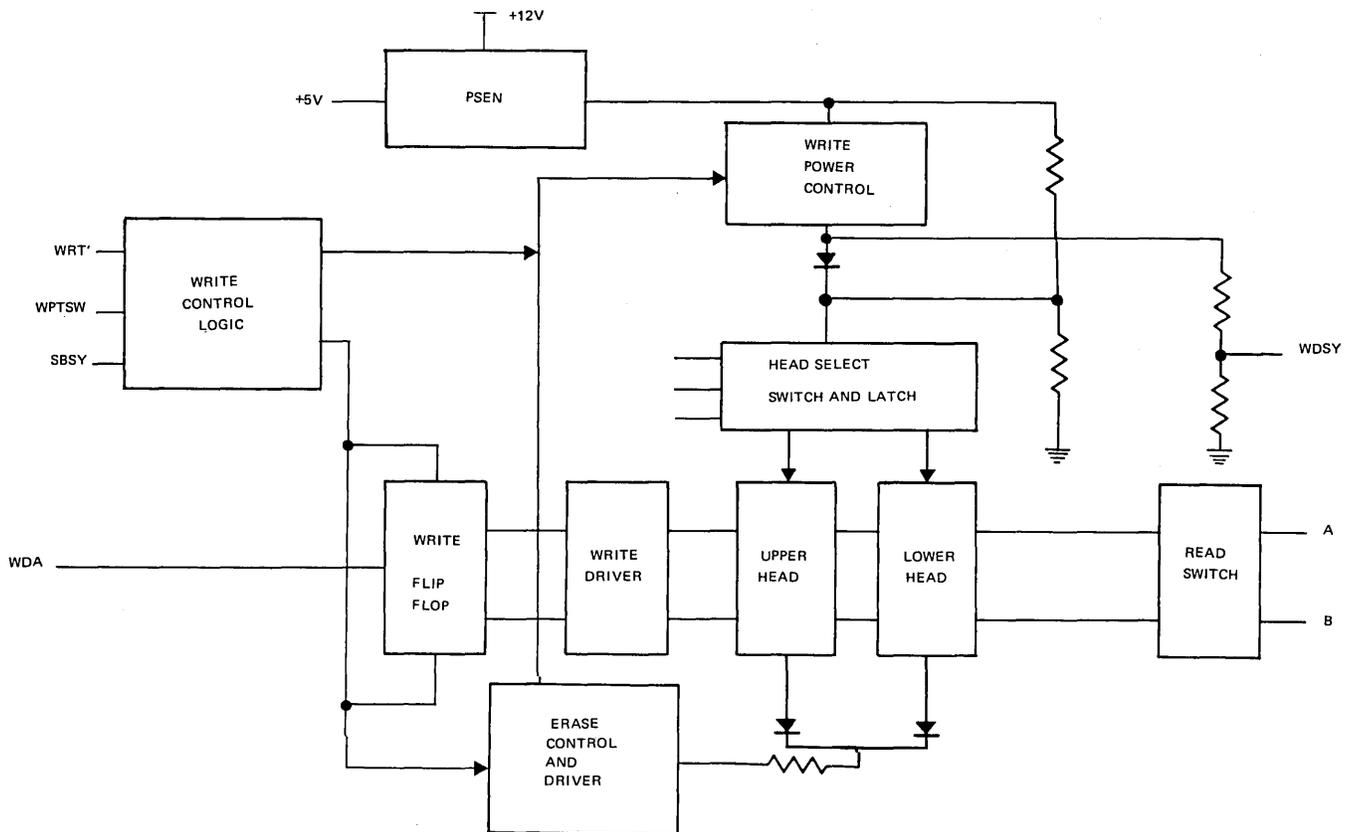


Figure 3-19. Dual Drive Write Circuits, Block Diagram

### Power Supply Enable (PSEN) Circuits

The power supply enable circuits (PSEN) allow the write current to flow only when the power supply voltages (+5V and +12V) are within operational tolerances. This prevents writing on the diskette during power-up or power-down sequences of the disk drive, or accidental power loss to the unit. The PSEN circuit consists of transistors Q1, Q2, and associated components. Initially, as +5V power rises to operational level, transistor Q2 conducts as soon as base voltage exceeds zener CR1 voltage plus the emitter-base drop of Q2, or about 3.4 volts. When Q2 collector current is sufficient to drop 0.7 volt across R16, transistor Q1 conducts providing +12 volts to the remaining circuits if the +12V power is present. At the same time, voltage divider R39, R40 generates a high power-on indicator, PSEN. The +12 volts is also divided by R35 and R36, producing approximately +6 volts, which is used in the input clamp of the read circuits. This voltage also feeds the center

tap of the read/write heads via select transistors Q4 and Q5 providing the correct bias for U16 in the read mode.

### Write Control Logic

The write control logic controls the write operation to the selected drive. When the dual drive system has been selected (SEL/ low) and a write command is received (WRT/ low) with the write protect switch off (WPT low), U6-6 goes high, enabling a low at U4-8, provided that a step command is not in progress (SBSY/high). The output of U4-8 is coupled to the base of Q3 through an inverting gate U4-11 and a driver U15-6, causing the write busy (WBSY) signal to be generated. The low at U4-8 releases the set and clear direct inputs on U11-9, enabling this flip-flop to respond to the write data (WDA) pulses from the interfaces (with the set and clear both low — both outputs pins 8 and 9 were both high).

### *Write Current Driver*

When the write control logic removes the set and clear direct control on write flip-flop U11, write data (WDA) pulses from the interface can be processed by the write current driver circuit. The flip-flop is connected so that each time a write pulse occurs, the flip-flop toggles on the trailing edge of that pulse. The complementary outputs of U11 are coupled by power drivers into the read/write head through R25 and R26. As the flip-flop toggles, power drivers U13-8 and U13-12 are energized sequentially, thus alternately driving a current through both halves of the selected read/write head. Diodes CR4 and CR5 are used to isolate the write circuits from the head during the read operation, to increase noise immunity. Resistors R21, R22 ensure that CR4 and CR5 are back biased when the write operation is concluded and also provide damping.

### *Erase Current Driver*

Resistors R18, R19, diode CR2, capacitor C14, and U14 combine the functions of an erase current driver with a delay generator that generates two different delays from the leading edge and the trailing edge of the input waveform. This causes the erase current to be switched on approximately 400 usec after the write control signal has been activated, and off 800 usec after the control signal is removed. When the circuits are not in the write mode, U13-6 is low and the output of erase drive U14 is high. When a write operation is initiated, U13-6 goes high, and driver U14 output now does not follow the change of state until delay network R19, C14 times out (approximately 400 usec). At this time, U14 senses the high stage of U13-6 and U14-3 goes low. This condition causes the erase current to flow from the center tap of the head through the erase wiring and diode CR8 or CR12, depending on which of the two drives has been selected. This current is defined by the values of R27 and R28.

### *Read Write Switch Circuits*

The read write switch consists of diodes CR13 through CR18, resistors R37, R38, R43, and R44. The function of this switch is to isolate the read circuit from the voltage excursions which occur when a write operation is in effect, and to allow the read cir-

cuits to access the head when the read mode is selected.

When the write command occurs and Q3 conducts, the anodes of CR15, CR16 go to about 11.5 volts. Thus, the cathode junctions of CR13 through CR18 are at about 11 volts. Since the anodes of CR17 and CR18 cannot rise above the 6.7 volt clamp in the read circuits (reference the read circuits description), the read circuits are effectively isolated from the read/write head. When the read mode is selected, Q3 is cut off since the WRT/ signal at U6-5 is high. This condition forces WBSY low, and allows the +6 volts developed by R35, R36 dividers access to the read/write head. Also, as transistor Q3 is cut off, diodes CR15, CR16 are back-biased and cease to conduct. Under these conditions, the circuit stabilizes with CR14 and CR15 cut off and diodes CR13, CR14, CR17, and CR18 conducting. The anodes of CR13 and CR14 are at approximately +6V since they are connected via the appropriate head select diodes and transistor to V2.

Approximately 0.25 mA is supplied through resistors R43, R44 and diodes CR17 and CR18. About 0.5 mA is drawn through R37 and R38. Thus each of the four diodes have approximately 0.25 mA flowing through them. In this way the diode bridge provides a low impedance path for the head signal to differentiator U16.

### *Head Selection Circuit*

The head select circuit consists of transistors Q4 and Q5, for drive B and drive A read/write heads, respectively, plus logic for head selection. When a drive selection signal (SELA or SELB) occurs and write busy is false (WBSY/high), the selection command is latched by U7-8, U7-11. This causes either Q6 or Q4 to turn on, depending on whether drive A or drive B was selected, raising the center tape voltage of the corresponding read/write head to about 11 volts, or 6 volts as required for write and read operations respectively.

A latch is used to prevent a change of drive select command from switching heads until the completion of the erase cycle of the previous operation.

### 3.11 FLOPPY DISK CONTROLLER PCBA FUNCTIONAL DESCRIPTION

The controller (Figure 3-20) is implemented on a 5-by-10 inch PCBA that plugs into the S100 bus. The controller contains the following major functional units:

- Control logic to interpret CPU selection and respond to CPU commands
- A sector separator and counter to separate sector and index pulses and to keep track of each sector as it passes under the read/write head
- Write logic to convert parallel-form bytes from the CPU to serial data suitable for recording on the disk

- Read logic to convert the serial data from the disk to parallel-form bytes for transfer to the CPU
- Bootstrap proms for reading sector zero of the system disk into RAM, then starting the program in RAM.

#### 3.11.1 Disk Data Format

Data is recorded on the disk in concentric tracks. The outermost track is track zero. Each track is divided into 16 sectors. The beginning of each sector is indicated by a sector hole punched in the disk. An index hole is located halfway between the holes for sector 15 and sector 0. The sector and index holes are sensed by a photo transistor in the disk drive.

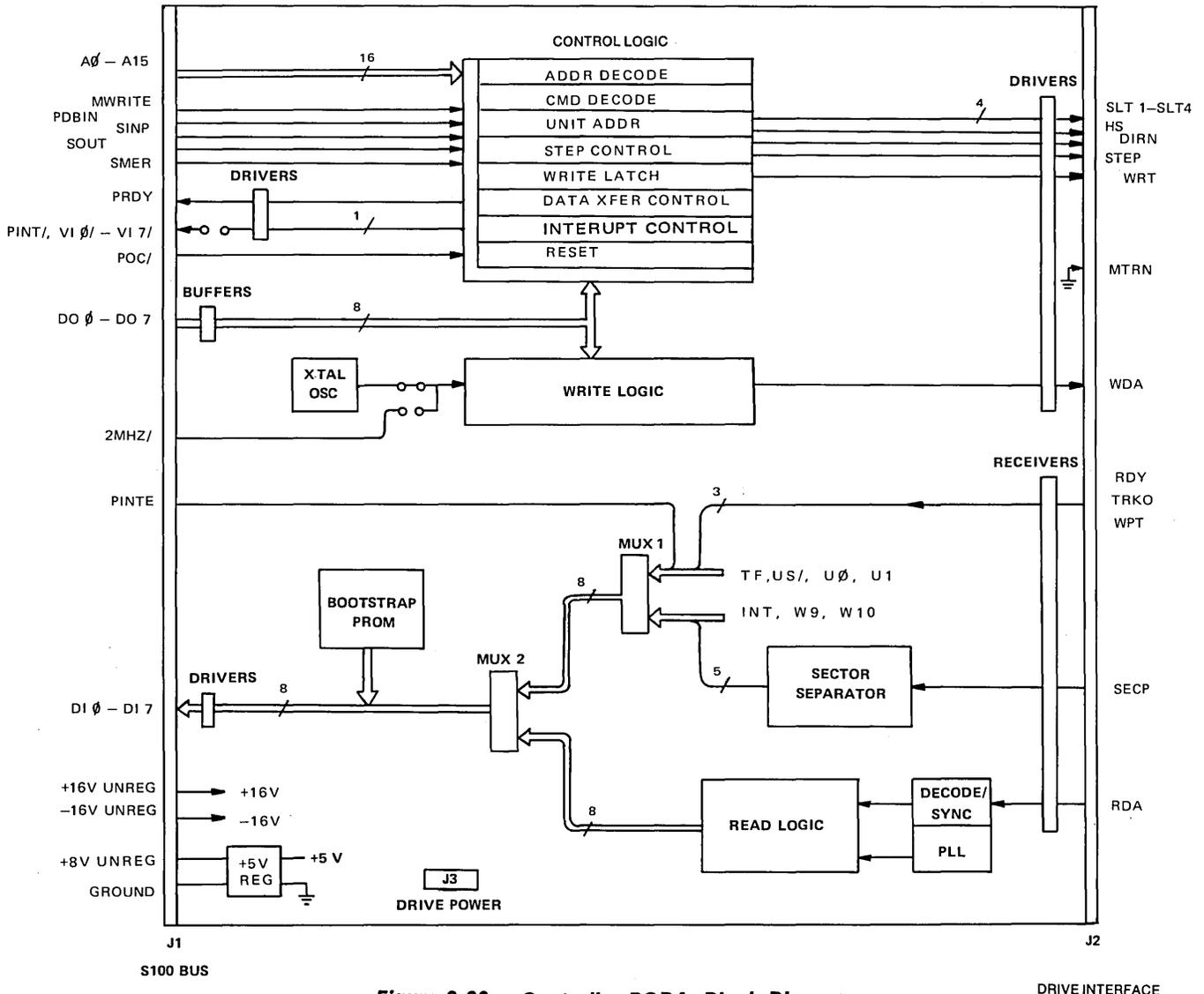


Figure 3-20. Controller PCBA, Block Diagram

DRIVE INTERFACE

Each disk sector consists of a preamble, sync byte, header, data, a checksum, and a postamble. Each of these fields are described below.

**Preamble**

The preamble is composed of approximately 40 bytes of zero (0) data bits. The preamble is automatically generated by the disk controller and is necessary to provide tolerance for the mechanical alignment and electrical characteristics of the sector/index sensor. It also provides a field of known data pattern for synchronization of the read data decoder.

**Sync Byte**

The sync byte is a byte of FFH data which is used in the disk controller to define the beginning of useful data.

**Header**

The header is a 2-byte block consisting of the binary track address of the track on which the sector resides (0-76 (34)) and the address of the sector (0-15). The header is used to verify that the proper sector is being accessed in a disk I/O operation.

**Data**

The data field consists of 266 bytes of user data.

**Checksum**

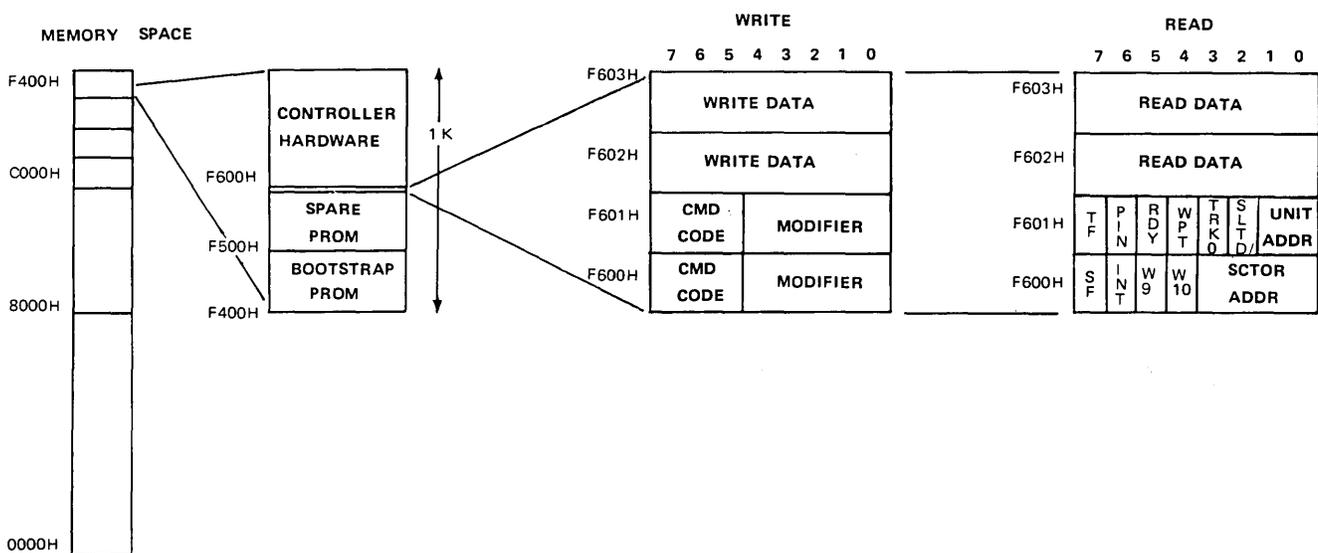
The checksum is a one byte error detection code which provides error detection in read operations. The checksum is computed by the CPU as follows: a) the accumulator and carry are initially cleared; b) each byte of the header and data fields is added to the accumulator with carry. In write operations, the computed checksum is written immediately following the data field. In read operations, the checksum is recomputed from the read data and is compared with the checksum byte which is read. If they do not compare, a read error has occurred.

**Postamble**

The rest of a sector from the checksum to the next sector hole is filled with zero data bits. The length of the postamble allows for the mechanical tolerance in the placement of sector holes on the disk and tolerance for disk speed and write clock variations.

**3.11.2 Controller Registers**

The controller is accessed using the *memory-mapped I/O* technique; that is, the controller command, status, and data registers are treated as memory addresses, so that the controller read/write commands are actually memory reference instructions. See Figure 3-21 for a pictorial illustration of the controller registers and the standard address configuration.



**Figure 3-21. Controller Registers and Addressing**

**TABLE 3-2. COMMAND REGISTER FORMAT**

Command Code (bits 7,6,5)	Command	Modifier (bits 0-4)
0	—	—
1	Select Drive/Head	(Bits 0,1: Select drive unit address (0-3) (Bit 4: Select head: 0=lower; 1=upper)
2	Interrupt Control	(Bit 0: =0 Disable Sector Interrupt =1 Enable Sector Interrupt)
3	Step 1 track	(Bit 0: =0 Step Out (decrease track number) =1 Step In (increase track number)
4	Set WRITE	Not used
5	Reset Controller	Not used
6	Not used	Not used
7	Not used	Not used

One kilobyte of the CPU's memory space is allocated for use by the controller. The upper 512 bytes are reserved for operating the controller, and the lower 512 bytes are allocated for the bootstrap PROMs. Because only half of the available PROM is used, only half of the lower space is used. The controller hardware registers occupy the first four locations of the upper 512 bytes; and the remainder of this address space duplicates these four addresses, over and over.

Jumpers W1 through W4 (ref. Sheet 2 of Dwg 100-087) allow the controller to be located at any one of the upper 16 1K blocks of CPU memory space (base addresses C000 through FC00). The controller is normally configured with only jumper W3 installed, selecting the memory block starting at F400, as shown in Figure 3-21. The controller command, status, and data registers are also indicated in this figure, and are accessed by the appropriate CPU memory read and write commands.

**Command Register**

The command register, located at F600 or F601 for CPU memory write operations, provides for drive unit/head selection, interrupt control, write enable, track-to-track stepping, and controller reset. The CPU sets the command code in bits 7, 6, 5 and sets the modifier in bits 0 through 4. Bit specifications for the command register are shown in Table 3-2.

**Sector Register**

The sector register, located at F600 for CPU memory read operations, contains the address of the sector currently passing under the read/write head, and contains the sector flag and sector interrupt flag as they occur. The sector register forms controller status byte zero. Bit specifications for the sector register are shown in Table 3-3.

**TABLE 3-3. SECTOR REGISTER FORMAT**

Bits	Definition
0-3	<b>Sector Address:</b> Address of the sector passing under the read/write head of the selected drive.
4	<b>Reserved:</b> Jumper W10
5	<b>Host CPU Speed:</b> Jumper W9 is installed according to host CPU speed as follows: 1 = 2 MHz CPU (W9 not installed) 0 = 4 MHz CPU (W9 installed)
6	<b>Sector Interrupt Flag:</b> Indicates an interrupt request has been generated by a sector pulse. Flag is reset by issuing a reset or an interrupt disable command. (Not used by Micropolis software.)
7	<b>Sector Flag:</b> Indicates the sector address is valid and that a read or write operation may be performed. Flag is true for 30 usec at the start of each sector. All data transfers must be initiated within 100 usec of the flag going true.

### Status Register

The status register, located at F601 for CPU memory read operations, contains drive select and status bits, CPU interrupt status, and a flag which enables the CPU to synchronize disk read and write operations. The status register forms controller status byte one. Bit specifications for the status register are shown in Table 3-4.

### Write Data Register

The write data register, located at F602/F603 for a CPU memory write operation, enables the CPU to write data on the disk. If the write data register is referenced when the transfer flag is set during a write operation, the controller expects a data byte to be on the S100 bus data lines. The PRDY line will be held false until the controller has accepted the data, then the PRDY line will be set true for 1 bit time (4 usec). (See the status register description for the definition of the transfer flag.)

### Read Data Register

The read data register, located at F602/F603 for a CPU memory read operation, enables the CPU to read disk data after it has been assembled into parallel form by the controller. If the read data

register is accessed when the transfer flag is set during a read operation, the controller will hold the PRDY line false until a byte of data is available. The controller will then place the data on the S100 bus data lines and set PRDY true for 1 bit time (4 usec). The data will only be available for this 1 bit time period.

### 3.11.3 S-100 Signals Definition

Pin assignments and identification of S-100 bus signals used by the controller are shown in Table 3-5. Bus timing for handshaking and data transfer are shown in Figure 3-22.

### 3.11.4 Control Logic

The control logic interprets the selection of the controller by the CPU (address decode), decodes the command byte to determine the selected drive unit and to execute CPU commands, controls data transfer between the drives and the CPU, and generates CPU interrupt signals corresponding to sector pulses.

*Address Decode* (Ref. Sheet 2 of Dwg 100087)

The address decode consists of decoder D8 and its associated NAND gate and inverters. It monitors the

**TABLE 3-4. STATUS REGISTER FORMAT**

Bits	Definition
0-1	<i>Unit Address</i> : Address of the currently selected drive. Address is valid only if SLTD/ is true (0).
2	<i>SLTD/</i> : Unit selected. This flag is low true, i.e., 0 = A drive is selected. 1 = No drive is selected.  SLTD/ is true if a drive has been selected and the 4-second timer has not expired. SLTD/ is low true so that the software may detect when the controller is not installed (non-existent memory references yield 0FFH).
3	<i>TK0</i> : Track 0 status from selected drive.
4	<i>WPT</i> : Write protected status from selected drive.
5	<i>RDY</i> : Ready status from the selected drive. When true, indicates the drive is ready to perform commands.
6	<i>PINTE</i> : PINTE status from the S100 BUS.
7	<i>TF</i> : Transfer flag. In write operations, indicates that the controller is ready to accept data from the computer. In read operations, indicates the controller has data available to the computer. When the software detects the transfer flag has set, all data transfers are performed by accessing the controller data register, which automatically synchronizes the transfer by use of the PRDY line.

**TABLE 3-5. DISK CONTROLLER S-100 BUS INTERFACE**

Signal	Pin	Dirn	Description	Signal	Pin	Dirn	Description	Note		
A00	79	IN	Address Bus	SINP	46	IN	I/O Input Cycle			
A01	80			SOUT	45	IN	I/O Output Cycle			
A02	81			SMEMR	47	IN	MEM Read Cycle			
A03	31			MWRITE	68	IN	MEM Write Strobe			
A04	30			PDBIN	78	IN	CPU Data In Strobe			
A05	29			PRDY	72	OUT	CPU Ready Line			
A06	82			POC/	99	IN	Poweron Clear			
A07	83									
A08	84					2MHZ/	49	IN	2.0 MHz Xtal Clock	4
A09	34									
A10	37					PINTE	28	IN	CPU INTE Line	5
A11	87					PINT/	73	OUT	CPU INT Line	5
A12	33									
A13	85					V10/	4	OUT	Vectored Interrupt Lines	5
A14	86					V11/	5			5
A15	32			V12/	6	5				
				V13/	7	5				
				V14/	8	5				
				V15/	9	5				
				V16/	10	5				
D00	36	IN	Data Out Bus	V17/	11		5			
D01	35									
D02	88					GND	50	IN	Ground	
D03	89					GND	100	IN	Ground	
D04	38									
D05	39					+8V	1	IN	+8V Unreg	
D06	40					+8V	51	IN	+8V Unreg	
D07	90									
DI0	95	OUT	Data In Bus	+16V	2	IN	+16V Unreg	6		
DI1	94					-16V	52		IN	-16V Unreg
DI2	41									
DI3	42									
DI4	91									
DI5	92									
DI6	93									
DI7	43									

**NOTES:**

1. Slash (/) at end of signal name indicates Low True polarity.
2. All signal lines at TTL levels. Input lines require 1.0 mA max drive current. Output lines driven by 74367 (32 mA sink).
3. Signal lines with notes are optional and are not used in the standard Micropolis controller configuration.
4. Jumper option selects 2 MHz bus clock for write circuits instead of internal oscillator.
5. Jumper option generates interrupt on PINT/ or V10/ thru V17/ on occurrence of each sector pulse. PINTE indicates current CPU interrupt status.
6. +16V power for optional disk drive power connector.

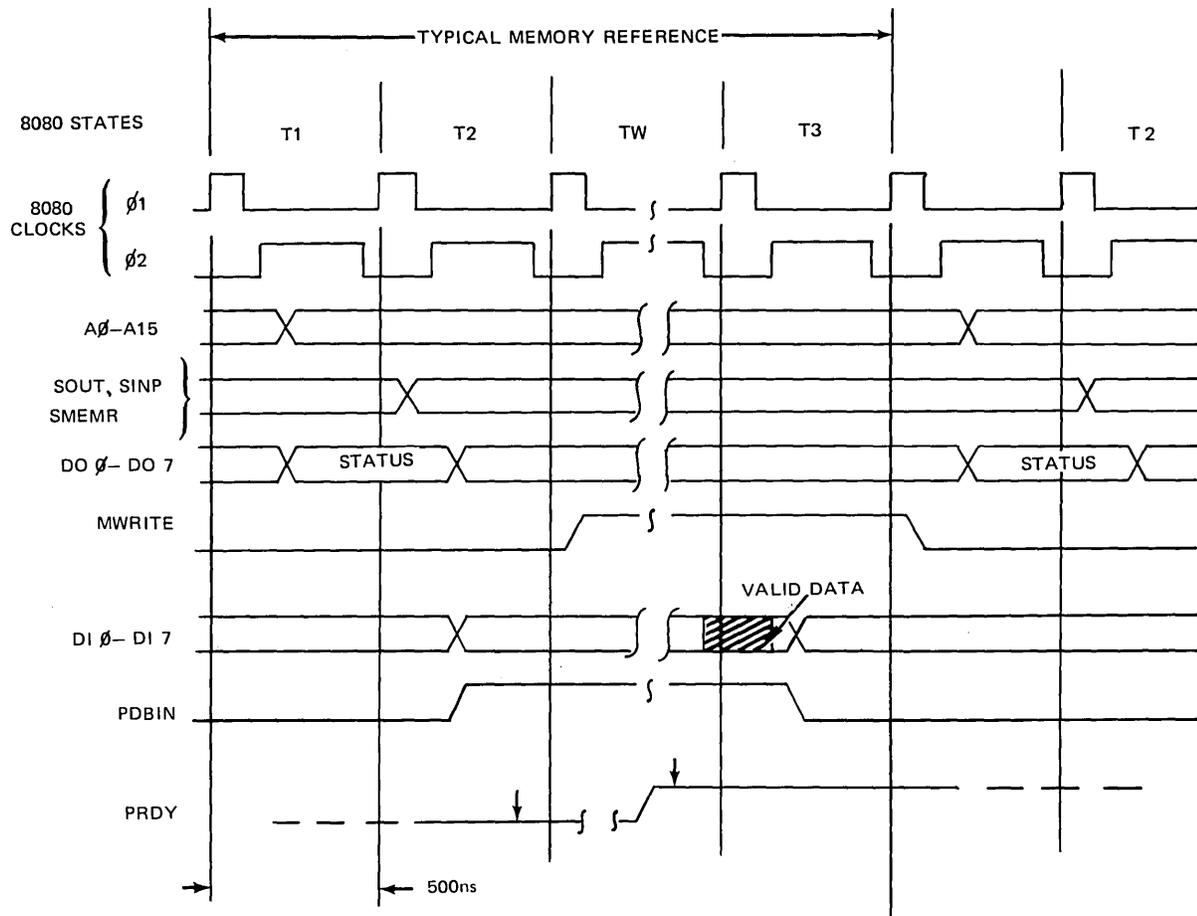


Figure 3-22. S100 Data Bus Signals, Timing Diagram

address lines from the CPU to interpret selection of the controller.

Whenever an address is within the 1K block assigned to the controller A10 through A15 will equal the logic address selected by W1-W4 and D8-9 will go low, and will be inverted by C7-8 to form BSEL (board select). Also the low at D8-9 will be gated at D6-10, with the inverse of A9, to form CSEL (controller select). CSEL is inverted by C7-4 to form CSEL/, and also is gated with A1 to form DSEL (data select). When CSEL and MWRITE (memory write) are high and A1 is low, C8-6 goes low to form CMD/ (command decode).

**Command Decode** (Ref. Sheet 7 of Dwg 100087)

Commands from the processor such as controller reset and STEP positioner are decoded by decoder D3, which examines the command modifier bits from the CPU and generates the controller command codes. D3 examines CMD/ and data bits D5, D6, D7, and generates one of five commands: ADRC/ (ad-

dress command for selected drive), INTC/ (interrupt command), STEPC/ (step command), WRTC/ (write command), and RSTC/ (reset command).

**Unit Address Control** (Ref. Sheet 8 of Dwg 100087)

The unit address control consists of register B3 and its associated NOR gates and line drivers. It examines data lines from the CPU, stores the selected drive and head addresses, and generates drive and head select signals for the drive interface.

When RST/ (reset) is high and a drive unit select command is executed to form ADRC/, B3 is clocked, and stores the contents of D0, D1 (drive address) and D4 (head address). Simultaneously, B3-10 is clocked causing US (unit select) to set. B4 decodes U0 and U1 into four drive select signals which are then gated with US by interface drivers B5. US remains set until it is cleared by a low RST/ as the result of a four-second timeout or an RSTC/ command. For a double-sided drive B3-15 selects either the lower (0) or the upper (1) head.

**Step Control (Ref. Sheet 8 of Dwg 100087)**

Step control is accomplished by flip-flop B2 and its associated inverter C7-2, and line drivers B6-6 and -12. Figure 3-23 shows the circuit timing. When a step command is issued, STEP/ goes low for approximately one-half microsecond; it is inverted by C7-2 and drives the step line via B6-12. B2-9 is clocked by the rising (leading) edge and copies the state of D0, which will be high for a step in command and low for a step out command. The output at B2-9 drives the DIRN (direction) line via B6-6. Consecutive, same-direction step pulses must be separated by 30 milliseconds; opposite-direction pulses, by 40 milliseconds for correct drive operation.

**Write Latch (Ref. Sheet 7 of Dwg 100087)**

The write latch logic consists of flip-flop B2-5 and its reset logic. When a write command is issued, WRTC/ goes low and the rising (trailing) edge sets flip-flop B2-5. The WRT (write enable) output at B2-5 enables the controller write circuits and asserts the WRT interface line via B6-8 (ref. Sheet 8 of Dwg 100087). Writing occurs in the selected drive when WRT is true. B2-5 is normally reset by SP/ (sector pulse) going low at the end of the sector; it will also be reset if RST/ is low or RDY (drive ready) is not present.

**Reset Circuits (Ref. Sheet 7 of Dwg 100087)**

The reset circuit generates RST/, the general reset signal for the controller. The circuit consists of a four-second one-shot D1-5 and associated logic.

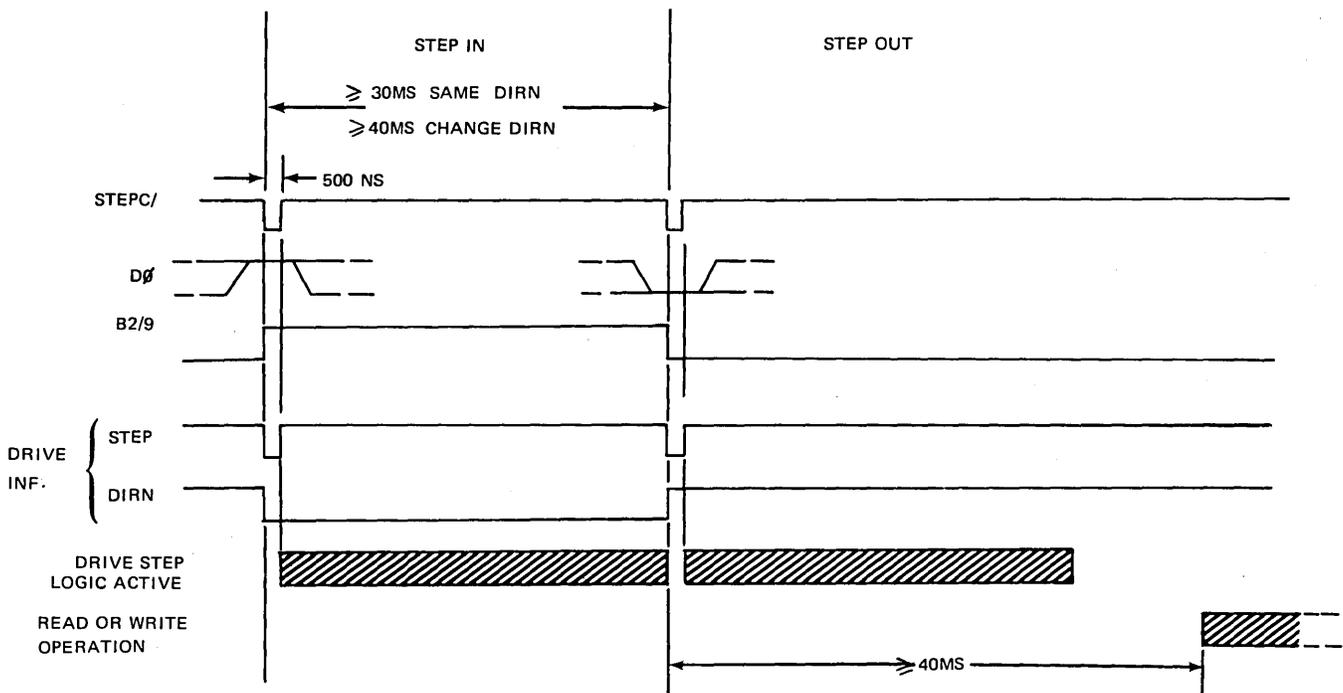
D1-5 is a retriggerable one-shot which is triggered by DIG/ each time the CPU reads from the controller status or data registers. This occurs many times a second when the controller is in use causing D1-5 to remain high. If there is no disk activity for a period of four seconds, D1-5 goes low causing a low on RST/. Other inputs to RST/ are RSTC/ (reset command) and POC (S100 power-on clear).

**Data Transfer Control (Ref. Sheet 6 of Dwg 100087)**

This logic generates three signals associated with the control and synchronization of data transfers between the controller and CPU. Waveforms are shown in Figure 3-24.

**TF: Transfer Flag**

This flag goes true one byte-time before the first (sync) byte is to be transferred to/from the controller. It is formed by gates D6-1 and D6-13 by OR'ing together WF (write flag) from the write logic and RF (read flag) from the read logic. TF is sensed by the CPU by reading Status Byte 1.



**Figure 3-23. Step Control Signals, Timing Diagram**

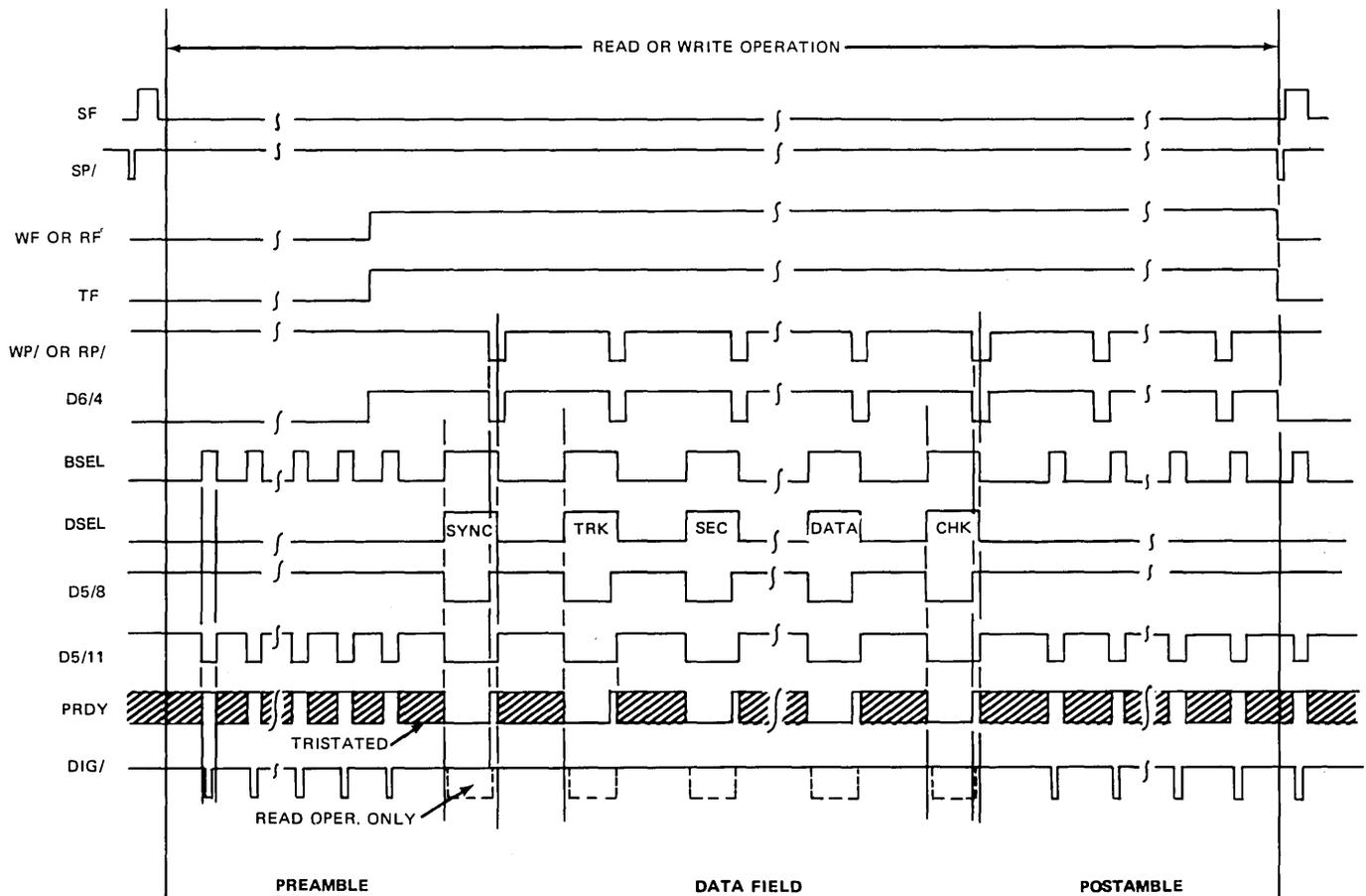


Figure 3-24. Data Transfer Control Signals, Timing Diagram

**PRDY: Processor Ready**

This line connects to the CPU ready input. When PRDY is low, the CPU executes continuous WAIT states, freezing program execution in the middle of the current machine cycle. The address and data out lines remain valid during this time. This facility is used to synchronize the transfer of disk read or write data between the CPU and controller.

The tri-state PRDY gate (D9-13) is enabled by NAND D5-11, and when enabled, gates the output of D5-8 onto the PRDY line. PRDY is enabled when the controller is being accessed (BSEL high) during a memory reference instruction (SINP and SOUT both low).

D5-8 is normally high except when the Read or Write data register is being accessed (DSEL high), TF is high (data area of the sector), and WP/ and RP/ are both high (controller not ready to accept a byte of

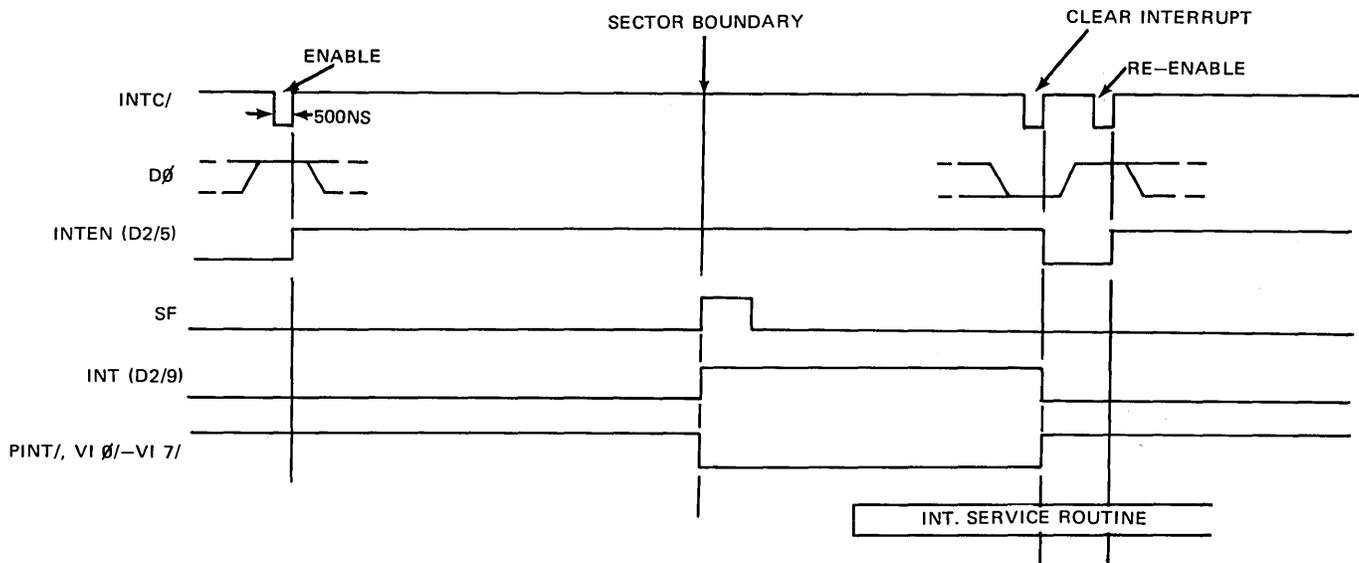
write data, or has not assembled a complete byte of read data). When the controller is ready for the transfer, WP/ or RP/ goes low for one bit-time allowing the software loop to proceed.

**DIG/: Data In Gate**

This signal gates controller status, read data, or PROM information onto the S100 bus data in lines, DI0 through DI7 (see Sheet 5 of schematic). DIG/ (C8-8) goes low when the controller is addressed (BSEL high) during memory read instructions (SMEMR and PDBIN both high).

**Interrupt Control** (Ref. Sheet 7 of Dwg 100087)

When enabled, the interrupt control logic generates an interrupt as the sector flag (SF) goes high at each sector boundary. Figure 3-25 illustrates the timing of this circuit. The interrupt may be jumpered to PINT/ (processor interrupt) or one of the vectored interrupt



NOTE: INTERRUPTS ARE NOT USED WITH MICROPOLIS SOFTWARE

Figure 3-25. Interrupt Signals, Timing Diagram

lines VI0/ through VI7/. The logic consists of interrupt enable flip-flop D2-5, interrupt flip-flop D2-9, and line driver D10-13.

When an Interrupt Control command is issued, D2-5 is either set or reset depending on the state of the modifier bit, D0. When set, interrupts are enabled allowing D2-9 (INT) to set at the following sector boundary (rising edge of SF). The resulting low at D10-13 drives the desired S100 interrupt line by means of a jumper connection. The interrupt is cleared by the interrupt service routine by issuing another Interrupt Control command with D0 = 0.

The interrupt logic is initially cleared by RST/ low.

### 3.11.5 Sector Separator (Ref. Sheet 6 of Dwg 100087)

The sector separator uses SECP (the drive sector hole photosense output received at B7-4) to generate the sector timing signals ROS (read one-shot) and its complement ROS/, WOS/ (write one-shot), SF (sector flag), SP/ (sector pulse), and S0 through S3 (sector count signals). It consists of one-shots C2, C1, and D1-13, and four-bit counter C3. Figure 3-26 illustrates the timing of this circuit.

ROS is generated as follows: one-shot C2-13 shapes the leading edge of SECP into a one-microsecond pulse which is used by one-shot C2-5 to form a pulse of approximately three-quarters of a sector period;

the pulse bridges the time during which the index pulse occurs. The pulse at C2-5 triggers one-shot C1-13, which forms a 700 microsecond ROS period to provide time for PLL and read logic-decode circuits to synchronize before a sector is read. C2-5 also triggers one-shot C1-5 which generates a 1200 us time period during which the preamble is written for write commands.

SF is a 30-microsecond pulse formed when one-shot D1-13 is triggered by the leading edge of the C2-5 pulse; the high formed at D1-13 is delayed through AND gate C6-3 by RC network C7 and R13 to form SF. This delay (approximately 200 ns) ensures that the sector counter is stable at the new sector address when the CPU senses SF true.

SP/ consists of a one-microsecond low-true pulse for each of the 16 sector holes in the diskette. Each pulse defines the end of one sector and the beginning of the next. No pulse is generated for the index hole. It is formed by gating C2-13 with C2-12.

S0 through S3 are the outputs of a 4-bit counter, C3, which is incremented at each sector boundary. These lines indicate the binary address (0-15) of the sector currently under the read/write head. The counter is synchronized with index by loading a count of 15 when the index hole is sensed. SF and S0 through S3 are sampled simultaneously by the CPU by reading Status Byte 0.

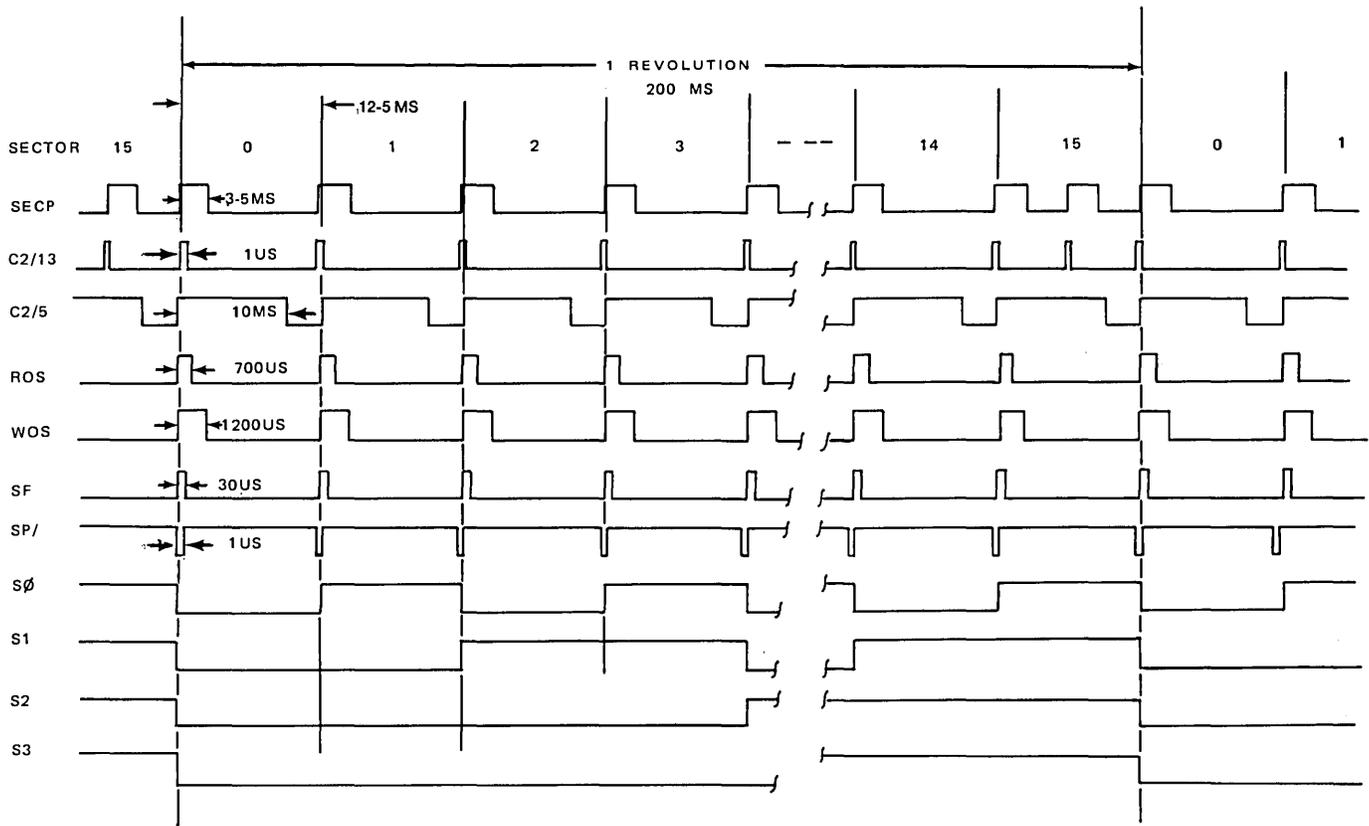


Figure 3-26. Sector Separation Signals, Timing Diagram

### 3.11.6 Write Circuits (Ref. Sheet 3 of Dwg 100087)

The write circuits accept parallel data bytes, DO0 through DO7, from the CPU via D9 and D10. The data is serialized, then encoded into MFM form to generate WDA (write data). This signal is routed to the selected drive via B6-10 (ref. Sheet 8 of Dwg 100087). This logic consists of the write bit and byte counters, shift register, encoding and pulse shaping circuits.

The write logic is normally configured for MFM encoding; double frequency encoding can be used in place of MFM if jumpers W6 and W7 are removed and jumpers W5 and W8 installed. The Micropolis software is configured for MFM operation only. Figures 3-27 and 3-28 provide timing information on the write circuits.

Write timing is derived from a 2 megahertz OSC/ (oscillator) signal from a crystal oscillator (ref. Sheet 7 of Dwg 100087). An alternate 2 megahertz signal may be obtained from the S100 data bus via J1-49 if jumper W12 is installed and W11 is omitted.

The following sequence of events occurs when a sector is written onto the diskette:

- The disk I/O driver software selects the required drive and moves the positioner to the desired track using DRIVE SELECT and STEP commands to the controller.
- The driver continually reads Status Byte 0 looking for SF true with the desired sector address.
- When the desired sector is found a SET WRITE command must be issued within 70 us (i.e., within 100 us of the physical beginning of the sector). This sets the WRT flip-flop in the controller causing the preamble to be written onto the diskette.
- The driver continually reads Status Byte 1 looking for the TF (transfer flag) true. This occurs at the end of preamble when the sync byte is about to be written.

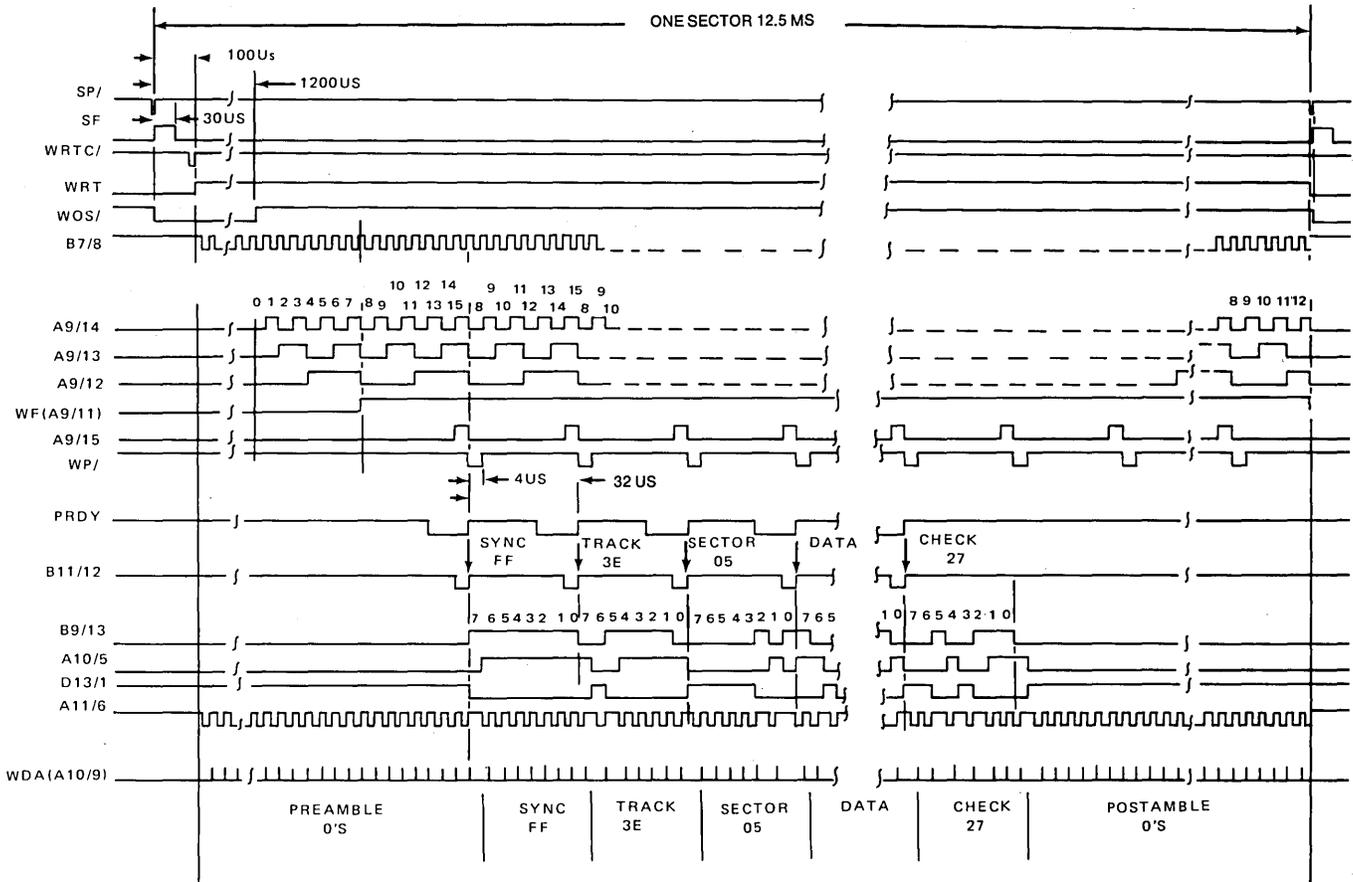


Figure 3-27. Write Logic (MFM), Timing Diagram

- e. The driver must write the sync byte pattern (FFH) to the write data register within 20 us after detecting TF true. The controller responds by pulling the PRDY line low thus holding the sync pattern on the DATA OUT lines until it is ready to accept the byte.
- f. One-byte time (32 us) after TF goes true the controller copies the sync byte into the write register and raises the PRDY line allowing execution of the software loop to proceed.
- g. During the following byte-time the sync byte is serialized, encoded, and written onto the disk. At the same time the driver accesses the following byte (cylinder address), computes a partial sum check, and writes the byte to the write data register, causing PRDY to go low again.
- h. Steps f and g are repeated for each byte of the header and data fields. The sum check byte is then written immediately after the last data byte.

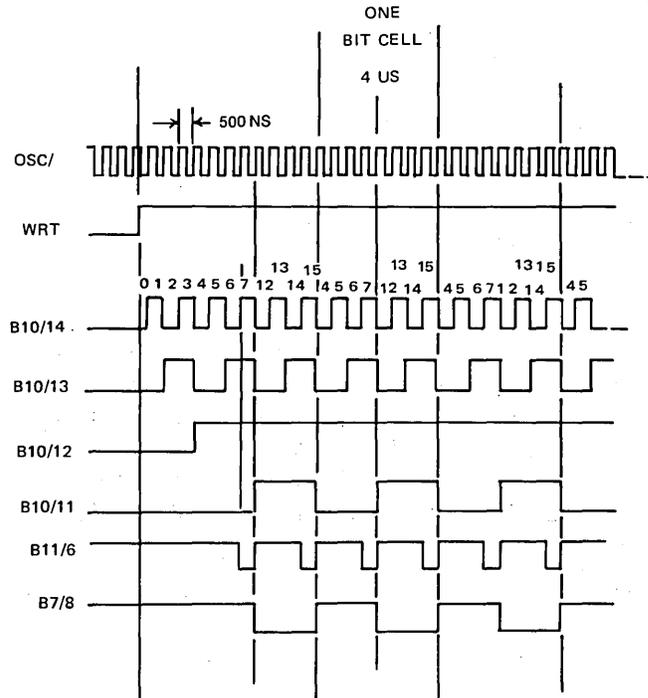


Figure 3-28. Write Clocking Logic, Timing Diagram

- i. The controller automatically fills the remainder of the sector with an all-zeroes pattern. When the following sector pulse is encountered WRT is automatically reset in the controller, ending the write operation.

#### *Write Bit Counter* (Ref. Sheet 3 of Dwg 100087)

The write bit counter consists of counter B10 and NAND gates B7-8 and B11-6.

The WRT signal from the write latch enables bit counter B10 and the remainder of the write circuits. B10 then counts the 2 megahertz OSC/ pulses and produces the waveforms shown in Figure 3-28. Output B10-11 (OSC divided by eight) consists of a square wave with a period of one bit-time (4 us). This is inverted by B7-8 and used to clock the byte counter A9, and data shift register B9. NAND gate B11-6 decodes a count of 7 or 15 in B10 causing a count of 12 or 4 respectively to be loaded into the counter. B11-6 goes low for 0.5 us at count 7 and 15.

#### *Byte Counter* (Ref. Sheet 3 of Dwg 100087)

The byte counter consists of A9, flip-flop B12-5, and inverter D14-4. The byte counter counts off consecutive groups of 8 bits which correspond to each byte of data recorded on the diskette. The signal WP/ (write pulse) goes low for one bit-time at the beginning of each byte.

Counter A9 is inhibited by WOS/ low while the preamble is being written (ref. Figure 3-23). After approximately 1200 microseconds, WOS/ goes high allowing A9 to be clocked by the rising edge of each bit time pulse from B7-8. A9 counts off consecutive bits of data until it reaches a count of 8; at that time, WF (write flag) goes high indicating that the sync byte is about to be written. A9 then continues counting until 15 is reached, at which time A9-15 (carry output) goes high causing A9 to load a count of 8, and then to continue in the sequence 8 — 15, 8 — 15, etc. Each 15 count (A9-15 high) corresponds to the last bit of a byte. This signal is delayed by B12-5 to form WP/ which goes low during the following bit time. WP/ low causes PRDY to go high for 4 us, allowing the software loop to proceed.

#### *Shift Register* (Ref. Sheet 3 of Dwg 100087)

The shift register logic consists of a parallel-to-serial register B9 and NAND gate B11-12. The shift register converts the parallel DO0 through DO7 data inputs to serial data output at pin 13, as shown in Figure 3-27.

During the last bit of each byte A9-15 high causes B11-12 to go low provided that the CPU is writing to the write register address (DSEL and MWRITE both high). This places the shift register in load mode causing the contents of DO0 through DO7 to be copied into the register on the following clock. This information is shifted right and appears at B9-13 in serial form during the following byte-time.

After the sum check has been written the software makes no further reference to the write register, and the register is not loaded. A continuous stream of zeroes entering at B9-1 is shifted through the register to form the postamble pattern.

#### *Encoding and Pulse Shaping Circuits* (Ref. Sheet 3 of Dwg 100087)

The encoding circuit consists of A10-5, D13-1, and A11-6. The pulse shaping circuit consists of D13-4 and A10-9. These circuits encode and shape the data stream from B9-13 to form WDA.

The rules for MFM (double density) and DF (single density) encoding are usually stated as follows:

*Rule 1*    *MFM and DF:* A flux transition is written in the middle of a cell if the current data bit is '1.'

*Rule 2*    *MFM:* A flux transition is recorded at the beginning of a cell if the current and preceding data bits are both '0.'

*DF:* A flux transition is recorded at the beginning of every cell.

In this implementation of the logic, Rule 2 has been modified to an equivalent form as follows:

*Rule 2A*    *MFM:* A flux transition is recorded at the end of a cell if the current and subsequent data bits are both '0.'

*DF:* A flux transition is recorded at the end of every cell.

Serial data from B9-13 is first delayed one bit-time by A10-5. This flip-flop contains the data bit currently being encoded. D13-1 and A11-6 then perform the encoding function as described above, where gate inputs A11-4/5 introduce the data transitions (Rule 1), and A11-2/3 introduce the clock transitions (Rule 2A). Output A11-6 goes low for half a bit-time for each transition to be recorded.

D13-4 and A10-9 shape this signal to form WDA which consists of a 0.5 us high-true pulse for each transition. Line driver B6-10 (Sheet 8) transmits WDA to the selected drive.

### 3.11.7 Read Circuits (Ref. Sheets 4 and 9 of Dwg 100087)

The following sequence of events takes place when a sector is read from the disk:

- a. The disk I/O driver software selects the required drive and moves the positioner to the desired track using DRIVE SELECT and STEP commands to the controller.
- b. The driver continually reads Status Byte 0 looking for SF true with the desired sector address.
- c. When the desired sector is found the driver continually reads Status Byte 1 looking for TF (transfer flag) true. This occurs one byte-time before the first (sync) byte of the sector is available for transfer to the CPU. Note that no explicit SET READ command is required since the controller is always attempting to read when it is not writing.
- d. The driver must attempt to read this byte from the read data register within 20 us after detecting TF true. The controller responds by pulling PRDY low until the byte is fully assembled.
- e. When the byte is assembled, PRDY goes high for one bit-time allowing the transfer to be completed. The driver must now process the sync byte and attempt to access the following byte (cylinder address) in less than one byte-time. This causes PRDY to go low again.
- f. Step e is repeated for each byte of the header, data, and sum check fields. The driver recomputes the sum check from the

header and data fields and compares this against the sum check read from the disk. A discrepancy indicates a disk data transfer error.

The read electronics consist of a phase-locked loop circuit (PLL), data decoder, clock synchronization circuit, serial-to-parallel converter, and control logic.

### PLL (Ref. Sheet 9 of Dwg 100087)

The purpose of the PLL is to provide a clock signal for decoding purposes which maintains a fixed phase relationship with the incoming read data signal, RDA. The PLL is a feedback system consisting of a phase comparator, a low-pass filter, error amplifier, and a voltage controlled oscillator (VCO).

A block diagram is shown in Figure 3-29. With no input signal applied the error voltage is zero and the VCO oscillates at its center frequency,  $f_o$ . When an input signal is applied, the phase comparator compares the phase and frequency of the input with the VCO output, and generates an error voltage  $V_e(t)$  that is related to the difference between the two signals. This error voltage is filtered, amplified, and routed to the control input of the VCO. Thus the control voltage,  $V_d(t)$  forces the VCO frequency to vary in a direction that reduces the frequency difference between  $f_o$  and the input signal. If the input signal,  $f_s$ , is sufficiently close to  $f_o$ , the feedback nature of the PLL causes the VCO to lock with the incoming signal. When locked, the VCO frequency is identical to the input signal, except for a small phase difference which is necessary to generate the correction signal which maintains the VCO at the input data frequency,  $f_s$ . In this way the PLL can track variations in the disk speed, generating a continuous clock having a fixed phase relationship with the incoming data, and which can be used to decode the data pattern.

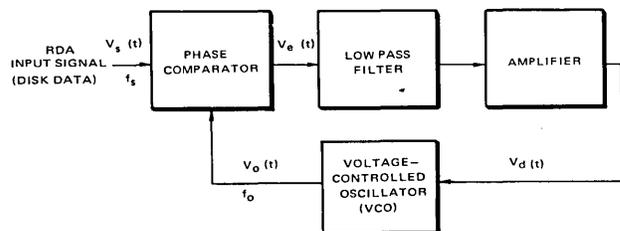
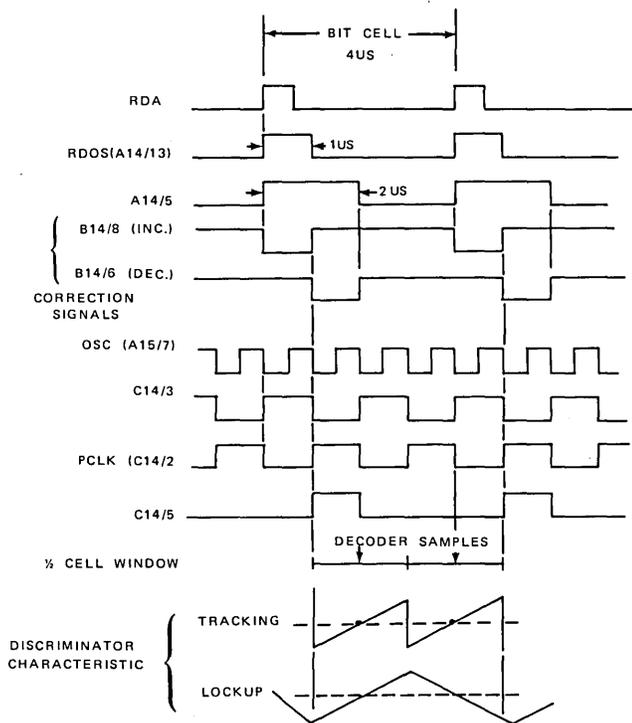


Figure 3-29. Phase-Locked Loop (PLL), Block Diagram

Figure 3-30 illustrates the timing of the PLL circuits. RDA is received at B7-10 (Sheet 8) and applied to one-shot A14-5 to produce a 2 us pulse for each flux transition read from the diskette. The one-shot output connects to a phase comparator consisting of flip-flop C14-5 and NAND gates B14-11, -8, and -6. The VCO oscillates at four times the data rate, and its output A15-7 is first divided by two by C14-3 before clocking the comparator flip-flop C14-5. Jumpers W14 and W16 are installed for MFM operation or W13 and W15 are installed for DF operation. The PLL timing diagram for MFM is shown in Figure 3-30.



**Figure 3-30. PLL Circuits (MFM), Timing Diagram**

Correction signals generated by B14-8 and B14-6 are applied to a balanced low pass filter formed by R30, R32, and C17 on one leg, and R31, R33, and C18 on the other leg. The filter output is amplified by differential amplifier B15, which in turn drives the control input to the VCO. The center frequency is adjusted by potentiometer R40, and should be set for 1.0 MHz for MFM (0.5 MHz for DF) with no data input.

Another one-shot, A14-5 (RDOS), delays the leading edge of each RDA pulse by 1.0 us before input to the read decoding logic (Sheet 4). When the PLL is locked, the falling edge of each PCLK pulse occurs

at the center of the decoder half-cell "windows," i.e., midway between the times at which potential flux transitions occur. One-shot A14-5 is adjustable allowing PCLK to be moved with respect to the decoding window. This provides a means of optimizing the window adjustment, and of measuring the read performance of the drive in terms of the error-free range of adjustment. The delay should be set to 1.0 us for normal operation.

**Read Data Decoder (Sheet 4 of Dwg 100087)**

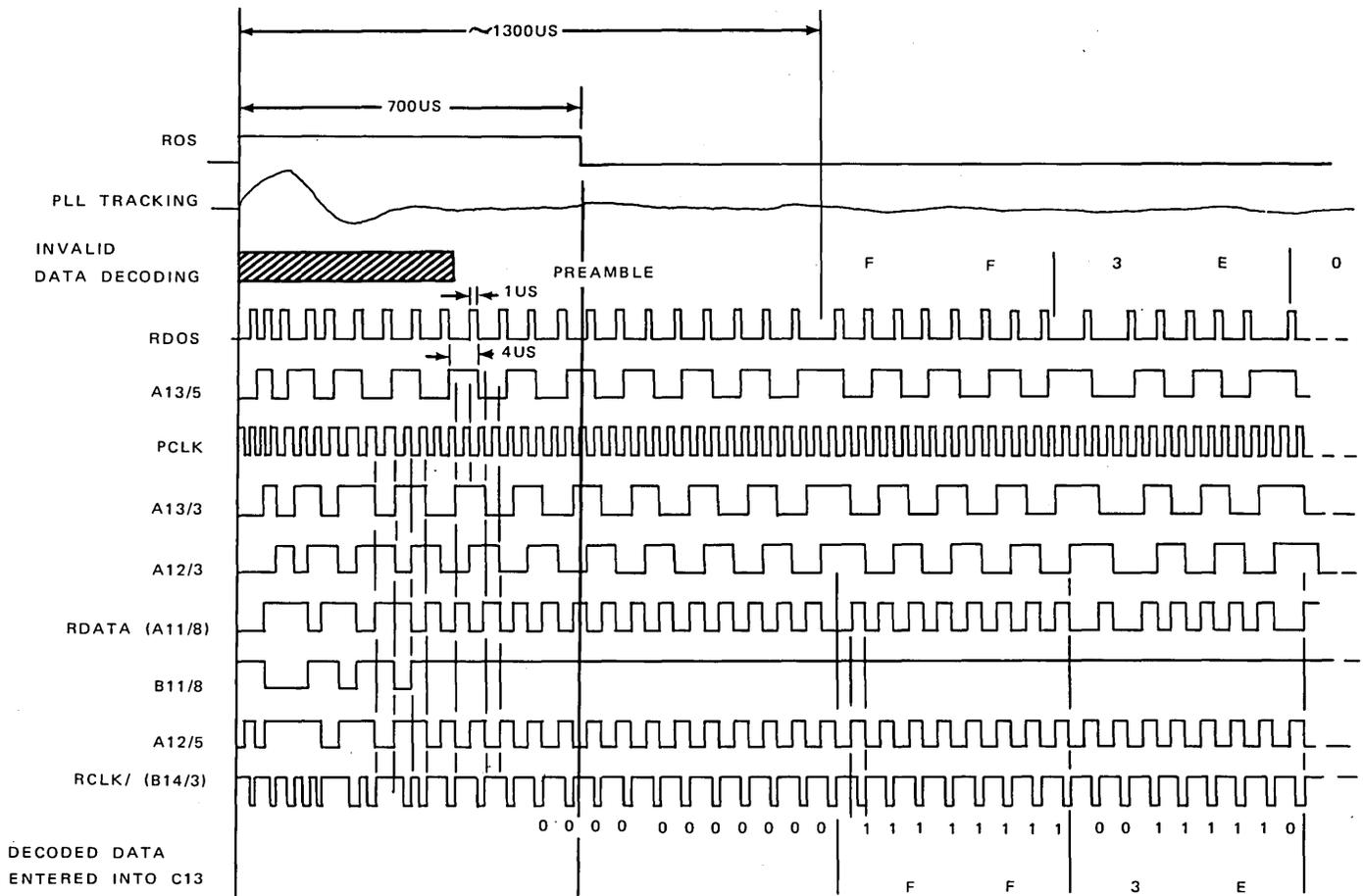
The decoder consists of flip-flops A13-5, A13-3, A12-3, and AND/OR inverter A11-8. Using the inputs RDOS and PCLK from the PLL, this circuit decodes the read data and generates a high output for half a cell-time on RDATA for each flux transition read from the disk. Timing for the read data decode circuits is shown in Figure 3-28.

The falling edge of each RDOS pulse toggles A13-5 as shown in Figure 3-28. This output is a replica of the flux pattern as it is recorded on the diskette. PCLK on A13-12 now samples the output from A13-5 at the center of each half-cell window causing A13-3 to set or reset accordingly. A13-3 is then delayed one half-cell by A12-3. AND/OR inverter A11-8 is connected as an exclusive OR and detects any change of state at A13-3. The output, RDATA, goes high for half a cell-time when any flux transition (data or clock) is detected.

**Read Clock Synchronization (Sheet 4 of Dwg 100087)**

The circuit consisting of B11-8, A12-5, and B14-3 generates a clock signal, RCLK/, for the data transitions only which is used to sample the decoded read data. This circuit must be initially synchronized during the preamble so that the correct (data) half-cell is selected.

Flip-flop A12-5 is clocked by PCLK causing the output to change state for each half-cell that NAND output B11-8 is high. A clock pulse is generated on RCLK/ when A12-5 is high as shown in Figure 3-31. In the preamble area the data pattern is known to be all zeroes; i.e., no transitions should be detected in the data half-cell. During the first 700 us of preamble (ROS high) B11-8 tests for this condition and the output goes low for one half-cell if a one-bit is detected. This inhibits A12-5 from changing state one time causing the other half-cell to be selected. Note the period of ROS is long enough to cover both sector-hole tolerancing and the PLL lockup time. During the



**Figure 3-31. Read Decoding and Sync Circuits, Timing Diagram**

remainder of the sector B11-8 remains high and RCLK/ pulses are generated during every second half-cell.

**Read Shift Register and Control Logic (Ref. Sheet 4 of Dwg 100087)**

Shift register C13 assembles the decoded data into byte-parallel form for transmission to the CPU. The control logic consisting of B12-9, D13-13, B13, and D14-6 generates two control signals, RF and RP/, which coordinate the transfer of each byte. See Figures 3-31 and 3-32.

C13 and B12-9 are initially held reset during the beginning of each sector by ROS/ low. When ROS/ goes high zero bits are entered into the register until the first bit of the sync byte is encountered. At this time C13-3 goes high and the rising edge clocks B12-9 causing RF to set. RF true causes TF (transfer flag) to go true signifying that the first (sync) byte is almost ready for transfer.

Counter B13 is initially preset to a count of one by a low output on D13-13. When RF goes true the preset condition is removed and the counter counts off consecutive groups of eight bits corresponding to each byte. A fully assembled byte is available in the shift register when a count of eight is reached. At this time the high output at B13-11 is inverted to form RP/. RP/ low forces PRDY high allowing the CPU to complete execution of the current instruction (read from read data register). B13-11 high also produces a low on D13-13 causing the counter to be preset to one again at the beginning of the following byte. The remaining bytes of the sector are transferred in this manner.

**3.11.8 Data In Bus Multiplexing (Ref. Sheet 5 of Dwg 100087)**

This logic gates PROM, status, or read data information onto the S100 data in bus according to the address specified in the current instruction.

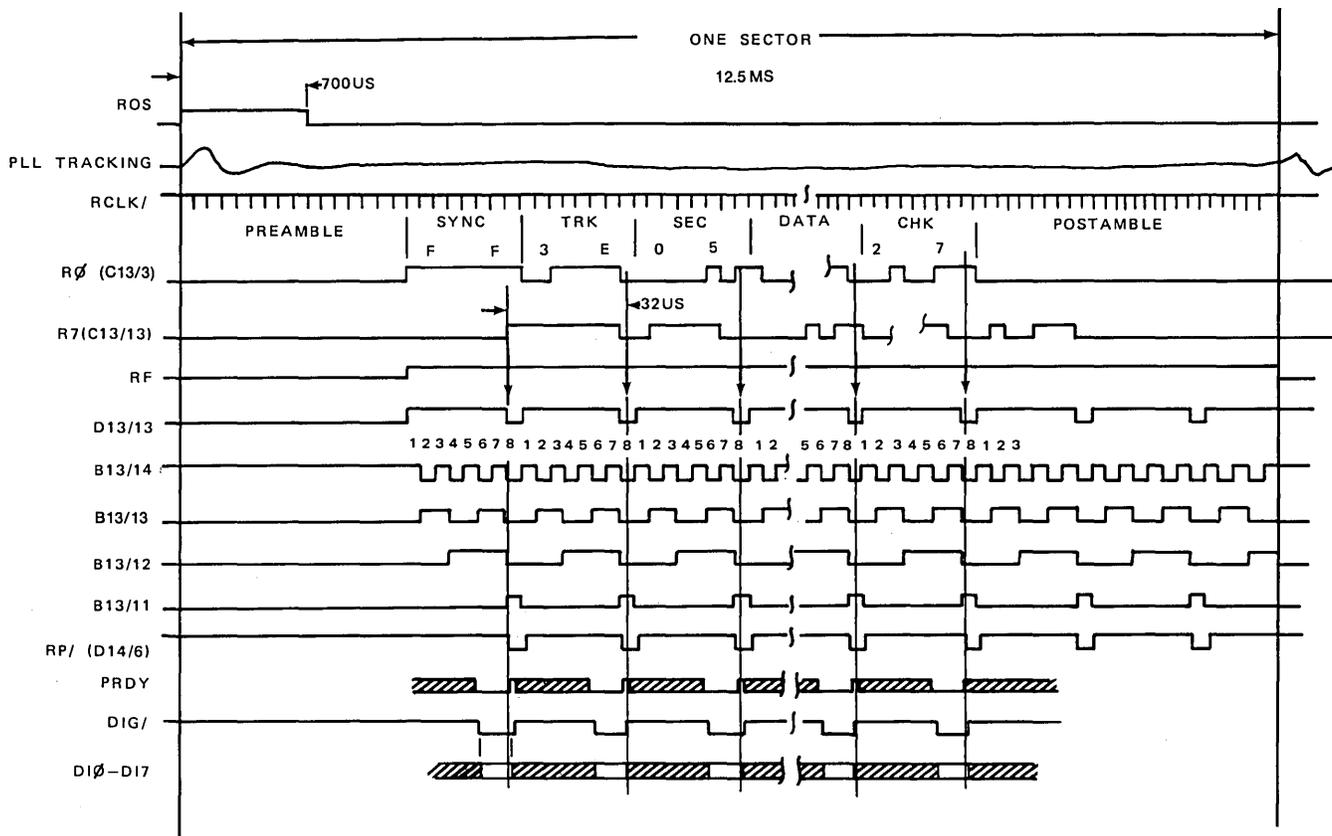


Figure 3-32. Read Logic, Timing Diagram

The PROM's C9 and C10 contain a bootstrap program which loads the system software from disk into memory after power-on. The bootstrap is entered by transferring control to the controller base address (normally F400). A description and listing of this program is given in Para. 6.7 of the Users Manual.

Signals comprising Status Bytes 0 and 1 and the

read register outputs, R0 through R7, are multiplexed together by C4, C5, C11, and C12. Status byte 0 is selected if A1.A0 = 00; Status byte 1 if A1.A0 = 01; and the read register is selected if A1 = 1. The tri-state outputs from either the PROMs or C11, C12 are enabled by CSEL or CSEL/ depending on whether the lower or upper half of the 1K controller address space is being accessed. The selected byte is gated onto data in lines DI0 through DI7, by D11 and D12 when DIG/ is low.

### TEST AND ADJUSTMENTS

#### 4.1 INTRODUCTION

This section provides information on unit testing and specifies the procedures necessary to adjust electrical and mechanical parameters. The tests and adjustments are presented in a sequence not necessarily required in testing the unit. Use the procedures in an order dictated by the operating condition of the drive system.

The tests and adjustments presented in this section cover:

- The controller model 1071-01
- Single drive modules with power supply 1022/1023/1042/1043
- Single drive modules without power supply 1021/1041
- Dual drive modules 1057/1037

In general the test requirements for the different module models are the same. However when the test requirements differ, the relevant paragraphs will specify those differences. Figures 4-1, 4-2 and 4-3 illustrate the location of PCBA-mounted components referenced in this procedure. Single drive PCBA P/N 100164 replaces P/N 100072. See drawing 100163 in Section 9 for test point controls and indicators.

#### *Adjustment Philosophy*

Acceptable limits are defined in each test and adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified.

When the measured value of any parameter is within the specified acceptable limits NO ADJUSTMENT should be made. Should the measured value fall outside the acceptable limits, adjustment should be made in accordance with the relevant procedure.

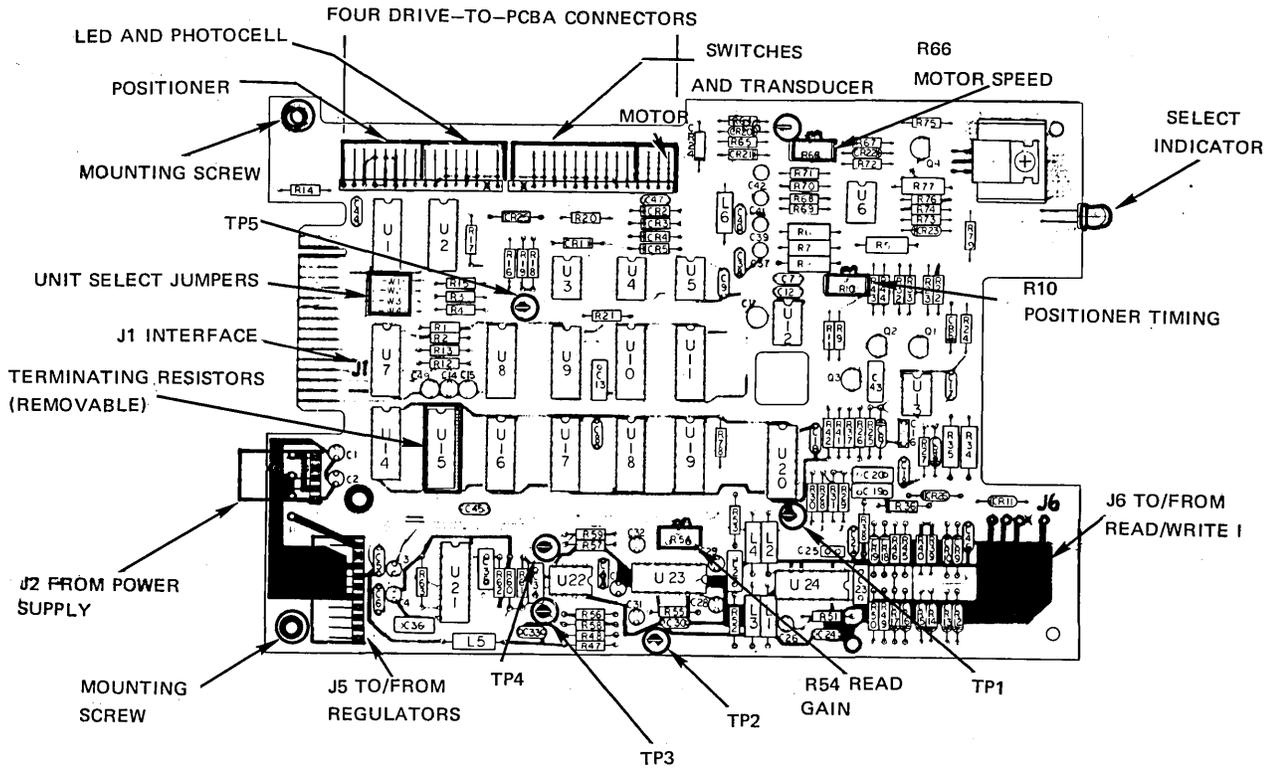


Figure 4-1. Connectors, Controls, Indicators, and Test Points for Single A Drive PCBA (P/N 10071)

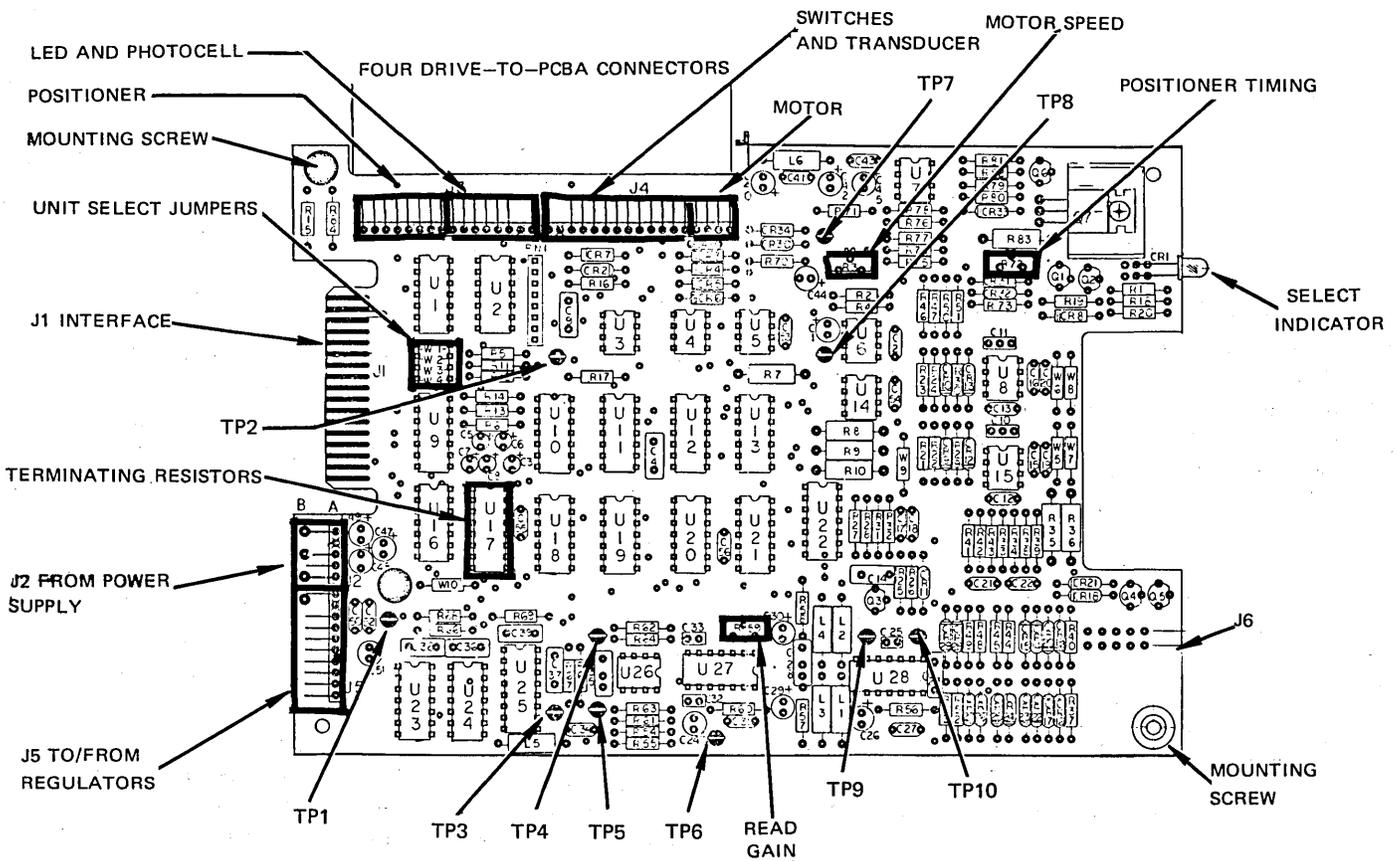


Figure 4-2. Connectors, Controls, Indicators, and Test Points for Single B Drive PCBA (P/N 10063)

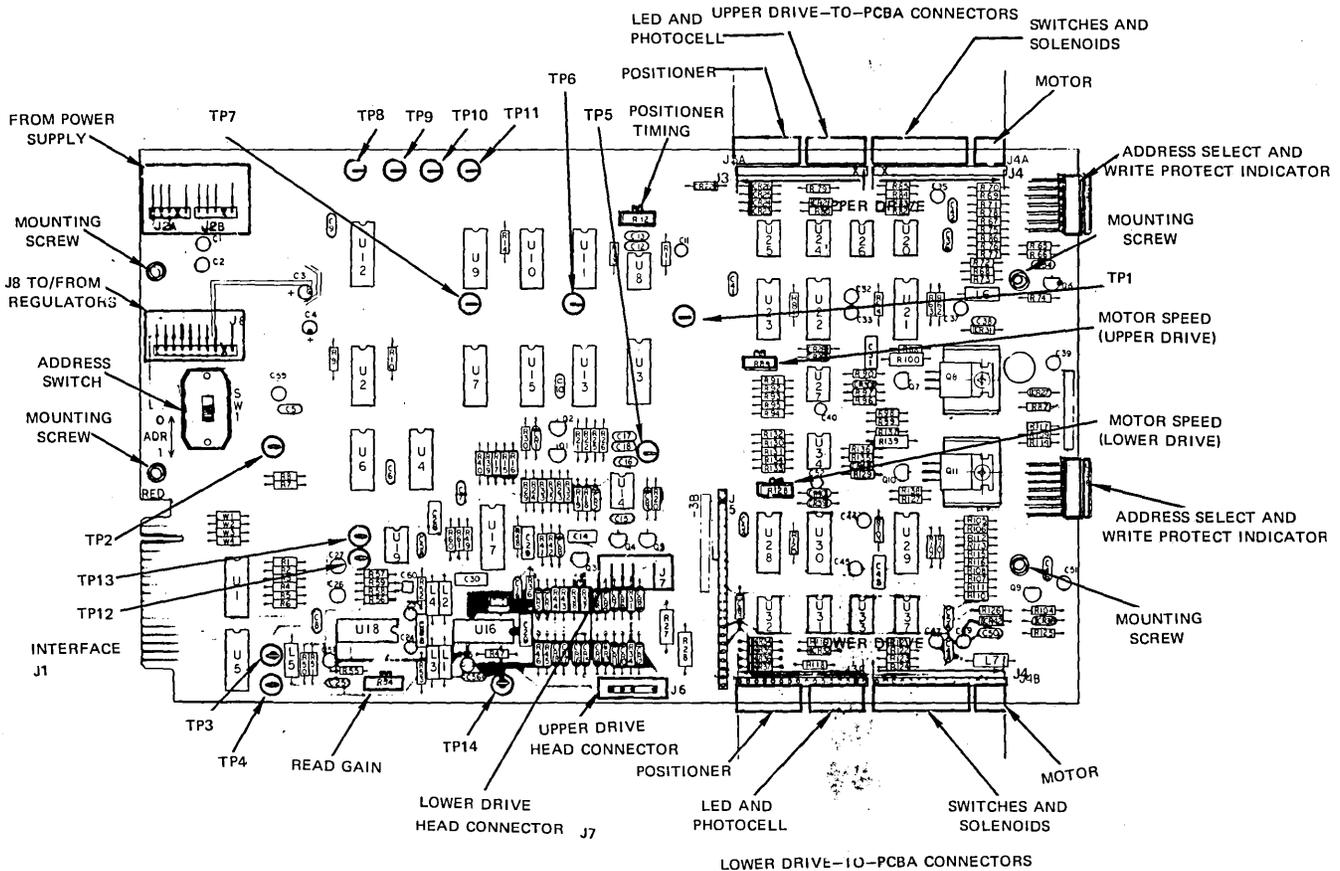


Figure 4-3. Connectors, Controls, Indicators, and Test Points for Dual Drive PCBA (P/N 10060)

### Use of Micropolis Diagnostic Disk

Many of the following procedures require the disk drive to be exercised in a particular manner. Individual procedures indicate, where necessary, the type of exercising required. The Micropolis Diagnostic Disk provides programs which, when an S100 computer system is available, allow the disk drives to be exercised in the desired manner.

Test Program numbers are referenced in the individual procedures.

### NOTE

Each program must be prefaced by the command Z, n, 0† where n is the address of the unit under test. Example:

4.2.1 requires the use of program X12. If the unit under test is Unit 0, then the sequence would be:

```
Z,0†
X,12†
```

(Where † indicates a carriage return)

Section 8 of this manual gives a detailed description of the use of the Micropolis Diagnostic Disk.

## 4.2 POWER SUPPLY (1022, 1023, 1033, 1057, 1037, 1042, 1043, 1053 Only)

Power supply regulators for +5 volt and +12 volt are mounted on a heatsink at the rear of the units. Supplies are tested under normal system load conditions. No adjustments are provided.

### 4.2.1 Test Configuration

- a. Apply power to the unit.
- b. Apply a low interface signal to the MTRN interface line (Pin 16 J1), if the module is not connected to a controller which causes the motor(s) to turn on. In case of a single drive module insert a work diskette in drive and load it.
- c. In case of a dual drive module insert a work diskette in both drives and load them.
- d. Apply interface signals that cause:
  - Drive to be selected.
  - Selected drive to position over its full stroke continuously.

### NOTE

Alternative is to select Program X12 on Micropolis Diagnostic.

#### 4.2.2 Test Procedure

- a. Using a digital voltmeter, verify following voltages:

*Single Drive:*

Voltages	Location	Acceptable Limits	
		Minimum	Maximum
+12V	Between J5-4 and TP1 (GND)	+11.4V	+12.6V
+5V	Between J5-7 and TP1 (GND)	+4.75V	+5.25V

*Dual Drive:*

Voltages	Location	Acceptable Limits	
		Minimum	Maximum
+12VA	Between J8-4 and TP5 (GND)	+11.4V	+12.6V
+5V	Between J8-7 and TP5	+4.75V	+5.25V
+12VB	Between J8-8 and TP5	+11.4V	+12.6V

#### 4.2.3 Adjustment Procedure

NONE, replace parts if tolerances are not met.

#### 4.2.4 External Power Supply (1021, 1041)

Connect external supply to J5. Voltages should lie within acceptable limits specified in Para. 4.2.2.

### 4.3 DRIVE MOTOR SPEED

Drive motor speed should be checked whenever:

- a. The motor is replaced.
- b. The PCBA is replaced.
- c. Any drive motor circuit components are replaced.
- d. Diskette interchange compatibility problems are encountered.

Two methods are available for checking drive motor speed. These involve (A), using the strobe disk attached to the large pulley on the drive (note earlier drives do not have this strobe disk) and (B), measuring the period between index pulses using a counter.

#### 4.3.1 Test Configuration A

- a. Apply power to unit.
- b. Apply a low interface signal to MTRN interface line (Pin 16 J1).
- c. For single drive module insert a work diskette in drive and load it.

For dual drive module insert a work diskette in drive under test and load it.

- d. Apply interface signals that cause:

Drive to be selected.

Selected drive to be positioned at track zero.

### NOTE

Alternative is to select Program X13 on Micropolis Diagnostic.

#### 4.3.2 Test Procedure A

- a. Cause strobe disk to be illuminated by a fluorescent lamp.
- b. Observe outer strobe pattern for 60 Hz power system and inner strobe pattern for 50 Hz power system, and time pattern rotation speed (ideally pattern is stationary).

- c. Acceptable limits:

6 revolutions per minute clockwise or counterclockwise maximum.

- d. For dual drive module repeat Para. 4.3.1, Step d, and repeat Steps a through c above for the alternate drive.

#### 4.3.3 Test Configuration B

- a. Perform Steps a through d of Para. 4.3.1 EXCEPT use single hole diskettes.

b. Connect counter timer to the index/sector test point TP5 and TP2 (GND) on a single drive module, TP2 and TP6 (GND) on a Single B drive, and TP3 and TP14 (GND) on dual drive module.

c. Observe that period of index pulses are within the following limits:

204 milliseconds maximum  
196 milliseconds maximum

d. For dual drive module, repeat Para. 4.3.3, Steps a through c, for the alternate drive.

#### 4.3.4 Adjustment Procedure

Using the procedures of Para. 4.3.1. through 4.3.3 adjust the appropriate drive speeds using:

- Potentiometer R66 on single drive module. (R72 on Single B drive PCBA P/N 100164).
- Potentiometer R89 on upper drive of dual drive module, and potentiometer R128 on lower drive of dual drive module.
- Using test configuration A, speed should be adjusted for a stationary strobe pattern. Using test configuration B, speed should be adjusted to an index pulse period of 200 milliseconds.

#### 4.4 INSTANTANEOUS SPEED VARIATION

Instantaneous speed variation (ISV) is change of rotational speed over a short period of time (approximately 1½ revolutions of the large pulley). Factors causing ISV include worn motor bearings, a defective motor or a defective belt.

ISV should be checked whenever:

- The motor is replaced.
- The PCBA is replaced.
- Any motor drive circuit components are changed.
- The belt is changed.
- Diskette interchange compatibility problems are encountered.

#### 4.4.1 Test Configuration

- Apply power to unit.
- Apply a low interface signal to MTRN interface line (Pin 16J1).
- For single drive module, insert a work diskette in drive and load it.

For dual drive module, insert a work diskette in drive under test and load it.

- Apply interface signals that cause an all zeroes pattern to be written on Track 0 of the drive.
- Apply interface signals that cause drive to be selected.

#### NOTE

Alternative use Program X14 on the Micropolis Diagnostic in place of Steps d and e.

#### 4.4.2 Test Procedure

- Connect oscilloscope to TP3 and TP2 (GND) (TP4 and TP6 on Single B drive) on a single drive module, and TP12 and TP14 (GND) on a dual module. Set vertical scale to 0.2V/CM and time base to 0.5 us/cm and using the 'variable' control, adjust the time base to display 1 cycle on the screen.
- Measure peak to peak ISV (width of trace) as shown in Figure 4-4.

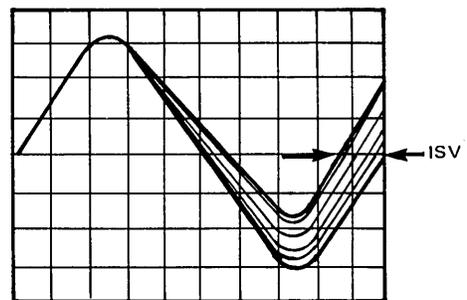


Figure 4-4. ISV Test Waveform

- c. Acceptable limits: 10% peak-to-peak maximum.
- d. In the case of the dual drive module, repeat Para. 4.4.1, Steps a, b, d, e, and f; and Steps a, b, and c of Para. 4.4.2 for the other drive.

#### 4.4.3 Adjustment Procedure

There are no adjustments for ISV, troubleshoot to the defective component.

### 4.5 POSITIONER STEP TIMING

The phase to phase internal timing for the 4-phase stepper motor positioner is determined by the period for which the gated oscillator (U12 for single drive, U6 for Single B drive, U8 for dual drive) is enabled (SBSY high). This adjustment should be checked whenever:

- a. The PCBA is replaced.
- b. Components in the positioner timing circuits are replaced.
- c. There is any indication of incorrect positioning.

#### 4.5.1 Test Configuration

- a. Apply power to unit.
- b. Apply a low interface signal to MTRN interface line (Pin 16 J1).
- c. For single drive module, insert a work diskette in drive and load it.  
  
For dual drive module, insert a work diskette in upper drive and load it.
- d. Apply interface signals that cause drive to be selected and perform a continuous full track seek.

#### NOTE

Alternatively select Program X12 on Micropolis Diagnostic.

#### 4.5.2 Test Procedure

- a. Connect oscilloscope to U12-4 and TP1 (GND) on single drive module (TP8, TP1 for Single B drive) and U8-4, TP5 (GND) on dual

module. Set vertical scale to 2V/cm and time base to 5 ms/cm. Trigger internally positive.

- b. Observe that duration of positive going position of waveform (Figure 4-5) is within the following limits:

100TPI (MOD II)	23.5 msec	maximum
	21.5 msec	minimum
48TPI (MOD I)	26 msec	maximum
	24 msec	minimum

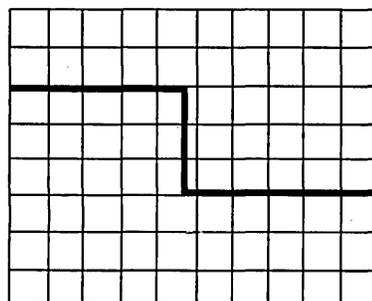


Figure 4-5. Positioner Step Timing Waveform

- c. For reference the duration of the individual "step times" can be observed at U8-8 on the single drive module, U16-4 on Single B drive, and U22-8 on the dual drive module. These are shown in Figure 3-12 for a correctly adjusted step-timing.

#### 4.5.3 Adjustment Procedure

Using the procedures of 4.5.2 adjust the step timing using:

- a. Potentiometer R10 on single drive module (R3 on Single B drive).
- b. Potentiometer R12 on dual drive module.
- c. Adjust timing to:

48TPI (MOD I)	25.0 msec
100TPI (MOD II)	22.5 msec

#### NOTE

Individual "step times" are not adjustable. If these are out of tolerance troubleshoot to defective component.

## 4.6 READ AMPLIFIER GAIN

The read amplifier gain control sets the signal level at the output of the amplifier chain. The adjustment should be checked whenever:

- a. The head is replaced.
- b. The PCBA is replaced.
- c. Components in the R/W switch, differentiator or amplifier circuits are replaced.

### 4.6.1 Test Configuration

- a. Apply power to the unit.
- b. Apply a low interface signal to the MTRN interface line (Pin 16 J1).
- c. For a single drive module, insert a work diskette and load it. For a dual drive module, insert a work diskette in both drives and load them.
- d. Apply interface signals that cause an all ones pattern to be written on track zero of drive(s).
- e. For single drive module, apply an interface signal that causes drive to be selected.

For dual drive module, apply interface signals causing upper and lower drives to be selected alternately.

#### NOTE

Alternatively use Programs X14 and X15 to achieve Steps d and e above.

### 4.6.2 Test Procedure

- a. Connect oscilloscope to TP3 and TP2 (GND) on the single drive module (TP5 and TP6 for Single B drive), and TP12 and TP14 (GND) on the dual drive module. Set the vertical scale to 0.5V/cm and the time base to 10 us/cm. Trigger internally.
- b. Measure the peak-to-peak amplitude of the read signal on the single drive module and the two signals from the upper and lower drives on the dual drive module. Ensure that limits are within the following tolerances:

2.0V peak-to-peak maximum  
1.0V peak-to-peak minimum

## 4.6.3 Adjustment Procedure

Using the procedure of 4.6.2 adjust the read gain using potentiometer R54 on either the single or dual drive module (R59 on Single B Drive). Adjust read signal amplitude to 1.5V peak-to-peak for single drive module. For a dual drive module the two amplitudes, when selecting first the upper drive then lower drive, should lie on either side of 1.5V nominal by equal amount.

## 4.7 HEAD COMPLIANCE

The head compliance test checks for the presence of the correct intimate contact between head and media. Good compliance is ensured when the head load pad presses the media uniformly against the head. Compliance should be checked whenever:

- a. Data errors are encountered.
- b. Whenever it is suspected that the load pad may have become worn or contaminated with oxide or dirt.

### 4.7.1 Test Configuration

- a. Apply power to unit.
- b. Apply a low interface signal to MTRN interface line (Pin 16 J1).
- c. For single drive module, insert a work diskette in drive and load it.

For dual drive module, insert a work diskette in both drives and load them.

- d. Apply interface signals that cause an all ones pattern to be recorded on Track 76 on a 100TPI (MOD II) drive and Track 34 on a 48TPI (MOD I) drive of drive under test.
- e. Apply interface signals that cause drive under test to be selected with positioner at track indicated in Step d.

#### NOTE

Alternatively use Program X16 on Micropolis Diagnostic.

### 4.7.2 Test Procedure

- a. Connect oscilloscope to TP3 and TP2 (GND) (TP5 and TP6 (GND) on Single B drive) on single drive module, and TP12 and TP14 (GND) on dual module.

- b. Monitor signal amplitude while increasing force on head load arm. (Note: application of too much force will cause disk to slow down.)
- c. Acceptable limits. Signal amplitude increase should be 15% maximum.
- d. For dual drive module, repeat Paragraph 4.7.1, Steps a, e, and f; and Steps a, b, and c above on second drive.

**4.7.3 Adjustment Procedure**

None, replace load pad. (Refer to Section 6, Para. 6.5.)

**4.8 CIRCUMFERENTIAL/AZIMUTH ALIGNMENT**

The circumferential/azimuth alignment test checks that:

- a. The relationship between the head and the index/sector photocell is correct.
- b. That the head moves along a line which passes through the center of the diskette, i.e. is a radius.

The alignment should be checked whenever:

- a. The head is replaced.
- b. The positioner subassembly is replaced.
- c. The platten assembly or photo transistor is replaced.
- d. The L.E.D. assembly or LED is replaced.
- e. Diskette interchange compatibility problems are encountered.

**4.8.1 Test Configuration**

- a. Apply power to unit.
- b. Apply a low interface signal to MTRN interface line (Pin 16 J1).
- c. For single drive module, insert an alignment diskette, Micropolis P/N 641 0590-1, Dysan P/N 282 and load it.

For dual drive module, insert alignment diskette in drive under test.

**4.8.2 Test Procedure**

- a. Connect oscilloscope to TP3 and TP2 (GND) (TP5 and TP6 on Single B drive) on a single drive module, and TP12, TP14 (GND) on a dual drive module. Set vertical scale to 0.5V/cm and time base to 50us/cm. Trigger oscilloscope from positive (leading) edge of index/sector pulse using TP5 on a single drive module, (TP2 on a Single B drive), and TP3 on dual module.

- b. Apply interface signals that cause drive under test to be selected. Position selected drive over:

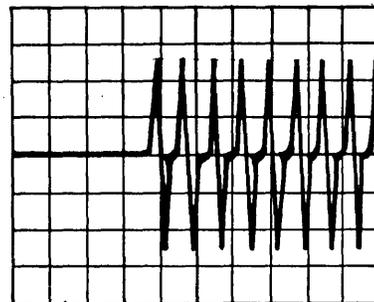
Track 5 for 100TPI (MOD II) systems

Track 1 for 48TPI (MOD I) systems

- c. Alternatively use Program X17 for 100TPI systems and X18 on 48TPI systems on Micropolis Diagnostic.
- d. Measure time between leading edge of index pulse and first peak of index alignment burst (Figure 4-6). When the diagnostic is used, make measurement when positioner is at outermost track. Note the value. Ensure that time is within the following limits:

300 useconds maximum

100 useconds minimum



**Figure 4-6. Circumferential/Azimuth Alignment Waveform**

- e. Apply interface signals that cause drive under test to be selected. Position selected drive over:

Track 76 for 100TPI (MOD II) systems

Track 35 for 48TPI (MOD I) systems

**NOTE**

Alternatively use Program X17 for 100-TPI system and X18 on 48TPI system on the Micropolis Diagnostic.

- f. Measure time between leading edge of index pulse and first peak of index alignment burst and compare this with value obtained in Step d. When diagnostic is used, make measurement when positioner is at outermost track. The two values obtained in Steps d and f above should differ in either direction by no more than 100 useconds maximum.

- g. If the acceptable limit in Step f is exceeded, perform the azimuth adjustment procedure of Para. 4.8.3 and then the circumferential adjustment procedure of Para. 4.8.4.

If the acceptable limit in Step f is NOT exceeded, but that of Step d is exceeded, perform the procedure of Para. 4.8.4 only.

- h. For dual drive module, repeat Para. 4.8.2 for the lower drive.

**NOTE**

As positioner azimuth is adjusted, significant changes of burst amplitude will occur. In extreme cases it may be necessary to readjust radial alignment, during azimuth alignment, to reestablish an on-track condition. If this procedure is necessary, check radial adjustment, Para. 4.9.

**4.8.3 Azimuth Adjustment Procedure**

- a. For a single drive module, remove drive mechanism plus PCBA from the chassis and connect it to power supply using power supply extender cable. For a dual drive module, remove PCBA and then upper and lower

drive mechanism as described in Section 6, Para. 6.2. The drive under test and PCBA should be reconnected into module using power supply and head extender cables as required.

**NOTE**

A standoff is provided in tool kit which should be installed at rear of drive under test (see Figure 4-7) so that mechanism does not rest on step motor when it is on bench.

- b. Perform Steps a through c of Para. 4.8.2.

**NOTE**

Step c below is performed to ensure that steps d through h can be achieved.

- c. Loosen two platten assembly mounting screws on platten assembly (Figure 4-7) and temporarily move platten using a screwdriver to implement a wedging technique between tongue on platten, and slots in chassis, until index to burst time after reclamping platten is approximately 6 cm (300 useconds).

- d. Loosen two positioner mounting screws (visible from below at rear of step motor, Figure 4-7) holding positioner spring plate to mounting block.

- e. If in Para. 4.8.2, index to index burst time in Step d (TK1 or TK5) exceeds that of Step f (TK35 or TK76), positioner azimuth should be moved towards drive motor. This will decrease both the above times, but will also tend to equalize them.

- f. If in Para. 4.8.2, index to index burst time in Step d is less than that of Step f, positioner should be moved away from drive motor.

- g. After each movement in Steps d or e above, tighten the screws and repeat Steps a through f of Para. 4.8.2 until difference of times is approximately zero.

- h. Perform procedures of Para. 4.8.4.

#### NOTE

Radial alignment *MUST* be checked after azimuth adjustment. Refer to Para. 4.9.

After adjustment of azimuth, it is possible that misstepping will occur. This should be checked using Steps a through e of Para. 4.12.1.

#### 4.8.4 Circumferential Adjustment Procedure

- a. Perform Steps a through c of Para. 4.8.2.

#### NOTE

If drive under test has already been removed from chassis, proceed to Step c. Otherwise perform Step b.

- b. For single drive module, turn chassis on its side and proceed with Step c. Screws are accessible through clearance holes in chassis (Figure 4-7). For a dual drive module, upper drive must be removed using procedure of Section 6, Para. 6.2.3.1.

#### NOTE

A maintenance stand-off is provided in tool kit which should be installed at rear of drive (see Figure 4-7) so that mechanism does not rest on step motor when it is on bench.

- c. Loosen two clamp screws on platten assembly and adjust platten as in Para. 4.8.3, Step c, so that the index to burst time is now the optimum  $200 \pm 30$  useconds after reclamping platten.
- d. Remove stand-off and reinstall drive (see Section 6, Para. 6.2.3.2).

#### 4.9 RADIAL ALIGNMENT

Radial alignment ensures that the head is operating at the required radius for the particular track number. Alignment is made using an alignment disk, Micropolis P/N 641 0590-1 Dysan P/N 282 which has a "cat's eye" pattern centered on:

Track 36 for 100TPI (MOD II) systems

Track 16 for 48 TPI (MOD I) systems

Radial alignment should be checked whenever:

- a. The head has been replaced.

- b. The positioner assembly has been changed.
- c. The positioner assembly has been adjusted for preload or azimuth.
- d. Diskette interchange compatibility problems are encountered.

#### 4.9.1 Test Configuration

- a. Apply power to unit.
- b. Apply a low interface signal to MTRN interface line (Pin 16 J1).
- c. For a single drive module, insert an alignment diskette and load it. For a dual drive module, insert alignment diskette in drive under test and load it.

#### 4.9.2 Test Procedure

- a. Connect oscilloscope to TP3 and TP2 (GND) on a single drive module (TP5 and TP6 for Single B drive) and TP12, TP14 (GND) on a dual drive module. Set vertical scale to 0.2V/cm and time base to 20 msec/cm. Trigger the oscilloscope from positive (leading) edge of index/sector pulse using TP5 on a single drive module, (TP2 for Single B drive), and TP3 on dual module.
- b. Apply interface signals that cause drive under test to be selected. Position selected drive over:

Track 36 for 100TPI (MOD II) systems

Track 16 for 48TPI (MOD I) systems

- c. Observe read signal (Figure 4-8). Adjust vertical scale such that peak amplitude of larger lobe is 5 major divisions (5 cm) and note amplitude of smaller lobe.
- d. Apply interface signals that cause selected drive's positioner to move off track in one direction by at least two tracks and return to:

Track 36 for 100TPI (MOD II) systems

Track 16 for 48TPI (MOD I) systems

- e. Observe read envelope.

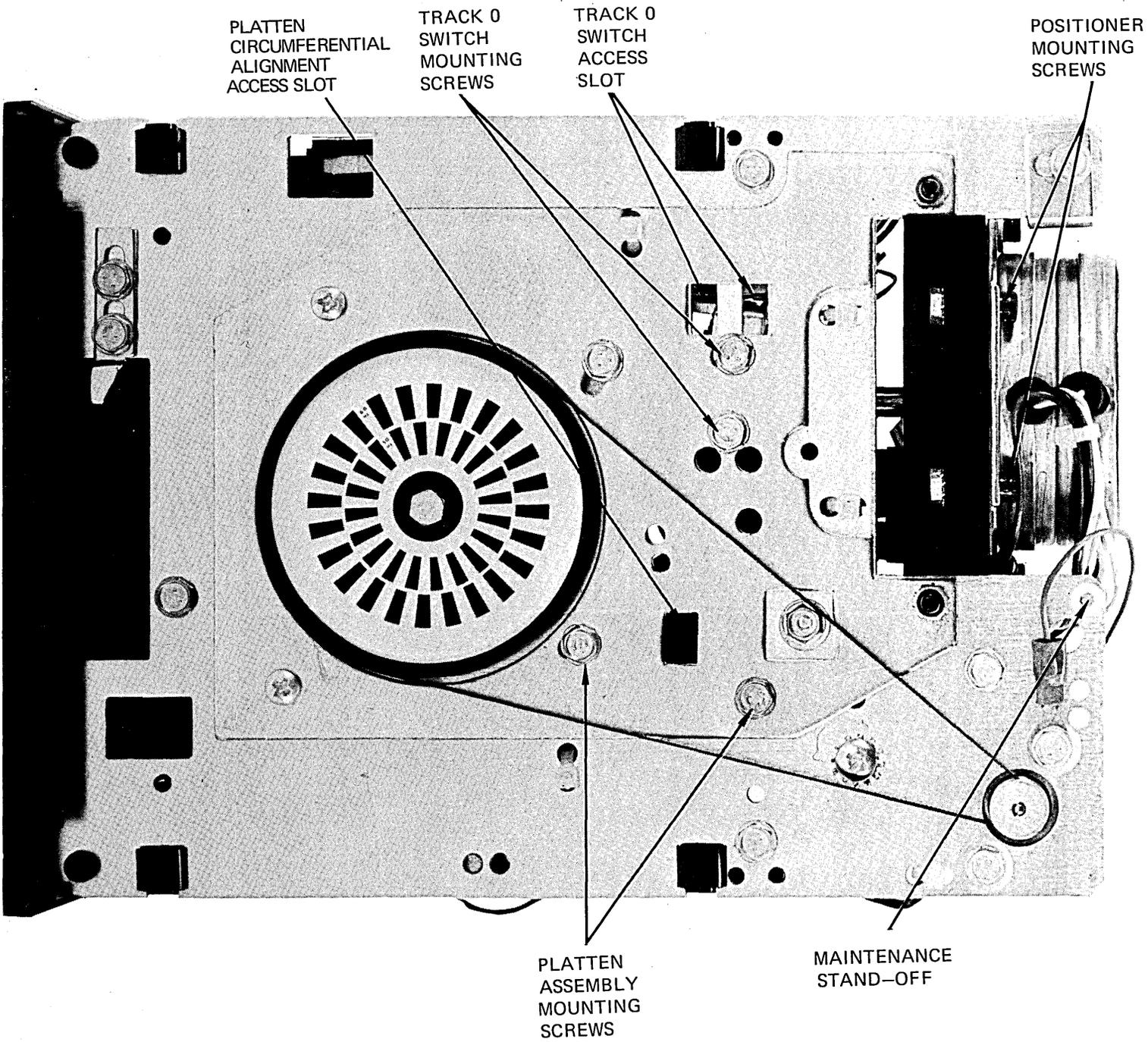
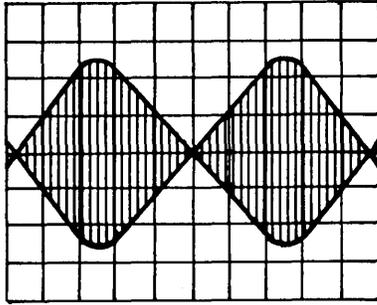


Figure 4-7. Drive Adjustment Access



**Figure 4-8. Ideal Cat's Eye Pattern for Radial Alignment**

- f. Repeat Step d causing positioner to move off track in other direction. Observe read envelope.

**NOTE**

Alternatively use program X7 for 100TPI systems and X8 for 48TPI systems on the Micropolis Diagnostic.

- g. Ensure that alignment is within the following limits:

Acceptable track alignment is indicated when peak-to-peak amplitude of two lobes of pattern are within 1 major division (1 cm) of being equal when larger lobe is set to 5 major divisions (Figure 4-8).

- h. For dual drive, repeat Para. 4.9.2 for other drive.

**4.9.3 Adjustment Procedure**

Using procedure of Para. 4.9.2, adjust radial alignment as follows:

- a. Follow Step a of Para. 4.8.3 EXCEPT in case of dual drive, upper drive may be adjusted in place.
- b. Loosen two positioner flange mounting screws that clamp positioner flange to the spring plate (Figure 4-9).
- c. Rotate positioner body as required to equalize lobes. Rotate CW if first lobe is greater than second and rotate CCW if first lobe is smaller than second.

**NOTE**

If the adjustment range is inadequate, the track zero switch needs to be moved one full tract. See Section 4.10.

**NOTE**

When using the Micropolis Diagnostic to perform Para. 4.9.2, Steps d and e, positioner stepping normally occurs automatically once every 10 seconds. Handling of positioner, loosening or tightening screws, etc. should not take place during stepping; otherwise, mis-step will occur and positioner will have to be rezeroed and program restarted.

Alternatively a "single mode" of operation may be used by using 'SUSPEND' and 'CONTINUE' modes of the Diagnostic (refer to Section 8).

- d. Retighten screws.
- e. Perform Steps d and e of Para. 4.9.2 and observe read envelope.
- f. Repeat adjustment as necessary to obtain equal lobe amplitudes.

**NOTE**

Sometimes lobe amplitudes cannot be equalized for conditions of both Steps d, e, and f of Para. 4.9.2. In this case, adjust radial alignment so that differential between lobes is equal and opposite for the conditions of Steps d and e. If under these conditions the acceptable limits are exceeded, check:

Positioner Step Timing — Paragraph 4.5

Positioner Mounting Mechanical Adjustment — Para. 4.12

- g. Remove the stand-off and reinstall the drive (see Section 6, Para. 6.2, as necessary).

**4.10 TRACK ZERO SWITCH AND STOP**

The track zero switch indicates to the controller that the head is at track zero. The zero stop is a mechanical stop on the lead screw which prevents the positioner from moving behind track zero.

The track zero switch and stop should be adjusted whenever:

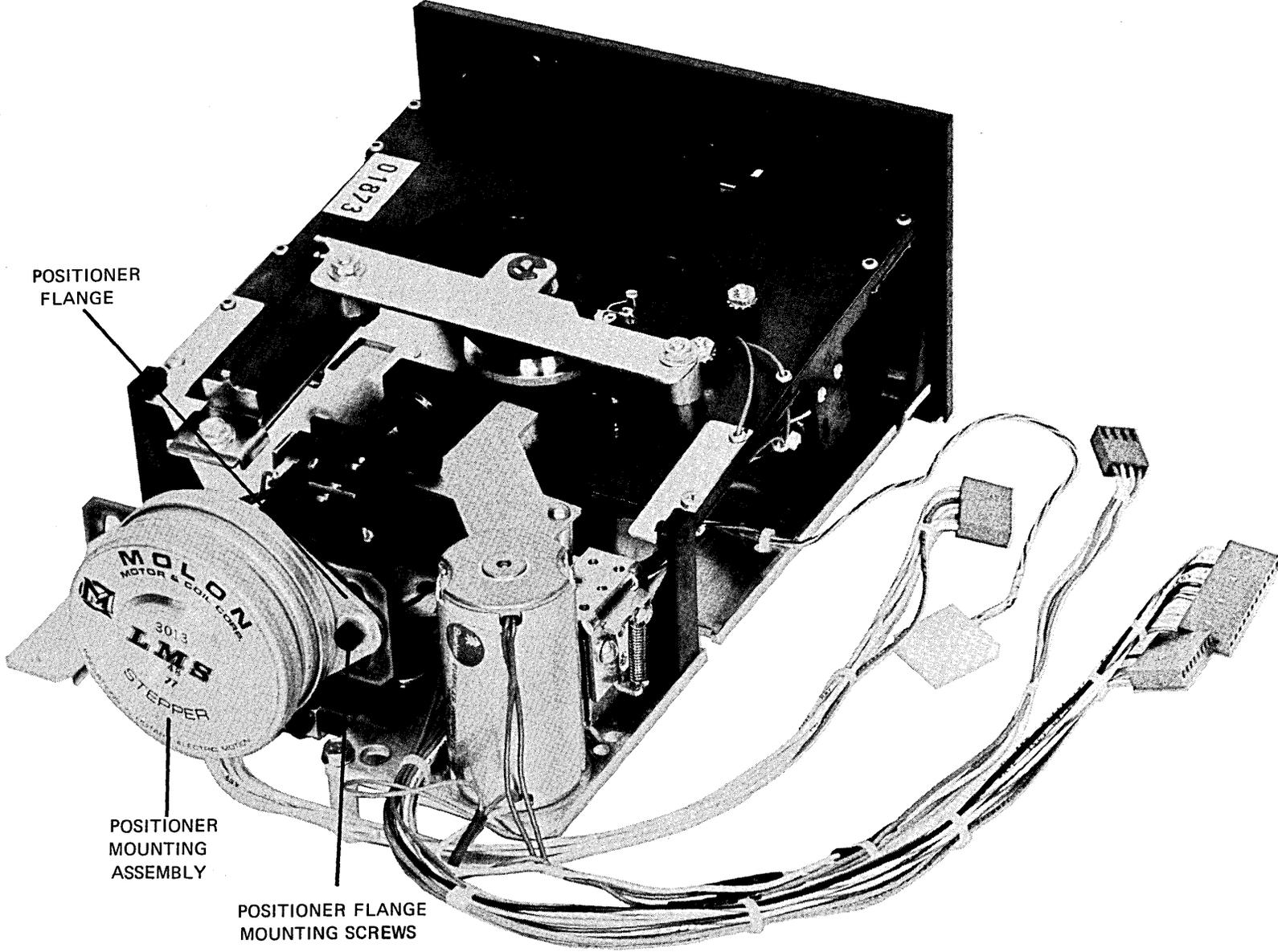


Figure 4-9. Positioner Adjustments

- a. The positioner has been replaced.
- b. The head has been replaced.
- c. The switch has been replaced.
- d. Radial alignment has been performed.
- e. The positioner is heard hitting against the mechanical stop.
- f. Correct radial alignment, Section 4.9, cannot be achieved.

#### 4.10.1 Test Configuration

- a. Apply power to unit.
- b. Apply a low interface signal to MTRN interface line (Pin 16 J1).
- c. For single drive module, insert a work diskette in drive and load it. For dual drive module, insert a work diskette in drive under test and load it.
- d. Apply interface signals that cause:

Drive to be selected.

Selected drive to position between tracks 0 and 1 with a turnaround time of approximately 200 msec.

#### NOTE

Alternatively use Program X9 on the Micropolis Diagnostic Disk.

#### 4.10.2 Test Procedure

- a. Connect channel 1 of oscilloscope to SBSY signal on U12-4 on single drive module (TP8 on Single B drive) and U8-4 on dual module. Set vertical scale to 2V/cm.
- b. Connect channel 2 of oscilloscope to track zero switch output U2-3 on single drive module (2-4 on Single B drive), and U3-9 on dual module. Set vertical scale to 2V/cm.
- c. Set time base to 2 msec/cm and trigger on positive going edge on channel 1 only.
- d. Observe waveform on channel 2. This is shown in Figure 4-10.
- e. Acceptable limits: High to Low transition and Low to High transition occur at same

time on alternate sweeps within  $\pm 2$  major divisions ( $\pm 4$  msec).

- f. In case of dual drive, repeat Steps d and e of Para. 4.10.1 and above steps for other drive.

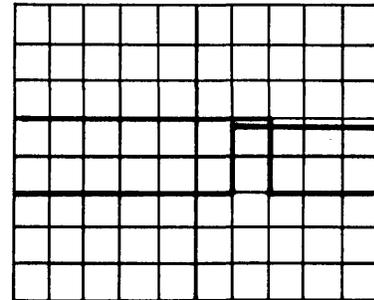


Figure 4-10. Track Zero Switch, Test Waveform

#### 4.10.3 Adjustment Procedure

Perform test procedure, Para. 4.10.2; then adjust track zero switch as follows:

- a. Place a screwdriver in slots adjacent to where track zero switch bracket is mounted to chassis, Figure 4-7. Two slots are accessible through holes in bottom of chassis in single drive module. In dual drive module slots in lower mechanism are accessible through holes in bottom of chassis. Slots in top mechanism are accessible from side of unit opposite PCBA.
- b. Use a wedging technique to move bracket backwards or forwards to line up transitions referred to in Para. 4.10.2, Step d. It may be necessary to slightly loosen switch bracket mounting screws.
- c. Adjust track zero stop so that when head is positioned at track zero, positioner cannot rotate more than 1/3 of a step behind track zero. If necessary, loosen socket screw and reset stop so that positioner can rotate 5° to 10° behind track zero before hitting the stop. Use an angled allen wrench for the lower drive of a dual drive module.

#### NOTE

A 5° to 10° free movement must be provided to prevent positioner from hitting stop due to overshoot when positioning to track zero normally.

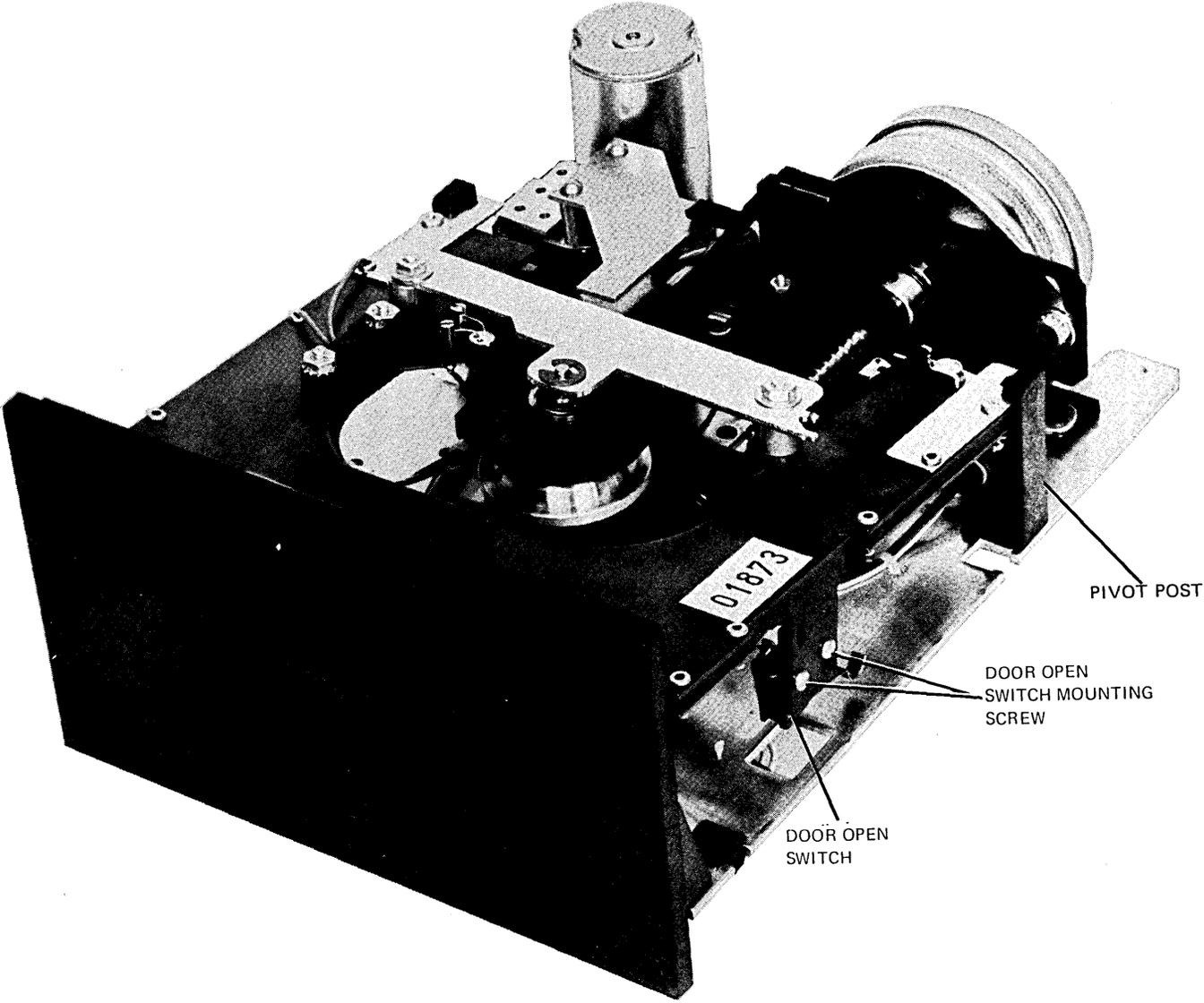


Figure 4-11. Door Open Switch and Mounting Location

#### 4.11 DOOR OPEN SWITCH (Ref. Figure 4-11)

The door open microswitch is required to activate when the receiver assembly has been depressed the minimum amount from its full open position. The door open switch should be adjusted whenever:

- a. The door switch has been replaced.
- b. The receiver assembly has been replaced.
- c. There is evidence of diskette misclamping.

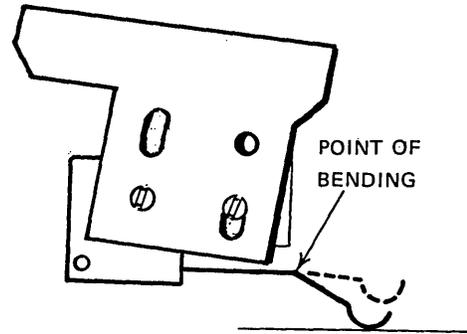


Figure 4-12. Door Open Switch Adjustment for Modules Prior to 812XXXX

##### 4.11.1 On-Line Test Configuration

Apply power to unit and apply a low interface signal to MTRN interface line (Pin 16 J1).

##### 4.11.2 Off-line Test Configuration

Connect an ohmmeter between the yellow and green wires in the 12 position Molex connector attached to the drive mechanism.

##### 4.11.3 Test Procedure

- a. Depress receiver assembly until motor rotates in the On-Line Configuration or the ohmmeter indicates continuity in the Off-Line Configuration. Ensure that switch activates within the following limits:

Switch should activate before top of receiver is more than  $\frac{1}{8}$ " below slot in front panel.

##### 4.11.4 Adjustment Procedure for Modules with S/N prior to 812XXXX

- a. Perform test procedure, Para. 4.11.3, then adjust door open switch by increasing bend angle on switch arm. (See Figure 4-12.) Note the point of bending should occur where the switch arm exits the switch profile (dotted arrow).
- b. Activate receiver assembly 10 times to stabilize bend and check that test meets acceptable limits.
- c. At point of maximum depression of receiver assembly, switch arm should clear switch body. If this does not occur, adjust position and amount of bend.

##### 4.11.5 Adjustment Procedure for Modules with S/N after 812XXXX

These drive mechanisms use a longer heavy gauge actuator, which should not be bent. The switch is adjusted by loosening the two switch mounting screws and rotating the switch until the results of Para. 4.11.3a is achieved.

#### 4.12 POSITIONER MECHANICAL ADJUSTMENT (Ref. Figure 4-9)

The positioner mounting block incorporates adjustments for the preload of the lead screw against the spindle housing and for azimuth alignment of the axis of travel of the headgap. The positioner mounting block adjustment is critical and complex and should only be performed if:

- a. The positioner is replaced or removed in order to install a new head.
- b. The positioner shows evidence of misstepping even after the Step Timing (Para. 4.5) has been adjusted.

##### 4.12.1 Test Configuration

- a. Perform Step a of Para. 4.8.3.
- b. Apply power to unit.
- c. Manually move lock bar backwards until it locks simulating existence of a diskette.

- d. Apply interface signals such that positioner can be caused to step inwards and restore to Track Zero.

**NOTE**

Alternatively use X12 on Micropolis Diagnostic Disk.

**4.12.2 Test Procedure**

- a. While performing Step d above, if misstepping occurs, proceed to adjustment.
- b. As positioner steps, apply gentle pressure to body of step motor at points shown (1, 2, 3, and 4 in Figure 4-13) until misstepping occurs. Assess qualitatively the pressure required to cause misstepping. If pressure is equal at all points, and/or a small region of free rocking exists in both axes, this is acceptable.

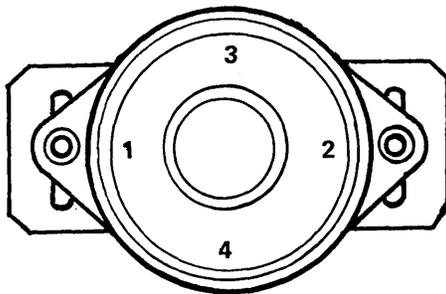


Figure 4-13. Pressure Points on Positioner

**4.12.3 Coarse Adjustment Procedure (Ref. Figure 4-14)**

- a. If positioner assembly is being newly installed, loosen positioner mounting block screws until block can be moved back and forth with small forces.
- b. Push one side and then the other towards spindle until C clip at end of lead screw JUST comes into contact with bearing at end of lead screw.
- c. Push positioner mounting block forward on one side about 1/32" and tighten mounting screw enough to hold block in place.

- d. Push other side of block forward the same amount and tighten other mounting screw. The block should now be parallel to slot in which block sits. If it is not, readjust relevant side to ensure this condition.

**NOTE**

Block must be parallel to slot in which block sits for step e measurement to be valid.

- e. Use a force gauge to measure the force required to pull positioner so that C clip JUST starts to leave bearing in spindle housing. This should be between 2½ and 3 lb.
- f. If the force is too high, move block away from the spindle.  
  
If the force is too low, move block towards spindle.
- g. Repeat Steps e and f to obtain the correct force.
- h. Use procedures of Para. 4.12.1 and 4.12.2 to check for misstepping.
- i. If misstepping still occurs or the acceptable limits are exceeded, it is because mounting block is not set parallel to slot. Perform fine adjustment procedure of Para. 4.12.4; otherwise proceed to Step j of this paragraph.
- j. Remove stand-off and reinstall drive (see Section 6, Para. 6.2).

**4.12.4 Fine Adjustment Procedure**

If the positioner assembly is already in place but needs adjustment:

- a. Perform Step b of Para. 4.12.2.

**NOTE**

Steps b and c which follow can be interactive so that the fine adjustment process is iterative.

- b. Ability to apply more pressure at 1 than 2 *without* misstep indicates that the '1' side of the block should be moved towards the spindle and vice-versa.

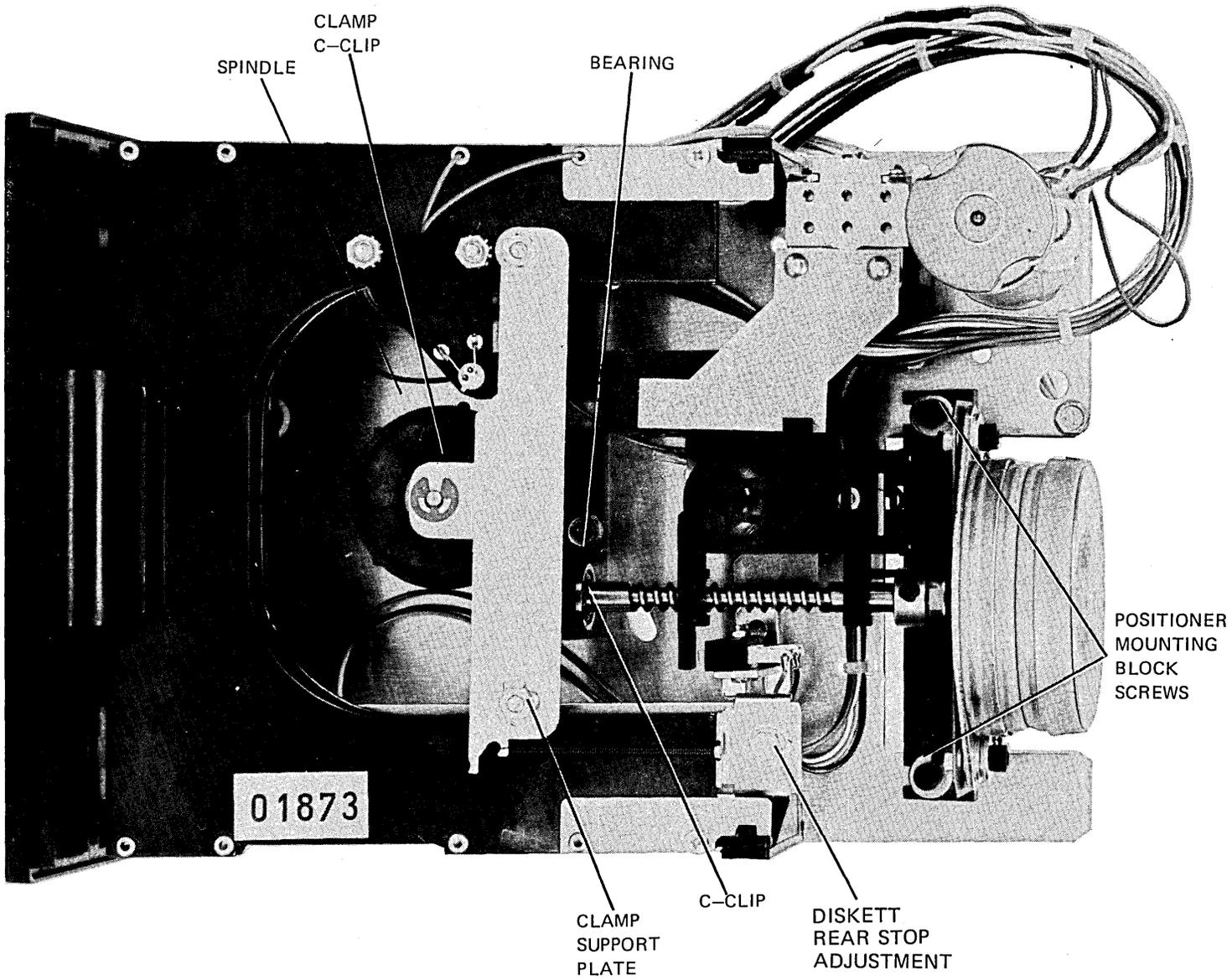


Figure 4-14. Drive Mechanism Only, Top Rear View

## NOTE

During adjustment in Step c, move block approximately 1/64" at a time.

- c. Ability to apply more pressure at 4 than 3 *without* misstep indicates that the *block as a whole* should be moved towards the spindle and vice-versa.
- d. Remove stand-off and reinstall drive (see Section 6, Para. 6.2).
- e. Recheck step e of Para. 4.12.3.

### 4.13 WRITE PROTECT SWITCH

The write protect switch is mounted on a tab on the receiver (opposite side from door-open switch). It senses the presence of a slot or no slot (covered by a write protect tab for the purpose of inhibiting write operation when the tab is in place). The switch should be adjusted whenever:

- a. The switch is replaced.
- b. False detection of either a write protected or not write protected condition occurs.

#### 4.13.1 Test Configuration

- a. Connect an ohmmeter between Black and White/Brown wires in 12 position Molex connector attached to drive mechanism.
- b. When drive under test is installed in a dual drive module, remove the PCBA to obtain access to the switch.

#### 4.13.2 Test Procedure

- a. Normally with no disk inserted switch is open.
- b. Insert feeler gauges from front of unit on left side of receiver slot with thicknesses ranging from 0.20" to 0.050" and observe ohmmeter reading for continuity. Use the following acceptance criteria:

Continuity readings for gauge thicknesses in range 0.025" to 0.045" is acceptable. Below 0.025" no continuity is required. Continuity for gauges above 0.045" thick is unacceptable.

### 4.13.3 Adjustment Procedure

- a. Perform test procedure of Para. 4.13.2, then adjust switch as follows:

## NOTE

Use care as the tab is breakable.

- b. Loosen, slightly, two screws mounting switch to receiver tab.
- c. Rotate switch so that continuity indication occurs when feeler gauge is 0.035".

### 4.14 CLAMP SUPPORT PLATE (ef. Figure 4-14)

The clamp support plate provides the mounting surface for the clamp. The clamp shaft must be centered in the support plate hole such that the shaft does not touch the support plate, either on the side or via the C-clip which secures the clamp shaft when the receiver assembly is in the loaded position.

This adjustment should be checked whenever:

The support plate is removed for any reason.

The spindle assembly is replaced.

There is evidence of severe disk wear at center of the disk in clamp area.

#### 4.14.1 Test Configuration

- a. For single drive module, remove PCBA and reconnect it using extender cables as necessary. For dual drive module, the upper drive is accessible. Remove upper drive to obtain access to lower drive (see Section 6, Para. 6.2).
- b. Set up drive mechanism so that spindle rotates if receiver is loaded by applying a low interface signal to Pin 16 of J1.

#### 4.14.2 Test Procedure

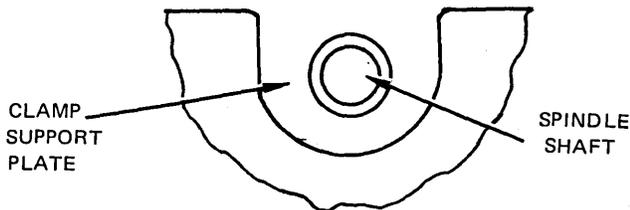
- a. Insert a diskette in drive and close door.
- b. Clearance should exist between clamp shaft and clearance hole in support plate.

- c. Clearance should also exist in loaded position between clamp C-clip and top of support plate to ensure that full clamp spring force exists. Otherwise, disk slippage and wear will occur.

#### 4.14.3 Adjustment Procedure

Using the test procedure of Para. 4.14.2, adjust the position of the support plate as follows:

- a. Loosen support plate mounting nuts.
- b. Move plate forwards, backwards and sideways as required to center clamp mounting shaft. Retighten screws.
- c. Unload and reload diskette two or three times and check that clearance still exists.



#### 4.15 DISKETTE REAR STOP TEST AND ADJUSTMENT PROCEDURE (Ref. Figure 4-14)

- a. Perform Step a of Para. 4.14.1.
- b. Insert a diskette in drive and carefully clamp it.
- c. Loosen rear stop adjustment screw and adjust its position on interlock bar so that with jacket seated against stop, the opening in center of diskette jacket is centered around clamp.
- d. Tighten stop adjustment screw.
- e. Unload diskette, reload it, and check adjustment.

#### 4.16 CONTROLLER ADJUSTMENTS (Ref. Dwg. 100087)

Controller adjustments consist of:

- a. Center frequency adjust.
- b. Two microsecond single-shot adjust.
- c. One microsecond single-shot adjust.

#### 4.16.1 Test Configuration Controller Adjustments

- a. Insert the controller in an S100-bus 8080/Z80 based computer using an extender card.
- b. Connect controller to any Micropolis storage module.

#### 4.16.1.1 Test Procedure, Center Frequency Adjust

- a. Ensure that the drive is not on.
- b. Connect oscilloscope to the oscillator output at A15-7. Set oscilloscope time base to 200 ns/cm.
- c. Measure frequency of oscillator. The center frequency shall be:
  - 970 kHz minimum
  - 1030 kHz maximum
- d. Adjust R40 until the output frequency is 1 MHz.

#### 4.16.1.2 Test Procedure, 2 us Single-Shot Adjust

Perform the center frequency test procedure above, then adjust R40 until the output frequency is 1 MHz.

#### Test Procedure, 2 us Single-Shot Adjust

- a. Insert a diskette in drive.
- b. Position the head to track zero and write a full track of 'ones' data (16 sectors).
- c. Perform a continuous read operation on track zero.
- d. Alternatively select program X14 to achieve Steps b and c.
- e. Connect oscilloscope to A14-5, set time base of oscilloscope to 200 ns/cm, and observe one-shot output. This output shall be:
  - 1.94 us minimum
  - 2.06 us maximum
- f. Adjust R27 for a period of 2 us.

#### 4.16.1.3 Test Procedure 1 us Single-Shot Adjust

- a. Proceed with Steps a through d of Para. 4.16.1.2.

b. Connect oscilloscope to A14-3, set time base of oscilloscope to 200 ns/cm and observe one-shot output. This output shall be:

0.97 usec minimum

1.03 usec maximum

c. Adjust R46 for a period of 1 us.

### TROUBLESHOOTING

#### 5.1 INTRODUCTION

This section contains information useful for isolating a fault first to the system element then to the specific component or subassembly.

#### 5.2 TROUBLESHOOTING, GENERAL INFORMATION

Troubleshooting information for the diskette drive is presented in three tables. In Table 5-1, troubleshooting is defined on a system level where the nature of malfunction does not clearly indicate which system component is at fault. Table 5-1 should be

used only when the fault has not been isolated to either the drive module or the controller. Table 5-2 offers troubleshooting information relevant to the drive module and PCBA. This includes both single and dual units. Table 5-3 provides troubleshooting information for the controller PCBA.

#### NOTE

Before proceeding to component level troubleshooting, substitute a known good drive module cable or controller if available for the suspected malfunctioning unit to verify that the fault is indeed in that unit.

**TABLE 5-1. ISOLATION OF FAULT TO THE SUBSYSTEM COMPONENT**

Symptom	Probable Cause	Action	Reference
On dual module, LED displays go out and stay out when door is closed and motor(s) do not turn. On single modules motor does not rotate.	Interface cable is not connected to controller or controller is not plugged into an operational S100 bus.	Check cable and/or controller. Check for presence of +8V and +16V to controller.	
	Defective drive motor or drive motor circuits.	Troubleshoot drive mechanism.	Table 5-2
	Power supplies internal to drive module are defective.	Check +5V and +12V regulator(s) outputs with door closed.	Table 5-2
Select light(s) is always on.	Interface cable reversed at one end.	Reverse cable.	

**TABLE 5-1. ISOLATION OF FAULT TO THE SUBSYSTEM COMPONENT (Cont'd)**

<b>Symptom</b>	<b>Probable Cause</b>	<b>Action</b>	<b>Reference</b>
Drive motor(s) rotate and select light(s) operate normally but program (Basic or DOS) will not load. The head/positioner does not step or restore.	Defective bootstrap PROMs on controller.	Check controller.	Table 5-3
	Defective controller.	Check controller.	Table 5-3
	Conflict between bootstrap PROM address and other S100 peripherals.	Check memory address of other peripherals. Readdress bootstrap.	
Drive motor(s) rotate and select lights operate normally, however program (Basic or DOS) will not load. The head/positioner steps normally then unloads.	Insufficient RAM memory in computer, memory incompatible with disc subsystem, dirty edge connectors on memory boards, faulty memory.	Clean RAM edge connectors and reseat boards. Ensure that system contains sufficient memory of adequate speed and type. Substitute known good memory.	
Computer hangs up or goes into a loop during a read operation.	No read data output or sector/index output from drive.	Troubleshoot drive.	Table 5-2
	No read or sector output from controller.	Troubleshoot controller.	Table 5-3
Computer goes into a loop when a new diskette is installed.	Other than a 16 sector diskette is installed.	Only 16 sector diskette may be used.	
Two or more drives select at the same time.	Two or more drives have the same address jumpers installed.	Remove incorrect jumper inside the drive modules.	
Drive 1 (single module) or Drive 2/3 will not select after Drive 0 (single module) or Drives 0/1 are removed or turned off.	An add-on, Unit 1 single or 2/3-dual will not operate without Drive 0 or 0/1 connected and turned on due to lack of interface termination.	Connect and turn on terminated module.	
When trying to load a program head continuously restores (buzzes) and the program does not load successfully.	Problem can be in either controller or drive module.	Substitute drive (lower drive on dual) and/or substitute controller.	

**TABLE 5-2. TROUBLESHOOTING THE MODULE**

<b>Symptom</b>	<b>Probable Cause</b>	<b>Action</b>	<b>Reference</b>
Drive motor does not rotate when diskette is installed and door is latched down.	No power to drive.	Check for correct line voltage. Check fuse.	
	Controller is not plugged into an active S100 bus which is operating.	Check for presence of +8V and +16V to controller.	

**TABLE 5-2. TROUBLESHOOTING THE MODULE (Cont'd)**

Symptom	Probable Cause	Action	Reference
	Controller is not connected to drive interface.	Check interface cable.	
	Power supply within drive module is defective.	Check for the presence of +5V at J5-7 for single or J8-7 for dual, and +12V at J5-4 for single and J8-8 for dual at the drive PCBA	
	Drive motor is defective.	Check by substitution or measure motor current by measuring voltage across 1 ohm current limiting resistor (Single = R77 (R83 Single B drive); Dual top drive = R100; Dual lower drive = R139). Nominal head loaded motor turning current is 300 to 500mA rising to 700mA with motor stalled.	
	Drive motor PCBA circuits are defective.	Troubleshoot drive motor circuits.	
	Door open switch is defective.	Check/replace switch	Para. 6.14
Drive motor rotates much more rapidly than 300 rpm.	Intermittent connector on drive motor.	Repair/replace connector.	
	Defective drive motor (open generator).	Replace drive motor.	Para. 6.4
	Failure of PCBA drive servo circuits.	Replace PCBA or troubleshoot servo circuits.	Para. 6.3
Head does not load.	Solenoid is open.	Replace solenoid.	Para. 6.8
	Failure of PCBA head load solenoid circuits.	Replace PCBA or troubleshoot solenoid logic and driver circuit.	
Head never unloads.	Residual solenoid magnetism (Module S/N below 8021000)	Install stainless steel strip on solenoid actuator.	Request PIB 001
	Insufficient spring tension.	Increase spring force by bending spring anchor on solenoid frame.	
	Solenoid driver shorted.	Troubleshoot PCBA driver circuits.	
Positioner (head) missteps, ends up at wrong track.	Positioner stepper motor defective.	Replace positioner.	Para. 6.6
	Positioner binding.	Readjust positioner	Para. 6.6
	Positioner circuits on PCBA failure.	Troubleshoot positioner circuits.	
Diskette slips after door is closed.	Insufficient clamping force. No gap between "C" clip and	Replace plate to ensure a minimum gap of 0.005" when door	

**TABLE 5-2. TROUBLESHOOTING THE MODULE (Cont'd)**

Symptom	Probable Cause	Action	Reference
	top of support plate when door is closed.	is shut and a diskette is in place.	
Diskette jams or miscenters.	Clamp miscentered.	Adjust support bar.	Para. 4.13
	Oxide on clamp or spindle.	Clean with alcohol.	
	Diskette rear stop maladjusted.	Adjust diskette rear stop.	Para. 4.14
	Clamp defective.	Replace clamp.	Para. 6.10
"Crunching" sound heard when closing drive door.	Not enough lubricant on the latch or bezel latch tabs.	Grease latch fingers with heavy weight grease.	
Door will not latch or will not unlatch.	Door latch is defective.	Replace door latch on receiver assembly.	Para. 6.16
Soft (non permanent) READ errors associated with the drive.	Load pad is dirty, loaded with oxide.	Replace load pad using tweezers (remove <i>all</i> gummed backing from old pad).	Para. 6.5
	Head is loaded with oxide.	Scrub head with alcohol (denatured or isopropyl) and dry using Q-tips. Avoid rubbing alcohol.	
	Excessive pulse type noise in read signal (appears as spikes when the read amp test point is viewed by oscilloscope).	Noise may be internally generated—drive motor, faulty power supply regulator. Or externally generated—high bus noise level, noisy cabling, radiating CRT, faulty electrical grounding. Isolate source of noise then repair/replace component.	
	Excessive spindle speed variation.	Check/replace motor. Check/replace drive belt.	Para. 6.4
	Intermittent or marginal component in read circuit.	Troubleshoot read circuits including amplifiers, one shots and input select diodes.	
	Permanent error on diskettes.	Change diskette.	
Write errors associated with the drive.	Load pad or head dirty.	See "soft READ error" above.	
	Intermittent write protect switch.	Check microswitch for noisy contacts. Troubleshoot write protect switch circuits.	Para. 6.13
	Intermittent diode(s) in read/write head switch.	Check diodes.	
	Incorrect erase turn-on/turn-off delays (turn-on approx. 400 us after write begins; turn-off approx. 800 us after write ends).	Check timing relationship between write turn-on/off and erase.	Sec. 3
	Failure in write circuits.	Troubleshoot write logic.	

**TABLE 5-2. TROUBLESHOOTING THE MODULE (Cont'd)**

Symptom	Probable Cause	Action	Reference
	Defective head.	If substitution of PCBA does not correct problem, replace head.	Para. 6.7
Read failure — complete.	Failure of read circuit component.	Check for read data at interface Pin 30. Check for presence of read signal at read test point. (Single: TP3 or 4; Single B drive TP5; Dual: TP12 or 13). Check for presence of read signal at output of first read amp.	
Drive is write protected all the time or does not write protect when write protect tab is installed on diskette.	Write protect circuit.	Check write protect circuits.	Para. 6.13
	Write protect switch failure.	Check/replace write protect switch.	
Drive loses select and/or unit number indicators flash intermittently (dual only).	Intermittent drive unit reversal switch SW1.	Clean with contact cleaner. Replace switch on PCBA.	
Diskette incompatible between drives.	Radial alignment out of alignment.	Adjust radial alignment.	Para. 4.9
	Circumferential alignment out of adjustment.	Adjust circumferential alignment.	Para. 4.8
	Motor speed of drives excessively different from one another.	Check/adjust motor speed.	Para. 4.3
	One of the drives is one full track off track.	Adjust track 0 switch.	Para. 4.10
	Marginal head or marginal read/write circuits in one or both drives.	Troubleshoot read/write circuits. Replace PC board. If problem persists, replace head.	Para. 6.3
	<b>NOTE:</b>		
If a problem exists in one drive only of a dual drive module, then the fault most probably lies in the head.			
	Diskette bowed or marginal.	Try another diskette.	Para. 6.5
	Load pad marginal.	Replace load pad.	

**TABLE 5-3. TROUBLESHOOTING THE CONTROLLER**

Symptom	Probable Cause	Action	Reference
Will not boot. Examination of boot memory address indicates PROM instructions incorrect.	Boot starting address is incorrect.	Check jumpers W1, W2, W3, W4.	
	Defective PROMs C9, C10.	Replace one or both PROMs.	
	Defective 5V regulator VR1 (no 5 volt).	Replace regulator.	

**TABLE 5-3. TROUBLESHOOTING THE CONTROLLER (Cont'd)**

Symptom	Probable Cause	Action	Reference
	PROM is not being addressed.	Troubleshoot circuits associated with PROM addressing: D6, D7, D8.	Sec. 7, Schematic Dwg. 100087
	PROM driver (bus data in) circuits malfunctioning.	Check circuits associated with D11, D12, C8.	
	CPU PRDY line is being held low.	Check PRDY logic D5, D9.	
Will not boot (PROM instruction OK. Drive is selecting and restores to track 0)	Controller read processing circuits are malfunctioning.	Proceed to "Massive read errors or loss of read data" symptom.	
	Sector counter failure.	(Check C3 pins 11, 12, 13, 14 for correct sector count relationship.) Troubleshoot sector counter C1, C2, C3 and D1.	Sec. 7, Schematic Dwg. 100087
Boots intermittently.	Loose PROM or dirty PROM socket.	Replace PROMs/sockets.	
	Temperature sensitive components in read, sector or PROM circuits.	Troubleshoot using vibration or thermal shock.	
Massive data errors or intermittent loss of data.	Failure in Phase-Lock-Loop (PLL) circuits, with continual data input to controller (i.e., consistent read operation), check the PLL center frequency, ¼ cell one shot and ½ cell one shot adjustments (Refer to Test/Adjustment section.)	Readjust as required. (NOTE: If the adjustments cannot be performed, then a failure of the PLL has occurred. Troubleshoot circuits on sheet 9.	Sec. 7, Schematic Dwg. 100087 Sec. 3
	PLL is not tracking data correctly.	Check PLL error voltage.	Sec. 3
	Failure of logic element in data path.	Check circuits shown on sheets 4, 5, 6 of Dwg. 100087.	Sec. 7, Schematic Dwg. 100087
Infrequent data errors attributed to controller.	PLL misadjusted.	Check three PLL adjustments as above.	
	Marginal read path logic element.	Troubleshoot circuits, sheets 4, 5, 6.	Schematic Dwg. 100087
Write failure. Controller/drive will read diskette written using different controller.	Write oscillator is inoperative.	Replace crystal. Troubleshoot oscillator circuits shown on sheet 7.	
	Drive is write protected (controller does not sense write protect status).	Troubleshoot drive.	

**TABLE 5-3. TROUBLESHOOTING THE CONTROLLER (Cont'd)**

<b>Symptom</b>	<b>Probable Cause</b>	<b>Remedy</b>	<b>Reference</b>
	Failure in write logic.	Troubleshoot circuits shown on sheet 3 and flip-flop B2 on sheet 7.	Sec. 7, Schematic Dwg. 100087
One or more drives will not select.	Failure in select logic.	Troubleshoot circuits on sheet 2 and on sheet 8 associated with element B3, B4, B4.	

### PARTS REMOVAL AND REPLACEMENT

#### 6.1 INTRODUCTION

This section provides the procedures necessary to replace subassemblies and parts of single and dual subsystem drive modules. The procedures are arranged in a sequence that first details the replacement of a complete drive mechanism, then the replacement of the PCBA, and finally the replacement of individual subassemblies and components. Wherever applicable, references are made to Section 4 for adjustments and tests that must be made to ensure that the drive module will function correctly when returned to service. The adjustment and test requirements are simplified by using partially assembled and aligned subassemblies as replacements instead of attempting individual replacement of parts such as lead screws and bearings. Illustrations are included where needed to clarify the procedures. The tools required are listed in Section 1.

#### 6.2 REPLACING THE DRIVE MECHANISM AS AN ASSEMBLY

The drive mechanisms used in both the single and dual modules differ only by two PCBA mounting supports present in single modules. MOD I (48TPI) and MOD II (100TPI) mechanisms differ by the positioner lead screw, the read/write head, and minor PCBA differences. The drive mechanisms are easily removed from the module for repair and/or replacement.

Replacement procedures for single and dual modules are not identical. Access to the drive mechanism in a single subsystem is gained by first removing the cover, then disconnecting each of connectors J2 and J5. Removing the three screws mounting the mechanism to the chassis bottom allows the mechanism, with PCBA, to be removed. In the dual subsystem, the PCBA is secured to mounting rails on the left of the two drive mechanisms, and does not affect upper drive mechanism replacement. The PCBA must, however, be removed to replace the lower drive mechanism.

##### 6.2.1 Single Subsystem with Power Supply (Models 1022, 1023, 1027, 1042, 1043)

###### 6.2.1.1 Removal

- a. Disconnect electrical power from drive module.
- b. Disconnect interface cable from controller.
- c. Remove seven cover-securing screws, then remove cover from drive module chassis.
- d. Disconnect J5 10-pin and J2 5-pin power connector from PCBA rear (Figure 6-1).
- e. While holding drive mechanism, remove three screws securing the mechanism to the bottom of the enclosure.
- f. Remove drive mechanism from module chassis.

**6.2.1.2 Installation**

Install the drive mechanism by reversing the removal procedure (Para. 6.2.1.1).

**CAUTION**

EXERCISE EXTREME CARE WHILE REPLACING COVER, NOT TO PINCH FRAGILE HEAD CABLE BETWEEN COVER AND CHASSIS.

**6.2.2 Single Subsystem Without Power Supply (Models 1021, 1041)**

**6.2.2.1 Drive Mechanism Removal**

- a. Disconnect DC power from drive module.
- b. Disconnect interface cable from controller.

- c. Remove upper three screws on each side (6 total) and remove cover with an upward and slightly backward motion.
- d. Remove lower two screws on each side (4 total) securing drive to chassis (Figure 6-2).
- e. Remove drive mechanism.

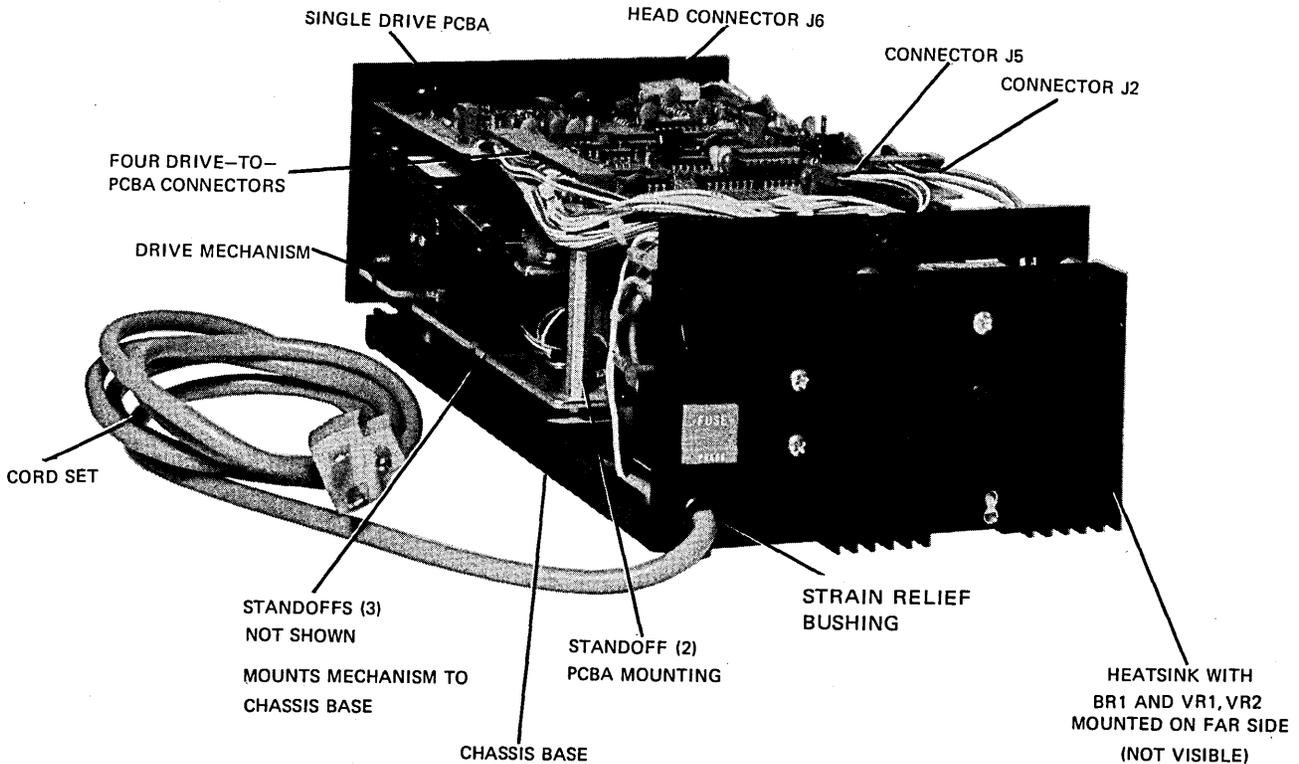
**6.2.2.2 Installation**

- a. Install drive mechanism in chassis by reversing removal procedure.
- b. Install cover by lowering cover onto unit from above in approximately correct location. Do not try to slide cover on from the rear.

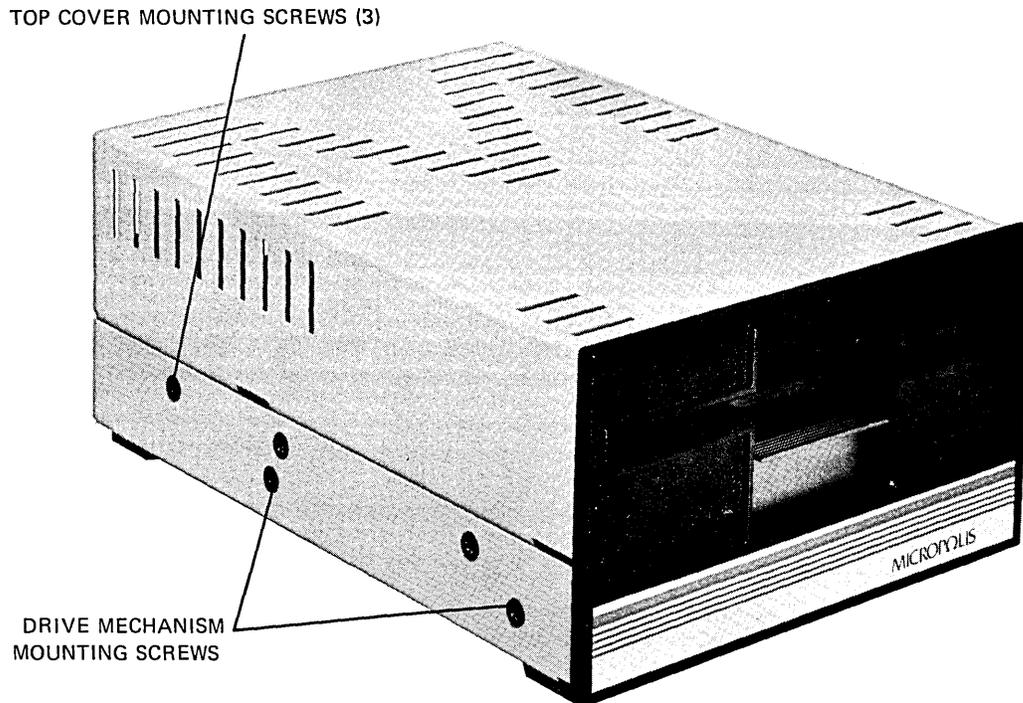
**CAUTION**

EXERCISE CAUTION IN REPLACING COVER. *DO NOT* PINCH HEAD CABLE BETWEEN COVER AND CHASSIS.

ENSURE THAT SUBASSEMBLY CABLES ARE DRESSED TO CLEAR COVER AND DO NOT BECOME TRAPPED.



**Figure 6-1. Single Drive with Power Supply, Rear View**



**Figure 6-2. Single Drive Assembly Without Power Supply**

## 6.2.3 Dual Subsystem

### 6.2.3.1 Removal of Top Drive Mechanism

- a. Disconnect electrical power from drive module.
- b. Disconnect interface cable from controller.
- c. Remove drive mechanism rear screw located between drive motor and positioner (Figure 6-3).
- d. Remove two drive mechanism side mounting screws securing mechanism to side rails (Figure 6-4).

#### NOTE

The drive mechanism screw on PCBA side is accessed through hole in PCBA.

#### CAUTION

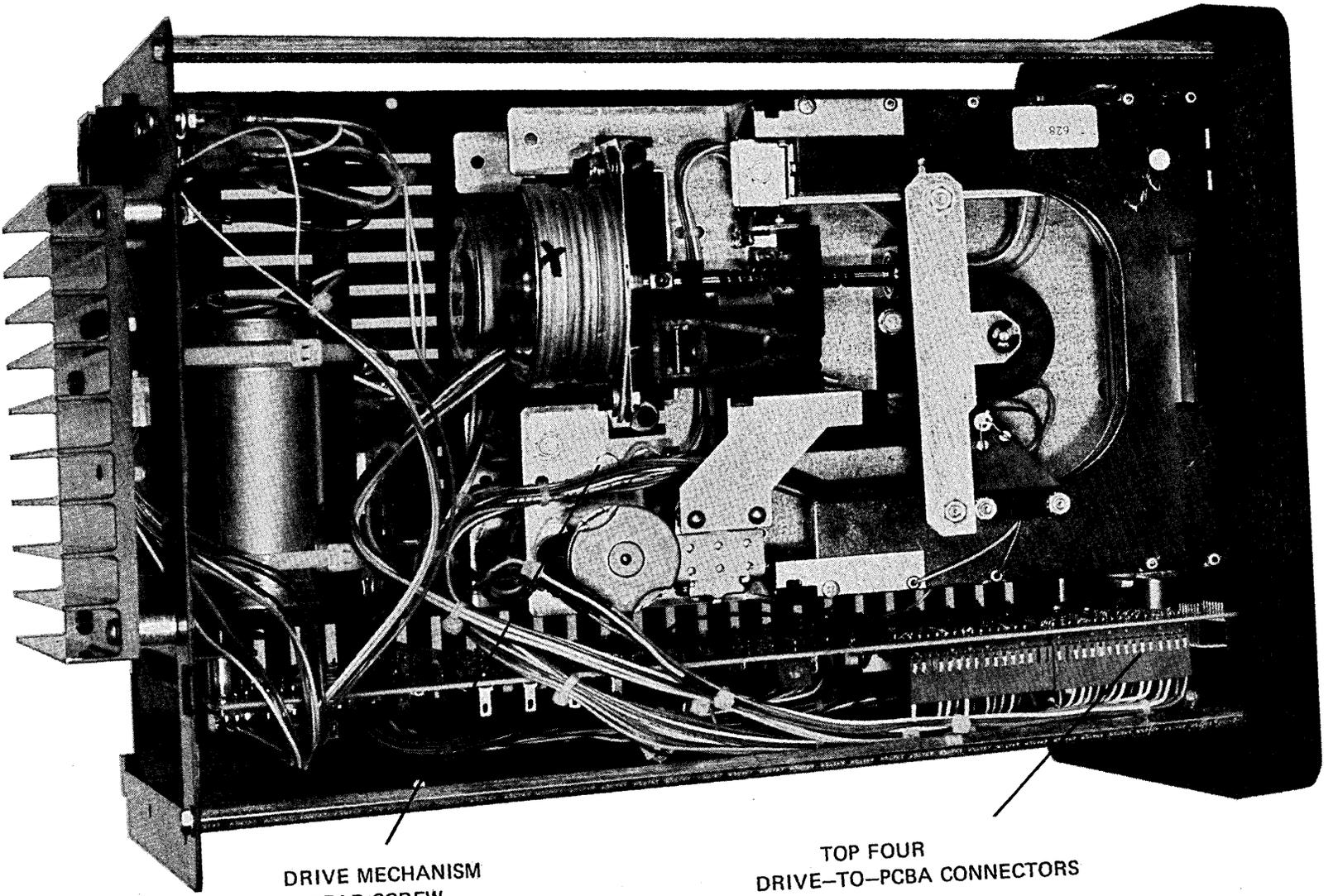
DURING FOLLOWING STEP, HANDLE HEAD CONNECTOR & CABLE

CAREFULLY BECAUSE IT IS FRAGILE AND IRREPARABLE.

- e. Disconnect head connector from PCBA connector P6 (Figure 6-5).
- f. Note location and orientation of top four drive-to-PCBA connectors, then disconnect from PCBA (Figure 6-5).
- g. Remove drive mechanism from side rails (Figure 6-4) with a rearward motion. If necessary, spread rails slightly outward to enable removal.

### 6.2.3.2 Installation of Top Drive Mechanism

- a. Spread side rails slightly outward, then slide drive mechanism from the rear into the cutout in bezel.
- b. Reverse procedures of Para. 6.2.3.1, Steps a through d, ensuring that drive is seated in bezel. Tighten rear screw first.
- c. Observing caution preceding Para. 6.2.3.1, Step e, mate head connector with PCBA connector P6.



DRIVE MECHANISM  
REAR SCREW

TOP FOUR  
DRIVE-TO-PCBA CONNECTORS

Figure 6-3. Dual Drive Top View, Cover Removed

### 6.2.3.3 Removal of Lower Drive Mechanism

Before performing the following procedures, remove the top drive mechanism (Para. 6.2.3.1) and the PCBA (Para. 6.3.2.1).

- a. Remove two drive mechanism side screws securing mechanism to side rails.
- b. Remove rear hex post located between drive motor and positioner (Figure 6-4).
- c. Remove drive mechanism with a rearward motion from side rails. If necessary, spread rails slightly outward to enable removal.

### 6.2.3.4 Installation of Lower Drive Mechanism

After performing the following procedures, install the PCBA (Para. 6.3.2.2) and top drive mechanism (Para. 6.2.3.2).

- a. Spread side rails slightly outward, then slide drive mechanism from the rear into cutout in bezel.
- b. Reverse procedures of Para. 6.2.3.3, Steps a and b, ensuring that the drive is seated in the bezel. Tighten the hex post first.

## 6.3 PCBA REPLACEMENT

The single subsystem PCBA (Figure 6-1) is mounted on the top of the drive mechanism; the dual subsystem PCBA (Figure 6-5) is mounted on the inside of the enclosure to the left of the drive mechanisms.

When a replacement PCBA is installed in either subsystem, drive motor speed and positioner timing and read amplifier gain must be adjusted in accordance with the procedures referenced in Para. 6.3.1.2, Step f, and 6.3.2.2, Step d.

### 6.3.1 Single Subsystem (All Models)

#### 6.3.1.1 Removal (Refer to Figure 6-1)

- a. Note location and orientation of four drive-to-PCBA connectors, then disconnect from PCBA.

#### CAUTION

DURING THE FOLLOWING TWO STEPS, HANDLE THE HEAD CONNEC-

TOR CABLE CAREFULLY BECAUSE IT IS FRAGILE AND IRREPARABLE.

- b. After noting location of tie wrap securing head connector cable to PCBA, cut tie wrap.
- c. Disconnect head connector from PCBA connector J6.
- d. Remove two PCBA mounting screws, then remove PCBA.

### 6.3.1.2 Installation

- a. Position PCBA so that it is supported between fingers on bezel.
- b. Install two PCBA mounting screws. Note in some cases a grounding lug may be present under one of the screws. Ensure that the lug is rotated so as to clear all etch before tightening.
- c. Observing caution of preceding Para. 6.3.1.1, Step b, mate head connector with PCBA connector J6.

#### CAUTION

DURING THE FOLLOWING STEP, LEAVE THE TIE WRAP LOOSE TO PREVENT CRUSHING THE HEAD CONNECTOR CABLE.

- d. Install tie wrap around head connector cable, locating it as noted in Para. 6.3.1.1, Step b.
- e. Mate four drive-to-PCBA connectors with PCBA, orienting as noted in Para. 6.3.1.1, Step a. Note that on 100164 PCBA there is one extra pin on P4 (mate to J4) nearest the *front* of the PCBA.
- f. Perform following procedures in order listed:

Procedure	Para No.
Drive motor speed	4.3
Positioner timing	4.5
Read amplifier gain	4.6

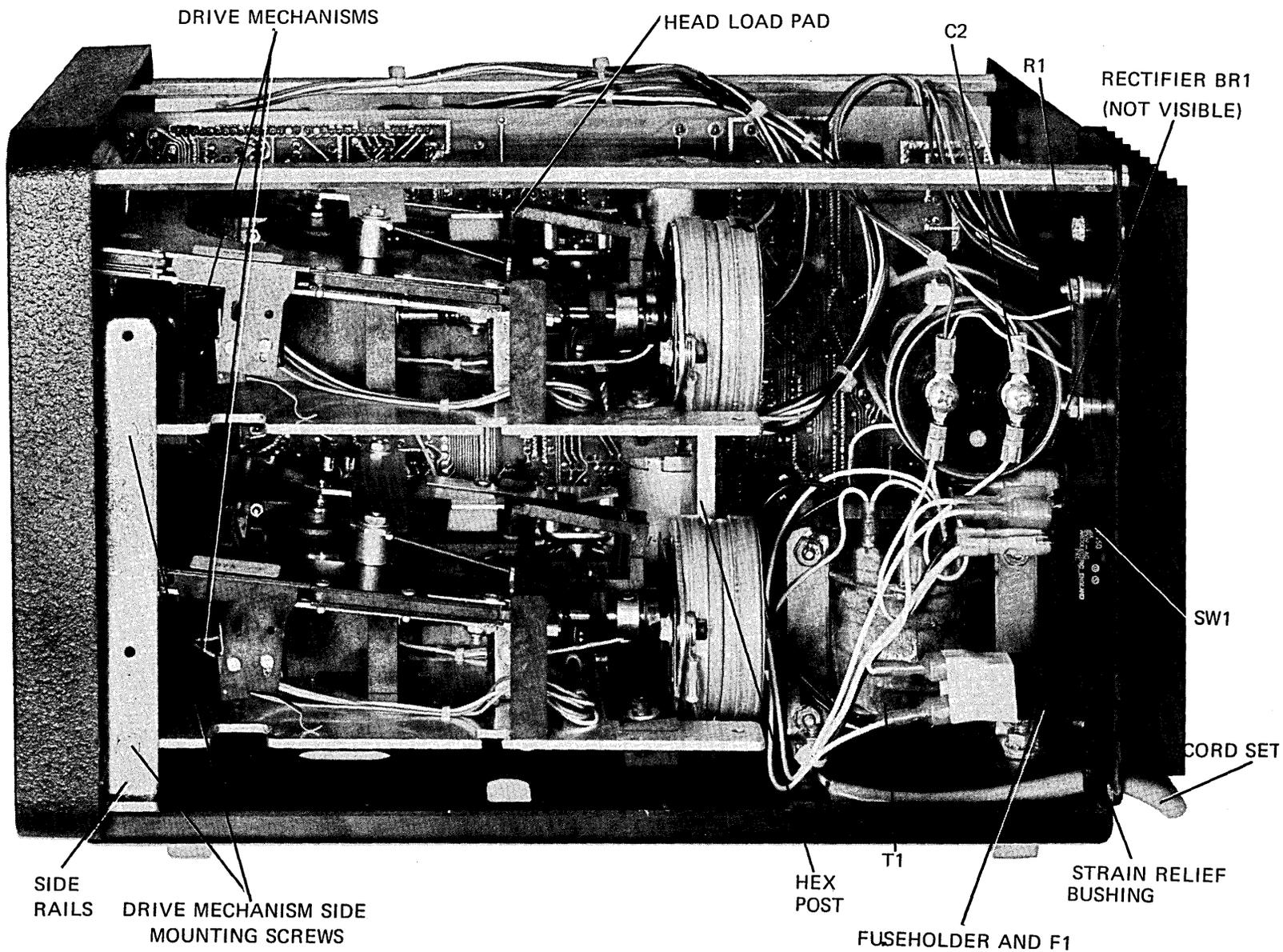
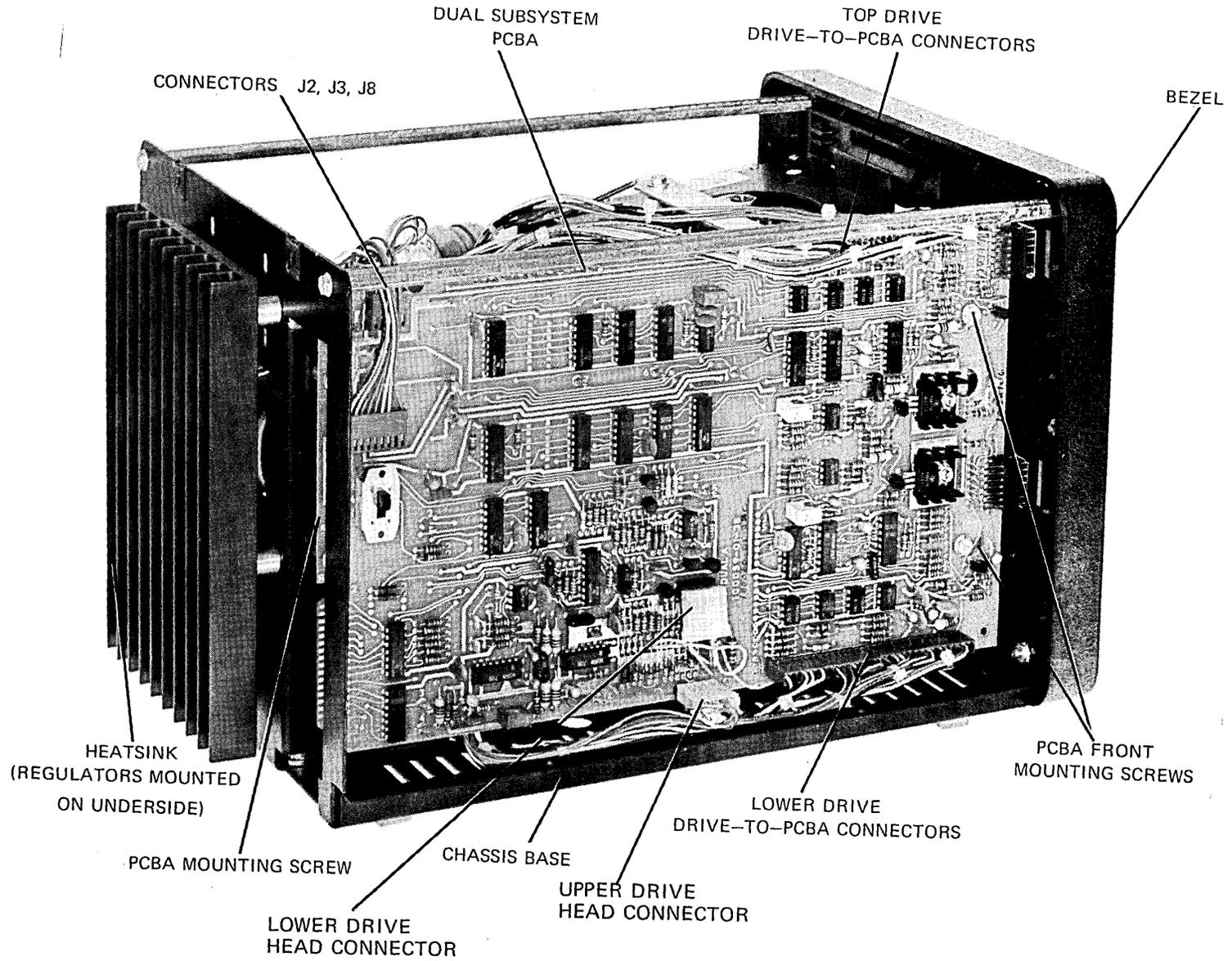


Figure 6-4. Dual Drive Side View, Right Side

Figure 6-5. Dual Drive Side View, Left Side



### 6.3.2 Dual Subsystem, All Models

#### 6.3.2.1 Removal ((Refer to Figure 6-5)

- a. Note location and orientation of eight drive-to-PCBA connectors (four top and four lower connectors), then disconnect from PCBA.
- b. Disconnect two power connectors from PCBA.

#### CAUTION

DURING THE FOLLOWING STEP, HANDLE THE HEAD CONNECTOR CABLES CAREFULLY BECAUSE THEY ARE FRAGILE AND IRREPARABLE.

- c. Disconnect head connectors from PCBA connectors J6 and J7.
- d. Remove two rear and two front PCBA mounting screws, then remove PCBA.

#### 6.3.2.2 Installation

- a. Position PCBA against its mounting bracket.
- b. Install two front and two rear mounting screws.
- c. Observing caution preceding Para. 6.3.2.1, Step c, mate two head connectors with PCBA connectors as follows:

Top drive mechanism head connector with J6 (lower connector)

Lower drive mechanism head connector with J7 (upper connector)

- d. Install the eight drive to PCBA connectors oriented as noted in Para. 6.3.2.1.
- e. Mate two power connectors at the rear of PCBA; the four-wire connector may be mated with J2 or J3 (Figure 6-5).
- f. Perform three following procedures in order listed:

Procedure	Para No.
Drive motor speed/ISV	4.3
Positioner timing	4.5
Read amplifier gain	4.6

### 6.4 DRIVE MOTOR AND BELT REPLACEMENT

The drive motor and belt (Figure 6-6) are accessible after the drive mechanism is removed from the drive module.

#### 6.4.1 Removal (Refer to Figure 6-6)

Two mounting screws secure the drive motor to the chassis. On some drive mechanisms one of these screws secures a drive motor ground lug, on others the lug is secured by a third screw; when removing the drive motor from one of the latter mechanisms, remove the third screw before removing the motor mounting screws.

In addition, when one of the motor mounting screws secures a ground lug, the motor is insulated from the chassis by a plastic disk and two insulating shoulder washers; retain them for use during installation.

#### CAUTION

DURING THE FOLLOWING STEP, DO NOT STRETCH OR KINK THE DRIVE BELT BECAUSE SUCH DAMAGE WILL ADVERSELY AFFECT THE DRIVE MECHANISM'S OPERATION.

- a. Slip drive belt off large pulley and remove from drive motor pulley. Retain belt if acceptable for reuse. Note which surface of the belt is in contact with the pulley.
- b. While holding drive motor, remove two mounting screws.
- c. Remove drive motor from chassis.

#### 6.4.2 Installation

If the drive mechanism includes a plastic insulator and two shoulder washers (Para. 6.4.1), install as instructed in the parenthetical parts of the following steps (see Figure 6-7).

- a. Hold drive motor (and plastic insulator) against chassis.
- b. Install right side motor mounting screw (and shoulder washer).
- c. If drive motor ground lug is secured by left side motor mounting screw, install screw through lug (and shoulder washer), then install.

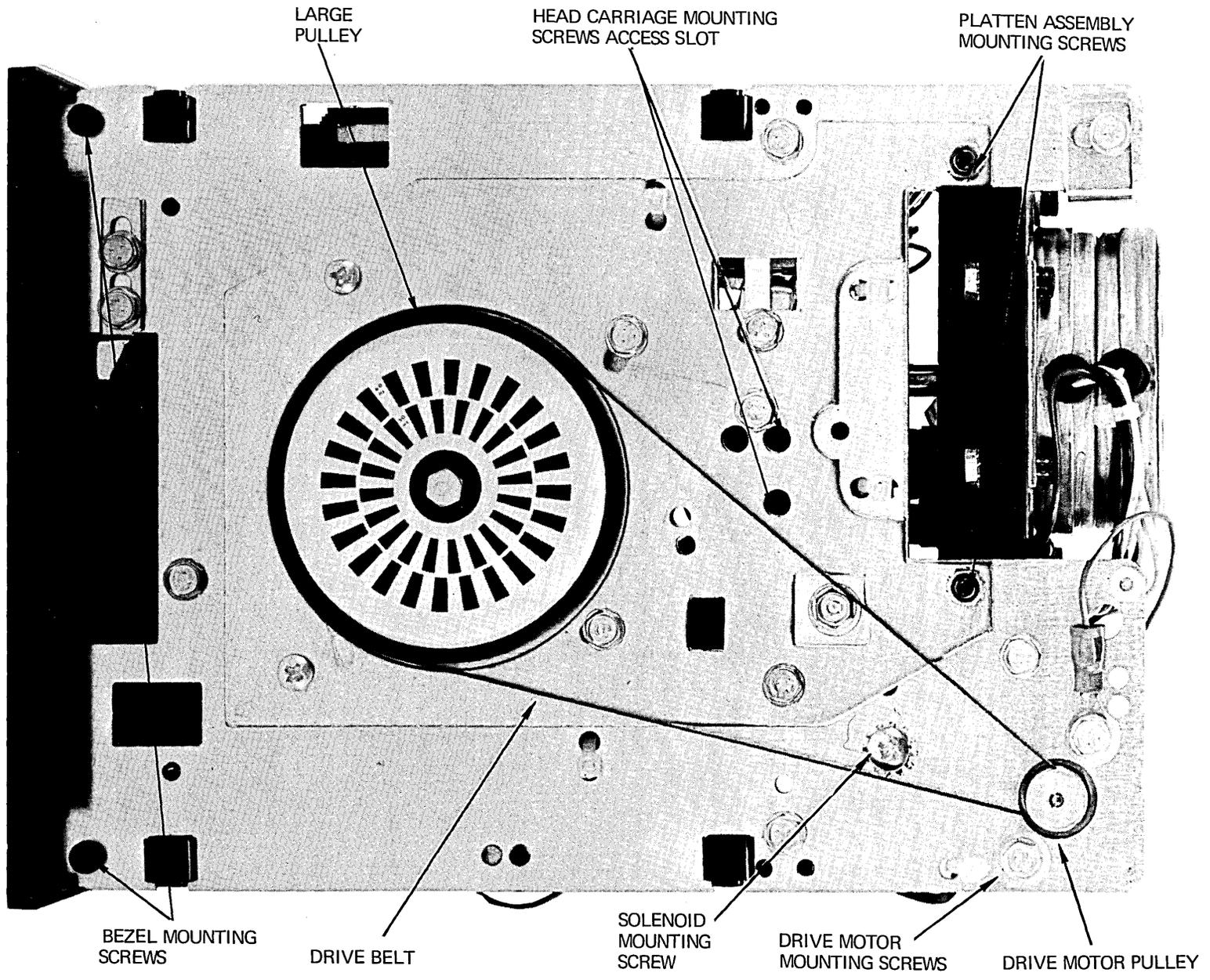


Figure 6-6. Drive Mechanism, Bottom View

- d. If drive motor ground lug is secured by third screw, position lug against chassis and secure with screw.
- e. Place drive belt over drive motor pulley (Figure 6-6), then rotate large pulley while slipping belt over it. Ensure correct surface of belt is in contact with pulley (see Para. 6.4.1, Step a).
- f. Perform drive motor speed/ISV procedures (para. 4.4).

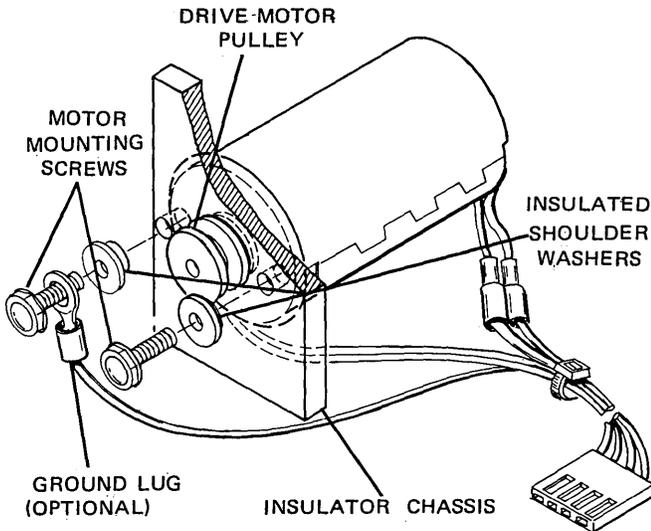


Figure 6-7. Drive Motor Installation

## 6.5 HEAD LOAD PAD REPLACEMENT

The head load pad (Figure 6-8) is secured to the head load arm by a double-sided adhesive. It is accessible on a single subsystem when the PCBA is removed from the drive mechanism (Para. 6.3.1), while on a dual subsystem the upper drive is accessible but the upper drive has to be removed from the enclosure (Para. 6.2.2) to access lower drive.

### 6.5.1 Removal

- a. Position head carriage assembly to the middle of its stroke.
- b. Pivot head load arm up until it is vertical and hold it in this position, using care not to allow spring or pins to slip out of place.
- c. Using tweezers, carefully remove old head load pad from arm. Adhesive will usually remain stuck to arm. Use caution not to damage load arm.

- d. Remove all adhesive from arm.
- ### 6.5.2 Installation

- a. Being careful not to touch adhesive, peel protective strip from back of replacement load pad.

### CAUTION

DURING THE FOLLOWING STEP, MAKE SURE THAT PAD IS FLAT. AN OFF-CENTER AND/OR OFF-LEVEL PAD WILL CAUSE DATA ERRORS.

- b. Position pad in load arm recess, then use a flat tool to press it into place.
- c. Lower load arm to solenoid plate.
- d. Check Read Amplifier Gain, Para. 4.6 and Compliance, Para. 4.7.

## 6.6 POSITIONER SUBASSEMBLY REPLACEMENT

The positioner subassembly (Figure 6-8) consists of a positioner motor, head carriage, and lead screw. The positioner is stocked with head/carriage already installed and tested to simplify replacement

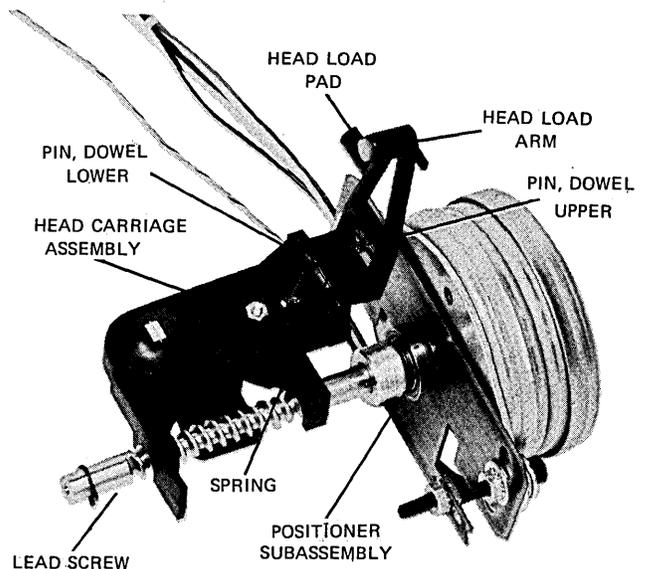


Figure 6-8. Head and Positioner Assemblies

and minimize the number of adjustments. If this procedure is followed only the six procedures listed in Para. 6.6.2, Step h, must be performed. The positioner subassembly is accessible on a single subsystem when the PCBA is removed (Para 6.3.1), and on a dual subsystem when the drive mechanism is removed from the enclosure (Para. 6.2.2).

**6.6.1 Removal**

**NOTE**

Do not loosen the two allen head screws that secure the positioner mounting block to the chassis. If the mounting block is not moved, the lengthy positioner mechanical alignment procedure may not be necessary.

**CAUTION**

DURING THE FOLLOWING STEP, HANDLE THE HEAD CONNECTOR CABLE CAREFULLY BECAUSE IT IS FRAGILE AND IRREPARABLE.

- a. Note routing of head connector cable and location of sleeving and tie wraps, then cut tie wraps and free cable from drive mechanism.
- b. Rotate lead screw until head carriage is fully forward (away from positioner motor).
- c. Loosen and rotate positioner stop bracket out of the way.
- d. Remove two positioner mounting screws located at the rear of the positioner (Figure 6-6).
- e. Move positioner subassembly away from spindle housing until lead screw clears spindle bearing (Figure 6-9).
- f. Remove positioner subassembly carefully from drive mechanism (Figure 6-8).

**6.6.2 Installation**

- a. Place positioner subassembly on chassis near its installed position, but without insert-

ing lead screw in spindle housing.

- b. Observing caution preceding Para. 6.6.1, Step a, route head cable and install tie wraps over sleeving as noted in that step. Make sure service loop is left at head end.
- c. Rotate lead screw until head carriage just clears retaining ring at spindle housing end of lead screw.

**CAUTION**

DURING THE FOLLOWING STEP, FORCE IS NOT NEEDED. IF THE POSITIONER ASSEMBLY DOES NOT SLIP INTO POSITION EASILY, IT IS NOT CORRECTLY ALIGNED WITH ADJACENT PARTS OR THE SPINDLE HOUSING BEARING. USING FORCE WILL DAMAGE THE DRIVE MECHANISM.

- d. Make sure projection on head load arm will be above solenoid activator arm, then insert lead screw into spindle housing bearing.
- e. Install two positioner mounting screws. Do not tighten.
- f. Adjust positioner subassembly to obtain as accurate a side-to-side centering as possible, then tighten mounting screws.
- g. If necessary, apply grease to lead screw.
- h. Using diagnostic program test, check for misstepping; correct if necessary by performing positioner mechanical adjustment (Para. 4.12).
- i. Perform following procedures in order listed:

<b>Procedure</b>	<b>Para. No.</b>
Radial alignment	4.9
Circumferential and azimuth alignment	4.8
Track zero switch and stop alignment	4.9
Radial alignment (2nd time)	4.9
Read amplifier gain adjustment	4.6
Head compliance test	4.7

- j. Reposition and tighten the positioner stop bracket.

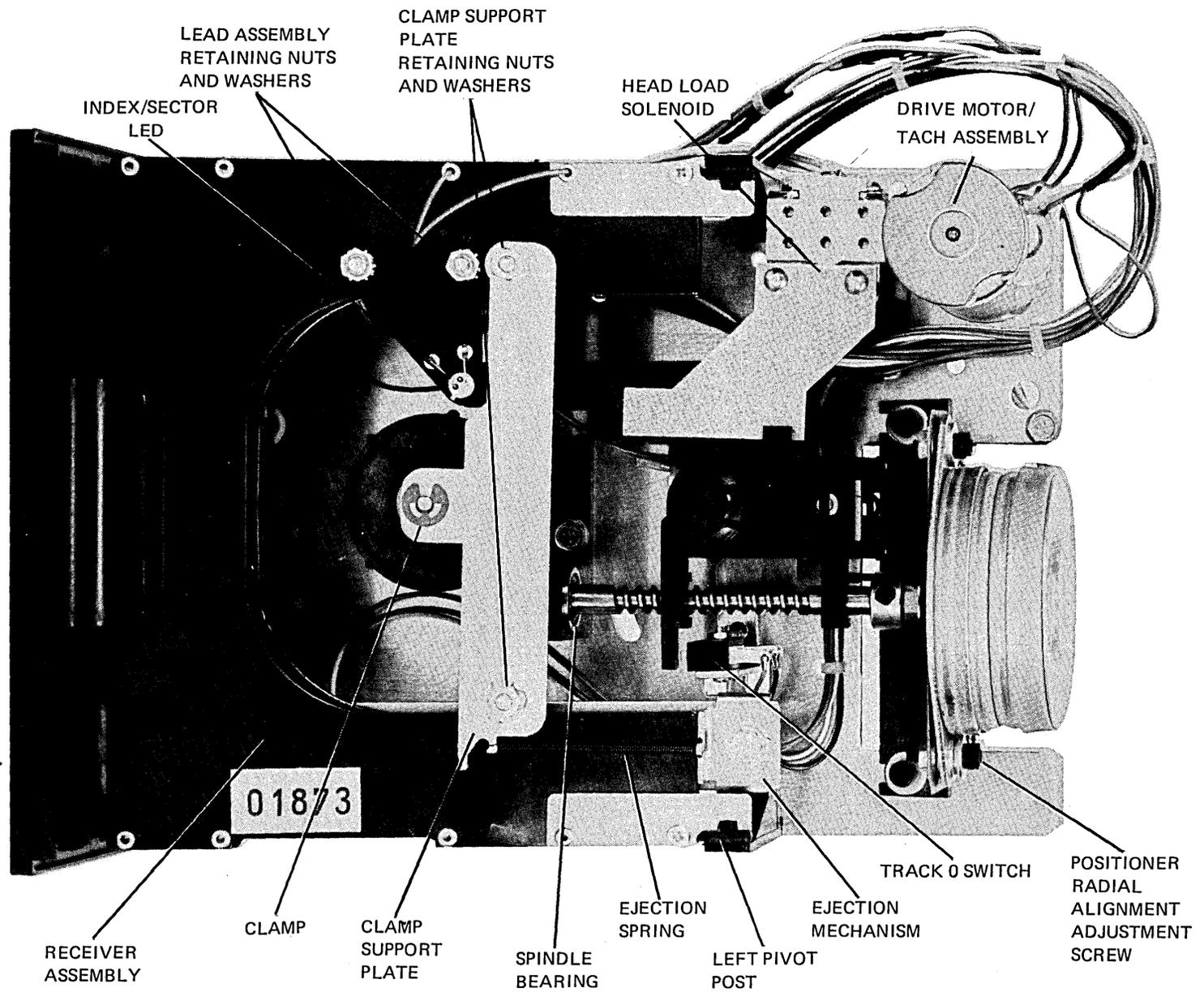


Figure 6-9. Single Drive, Top View, PCBA Removed

## 6.7 HEAD REPLACEMENT

The head (Figure 6-8) is replaced by replacing the head carriage, which is accessible on a single subsystem when the PCBA is removed (Para. 6.3.1), and on a dual subsystem when the drive mechanisms are removed from the enclosure (Para. 6.2.2).

### NOTE

It is easier to replace the entire positioner, with head installed, as detailed in Para. 6.6.

#### 6.7.1 Removal

- a. Rotate lead screw until head carriage is positioned so that its three mounting screws are visible through head carriage mounting screws access holes in chassis (Figure 6-6).
- b. Remove mounting screws by inserting hex key through each hole in turn.

### CAUTION

DURING THIS OPERATION SUPPORT THE CARRIAGE FIRMLY TO ABSORB THE FORCES CAUSED BY REMOVING THE SCREWS.

Use tweezers to remove screws; holes are too small to pass them.

- c. Remove head carriage spring plate.

### CAUTION

DURING THE FOLLOWING STEP, HANDLE THE HEAD CONNECTOR CAREFULLY BECAUSE IT IS FRAGILE AND IRREPARABLE.

- d. Note routing of head connector cable and location of sleeving and tie wraps, then cut tie wraps and free cable from drive mechanism.
- e. Lift head carriage from lead screw and remove from drive mechanism.

#### 6.7.2 Installation

- a. If replacement head/carriage includes spring plate, note quantity and location of at-

taching hardware; remove and retain hardware.

- b. Place head/carriage on lead screw so that projection on head load arm is above solenoid activator arm and holes for spring plate are aligned with access holes in chassis.
- c. Install flat washers on screws as noted in Step a above.
- d. Position spring plate under lead screw and against head carriage, then use tweezers to hold screws in place.
- e. Insert hex key through access hole and install screw. Observe CAUTION of Para. 6.7.1, Step b.
- f. Repeat step e for two remaining screws. Check that spring is perpendicular to carriage and readjust if necessary.
- g. Observing CAUTION preceding Para. 6.7.1, Step d, route cable and install tie wraps over sleeving as noted in that step. Make sure service loop is left at head end.
- i. Manually rotate lead screw. Head carriage should move smoothly on lead screw but not be so loose that spring plate does not hold carriage against lead screw.
- j. Perform following procedures in order listed:

Procedure	Para No.
Radial alignment	4.9
Circumferential and azimuth alignment	4.8
Track zero switch and stop alignment	4.10
Radial alignment (2nd time)	4.9
Track zero switch and stop alignment (2nd time)	4.10
Read amplifier gain adjustment	4.6
Head compliance test	4.7

## 6.8 HEAD LOAD SOLENOID REPLACEMENT

The head load solenoid (Figure 6-9) is secured to the chassis by a single screw and external-tooth lockwasher. Two wires connect it to the PCBA. The solenoid is accessible after the drive mechanism is removed from the drive module.

### 6.8.1 Removal

- a. Unsolder wires from solenoid terminals.
- b. Remove solenoid mounting screw (Figure 6-6), then slide solenoid sideways out of drive mechanism.

### 6.8.2 Installation

- a. Lift head load arm and slide solenoid into position on chassis.
- b. Align solenoid mounting hole and key with respective holes in chassis.
- c. Install mounting screw and lockwasher.
- d. Solder wires to solenoid terminals.
- e. Check freedom of solenoid action by manually operating solenoid plate.

## 6.9 SPINDLE AND PULLEY REPLACEMENT

The spindle and pulley (Figure 6-6) are secured to each other by a single pulley retaining screw; the spindle and spindle housing are secured to the chassis by two screws. The pulley and spindle are accessible after the drive mechanism is removed from the drive module in a single or dual module.

### 6.9.1 Removal

#### CAUTION

DURING THE FOLLOWING STEP, DO NOT STRETCH OR KINK THE DRIVE BELT BECAUSE SUCH DAMAGE WILL ADVERSELY AFFECT THE DRIVE MECHANISM'S OPERATION.

- a. Slip drive belt off large pulley and remove from drive motor pulley. Note which side of the belt is in contact with the pulley.
- b. While holding the large pulley with one hand remove large pulley mounting screw, then remove large pulley.
- c. On the top of receiver remove two clamp support plate retaining nuts and washers (Figure 6-9).
- d. Disconnect ejection spring from clamp support plate, then remove clamp support plate

with clamp attached (Figure 6-9) from drive mechanism.

- e. Remove two (on some models there are three screws) spindle retaining screws and remove spindle and spindle housing (Figure 6-10) from drive mechanism by raising the housing from the base plate and sliding it towards the bezel (toward front of unit) to clear the lead screw.

### 6.9.2 Installation

- a. Slide housing over the end of the lead screw. Align spindle housing mounting holes and key with respective holes in chassis.
- b. Install two (three) mounting screws and tighten securely.
- c. Install clamp support plate (with clamp) and secure with two flat washers and nuts.
- d. Install ejection spring.
- e. Perform clamp and support plate check and adjustment procedure (Para. 4-14).
- f. Place large pulley against spindle and install retaining screw.
- g. Place drive belt over drive motor pulley, then rotate large pulley while slipping belt over it. Ensure that the correct side of the belt is in contact with the pulley (see Para. 6.9.1, Step a).
- h. Perform the following procedures in the order listed:

Procedure	Para No.
Circumferential and azimuth alignment	4.8
Radial alignment	4.9
Track zero switch and stop alignment	4.10

### 6.10 CLAMP REPLACEMENT

The clamp and clamp support plate (Figure 6-10) are secured to the drive mechanism by two nuts and flat washers, and are replaced as an assembly. They are accessible on a single subsystem after the PCBA is

removed and on a top drive of a dual subsystem with the drive mechanism installed in the drive module; on a lower drive of a dual subsystem, the drive mechanism must be removed from the drive module.

#### **6.10.1 Removal**

- a. Remove two clamp support plate retaining nuts and washers (Figure 6-9).
- b. Disconnect ejection spring (Figure 6-9) from plate, then remove plate (with clamp) from drive mechanism.

#### **6.10.2 Installation**

- a. Install clamp support plate (with clamp) and secure with two flat washers and nuts.
- b. Install ejection spring.
- c. Perform clamp and support plate check and adjustment procedure (Para. 4-14).

### **6.11 INDEX/SECTOR LED REPLACEMENT**

The index/sector LED (Figure 6-9) is part of an assembly that consists of a LED bracket and the LED. The assembly is secured to the diskette receiver by two nuts and lockwashers. It is accessible on a single subsystem with the PCBA removed and on a top drive of a dual subsystem with the drive mechanism installed in the drive module; on a lower drive of a dual subsystem, the upper drive mechanism must be removed from the drive module.

#### **6.11.1 Removal**

- a. Remove two LED assembly retaining nuts and washers.
- b. Note wire colors going to the two terminals.
- c. Unsolder wires from the terminals.
- d. Remove LED assembly from drive mechanism.

#### **6.11.2 Installation**

- a. Solder the two wires to feed-through terminals on bracket as noted in Para. 6.11.1, Step b.

- b. Route wires through notch on underside of bracket, then install bracket over studs and secure with two washers and nuts.

### **6.12 INDEX/SECTOR PHOTO CELL REPLACEMENT**

The index/sector photo cell (Figure 6-10) is part of an assembly that consists of a platen and the photo cell. The assembly is secured to the drive mechanism chassis by two screws. It is accessible when the drive mechanism is removed from the drive module.

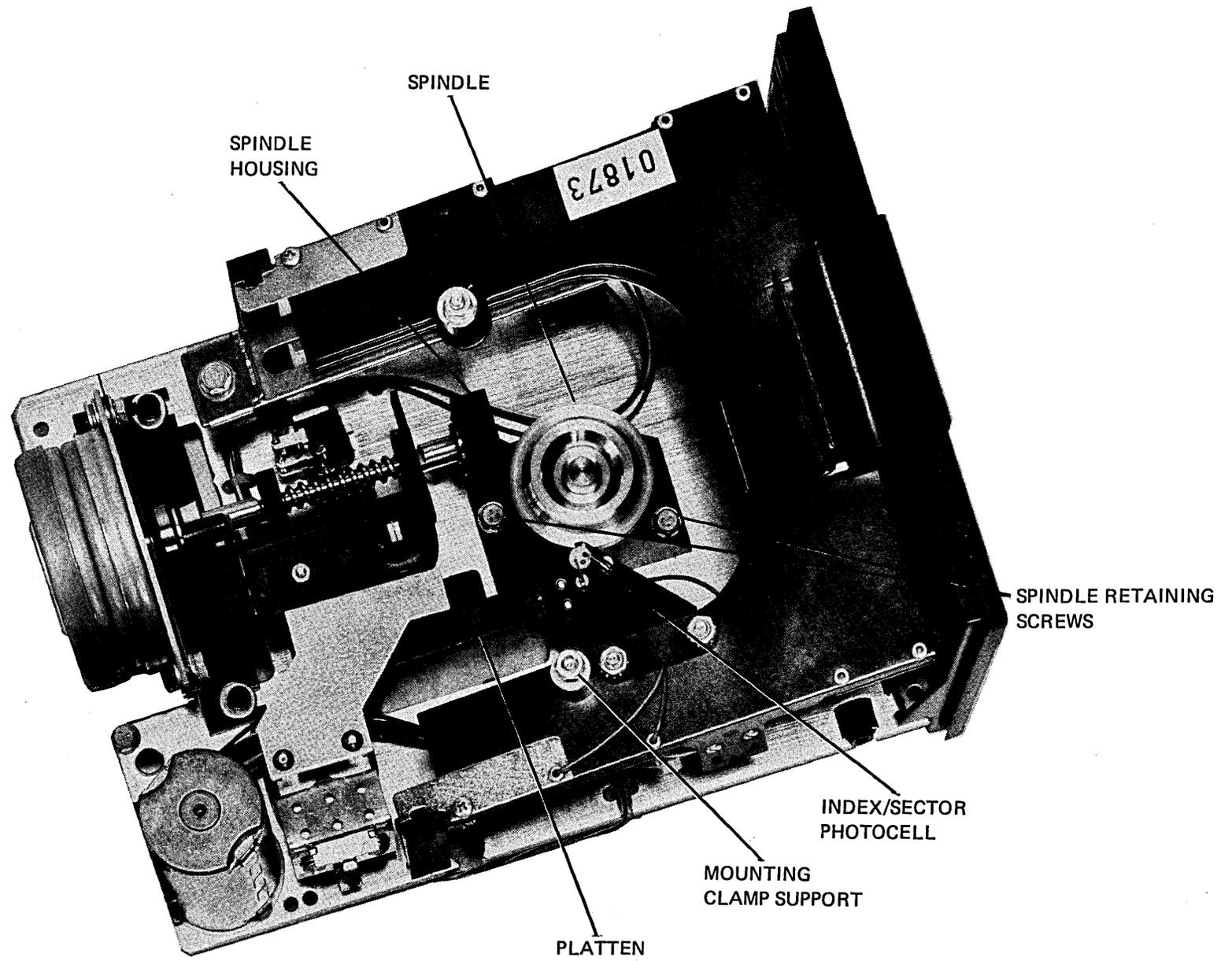
#### **6.12.1 Removal**

- a. While holding platen, remove two mounting screws.
- b. Slide platen toward side of chassis until it is freed from head carriage and spring plate.
- c. Tilt platen and slide it out between receiver and chassis.
- d. Unsolder insulated wires from the two terminals on platen.
- e. Remove platen from drive mechanism.

#### **6.12.2 Installation**

- a. Solder blue wire to terminal that is closest to spindle housing.
- b. Solder green wire to remaining terminal.
- c. Lubricate both sides of platen lip with lubricant (Para. 1.8).
- d. Tilt platen and slide it onto chassis.
- e. Position platen so that photo cell is toward front of drive mechanism, spring plate on the head carriage assembly (Figure 6-8) is below platen's lip and head carriage is above it, and platen mounting holes are aligned with holes in chassis.
- f. Make sure head connector cable is not underneath platen, then install platen mounting screws.
- g. Perform circumferential alignment (Para. 4.8).

Figure 6-10. Single Drive, Top View, PCBA and Clamp Assembly Removed



## 6.13 WRITE PROTECT SWITCH REPLACEMENT

The write protect switch (Figure 6-11) is secured to a tab on the drive motor side of the receiver by two screws, lockwashers, and nuts. It is accessible when the drive mechanism is removed from the drive module.

### CAUTION

WHEN PERFORMING THE FOLLOWING PROCEDURES, DO NOT STRESS THE FRAGILE TAB IN WHICH THE SWITCH IS MOUNTED. IF THE TAB IS DAMAGED, THE ENTIRE RECEIVER MUST BE REPLACED.

#### 6.13.1 Removal

- a. Support receiver tab and remove two write protect switch retaining screws and lockwashers. If necessary, use long nut driver to hold nuts. Retain flat washers installed between tab and switch (if used).
- b. Note color coding of wire connected to each switch terminal, then unsolder wires.
- c. Remove switch from drive mechanism.

#### 6.13.2 Installation

- a. Observing connections noted in Para. 6.13.1, Step c, solder three wires to switch terminals.
- b. Insert two screws through receiver tab, then install two flat washers (if used) on each screw.
- c. Install switch on two screws, making sure switch actuator is inside notch in receiver.
- d. Loosely install lockwasher and nut on each screw.
- e. Perform write protect switch test/adjustment procedure (Para. 4.13).

## 6.14 DOOR OPEN SWITCH REPLACEMENT

The door open switch (Figure 6-12) is secured to a tab on the diskette ejector side of the receiver by two screws, lockwashers, and nuts. It is accessible when the drive mechanisms are in or out of the module.

### CAUTION

WHEN PERFORMING THE FOLLOWING PROCEDURES, DO NOT STRESS THE FRAGILE TAB ON WHICH THE SWITCH IS MOUNTED. IF THE TAB IS DAMAGED, THE ENTIRE RECEIVER MUST BE REPLACED.

#### 6.14.1 Removal

- a. Support receiver tab and remove two door open switch retaining screws and lockwashers. If necessary, use long nut driver to hold nuts.
- b. Note color coding of wire connected to each switch terminal, then unsolder wires.
- c. Remove switch from drive mechanism.

#### 6.14.2 Installation

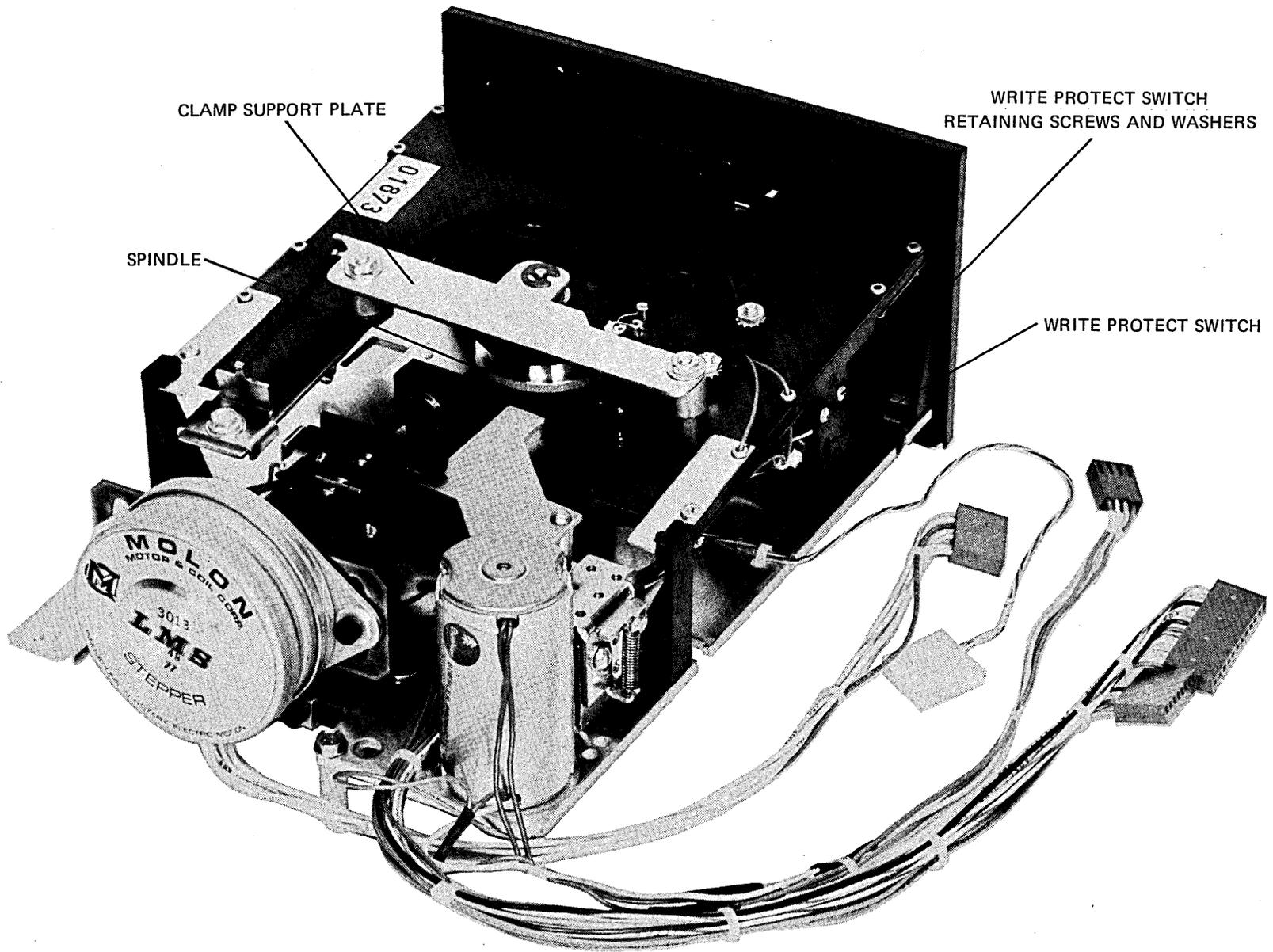
- a. Observing connections noted in Para. 6.14.1, Step b, solder three wires to switch terminals.
- b. Hold switch against tab with actuator positioned down and toward rear of drive mechanism, then loosely install two screws, lockwashers, and nuts.
- c. Do not reshape the heavier actuator arm on replacement switches.
- d. Perform door open switch test/adjustment procedures (Para. 4.11).

## 6.15 TRACK ZERO SWITCH REPLACEMENT

The track zero switch (Figure 6-9) is secured to a bracket by two screws, lockwashers, and nuts. The bracket is secured to the chassis by two (or three) screws. The switch and bracket are replaced as an assembly, and are accessible after the drive mechanism is removed from the drive module.

#### 6.15.1 Removal

- a. Note color coding of wire connected to each switch terminal, then unsolder wires.
- b. Remove track zero switch retaining screws.
- c. Remove switch and bracket from drive mechanism.



CLAMP SUPPORT PLATE

WRITE PROTECT SWITCH  
RETAINING SCREWS AND WASHERS

SPINDLE

WRITE PROTECT SWITCH

Figure 6-11. Single Drive, Top Rear View, PCBA Removed

### 6.15.2 Installation

- a. Hold bracket against chassis and loosely install retaining screws.
- b. Observing connections noted in Para. 6.15.1, Step a, solder three wires to switch terminals.
- c. Perform track zero switch alignment (Para. 4.10).

### 6.16 RECEIVER SUBASSEMBLY REPLACEMENT

The receiver subassembly (Figure 6-10) includes the receiver, write protect and door open switches, index/sector LED, and eject mechanism; it does not include the clamp and clamp support plate. The

receiver subassembly is accessible when the drive mechanism is removed from the drive module.

#### 6.16.1 Removal

- a. Loosen two bezel mounting screws (Figure 6-6).
- b. Slide eject mechanism rearward until it latches.
- c. Move bezel forward and up until clear of handle, then remove from drive mechanism.
- d. Loosen drive's left hand pivot post retaining screw, then separate receiver subassembly from left pivot (Figure 6-9).
- e. Rotate receiver subassembly on right pivot post (Figure 6-12) while moving it to left until

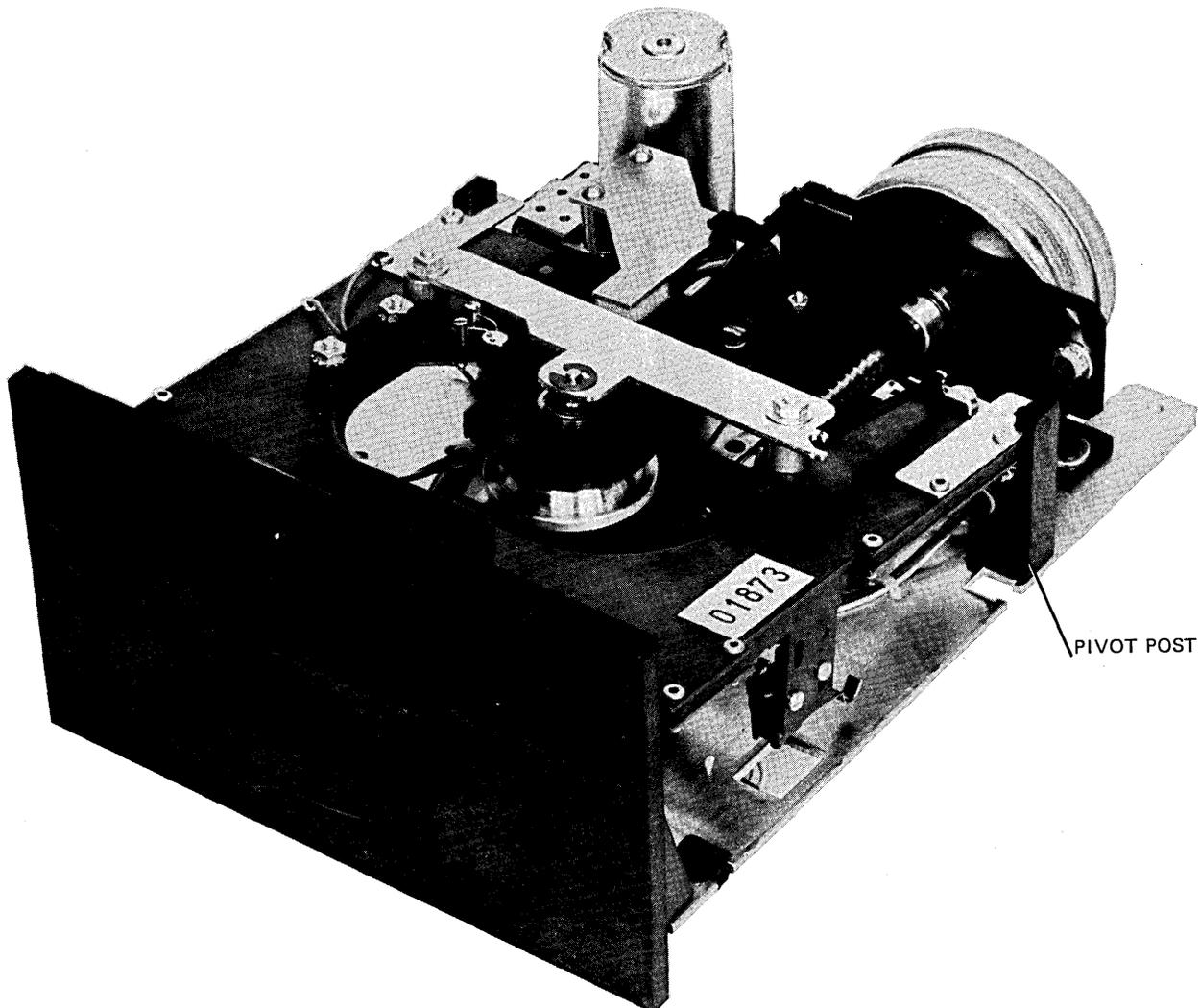


Figure 6-12. Single Drive, Top Front View, PCBA Removed

receiver subassembly is removed from drive mechanism. Retain door open spring (Figure 6-13).

- f. Note location of tie wraps securing receiver subassembly wires to chassis, then cut them.
- g. Separate receiver subassembly wires from remainder of drive mechanism wires.
- h. Proceed to installation procedures (Para. 6.16.2).

#### 6.16.2 Installation

- a. With removed receiver subassembly still attached to drive mechanism by wires, place replacement subassembly so that its wires can be routed in the same manner as those of the removed one.
- b. Select wire from removed receiver subassembly and trace it to connector.
- c. Insert pointed tool such as scribe through connector window adjacent to selected wire and press metal tab that locks connector contact in connector body.
- d. Slide contact toward wire end of connector until tab is concealed in connector body, then gently pull on wire while using scribe to push contact out of connector.
- e. Select corresponding wire on replacement receiver subassembly and align its contact, metal tab toward window, with connector socket.
- f. Push contact into connector until seated.
- g. Repeat Steps b through f for remaining wires.
- h. Make sure door open spring is in place, then position replacement receiver subassembly in right pivot with left side up.
- i. Install left pivot post in place over receiver pivot. Tighten left pivot retaining screw.
- j. Slide eject mechanism rearward until it latches.
- k. Install bezel over handle, then move down and rearward until it can be secured with bezel retaining screws and nuts.
- l. Install tie wraps at locations noted in Para. 6.16.1, Step f.
- m. Remove clamp from removed receiver subassembly and install on replacement receiver subassembly (Para. 6.10).
- n. Perform following procedures in order listed:

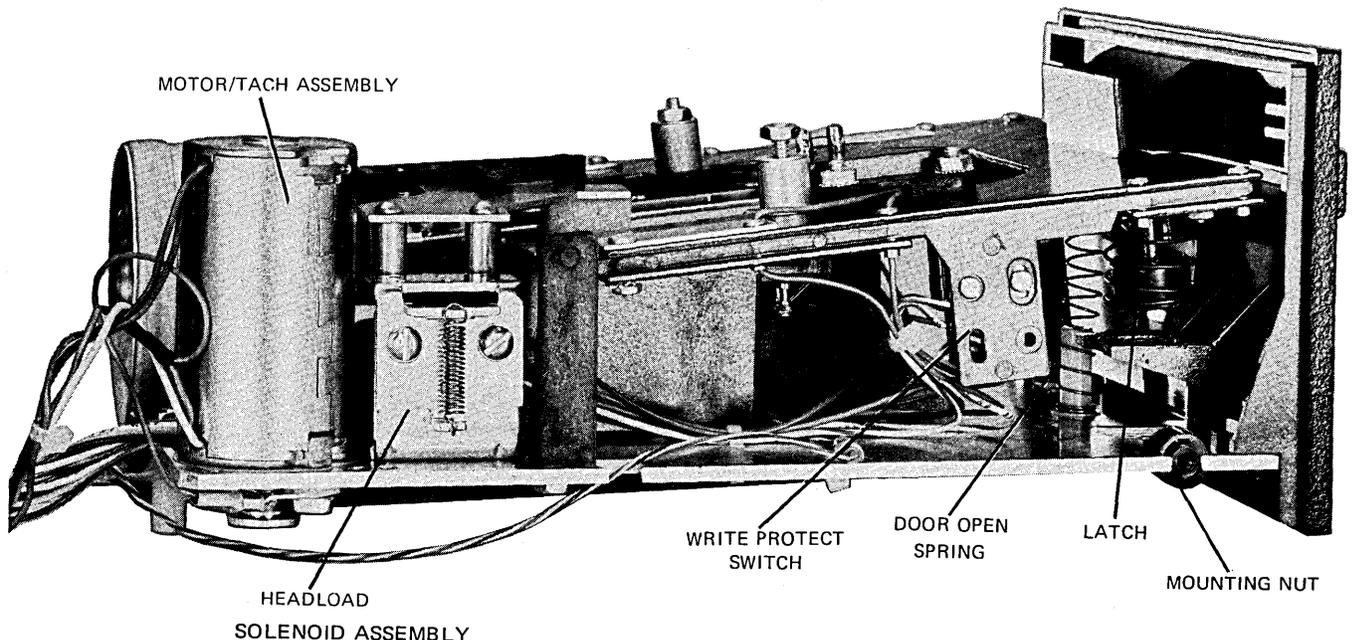


Figure 6-13. Single Drive, Side View, PCBA Removed

Procedure	Para No.
Door open switch test/ adjustment	4.11
Write protect switch test/ adjustment	4.13
Clamp and support plate check and adjustment	4.14
Diskette rear stop check and adjustment	4.15

**NOTE**

Handle will fit through bezel *without* use of force.

- d. Receiver may now be rotated upward to gain access to two nuts securing latch to receiver. Remove these nuts.
- e. Remove latch.

**NOTE**

Take care not to lose 4 flat washers located between latch and receiver.

**6.17 LATCH MECHANISM (Figure 6-13)**

The latch mechanism should be replaced whenever the door cannot be latched or unlatched without difficulty (i.e., binding, not releasing, not latching, etc.).

**6.17.1 Removal**

- a. Remove drive mechanism from module. On single drive subsystem remove PCBA from mechanism.
- b. Loosen two allen head bezel mounting screws holding bezel to base plate (Figure 6-6).
- c. While holding eject mechanism in backward position, carefully remove bezel from drive.

**6.17.2 Installation**

- a. Install 2 flat washers over each latch mounting stud on receiver.
- b. Install latch over two studs.
- c. Install and tighten 2 mounting nuts.
- d. Apply a heavy coat of grease Micropolis P/N 732-0001 to entire latch mechanism.
- e. If door open spring (over white post) was removed, reinstall spring no. 715-1002.
- f. Reverse Steps a through c of Para. 6.17.1.

### PARTS LIST

#### 7.1 INTRODUCTION

This section provides information useful in identifying components or assemblies within the single and dual modules. Only replaceable components and assemblies are identified. Assemblies are identified at their lowest spared level (i.e., individual parts of the subassemblies are not identified or stocked).

Parts information for the single, dual and controller PCBAs are contained on sheet 1 of each of the respective schematics.

**TABLE 7-1. SINGLE ENCLOSURE WITH POWER SUPPLY PARTS LIST**

Part No.	Description	Fig. Ref.
120-0150-9	15 ohm Resistor Chassis (R1) Mount 5% 15W	
175-8907-8	Capacitor 8, 900uf 25WVDC (C2)	
230-0001-1	Rectifier Bridge (75 JB1) (BR1)	6-1
380-7805-1	Regulator 7805 5V (VR2)	6-1
380-7812-7	Regulator 7812 (2) 12V (VR1)	6-1
610-0001-4	Switch, Rocker (SW1)	
626-0002-8	Fuse, 1 amp (F1)	
627-0001-8	Fuse Holder	
320-0002-0	Transformer, Power (T1)	
664-0001-1	Cord Set 18/3 SVT 6 ft	6-1
671-0001-6	Strain Relief Bushing	6-1
680-0504-0	5 Pin Housing, Molex	
680-0801-0	8 Pin Housing, Molex	
680-1002-4	10 Pin Housing, Molex	
681-0003-1	Pin, Molex	
682-0001-3	Key, Molex	
683-2501-8	¼ Faston Female 18-22 AWG Terminal	
683-2504-2	¼ Faston Female 14-16 AWG Terminal	
100055-01-1	Heatsink	6-1
100056-01-9	Chassis, Base	6-1

**TABLE 7-1. SINGLE ENCLOSURE WITH POWER SUPPLY PARTS LIST**

Part No.	Description	Fig. Ref.
100057-01-7	Cover	
100071-01	PCBA, Single A drive (100 TPI)	6-1
100163-01	PCBA, Single B drive (100 TPI)	6-1
100071-03	PCBA, Single A drive (48 TPI)	6-1
100163-03	PCBA, Single B drive (48 TPI)	6-1
100075-01	Drive Mechanism 100TPI	6-1
100075-02	Drive Mechanism 48TPI	6-1
100100-01-5	Stand Off (Drive Mechanism to Chassis)	6-1
100100-05-6	Stand Off (PCBA Support)	6-1

**TABLE 7-2. DUAL ENCLOSURE PARTS LIST**

Part No.	Description	Fig. Ref.
120-0075-8	7.5 ohm Resistor (R1) Chassis Mount 5% 15W	6-4
175-2008-1	Capacitor 20,000uf 25WVDC (C2)	6-4
230-0001-1	Rectifier Bridge (75 JB1) (BR1)	6-4
380-7805-1	Regulator 7805 5V (VR2) Mounted behind heatsink	6-5
380-7812-7	Regulator 7812 12V (VR1, VR3) Mounted behind heatsink	6-5
610-0001-4	Switch, Rocker (SW1)	6-4
626-0002-8	Fuse, 1 amp (F1)	6-4
627-0001-8	Fuse Holder	6-4
630-0002-0	Transformer, Power (T1)	6-4
664-0001-1	Cord Set 18/3 SVT 6 ft	6-4
671-0001-6	Strain Relief Bushing	6-4
680-0504-0	5 Pin Housing, Molex	
680-1002-4	10 Pin Housing, Molex	
680-1301-0	13 Pin Housing, Molex	
681-0003-1	Pin, Molex	
682-0001-3	Key, Molex	
683-2501-8	¼ Faston Female 18-22 AWG	
683-2504-2	¼ Faston Female 14-16 AWG	

**TABLE 7-2. DUAL ENCLOSURE PARTS LIST (Cont'd)**

Part No.	Description	Fig. Ref.
100048-01-6	Chassis, Base	6-5
100049-01-4	Cover	
100050-02-0	Display (Front Overlay)	
100053-01-6	Bezel	6-5
100061-01	PCBA, Dual 100 TPL	6-5
100068-01-4	Heatsink	6-5
100075-01	Drive Mechanism (2) 100 TPI	6-4

**TABLE 7-3. DRIVE MECHANISM PARTS LIST**

Part No.	Description	Fig. Ref.
612-0001-0	Switch (Door Open & Write Protect)	6-13 6-12
681-0002-1	Pin, Molex	
703-0605-5	Screw, 5/16 Taptite	
709-0001-4	Latch Mechanism	6-13
710-0605-0	Mounting Nut, #6, Plastic	6-13
715-1002-8	Spring (Door Open)	6-13
715-2001-9	Spring (Eject)	6-13
715-2002-7	Spring (Carriage Assembly)	6-8
717-0601-4	Pin, Dowel (Carriage Assembly) Upper	6-8
717-0602-2	Pin, Dowel (Carriage Assembly) Lower	6-8

**TABLE 7-3. DRIVE MECHANISM PARTS LIST (Cont'd)**

Part No.	Description	Fig. Ref.
725-1201-5	Belt	6-6
100007-01-2	Pulley	6-6
100012-01-2	Motor Tach. Assembly	6-9
100014-01-8	Pivot Post	6-9
100015-01-5	Receiver Assembly	6-9
100023-01-9	Index/Sector L.E.D. Assembly	6-9
100028-01-8	Bezel	6-9
100029-01-6	Platten Assembly (with Index/Sector Photocell)	6-10
100036-01-1	Load Arm	6-8
100034-01-6	Head/Carriage Assembly (48 TPI)	6-8
100037-01-8	Head/Carriage Assembly (100 TPI)	6-8
100074-01-2	Load Pad	6-8
100076-01-9	Positioner Assembly Complete (48 TPI)	6-8
100076-02-7	Positioner Assembly Complete (100 TPI)	6-8
100077-01-5	Spindle Assembly	6-10
100078-01-3	Clamp Assembly with Support Plate)	6-9
100079-01-1	Head/Load Solenoid Assembly	6-9
100081-01-7	Track 0 Switch Assembly	6-9

### MICROPOLIS DISK DIAGNOSTIC

#### 8.1 INTRODUCTION

The Micropolis Disk Diagnostic is an 8080 Assembly Language Program which runs under Micropolis PDS. The diagnostic provides the proper test environment to perform the maintenance and adjustment of Micropolis 1040/1050 Series Subsystems described in this manual.

#### 8.2 SYSTEM REQUIREMENTS

The standard version of the diagnostic requires the following minimum system configuration:

- a. S100-bus computer with Z-80, 8080, or 8085 processor.
- b. A minimum of 16K of RAM memory starting at address 0. RAM access requirements are described in the 1040/1050 Series Users Manual.
- c. A 1040/1050 Series Subsystem consisting of a Controller-B and 1 or more Micropolis Storage Modules.
- d. A system terminal device consisting of a keyboard entry and display device and the necessary interface board.
- e. A configured PDS DOS Diskette.
- f. Scratch diskettes as required by the maintenance programs.
- g. Micropolis Diagnostic Diskette.

#### 8.3 OPERATING PROCEDURE

##### 8.3.1 Loading the Diagnostic

The diagnostic is a PDS overlay file which may be invoked as follows:

- a. Boot a configured PDS system diskette.
- b. When MODS completes its sign-on, load the diagnostic diskette into drive 0 and type DIAG{(\ denotes carriage return).

- c. The diagnostic will sign on at the terminal:

Micropolis Disk Diagnostic VS X.X

Copyright Micropolis Corporation 1978

Front Panel (Y or N)?

If your computer has a front panel with program sense switches which may be read by an IN OFFH, then respond to the prompt with Y, otherwise enter N.

- d. The diagnostic will prompt:

"Enter High Track."

Enter 76 if the drive to be tested is a Mod II (IV) drive and 35 if it is a Mod I (III).

- e. The diagnostic is now initialized and will prompt for a command. Remove the diagnostic diskette from drive 0.

##### 8.3.2 Warm Starting the Diagnostic

If it is necessary to reset your system, the diagnostic may be restarted by starting execution at the standard PDS warm start address. Refer to the Micropolis User's Manual, Document Number 100089-1.

##### 8.3.3 Exiting the Diagnostic

The diagnostic overlays MDOS and parts of RES so it is not possible to return to MDOS without rebooting.

##### 8.3.4 Entering Commands

The diagnostic is an interpretive language processor which executes command strings entered at the terminal. A command string consists of one or more test commands. Commands must be separated from each other by one or more blanks. A command string is terminated by a carriage return. During entry, a command line is subject to the following editing facilities:

- a. Entering the rubout key deletes the last previously typed character from the command string.

- b. Depressing the control key and entering the X key (CTL/X) deletes the current command string.
- c. Entering a line feed as a separator between commands causes a carriage return/line feed at the terminal without terminating the command. (This feature is helpful if a command string exceeds one line on the terminal and the auto-wrap feature in the PDS terminal handler is not enabled).

A list of the valid test commands is given in Para. 8.4 of this section.

Execution of a command string may be suspended by depressing the control key and entering the C key (CTL/C). The diagnostic will prompt with "Interrupt?." Entering C will cause resumption of the interrupted command string. Entry of any other key will abort the command string.

### 8.3.5 Error Messages

#### Command Errors

If an invalid command is entered, the following message is printed:

Error Message P\*\* Cnn

where P\*\* indicates the error is in the command string entered at the terminal and Cnn indicates the error is in command nn of that command string.

The error message will be "Invalid Command" if the command is not found or "Invalid Parameter" if a parameter associated with the flagged command is not valid.

#### Disk Errors

A disk error will be reported as follows:

Pnn Cnn Unn Hnn Snn Tnn Enn

where:

- Pnn = Test program in which error occurred
- Cnn = Command in program which resulted in error
- Unn = Drive unit number selected

- Hnn = Selected head
  - 0 — Lower Surface
  - 1 — Upper Surface (Mod III or IV only)
- Snn = Desired sector
- Tnn = Desired track
- Enn = Error code
  - 1 = Drive not operational
  - 2 = Header check error
  - 3 = Restore operation cannot find track 0
  - 4 = Checksum error
  - 5 = Track address error (VT command only)
  - 6 = Unit address error (VU command only)
  - 7 = Data buffer verify error
  - 8 = Write protect error

Additional information will be printed after some errors as follows:

- a. Error 2: Contents of header read from sector in error as follows:
  - HH SS TT
  - where HH = Head address, SS = Sector address, and TT = Track address.
- b. Error 5: Track address read from a sector on the offending track.
- c. Error 6: Unit address read from a sector on the offending unit.
- d. Error 7: Expected data and data found for first byte in error in a buffer compare
  - S/B XX            WAS XX

### 8.4 TEST COMMANDS

A test command consists of a command keyword and zero or more parameters. Parameters must be separated from the keyword and each other by a comma (.). Numeric parameters may be specified in decimal notation or hexadecimal notation. Decimal values must be unsigned numbers from zero to

65529. Hexadecimal notation is indicated by appending the letter "H" to the number entered. Hexadecimal values may be in the range 0H to FFFFH. Most commands require single byte parameters and will ignore the most significant byte of the converted binary value of parameters entered.

Three system variables are also available for use as parameters:

T% = Max track value specified in initialization dialogue

U% = Last unit selected

H% = Last head selected

### Select Unit

U, u, h — Select drive unit u, Head h where h = 0 — lower surface; = 1 — upper surface (dual head unit only) ( $0 \leq u \leq 3$ )

Z, u, h — Select drive unit u, Head h and restore selected drive to track 0

### Position Unit

T, n — Position drive to track n  
 ( $0 \leq n \leq \text{Trackmax}$ ) — where trackmax is high track specified in sign on dialogue  
 if  $n = 99$  a random track address is used  
 if  $n > \text{trackmax}$  and  $n \neq 99$  then track address = 0

SI, n — Step in n tracks from current track (must be preceded by a Z or T command when unit is selected)  
 if  $(\text{current track} + n) > \text{trackmax}$  then track reverts to zero

SO, n — Step out n tracks from current track (must be preceded by a Z or T command when unit is selected)  
 if  $(\text{current track} - n) < 0$  then track reverts to trackmax

### Read/Write Commands

s = Sector address ( $0 \leq s \leq 15$ )

p = Data pattern

0 — Switch register — 1 byte pattern read from the sense switches of a computer with a front panel. In computers without a front panel, pattern 0 may be specified with the SP command.

1 — Random

2 — Binary count

3 — All 1's

4 — Alternate 1's and 0's

n = Number of sectors ( $1 \leq n \leq 16$ )

I, p — Initialize selected surface of selected drive with pattern p

IW, p, s — Write pattern p to sector s without verifying header

W, p, s — Verify header then write pattern p on sector s

WT, p — Verify header then write pattern p to all sectors of current track

WD, p — Verify header then write pattern p to all sectors of all tracks of currently selected drive/surface

MW, p, n — Write pattern p to first n sectors of current track — n sectors are written in 1 revolution

R, p, s — Read sector s of current track  
 Verify header and compare data  
 Read with pattern p

RT, p — Read and compare all sectors of current track

RD, p — Read and compare all sectors of all tracks on currently selected drive/surface

MR, n — Read first n sectors of current track  
 Header and checksum only are verified  
 n sectors read in 1 revolution

SP,m — Set pattern 0 to m

VT — Read first sector which comes around and verify track address against desired track

VU — Read first sector which comes around and verify unit address against desired unit

### Miscellaneous Commands

DL,nn — Wait nn milliseconds

PB,m — Print contents of read buffer

m ≠ 0 — Dump buffer without conversion

m = 0 — Print in hex notation as follows:

```

ENTER COMMAND T,76
ENTER COMMAND W,2,15
ENTER COMMAND R,2,15
ENTER COMMAND PB,0
4C 0F 00 00 5B FF 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D
0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21
22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33 34 35
36 37 38 39 3A 3B 3C 3D 3E 3F 40 41 42 43 44 45 46 47 48 49
4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D
5E 5F 60 61 62 63 64 65 66 67 68 69 6A 6B 6C 6D 6E 6F 70 71
72 73 74 75 76 77 78 79 7A 7B 7C 7D 7E 7F 80 81 82 83 84 85
86 87 88 89 8A 8B 8C 8D 8E 8F 90 91 92 93 94 95 96 97 98 99
9A 9B 9C 9D 9E 9F A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 AA AB AC AD
AE AF B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 BA BB BC BD BE BF C0 C1
C2 C3 C4 C5 C6 C7 C8 C9 CA CB CC CD CE CF D0 D1 D2 D3 D4 D5
D6 D7 D8 D9 DA DB DC DD DE DF E0 E1 E2 E3 E4 E5 E6 E7 E8 E9
EA EB EC ED EE EF F0 F1 F2 F3 F4 F5 F6 F7 F8 F9 FA FB FC FD
FE FF 00 01 02 03 04 05
ENTER COMMAND

```

PE,m — Printer echo — if the I/C handler on the PDS diskette is configured for a line printer then:

m = 0 — Disable printer

m = 1 — Echo console output on line printer

#### Program Control

X,m — Execute one of the built-in maintenance programs (0 ≤ m ≤ 19)

L — Repeat the current command string (Example U,0,0 L Selects unit 0, head 0 until interrupted)

LC,m — Repeat the current command string until the iteration count (which starts from 0) is equal to m

Example:

Z,0,0

MR,16 SI,1 LC,76

This example reads all sectors of tracks 0 thru 76

PL — Print value of the iteration count associated with the current command string

### 8.5 MAINTENANCE ADJUSTMENT PROGRAMS

The programs required to perform the maintenance adjustments specified in this manual are provided as built in programs which may be invoked, by the X command described in Para. 8.4. Use of the programs is described in Section 4.

Table 8-1 shows equivalent program listings of the built-in Test Programs. The built-in programs exercise their own control over error handling, so printouts obtained from these programs will be different from results obtained by executing command strings consisting of these commands.

### 8.6 SUBSYSTEM VERIFICATION

Overall performance of a subsystem may be verified by executing the following commands which perform a mix of data handling and positioning functions.

Z,u,h X,4 PL L — for Mod I subsystems

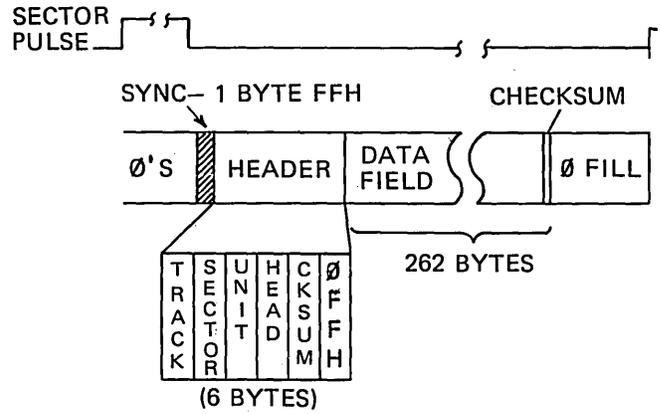
Z,u,h X,3 PL L — for Mod II subsystems

**TABLE 8-1. MAINTENANCE PROGRAMS**

0	MR,16 SI,1 LC,T%
1	MW,2,16 SI,1 LC,T%
2	MW,1,16 SI,1 LC,T%
3	X,1 RD,2 X,2 RD,1 X,5 X,11
4	X,1 RD,2 X,2 RD,1 X,5 X,10
5	T,99 MR,16 LC,99
6	DL,2500 DL,2500
7	T,40 T,36 X,6 T,30 T,36 X,6 L
8	T,22 T,16 X,6 T,10 T,16 X,6 L
9	Z,U%,H% DL,250 T,1 DL,250 L
10	T,17 VT T,15 VT T,19 VT T,13 VT T,22 VT T,25 VT T,7 VT T,30 VT T,4 VT T,34 VT T,0 VT LC,5
11	T,38 VT T,37 VT T,39 VT T,36 VT T,40 VT T,34 VT T,42 VT T,30 VT T,46 VT T,22 VT T,54 VT T,6 VT T,70 VT T,0 VT T,76 VT LC,5
12	Z,U%,H% T,T% L
13	U,U%,H% L
14	MW,0,16 X,13
15	Z,0,0 MW,0,16 Z,1,0 MW,0,16 X,19
16	T,T% MW,0,16 X,13
17	T,5 U,U%,H% X,6 T,76 U,U%,H% X,6 L
18	T,1 U,U%,H% X,6 T,35 U,U%,H% X,6 L
19	U,0,0 U,1,0 L

**8.7 DISKETTE FORMAT**

The sector format used by the diagnostic is given below:



### SCHEMATIC AND ASSEMBLY DRAWINGS

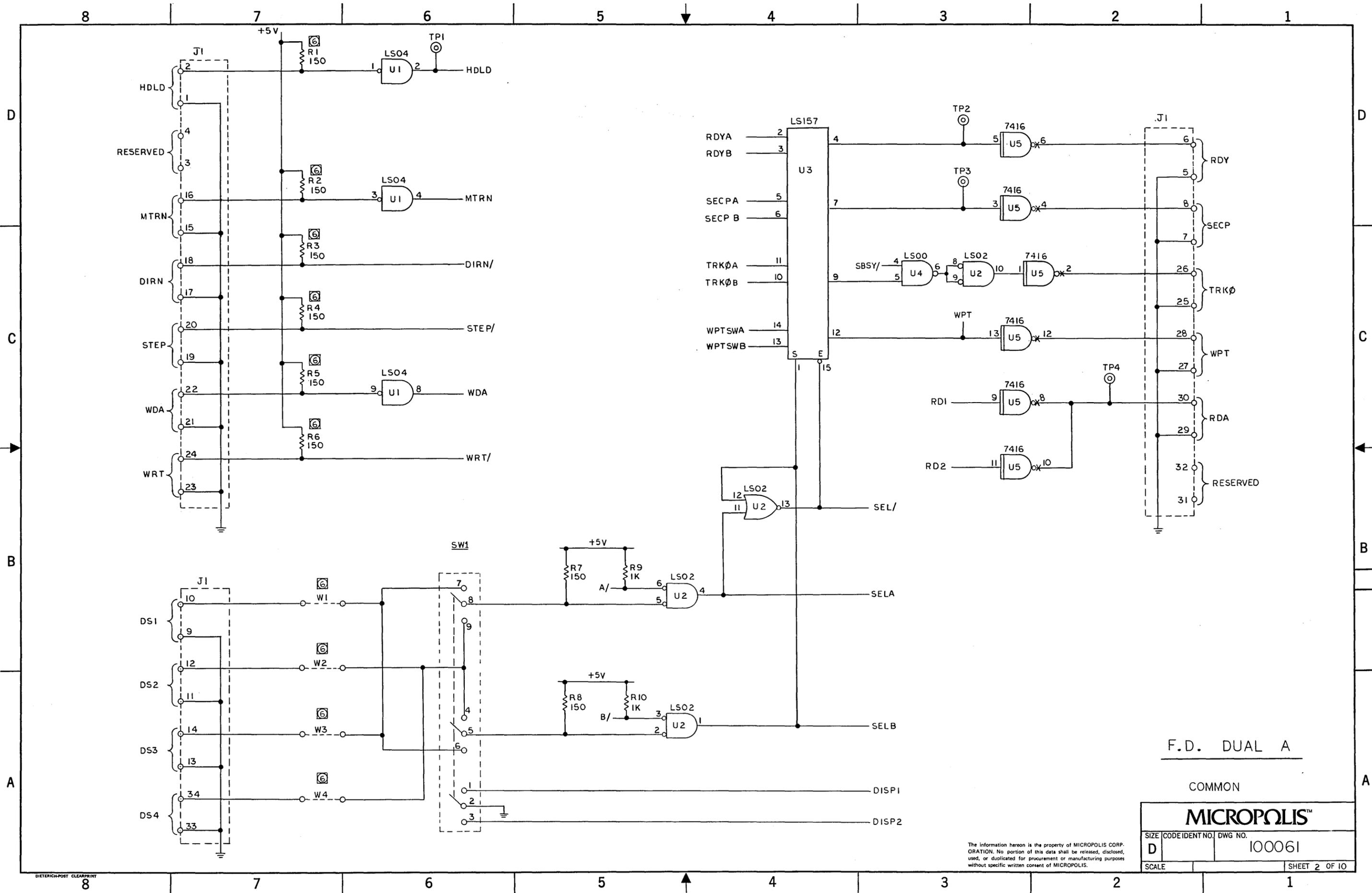
#### 9.1 INTRODUCTION

This section contains the assembly drawings and schematics for all the PCBAs used in the Micropolis Floppy Disk Storage subsystem. Drawings are arranged in numerical order, starting with the F.D. Dual A board assembly, part number 100060. The assembly drawing is followed by 10 pages of logic diagrams for the same board. Parts on the board are identified in the first page of the logic diagram sheets. Board model variations are also defined on that first page.

In turn, the F.D. Single A board assembly is illustrated, in drawing number 100071, which is followed by the logic diagrams for that board. As previously, all parts values and model variations are defined on the first page of the logic diagram. The F.D. Single B board assembly drawing number 10-0164 follows the single drawings which it replaces. The assembly drawing for the controller PCBA, part number 100087, follows the drive logic diagrams. The section concludes with nine pages of controller logic diagrams.







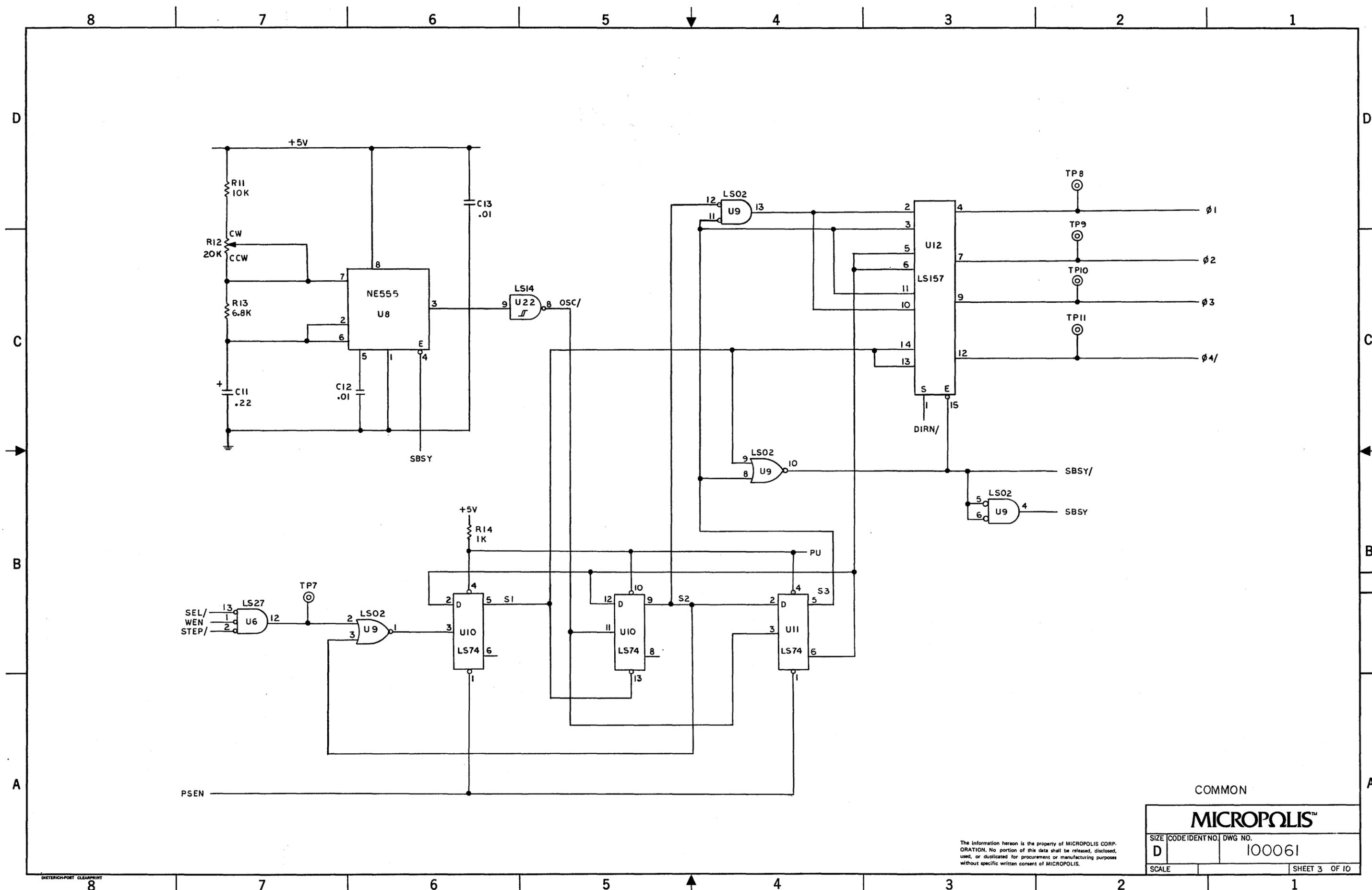
F.D. DUAL A

COMMON

**MICROPOLIS™**

SIZE	CODE/IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 2 OF 10	

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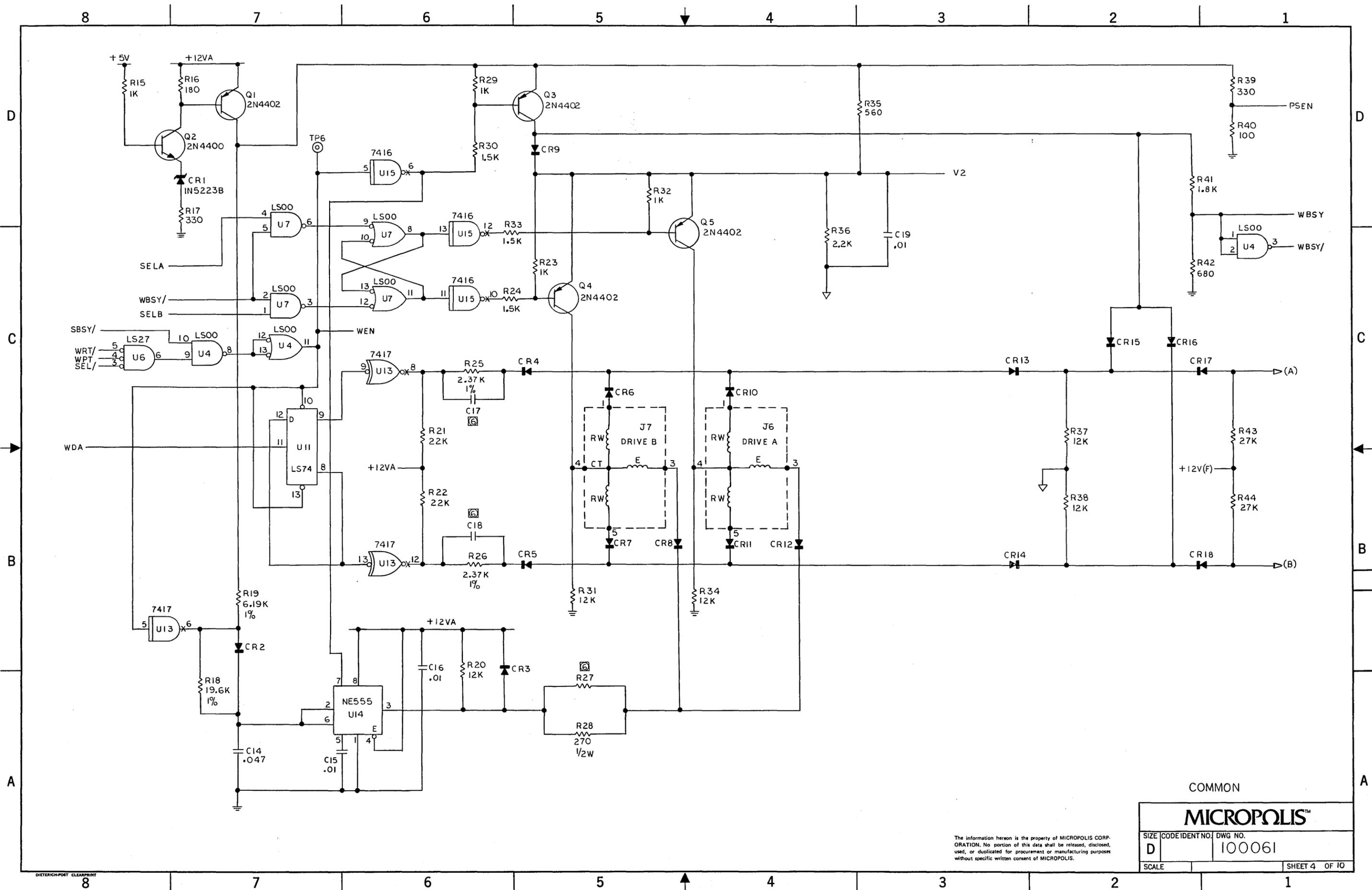


COMMON

**MICROPOLIS™**

SIZE	CODE/IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 3 OF 10	

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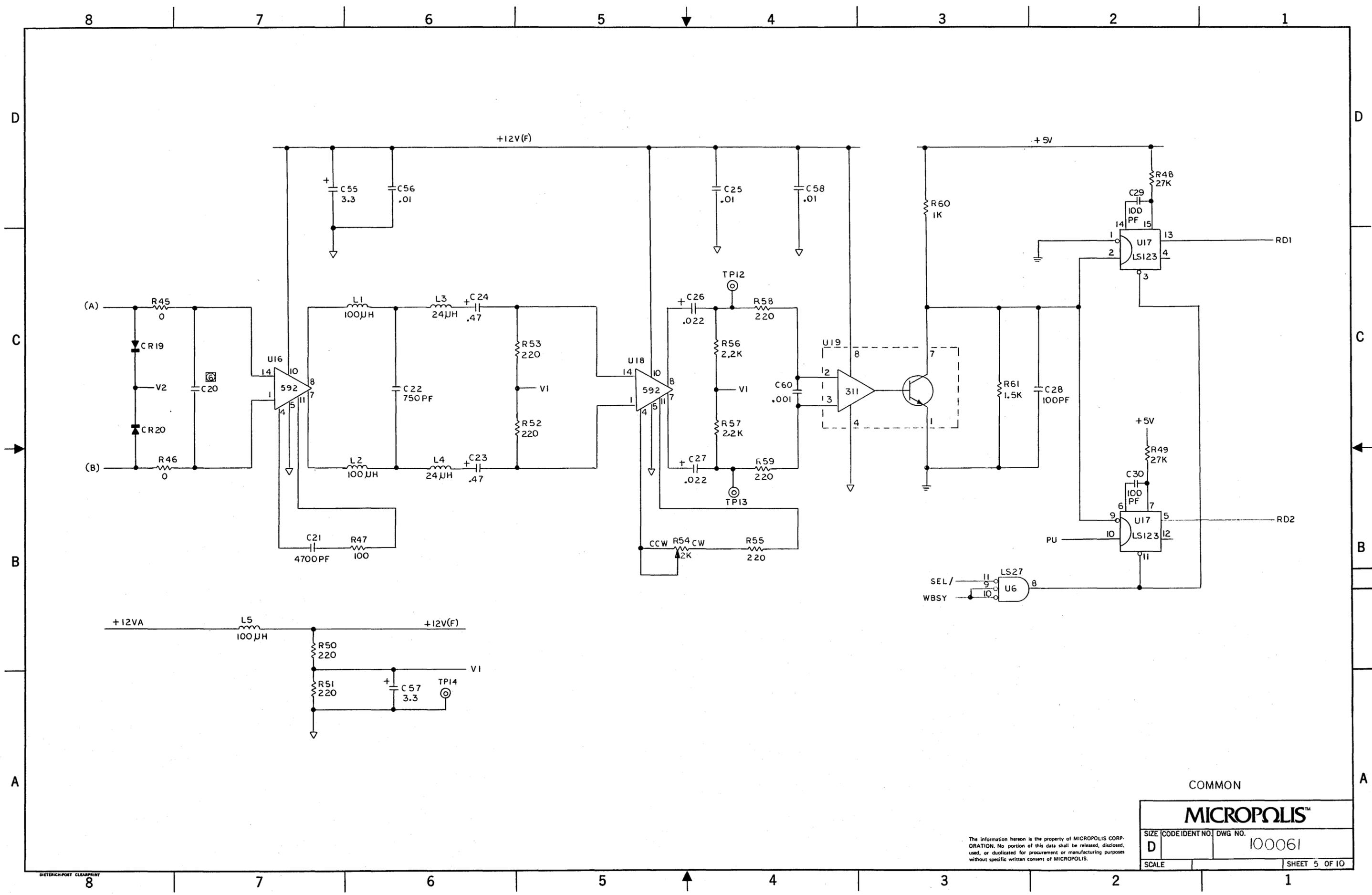


COMMON

**MICROPOLIS™**

SIZE	CODE IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 4 OF 10	

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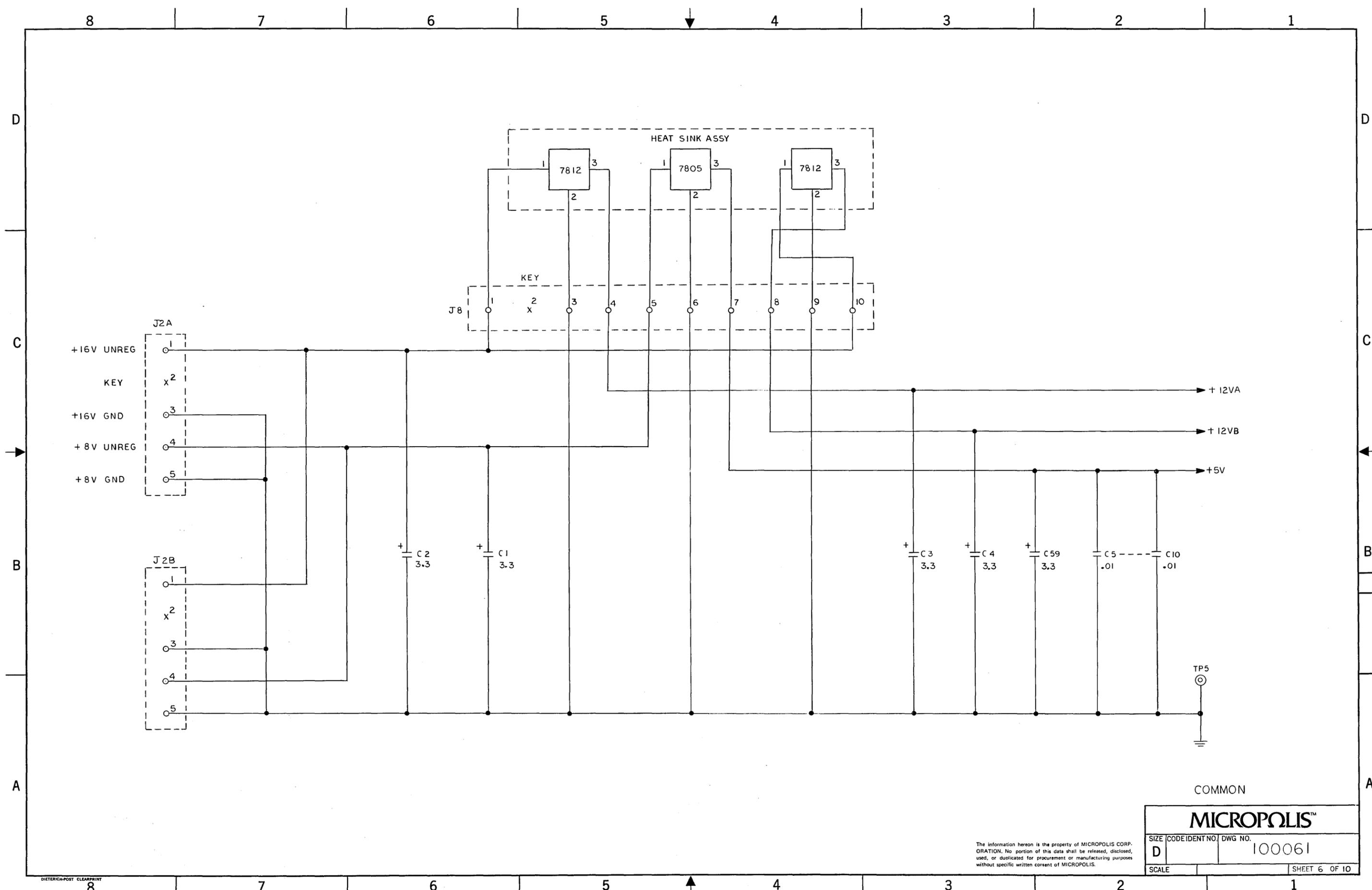


COMMON

**MICROPOLIS™**

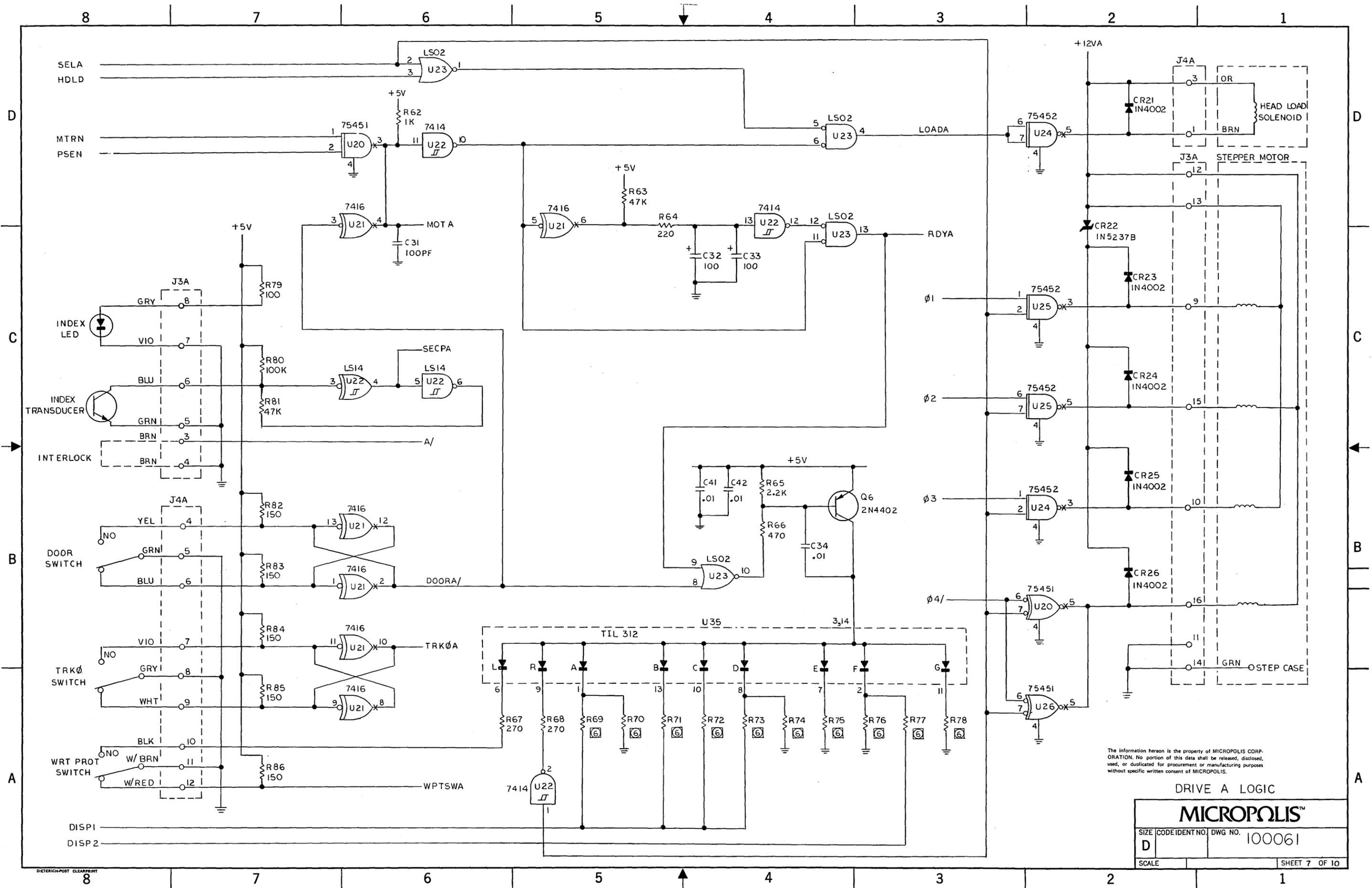
SIZE	CODE IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 5 OF 10	

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<b>MICROPOLIS™</b>		
SIZE	CODE IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 6 OF 10	



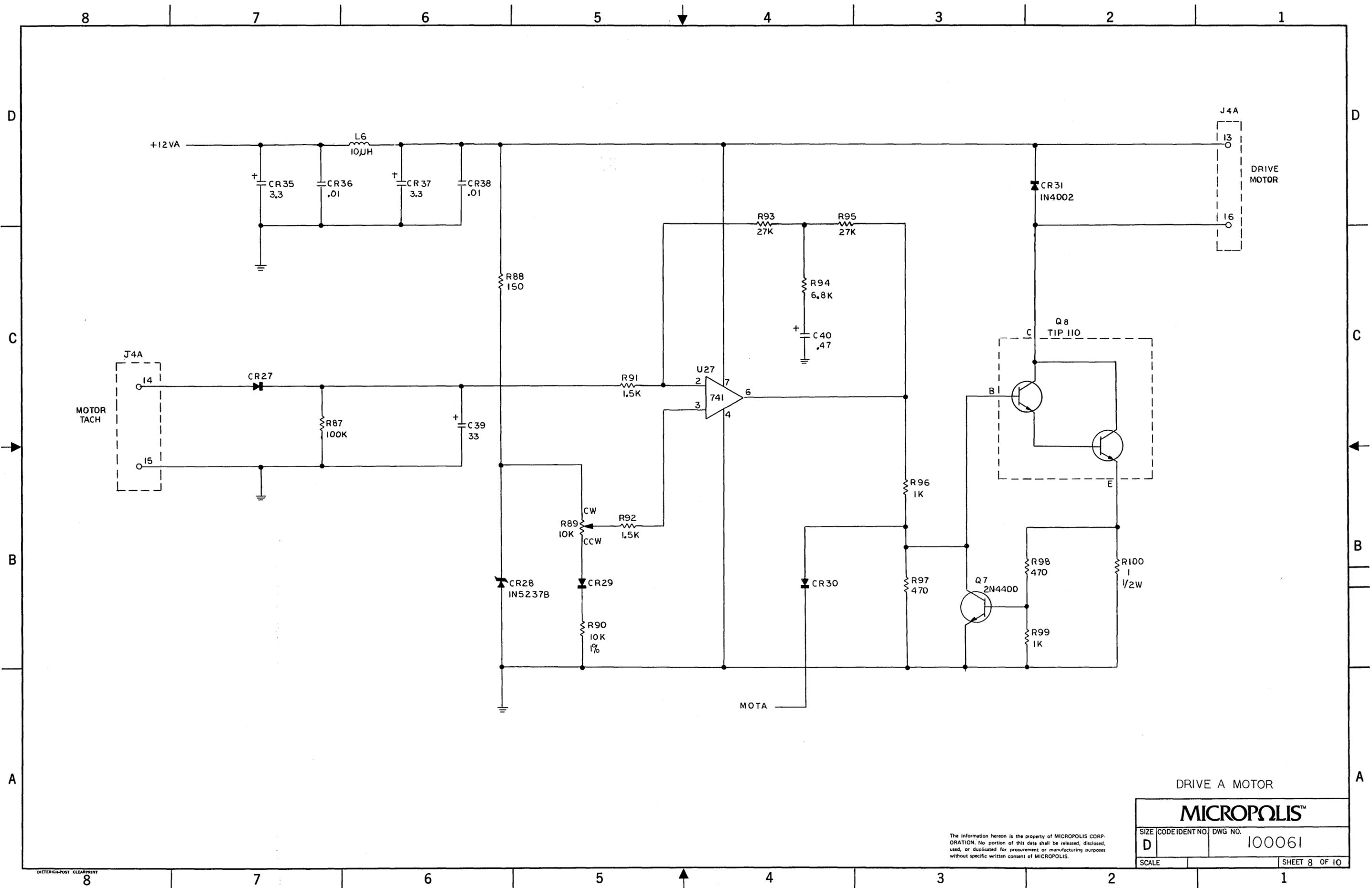
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DRIVE A LOGIC

**MICROPOLIS™**

SIZE CODE IDENT NO DWG NO. 100061

SCALE SHEET 7 OF 10

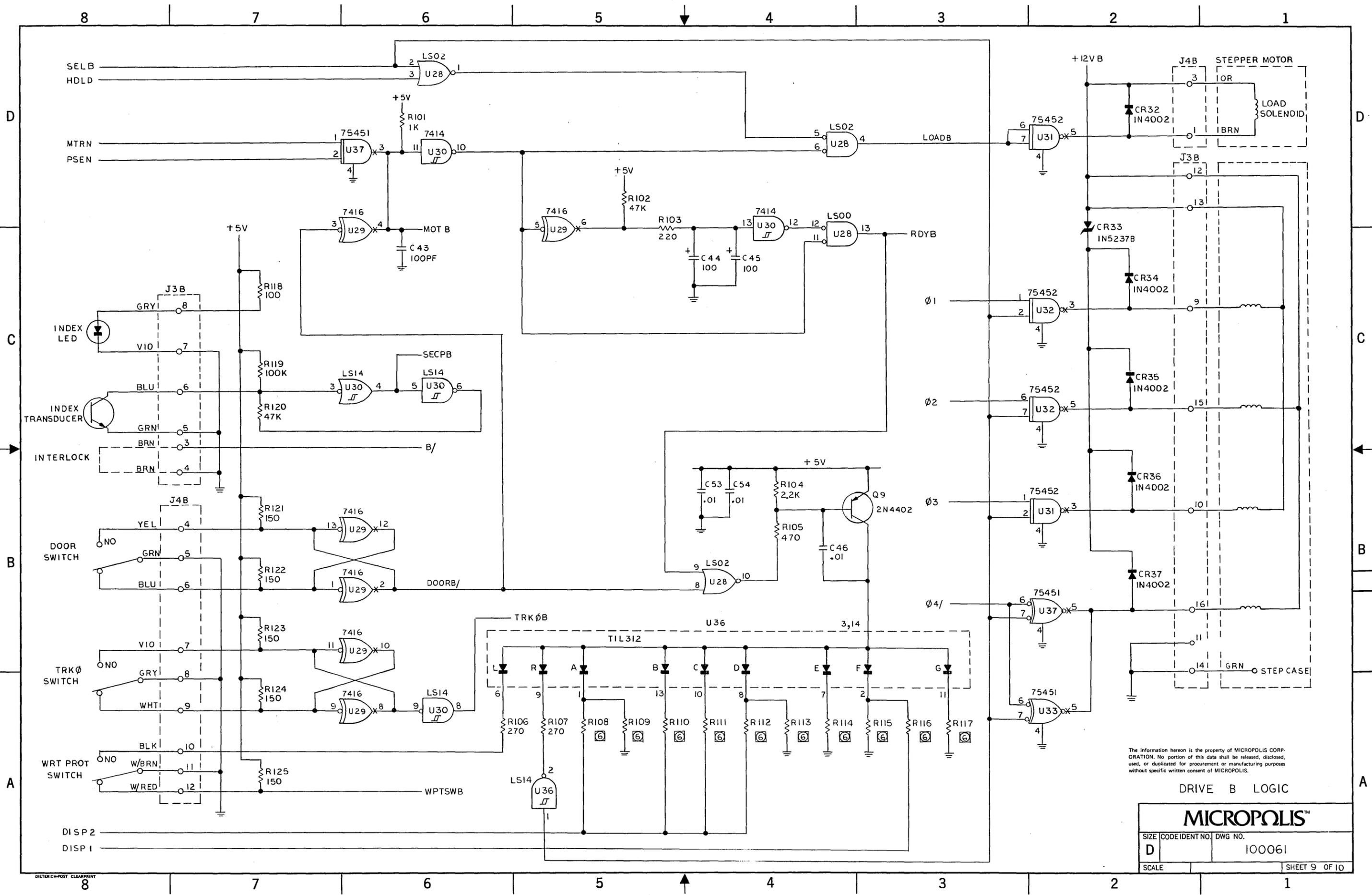


DRIVE A MOTOR

**MICROPOLIS™**

SIZE	CODE IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 8 OF 10	

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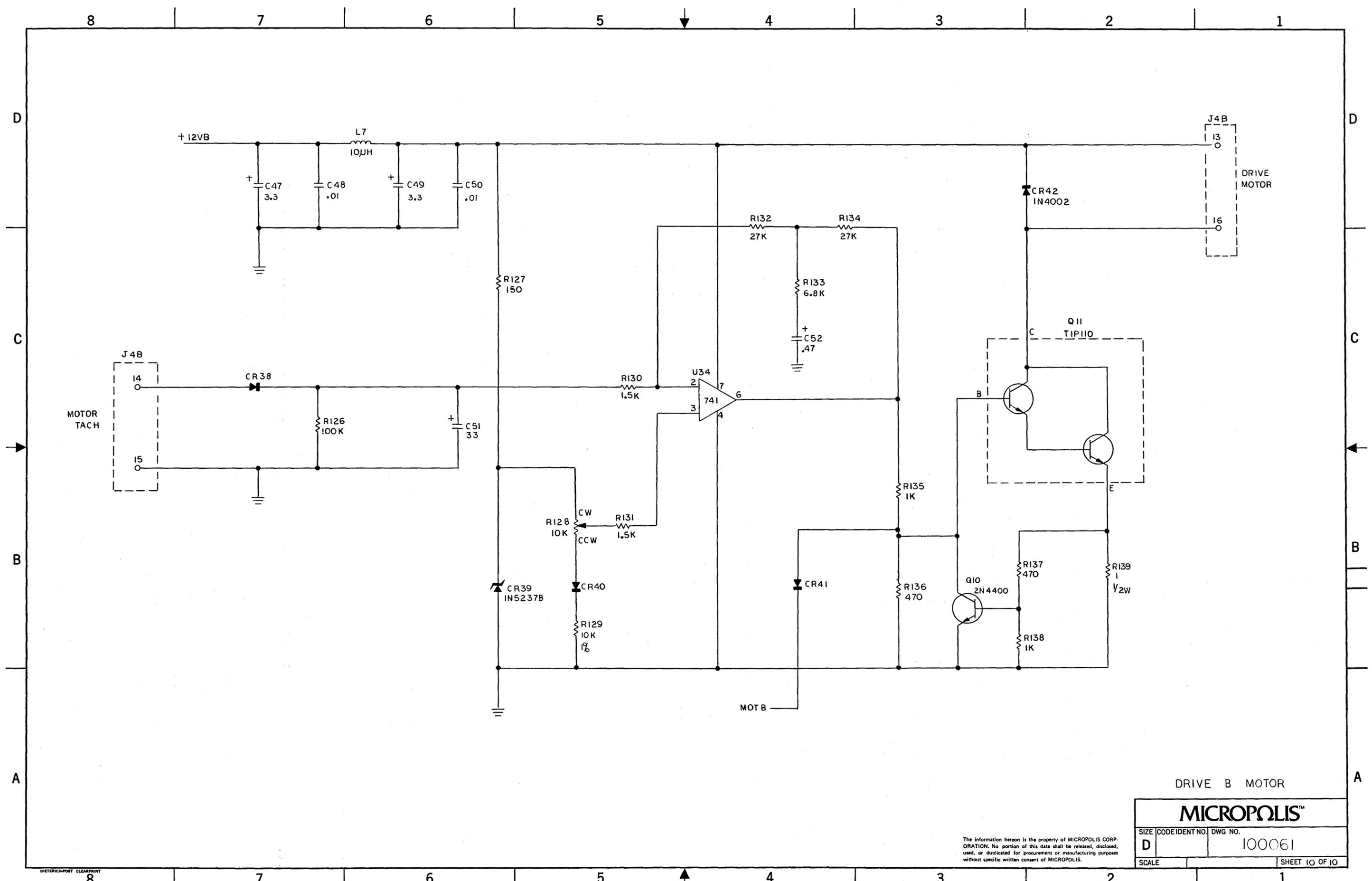


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DRIVE B LOGIC

**MICROPOLIS™**

SIZE	CODE IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 9 OF 10	



DRIVE B MOTOR

**MICROPOLIS™**

SIZE	CODE IDENT NO.	DWG NO.
D		100061
SCALE	SHEET 10 OF 10	

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
A		PROD RELEASE EN 0118	5/22/78	<i>Sch...</i>
B		EN0122 CHANGE U6,U7	6/9/78	<i>Sch...</i>
C		EN 0198	2/26/79	<i>L.S.D.</i>

HTSNK (124) (127) (128) APPLY SILICON GREASE (125) BETWEEN XSISTOR & HTSNK

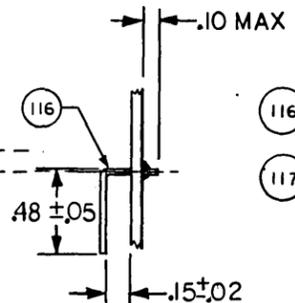
FLUSH TO WITHIN .020

SOCKET (119)

PIN 2 KEYED  
4 PLACES

(120) SOCKET

(122) (10) ORIENTATE AS SHOWN



ASSY VERSIONS  
100163-52-6  
100163-54-2

ASSY VERSIONS  
100163-51-8  
100163-53-4

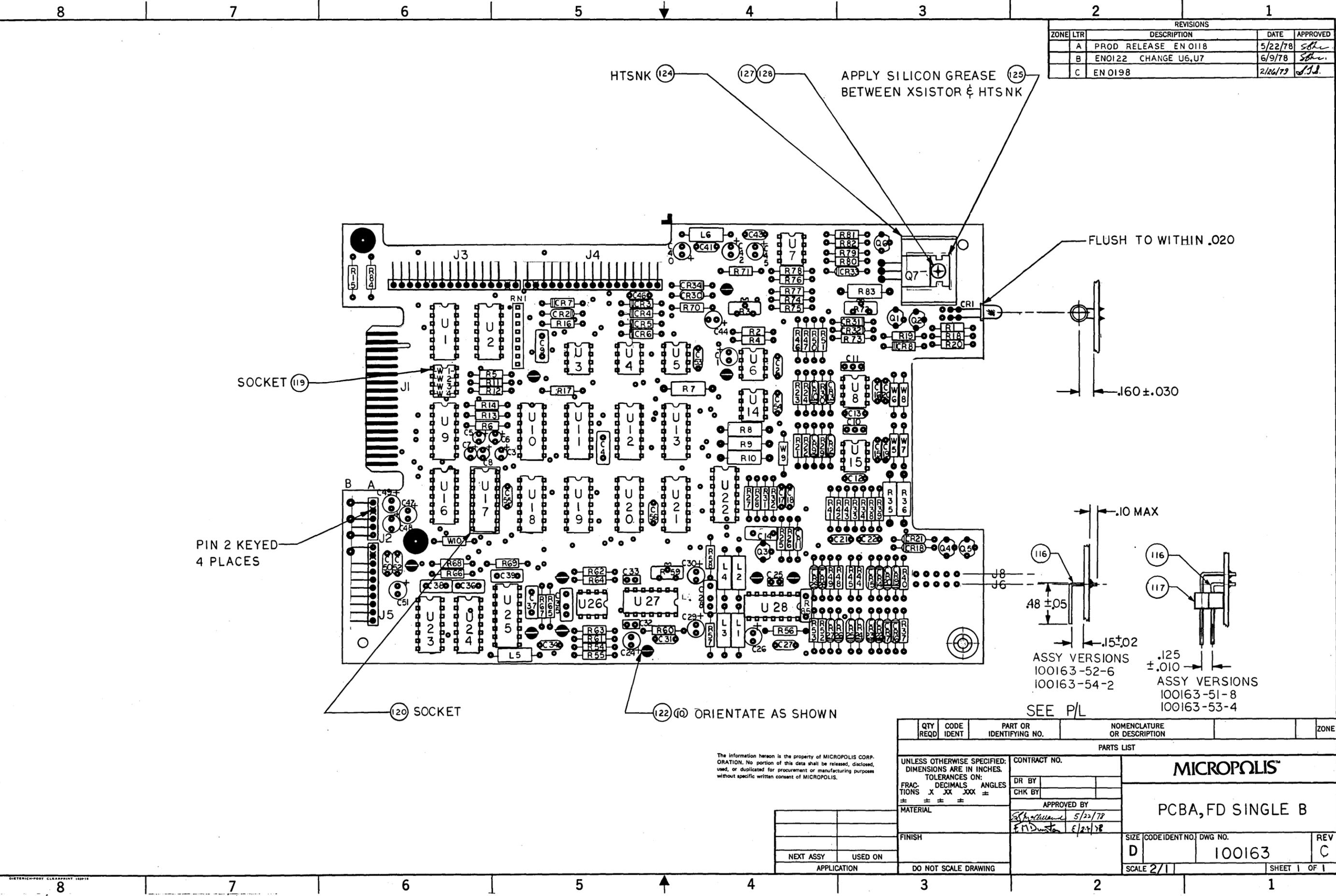
SEE P/L

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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X XX XXX ± DECIMALS ANGLES ± ± ± ±		CONTRACT NO.		<b>MICROPOLIS™</b>  PCBA,FD SINGLE B
MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY USED ON		APPROVED BY <i>E. N. Dunton</i> 5/22/78 <i>E. N. Dunton</i> 6/24/78		
APPLICATION		DO NOT SCALE DRAWING		SCALE 2/1
			SIZE CODE IDENT NO. DWG NO.	REV
			D 100163	C
			SHEET 1 OF 1	

100163

A



DESCRIPTION				REVISIONS				
ZONE	LTR	DATE	APPROVED	ZONE	LTR	DATE	APPROVED	
D	ENO198	2/24/78	SLA	A	PROD RELEASE	ENO118	5/24/78	SLA
E	ENO206	2/24/78	JJA	B	ENO122	R41,R42 VALUES	6/9/78	SLA
				C	ENO186		11/29/78	RL
				CI	ENO188		11/29/78	RL

TABLE II

ASSY VERSION	VERSION CHARACTERISTIC	U8	Q5	CR10,CR13,CR19,CR20,CR21	J6	J8	W6 W8	W9	R23	R24	R30 R40	R31 R32	R35	R36	R38	R39			R67	R85	C11	C13 C16
-51-8	100TPI, GCR DUAL HEAD	NE 555 410-0555-4	2N4402 300-4402-8	IN4446 200-4446-7	HEADER 680-0506-5	HEADER 680-0505-7	IN		6.19K,1%	19.6K,1%	12K	3.16K,1%	390Ω,1/2W	390Ω,1/2W	1.5K	1K			17.8K,1%	22K	.047UF	.01UF
-52-6	100 TPI, GCR SINGLE HEAD				PINS (4) 684-0004-3			IN				3.16K,1%	390Ω,1/2W					17.8K,1%	22K			
-53-4	48 TPI, MFM DUAL HEAD	NE555 410-0555-4	2N4402 300-4402-8	IN4446 200-4446-7	HEADER 680-0506-5	HEADER 680-0505-7	IN		6.19K,1%	19.6K,1%	12K	1.82K,1%	120Ω,1/2W	120Ω,1/2W	1.5K	1K			35.7K,1%	4.7K	.047UF	.01UF
-54-2	48 TPI, MFM SINGLE HEAD				PINS (4) 684-0004-3			IN				1.82K,1%	120Ω,1/2W					35.7K,1%	4.7K			
-55-9	100TPI, MFM DUAL HEAD	NE555 410-0555-4	2N4402 300-4402-8	IN4446 200-4446-7	HEADER 680-0506-5	HEADER 680-0505-7	IN		6.19K,1%	19.6K,1%	12K	3.16K,1%	390Ω,1/2W	390Ω,1/2W	1.5K	1K			35.7K,1%	22K	.047UF	.01UF
-56-7	100TPI, MFM SINGLE HEAD				PINS (4) 684-0004-3			IN				3.16K,1%	390Ω,1/2W					35.7K,1%	22K			

TABLE I

TABLE I (CONT.)

TABLE I (CONT.)

TABLE III

PART NO.	REF. DESIGNATION
100-0000-8	R42,52,53 W5,7,10
100-1000-7	R15,51
100-1500-6	R1,6,71,57,58
100-1800-0	R19
100-2200-2	R13,14,54,55,60
100-3300-9	R20,50,66,68
100-4700-3	R65,80,81,63,64
100-5600-0	R41
100-6800-5	R47
100-1001-5	R18,25,34,79,82,84
100-0470-3	R56
100-1501-4	R26,33,74,75
100-1801-8	R46
100-2201-0	R43,61,62
100-6801-3	R4
100-1002-3	R2
100-1202-9	R29,37,44,45,69
100-2202-8	R27,28,
100-2702-7	R48,49,76,78
100-4702-5	R11,12,17
100-1003-1	R16,70
101-0010-5	R83
101-0680-5	R7,8,9,10
105-1741-5	R5
105-6191-8	R21
105-1002-2	R73
105-1962-7	R22
130-2002-9	R3
130-2001-1	R59
130-1002-0	R72

PART NO.	REF. DESIGNATION
116-0002-0	RN1
115-0001-4	U17
160-3300-3	C35
160-1000-1	C4,14,39
160-1500-0	C37
160-4700-3	C9
160-7500-4	C38,36
161-1501-6	C28
161-4701-9	C25
161-2202-0	C32,33
162-4702-5	C10
163-2203-4	C1
163-4703-1	C29,30
163-3304-9	C24,26,40,42,47,48,49,51
163-3305-6	C3,44
163-1006-2	C5,6,7,8
165-1002-6	C2,12,15,19,20,21,22,27,31,34,41,43,46,50,52,53,54,55,56
190-0240-9	L3,L4
190-1000-8	L1,2,5
191-0100-5	L6
200-4446-7	CR9,11,12,14,15,16,17,18,22,23,24,25,26,27,28,29,30,32,33
210-5223-8	CR8
210-5237-8	CR2,31
220-4002-6	CR3,4,5,6,7,34
300-4400-2	Q1,6
300-4402-8	Q2,3,4

PART NO.	REF. DESIGNATION
340-0110-7	Q7
400-0000-2	U12,18
400-0002-8	U11
400-0014-3	U10,16
400-0027-5	U20
400-0051-5	U19
400-0074-7	U13,21,23
400-0086-1	U24
400-0123-2	U25
401-0016-6	U2,9
401-0017-4	U22
401-0038-0	U1
406-0451-4	U4,14
406-0452-2	U3,5
410-0311-2	U26
410-0555-4	U6,15
410-0592-7	U27,28
410-0741-0	U7
622-0001-9	CR1
680-0503-2	J2A
680-1001-6	J5
680-1601-3	J3
680-1701-1	J4
680-0802-8	W1,2,3,4
680-1603-9	U17
684-0001-9	W1,2,3,4
684-0003-5	TP1 THRU 10
650-0001-0	

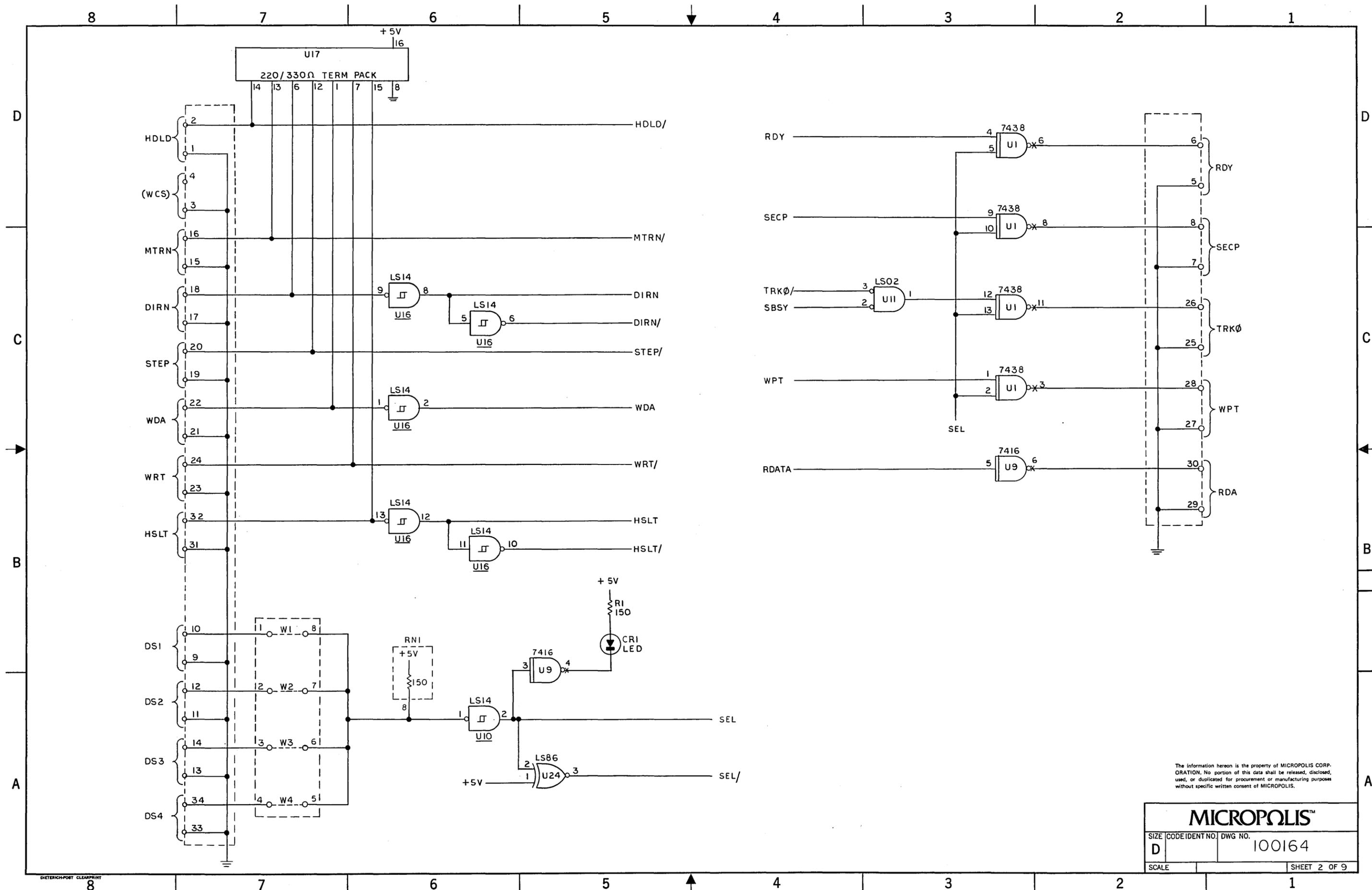
LAST USED	NOT USED	DELETED
U28		
CR34		
Q7		
R84		
RN1		
C56	C17,18,19,20,23	
L6		
J8		J7
W10		
TP10		

- 7 FOR LAST USED, NOT USED, AND DELETED REF DESIGNATION SEE TABLE III.
- 6 FOR COMPONENTS AFFECTED BY VERSION SEE TABLE II.
- 5 FOR PART NO. OF COMPONENTS NOT AFFECTED BY VERSION SEE TABLE I.
- 4. FOR PCBA SEE DRAWING NO. 100163.
- 3. ALL DIODES ARE IN4446
- 2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
- 1. ALL RESISTOR VALUES ARE IN OHMS.

NOTE: UNLESS OTHERWISE SPECIFIED:

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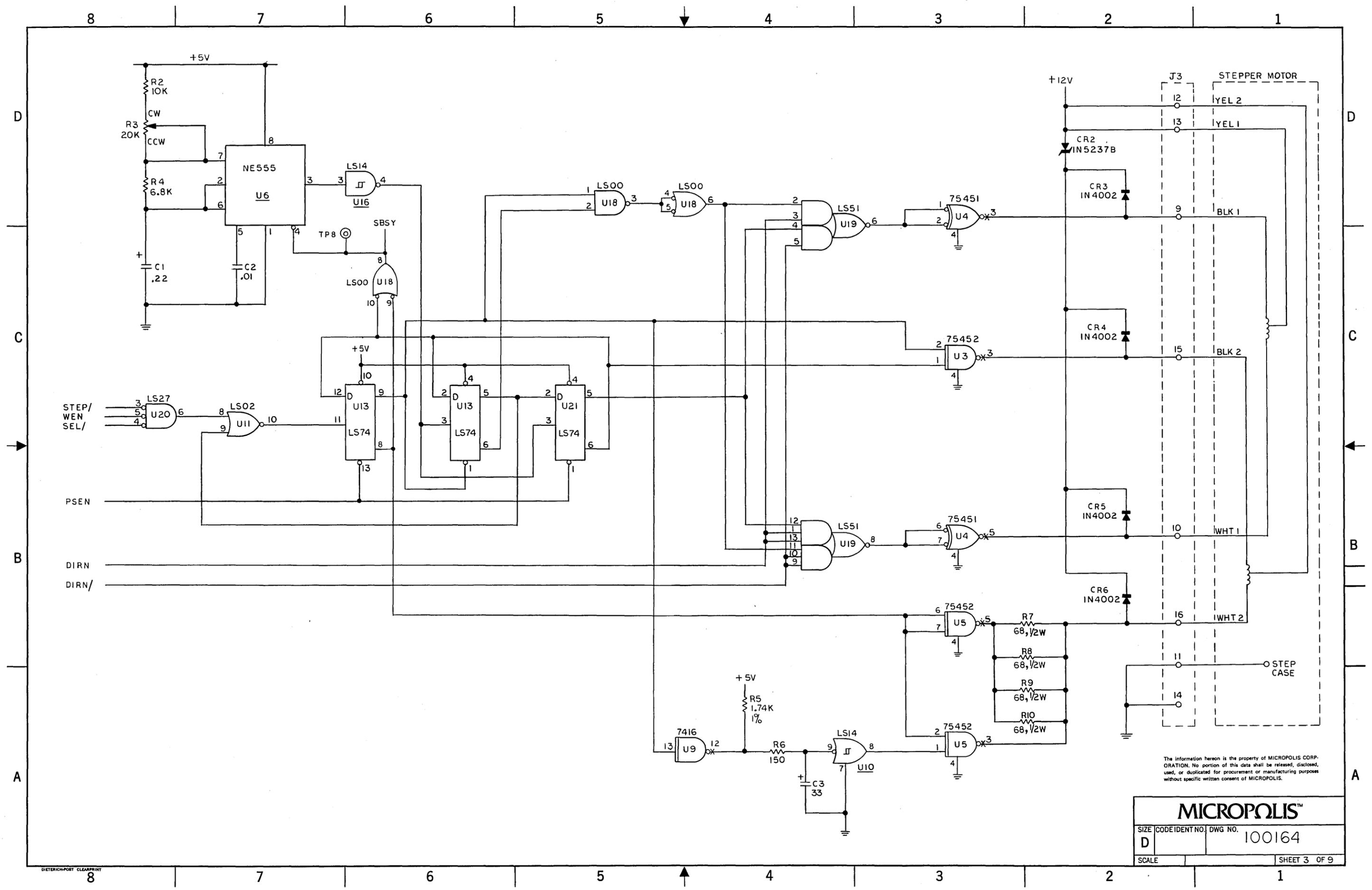
QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES.		CONTRACT NO.		
TOLERANCES ON:		DR BY		
FRAC TIONS	DECIMALS	ANGLES	CHK BY	
±	±	±	APPROVED BY	
MATERIAL		5/24/78		
FINISH		5/24/78		
NEXT ASSY		USED ON		
APPLICATION		DO NOT SCALE DRAWING		
SIZE	CODE IDENT NO.	DWG NO.	REV.	
D		100164	E	
SCALE			SHEET 1 OF 9	



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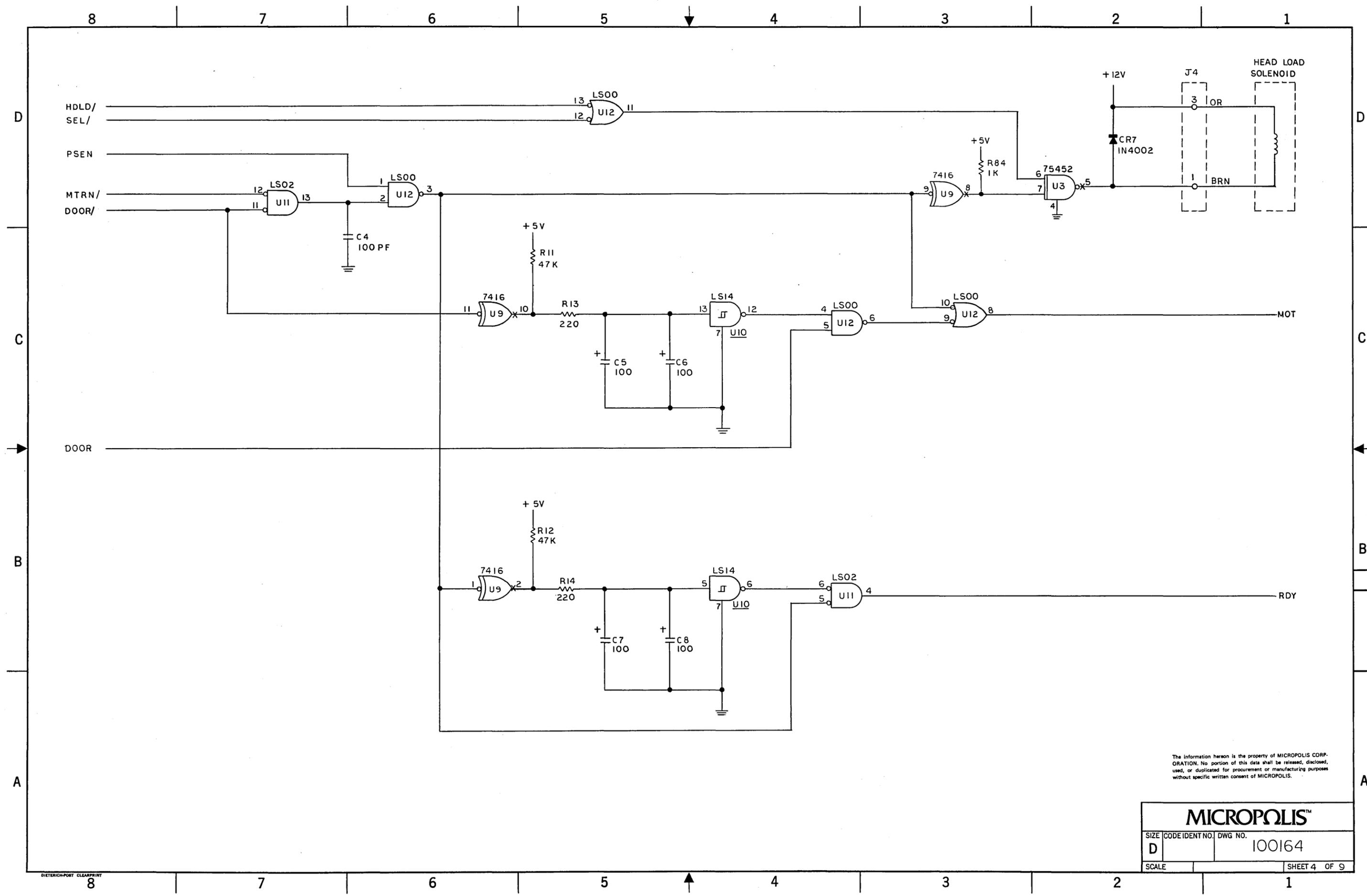
<b>MICROPOLIS™</b>	
SIZE	D
CODE IDENT NO.	100164
DWG NO.	100164
SCALE	SHEET 2 OF 9

DIETERICH-POST CLEARPRINT



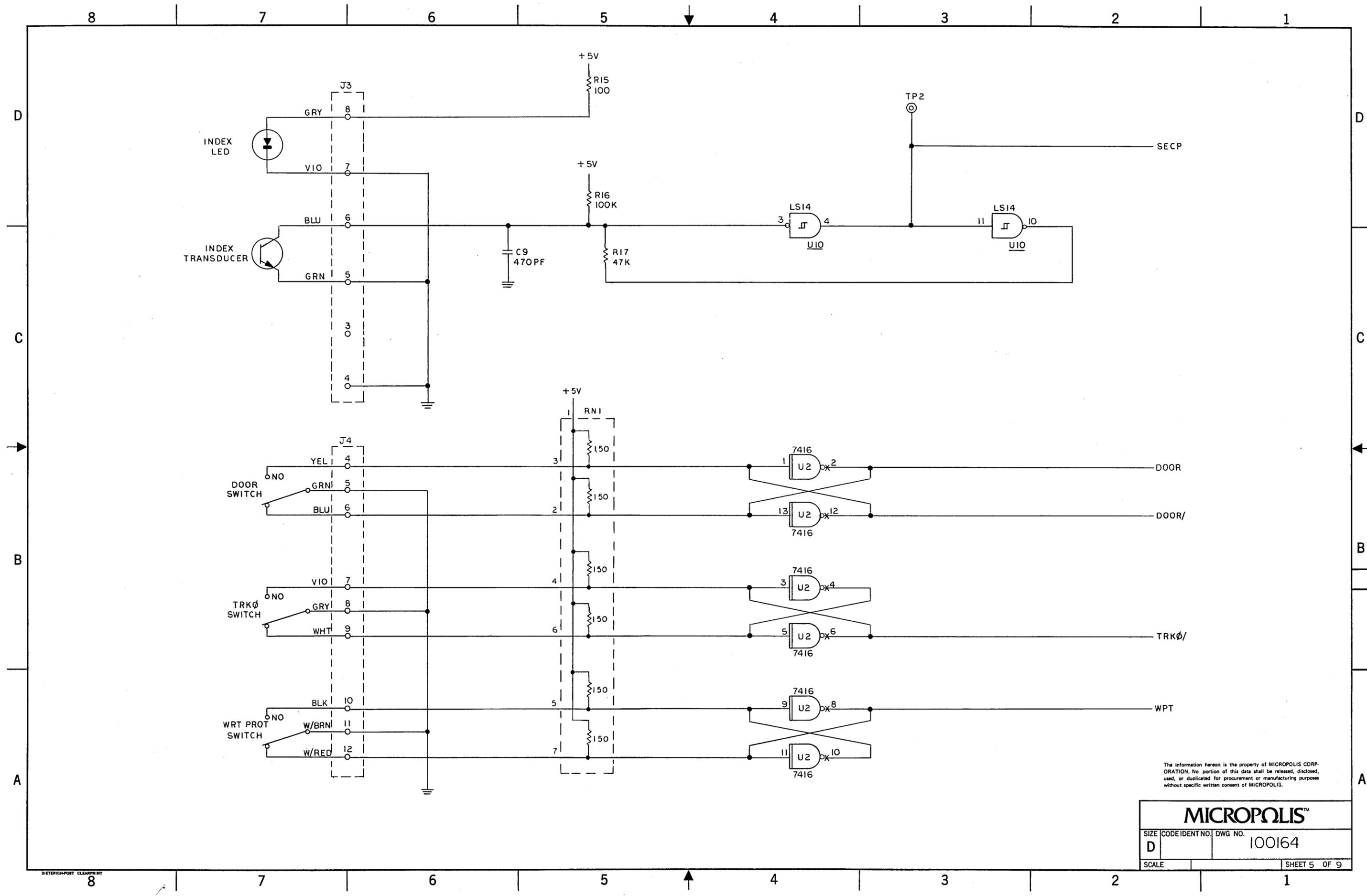
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<b>MICROPOLIS™</b>		
SIZE	CODE IDENT NO.	DWG NO.
D		100164
SCALE	SHEET 3 OF 9	



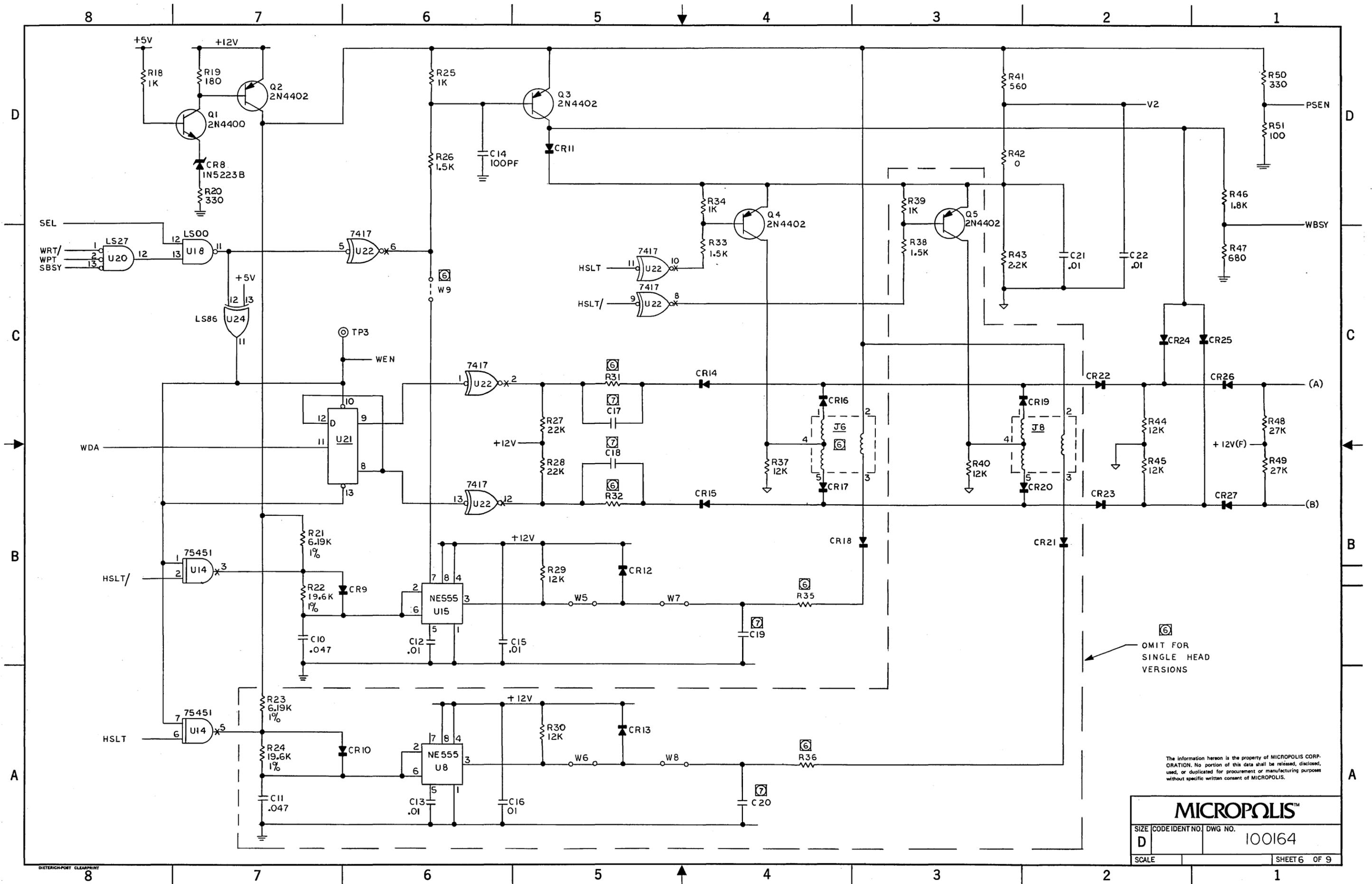
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<b>MICROPOLIS™</b>		
SIZE <b>D</b>	CODE IDENT NO.	DWG NO. 100164
SCALE	SHEET 4 OF 9	



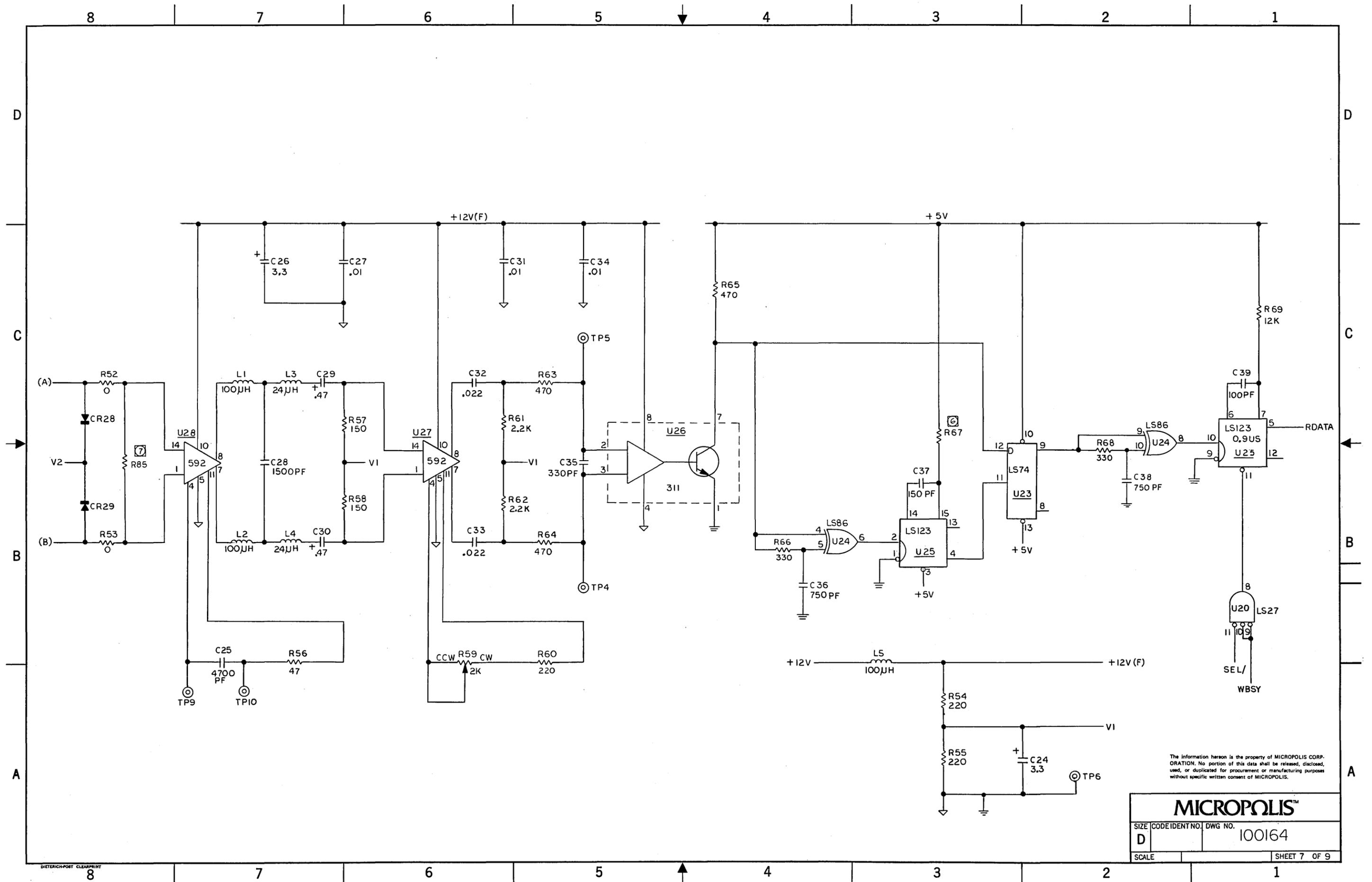
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<b>MICROPOLIS™</b>		
SIZE	CODE IDENT NO.	DWG NO.
D		100164
SCALE		SHEET 5 OF 9



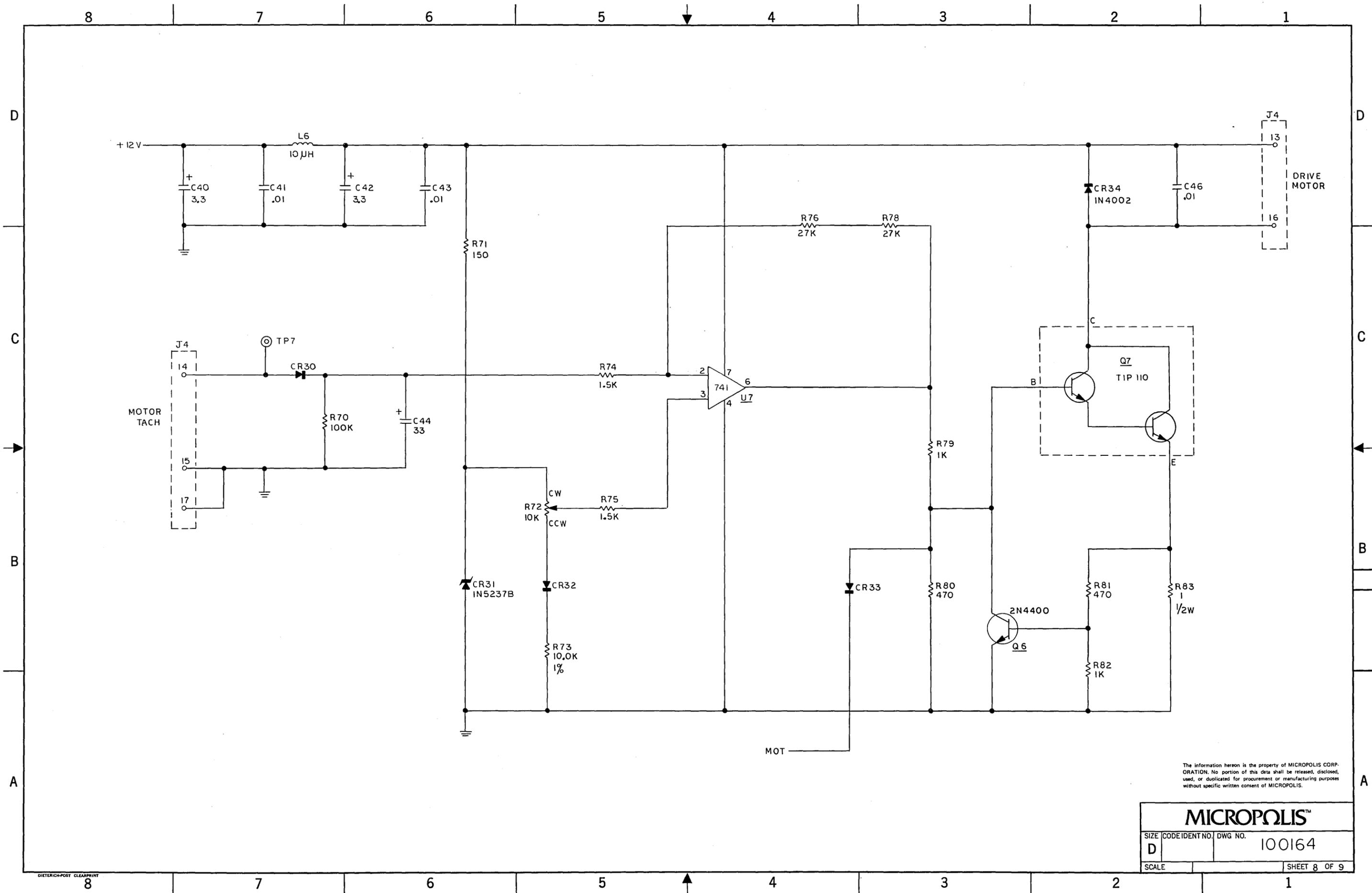
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<b>MICROPOLIS™</b>		
SIZE	CODE IDENT NO.	DWG NO.
D		100164
SCALE	SHEET 6 OF 9	



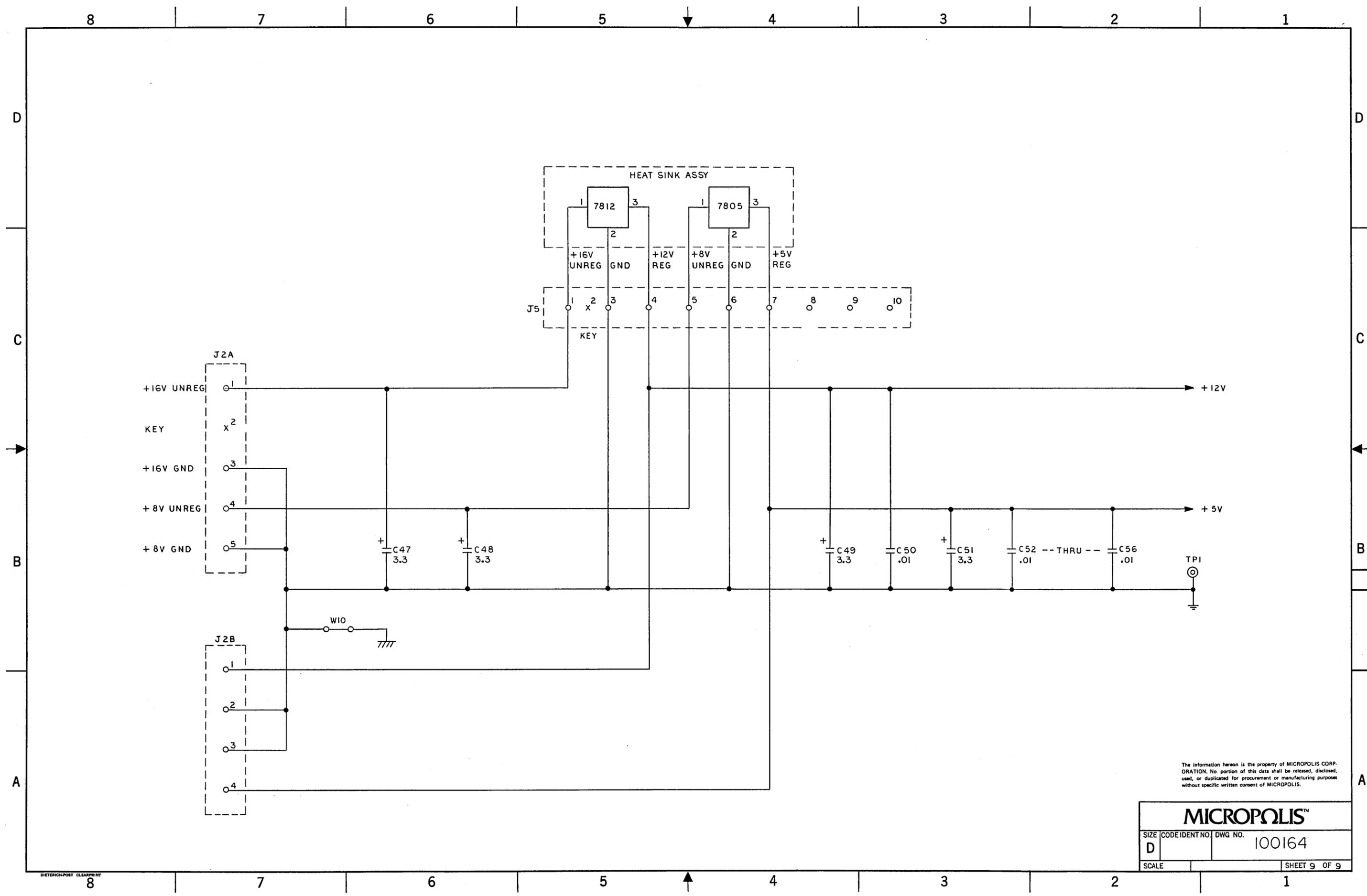
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<b>MICROPOLIS™</b>	
SIZE	CODE IDENT NO. DWG NO.
D	100164
SCALE	SHEET 7 OF 9



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<b>MICROPOLIS™</b>	
SIZE	CODE IDENT NO. DWG NO.
D	100164
SCALE	SHEET 8 OF 9

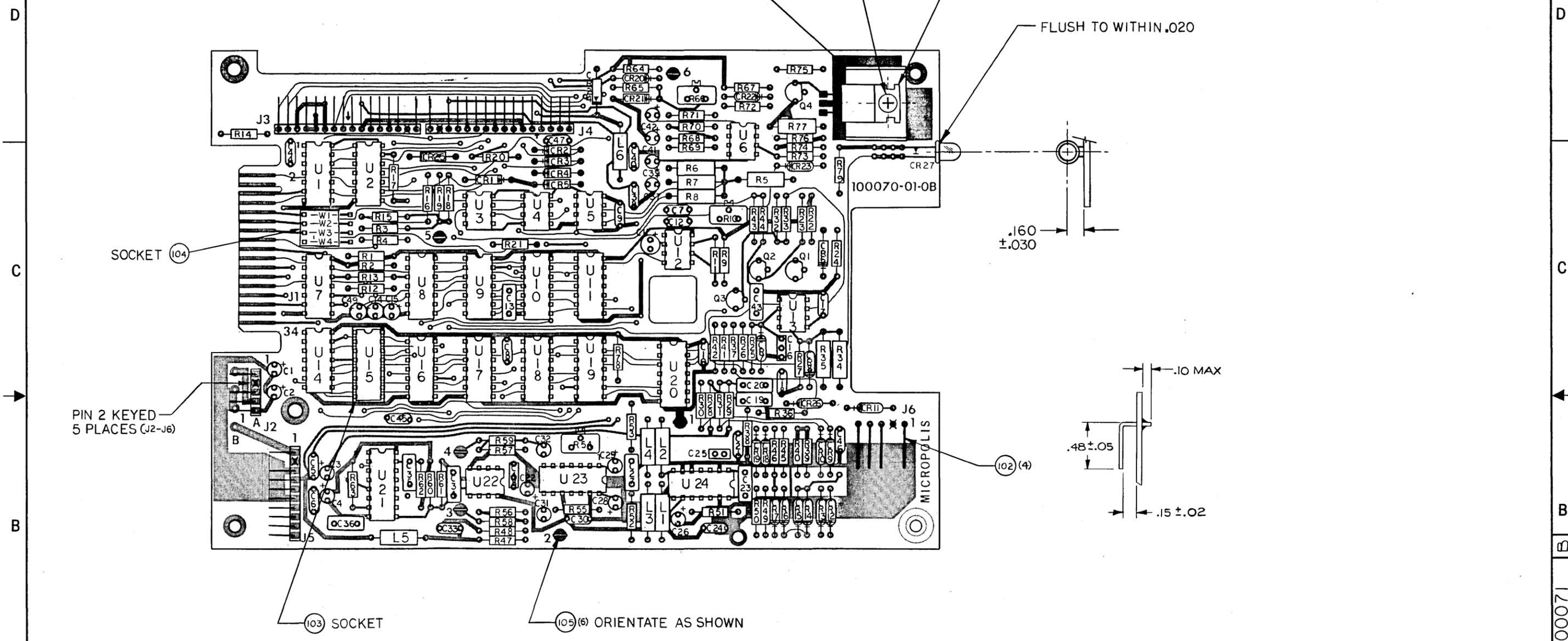


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<b>MICROPOLIS™</b>	
SIZE	CODE IDENT NO.   DWG NO. 100164
D	
SCALE	SHEET 9 OF 9

8 7 6 5 4 3 2 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B	REVISED AND REDRAWN	5-15-77	<i>S.M.</i>
	C	REVISED EN 0079	2-27-78	<i>S.M.</i>



SEE P/L

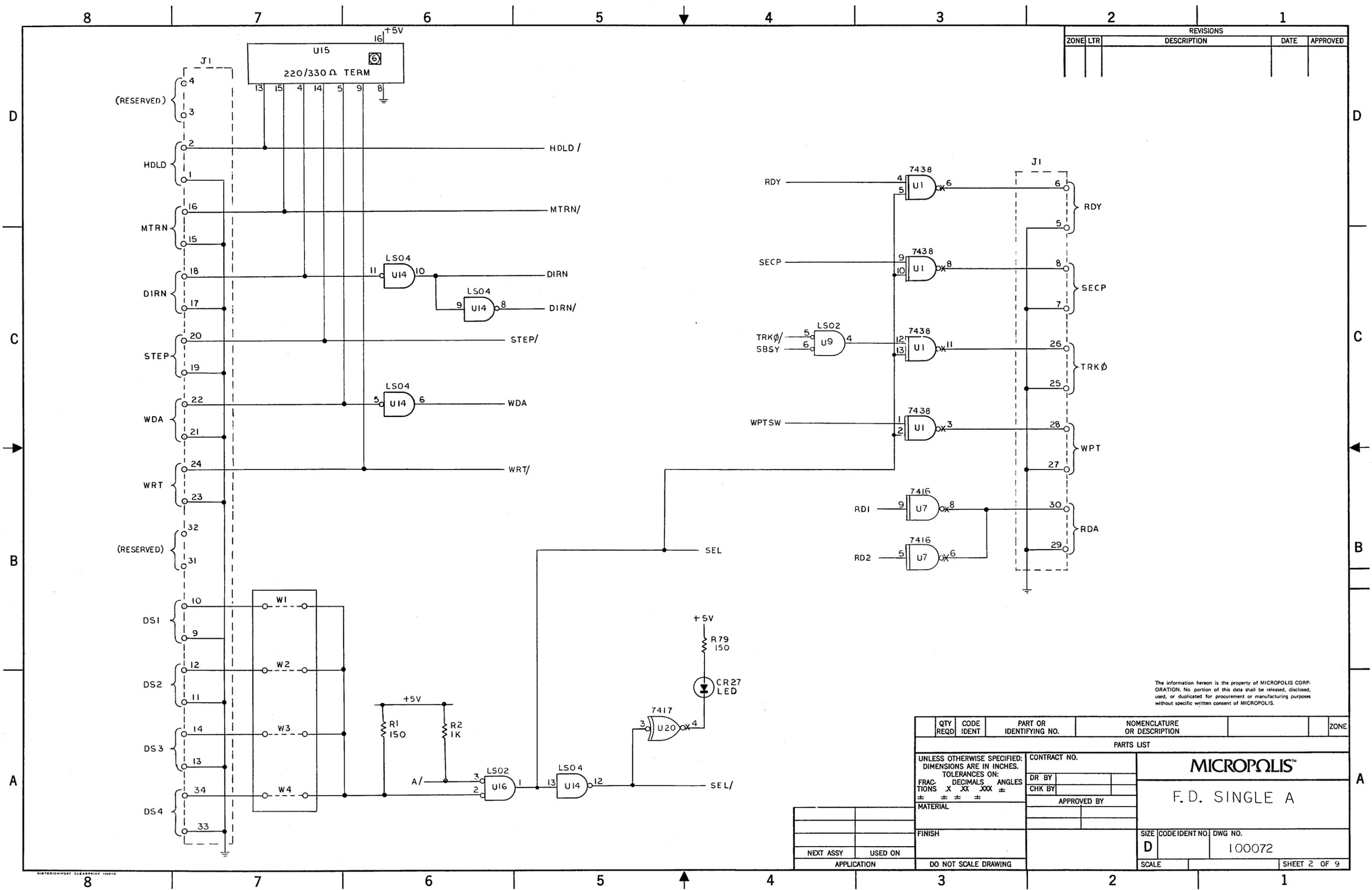
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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS .XX .XXX ± DECIMALS .XX .XXX ± ANGLES ± ± ±		CONTRACT NO.		<b>MICROPOLIS™</b>  PCBA, FD SINGLE A
MATERIAL		DR BY J. Fazio 5-15-77	CHK BY	
FINISH		APPROVED BY <i>E.D. Janssen</i> 7-22-77 <i>S.M.</i> 7-22-77		
NEXT ASSY	USED ON	SIZE CODE IDENT NO. DWG NO.		REV
APPLICATION	DO NOT SCALE DRAWING	D 100071		C
SCALE 2/1				SHEET OF

8 7 6 5 4 3 2 1

100071





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

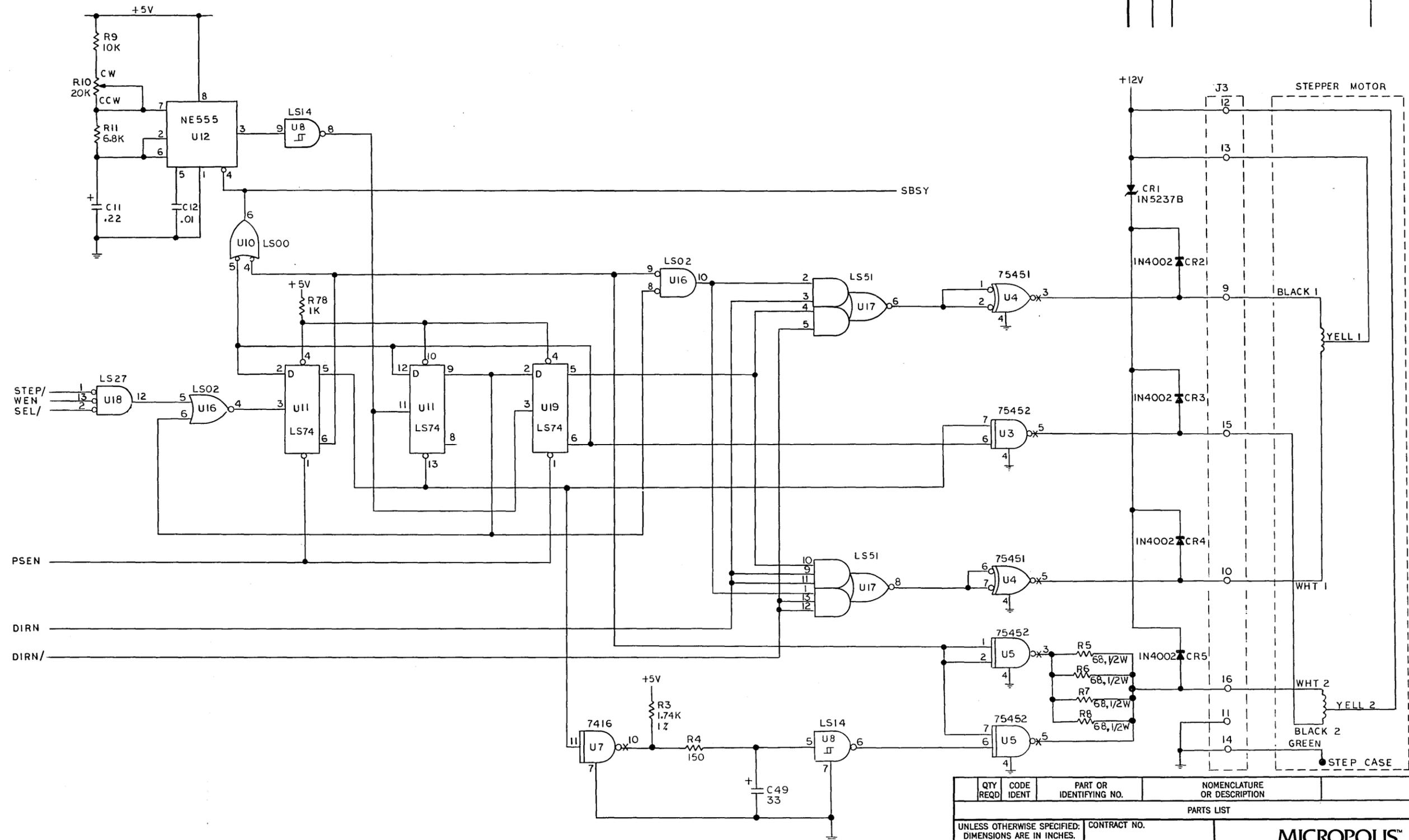
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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC. DECIMALS ANGLES TIONS X XX XXX ± ± ± ±		CONTRACT NO.		<b>MICROPOLIS™</b>  F.D. SINGLE A
MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY		APPROVED BY		SIZE
APPLICATION		DO NOT SCALE DRAWING		CODE IDENT NO. DWG NO. D 100072
SCALE				SHEET 2 OF 9

8 7 6 5 4 3 2 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

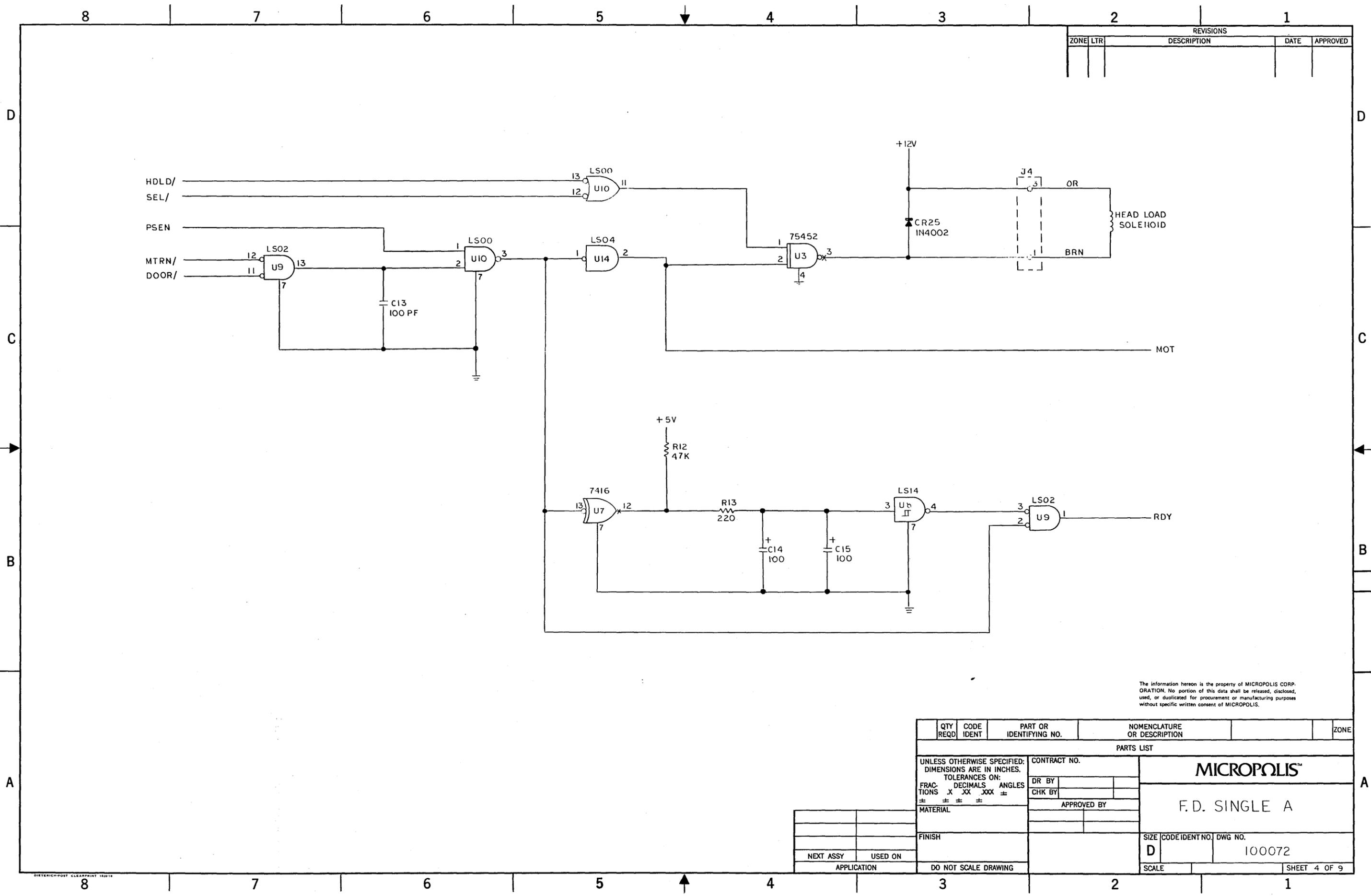
D  
C  
B  
A



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X XX XXX ± DECIMALS ANGLES ± ± ± ±		CONTRACT NO.		MICROPOLIS™
MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY		USED ON		F.D. SINGLE A
APPLICATION		DO NOT SCALE DRAWING		SIZE CODE IDENT NO. DWG NO. D 100072
				SCALE SHEET 3 OF 9

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8 7 6 5 4 3 2 1



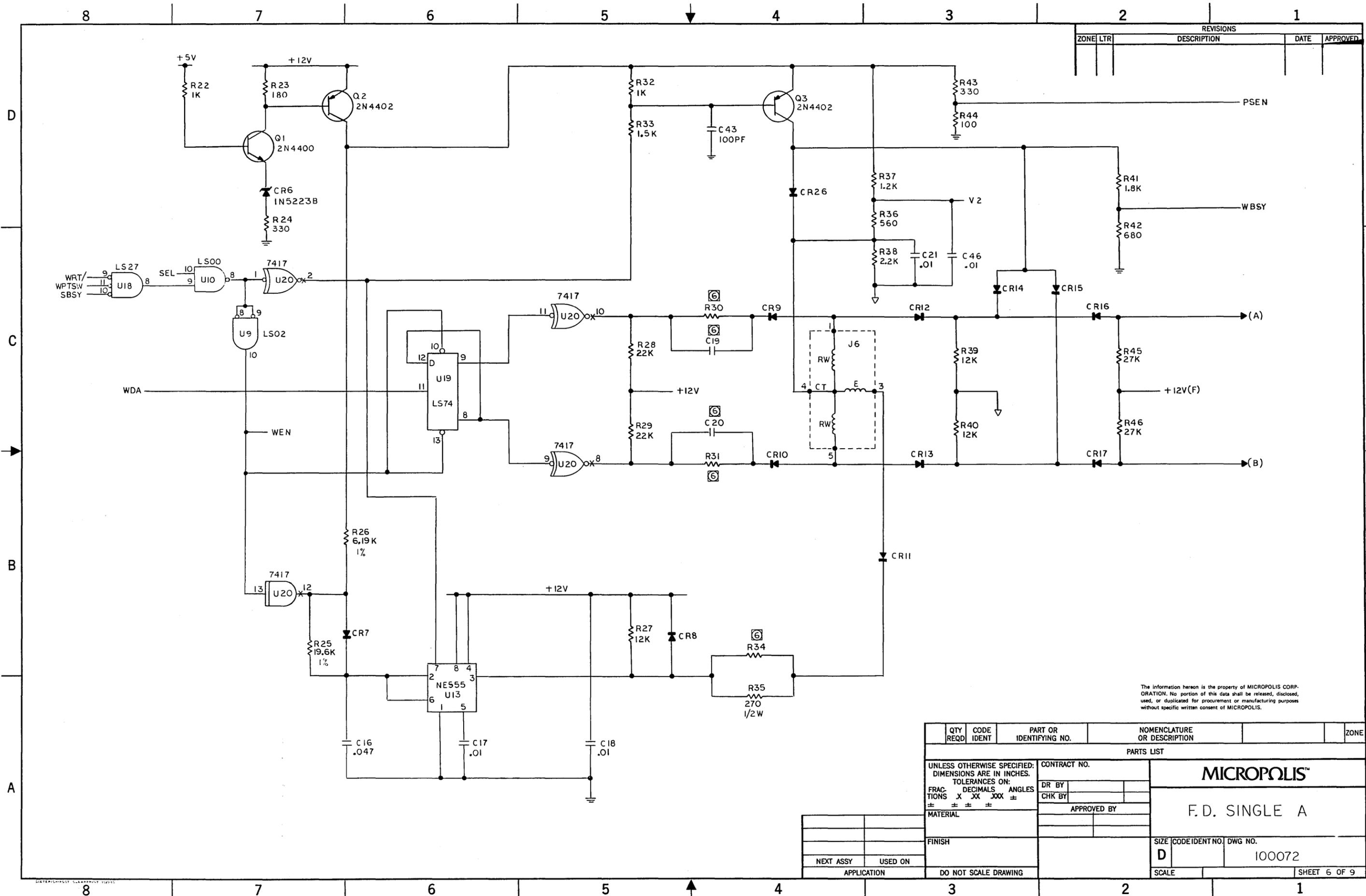
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC. DECIMALS ANGLES TIONS .X .XX .XXX ±		CONTRACT NO.		<b>MICROPOLIS™</b>  F.D. SINGLE A
MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY		USED ON		
APPLICATION		DO NOT SCALE DRAWING		SIZE CODE IDENT NO. DWG NO. D 100072
				SCALE SHEET 4 OF 9



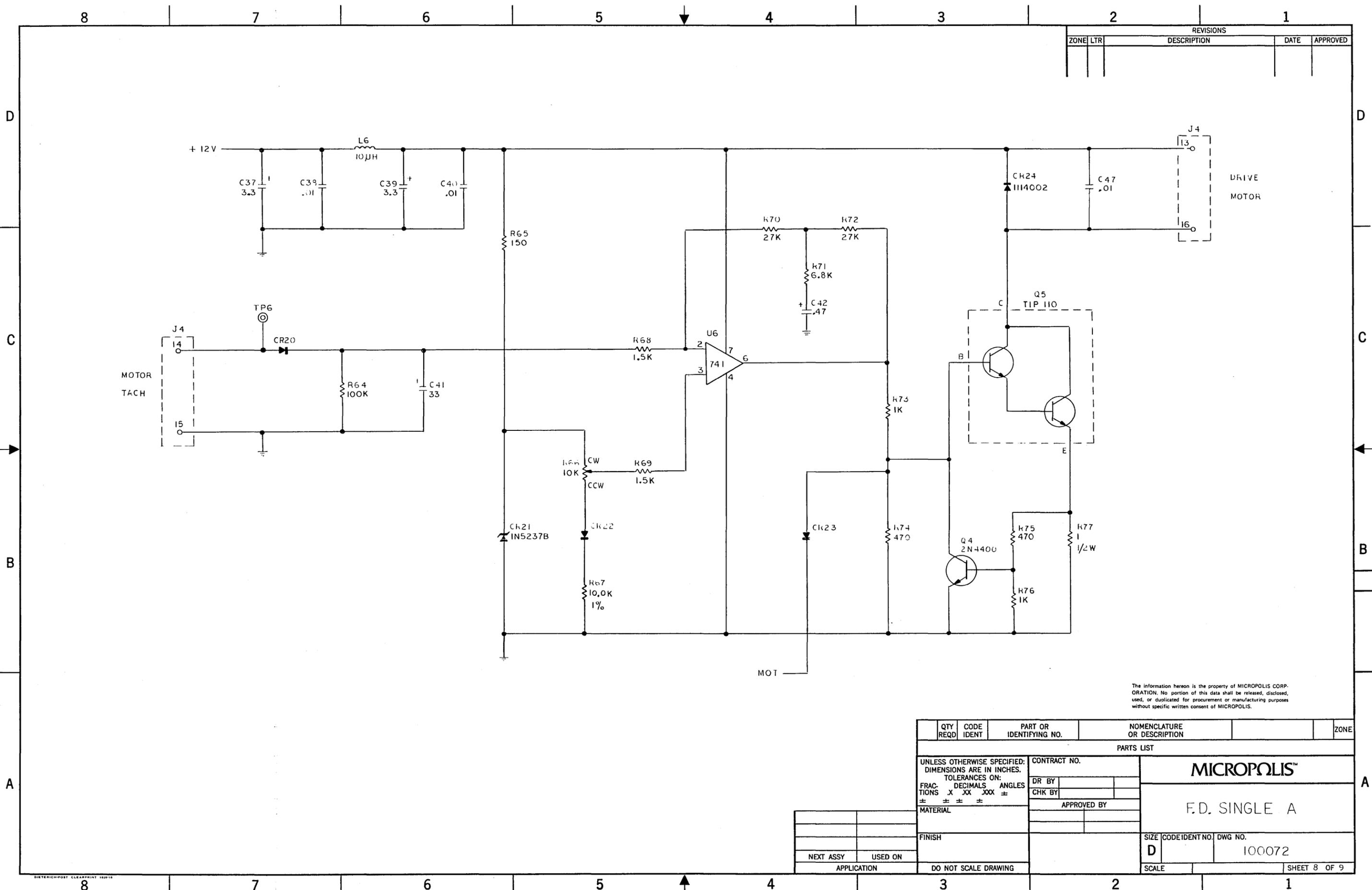
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X XX XXX ± DECIMALS ANGLES ± ± ± ±		CONTRACT NO.		
MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY		APPROVED BY		
USED ON				
APPLICATION				
DO NOT SCALE DRAWING				
		<b>MICROPOLIS™</b>		
		F.D. SINGLE A		
		SIZE	CODE IDENT NO.	DWG NO.
		D		100072
		SCALE	SHEET 6 OF 9	





REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC. DECIMALS ANGLES X XX .XXX ± ± ± ± ±		CONTRACT NO.		<b>MICROPOLIS™</b>  F.D. SINGLE A
MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY		USED ON		APPROVED BY
APPLICATION		DO NOT SCALE DRAWING		SCALE
SIZE			CODE IDENT NO.	DWG NO.
D				100072
SHEET 8 OF 9				

8

7

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4

3

2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

D

D

C

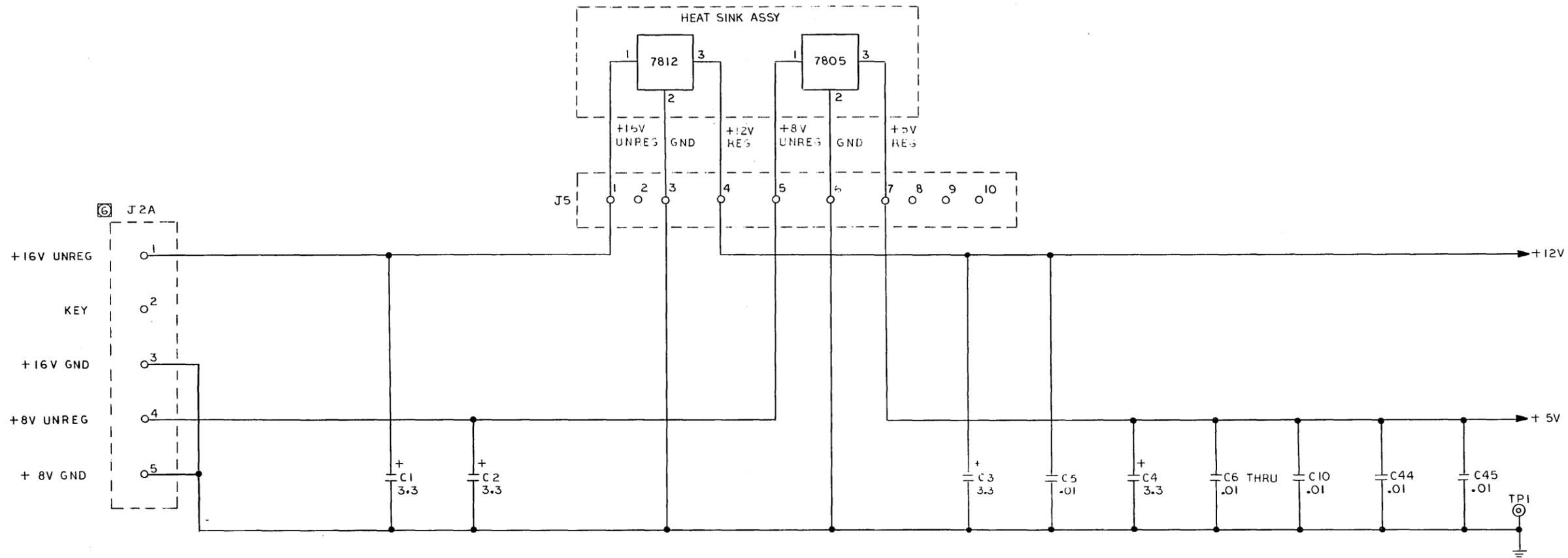
C

B

B

A

A



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QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE
PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC. DECIMALS ANGLES X XX XXX ± ± ± ± ±		CONTRACT NO.		<b>MICROPOLIS™</b>
MATERIAL		DR BY		
FINISH		CHK BY		F.D. SINGLE A
NEXT ASSY		APPROVED BY		
USED ON		SCALE		SIZE CODE IDENT NO. DWG NO.
APPLICATION		DO NOT SCALE DRAWING		D 100072
				SHEET 9 OF 9

8

7

6

5

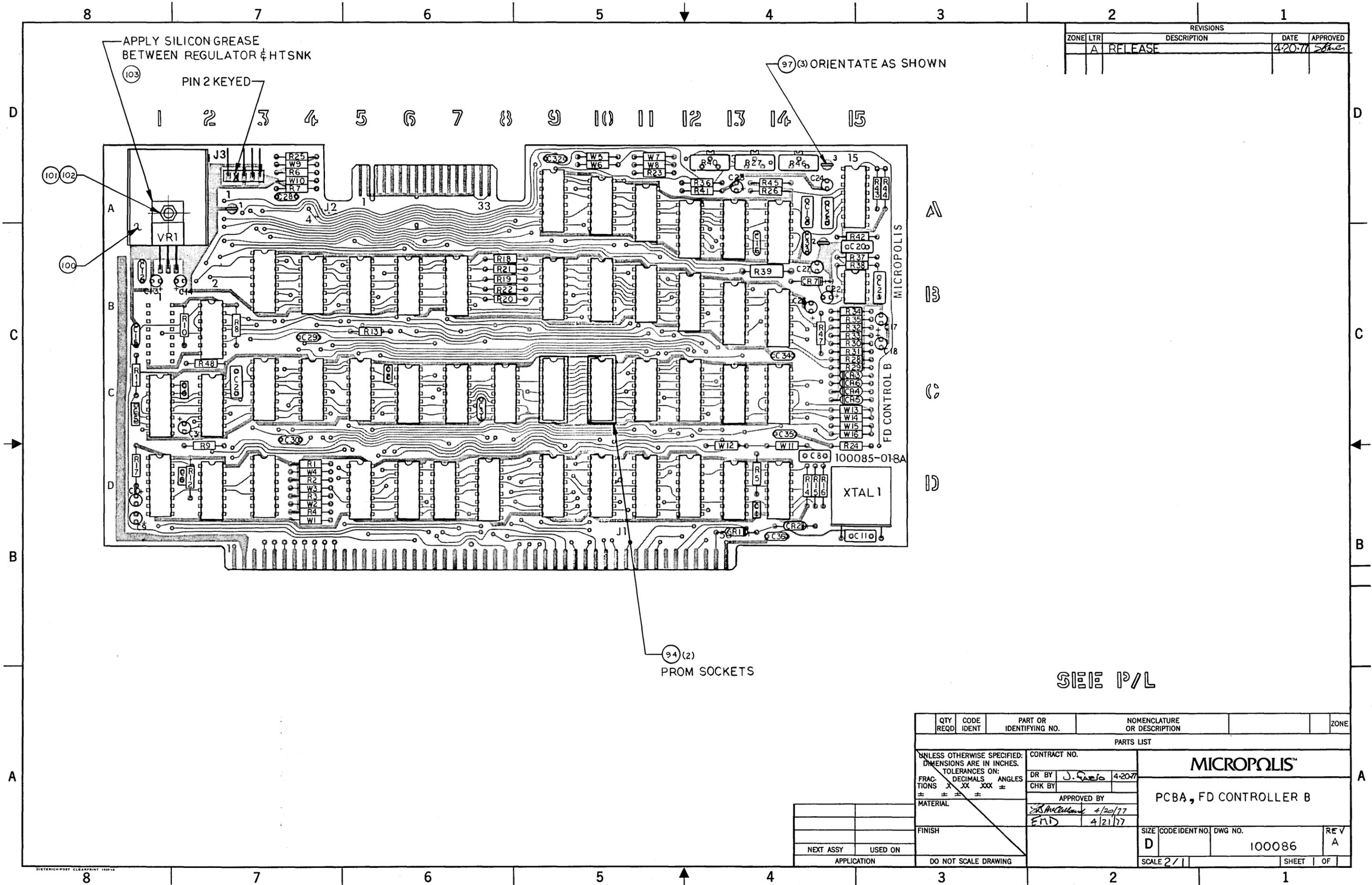
4

3

2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE	4-20-77	<i>Sh...</i>



SEE P/L

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	ZONE	
PARTS LIST					
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X XX XXX ± DECIMALS     ANGLES     ± ± ± ±		CONTRACT NO.	<b>MICROPOLIS™</b>  PCBA, FD CONTROLLER B		
MATERIAL		DR BY <i>J. Saeio</i> 4-20-77 CHK BY APPROVED BY <i>J. McCallum</i> 4/20/77 END 4/21/77			
FINISH		SIZE	CODE IDENT NO.	DWG NO.	REV
NEXT ASSY		D		100086	A
APPLICATION		SCALE 2/1		SHEET OF	
DO NOT SCALE DRAWING					

8

7

6

5

4

3

2

1

TABLE I

PART NO.	REF. DESIGNATION
100-0100-6	R47
-0680-7	R 32, 33
-1500-6	R18,19,20,21,22
-2200-2	R28,29
-4700-3	R13,42
-1202-9	R26,45
-1001-5	R1,2,3,4,6,7,14, 15,23,24,25,48
-1801-8	R30,31
-1502-2	R8
-3902-2	R12
-2203-6	R17
-3301-7	R16
-0000-8	H5,41
101-5600-8	R39
105-2150-8	R36,43
-5110-9	R44
-1782-9	R34,35
-3832-0	R11
-4642-2	R10
-6192-6	R9
-2153-2	R37,38
130-1002-0	R27,46
-1000-4	R40
160-0330-3	C11,20,21
-0750-2	C19
-1000-1	C2
-1500-0	C16
-7500-4	C5
161-2201-3	C6,7
-2202-0	C4
162-4702-5	C5
163-2203-4	C3
-1004-7	C17,18
-3304-9	C13,14,22,23,26,27

TABLE I (CONT.)

PART NO.	REF. DESIGNATION
165-1002-6	C12,15,28 THRU 36
173-1006-1	C9,10
200-4446-7	CR1 THRU 6
210-5231-1	CR7
380-7805-1	VR1
400-0000-2	B14, D5
-0002-6	B4, D6, D13
-0004-4	B7, C7, D14
-0008-5	C6
-0010-1	B11, C8
-0014-3	D7
-0042-4	C3
-0051-5	A11
-0074-7	A10, B2, B12, D2
-0107-5	A12, A13, C14
-0123-2	D1
-0124-0	A15
-0161-2	A9, B10, B13, C3
-0164-6	C13
-0175-2	B3
-0221-4	A14, C1, C2
-0257-8	C4, C5, C11, C12
401-0016-6	B6
-0038-0	B5
-0166-9	B9
-0367-3	D9, D10, D11, D12
408-0003-9	D8
410-0318-7	B15
650-0002-8	HEATSINK
680-1603-9	SOCKET C9, C10
-0503-2	CONNECTOR J3
684-0003-5	TPI, 2, 3

TABLE II

ASSY. 100086 DASH NO	VERSION CHARACTERISTIC	JUMPERS (PART NO. 100-0000-8)																XTALI	C 24 C1	C 25	PROM C10	PROM C9
		W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16					
-01-6	ADDRESS F4 MFM EXT OSC.			X			X	X				X		X		X			100 PF 160-1000-1	800001-01-8	800001-02-6	
-02-4	ADDRESS F4 MFM INT OSC.			X			X	X			X		X		X		2.0 MHZ 500-2004-9		100 PF 160-1000-1	800001-01-8	800001-02-6	
-03-2	ADDRESS F4 DF EXT OSC.			X		X		X			X	X		X				150 PF 160-1500-0	800001-01-8	800001-02-6		
-04-0	ADDRESS F4 DF INT OSC.			X		X		X			X		X		X		2.0 MHZ 500-2004-9		150 PF 160-1500-0	800001-01-8	800001-02-6	
-52-9	ADDRESS F4 MFM, INT OSC, RELOC. PROMS			X			X	X			X		X		X		2.0 MHZ 500-2004-9		100 PF 160-1000-1	800003-01-4	800003-02-2	

TABLE III

LAST USED	DELETED
R48	
C36	
CR7	
VR1	
XTALI	
TP3	
J3	
W16	
U47	

- ⑦ FOR LAST USED AND DELETED REF DESIGNATION SEE TABLE III.
- ⑥ FOR COMPONENTS AFFECTED BY VERSION SEE TABLE II.
- ⑤ FOR PART NO OF COMPONENTS NOT AFFECTED BY VERSION SEE TABLE I.
- 4. FOR PCBA SEE DRAWING NO. 100086.
- 3. ALL DIODES ARE IN4446.
- 2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
- 1. ALL RESISTOR VALUES ARE IN OHMS.  $\sqrt{4W}$ ,  $\pm 5\%$ .

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PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRAC- DECIMALS ANGLES TIONS X XX XXX ± ± ± ± ±		CONTRACT NO.		<b>MICROPOLIS™</b>
MATERIAL		APPROVED BY <i>[Signature]</i> 4/77		
FINISH		F.D. CONTROLLER B		F.D. CONTROLLER B
NEXT ASSY USED ON		SIZE CODE IDENT NO. DWG NO. 100087 REV C		
APPLICATION		DO NOT SCALE DRAWING		SHEET 1 OF 9

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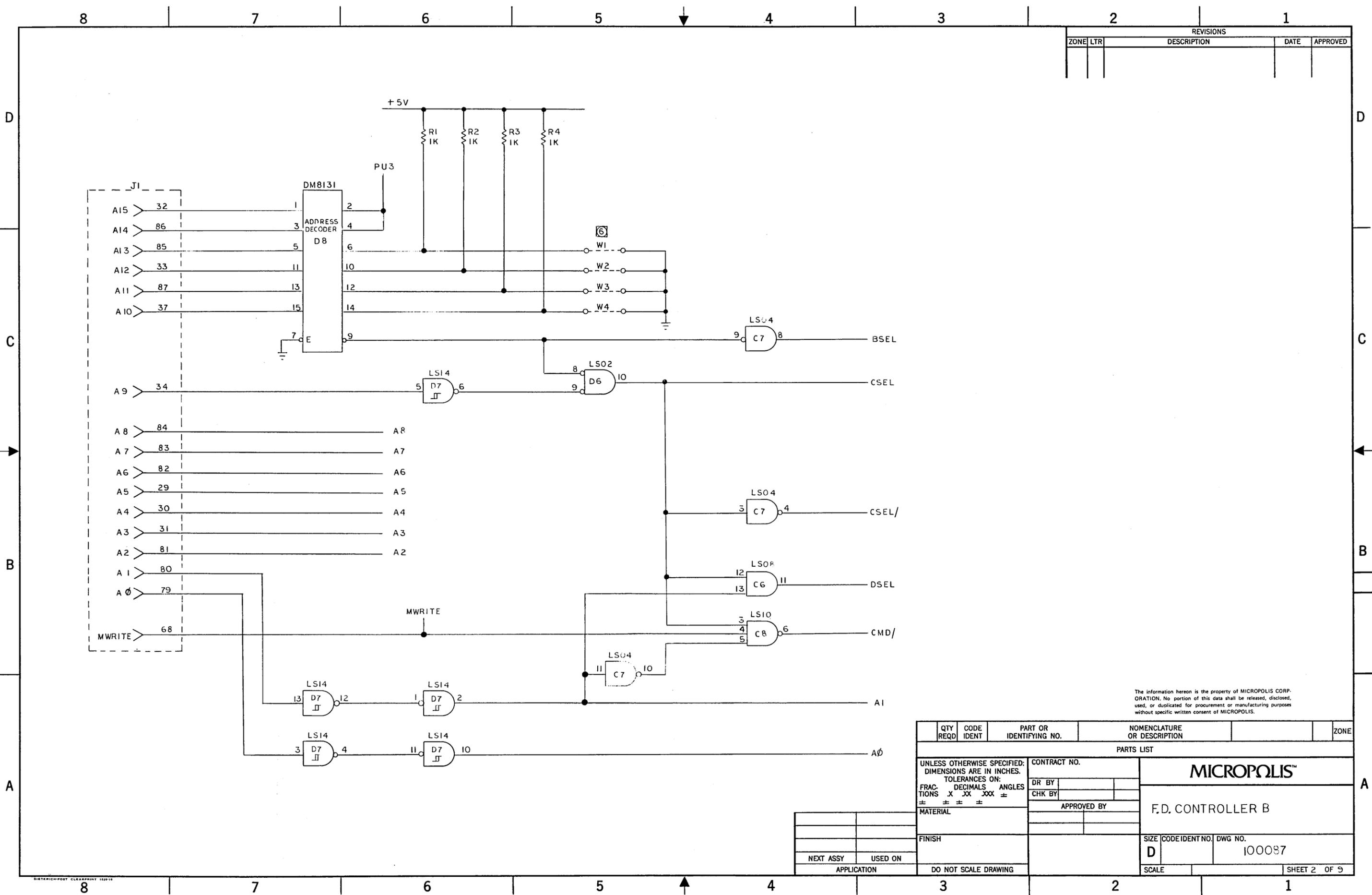
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TOLERANCES ON:		DR BY		
FRAC-	DECIMALS	ANGLES	CHK BY	
±	±	±	±	APPROVED BY
MATERIAL				F.D. CONTROLLER B
FINISH				SIZE CODE IDENT NO. DWG NO.
NEXT ASSY		USED ON		D 100087
APPLICATION		DO NOT SCALE DRAWING		SCALE SHEET 2 OF 9

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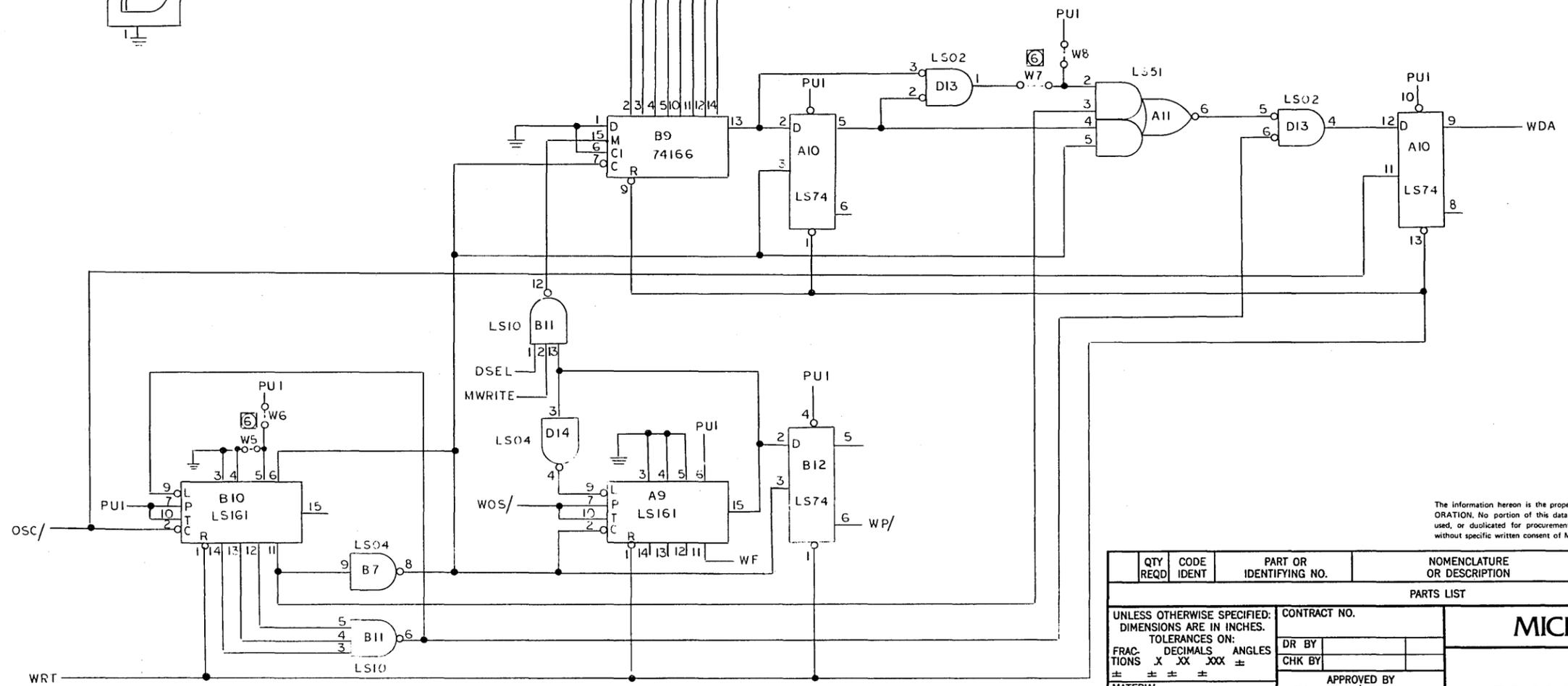
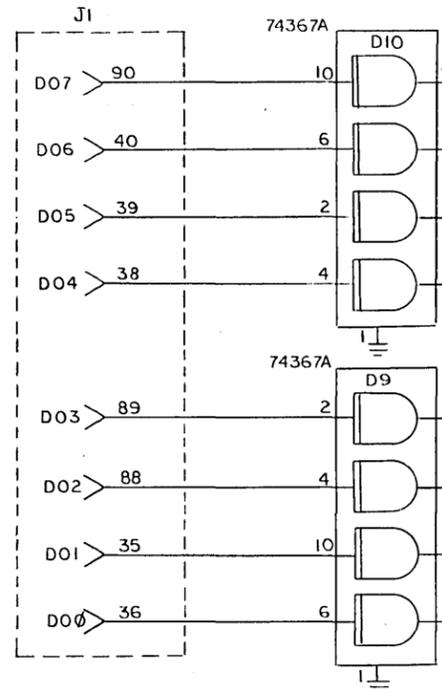
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PARTS LIST				
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X XX .XXX ± DECIMALS ANGLES ±			CONTRACT NO.	
MATERIAL			DR BY	
FINISH			CHK BY	
NEXT ASSY			APPROVED BY	
USED ON			MICROPOLIS™	
APPLICATION			F.D. CONTROLLER B	
DO NOT SCALE DRAWING			SIZE CODE IDENT NO. DWG NO.	
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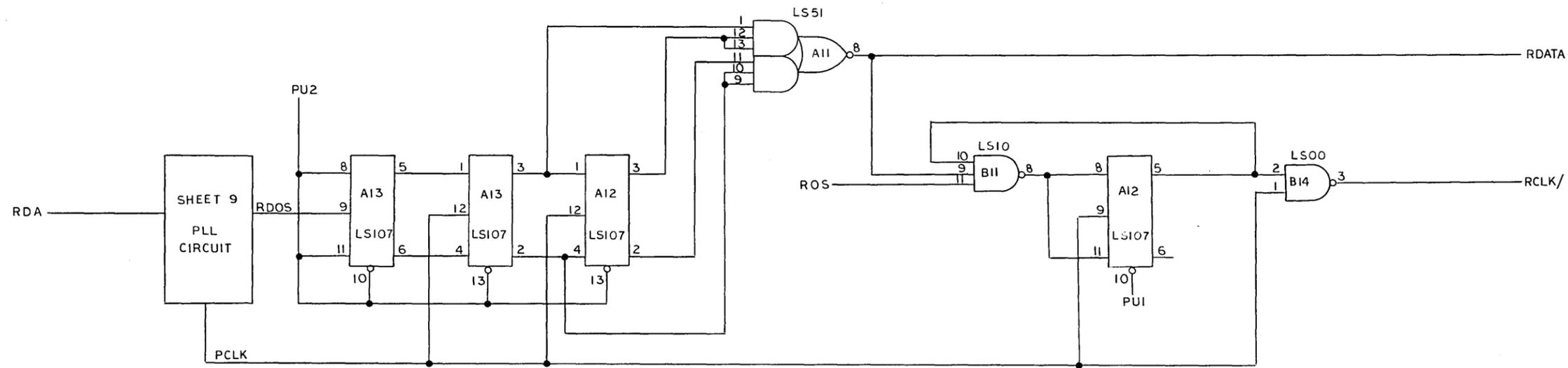
2

1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

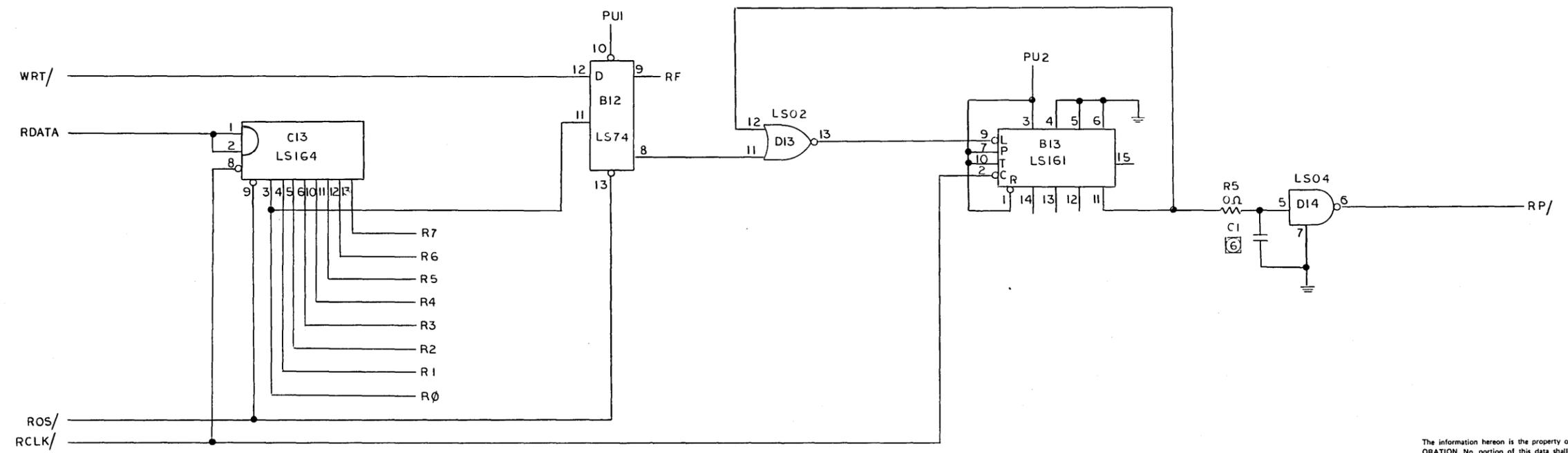
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MATERIAL		DR BY		
FINISH		CHK BY		
NEXT ASSY		USED ON		APPROVED BY
APPLICATION		DO NOT SCALE DRAWING		SCALE
SIZE			CODE IDENT NO.	DWG NO.
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SHEET 4 OF 9				

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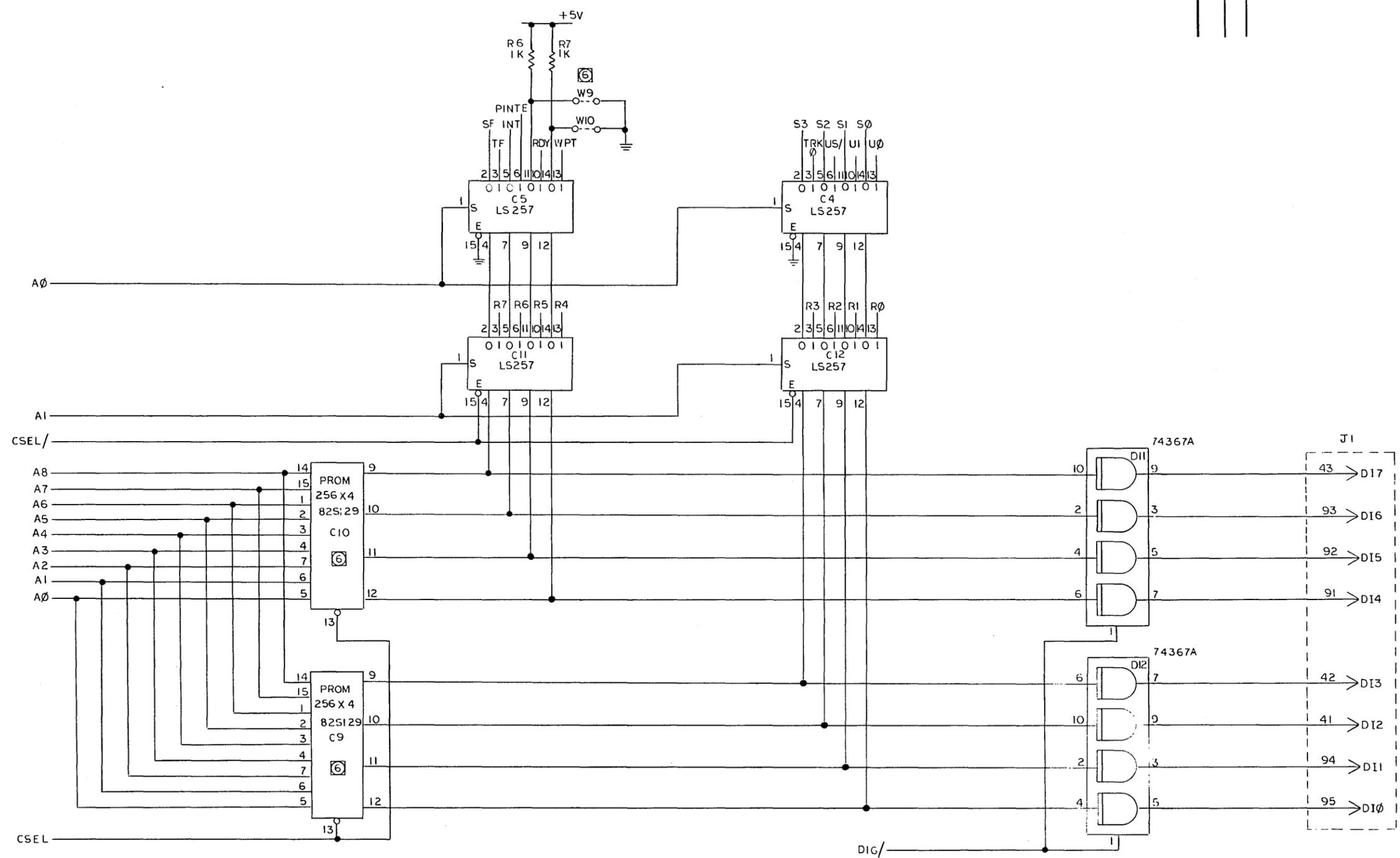
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FRAC.	DECIMALS	ANGLES	DR BY	<b>MICROPOLIS™</b>
TIONS .X	XX	XXX ±	CHK BY	
±	±	±	±	APPROVED BY
MATERIAL		F.D. CONTROLLER B		
FINISH				
NEXT ASSY	USED ON	SIZE	CODE IDENT NO.	DWG NO.
APPLICATION		D		100087
DO NOT SCALE DRAWING		SCALE	SHEET 5 OF 9	

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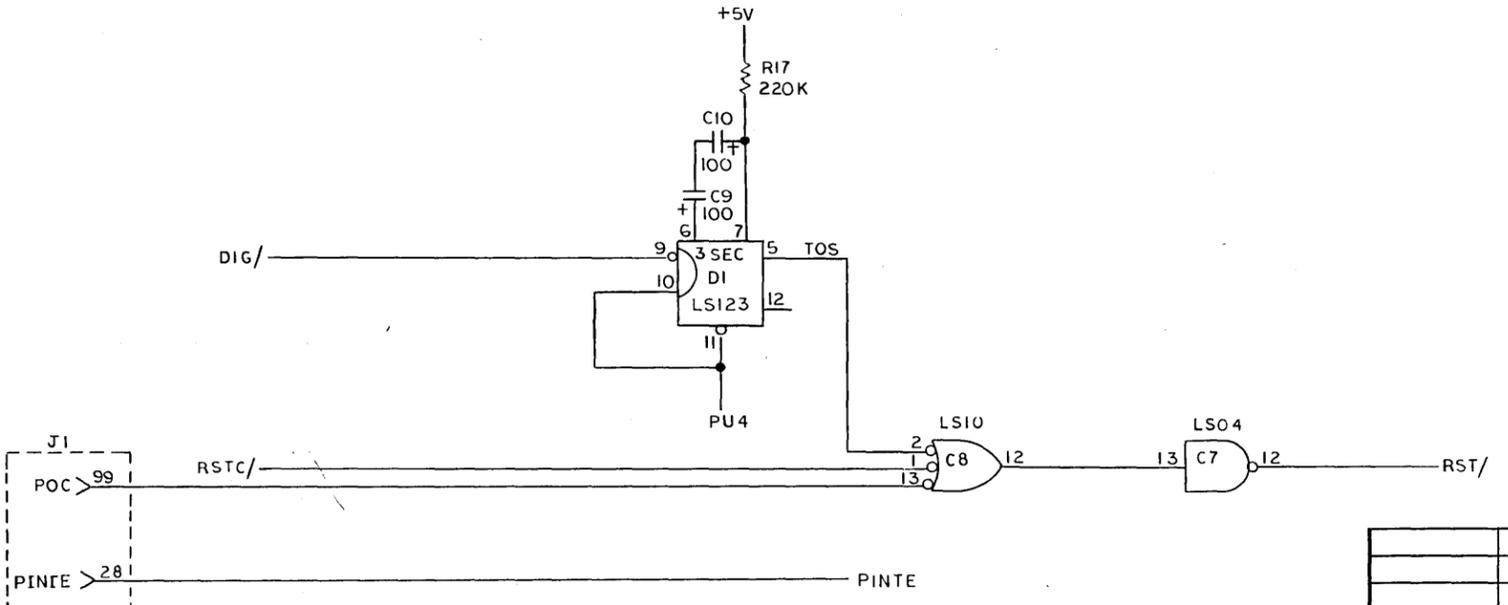
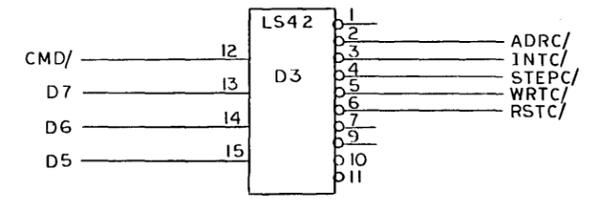
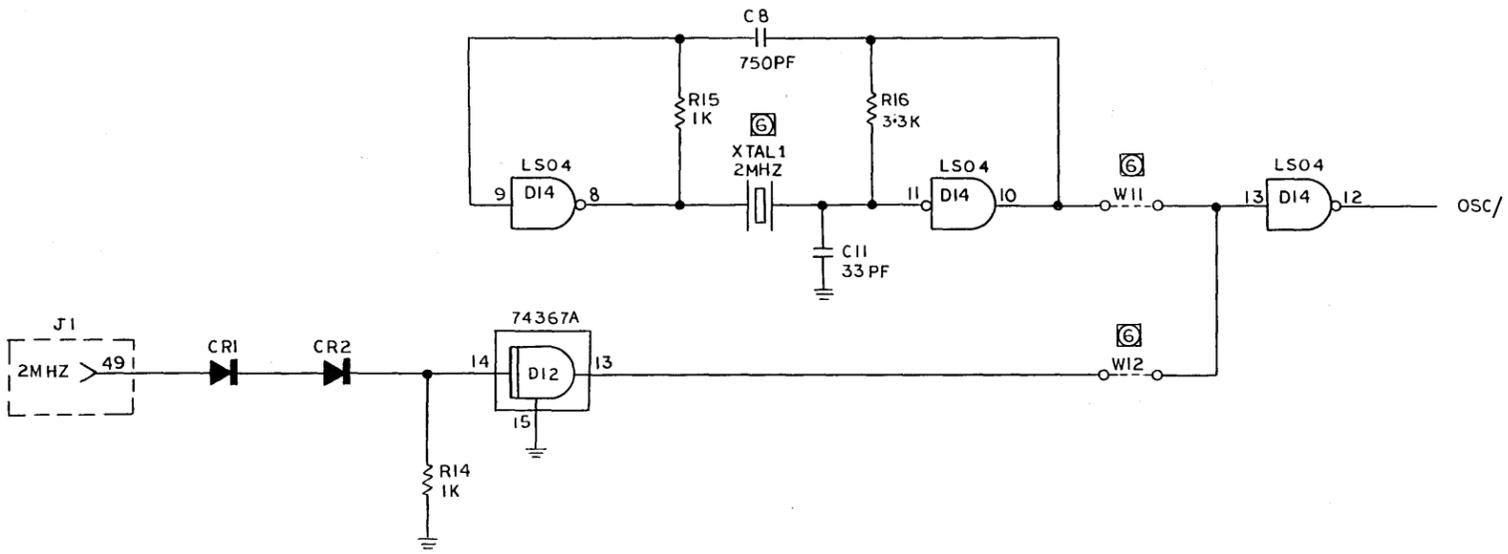
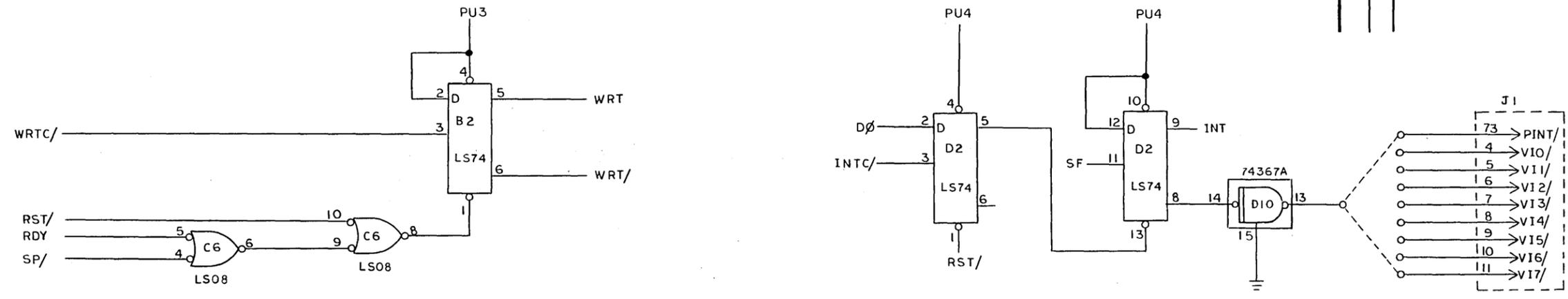
3

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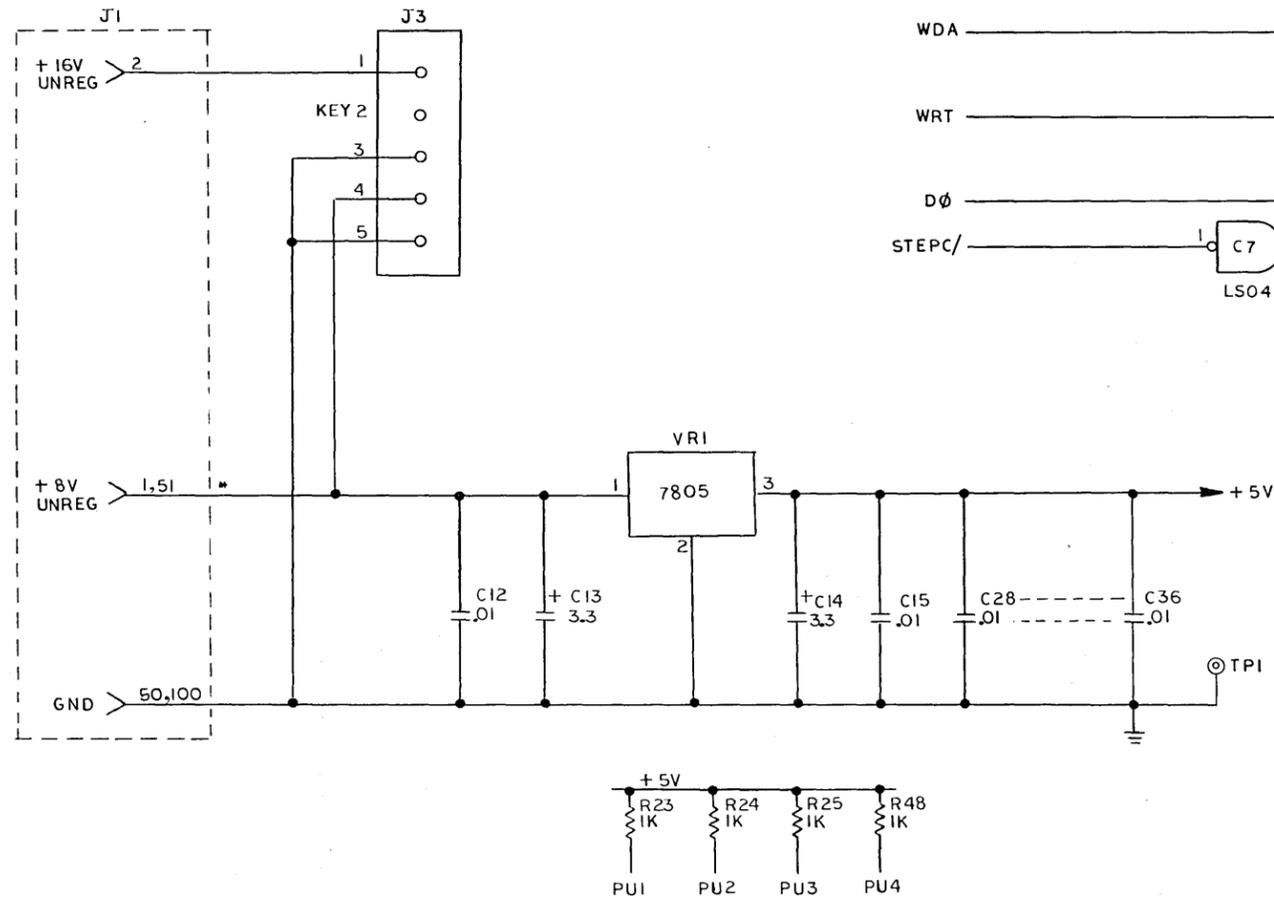
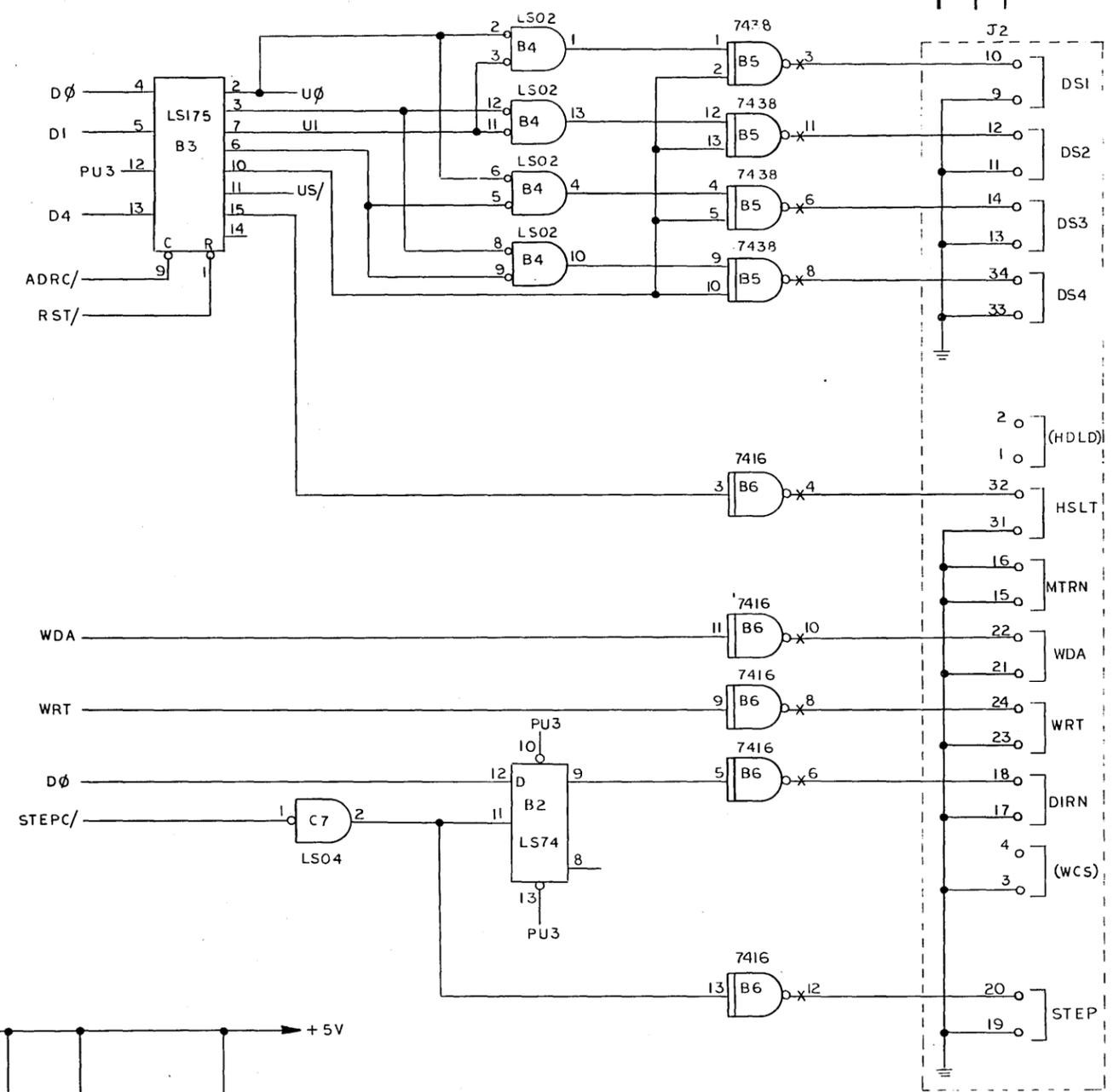
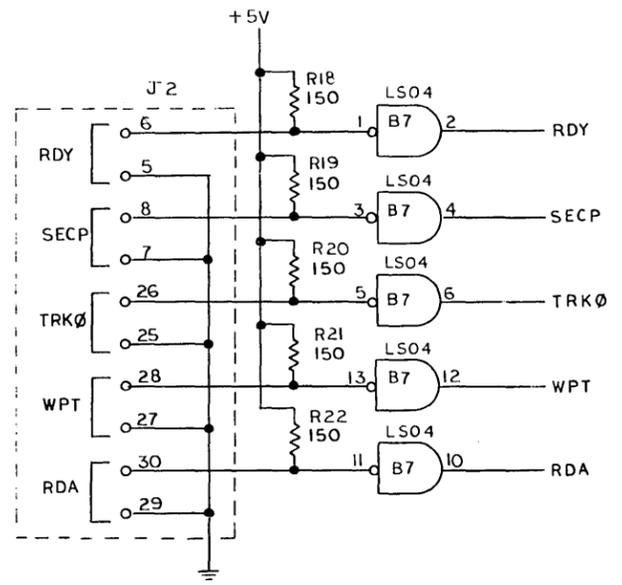


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FINISH		CHK BY		
NEXT ASSY		USED ON		APPROVED BY
APPLICATION		DO NOT SCALE DRAWING		F.D. CONTROLLER B
				SIZE CODE IDENT NO. DWG NO.
				D           100087
				SCALE SHEET 7 OF 9

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NEXT ASSY			APPROVED BY	
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