J. A. O'Brien

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: THE WWI AUXILIARY MAGNETIC DRUM SYSTEM

To: 6889 Engineers

From: J. W. Forgie

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Abstract: The auxiliary magnetic drum soon to be incorporated into the WWI input-output system will add approximately 25,000 registers of moderately high speed storage to the computer. The drum is a modified version of a standard model manufactured by Engineering Research Associates, Inc. The storage principle used in the drum system is akin to that used in the magnetic tape equipment already in use in the computer, but the actual mechanical and logical operations of the two storage systems are distinctly different. The auxiliary magnetic drum will communicate with the computer proper through the input-output element. Consequently, transfer of information from the drum to electrostatic storage is accomplished by the use of the input-output orders. Efficient operation of the drum system requires the use of the block transfer orders, bo and bi. A description of the operation of these orders illustrates the timing problems encountered in using the auxiliary drum with WWI.

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1.0 INTRODUCTION

This report is intended to deal specifically and in detail with the logical operation of the auxiliary magnetic drum soon to be installed in the WWI input-output system. Since the report precedes the installation and operation of the drum, it represents design thinking rather than operating experience. It is possible that phenomena presently unknown may force changes in the logical design, but on the whole, this report describes a system which is considered a final rather than a temporary or experimental design.

This report, in conjunction with E-466, "Operation of the In-Out Element", and E-499, "Operation of the Block Transfer Orders", is intended to give a complete description of the auxiliary magnetic drum and its operation in the input-output system. Since this report is the more detailed and specific, it is assumed that the reader has read and is familiar with the basic philosophy and operation of the in-out element as set forth in E-466 and E-499. This report will make many references to the above-mentioned reports, and the reader will probably find it convenient to have copies of them available, particularly since this report makes use of drawings attached to the others.

An attempt has been made in this report to explain a little of the physical as well as the logical operation of the auxiliary magnetic drum. In addition, the programming requirements for use of the drum have been discussed in some detail. Readers interested in these aspects of the drum should refer to sections 2.0 and 3.0. For those who want or need a pulse-by-pulse description of activities in the drum system, sections 4.0 and 5.0 are provided. Section 4.0 considers the drum system in block diagram sections and by logical function. Section 5.0 follows the action of the in-out orders in relation to the drum system and places emphasis on the timing aspects of the operation.

2.0 GENERAL DESCRIPTION OF THE AUXILIARY DRUM SYSTEM

2.1 The Function of the Auxiliary Drum as a Computer Element

It has long been apparent that the present capacity or even the projected final capacity of electrostatic storage was inadequate for many of the complex problems confronting the computing field today. Magnetic tape and drums are storage media which can be used to achieve relatively large storage capacity at moderate cost. Magnetic tape offers essentially unlimited storage capacity, but this advantage is obtained at the cost of a relatively long access time. The magnetic drum offers a relatively large capacity compared to electrostatic storage and an access time much shorter than magnetic tape. Access to a random register on a magnetic drum is generally much slower than access to a register of electrostatic storage, but if a block of registers can be handled in sequence, the average access time per register will be comparable. The capacity of the drum is obviously limited in comparison to magnetic tape, but is still large enough to afford a considerable improvement over electrostatic storage.

The auxiliary storage drum to be used with WWI will have a capacity of 24,576 sixteen-digit registers. These are divided into 12 groups of 2048 registers each. The random access time to any register is at most 29 milliseconds and to the registers of any one group at most 17 milliseconds. The difference in the above-mentioned access times results when it is necessary to change the group of registers to which access is to be made. When this change is required approximately 12 milliseconds of additional time must be allowed for the group selection relays to operate.

The auxiliary drum will be connected to the computer through the input-output system, and information will be transferred between the computer and the drum in the same fashion as between the computer and magnetic or paper tape units. The drum will be selected by si orders, and rc, rd, bo and bi orders will transfer the information. Differences between the auxiliary drum and magnetic or paper tape units arise principally from the much greater speed capabilities of the drum. The drum handles information in 16-digit words rather than 2 or 6-digit lines as in the case of the two types of tape units. Once the first register of a block of information has been located, the remainder of the block can be transferred at a rate very nearly as great as the maximum speed of electrostatic storage.

In contrast to electrostatic storage, magnetic drum storage is non-volatile. Consequently, information can remain indefinitely on the drum, unless accidentally erased. If it is desired to use a portion of the drum storage capacity for permanently recorded information such as a conversion program or much used sub-routines, the recording circuits to one or more groups of heads could be disconnected after making the desired recordings, so that it would be impossible to erase the information stored in those groups.

2.2 Physical Description of the Auxiliary Drum

The auxiliary drum itself is an aluminum cylinder 8 1/2 inches in diameter. The outside of the cylinder is coated with a thin layer of red iron oxide similar to the coating on ordinary magnetic recording tape. The cylinder is housed in a two-piece aluminum casting which also holds the read-record heads. The casting is made of the same material as the drum so that the gap between the heads and the drum surface will remain as nearly constant as possible with changes in temperature. The heads are mounted in small threaded cylinders which fit into holes in the housing. Since there are a great many heads on the drum, they must be staggered around the circumference of the cylinder. As a result, the outside of the drum housing, with the exception of the base and the seam between the sections, is almost completely covered with head assemblies. The drum cylinder is rotated by a 2-pole induction motor at a speed slightly less than 3600 rpm. This motor is mounted directly at one end of the drum housing.

Each read-record head scans a track around the circumference of the drum. On the auxiliary drum there is only one head per track, although two or more heads may be used in general. Tracks may be put on the drum at a density of 16 tracks per axial inch. The auxiliary drum itself is a standard 208-track drum built by Engineering Research Associates, Inc., but in use with WWI only 196 tracks will be utilized. There are 12 groups of 16 tracks each for information plus 2 tracks for timing and synchronization purposes. On the timing track are permanently recorded 2048 equally spaced pulses. Each of these pulses serves to mark the angular position of 12 storage registers (one register in each of the 12 groups). The relative angular position of the drum is indicated by an 11-digit flip-flop counter which counts the timing pulses as they pass the head on the timing track. In order for this angular position counter to indicate the correct absolute angular position of the drum, a single, permanently-recorded pulse on the other synchronizing track is used to initially clear the angular position counter. The synchronizing pulse occurs once each revolution of the drum. If the end-carry from the angular position counter does not immediately precede the synchronizing pulse an alarm will be given. In this fashion, angular positions on the drum are uniquely related to numerical quantities (the contents of the angular position counter) which can in turn be related to drum storage address registers.

Since there are 2048 angular positions of the drum identified by timing pulses, and since the drum rotates at a speed slightly less than 3600 rpm, one identifiable angular position comes under the read-record heads approximately every 8 μseconds. Since reading and writing operations in electrostatic storage require considerably more than 8 μseconds, it is convenient to number the drum address registers so that consecutively numbered registers will be spaced around the drum. In the case of the auxiliary drum, consecutively numbered registers are spaced 8 angular positions apart so that approximately 64 μseconds can elapse between the arrival of consecutively numbered registers. Thus, going from register 0 around the drum, consecutive angular positions are numbered 0, 256, 512, 768, 1024, 1280, 1536, 1792, 1, 257, etc. This artifice permits the bi and bo orders to transfer information between the drum and electrostatic storage at very nearly the maximum possible speed. Without the artifice, it would be necessary to wait one entire drum revolution time of 17 milliseconds between words in the block. A block transfer of 1000 words would then require 17 seconds as opposed to 64 milliseconds using the interlacing scheme.

Recording on the drum is accomplished by magnetizing spots on the drum surface. The entire surface is initially brought to zero magnetization by applying a rapidly alternating signal to all the recording heads. Zeros are then recorded in all registers on the drum. A zero is recorded by magnetizing a spot on the drum to saturation in one polarity. An all-zeros recording results in a pattern of alternating magnetized and un-magnetized spots in each track around the drum. When the drum has been prepared in the above fashion, it is ready for

use. In normal operation, ones are recorded by magnetizing spots in the opposite polarity to that used in recording zeros. As a result, the waveform produced by the reading heads as the drum rotates is a series of half-sine-wave pulses. The polarity of the pulse at a given instant indicates whether a one or a zero has been stored at the corresponding spot on the drum. The heads which do the recording have ferrite cores to allow for the high pulse frequencies handled. Since the heads cannot be permitted to contact the drum surface because wear would be excessive, the heads must have relatively wide gaps and large leakage fluxes. In fact, a silver shim is introduced into the air gap to increase the leakage flux. Eddy currents in the silver cause more of the flux to extend beyond the pole pieces and into the drum surface. Because increased spacing between the head and the drum surface results in loss of signal amplitude and resolution, the drum-to-head clearance is made as small as practicable in the face of the mechanical problems involved with the spinning drum. In the case of the auxiliary drum the clearance is approximately 0.002 inches.

All 12 groups of heads use the same recording and reading circuits. Relays connect the recording circuits to the desired group of heads, and consequently the in-out control must count a delay to allow the relays to actuate whenever the selected group is changed. The reading circuits are connected to the heads through crystal gates and therefore switch quite rapidly when the selected group is changed, but since the relays are always switched even though no recording is desired, the delay is always counted by in-out control and no use is made of the fast selection capabilities of the reading gate circuits.

3.0 PROGRAMMING REQUIREMENTS FOR THE AUXILIARY DRUM

3.1 Storage Addresses on the Drum

The 24,576 registers of the drum are divided into 12 groups of 2048 each. The group in which reading or recording is to take place is selected by means of relays, and changing groups is consequently a slow process. Selection of a given register within a group is made electronically and is therefore fast. Group selection is controlled by a 4 flip-flop register called the "group selector register" (GSR). This register is connected to digits 1-4 of the bus. The group selector register is read into from digits 1-4 of the accumulator when an si (auxiliary-drum-change-group) is ordered. The selection of a register within any group is determined by the storage address register (SAR). The SAR is read into from digits 5-15 of the accumulator when an si (auxiliary-drum-change-position) is ordered. The SAR is an 11-digit counter which is advanced one for each word read or recorded. If the count exceeds 2047, an end-carry is not produced, and the counter merely starts over again at zero. In other words, the addresses of the 24,576 registers on the drum are numbered consecutively from 0 through 24,575, but the automatic index of SAR does not carry over from one group of

registers to the next. It is necessary to specifically order an si (change-group) to pass from one group to the next. It is also important to note that if the reading or recording of a word with a drum address greater than 24,576 is ordered, all groups on the drum will be unselected and the reading or recording of the word will not take place. If a recording is ordered, the computer will continue, and no indication will be given that the recording did not take place. If a read is ordered, the computer will continue, and the word read will be all zeros.

3.2 Recording on the Drum

The auxiliary drum is prepared for recording by giving the appropriate si order. The actual recording is accomplished by an rc order in case a single word is to be recorded or by a bo in case a block of words is to be recorded. In either case, the si orders are the same.

There are 4 si orders which prepare the auxiliary drum for recording. These orders (with octal addresses) are as follows:

(1) si 704 - Auxiliary Drum Record. This order activates the recording circuits of the drum, but has no effect on the storage address register (SAR) or group selector register (GSR). An rc or bo order following an si 704 will result in a recording being made in the register whose group and position are left over from some previous drum operation.

(2) si 705 - Auxiliary Drum Record and Change Position. This order activates the recording circuits, and at the same time reads the contents of digits 5 through 15 of the accumulator into the SAR so that an rc or bo will cause a recording to start at the address specified by the right 11 digits of AC. GSR is left unchanged with the result that the recording takes place in the group used by the last drum operation.

(3) si 706 - Auxiliary Drum Record and Change Group. This order activates the recording circuits, and at the same time reads the contents of digits 1 through 4 of the accumulator into GSR so that a following rc or bo order will cause a recording to be made in the group specified by digits 1 through 4 of AC. The position (SAR content) remains unchanged.

(4) si 707 - Auxiliary Drum Record and Change Group and Position. This order is a combination of si 705 and si 706 and results in the complete resetting of the drum address according to the contents of digits 1 through 15 of AC.

It should be noted that if the starting address of a recording (or reading) operation is to be any other than that left over from a previous operation, the new address must be in the accumulator when the si order is given.

Once the si (record, etc.) order has set up the desired initial storage address, the actual recording is done by an rc or a bo order. The rc order will wait until the drum has rotated to the position corresponding to the contents of SAR and will then record one word on the drum. After the recording is accomplished, the contents of SAR are increased by one so that a following rc will record at the next consecutively numbered address. The rc order transfers the contents of the accumulator to the in-out register (IOR) and from there to the drum when the correct angular position has been found. During the hunting time the computer may continue with a program containing any but in-out orders.

The rc order is intended primarily for use when it is desired to record only one or perhaps two words at a time. While up to 17 milliseconds may be required to find a given drum address, the next consecutively numbered address will be available in 64 μseconds. Since somewhat more than 64 μseconds are required to do a ca plus another rc, it is possible to record in at most a few consecutively numbered registers before the computer falls behind the drum and a full drum revolution must elapse between recordings. It can be seen, therefore, that a block of information cannot be efficiently recorded using rc orders. The rc order can be most efficiently used when a relatively large amount of calculation can conveniently occur between rc orders. In this case a single si order can precede the calculation, and each result can be transferred to the drum by merely giving an rc order.

When it is desired to record a block of information, the bo x order should be used. The bo x order takes a block of information beginning at register x of electrostatic storage and records it on the drum beginning at the drum register set up by the si order which preceded the bo x. The number of words in the block is determined by the magnitude (times 2^{15}) of the number in the accumulator at the time the bo order is given. The normal maximum block length is 2048 words. If a block of more than 2048 words is ordered, the drum will continue to record on top of the information previously recorded. Likewise if a block containing a larger number of words than the number of registers in electrostatic storage is ordered, the recording will start over with register zero and continue cycling through electrostatic and test storage until the required number of words is recorded. A block transfer of this magnitude is not a recommended mode of operation and is mentioned here merely to indicate what would happen if such an order were accidentally programmed. A zero length block transfer will cause no trouble with recording, but since some confusion results when reading, it is suggested that zero length block transfers be avoided generally.

It should be noted that at the close of the bo order the accumulator contains one more than the ES address of the last register

in the block. AR contains the address of the first word in the block. The time required for recording orders is as follows:

si 704 - one timing cycle plus 15 μseconds for setting IOS.

si 705 - same as si 704.

si 706 - approximately 12 milliseconds to allow the group selection relays to set up. The computer does not wait unless another in-out order is given before the 12 milliseconds are over.

si 707 - same as si 706.

rc - one timing cycle plus up to 17 milliseconds required to find the correct drum angular position. The computer may continue with any but in-out orders.

bo - a hunting time of 0 to 17 milliseconds required to find the first drum address plus 64 μseconds for each additional word in the block. The computer can do nothing else from the time the hunting starts until the block transfer is complete.

3.3 Reading from the Drum

Reading very nearly parallels recording as far as orders are concerned. Four si orders are available to set up the drum for reading. They are as follows:

(1) si 700 - Auxiliary Drum Read. The reading circuits are activated, but no change is made in the contents of GSR and SAR. A short (64 μseconds) delay is counted to allow transients to subside in the reading amplifiers. When the drum has rotated to the angular position corresponding to the contents of SAR, a word is read from the group selected by GSR into the in-out register (IOR). At this time the contents of SAR are increased by one so that the next operation will consider the next consecutively numbered register.

(2) si 701 - Auxiliary Drum Read and Change Position. Action is the same as that on the si 700 order except that the word is read into IOR from the angular position corresponding to digits 5-15 of the accumulator when the si 701 was given. At the end of the order SAR is left holding one more than the contents of the accumulator when the order was given.

(3) si 702 - Auxiliary Drum Read and Change Group. Action is the same as si 700 except that the word is read from the group corresponding to the contents of digits 1-4 of the accumulator when the order was given.

(4) si 703 - Auxiliary Drum Read and Change Group and Position. This order is a combination of si 701 and si 702. The word is read from the group and position corresponding to digits 1-15 of the accumulator.

It must be stressed at this point that the above si (read) orders must always be followed by an rd or a bi order. The rd or bi order will make certain that the in-out system waits for the word that the si (read) order has requested. If an si (read) order is followed by any other si order without an intervening rd or bi, serious confusion can result in the in-out system.

As might be expected from the differences in si (record) and si (read) orders, the rd order does not behave in a fashion analogous to the rc order. The rd order merely waits until the si (read) order has completed its activity and then transfers, from IOR to the accumulator, the word obtained from the drum by the si (read). The rd order does not request another word from the drum. If a second rd order should be given, it will be unable to proceed, and the computer will hang up. If it is desired to read another word, a second si (read) order must be given after the first rd. In order to read a group of words with rd orders, it is necessary to give a new si (read) order for each word read.

If a block of information is desired from the drum, a bi x order should be given following an si (read). The bi x order will take a block of information from the drum, starting with the drum address determined by the si (read) order, and store it in electrostatic storage starting at register x. The number of words in the block is determined in the same fashion as for the bo order, and the same situation will result if too large a block is ordered. Since the first word of the block is obtained by the si (read) order, one word will always have been read from the drum even though a zero length block is ordered. If a zero length block read is ordered, this word will not be read into the accumulator, but will remain in IOR. The computer will consider the transfer to be complete and go on with the program. The drum SAR, however, will be left holding one more than the address ordered by the si (read). In other words, as far as the computer is concerned, no reading has taken place, but the drum thinks one word has been read. With the auxiliary drum this situation causes no basic difficulty so long as the program does not assume the wrong contents to be in SAR, but since with the buffer drum, the word read to IOR but not to the accumulator will be permanently lost, it is recommended that bi transfers of zero length be avoided in general.

For normal operation the bi order must follow an si (read) order since the si (read) is necessary to obtain the first word from the drum. However, it is possible for a bi to follow another bi without an intervening si (read). In this case, the first word read is always +0. The second word of the block as it appears in ES will be the first word actually read from the drum. This word will be the contents of the drum register corresponding to the contents of SAR left over from the previous bi order. As far as the drum is concerned, the transfer will start where the previous transfer stopped but will extend for one word less than a normal transfer of the same nominal length (same contents of AC when order was given). The bi order can be used in this fashion only following another bi. A bi following an rd will cause the computer to hang up while an rd following a bi will merely clear the accumulator.

The times required for reading orders are as follows:

si 700 - one timing cycle plus a counted delay of approximately 64 μseconds to allow transients to subside in the reading amplifiers before the drum is asked for a word. A hunting time of 0 to 17 milliseconds must occur before the correct word is found and transferred to IOR. During this time the computer goes on with the program unless an rd or bi order is given. In that case the computer stops and waits until the word has been located on the drum.

si 701 - same as si 700.

si 702 - same as si 700 except that an additional 12 millisecond delay is counted before the hunting begins to allow the group selection relays to actuate.

si 703 - same as si 702.

rd - one timing pulse cycle. The read order must wait for the preceding si (read) to find the desired word.

bi - if the si (read) order has found the first word, it is transferred from IOR to ES immediately. A 0 to 17 millisecond hunting time must elapse before the second word is found. After that time a new word is read every 64 μseconds. The computer can do nothing else during the time occupied by the bi order.

4.0 LOGICAL OPERATION OF THE AUXILIARY DRUM SYSTEM

In the following section constant reference will be made to portions of the auxiliary drum system by name, abbreviation, and/or system number, i.e. - 1034, group selector register (GSR). Unless noted otherwise, these references will be to drawing E-37318, a reduction of which is attached to this report.

4.1 Timing Control in the Auxiliary Drum System

The origin of all timing pulses on the auxiliary drum is the timing track on the drum itself. During the manufacture of the drum, 2048 equally spaced pulses were recorded on this track. These pulses are fed into the timing control (1020), which supplies timing pulses to the remainder of the drum system and checks to make sure that the contents of the angular position counter (1033) bear the proper relationship to the actual angular position of the drum.

To understand the operation of the timing control, assume that it is operating normally. In this case the gas tube is off and the inverter keeps GT02 on so that timing pulses are supplied to the remainder of the system. FF01 holds a zero with the result that GT01 is off, and timing pulses are not supplied to the gas tube. The timing pulses from GT02 are added to the angular position counter, and after 2048 of them have been added, an end-carry appears. This end-carry will complement FF01 and turn on GT01. In normal operation the end-carry will be followed in about 4 μseconds by a pulse from the mark track. This mark pulse will recomplement FF01 and turn off GT01 before the next timing pulse occurs. (The timing pulses are separated by approximately 8 μseconds.) The gas tube thus never receives a firing pulse unless the mark pulse fails to follow the end-carry before the next timing pulse can occur. Since there is only one mark pulse recorded in the mark track, the angular position counter must always start over at the same angular position of the drum.

If the mark pulse and the angular position counter end-carry fail to bear the proper time relationship to each other, a timing pulse will pass through GT01 and fire the gas tube. This situation will occur if there is any failure in the angular position counter or associated circuits. When the gas tube fires, the timing pulses will be cut off from the drum system, and an alarm light will indicate that trouble has occurred. This alarm need not stop the computer, because without timing pulses no drum operations can be performed. The computer will hang up if an attempt is made to use the drum when the timing control alarm has indicated trouble.

Once the gas tube has fired, operation can be resumed only by pushing the reset alarm pushbutton. This button turns off the gas tube and holds it off. Timing pulses then go out to the remainder of the drum system and start counting into the angular position counter.

The button also holds FF01 in the clear position so that the timing pulses cannot fire the gas tube. Finally, the reset alarm button allows the mark pulse to clear the angular position counter so that the count will start correctly. As long as the button is held depressed, timing pulses will continue to be supplied, and the angular position counter will be cleared once each drum revolution by the mark pulse. If the reset alarm button is now released, there is a good chance that normal operation will be resumed. The chances are about 5000 to 1. The possibility that normal operation will not be resumed arises from the chance that the button will be released in the 4 μsecond period between the arrivals of the end-carry pulse and the mark pulse. If the button is still depressed when the end-carry pulse arrives, but is released before the mark pulse appears, FF01 will be left holding a one, and the gas tube will fire on the next timing pulse. Since the period in which the button can be safely released is approximately 5000 times as long as the 4 μsecond danger period, there is reason to believe that no serious trouble will be caused by this behavior, although it may occasionally be necessary to push the button more than once before normal operation is restored.

4.2 Address Selection in the Auxiliary Drum System

The 24,576 storage address registers of the drum are divided into twelve groups of 2048. Each group has 16 read-write heads, one for each digit in the register. The 2048 registers in each group are distributed around the circumference of the drum. The twelve groups are arranged axially along the drum. The selection of a given storage address is actually a selection of a given region of drum surface, but since the drum is rotating, it is necessary to make a selection in both time and space. Group selection is logically a spacial selection, while address selection within the group is a time selection. The group selection circuits tell the reading and writing circuits where to operate, and the address selection circuits tell them when to operate.

Group selection is accomplished by the group selector (1050), the group selector switch (1035), and the group selector register (1034). The group selector register receives a group number from the accumulator when an si (read-or-record-and-change-group) order is given and stores the number until the next such order. When one of these orders is given, line MD04 from IOS turns on GT05 and GT06 of GSR read in control so that a GSR CLEAR pulse on TP8 of the si order and a GSR READ IN on TP1 will set the four flip-flops of GSR to correspond to the contents of digits 1-4 of the accumulator. The flip-flops of GSR drive a crystal matrix called the group selector switch. This matrix is so connected that if GSR holds a number between and including zero and eleven, one of twelve output lines will be selected. If the number in GSR is greater than eleven, no output will be selected. The output lines run to the group selector. There each line controls a relay and a set of crystal gates. The relay connects the writing circuits to the read-write heads on the drum when the line is selected. The crystal gates connect the reading

circuits to the same heads. When a given group is selected, both reading and writing circuits are connected to the heads of that group. Reading can then be accomplished by merely sensing the output gate tubes of the reading circuits at the correct instant of time. Recording can likewise be accomplished by sending a pulse to the recording circuits at the right moment.

The correct instant of time at which reading or writing operations should take place depends upon the storage register to be considered. The storage address is read into the storage address register (SAR) from the accumulator on an si (read-or-record-and-change-position) in a fashion similar to that described above for the group number. The contents of SAR remain unchanged until another si (change-position) order is given, or until a reading or writing operation actually takes place. The pulse which performs the reading or writing operation is sent to SAR as an ADVANCE SAR pulse which adds one to the number in SAR so that the next drum operation will consider the next consecutively numbered storage address unless the address is changed by an intervening si (change-position). SAR is an eleven digit counter which counts from 0 through 2047. If the register holds all one's (2047) and an ADVANCE SAR pulse appears, an end-carry will not be produced, and the register will merely be left holding all zeros with the result that the next operation will consider register zero. For this reason it is necessary to change groups by means of an si (auxiliary-drum-change-group) if it is desired to record more than 2048 words on the drum.

The storage address register holds the address of a desired register on the drum, while the angular position counter (1033) holds a number representing the actual drum register available at any instant. It is necessary to relate the contents of these two registers in some fashion and to generate a pulse at the instant when the rotating drum has placed the desired register under the read-record heads. The coincidence detector (1032) accomplishes the latter function. As can be seen from the diagram, the "one" side of each flip-flop in SAR supplies one of the two inputs to a GT02 in the coincidence detector. This same gate tube receives its second input from the "zero" side of a flip-flop in the angular position counter. The other sides of the same two flip-flops supply the inputs to a GT01 in the coincidence detector. The outputs of GT01 and GT02 are added together with the result that a signal appears at the summing point unless both flip-flops hold the same information. The summed outputs from GT's 01 and 02 on each of the 11 digits of the coincidence detector are again added together and fed into an inverter which in turn feeds GT03. There is no output from the inverter unless all 11 digits of SAR agree with the 11 digits of the angular position counter. When agreement occurs, a timing pulse passes through GT03 to become a COINCIDENCE pulse. This pulse causes a reading or writing operation to take place if the computer has ordered one but otherwise does nothing. The appearance of the COINCIDENCE pulse indicates the fact that the space on the drum surface corresponding to the contents of SAR is just passing under the read-record heads. Since the contents

of SAR are uniquely related to the contents of the angular position counter (APC), and the contents of APC are uniquely related to drum angular position, the COINCIDENCE pulse uniquely identifies the instant of time at which the drum angular position corresponding to the contents of SAR is available to the reading and writing circuits.

It was stated in section 2.2 of this report that consecutively numbered address registers should be spaced 8 angular positions apart so that there would be time for electrostatic storage operation between the arrival of consecutively numbered drum registers. In terms of the drum system, this condition requires that, if SAR is advanced one at the appearance of a COINCIDENCE pulse, coincidence shall not occur again until the angular position counter has counted 8 timing pulses. A moment's reflection will show, however, that merely counting 8 timing pulses to each coincidence pulse will not achieve exactly the desired result. If, for instance, we start with coincidence at the angular position corresponding to register zero, and count 8 timing pulses 256 times, we will have counted 2048 pulses and will be back at the angular position at which we started. Register 256 would therefore correspond exactly to register 0 and we would be treating all storage address registers modulo 256. We would therefore be able to use only 256 of our 2048 angular positions. However, if when we have counted 8 timing pulses 255 times, we count 9 pulses the next time, we will end up with register 256 just one angular position beyond register 0. If we now go back to counting 8 pulses for each coincidence until we get to register 511, and then count 9 pulses again, we will end up with register 512 lying two angular positions beyond register 0. We continue this process until we get to register 2047. Register 2047 will be seven angular positions beyond register 255 and one angular position before register 0. We therefore now require a count of only one timing pulse to reach coincidence with register zero. With this scheme we will be able to identify and use all 2048 angular positions on the drum.

The scheme described above can be easily and rather elegantly realized by causing the timing pulses to add into the angular position counter at the third digit from the left rather than at the right end. Essentially the 11 digit angular position counter is broken into two counters. The right 8 digits count the 256 registers which can reach coincidence each drum revolution. The left 3 digits count the drum revolutions modulo 8 and also the 8, 9, or 1 timing pulses which must separate consecutively numbered registers. In order to see exactly how these counters operate it is necessary to consider three illustrative examples.

First, assume that at some instant of time APC and SAR both contain all zeros. Further assume that the storage control is prepared for reading or recording, so that each time a timing pulse becomes a coincidence pulse, it will add one to the contents of SAR. For convenience, let us renumber the flip-flops of APC and SAR so that they start with FF1 on the right end and go through FF11 on the left end. The

timing pulses are therefore added into FF9 (or digit 9) of APC. Now since all flip-flops of APC and SAR contain zeros, the next timing pulse to appear will become a coincidence pulse and add to SAR. At the same time this pulse puts a one in digit 9 of APC. We thus are left with the following:

APC	001	00000000
SAR	000	00000001

Six time pulses later the situation will be:

APC	111	00000000
SAR	000	00000001

The next time pulse will produce a carry from digit 11 of APC into digit 1 of APC so that we will have

APC	000	00000001
SAR	000	00000001

Now the next time pulse (the eighth) will become a coincidence pulse and the drum will have rotated 8 angular positions in going from register 0 to register 1. If we allow this process to continue, we will get a coincidence pulse for every eight time pulses until we reach the coincidence pulse for register 255. Let us assume that we have received the time pulse immediately preceding the coincidence pulse for register 255, i.e., we have

APC	000	11111111
SAR	000	11111111

The next pulse is a coincidence pulse, and it leaves us with

APC	001	11111111
SAR	001	00000000

Six pulses later we have

APC	111	11111111
SAR	001	00000000

The seventh pulse results in

APC	000	00000000
SAR	001	00000000

and the eighth pulse does not now produce a coincidence pulse but leaves us with

APC	001	00000000
SAR	001	00000000

so that the ninth pulse gives us coincidence. We have thus located register 256 one angular position beyond register 0. At this point the situation reverts to a coincidence pulse for every eight timing pulses until register 511 is reached, at which time another count of nine occurs, etc.

Let us now continue on until we are just ready to achieve coincidence with register 2047, i.e., we have

APC	111	11111111
SAR	111	11111111.

The next pulse now shows coincidence with register 2047 and leaves us with

APC	000	00000000
SAR	000	00000000

so that coincidence is again achieved on the next time pulse, and we have returned to register 0.

It should be noted that since the drum storage control requires at least one timing pulse between coincidence pulses, it is impossible to read or record in register 0 immediately after reading or recording in register 2047. One complete drum revolution must take place before an operation can take place in register 0. For this reason a block transfer which crosses over from register 2047 to register 0 requires an extra 17 milliseconds for completion.

4.3 Reading and Recording Operations in the Auxiliary Drum System

The auxiliary drum storage control (1040) accepts pulses from the computer ordering the reading or recording of a word on the drum and causes the required action to take place at the correct instant of time. Since as far as the drum system is concerned information is always handled on a single word basis, the storage control requires a pulse from the computer for each word read or recorded. The word may be part of a block transfer (bi or bo order), but the action of the drum system is the same as that for a single word transfer (rd or rc order). Accordingly, the following discussions consider the recording and reading operations that take place within the drum system rather than recording and reading orders in the computer. In section 5.0 of this report the actions of the drum system which take place on si, bo, bi, rc, and rd orders are discussed from the point of view of computer timing.

4.31 Recording Operations

Recording operations take place on bo and rc orders. In either case an si (auxiliary-drum-record, etc.) order must have preceded the bo or rc. The si order will have energized line MD02 from the in-out switch (IOS) to auxiliary drum storage control (ADSC). The drum storage address will have been set either by the si order or will be left over from some earlier drum operation. During the rc or bo order, an INITIATE RECORD pulse is sent from the control matrix (rc) or IOC (bo) to ADSC. This pulse sets FF's 01 and 03 of ADSC. FF01 has previously been clear since it was cleared at the completion of the last drum operation. The setting of FF01 allows drum timing pulses to pass through GT01 to set FF02 which in turn opens GT02. The two flip-flops (01 and 02) and their associated gate tubes form a synchronizer which permits the first COINCIDENCE pulse following the INITIATE RECORD pulse and at least one timing pulse to pass on to accomplish a reading or recording operation. It is necessary to use the two flip-flops to insure that a good pulse leaves GT02 when coincidence is reached. If, for instance, the INITIATE RECORD pulse had been used to set FF02, and since the time of arrival of the COINCIDENCE pulse is completely independent of that of the INITIATE RECORD pulse, it would be possible for the COINCIDENCE pulse to be just sensing GT02 at the moment when FF02 was turning it on. A misshapen output pulse could then appear which would perform some but not all of the functions assigned to it. The use of two flip-flops to accomplish synchronization overcomes this difficulty. If the first TIMING pulse passing through GT01 is misshapen it either will or will not set FF02. If it does, the situation is normal, if it does not, the next pulse will, and the situation will again be normal.

It should be noted that if a COINCIDENCE pulse is the first pulse to appear after the INITIATE RECORD pulse, it will not pass GT02 because FF02 requires 2 μseconds or so to turn on GT02. Therefore at least one timing pulse must appear between the INITIATE RECORD pulse and the first COINCIDENCE pulse if it is to pass GT02. As a result of this action the INITIATE RECORD (or READ) pulse must precede a given COINCIDENCE pulse by at least 10 μseconds, if that pulse is to actuate the recording circuits without waiting a drum revolution time of 17 milliseconds.

The output pulse from GT02 passes through GT04 since the INITIATE RECORD pulse has set FF03. The output pulse from GT04

(1) triggers the writing circuits which record the contents of IOR in the desired drum register,

(2) clears FF's 01 and 02 of ADSC so that no further operations will take place until another pulse comes from the computer,

(3) advances SAR so that the next operation will take place in the next consecutively numbered register, and

(4) returns to IOC as an ASYNCHRONOUS INITIATION #2 pulse to announce that the recording has taken place.

At this point the drum system has indicated to the computer that the recording operation is complete, but another 2 μseconds must elapse before the writing circuits have actually performed the recording. The RECORD pulse from GT04 of ADSC sets FF01 of the writing circuits and after being delayed 2.0 μseconds clears the same flip-flop. The effect of this action is to produce a 2.0 μsecond pulse which is fed to the gate tubes connected to the digit columns of IOR. Gate tubes are connected to both sides of the IOR flip-flops because it is necessary to write both zeros and ones on the drum. Not writing a one is not equivalent to writing a zero. The gate tubes on the digit columns of IOR are connected to center-tapped transformers which drive the heads. A one in a digit of IOR causes current to flow in one direction in the head while a zero causes current to flow in the opposite direction. In the absence of the 2.0 μsecond record pulse initiated by ADSC, no current at all flows in the heads.

4.32 Reading Operations

Reading operations take place on si and bi orders. It should particularly be noticed that reading operations do not take place on the rd order. The rd order merely transfers from IOR to AC a word obtained from the drum on an si order. An si (auxiliary-drum-read, etc.) will set the address and group selector registers if requested and will read one word from the drum. A 64 μsecond delay is also counted before the word is requested from the drum to allow transients to die out in the reading amplifiers. Transients will exist only when a recording operation has immediately preceded a reading operation, and while this situation is likely to occur only occasionally, it is necessary to count the delay on every si (auxiliary-drum-read) order. At the end of the delay period (64 μseconds normally, 12 milliseconds if the group selector is changed), a CYCLE pulse is sent from IOC to ADSC. The si (read) order has energized line MD01 from IOS, and GT05 of ADSC input control is consequently on. The CYCLE pulse then passes through to set FF01 and clear FF03 of ADSC. The setting of FF01 results in the same synchronizer action that was discussed in section 4.31 for the INITIATE RECORD pulse. FF03 is cleared so that when a COINCIDENCE pulse passes GT03 it will become a READ pulse. When this pulse leaves GT03, it is delayed a nominal 3.0 μseconds before being sent to clear the synchronizer flip-flops 01 and 02 and to advance SAR. The same pulse is delayed another 4.0 μseconds and used to sense 16 gate tubes at the outputs of the reading circuits. These gate tubes then send pulses to IOR if their respective channels contained ones at the instant the drum passed under the heads. The nominal delay of 7.0 μseconds which the READ pulse experiences is introduced to allow for the delays which the drum signals encounter in passing through the reading amplifiers. The exact amount of this delay will have to be determined experimentally when the drum equipment is finally set up. It is necessary to adjust the READ pulse delay so that it senses just the right portion of the waveform generated at the output of the reading amplifiers. The READ pulse is also sent back to IOC as an ASYNCHRONOUS INITIATION pulse to announce that the reading has been completed.

On the bi order the action is exactly the same except that an INITIATE READ pulse comes from IOC for every reading operation.

5.0 ACTION OF THE IN-OUT ORDERS IN RELATION TO THE AUXILIARY DRUM SYSTEM

In this section reference will be made to the block diagram of in-out control (IOC). A copy of this drawing (SD-37367-1) is attached to E-499, Operation of the Block Transfer Orders. The reader is referred to that report for a detailed discussion of the block transfer orders. The orders described there and in this report differ somewhat from those described in E-466, Operation of the In-Out Element. This report assumes that the reader is acquainted with both E-466 and E-499. In general, only those aspects of the in-out orders which apply specifically to the auxiliary drum are discussed here.

5.1 The si (Auxiliary-Drum-Record, etc.) Orders

There are four si orders which prepare the auxiliary drum for recording. Until IOS is set up after TP7, the action on these orders is the same as that for all si orders. This action is explained in E-466. On TP8 a CLEAR pulse is sent out from the control matrix to the horizontal decoders and to the auxiliary drum system. This pulse always clears the horizontal decoders, and it must clear SAR and GSR in the drum system if the contents of these registers is to be changed. If the order was si 704 (auxiliary-drum-record), this clear pulse will do nothing because lines MD03 and MD04 from IOS to the drum read in control will be off. If the order was si 705 (record-and-change-position), line MD03 will be on, and SAR will be cleared. Similarly, if the order was si 706 (record-and-change-group), MD04 would be on and GSR would be cleared. In case the order was si 707 (record-and-change-group-and-position), both MD03 and MD04 would be on, and both SAR and GSR would be cleared.

On TP1 the contents of the accumulator are read to the bus. A READ IN pulse is simultaneously sent to the horizontal display decoders and to the drum system. As in the case of the CLEAR pulse on TP8, the appropriate digits on the bus will be read into SAR, GSR, both, or neither according to voltages on lines MD03 and MD04. It should be noted that the transfer between the accumulator and SAR or GSR is not checked. Checking in the usual fashion would be quite complex because the transfer is conditional and because the flip-flops of SAR and GSR are not as fast as those normally used in WWI.

If GSR is changed by the si order, it is necessary to count a delay. This delay is initiated by the IOC RESET pulse on TP1. If the si address was 706 or 707, lines MD04 and C05 will be on. MD04 goes to GT12 of IOC reset control, and when MD04 is on, the IOC RESET (si) pulse will be allowed to reset the delay counter for a delay sufficiently long to allow the group selection relays to operate. At present estimates this delay will be approximately 12 milliseconds long. Line C05 from IOS to IOC allows the IOC RESET (si) pulse to set the interlock and clear the alarm control so that another in-out order will wait until the delay has been counted. If GSR is not to be changed (si 704 or 705), no delay is counted, and a following in-out order can proceed immediately.

The four si orders just discussed, in common with all si orders which select recorders, turn on line C01 to the IOC interlock so that a following si order must sense the interlock before it can proceed to alter the contents of IOS.

The only action which the si (auxiliary-drum-record) orders perform to prepare the drum for recording is the energizing of line MD02 to the drum storage control. The mode flip-flop (FF03) of storage control is not set into the record position until an rc or a bo order appears.

5.2 The rc Order

Action on the rc order exactly follows that described in E-466. On TP1 the contents of the accumulator are read to IOR. On TP2 the IOC RESET pulse sets the interlock and clears the alarm control. Also on TP2 an INITIATE RECORD pulse is sent to the drum system. This pulse passes through GT06 of the drum storage control if an si (auxiliary-drum-record) order has preceded the rc order. The output of GT06 initiates one drum recording operation as explained in section 4.31 of this report. When the recording operation is completed, an ASYNCHRONOUS INITIATION pulse is sent to IOC from the drum storage control. This pulse becomes a SYNC COMPLETION pulse which sets the alarm control and either clears the interlock or starts the computer clock if necessary.

5.3 The bo x Order

As explained in E-466 and E-499, the bo x order takes a block of information from electrostatic storage and transfers it to some output device. The number of words in the block is assumed to be in the accumulator at the time the bo x order is given. The complement of the number of words is transferred to IODC on TP7 of the order, and one is added to the contents of that counter for each word transferred until an end-carry is produced as an indication that the block transfer is complete. The ES address from which each word of the block is obtained is indexed by adding one to the accumulator each time a word is transferred. The accumulator receives the initial address (the x in bo x) from the storage switch on TP8 and adds one to it on every TP3 thereafter until the transfer is complete. When the order gets to TP5, the time pulse distributor is cleared so that the next time pulse to appear is TP1. Time pulses 6, 7, and 8 occur only on the first cycle of the order and are used merely to get the cycling action started. Once each cycle the block control is sensed to determine whether another word is to be recorded or the order is to be terminated.

Let us now assume that we are interested only in a block transfer to the auxiliary drum. We can therefore ignore the possibility of an incomplete transfer which was mentioned in E-499 and which at present can only occur on a transfer to the buffer drum. Let us further assume that we have given the correct si order to prepare the drum for recording in the desired register and that we have placed either the positive or negative number of words ($x\ 2^{-15}$) in the accumulator. We now give a bo x order.

On time pulses 6, 7, and 8 operations take place which prepare for the transfers to occur later. The reader is referred to E-499 for a detailed description of these operations. To avoid needless repetition here, let us be content with a summary of the state of affairs which exists after TP8 has appeared. When TP8 has just passed, we have

(1) placed in AC and AR the storage address of the first word in the block,

(2) read the negative of the number of words in the block into IODC and added one to the contents of that register,

(3) read the contents of register x from the storage tubes into the program register if x was 32 or greater,

(4) stopped the computer clock for 2 μseconds to allow the pulse added to IODC to appear as an end-carry if a zero length block has been ordered, and

(5) performed certain other operations which are described in E-499 but are left out here because they are of secondary importance to the present discussion.

When the 2 μsecond delay has elapsed, the clock is started and TP1 appears. On this time pulse the contents of register x are read into IOR and the check register. At the same time the storage switch is cleared so that it may be set to a new register for the next cycle of the order. At this time a BLOCK CONTROL SENSE #2 pulse is sent from the control matrix to IOC. This pulse senses GT's 01 and 04 on the block control flip-flop. If this flip-flop holds a one, the sense pulse will pass through GT01 to terminate the order as described in section 3.55 of E-499. The block control flip-flop will hold a one at this time only if a zero-length block transfer was ordered. Let us assume that we have asked for a block of two or more words so that the block control holds a zero at this time. Under this condition, the SENSE #2 pulse passes through GT04 to become an INITIATE RECORD pulse which goes to the drum system to start a recording operation. The pulse from GT04 also becomes an IOC reset pulse which does nothing except set the interlock and clear the alarm. The in-out control has now requested that the word just placed in IOR be recorded on the drum and is prepared to wait for a pulse indicating that the operation is complete. The computer, meanwhile, is free to go on, but 1/2 μsecond after TP1 a SENSE INTERLOCK pulse is sent from the control matrix. Since there is no possibility that the drum recording operation is complete at this time, the interlock will always be set, and the SENSE pulse will always stop the computer clock. Now both the computer and the in-out control must wait until the drum has found the correct angular position and performed the recording operation.

The length of time that the computer must wait for the recording operation to be completed obviously depends on the angular position of the drum at the instant the INITIATE RECORD pulse arrives at the drum

system. As explained in section 4.31 of this report, a record operation cannot be performed within at least 10 μseconds after the arrival of the INITIATE RECORD pulse. This delay results from the synchronizer action of the auxiliary drum storage control. Any time after this 10 μsecond period, the appearance of a COINCIDENCE pulse in the drum system will result in the performance of the desired recording operation. On this first cycle of the bo order we have no knowledge concerning the drum's angular position, and therefore we must expect to have to wait up to 17 milliseconds to complete the recording operation. On succeeding cycles we do have information regarding the drum position and can predict approximately when the next drum register will be available. We must have completed all operations in the computer proper and IOC and have given another INITIATE RECORD pulse at least 10 μseconds before the next COINCIDENCE pulse arrives.

Let us now assume that the first COINCIDENCE pulse has appeared, the recording operation has been completed, and an ASYNC INITIATION #2 pulse has been sent back to IOC to announce the completion of the recording operation. This pulse enters synchronizer #2 in IOC. At most 6 μseconds later a synchronized pulse leaves the synchronizer and goes to IOCC which holds all ones so that the same pulse appears as a COMPLETION pulse and starts the computer clock. The COMPLETION pulse normally follows the ASYNC INITIATION pulse by only 2 μseconds, but since the low frequency supply pulses (LFSP) which feed the synchronizer are interrupted for restoration, it is possible that a delay of 6 μseconds can occur at this time, and we must be sure to consider the worst possible cases in examining the timing in the block transfer orders.

Let us now temporarily forget about restoration and consider what happens on the remainder of the bo cycle. One μsecond after the COMPLETION pulse has started the clock, TP2 appears. The only command pulse on this time pulse is a SENSE BLOCK CONTROL #3. This sense pulse is intended to discover whether an incomplete recording on the buffer drum has taken place. Since we are considering a block transfer to the auxiliary drum, this pulse does nothing. On TP3 (one μsecond later) the contents of IOR are read to the check register in preparation for a transfer check on TP3.5. At the same time an END-AROUND CARRY pulse adds one to the contents of the accumulator which will then be the storage address of the next word in the block of information being transferred.

If we assume that the transfer check on TP3.5 did not produce an alarm, TP4 will follow. On this time pulse the contents of the accumulator are read to the storage switch in preparation for the storage reading operation which may follow on TP5. In addition, IOR is cleared in preparation for the word it will receive on TP1 of the next cycle. At the same time an ADD ONE pulse is sent to IODC to indicate that one word of the block has been recorded.

On TP5 the time pulse distributor is cleared so that the next time pulse to appear will be #1. At the same time, if the storage switch holds an ES address (32 or greater), an ES read operation is initiated. The ES read operation stops the computer clock for 17 μseconds, so that TP1 appears 18 μseconds after TP5 if ES is used. When TP1 appears the bo cycle is complete.

If we now ignore restoration and compute the time which must elapse between the arrival of the ASYNC INITIATION pulse from the drum system and the appearance of the INITIATE RECORD pulse for the next drum operation we find the total to be 24 μseconds. Since normal restoration can occur every 16 μseconds, we might expect 2 restoration periods during the cycle, but normal restoration is prohibited during the ES read operation which lasts 17 μseconds, and consequently just one restoration period of 5 μseconds can occur during the cycle. Therefore the total cycle time is at most 28 μseconds. We have 64 - 10 or 54 μseconds allowed by the drum system to complete the cycle, and it is therefore apparent that timing is not critical. Unfortunately, the same cannot be said for the bi order which requires two ES operations per cycle. We have discussed the bo timing in such detail largely because it can be readily compared to the bi timing which is more complex and much more critical.

Let us now return to the second cycle of the bo x order. With the appearance of TP1 the block control is again sensed to determine whether another recording operation should be initiated. If we had asked for a one-word block, the ADD ONE to IODC pulse on TP4 of the first cycle would have produced an end-carry and the block control flip-flop would be set when the sense pulse appears on TP1. The order would then be terminated as described in E-499. If we had asked for more than one word, the block control flip-flop would be clear when sensed, and another recording operation would be initiated. In that case the cycle will repeat until an end-carry from IODC is finally produced.

5.4 The si (Auxiliary-Drum-Read, etc.) Orders

Until the IOC RESET pulse occurs on TP1, the si(Read) orders perform the same actions as the corresponding si (Record) orders discussed in section 5.1, i.e. - the contents of SAR and GSR are set in the same fashion. The order si 700 leaves both SAR and GSR unchanged. The order si 701 changes SAR while si 702 changes GSR, and si 703 changes both. The same lines (MD03 and MD04) from IOS are energized as required to permit the desired changes. However, when the IOC RESET pulse appears it finds the situation quite different. In the case of the record orders the reset pulse does nothing unless the group is to be changed. In the case of the read orders, however, it always finds GT's 02 and 10 of IOC reset control open because lines C05 and C04 are energized. GT02 allows the reset pulse to set the interlock and clear the alarm, and GT10 allows it to reset IOCC for a count of two. Line C04 also opens GT11 which allows the pulse to set and start IODC for a delay of approximately

64 μseconds. This delay allows transients in the reading amplifiers to subside. Lines C04 and C05 are energized for all si (Read) orders. If the group selector is to be changed, line MD04 will also be energized, and GT12 will permit the IOC RESET pulse to set and start the delay counter for the long (12-15 millisecond) delay required by the group selector relays. In this case the normal 64 μsecond delay is also set up at the same time, and the resultant delay is the sum of the long and short delays. It is not expected that any difficulty will result from requesting two different delays simultaneously. Since 64 μseconds is negligible compared to 12 milliseconds, nothing is lost by counting the sum of the two delays.

When the delay has been counted, the end-carry from IODC adds one to IOCC and becomes a CYCLE pulse. The CYCLE pulse goes to the auxiliary drum system and initiates a reading operation as explained in section 4.32 of this report. When the reading operation has been completed, an ASYNC INITIATION #2 pulse returns to IOC. This pulse, after being synchronized, becomes a COMPLETION pulse which clears the interlock and/or starts the clock.

Since line C01 from IOS to IOC is not energized for si (Read) orders, following si orders will not sense the interlock to determine whether the in-out system has completed its operations. For this reason it is always necessary to follow an si (Read) with either an rd or a bi. If the si (Read) is followed by another si, without an intervening rd or bi, the in-out control may be in the process of counting a delay or receiving information from an external unit, in which case the new si order can produce a situation of considerable confusion within the in-out system.

5.5 The rd Order

The rd order, when used with the auxiliary drum, merely transfers the contents of IOR to the accumulator. The IOC RESET pulse which appears on TP2 of the order prepares IOC for the receipt of another word but does not send a pulse to the drum requesting this word. Consequently no word appears and no ASYNC INITIATION pulse comes along to clear the interlock. If now another rd or bi order is given, the SENSE pulse on TP6 will find the interlock set and will therefore stop the clock to wait for the word which never comes. For this reason, an rd must be followed by another si before another word can be read.

The rd order does not request another word from the drum (or from any external unit) because there is no assurance that another word is desired. It does, however, prepare the in-out system for handling another word in case a free-running reader such as magnetic tape is being used. The free-running reader sends words to the in-out system when they are ready and does not need to be asked for another word each time.

5.6 The bi x Order

The purpose of the bi x order is to take a block of information from some external unit and store it in electrostatic storage beginning at register x. Basically, the bi x order operates in the same fashion as the bo x order. The ES registers are indexed in the same fashion, the words in the block are counted in a similar manner, and the decision of whether to read another word or terminate the order is determined by sensing the block control just as in the bo order. Differences arise from the fact that the first word of the block must be placed in IOR by an si (Read) order and from the necessity of doing two ES operations during each cycle. Logically it would be necessary to do only one ES operation, i.e. - an ES write operation, but since a selective writing process is used in WWI electrostatic storage, it is necessary to read the contents of a register before writing in that register.

On time pulses 6, 7, and 8 the action of the bi x order is essentially the same as that of the bo x order. There are two operations which occur in this part of the bi x order but do not occur on the bo x order. On TP6 of both orders, the contents of register x (if x is greater than 32) are read from the storage tubes into the program register. In the bo order, this word is the first word of the block to be recorded and will later be transferred to IOR and from there to the external unit. In the bi order, this word is needed only for the selective writing process and must therefore be removed from the program register and stored until the new word which is to be placed in register x has been obtained from IOR. Accordingly, the contents of the program register are read to the check register via the check bus on TP7. On TP1 the check register is complemented, and on TP2 the new word is read from IOR into the program register and the check register. As a result of this series of operations, a given digit of CR will hold a one if that digit was the same in both old and new words, and a zero if the digit was different. During the ES write operation which starts with TP2, the check register digits are examined and writing takes place in the storage tube for a given digit if and only if that digit of the check register holds a zero. Thus writing takes place in only those digits in which the old and new contents of register x differ.

The second difference between the early portions of the bi and bo orders is a SENSE INTERLOCK #3 pulse which occurs on TP8 of the bi order. This sense pulse determines whether a word was obtained from the buffer drum on the si order which preceded the present bi. If no information was available from the buffer drum, the block control will be set at this time, and the order will be terminated as explained in E-499. When the bi order is used with the auxiliary drum, this sense pulse does nothing.

On TP8 of both the bi and bo orders an ADD ONE pulse is sent to IODC and the clock is stopped for 2 μseconds to allow an end-carry to appear in case a zero length block transfer has been requested.

In both orders the block control is sensed on TP1, and the orders are terminated at that point if zero-length blocks have been requested. In the case of the bo order no confusion can result because the order is terminated before any in-out operations have taken place. However, with the bi order, one word has been read into IOR from the external unit before it is discovered that no words are desired. In the case of the auxiliary drum the word is not lost, but SAR has been indexed one step, so that unless SAR is reset by an si 701 or 703, the word will be skipped. In the case of the buffer drum, however, the situation is worse because in some modes of operation the word may be permanently lost.

Let us assume that the SENSE BLOCK CONTROL #4 pulse on TP1 of the first cycle of the bi order finds the block control clear and consequently does nothing. We have therefore not asked for a zero-length transfer. It is now necessary to determine whether a one-word transfer has been ordered. In order to avoid requesting another word from the external unit and then discovering that the other word is not wanted, we must add one to IODC and wait for a possible end-carry before requesting another word. Accordingly an ADD ONE pulse is sent to IODC on TP1 and the computer clock is stopped for 2 μseconds to allow an end-carry from the counter to appear if it will.

Let us now assume that the block to be read contains more than one word. The block control will then remain clear, and when the SENSE BLOCK CONTROL #1 pulse appears on TP2 it will not terminate the order but will become an INITIATE READ pulse which goes to the drum system to initiate a reading operation. The same pulse also becomes an IOC RESET pulse which sets the interlock and clears the alarm control. At the same time, the word in IOR is transferred to the program register and if the storage address is in ES, an ES writing operation is started. Also on TP2 an END-AROUND CARRY pulse adds one to the contents of the accumulator so that the next word of the block will be placed in the next ES register. It should be noted that these last two actions occur whether or not the order was terminated by the SENSE BLOCK CONTROL #1 pulse. The effect of the termination does not appear until the clock is restarted after the ES writing operation. The END-AROUND CARRY results in the accumulator holding a number one greater than the ES address of the last word in the block.

The clock is stopped for 36 μseconds during the ES writing operation. When it is restarted TP3 appears and the contents of the accumulator are transferred to the storage switch in preparation for storing the next word. On TP4 a SENSE INTERLOCK pulse is sent to IOC. This pulse stops the clock if the drum reading operation is not yet complete. Also on TP4 an ES reading operation is initiated as the first part of the selective writing process for the next word in the block. This operation is performed even though the SENSE INTERLOCK pulse has stopped the clock. The clock will be restarted, however, only when both the drum reading operation and the ES reading operation, which requires 17 μseconds, are complete.

On TP5 the time pulse distributor is cleared so that TP1 will follow and the cycle will repeat. At the same time the contents of the program register are read to the check register as part of the selective writing process, and a SENSE BLOCK CONTROL #3 pulse is sent out to see if the buffer drum has been unable to supply the word requested by the INITIATE READ pulse on TP2. When the auxiliary drum is selected, this SENSE pulse does nothing, and the order goes on to the next cycle.

When IODC finally produces an end-carry in response to the ADD ONE pulse on TP1 of some cycle of the order, the SENSE BLOCK CONTROL #1 pulse on TP2 of that cycle will terminate the order leaving the accumulator holding one more than the ES address of the last word of the block.

Let us now examine the timing of the bi order with reference to the auxiliary drum. We assume, for convenience, that the bi order has been given sufficiently soon after the si (Read) order that the drum has not yet found the first word of the block when the bi order begins. The SENSE INTERLOCK pulse on TP6 then stops the clock but the ES read operation goes on. If the word has not arrived from the drum when the ES read operation is completed, the computer stops all activity and waits for the ASYNC INITIATION pulse from the drum which will announce the fact that the desired word has been placed in IOR.

Let us start counting the time which is required for the order from the instant that the ASYNC INITIATION pulse arrives. We will first ignore restoration and then go back and examine its effect on the total time requirements of the order. Within 3 μseconds after the ASYNC INITIATION pulse TP7 will appear. Because of the two stop-clock delays on the first cycle, TP2 will not appear for another 5 μseconds. With the appearance of TP2, and assuming another word is to be read, an INITIATE READ pulse goes to the drum system. Because of the delays in the drum reading circuits, this pulse must be sent within a period of approximately 45 μseconds after the arrival of the ASYNC INITIATION pulse if the next word is to be read without waiting an entire drum revolution. In this case the delay has been only 8 μseconds, and there is thus a considerable timing margin at this stage of the order.

On TP2 an ES write operation is initiated, and TP3 does not therefore appear for 37 μseconds. TP4 appears 1 μsecond later and at this point the interlock is sensed to see if the next word is available yet. So far 46 μseconds have elapsed since the first word arrived, and the clock will be stopped to wait for the next word which is not due until 64 μseconds after the first word. Also on TP4 an ES read operation stops the clock for 17 μseconds so that even though the word arrives the clock cannot restart until at least 64 μseconds (46 + 17 + 1) after the first ASYNC INITIATION pulse. If restoration is taken into account, this time becomes somewhat longer. The exact amount of elapsed time depends upon the time relationship between the frequency divider

output which feeds the restorer pulse generator and the ASYNC INITIATION pulse which started the sequence of operations. In any case, the first cycle of the order can be expected to take somewhat more than 64 μseconds so that the clock will not be stopped to wait for the second word to be placed in IOR.

When TP5 appears at least 64 μseconds after the first ASYNC INITIATION pulse, the order is effectively at the same position it was on TP7 of the first cycle. From TP7 to TP2 of the first cycle at least 5 μseconds must elapse, but between TP5 and TP2 of the next cycle only 3 μseconds are required. The first cycle is thus seen to be at least 2 μseconds longer than succeeding cycles. In addition, the first cycle requires 3 μseconds between the arrival of the ASYNC INITIATION pulse and the first time pulse to appear (TP7) after the clock is started. On cycles after the first, the ASYNC INITIATION pulse usually arrives during the ES read operation following TP4. In this case no time is lost while this pulse is being synchronized. Cycles after the first are therefore approximately 5 μseconds shorter than the first cycle. This 5 μseconds is nearly enough to allow for the average increase in required time due to restoration. Some cycles will be longer than 64 μseconds, but some will also be shorter, and as long as the total elapsed time for n cycles does not exceed $64n + 37$ μseconds the order will catch every word without having to wait whole drum revolution times for each word. The additional 37 μseconds comes from the margin achieved by starting the bi order before the drum has found the first word. The computer thus is allowed to start its first cycle very shortly after the arrival of the first word.

An examination of the various possible occurrences of restoration times during a bi cycle indicates that a periodic pattern will be set up due to the periodicity of both drum coincidence pulses and restorer pulses. The result of this periodic behavior is an average lost time due to restoration that is much less than would be anticipated if restoration were assumed to occur randomly. If this periodicity should fail to occur, or if for other reasons, as yet undiscovered, the timing should prove too critical, the situation can be remedied by forcing restoration to occur only at the correct times during the order. In addition one or two μseconds per cycle can be saved by reducing the amount of time that the clock must be stopped while waiting for an end-carry to appear from IODC.

SIGNED J. W. Forgie
J. W. Forgie

APPROVED E. S. Rich
E. S. Rich

JWF/cp
Table I Attached
Drawing Attached: E-37318

TABLE I

si ORDERS RELEVANT TO THE AUXILIARY DRUM

Function	Octal Address	Decimal Address	Binary Representation
Prepare for recording	si 704	si 452	0000000 111 000 100
Prepare for recording and change position	si 705	si 453	0000000 111 000 101
Prepare for recording and change group	si 706	si 454	0000000 111 000 110
Prepare for recording and change group and position	si 707	si 455	0000000 111 000 111
Prepare for reading	si 700	si 448	0000000 111 000 000
Prepare for reading and change position	si 701	si 449	0000000 111 000 001
Prepare for reading and change group	si 702	si 450	0000000 111 000 010
Prepare for reading and change group and position	si 703	si 451	0000000 111 000 011

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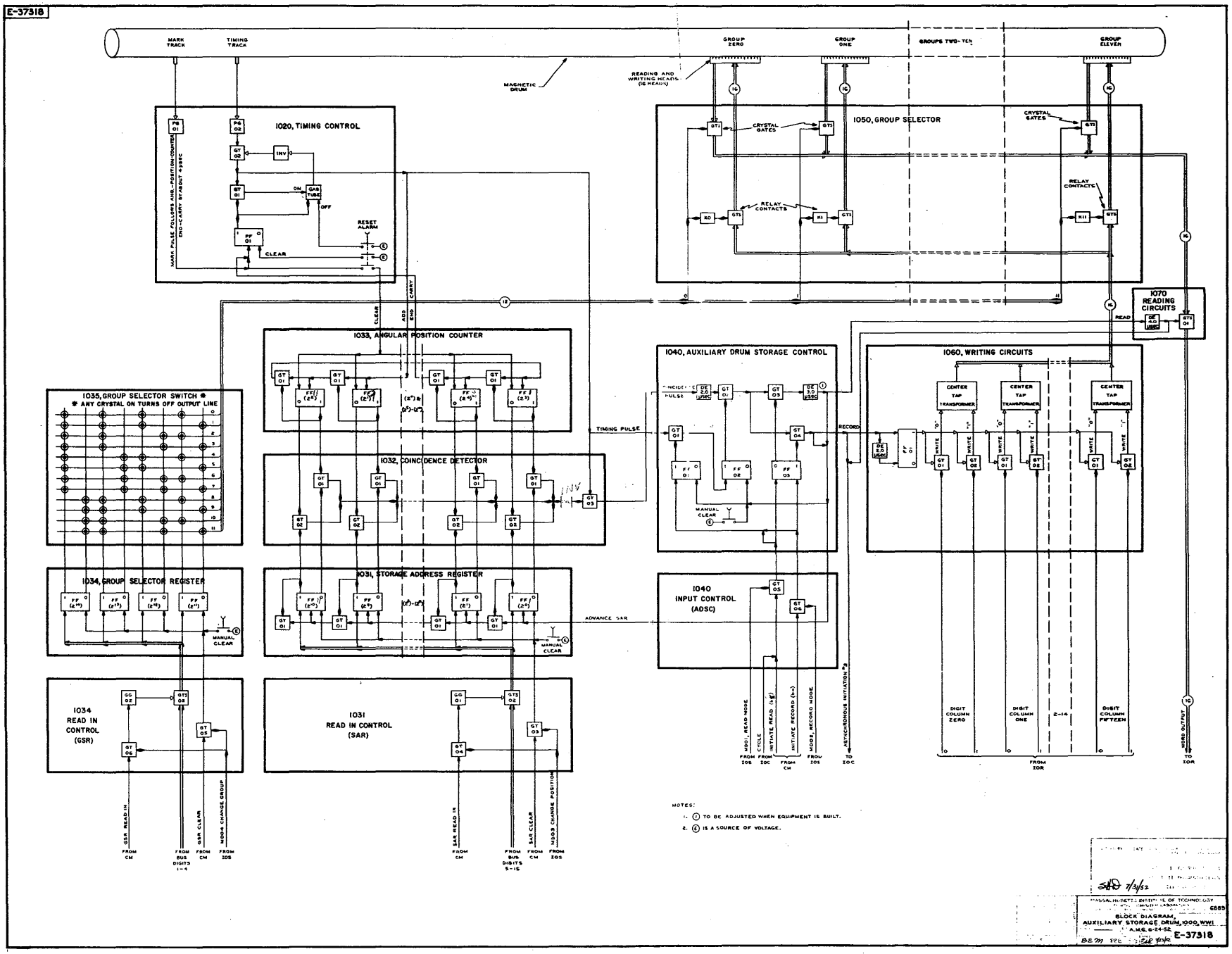

SHD 7/3/52

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6885

BLOCK DIAGRAM,
AUXILIARY STORAGE DRUM, 1000, WWI
A.M.S. 6-24-52

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