

ENTER  
R

GROUP 0 1 2 3 4 5 REGISTER

CONSOLE INTERRUPT



# Systems Design Handbook



# MODCOMP Makes the Tools

Modular Computer Systems, Inc., or "MODCOMP" as the marketplace has come to call us, is a real-time computer systems company. We specialize in offering all of the hardware and software tools needed for:

- Measurement and Control
- Communications
- FORTRAN Computing

End users and turn-key system suppliers can select a set of MODCOMP tools matched to almost any requirement in these application areas. With a complete and compatible set of tools, the user can concentrate on his application and get on-line in minimum time.

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## MODCOMP Tools Include

### ■ A Family of 16-Bit Computers

The compatible MODCOMP I, MODCOMP II and MODCOMP III computers cover almost all 16-bit applications and many presently handled by 32-bit computers.

### ■ A Choice in Programming Approach

You can write real-time as well as scientific programs in MODCOMP FORTRAN and minimize your programming effort. Or you can program your system in macro assembly language and optimize programs for your requirements. In either case, you can run your programs under MAX III, the most complete real-time, multiprogramming executive in operation with any 16-bit computer. MAX III offers an unmatched set of re-entrant services which reduces your programming job even more. BASIC, cross assemblers and other MAX executives are also available.

### ■ Data Processing Peripherals

A broad range of paper tape, magnetic tape, disc, printer, display and punched card equipment is offered with MODCOMP computers. And MODCOMP software supports all offered peripherals.

### ■ Real-Time Peripherals

MODCOMP designs and builds equipment which can handle almost all types of analog inputs, analog outputs, digital inputs and digital outputs.

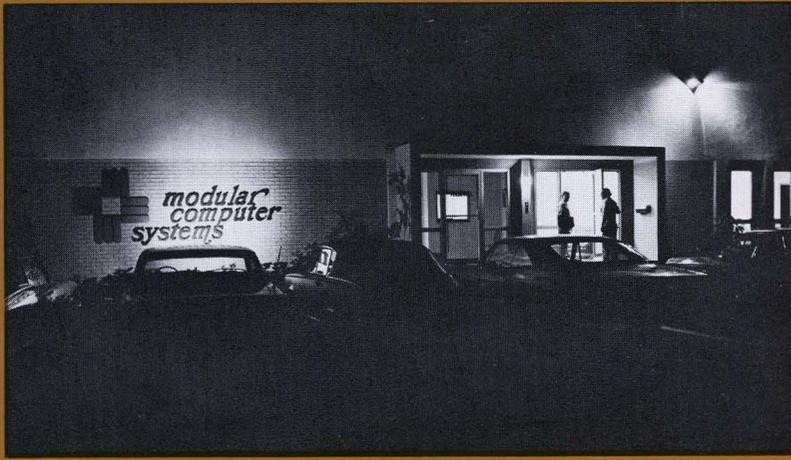
### ■ Communications Interfaces

A choice of communications multiplexers is available for line concentration, preprocessing and message switching applications. Individual line interfaces are also available to enable MODCOMP computers to communicate with remote computers and terminals.

### ■ Custom Engineering and Programming

MODCOMP has system engineers and programmers who are ready to develop special interfaces, terminals and programs to expand system capabilities.

# MODCOMP Facilities



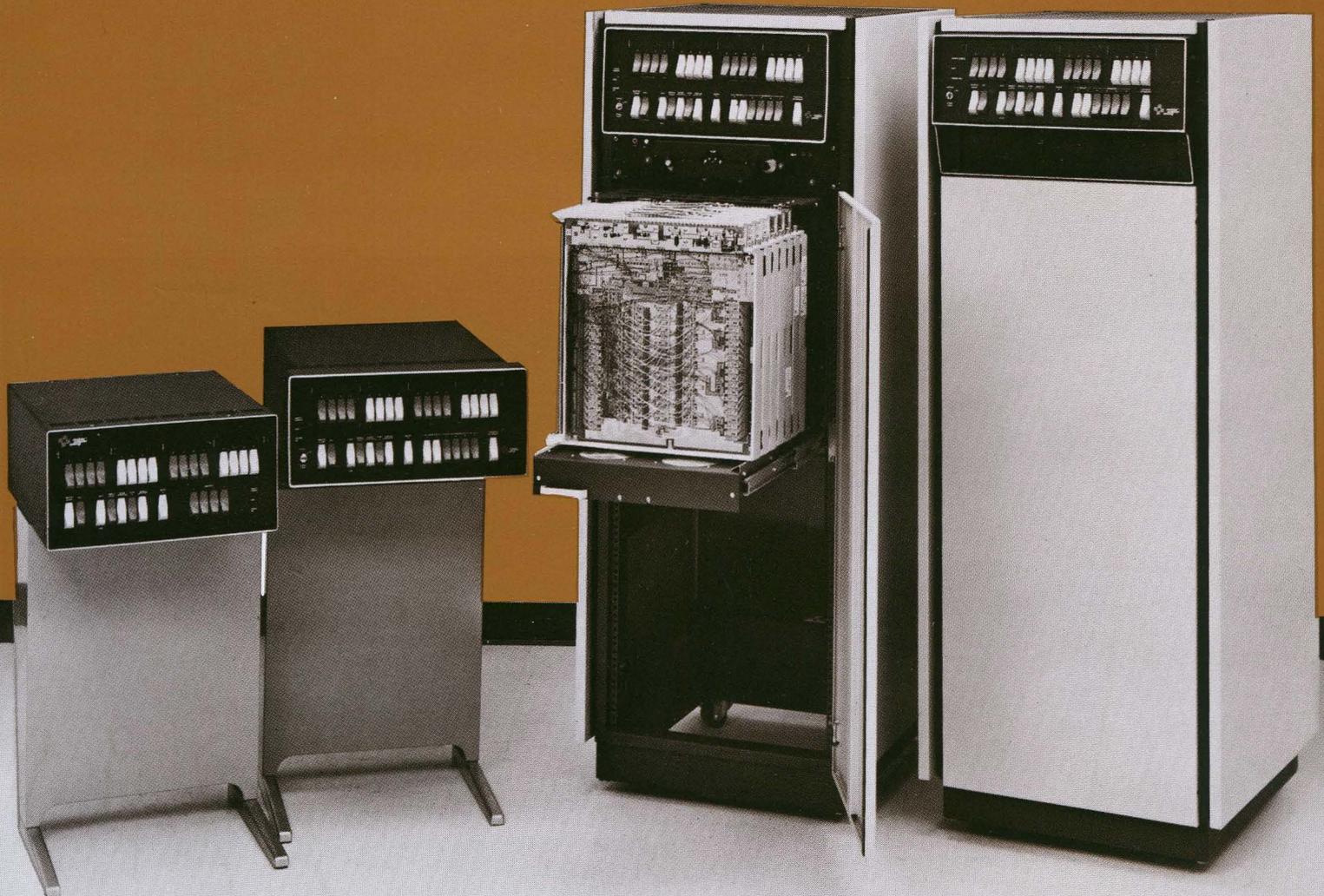
MODCOMP is a dynamic, rapidly growing company. Headquarters, shown left, are located in Ft. Lauderdale, Florida. Our present sales and service centers include:

New York	Dallas
Washington, D.C.	Houston
Detroit	San Francisco
Chicago	Los Angeles
Atlanta	Seattle

## EUROPEAN REPRESENTATIVES

Dynatec, A.G.	
Dusseldorf	Hamburg
Frankfurt	Munich
Telecontrol International, S.P.R.L.	
Brussels	Antwerp

Four members of the MODCOMP computer family are, left to right, the MODCOMP I/5, MODCOMP II/5, MODCOMP II/20 and MODCOMP III/5. The small computer enclosures can hold up to 32K words of memory and the larger enclosures up to 64K words.



# MODCOMP Has Delivered

From its modern manufacturing / office facility, Modular Computer Systems has delivered to customers in almost every industry.

MODCOMP systems are now being used in many university, laboratory, factory, and government facilities. Application examples include:

## University

- Communications Preprocessing – Central Computing Facility
- Centralized Data Collection – Interdepartment Communications Network
- Man-Machine Interaction Studies – Psychology
- Data Reduction – Space Laboratory
- Data Collection and Control – Physics, Chemistry, Medicine

## Laboratory

- Signal Analysis – Communications
- Radar Data Analysis – Aerospace
- Growth Environment Control – Agriculture
- Reactor Control – Nuclear
- Emission Testing – Automotive
- Mass Spectrometer Control – Metals

## Factory

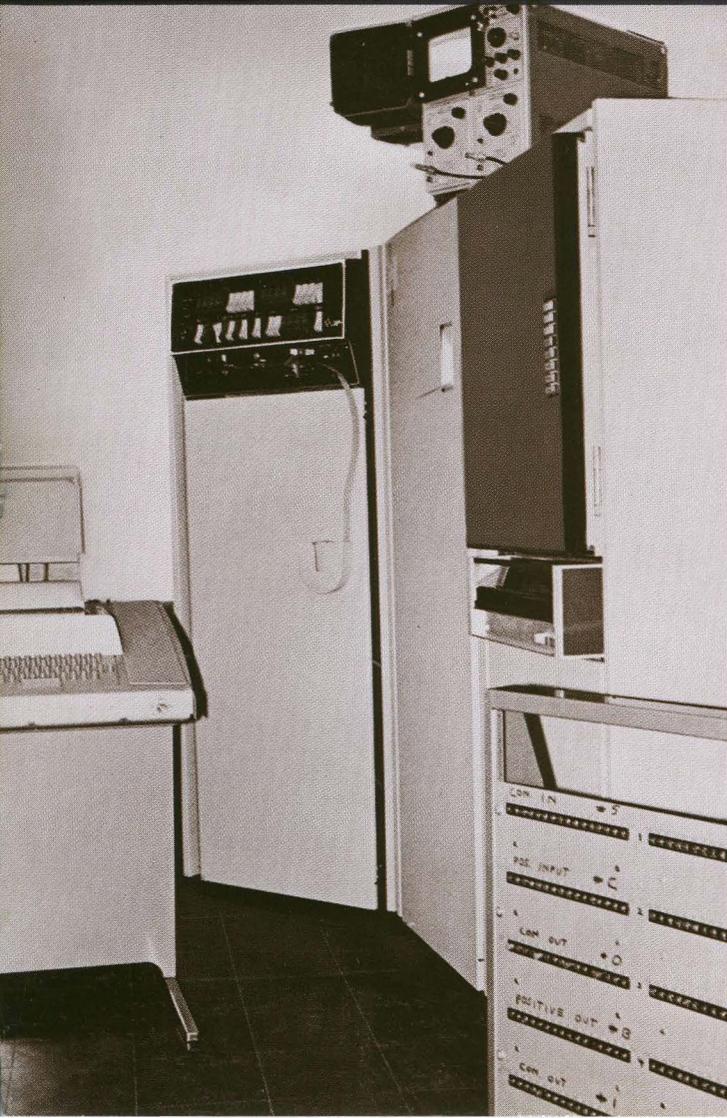
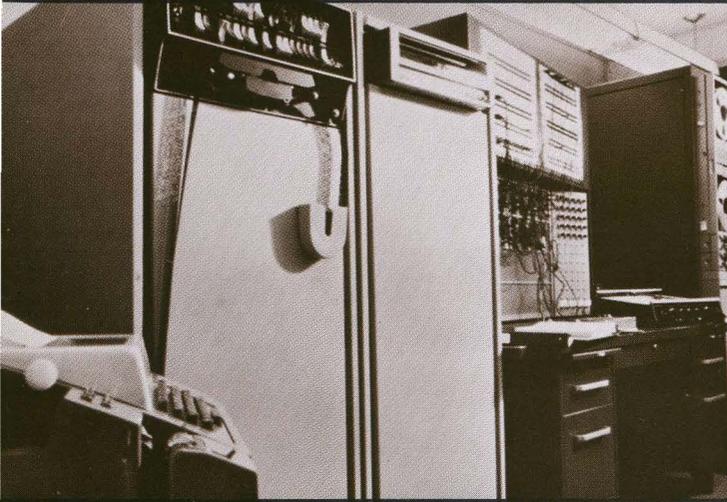
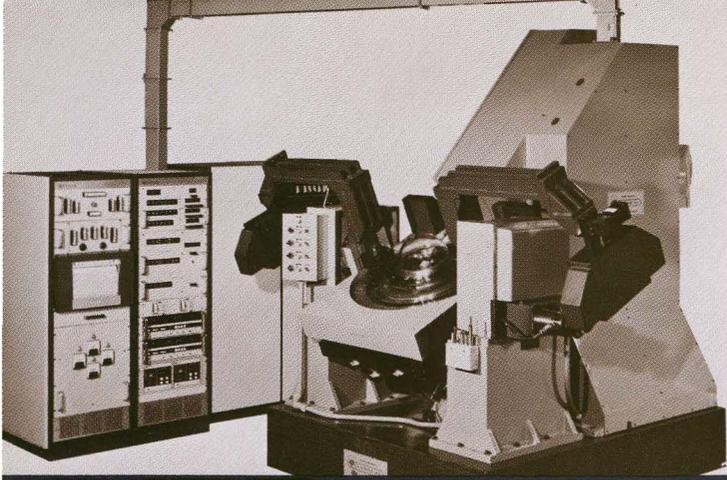
- Factory Information Systems – Chemical
- Loom Monitoring – Textile
- Process Scheduling – Metal Finishing
- Process Control – Metals and Chemicals
- Manufacturing Parts Testing – Automotive
- Engine Test Stand Control – Aircraft
- Gaging System Control – Nuclear
- Precision Welding Control – Nuclear

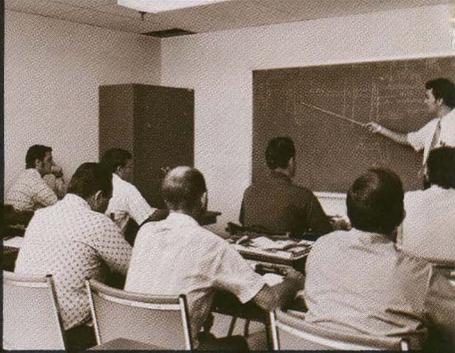
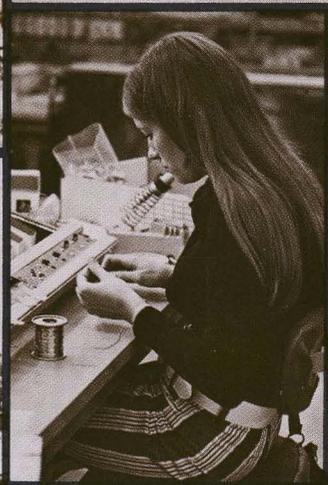
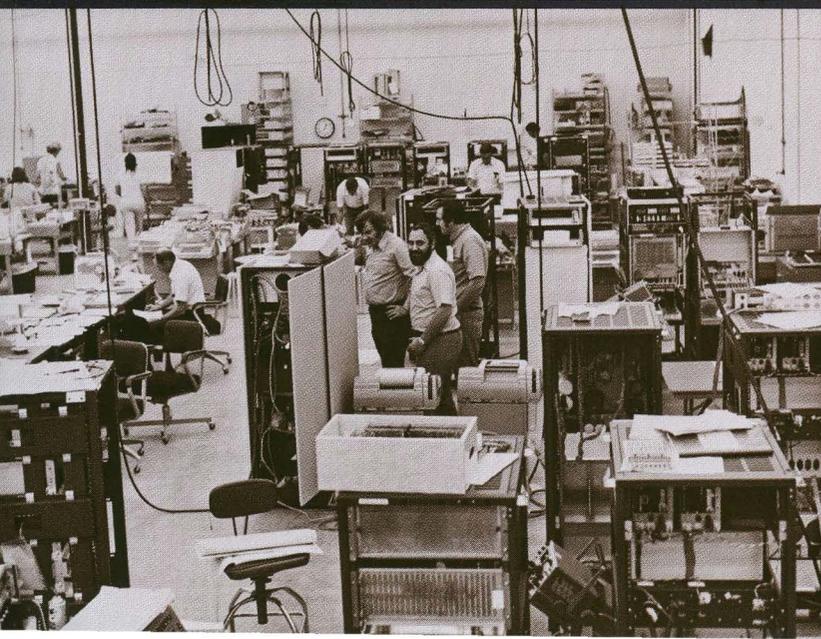
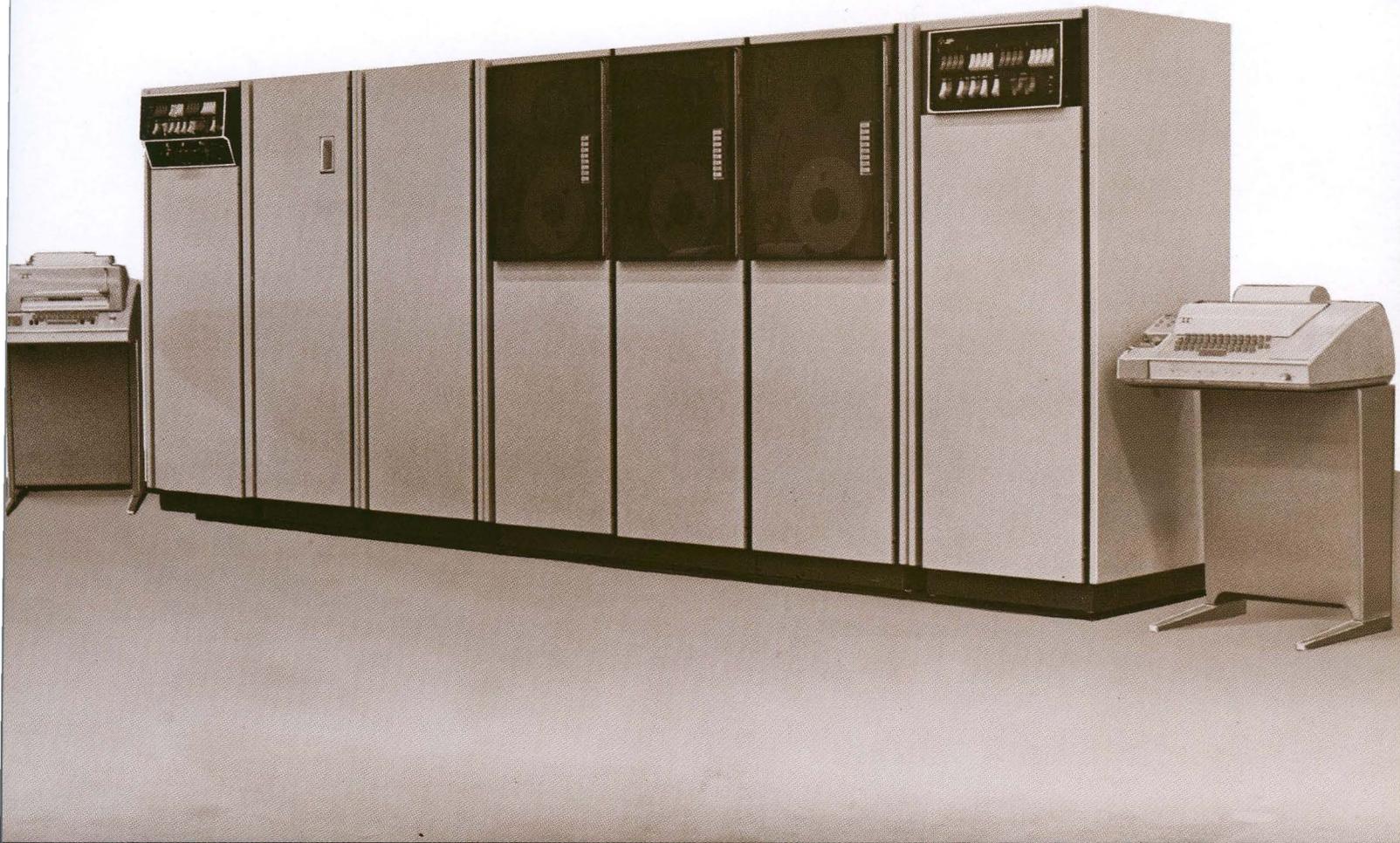
## Government

- Remote Job Entry
- City Traffic Control
- Test Range Control and Telemetry Data Collection
- Animal Test Data Collection and Processing
- Military Equipment Testing
- Post Office Scheduling and Control

## Other

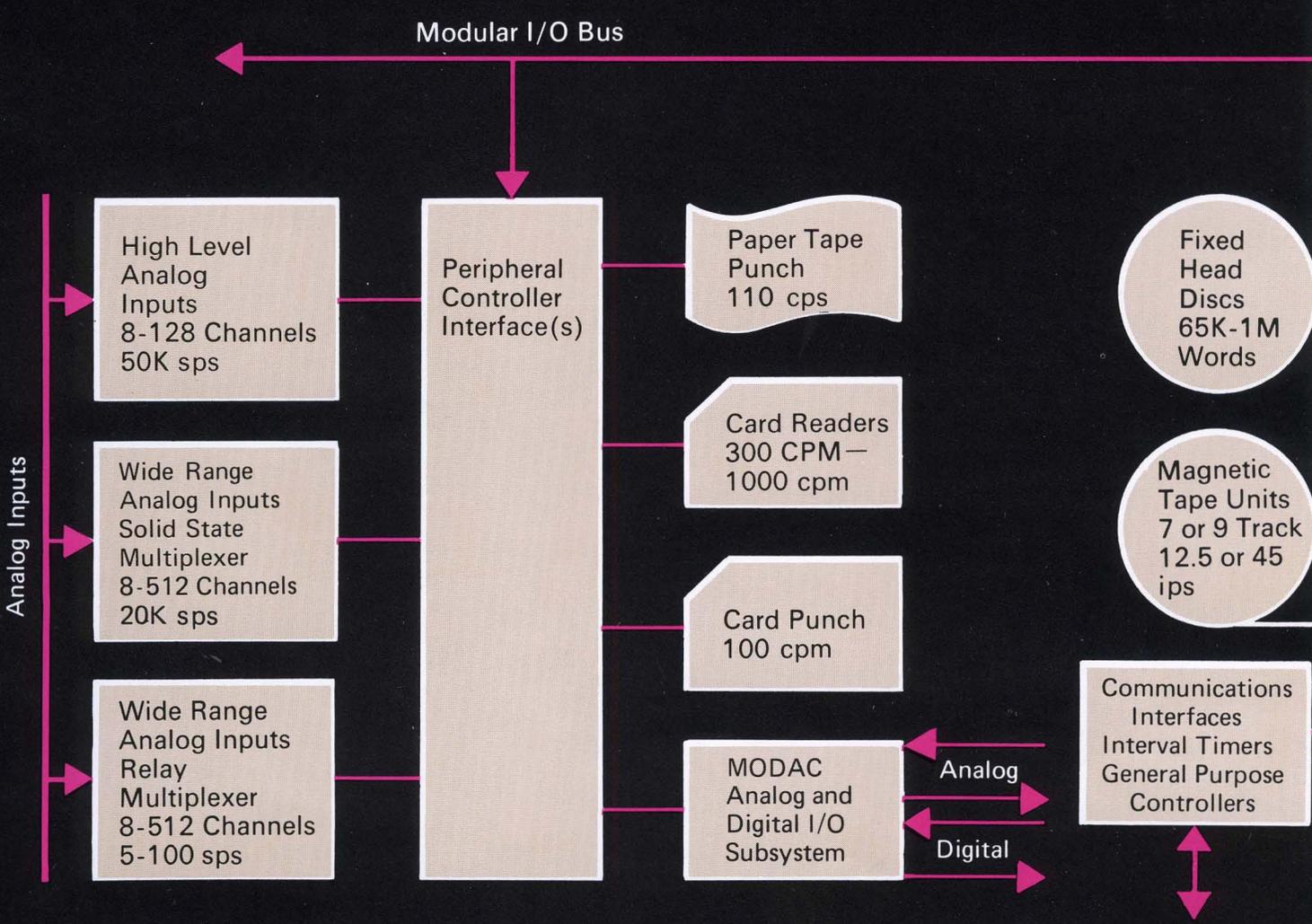
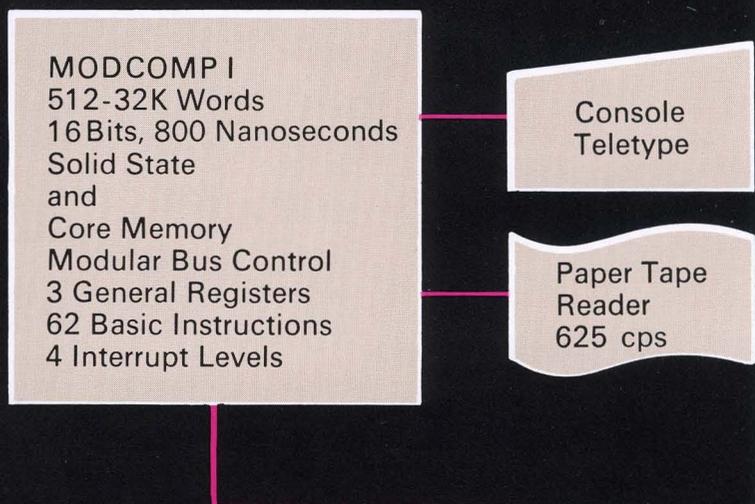
- Communications Line Concentration
- Time-Shared Accounting
- Building Environment Control
- Power Generation Control





The overall block diagram at right summarizes the MODCOMP family of compatible system building blocks. The hardware modularity permits MODCOMP systems to remain the most advanced state of the art systems available, because MODCOMP computers and other products have been designed to permit easy upgrading and expansion. At the same time, new MODCOMP systems will remain program and input/output compatible with existing systems.

Therefore an investment in a MODCOMP system provides for the future as well as meeting present requirements. Users can be assured of long term support for their present systems and availability of higher performance but compatible units when they need them.



**MODCOMP II**  
 4-64K Words  
 16 Bits, 800 Nanoseconds  
 15 General Registers  
 Floating Point Hardware  
 Memory Protect  
 Multiport Memory  
 145 Basic Instructions  
 8 Direct Memory Channels  
 16 Interrupt Levels

Console  
 Teletype

Paper Tape  
 Reader  
 625 cps

**MODCOMP III**  
 4-64K Words  
 16 Bits, 800 Nanoseconds  
 15 General Registers  
 Floating Point Hardware  
 Memory Protect  
 Second Memory Port  
 Microprogrammable ROM  
 Firmware CRC and  
 Communications Character  
 Processing

Peripheral  
 Controller  
 Interface(s)

Moving  
 Head  
 Disc  
 1-26M  
 Words

Line  
 Printers  
 50-150 lpm  
 300 lpm  
 600 lpm

Communications  
 Multiplexers  
 Synchronous  
 Asynchronous

Modems

Terminals

Teletypes

Input/  
 Output  
 Interface  
 Subsystem

Contact Inputs & Outputs

Logic Level Inputs & Outputs

Analog Outputs

A-C Outputs

Common Alarm Inputs

Counter Inputs

Teletypes and Terminals

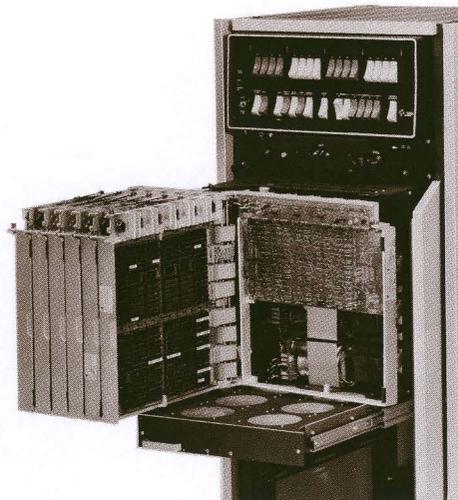
External Sync

# The Compatible Family of MODCOMP Computers

## MODCOMP I

This smallest MODCOMP computer is intended for dedicated data collection, processing and control applications. It offers many standard and optional features:

- 16-Bit Word Length
- 800 Nanosecond Cycle Time
- 2 - 32K Words of Core Memory
- Solid State Random Access Memory
- Solid State Read Only Memory
- Memory Parity
- Power Fail Safe / Auto Start
- Hardware Fill
- Hardware Multiply / Divide
- 8 Direct Memory Channels
- Real Time Clock - 1 msec.
- Optional Programmer's Panel
- 3 General Registers
- 4 Interrupt Levels
- 128 Interrupt Sublevels
- Modular Bus Control - External Control Capability For All Machine Resources
- Optional Internal Modem
- Upward Program Compatibility With MODCOMP II and III



## MODCOMP II

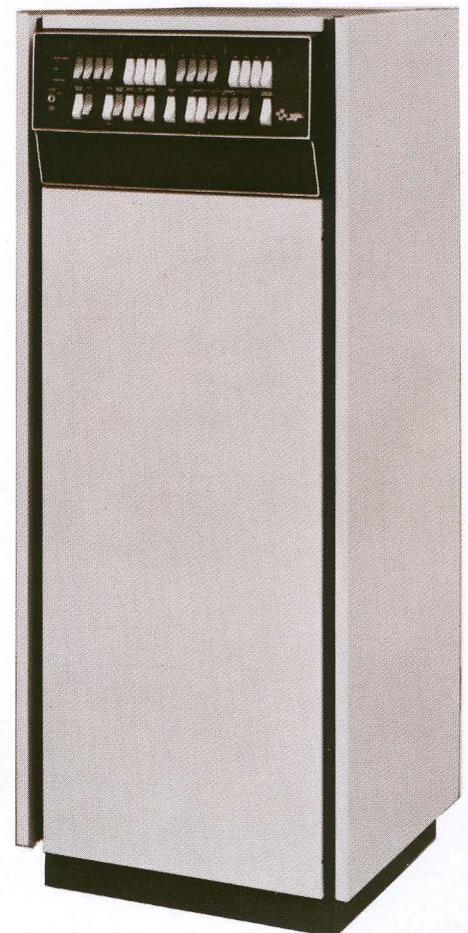
This newest MODCOMP computer has the same instruction set and most of the speed and other features of the big MODCOMP III. It is available in several different models which, collectively, offer:

- 16-Bit Word Length
- 800 Nanosecond Cycle Time
- 4 - 64K Words of Core Memory
- All Memory Directly Addressable
- Memory Parity
- Memory Protect
- Multi-port Memory
- Power Fail Safe / Auto Start
- Hardware Fill
- Console Interrupt
- Panel Protect Keyswitch
- 15 General Purpose Registers
- Hardware Multiply / Divide
- Hardware Floating Point
- Bit, Byte, Word, Doubleword and File Manipulation
- 174 Microprogrammed Instructions
- 8 Direct Memory Channels
- Real-Time Clock - 5 msec.
- 16 Priority Interrupt Levels
- 128 Interrupt Sublevels

## MODCOMP III

The largest MODCOMP computer has all of the characteristics of the MODCOMP II plus these additional features:

- Optional Control ROM
  - Additions to the standard instruction set can be microprogrammed and added to increase capabilities in specific application areas.
- Communication Processing
  - The MODCOMP III/5 Communications Processor provides microprogrammed instruction extensions which perform character editing and CRC generating / checking with firmware. The MODCOMP III/5 CP also supports direct memory transfers for up to 256 communication lines. Additional capabilities include:
- 32 Interrupt Levels
- 16 Direct Memory Channels



# MODCOMP Software

**MODCOMP I** is supplied with MIN I, an easy-to-use program preparation system plus SAX I, a small real-time multiprogramming executive. An assembler, relocatable loader, text editor, utilities and diagnostics all operate in basic configurations. In addition, a cross assembler which operates in an IBM 360 or 370 and a compatible assembler which operates in MODCOMP II and III computers are available. Application software includes communications line handlers and remote data acquisition handlers.

**MODCOMP II and III** are supplied with the most advanced software offered with any 16-bit computer. Three Modular Application Executives and a choice of assemblers and compilers are available and field proven.

**MAX I** is a core-resident program preparation and debugging system for small configurations.

**MAX II** is a batch processing system available as a core resident system or disc operating system with file management capabilities available to both the assembler and FORTRAN users.

**MAX III** is a task-oriented, real-time multiprogramming system for foreground/background applications as well as for dedicated data acquisition and control applications. It consists of software modules linked by a system generation program forming a real-time executive tailored to the user's application. The basic MAX III features include:

- Up to 128 foreground task priority levels.
- Up to 127 additional middleground task priority levels.
- Background batch processing.
- Task activation by interrupt, operator request, other active task, elapsed time or time-of-day.
- Directly connected task capability.
- Queued input / output.
- Dynamic core and disc allocation.
- Disc file management.
- Re-entrant executive services.
- Global communication capability for resident, re-entrant library and data accessed by multiple tasks.
- Flexible operator communications package.
- Checkpointing capability.

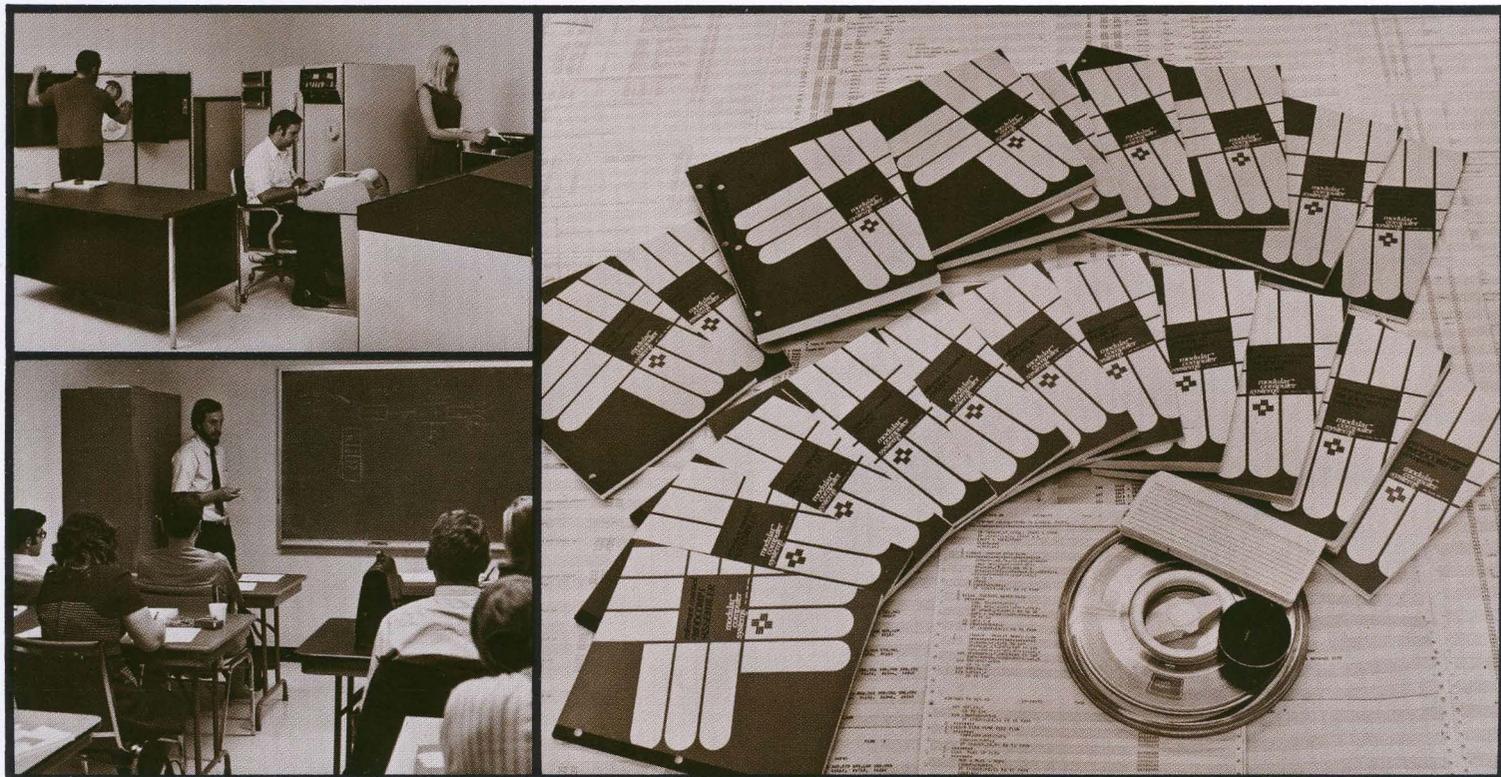
**FORTRAN IV** — MODCOMP Real-Time FORTRAN is one of the few 16-bit compilers which meets the full ANSI specifications. It is available in three versions — ANSI standard, extended, and extended overlay. Subscript and block optimization techniques are used in the extended versions.

**Assemblers** — A basic assembler, macro assembler, and a MODCOMP I cross assembler all operate under the MAX systems. In addition, a FORTRAN-coded cross assembler is available which operates in IBM and CDC computers.

**BASIC** — This interactive system operates both under MAX II and as a multiterminal middleground task under MAX III.

**Diagnostics, Utilities, Math Library** — a wide variety of support software is offered with MODCOMP systems.

**Communications Software** — Device independent line handlers are available for all multiplexers and line interfaces. Both MAX and SAX systems support line handlers. Remote job entry and other packages including binary synchronous discipline are also available.



# Communications

MODCOMP systems are being used both as dedicated communications systems and as measurement and control or scientific systems with communications extensions. Dedicated communications functions include:

- Line Concentration
- Message Switching
- Preprocessing and Front Ending

Communications extension functions include:

- Communications with Remote Computers
- Communications with Remote Terminals
- Remote Data Acquisition
- Remote Job Entry

MODCOMP communication line interfaces are available to support either one or a few lines per system. These interfaces are supported by software handlers which operate under the MAX operating systems. Therefore, it is possible to perform functions such as Remote Job Entry as one task in a system which is also performing other real-time tasks such as data acquisition and control.

MODCOMP communication line multiplexers are available for systems requiring many line interfaces.

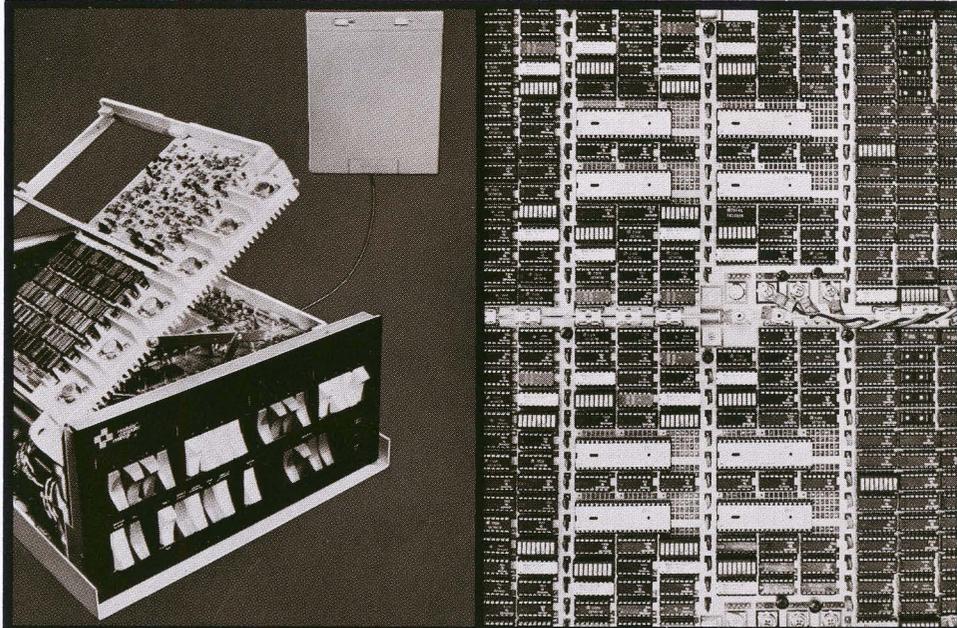
## Asynchronous Multiplexer

- 4 - 128 Lines per Controller
- Full or Half Duplex Operation
- 75 - 9600 Baud
- Programmable Baud Rate
- Programmable Frame Size
- Programmable Parity Checking
- RS232C and Current Loop Line Interfaces

## Universal Multiplexer

- 4 - 64 Lines per Controller
- Synchronous and Asynchronous Line Interfaces
- Full or Half Duplex Operation
- Direct Memory Transfer with MODCOMP III/5 Communications Processor
- 110 - 50K Baud Rate
- Programmable Baud Rate
- Programmable Frame Size
- Programmable Parity Checking
- Special Character Detection
- RS232C and Current Loop Line Interfaces

Shown are the MODCOMP I computer with line interface and modem; one plane of the Universal Communications Multiplexer which can contain eight synchronous or asynchronous interfaces and a MODCOMP III system being used at a state university for space data reduction and remote job entry into the campus central computing facility.



# Measurement and Control

MODCOMP offers a choice of five measurement and control subsystems which can be configured to meet most requirements.

## Wide Range Solid State Analog Input Subsystem

- $\pm 5\text{MV}$  to  $\pm 10.24\text{V}$  Full Scale Inputs
- 12 Programmable Gain Ranges
- 8 - 512 Input Channels
- 20,000 Samples per Second
- 12-Bit Binary A-D Converter
- Auto Ranging
- Zero Suppression - 15 Bits
- Selectable Input Filters
- Guarded Differential Inputs with 3 MOS FET Switches per Channel

## Wide Range Relay Analog Input Subsystem

- $\pm 5\text{MV}$  to  $10.24\text{V}$  Full Scale Inputs
- 12 Programmable Gain Ranges
- 8 - 512 Input Channels
- 5 - 100 Samples per Second
- 12 Bit Integrating A-D Converter
- Auto Ranging
- Zero Suppression - 15 Bits
- Selectable Input Filters
- Guarded Differential Inputs with 3 Mercury Relay Switches per Channel
- $\pm 200\text{V}$  Common Mode Voltage ( $\pm 500\text{V}$  on Special Order)

## High Level Analog Input Subsystem

- $\pm 10.24\text{V}$  or  $\pm 102.4\text{V}$  Full Scale Inputs
- 8 - 128 Input Channels
- Single-Ended or Differential Inputs
- 50,000 Samples per Second
- 12 Bit Binary A-D Converter
- Selectable Input Filters
- MOS FET Gate Switches

## Input/Output Interface Subsystem

- 16-Bit Digital Input Channels
  - Voltage Inputs
  - Contact Inputs
  - Isolated Inputs
- 16-Bit Digital Output Channels
  - Voltage Outputs
  - Contact Outputs
  - Electronic Switch Outputs
  - A-C Switch Outputs
- Storage CRT Interfaces
- Common Alarm Channels
- Interrupt Couplers
- Interval Timers
- Asynchronous Communications Interfaces for Terminals

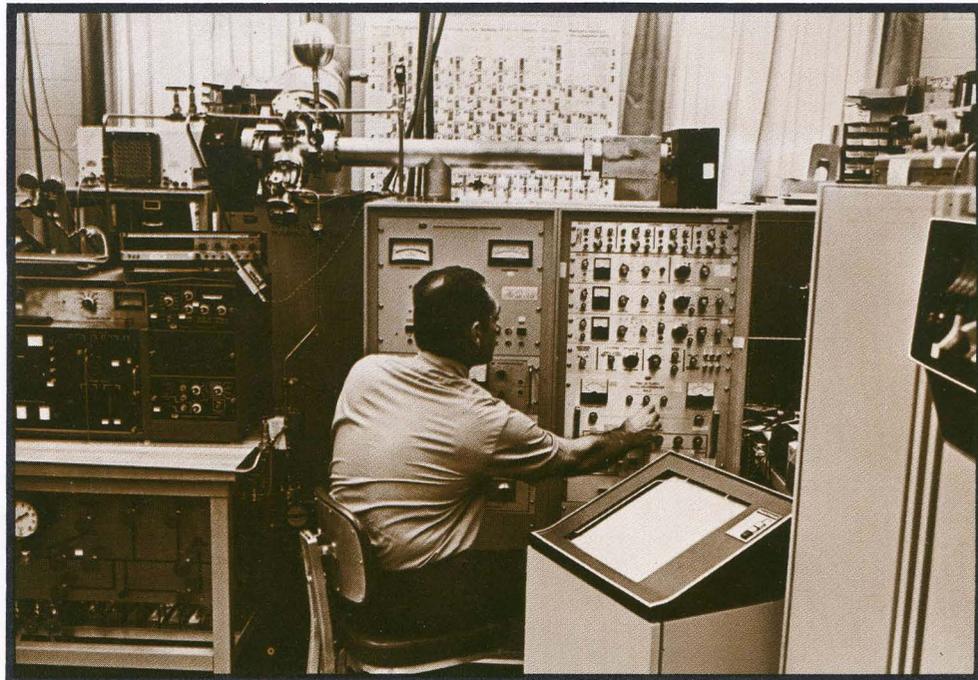
## MODAC Analog and Digital Subsystem

MODAC Subsystems are economical for small numbers of inputs and outputs.

- Analog Input Module
  - 16 or 32 10-Volt Inputs
  - 20,000 Samples per Second
  - 12-Bit Binary A-D Converter
- Analog Output Module
  - 4 or 8 Analog Outputs
  - Current Outputs
  - Voltage Outputs
- Digital Input Module
  - 32 Voltage or Contact Inputs
- Digital Output Module
  - 32 Voltage, Contact or Electronic Switch Outputs

A MODAC unit can contain up to seven modules of any type.

Below is a time-of-flight mass spectrometer controlled by a MODCOMP III computer.



# MODCOMP I

## General-Purpose 16-Bit Computer



## Features

The MODCOMP I computer is the smallest member of the compatible MODCOMP computer family. It is designed for applications such as:

- Data Acquisition
- Dedicated Control
- Line Concentration
- Remote Terminal Control

### Broad Range of System Components

The complete line of measurement, control, communications, and peripheral equipment available with the MODCOMP I enables most system hardware requirements to be met by a single supplier. MODCOMP I software also offers a broad choice including executives, assemblers, loaders, editors and utilities.

### Family Compatibility

The MODCOMP I is input/output compatible with the MODCOMP II and III computers. Peripheral controllers and I/O interfaces developed for one machine are usable on the other machines.

MODCOMP I is also upward program compatible with the larger MODCOMP computers. Programs can be assembled and debugged in the larger machines and then loaded and executed in MODCOMP I.

### Modular Construction

The modular construction of MODCOMP I offers a particular advantage for applications requiring a computer plus a moderate amount of system interface circuits. An option plane which can contain over 300 integrated circuits, a modem or other user interface can be mounted and powered inside the 8-3/4" x 19" x 21" computer enclosure. Interfaces can be connected to the I/O Bus or directly to the internal bus using the Modular Bus Control. Many existing MODCOMP I systems used for remote data acquisition and communication take advantage of these capabilities.

## Software Features

Two small operating systems are available:

- MIN I — For program preparation, debugging and source editing



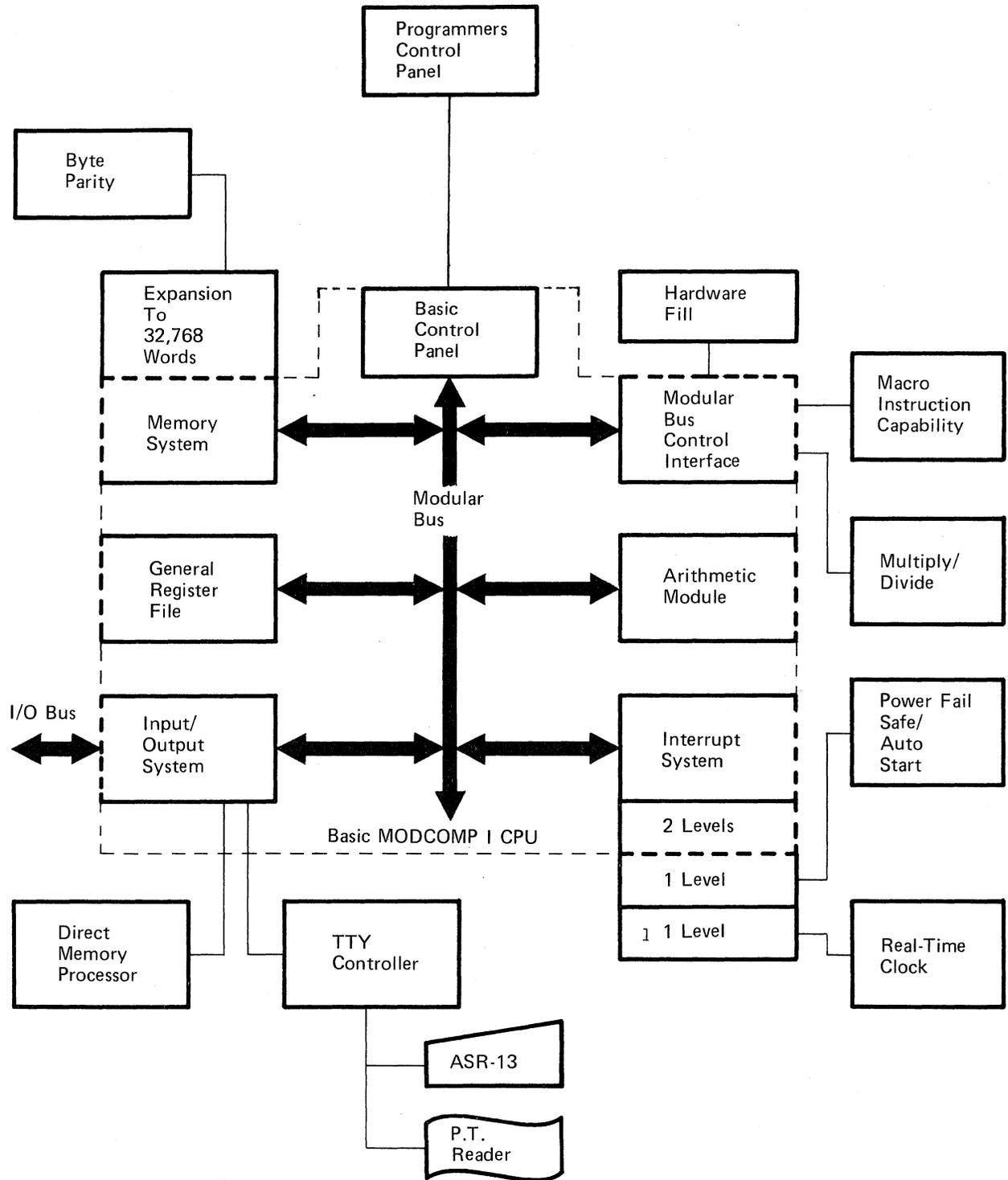
MODCOMP I Computer

- SAX I — A real-time executive which enables multiple tasks to be scheduled and executed on a priority basis.
- A choice of four assemblers exists:
- Basic Assembler — For 2K memory configurations.
  - Extended Assembler — For 4K memory configurations and above. Generates relocatable output.
  - 360, 370 Cross Assembler
  - MODCOMP II, III Cross Assembler

In addition to executives and assemblers, a relocatable loader, diagnostics and communication line handlers are available with MODCOMP I.

## Hardware Features

- 16-bits
- 800 Nanosecond Cycle Time
- 2K-32K Words of Core Memory
- All Memory Directly Addressable
- Memory Parity
- 2K-16K Words of Solid State Random Access Memory
- 512-2K Words of Solid State Read Only Memory
- Hardware Fill
- 3 General Purpose Registers plus Program Addressable Console Switch Register
- Hardware Multiply/Divide
- Power Fail Safe/Auto Start
- Real Time Clock
- Optional Programmer's Control Panel
- Modular Bus Control — External Control Capability for All Internal Resources
- Internal Modem Interface and Asynchronous Modem (110-9600 Baud)



Modcomp I Block Diagram

# MODCOMP I Organization

The organization of the MODCOMP I is shown in the Block Diagram. The elements which comprise the basic MODCOMP I are enclosed by the dashed lines. The other elements shown outside of the dashed lines can be added to the basic MODCOMP I in various combinations to suit the requirements of the application.

The MODCOMP I consists of storage, processing, and input/output modules and a modular bus through which all inter-module transfers are made. The major features of each module are summarized below:

## Memory System

- 2,048 to 32,768 words of core memory
- 2,048 to 16,384 words of solid state random access memory
- 512 to 2,048 words of solid state read only memory (ROM) intermixable with RAM or core memory
- 800 nanosecond full cycle time for all three types of memory
- Optional Byte Parity
- All memory locations directly addressable
- Four memory addressing modes including direct, indexed, immediate and displacement

## General Register File

- 3 addressable, general purpose registers
- All three registers available as index registers
- 800 nanosecond execution time for register to register instructions

## Arithmetic Module

- Parallel operation
- Arithmetic, logical, compare and shift capabilities

## Input/Output System

- Program controlled transfers to/from 63 peripheral devices.
- Transfers may be made under interrupt control
- Transfers can be made between any general register and any device
- I/O Bus is buffered to isolate the computer from external cable and controller delays
- Optional TTY controller will operate both ASR-33 and high speed paper tape reader
- Direct Memory Processor available for automatic block transfers to/from eight peripheral devices on a multiplexed, cycle-stealing basis

Many computers offer a "Direct Memory Access" feature which enables peripheral devices to transfer data to/from computer memory on a cycle-stealing basis. The MOD-

COMP I offers a Direct Memory Processor which enables up to eight devices to perform cycle-stealing, block transfer inputs or outputs concurrently. This unit contains the address and word count registers for each of the eight channels and the processing logic in addition to the basic memory access logic.

## Interrupt System

- Two standard interrupt levels each with 64 vectored sublevels
- Two optional interrupt levels for real-time clock and Power Fail Safe/Auto Start

## Modular Bus Control Interface

- Provides direct access to all central processor resources including memory, general purpose registers and arithmetic/logical unit

The Modular Bus control provides a unique capability among 16-bit computers. It enables data not only to be transferred to/from the computer under external control but also be manipulated in the computer under external control.

The Modular Bus Control brings the internal micro-control signals from within the computer to a set of connectors. Logic added by the user on an option plane inside the computer or even external to the computer can request use of all computer resources. The Modular Bus Control recognizes this request and grants resource control after the execution of the current instruction is completed. The user logic can then:

- Transfer words to/from core memory at rates up to 1,250,000 words per second
- Perform arithmetic and logical operations on data in addition to performing transfers to or from memory
- Perform special micro-coded operations which would require execution of several conventional machine instructions

These features offer the user a new type of capability in implementing computer control systems.

## Physical Characteristics

- 0-55C ambient operating temperature range
- 5 to 95% relative humidity, non-condensing
- 120 ± 10% VAC, 48 to 62 Hz
- Packaged for mounting in a standard 19 inch cabinet
- Height 8.75 inches, width 19 inches, depth 21 inches
- Weight — 70 pounds maximum
- Power — 600 watts maximum

## MODCOMP I INSTRUCTION LIST

<u>MNEMONIC</u>	<u>NAME</u>	<u>EXECUTION</u>	<u>BIT MANIPULATION</u>	
<u>LOAD, STORE AND TRANSFER</u>		<u>TIME (us)</u>		
LDM	Load Register from Memory	2.4	ABR Add Bit in Register 0.8	
LDI	Load Register from Memory Immediate	1.6	ABRB Add Bit in Register and Branch if Nonzero 1.6	
LDS	Load Register from Memory Short Displaced	1.867	LBR Load Bit in Register 0.8	
STM	Store Register in Memory	2.4	LBRB Load Bit in Register and Branch Unconditionally 1.6	
STI	Store Register in Memory Immediate	1.6	OBR OR Bit in Register 0.8	
STS	Store Register in Memory Short Displaced	1.867	OBRB OR Bit in Register and Branch Unconditionally 1.6	
TRR	Transfer Register to Register	0.8	SBR Subtract Bit in Register 0.8	
TRRB	Transfer Register to Register and Branch if Nonzero	1.6	SBRB Subtract Bit in Register and Branch if Nonzero 1.6	
GMR	Generate Mask in Register	0.8	TBRP Test Bit in Register and Branch if One 1.6	
GMRB	Generate Mask in Register and Branch Unconditionally	1.6	XBR Exclusive OR Bit in Register 0.8	
<u>ARITHMETIC</u>			XBRB Exclusive OR Bit in Register and Branch if Nonzero 1.6	
ADM	Add Memory to Register	2.4	ZBR Zero Bit in Register 0.8	
ADI	Add Memory to Register Immediate	1.6	ZBRB Zero Bit in Register and Branch if Nonzero 1.6	
ADS	Add Memory to Register Short Displaced	1.867	<u>BYTE MANIPULATION</u>	
ADR	Add Register to Register	0.8	IBR Interchange Bytes Register to Register 0.8	
ADRB	Add Register to Register and Branch if Nonzero	1.6	MBL Move Byte Left Register to Register 0.8	
DIV	Divide Register by Register	12.0	MBR Move Byte Right Register to Register 0.8	
MUL	Multiply Register by Register	10.0	MLR Move Lower Byte Register to Register 0.8	
SUM	Subtract Memory from Register	2.4	MUR Move Upper Byte Register to Register 0.8	
SUI	Subtract Memory from Register Immediate	1.6	<u>UNCONDITIONAL BRANCH</u>	
SUS	Subtract Memory from Register Short Displaced	1.867	BLM Branch and Link 1.6	
SUR	Subtract Register from Register 0	0.8	BRU Branch Unconditionally 1.6	
SURB	Subtract Register from Register and Branch if Nonzero	1.6	HOP Branch Short Displaced 1.067	
TTR	Transfer Two's Complement Register to Register	0.8	<u>CONTROL</u>	
<u>SHIFT</u>			HLT Halt —	
RAS	Shift Right Arithmetic Single	0.8	NOP No Operation 1.067	
<u>LOGICAL</u>			<u>INTERRUPT AND CALL</u>	
ETM	Extract Memory from Register	2.4	CIR Clear Interrupt and Return 1.867	
ETI	Extract Memory from Register Immediate	1.6	RIE Reset Interrupt Enable 0.8	
ETS	Extract Memory from Register Short Displaced	1.867	SIE Set Interrupt Enable 0.8	
ETR	Extract Register from Register	0.8	<u>INPUT/OUTPUT</u>	
ETRB	Extract Register from Register and Branch if Nonzero	1.6	IDA Input Data from I/O Group A 1.6	
ORM	OR Memory and Register	2.4	IDB Input Data from I/O Group B 1.6	
ORI	OR Memory and Register Immediate	1.6	IDC Input Data from I/O Group C 1.6	
ORS	OR Memory and Register Short Displaced	1.867	IDO Input Data from I/O Group D 1.6	
ORR	OR Register and Register	0.8	ISA Input Status from I/O Group A 1.6	
ORRB	OR Register and Register and Branch if Nonzero	1.6	ISB Input Status from I/O Group B 1.6	
TERB	Test Register and Register and Branch if Any Ones Compare	1.6	ISC Input Status from I/O Group C 1.6	
XOM	Exclusive OR Memory and Register	2.4	ISD Input Status from I/O Group D 1.6	
XOI	Exclusive OR Memory and Register Immediate	1.6	OCA Output Command to I/O Group A 1.067	
XOS	Exclusive OR Memory and Register Short Displaced	1.867	OCB Output Command to I/O Group B 1.067	
XOR	Exclusive OR Register and Register	0.8	OCC Output Command to I/O Group C 1.067	
XORB	Exclusive OR Register and Register and Branch if Nonzero	1.6	OCD Output Command to I/O Group D 1.067	
ZRR	Zero Register	0.8	ODA Output Data to I/O Group A 1.067	
			ODB Output Data to I/O Group B 1.067	
			ODC Output Data to I/O Group C 1.067	
			ODD Output Data to I/O Group D 1.067	

# MODCOMP II

## General-Purpose 16-Bit Computer



## Features

The MODCOMP II computer is the intermediate member of the compatible MODCOMP computer family. It has the large instruction set, 15 general registers, and other features which enable it to use the higher-level software developed and proven with MODCOMP III computers. In price and size, it is much closer to the MODCOMP I, which is the smallest family member.

The MODCOMP II is available in two enclosure sizes and several different models. The photograph on the right shows the largest hardware configuration.

## Software Features

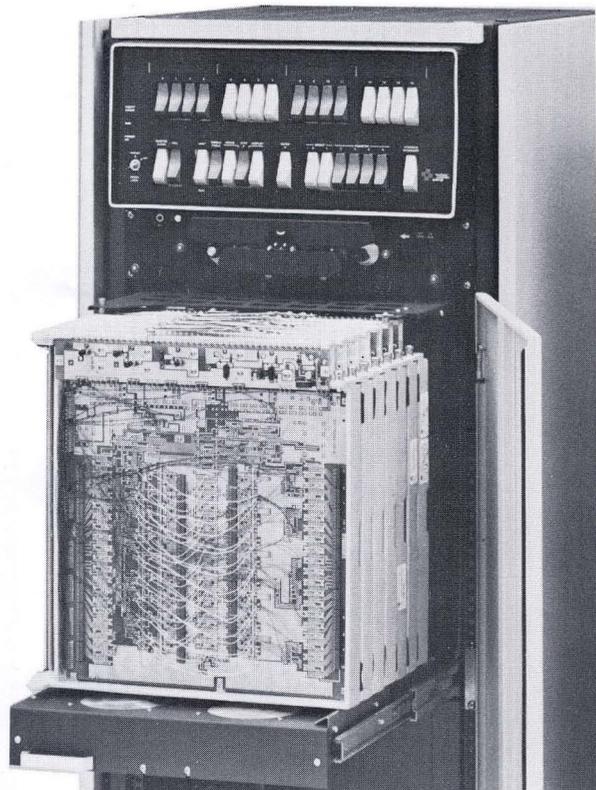
MODCOMP II computers offer higher-level software previously available only with more expensive 16 and 32 bit computers. This software consists of three Modular Application Executives:

- MAX I — A basic program-development executive
- MAX II — A disc operating system for general-purpose batch-processing applications
- MAX III — The most advanced real-time executive available. MAX III offers a versatile set of task scheduling, input/output handling, and resource allocation services. Tasks may be executed in foreground, middleground, or background environments.

The available language processors include:

- FORTRAN IV — Available in three versions optimized for different applications
- Macro Assembler — Assembler and compiler language can be mixed or used separately
- Cross Assembler — For IBM 360/370 and CDC 6000 computers
- BASIC — For interactive, multi-terminal applications

MODCOMP II software enables the user to choose the programming language and executive which best fit his needs. Real-time as well as scientific jobs can be programmed most easily in MODCOMP FORTRAN, and MODCOMP assembly language remains the best approach for producing tightly-coded tasks.



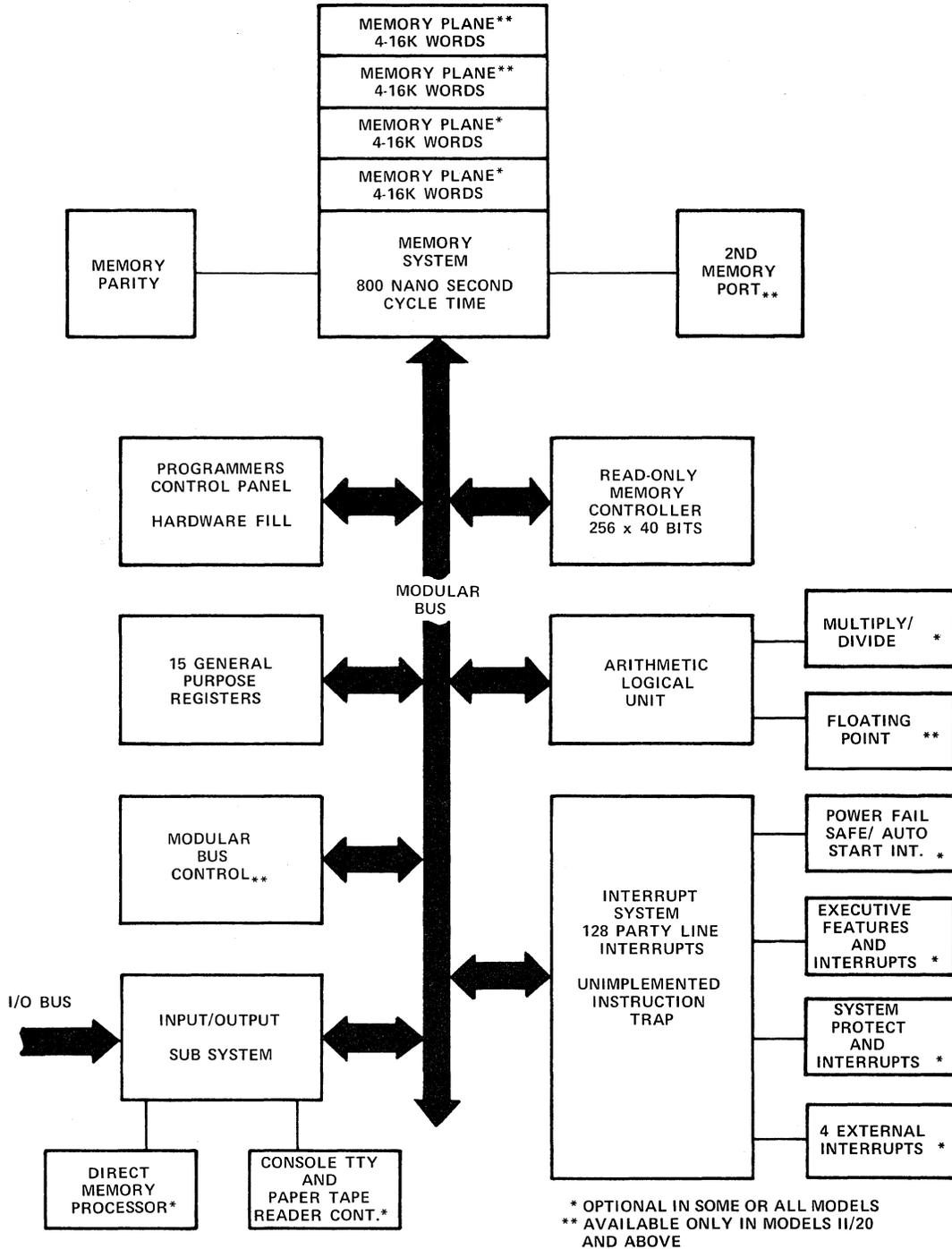
MODCOMP II/20 computer. The vertically hinged planes shown can contain 64K words of multiport core memory, floating point hardware, and all other CPU options.

## Hardware Features

This Technical Bulletin describes the MODCOMP II hardware features. The MODCOMP II offers:

- 4K-64K Words of Memory
- All Memory Directly Addressable
- 800 Nanosecond Cycle Time
- Memory Protect and Parity
- Seven Memory Addressing Modes
- Multi-Port Memory
- 15 General Purpose Registers
- Bit, Byte, Word, Double Word and File Manipulation
- Fixed and Floating Point Arithmetic Hardware
- 174 Microprogrammed Instructions
- 16 Priority Interrupt Levels
- 128 Vectored Sub Levels
- Eight Direct Memory Channels

# MODCOMP II Organization



**MODCOMP II Block Diagram**

The MODCOMP II block diagram shows the basic organization of the computer. All major system elements are connected to the Modular Bus structure, which is the 16-bit parallel path used for all data transfers within the computer.

Data transfers and processing are controlled by the execu-

tion of 40-bit microinstructions stored in the Read Only Control Memory. A new microinstruction is accessed and executed each 267 nanoseconds. Therefore three microinstructions are executed per 800-nanosecond main memory cycle. This rate enables many instructions, such as register-to-register operations, to be accessed from core memory and executed in a single memory cycle.

## Core Memory

Core memory is available in increments of 4K, 8K, or 16K word modules in configurations up to 64K words. The basic features of the core memory are:

- Cycle Time — 800 nanoseconds.
- Parity — Parity is available in all MODCOMP II computers.
- Protect — Three registers are provided which establish protect boundaries in memory. A program stored between two of these boundaries cannot write into any location outside the boundaries. Instructions are provided to load the protect registers. The third register establishes the lower boundary for protected COMMON in high memory.
- Four Port Memory — Three additional access paths to memory are available. These paths, which operate at a cycle time of one  $\mu$  sec, can be used for multiprocessor configurations or non-cycle stealing, direct-memory input/output transfers.

## Memory Addressing

**Word Addressing** — All memory is directly addressable in the MODCOMP II computer. The restrictions of page addressing, found in many other machines, have been eliminated to permit many tasks, separately assembled or compiled, to reside anywhere in memory without conflict or restriction.

Seven memory addressing modes are provided in memory reference instructions:

- Direct
- Indirect
- Indexed
- Indexed and Indirect
- Immediate
- Short Displaced
- Short Indexed

This wide choice of addressing modes permits unmatched optimization both in assembler and compiler generated code.

**Double Word and File Addressing** — Both double-words and files up to eight words in length can be accessed or replaced in memory by individual instruction execution.

**Byte Addressing** — A set of byte instructions is provided which enables lists of bytes stored in memory to be individually accessed or replaced.

**Bit Addressing** — In the extensive set of bit manipulation instructions, any bit in memory or in any general register can be individually addressed.

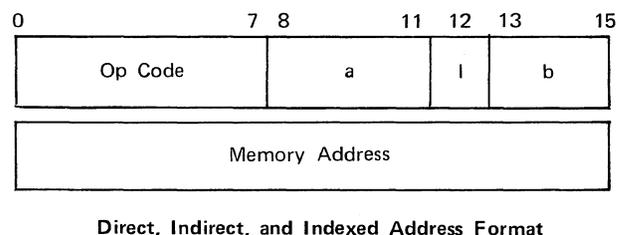
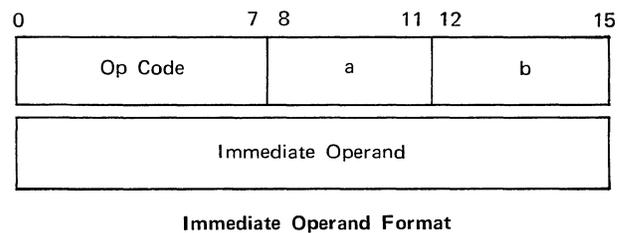
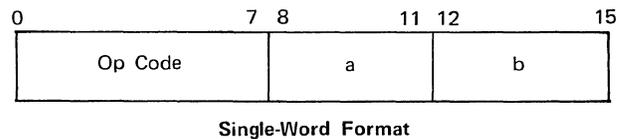
## Register File

MODCOMP II has 15 general registers addressable in most instructions. All of these registers are high-speed flip-flop registers. In addition, a sixteenth addressable register  $R_0$

(the control panel switch register) is provided for direct operator communication with the program. Seven of the high-speed general registers ( $R_1 - R_7$ ) may be used as index registers. The large register file makes the MODCOMP II very capable of handling high speed computation as well as communications and control applications. For many problems, all operands can be held in the high speed registers and operated on by the high speed register-to-register instruction set.

## Instruction Set

The principal MODCOMP instruction formats are:



where a and b define operand register, index register, bit address within a word, displacement address (up to 16 locations) with respect to a base address, shift count, interrupt level or peripheral device address; and l specifies indirect addressing.

All register-to-register, shift, input/output, and control instructions use the single-word format. Many memory reference instructions also use this format and obtain a 16-bit operand address by the short displaced, short indexed, or immediate addressing technique. The short displaced technique is ideal for processing lists of up to 16 operands stored in adjacent locations anywhere in memory. The base address is loaded into general register one ( $R_1$ ) and then the displacement with respect to the base address is contained in the b field of the instruction word. The short indexed mode is ideal for applications in which the operand address requires generation, loading, or manipulation in a general register. The b field specifies the register which contains the operand address in this addressing mode.

In the immediate mode, the operand is contained in the memory location following the instruction location.

In the third format shown, the second word contains either the direct operand address or the indirect address, if I = 1. The b field in the instruction word specifies any of seven index registers with b = 0 designating no indexing.

Use of eight bits for the operation code enables MODCOMP II to have an instruction set which matches that of many 32-bit computers. In particular, the bit manipulation, byte manipulation, register-to-register, register-to-memory, file transfer, test and conditional branch, and interrupt control instruction groups are much more complete than those in almost any other 16-bit computer. And the execution times match the fast memory cycle time.

**MODCOMP II INSTRUCTION LIST**

<u>MNEMONIC</u>	<u>NAME</u>	<u>EXECUTION TIME (μs)</u>
<b><u>LOAD, STORE AND TRANSFER</u></b>		
LDM	Load Register from Memory	2.4
LDI	Load Register from Memory Immediate	1.6
LDS	Load Register from Memory Short Displaced	1.87
LDX	Load Register from Memory Short Indexed	1.87
STM	Store Register in Memory	2.4
STI	Store Register in Memory Immediate	1.6
STS	Store Register in Memory Short Displaced	1.87
STX	Store Register in Memory Short Indexed	1.87
LBX	Load Byte From Memory	2.13
SBX	Store Byte in Memory	2.4
LFM	Load File from Memory	2.93 + .8 (R-1)
LFS	Load File from Memory Short Displaced	2.4 + .8 (R-1)
LFX	Load File from Memory Short Indexed	2.4 + .8 (R-1)
SFM	Store File in Memory	1.87 + .8 (R-1)
SFS	Store File in Memory Short Displaced	1.87 + .8 (R-1)
SFX	Store File in Memory Short Indexed	1.87 + .8 (R-1)
TRR	Transfer Register to Register	0.8
TRRB	Transfer Register to Register and Branch if Nonzero	1.6
<b><u>ARITHMETIC</u></b>		
ADM	Add Memory to Register	2.4
ADI	Add Memory to Register Immediate	1.6
ADS	Add Memory to Register Short Displaced	1.87
ADX	Add Memory to Register Short Indexed	1.87
ADMM	Add Register to Memory	3.47
ADMB	Add Register to Memory and Branch if Nonzero	4.27
ADSM	Add Register to Memory Short Displaced	2.93
ADSB	Add Register to Memory Short Displaced and Branch if Nonzero	3.83
ADXM	Add Register to Memory Short Indexed	2.93
ADXB	Add Register to Memory Short Indexed and Branch if Nonzero	3.83
ADR	Add Register to Register	0.8
ADRB	Add Register to Register and Branch if Nonzero	1.6

<u>MNEMONIC</u>	<u>NAME</u>	<u>EXECUTION TIME (μs)</u>
DAR	Double Precision Add Register to Register	1.6
SUM	Subtract Memory from Register	2.4
SUI	Subtract Memory from Register Immediate	1.6
SUS	Subtract Memory from Register Short Displaced	1.87
SUX	Subtract Memory from Register Short Indexed	1.87
SUR	Subtract Register from Register	0.8
SURB	Subtract Register from Register and Branch if Nonzero	1.6
MPM	Multiply Memory by Register	7.2
MPS	Multiply Memory by Register Short Displaced	6.67
MPX	Multiply Memory by Register Short Indexed	6.67
MPR	Multiply Register by Register	6.13
DVM	Divide Register by Memory	9.87
DVS	Divide Register by Memory Short Displaced	9.33
DVX	Divide Register by Memory Short Indexed	9.33
DVR	Divide Register by Register	8.8
CRMB	Compare Memory and Register	4.8
CRSB	Compare Memory and Register Short Displaced	4.27
CRXB	Compare Memory and Register Short Indexed	4.27
TRO	Transfer and Reset Overflow Status	0.8
TTR	Transfer Two's Complement Register to Register	0.8
TTRB	Transfer Two's Complement Register to Register and Branch if Nonzero	1.6
<b><u>LOGICAL</u></b>		
ETM	Extract Memory from Register	2.4
ETI	Extract Memory from Register Immediate	1.6
ETS	Extract Memory from Register Short Displaced	1.87
ETX	Extract Memory from Register Short Indexed	1.87
ETMM	Extract Register from Memory	3.47
ETMB	Extract Register from Memory and Branch if Nonzero	4.27
ETSM	Extract Register from Memory Short Displaced	2.67
ETSB	Extract Register from Memory Short Displaced and Branch if Nonzero	3.47
ETXM	Extract Register from Memory Short Indexed	2.67
ETXB	Extract Register from Memory Short Indexed and Branch if Nonzero	3.47
ETR	Extract Register from Register	0.8
ETRB	Extract Register from Register and Branch if Nonzero	1.6
ORM	OR Memory and Register	2.4
ORI	OR Memory and Register Immediate	1.6
ORS	OR Memory and Register Short Displaced	1.87
ORX	OR Memory and Register Short Indexed	1.87
ORMM	OR Register and Memory	3.47
ORSM	OR Register and Memory Short Displaced	2.67
ORXM	OR Register and Memory Short Indexed	2.67
ORR	OR Register and Register	0.8
ORRB	OR Register and Register and Branch if Nonzero	1.6



<u>MNEMONIC</u>	<u>NAME</u>	<u>EXECUTION TIME (us)</u>
<b>INTERRUPT AND CALL</b>		
SIE	Set Interrupt Enable	1.33
RIE	Reset Interrupt Enable	1.33
SIR	Set Interrupt Request	1.33
RIR	Reset Interrupt Request	1.33
SIA	Set Interrupt Active	1.33
RIA	Reset Interrupt Active	1.33
REX	Request Executive Service	0.8
RMI	Request Multiprocessor Interrupt	0.8
CAR	Clear Active and Return	1.87
CIR	Clear Interrupt and Return	1.87
<b>INPUT/OUTPUT</b>		
ISA,B,C,D	Input Status from I/O Group A,B,C,& D	1.6
IDA,B,C,D	Input Data from I/O Group A,B,C & D	1.6
OCA,B,C,D	Output Command to I/O Group A,B,C & D	1.33
ODA,B,C,D	Output Data to I/O Group A,B,C & D	1.33

## Input/Output

Two types of input/output capabilities are available in MODCOMP II, to meet the requirements of most applications.

**Register Input/Output** — The basic I/O structure in MODCOMP computers consists of a party-line bus capable of transferring words or characters between any of 64 peripheral devices and any of the 15 general registers. Transfers can be timed either by peripheral device interrupts or by program testing of device status.

The party-line bus is ideally suited both for real-time applications and peripheral devices which are asynchronous and moderate in speed. A word or character is transferred over the bus by execution of a single instruction which contains all of the necessary information:

1. The device number (1 of 64)
2. The general register address
3. The direction of transfer
4. The type of information — data in or out, command out or status in

Immediately after execution of an I/O instruction in 1.33 microseconds (output) or 1.6 microseconds (input), a new I/O instruction can be executed, specifying a different device and all other transfer parameters. Therefore transfer routines for many different devices can be performed at the same time on an independent, interrupt-driven basis.

**Direct Memory Processor** — The DMP option consists of eight automatic, multiplexed transfer channels. It enables up to eight blocks of words to be transferred between memory and peripheral devices or measurement, control and communication sub-systems. The capability for automatic data chaining is also provided.

Transfers are made over the standard party line bus but have higher priority than program controlled transfers. The DMP automatically steals cycles from the program whenever word transfers are requested by active peripheral devices connected to the DMP channels.

All eight of the DMP channels contain a pair of 16-bit registers which hold the memory address for the next transfer and the number of words remaining to be transferred in the current block. These channels can transfer words at combined rates up to 412K (input) or 375K (output) words per second.

**External Direct Memory Processor** — In multipoint memory configurations, an external DMP can be connected to a separate memory port, providing 625K words per second transfer capability on a non-cycle-stealing basis. The external DMP is also connected to the I/O bus to provide program compatibility with the internal DMP.

## Interrupts

The MODCOMP II Priority Interrupt System contains three standard interrupt levels and is expandable to a total of 16 interrupt levels. In addition, two of the three standard levels can each have up to 64 priority sub-levels. The maximum number of priority levels and sub-levels is 142. Each level is assigned a pair of memory locations, one for the entry address of the interrupt routine and one for the return address. The return address is stored by the context switching operation which is performed automatically when an interrupt signal occurs and is the highest priority signal in the interrupt queue.

Each level can be selectively enabled and disabled under program control. In addition, two special program control features are provided:

1. Request signals for all levels can be program generated both as a debugging aid and to reduce overhead in monitor operations.
2. The priority queue can be program manipulated by temporarily deferring the processing of interrupts from any level down to the low priority end of the queue.

A specific function is assigned to each of the three standard interrupt levels:

**Unimplemented Instruction Trap** — This standard interrupt occurs if execution of one of the optional instructions is attempted in a computer not having the optional instruction. The interrupt routine can perform the execution by software rather than by hardware. Therefore programs are downward as well as upward compatible between all MODCOMP II and III computers.

**Request Executive Service** — The execution of this instruction always causes the unimplemented instruction trap to be generated. This monitor call feature is used extensively in all Modular Application Executives (MAX I, II, and III).

**Input/Output Interrupt Party Lines** — The two remaining standard interrupt levels are party-line levels connected to all peripheral devices through the I/O cable. Up to 64 devices can be connected to each of these levels. Connec-

tion is performed under program control. Therefore only selected devices are connected to each of these levels at any given time.

One of the two levels is used by each device to request a character or word transfer. The second is used to signify an end-of-record or end-of-transfer condition, if appropriate.

A dedicated memory location is assigned to each sub-level for an interrupt routine entry address. Therefore, when a parity-line interrupt signal occurs, the appropriate interrupt routine is entered automatically. No testing is required to determine which of the possible 64 signals occurred.

### Modular Bus Control

In MODCOMPS II/20 and II/25, all of the computer micro-control lines are brought out to externally available connectors. External processors or user equipment can interrupt internal processing and take over all internal machine resources. This capability enables both new instructions to be implemented by external processors and internal processing capabilities to be used by external equipment.

### Executive Features

This MODCOMP option consists of three additional hardware features, each of which is connected to a separate interrupt level. These features are requirements of the MAX II and III software systems.

**Real Time Clock** — When level 6 is enabled, an interrupt occurs at a 200 Hz rate.

**Console Interrupt** — The Console Interrupt switch on the control panel is connected to level E<sub>16</sub>.

**Task Scheduler** — The real-time executive (MAX III) uses level F<sub>16</sub> to maintain a software task queue below the hardware priority interrupt queue.

### Power Fail Safe/Auto Start

This feature is connected to the highest priority level (O<sub>16</sub>). Anytime the a-c power is turned on or off, the interrupt occurs.

### System Protect

This optional feature includes memory protect and privileged instruction trap capabilities. The protect feature is enabled and disabled by operation of a keyswitch on the control panel. This standard switch also disables the other panel switches, except the data switches.

**Memory Protect** — This System Protect feature enables all of memory, except the user program currently being executed and a common area in upper memory, to be protected against modification or program entry. The program protect status can be modified under program control by changing the contents of two registers — the upper and lower protect registers. These registers have a granularity of 128 words. If a program being executed in the area between these two boundaries attempts to modify or branch into a protected outside memory location, a trap is generated at level 2 and the instruction

execution is aborted. A third register is used to define the lower COMMON boundary. COMMON extends to the upper memory boundary.

**Privileged Instruction Trap** — This feature is an additional safeguard of system integrity. No instruction which affects input/output, interrupts or machine operating states can be executed in unprotected programs. A trap (level 2) is generated if execution of one of the privileged instructions is attempted.

## Physical Characteristics

### Size and Packaging

All MODCOMP II computers are designed for mounting in equipment cabinets which have standard 19 inch rails and are 24 inches or more in depth. Slides are provided for convenient front access to all electronics. The hinged-plane packaging enables all internal circuits to be tested without the use of extenders or any other special equipment.

The integrated circuits are mounted in sockets. This packaging technique minimizes spares requirements and servicing tools, in addition to providing easy access to all test points.

The height of the MODCOMP II/5 and II/10 is 8.75 inches, including the integrally mounted control panel and power supplies.

The MODCOMP II/20 and II/25 plane enclosure is 21 inches in height. This enclosure contains all required power supplies. The control panel can be mounted in front of this enclosure to provide 21 inches of height overall.

The optional high speed paper tape reader is normally mounted directly below the control panel. It is too deep to be mounted directly in front of the computer. Therefore in "stand up operation" configurations, the control panel and paper tape reader are mounted above the plane enclosure, requiring a total of 32.75 inches of vertical rack space. In "sit down operation" configurations, the control panel and reader are both mounted below the plane enclosure to meet human engineering height guidelines. This configuration also requires 32.75 inches in height.

### Weight, Power, and Environmental

A full MODCOMP II/5 or II/10 weighs 70 pounds.  
A full MODCOMP II/20 or II/25 weighs 160 pounds.

The power requirements are 120 VAC  $\pm 10\%$  at 48 to 62 Hz. The power dissipation of a full MODCOMP II/5 or II/10 is 600 watts and 1,800 watts for a full MODCOMP II/20 or II/25.

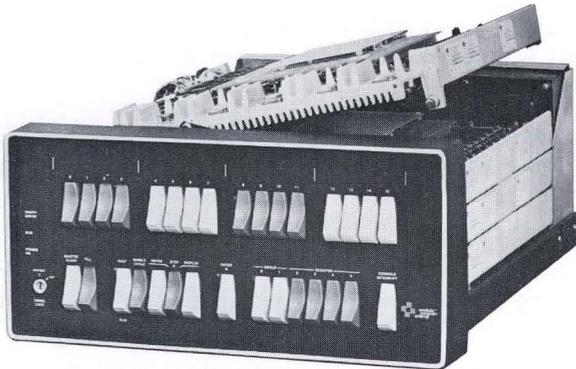
All models are designed for the following ambient environments:

Operating Temperature — 0 to 55°C  
Relative Humidity — 10 to 90%, noncondensing  
Altitude — 6,000 feet without added cooling

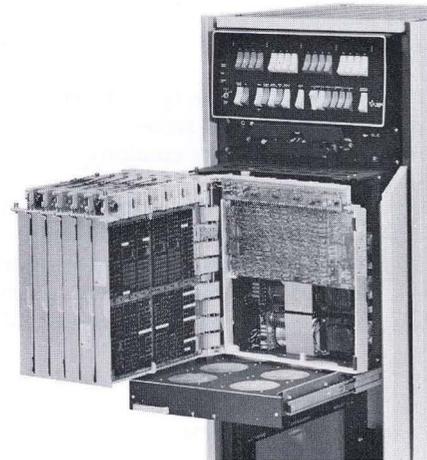
## MODCOMP II Models

The MODCOMP II computer is available in four models — II/5, II/10, II/20, and II/25. The MODCOMP II/5 and II/10 are packaged on either three or four horizontally mounted planes, as shown in the photograph. The CPU and options are packaged on the bottom two planes. Each of the top two planes can contain a 4K, 8K, or 16K memory module. Therefore the memory size range is 4K-32K words.

The addressing range provided for each plane is 16K words. Therefore, to avoid non-contiguous memory addressing, the lower plane should contain a 16K word module before the upper plane is added. For contiguous addressing, the valid memory sizes are: 4K, 8K, 16K, 20K, 24K, and 32K words.



The MODCOMP II models 5 and 10 are packaged in this 8-3/4 inch high rack-mountable enclosure. This enclosure can contain up to 32K words of memory.



The MODCOMP II models 20 and 25 are packaged in this 21 inch high rack-mountable enclosure. This enclosure can contain up to 64K words of memory. The control panel can be mounted in front of as well as above or below the CPU enclosure.

The MODCOMP II/20 and II/25 are packaged on three to nine vertically mounted planes as shown in the photograph. The contents of each plane are:

Plane	Contents
1	Options
2	Options
3	CPU
4	CPU
5	Four Port Memory Access
6-9	Memory Modules

The principal standard features and all optional features of the four models are defined in the table below:

Feature	II/5	II/10	II/20	II/25
15 General Registers	S	S	S	S
Programmers Control Panel	S	S	S	S
Hardware Fill	S	S	S	S
Panel Keyswitch	S	S	S	S
Memory Size (Wds)	4-32K	16-32K	4-64K	16-64K
Memory Parity	O	S	O	S
Standard Interrupt Levels	3	8	3	8
Power Fail Safe/Auto Start	O	S	O	S
Executive Features & Interrupts	O	S	O	S
System Protect & Interrupts	O	O	O	O
External Interrupt Levels Available (In addition to 128 sub-levels)	5	5	5	5
Hardware Multiply / Divide	O	S	O	S
Hardware Floating Point	N	N	O	O
Direct Memory Processor — 8 Channels	O	O	O	O
Modular Bus Control	N	N	S	S
Four Port Memory (1 $\mu$ sec)	N	N	O	O
External Direct Memory Processor — 4 Channels	N	N	O	O
Controller for Console Teletype and High Speed Paper Tape Reader	O	O	S	S

Standard and Optional Features of MODCOMP II Models Legend S — Standard • O — Optional • N — Not Available

# MODCOMP III CP

## Communications Processor



## Features

The MODCOMP III Communications Processor has the same standard features as the general purpose MODCOMP III/5 computer plus a set of powerful communications-oriented macro instructions. The combined features of the MODCOMP III CP enable throughput rates up to 100K bytes per second and burst data rates in excess of 200K bytes per second.

The standard instruction set features bit and byte addressing/processing instructions as well as the more common word oriented instructions. The large instruction repertoire combined with 15 general purpose registers provide fast, efficient processing capabilities.

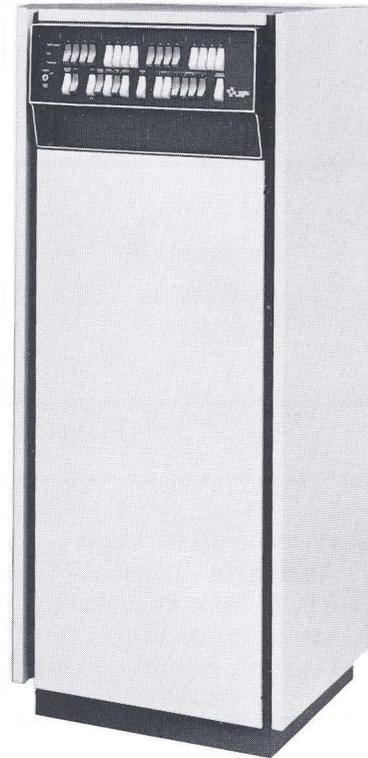
## Software Features

MODCOMP III computers offer higher-level software previously available only with more expensive 16 and 32 bit computers. This software consists of four Modular Application Executives:

- MAX I — A basic program-development executive
- MAX II — A disc operating system for general-purpose batch-processing applications
- MAX III — The most advanced real-time executive available. MAX III offers a versatile set of task scheduling input/output handling, and resource allocation services. Tasks may be executed in foreground, middle-ground, or background environments.
- SAX III — A real-time executive providing control and scheduling of programs in a multiprogramming environment with a minimum of core overhead.

The available language processors include:

- FORTRAN IV — Available in three versions optimized for different applications
- Macro Assembler — Assembler and compiler language can be mixed or used separately
- Cross Assembler — For IBM 360/370 and CDC 6000 computers



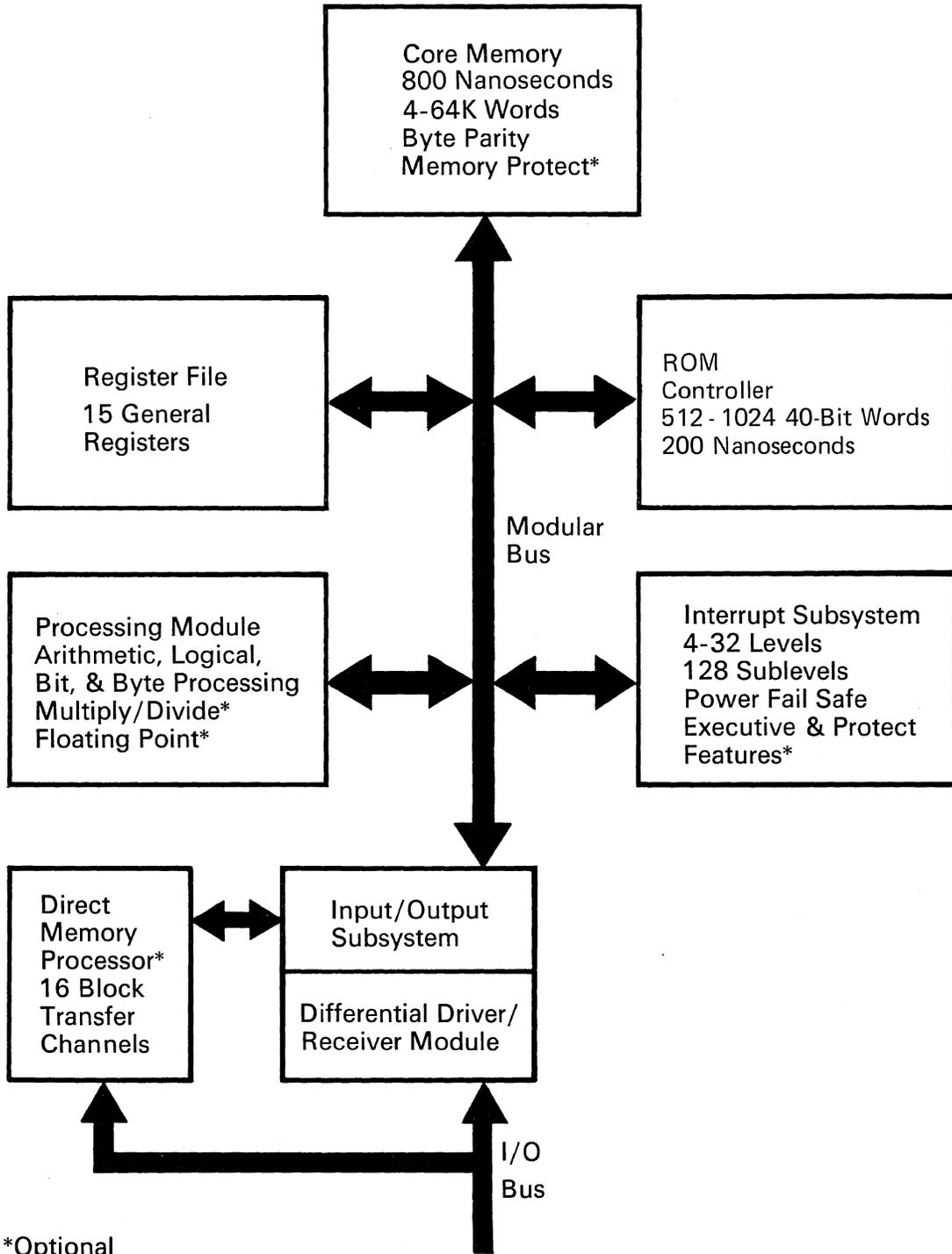
MODCOMP III Computer. The cabinet shown can contain 64K words of memory and all options.

## Hardware Features

This technical Bulletin describes the MODCOMP III CP hardware features. The MODCOMP III CP offers:

- 4K-64K Words of Memory
- All Memory Directly Addressable
- 800 Nanosecond Cycle Time
- Memory Protect and Parity
- Seven Memory Addressing Modes
- 15 General Purpose Registers, 7 Usable as Index Registers
- Bit, Byte, Word, Double Word, and File Manipulation
- Fixed Point Arithmetic Hardware
- 172 Microprogrammed Instructions/Macros
- 32 Priority Interrupt Levels
- Sixteen Direct Memory Channels
- Firmware CRC/LRC Accumulation/Generation
- Move and Compare Byte Macros
- Pack and Unpack Character String Macros

# MODCOMP III Organization



## Core Memory

Core Memory is available in increments of 4K or 8K word modules in configurations up to 64K words. The basic features of the core memory are:

- Cycle Time — 800 nanoseconds
- Parity — Byte Parity is available in all MODCOMP III computers.
- Protect — The protect boundary can be established by program control at any 2K boundary in core. Programs above this boundary are unprotected. An attempt to modify or branch into a protected location from unprotected core causes a trap and execution of the instruction is aborted.

## Memory Addressing

Word Addressing — All memory is directly addressable in the MODCOMP III computer. The restrictions of page addressing, found in many other machines, have been eliminated to permit many tasks, separately assembled or compiled, to reside anywhere in memory without conflict or restriction.

Seven memory addressing modes are provided in memory reference instructions:

- Direct
- Indirect
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This wide choice of addressing modes permits unmatched optimization both in assembler and compiler generated code.

Double Word and File Addressing — Both double-words and files up to eight words in length can be accessed or replaced in memory by individual instruction execution.

Byte Addressing — A set of byte instructions is provided which enables lists of bytes stored in memory to be individually accessed or replaced.

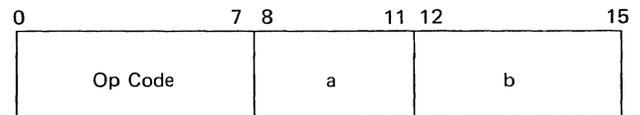
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## Register File

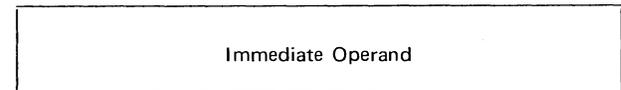
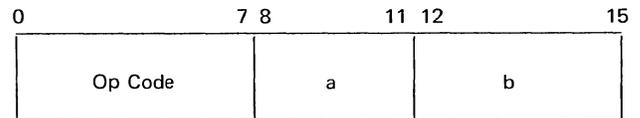
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## Instruction Set

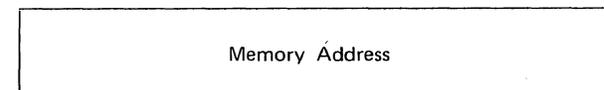
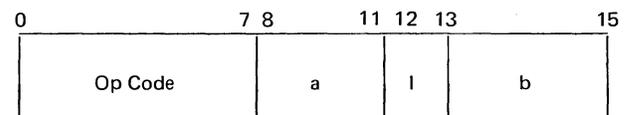
The principal MODCOMP instruction formats are:



Single-Word Format



Immediate Operand Format



Direct, Indirect, and Indexed Address Format

where a and b define operand register, index register, bit address within a word, displacement address (up to 16 locations) with respect to a base address, shift count, interrupt level or peripheral device address; and l specifies indirect addressing.

All register-to-register, shift, input/output, and control instructions use the single-word format. Many memory reference instructions also use this format and obtain a 16-bit operand address by the short displaced, short indexed, or immediate addressing technique. The short displaced technique is ideal for processing lists of up to 16 operands stored in adjacent locations anywhere in memory. The base address is loaded into general register one ( $R_1$ ) and then the displacement with respect to the base address is contained in the b field of the instruction word. The short indexed mode is ideal for applications in which the operand address requires generation, loading, or manipulation in a general register. The b field specifies the register which contains the operand address in this addressing mode.

In the immediate mode, the operand is contained in the memory location following the instruction location.

In the third format shown, the second word contains either the direct operand address or the indirect address, if  $l = 1$ . The b field in the instruction word specifies any of seven index registers with  $b = 0$  designating no indexing.

Use of eight bits for the operation enables MODCOMP III to have an instruction set which matches that of many 32-bit computers including bit, byte, word, doubleword, and file manipulation capabilities.

# Typical Instructions

<u>MNEMONIC</u>	<u>NAME</u>	<u>EXECUTION TIME (μs)</u>
<u>LOAD, STORE AND TRANSFER</u> 20 INSTRUCTIONS		
LDM	LOAD Register from Memory	2.4
LDX	Load Register from Memory Short Indexed	1.6
STX	Store Register in Memory Short Indexed	1.6
LBX	Load Byte from Memory	2.0
SBX	Store Byte in Memory	2.6
LFX	Load File from Memory Short Indexed (1 to 8 Registers)	2.2+ .8xR
SFX	Store File in Memory Short Indexed (1 to 8 Registers)	1.8+ .8xR
TRR	Transfer Register to Register	.8
TRRB	Transfer Register to Register and Branch if Nonzero	1.6
<u>ARITHMETIC</u> 33 INSTRUCTIONS		
ADM	Add Memory to Register	2.4
ADI	Add Memory to Register Immediate	1.6
ADM	Add Register to Memory and Branch if Nonzero	3.4
ADR	Add Register to Register	0.8
ADRB	Add Register to Register and Branch if Nonzero	1.6
DAR	Double Precision Add Register to Register	1.8
SUM	Subtract Memory from Register	2.4
SUR	Subtract Register from Register	0.8
SURB	Subtract Register from Register and Branch if Nonzero	1.6
MPX	Multiply Memory by Register Short Indexed	6.4
MPR	Multiply Register by Register	6.0
DVM	Divide Register by Memory	12.2
DVR	Divide Register by Register	11.0
CRMB	Compare Memory and Register	4.0
TTR	Transfer Two's Complement Register to Register	0.8
<u>LOGICAL</u> 32 INSTRUCTIONS		
ETMM	Extract Register from Memory (AND)	3.4
ETR	Extract Register from Register	0.8
ORM	OR Memory and Register	2.4
ORX	OR Memory and Register Short Indexed	1.6
ORR	OR Register and Register	0.8
ORRB	OR Register and Register and Branch if Nonzero	1.6
XOM	Exclusive OR Memory and Register	2.4
XOX	Exclusive OR Memory and Register Short Indexed	1.6
XOR	Exclusive OR Register and Register	0.8
XORB	Exclusive OR Register and Register and Branch if Nonzero	1.6
TOR	Transfer One's Complement to Register	0.8
TRXB	Test Register and Memory and Branch if Any Ones Compare	2.6
TERB	Test Register and Register and Branch if Any Ones Compare	1.6
<u>SHIFT</u> 9 INSTRUCTIONS		
LAD	Shift Left Arithmetic Double	2.2+4 (S-1)
RAD	Shift Right Arithmetic Double	1.8+4 (S-1)
LLS	Shift Left Logical Single	2.4+0.2(S-1)
LRS	Left Rotate Single	0.8
<u>BIT MANIPULATION</u> 34 INSTRUCTIONS		
LBR	Load Bit in Register	0.8
ADDM	Add Bit in Memory	3.4
ABR	Add Bit in Register	0.8
SBR	Subtract Bit in Register	0.8

<u>MNEMONIC</u>	<u>NAME</u>	<u>EXECUTION TIME (μs)</u>
ZBMM	Zero Bit in Memory	3.4
OBMM	OR Bit in Memory	3.4
XBR	Exclusive OR Bit in Register	.8
TBXB	Test Bit in Memory and Branch if One	2.6
CBMB	Compare Bit and Memory	4.0
<u>BYTE MANIPULATION</u>		5 INSTRUCTIONS
MUR	Move Upper Byte Register to Register	0.8
MLR	Move Lower Byte Register to Register	0.8
IBR	Interchange Bytes Register to Register	0.8
<u>UNCONDITIONAL BRANCH</u>		5 INSTRUCTIONS
BLM	Branch and Link	1.6
BRU	Branch Unconditionally	1.6
BRX	Branch Short Indexed	0.8
<u>CONTROL</u>		3 INSTRUCTIONS
HLT	HALT	—
SPR	Set Protect Register	0.8
<u>INTERRUPT AND CALL</u>		10 INSTRUCTIONS
SIE	Set Interrupt Enable	1.2
SIA	Set Interrupt Active	1.2
REX	Request Executive Service	0.8
CIR	Clear Interrupt and Return	1.8
<u>INPUT/OUTPUT</u>		16 INSTRUCTIONS
ISA	Interrupt Status from I/O Group A	2.0
IDA	Input Data From I/O Group A	2.0
OCA	Output Command to I/O Group A	1.2
ODA	Output Data to I/O Group A	1.2

## Input/Output

Two types of input/output capabilities are available in the MODCOMP III, to meet the requirements of most applications.

**Register Input/Output** — The basic I/O structure in MODCOMP computers consists of a party-line bus capable of transferring words or characters between any of 64 peripheral devices and any of the 15 general registers. Transfers can be timed either by peripheral device interrupts or by program testing of device status.

The party-line bus is ideally suited both for real-time applications and peripheral devices which are asynchronous and moderate in speed. A word or character is transferred over the bus by execution of a single instruction which contains all of the necessary information:

1. The device number (1 of 64)
2. The general register address
3. The direction of transfer
4. The type of information — data in or out, command out or status in

Immediately after execution of an I/O instruction a new I/O instruction can be executed, specifying a different device and all other transfer parameters. Therefore transfer routines for many different devices can be performed

at the same time on an independent, interrupt-driven basis.

**Direct Memory Processor** — The DMP option consists of sixteen automatic multiplexed transfer channels. It enables up to sixteen blocks of words to be transferred between memory and peripheral devices or measurement, control and communication subsystems. The capability for automatic data chaining is also provided.

Transfers are made over the standard party line bus but have higher priority than program controlled transfers. The DMP automatically steals cycles from the program whenever word transfers are requested by active peripheral devices connected to the DMP channels.

## Interrupts

The MODCOMP III Priority Interrupt System consists of three standard interrupt levels and is expandable to a total of 32 interrupt levels. In addition, two of the four standard levels can each have up to 64 priority sub-levels. Each level is assigned a pair of memory locations, one for the entry address of the interrupt routine and one for the return address. The return address is stored by the context switching operation which is performed automatically when an interrupt signal occurs and is the highest priority signal in the interrupt queue.

Each of the 64 sub-levels associated with each level has a unique priority. A dedicated memory location is assigned to each sub-level for an interrupt routine entry address. Therefore, when a party-line interrupt signal occurs, the appropriate interrupt routine is entered automatically. No testing is required to determine which of the possible 64 signals occurred.

Each level can be selectively enabled and disabled under program control. In addition, two special program control features are provided:

**Unimplemented Instruction Trap** — This standard interrupt occurs if execution of one of the optional instructions is attempted in a computer not having the optional instruction.

**Request Executive Service** — The execution of this instruction always causes the unimplemented instruction trap to be generated.

## Executive Features

**Real Time Clock** — When level 6 is enabled, an interrupt occurs at a 120 Hz rate, derived from the A-C power frequency.

**Console Interrupt** — A momentary-action switch on the control panel is connected to level E<sub>16</sub> to provide a convenient means for an operator to interrupt the computer without halting it.

**Task Scheduler** — The real-time executive (MAX III) uses this level to maintain a software task queue below the hardware priority interrupt queue.

## System Protect

This optional feature includes memory protect and privileged instruction trap capabilities. The protect feature is enabled and disabled by operation of a keyswitch on the control panel. This switch also disables the other panel switches, except the data switches.

**Memory Protect** — This feature is available to enable part of memory to be protected from modification or entry by programs in unprotected memory. The resident executive and real-time tasks can be protected from modification by undebugged programs which are brought into core for execution. The protect boundary can be established by program control at any 2K boundary in core. Programs above this boundary are unprotected. If an unprotected program attempts to modify or branch into a protected location, a trap is generated at level 2 and the execution of the instruction is aborted.

**Privileged Instruction Trap** — This feature is an additional safeguard of system integrity. No instruction which affects input/output, interrupts or machine operating states can be executed in unprotected programs. A trap (level 2) is generated if execution of one of the privileged instructions is attempted.

## Communication Macro Instructions

The most significant features of the MODCOMP III CP are the special macro instructions which are provided to aid in the processing of communications data. The instructions enable formatting of message blocks to meet full Binary-Synchronous protocol as well as almost any subset thereof. The instructions also provide fast, efficient means of searching character strings and moving blocks of data from core to core.

All macro instructions are executed in a maximum of 5 us. The program, through use of the macro control word, can cause any or all of the following functions to be performed on data streams.

- Search for and discard from a character string or message any desired character specified by program.
- Generate and accumulate CRC<sub>16</sub> or LRC check characters for a block of data.
- Compare each character against an array of up to 8 characters or masks.
- Automatically branch to the appropriate subroutine upon mask compare.
- Check block size of message or data stream to insure a limit on the block size.
- Move each byte, from one place in memory to another.
- Pack or unpack as data is moved, (e.g. one byte/word → two bytes/word, two bytes/word → one byte/word).

Each of the above functions is performed only as specified by the control word. Regardless of how many functions

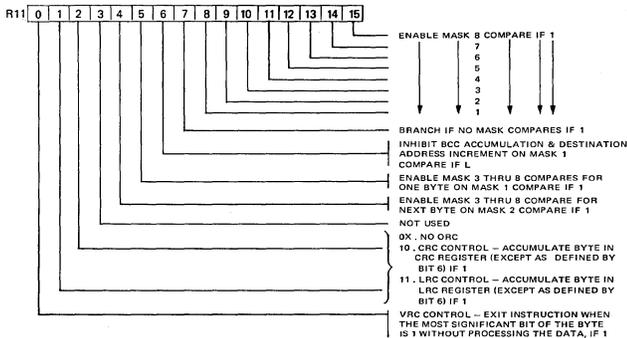
**MOVE BYTE INSTRUCTION FORMAT**

LOCATION	CONTENTS
P	MACRO OPCODE (5000 <sub>16</sub> )
P+1	BRANCH ADD. MASK 8 COMPARE
P+2	" " " & "
P+3	" " " 6 "
P+4	" " " 5 "
P+5	" " " 4 "
P+6	" " " 3 "
P+7	" " " 2 "
P+8	" " " 1 "
P+9	" " " BUFFER LIMIT = 0
P+10	" " " PARITY ERROR (VRC)
P+11	" " " NO COMPARE
P+12	P (LOOP BACK)

**REGISTER FORMAT (Registers 8 thru 15)**

R8	SOURCE WORD ADDRESS 0-32K INCREMENTED AUTOMATICALLY	B	0=MOST SIGNIFICANT BYTE 1=LEAST SIGNIFICANT BYTE
R9	DESTINATION WORD ADDRESS 0-32K	B	0=MOST SIGNIFICANT BYTE 1=LEAST SIGNIFICANT BYTE
R10	BLOCK LIMIT COUNT DECREMENTED AUTOMATICALLY		CAUSES EXIT THRU P+10 WHEN COUNT GOES TO 0
R11	CONTROL WORD		SEE BELOW
R12	MASK 1	MASK 2	MASK AGAINST WHICH EACH BYTE IS COMPARED, IF ENABLED, EXIT THRU DEFINED LOCATIONS OCCURS
R13	" 3	" 4	
R14	" 5	" 6	
R15	" 7	" 8	

**CONTROL WORD FORMAT - USE BYTE FILE INSTRUCTION**



are performed, execution will occur in a maximum of 5  $\mu$ s per character processed.

The macro instructions are:

INSTRUCTION	OPCODE	EXECUTION TIME
MOVE BYTE	5000	5.0 $\mu$ s
MOVE BYTE & UNPACK	5200	5.0 $\mu$ s
MOVE BYTE & PACK	5400	4.4 $\mu$ s
READ LRC/CRC	56R0	1.6 $\mu$ s
LOAD LRC/CRC	57R0	1.6 $\mu$ s

**Operation**

When the move byte instruction is executed, the following sequence occurs:

- Fetch Byte from location specified by R8
- Store Byte in location specified by R9
- Perform comparisons and accumulations specified by R11
- Increment R8
- Conditionally Increment R9
- Conditionally Decrement R10

- Conditionally branch according to the following:  
 IF VRC ERROR, BRANCH to (P+9)  
 IF BLOCK LIMIT = 0, BRANCH to (P+10)  
 IF BYTE = MASK 1 thru 8 RESPECTIVELY, BRANCH to (P+1) thru (P+8)  
 IF NONE OF THE ABOVE, LOOP

As long as no exception conditions occur, the instruction will loop on itself until the block limit goes to 0. Therefore, a file will be relocated at a 200KC rate.

An interrupt window occurs after the transfer of each byte. All current context information is stored in the upper register file, leaving R1 thru R7 available for interrupt processing.

The instruction and register formats for the MOVE BYTE and PACK/UNPACK are the same except for the opcodes which are 5400 and 5200, respectively. All of the same functions can be performed as defined in the MOVE BYTE.

The READ and LOAD CRC/LRC macros are short format instructions. The register (R) specified in the instructions may be any of the general registers. The instruction is used to read or load the firmware register which is used to accumulate the check characters.

**Summary**

The combined features of the standard MODCOMP instruction repertoire and the communication macros provide an exceptionally powerful central processor for large communication applications. When the central processor features are used in conjunction with the highly flexible MODCOMP Universal Communications Subsystem, networks consisting of almost any mix of synchronous or asynchronous devices can be easily accommodated.

The MODCOMP III CP is particularly adaptable to front-end preprocessors and large mixed terminal message switching systems. The MODCOMP III CP has proven its capabilities in the field both from a reliability and performance standpoint.

**Physical Characteristics**

All MODCOMP computers are designed for mounting in equipment cabinets which have standard 19-inch rails and are 30 inches or more in depth. Slides are provided for convenient front access to the electronics. The hinged-plane packaging enables circuits to be tested without the use of extenders or any special equipment.

The integrated circuits are mounted in sockets. This packaging technique minimizes spares requirements and servicing tools, in addition to providing easy access to all test points.

The MODCOMP III CP with all power supplies and memory expansion to 64K is housed in a standard computer system cabinet. The dimensions are 25-1/2" x 30-1/4" x 62-1/2". The total weight is 450 pounds.

Power consumption is 1200 watts at 120 VAC  $\pm$ 10%, 60 $\pm$ 2 Hz.

The MODCOMP III CP operates over the temperature range of 0-55°C (32-131°F) with a relative humidity range of 10% - 90%, non-condensing.

# MODCOMP I Software



## Features

The MODCOMP I software is designed to provide the user with a convenient means for program preparation and execution. The available utilities and executive systems allow the assembly language user to operate in a stand-alone environment or to use larger machines such as the MODCOMP II, III and IBM 360/370 for program preparation.

The software packages available include:

- Assembler
- Extended Assembler
- Modcomp II/III Cross-Assembler
- IBM 360-370 Cross-Assembler
- Relocating Loader
- Link Loader
- Link Editor
- Source Update Program
- MIN I Executive
- SAX I Multiprogramming Executive

### Assembler

The assembler requires 2K words of memory and an ASR-33 input/output device. It accepts source input from the paper tape reader and generates binary output to the paper tape punch and listing output to the keyboard printer. The binary output is in absolute format.

### Extended Assembler

The extended assembler is a superset of the assembler. It requires a minimum of 4K words of memory and an ASR-33. In addition, it is capable of utilizing other peripherals such as card reader, line printer and high speed paper tape reader and punch. Binary output may be either absolute or relocatable.

### MODCOMP II/III Cross-Assembler

The MODCOMP II/III Cross-assembler operates in any MODCOMP II or III system operating under the Max II or III operating systems. It generates object code which can be loaded and executed in the MODCOMP I, II or III central processors.

### IBM 360/370 Cross-Assembler

The IBM 360/370 Cross-assembler is a FORTRAN coded assembler which operates on an IBM 360/370 system operating under DOS or OS.

This assembler is compatible with the MODCOMP assembler in both source language and object output.

### Relocating Loader

The relocating loader loads into memory the relocatable output of the extended assembler. It also provides diagnostic messages in case of load errors.

### Link Loader

The link loader provides the user with the capability of linking and loading program segments which have been assembled separately. When all segments and external names have been satisfied, a memory map is generated on the keyboard/printer. Diagnostic messages are provided for unsatisfied external names.

### Link Editor

The link editor allows the user to link program segments assembled separately and to generate a link-edited relocatable paper tape. Memory maps and diagnostic messages are identical to those provided by the link loader.

### Source Update Program

The source update program allows the user to modify source programs by adding, replacing, copying, listing, or deleting source lines. Updated source listings are printed on the listing device. Supported peripherals include the ASR-33 Teletypewriter, card reader, line printer and high speed paper tape reader/punch.

### MIN I Executive

The MIN I Executive provides the user with capabilities to load, execute and debug application programs written in assembly language. In addition, the extended assembler,

link loader and link editor execute under control of the Min I Executive. Supported peripherals include the ASR-33 Teletypewriter, card reader, line printer and high speed paper tape reader and punch.

I/O handlers for the above peripherals are provided as well as a comprehensive set of operator commands to control program execution.

The MIN I I/O system is device independent, allowing symbolic file output to the three standard files: symbolic input (SI), listing output (LO) and binary output (BO). Device assignment to the three files is done when the system is initialized (SYSGEN time).

A set of operator directives is provided for program preparation and execution. All directives are entered through the console typer and perform the following functions:

**LOAD** — loads a relocatable program from the paper tape reader at the first unused location above the executive or at any specified address.

**PAUSE** — inserts a pause at any specified address.

**GO** — branches to the first instruction of a loaded program or to any specified memory address.

**DISPLAY** — displays the contents on the listing output device (LO) of any register or memory block.

**MODIFY** — modifies the contents of any register or memory block.

## **SAX I Multiprogramming Executive**

The MODCOMP I Special Application Executive (SAX I) is a real-time system designed to control and schedule the execution of user written tasks in a multiprogramming environment.

A minimum system can operate in 4K words of memory but may be expanded to maximum memory size (32K).

Executive Services are provided for I/O operations, task scheduling and timer functions. An operator communication package is also provided.

In addition, the system requires the real-time clock feature and programmer's control panel. The only required peripheral is a console typer (ASR-33 or equivalent).

SAX I provides four executive services which are callable from any user task. These are:

**EXIT** — suspends task execution until activated by an interrupt or another task.

**ABORT** — transfer control to a user supplied abort routine or set the task to an EXIT condition.

**RELINQUISH** — gives control to other active tasks.

**DELAY** — suspends execution for a specified time duration.

I/O and code conversion subroutines are also provided for all supported peripherals such as the console typer, paper tape reader/punch, card reader, line printer and process I/O peripherals (analog and digital).

An operator communication task accepts commands from the console typer in the form of sample English sentences. The directives provided are:

**TIME** — allows the user to display and modify the time of day.

**DATE** — displays and modifies the date.

**DISPLAY** — causes a hexadecimal dump of a core memory block.

**EXIT** — terminates the operator communication task.

A syntax analyzer is provided for special character search and word number conversion, which is directly callable from any user task.

# MODCOMP II and III Software



The MODCOMP II and III software is designed to provide the user with the most efficient utilization of his system configuration. The available software systems may be divided in three categories:

- Language processors
- Utility processors
- Executive Systems

## Language Processors

### Assembler

The MODCOMP II and III Assembler is a language processor which enables instructions, addresses and other program parameters to be written in an efficient symbolic language.

The assembler is designed to operate under MAX I or MAX II. Operation is two pass, with the source input being copied to a scratch file if one is assigned. The input to the second pass is then the scratch file. The minimum system hardware configuration required to support the assembler is a MODCOMP II or III having at least 4K words of memory and an ASR-33. Even in this minimum system the user can expect to handle up to 200 symbol names. As more core memory is made available, the symbol table is extended to make use of this space. Additional symbols can be added at the rate of one symbol for every three words of memory.

The following Assembler features contribute to the ease of writing programs for MODCOMP computers.

- Both absolute and relocatable object format
- Free field assembly format
- Extensive set of directives for aiding in expressing constants, allocating storage, inter-program communications and listed output formatting

- Complete error diagnostics
- Object listing including the source statements and the object code produced by each
- Symbolic addressing which allows a symbol rather than absolute values to be used for memory locations, registers, bit assignments and short displacement addressing
- Mnemonics for representing each MODCOMP instruction
- Ability to define new instructions implemented in the ROM controller

The Assembler is capable of accepting constants both as operands in an immediate instruction and in data statements. The following types of constants are recognized:

- Decimal Integer
- Hexadecimal Integer
- Character String
- Address Constant
- Compressed Alphanumeric Character String

## FORTRAN-Coded Cross Assembler

The FORTRAN-Coded Assembler is a cross assembler that allows MODCOMP programs to be assembled on an IBM 360 or 370 or a Control Data 6000 series computer. This cross assembler accepts source inputs and produces object outputs that are identical to those of the standard MODCOMP assembler. It operates on an IBM 360 or 370 under DOS. The required system configuration includes 65K bytes of core memory, a card reader, a line printer, a card punch, and optionally a disc file or magnetic tape.

## Macro-Assembler

The MODCOMP Macro Assembler provides an even more powerful assembly capability than the MODCOMP Assembler. It is a superset of the MODCOMP Assembler and contains all of the Assembler capabilities, plus additional capabilities including the generation of nested macros, recursive macro calls, conditional assembly statements, assembly time branches and macro exits. Any program that can be processed by the Assembler can be processed by the Macro Assembler. The Macro Assembler is designed to operate under MAX II or MAX III in a system with at least 16K words of memory. The Macro Assembler itself operates in approximately 6K words of memory.

This includes the table area required for storing macro-prototypes and the symbol table. Operation is two-pass with the source input being copied to a scratch file when one is assigned.

The Macro Assembler accepts the additional constant formats:

- Fixed Point Single Precision
- Fixed Point Double Precision
- Floating Point Single Precision
- Floating Point Double Precision

The Macro Assembler contains directives which allow the definition of macro-prototypes, conditional assembly, custom hardware macros and symbol definition. Labels that are defined in the main program can be referenced from the main program or from within a macro called by that program. Labels that are defined in a macro can be referenced by that macro or by any macro that it may call. Labels in a macro can be defined as global to permit reference by a calling macro or the main program.

The Macro Assembler provides the capability for defining COMMON blocks for communication between FORTRAN programs and assembly language subroutines.

## **FORTRAN IV**

The MODCOMP FORTRAN IV compiler meets the specifications of the American National Standards Institute (X3.9, 1966). In addition, it has a set of real-time extensions which make FORTRAN a useful data acquisition and control language.

MODCOMP FORTRAN is designed to produce efficient code through subscript optimization, block level optimization and the utilization of all machine capabilities such as all general registers and the full instruction set.

Direct access I/O to disc files is provided through DEFINE FILE statements. A Direct Maintenance Processor (DAMP) provides the utility functions for the creation and deletion of disc files to be used with the FORTRAN direct access I/O system.

The programmer using the MODCOMP FORTRAN IV compiler can write source programs incorporating in-line assembly language coding including macro directives. The user can also call all of the MAX executive services through in-line assembly language coding for maximum run-time efficiency.

A set of CALL subroutines have been added to the FORTRAN run-time package which are compatible with process control industry recommendations. These extensions are based upon the proceedings of the Workshop on Standardization of Industrial Computer Language, Purdue University, 1970. They provide real-time capabilities for execution control of real time tasks, status testing, and interrupt utilization.

Array extensions provide the user with the freedom of using any arithmetic expression as an array subscript.

Program writing with the MODCOMP FORTRAN IV compiler is aided by a comprehensive diagnostic capability which provides maximum assistance in the form of error printouts indicating the types and number of errors that exist in any line of coding.

## **Basic**

### **Language**

The MODCOMP BASIC enables users having no previous programming experience to write programs in a simple, quickly learnable language. In medium-size machine configurations, it supports an extended set of the elementary capabilities defined by the Dartmouth specification. Therefore, it is a very useful tool for performing mathematical computations.

### **Real Time Extensions**

The MODCOMP BASIC also contains an important extension which makes it a very useful tool for real-time and other special purpose applications. A CALL statement is included. A user can prepare and then CALL a set of subroutines which perform special functions useful to him. For example, one subroutine could cause an analog value to be measured and read into the computer. Subsequent statements could then perform operations on the measured value.

The CALL statement enables BASIC to be used to conduct interactive, on-line experiments. In applications such as factory testing, test procedures for new devices to be tested by the system can be developed and checked out in an on-line interactive mode by the test engineer.

## **Utility Processors**

Utility processors execute under the MAX II or MAX III operating systems as a batch processing function. These utility processors are:

- DEBUG EXECUTIVE
- SOURCE UPDATE
- SOURCE MAINTENANCE CONTROL
- LIBRARY UPDATE
- LINK EDITOR
- CATALOGER
- DIRECT ACCESS MAINTENANCE PROCESSOR

## **Debug Executive**

The DEBUG EXECUTIVE provides an easily used program debugging service. It is controlled through the use of debug directives which are similar in form to the standard job control statements. All debug directives are entered at program execution time, thus eliminating the need to assemble in any special calls for debug services. The functions available under control of the Debug Executive are:

- Snapshot dumps of any memory location
- Mnemonic trace of any program segment
- Pause for operator action at any specified location
- Modification of memory or general registers
- Transfer of control to any specified location
- Display of memory and/or general registers
- Setting of specified memory locations to a constant
- Modification of logical file assignments

## Source Update

SOURCE UPDATE allows user manipulation of source files by adding, deleting and listing individual or blocks of records.

Source files may be on any supported media such as cards, paper tape, magnetic tape or disc storage.

Source update commands may be entered through the command input file which may be assigned to the console typer, card reader, paper tape reader, magnetic tape or disc storage.

## Source Maintenance Control (SMC)

The source Maintenance Control processor is designed for the user which maintains source files on disc storage. It provides a directoried disc file for source programs and a comprehensive set of commands for adding, deleting, listing and compressing the source modules.

In addition, a set of simplified JOB CONTROL STATEMENTS are provided for ease of operation in compile, assembly, link-edit, cataloging and execute sequences.

## Library Update

LIBRARY UPDATE provides the user with the capability to manipulate object records on any supported media. Input commands are available to add, delete, list, compress and retrieve binary records.

## Link Editor

The LINK EDITOR allows the linking of object modules which have been assembled separately. In addition, external references to GLOBAL COMMON areas or GLOBAL SUBROUTINES are satisfied at link-edit time, allowing for maximum flexibility since its actual addresses need not be defined at assembly time.

After a successful link edit operation an optional map is printed with the starting and ending location of every named module. Diagnostic messages for linking errors and missing modules are also generated.

## Cataloger

The CATALOGER is the maintenance processor for the load module files. Its main function is to catalog object or link-edited modules in preassigned disc files.

The CATALOGER maintains a directory of all cataloged modules on every load module file. Ancillary functions include:

- Creation of directories on any preassigned file
- Listing of directory entries
- Compression of files
- Reassignment of system files
- Deletion of cataloged modules

## Direct Access Maintenance Processor

The DIRECT ACCESS MAINTENANCE PROCESSOR provides the utility functions required to maintain data files in disc storage. A directory is maintained in the standard RAD file which contains information on the data file name, size and starting sector address. Input commands are provided to create directory entries, allocate, delete and compress files.

## Executive Systems

Three Modular Application Executive (MAX) systems are available with MODCOMP computers to meet the requirements of a wide range of operating environments. The MAX systems consist of a family of interlocking software elements that can be combined to form complete operating systems. MAX systems can be tailored by means of a system generation procedure to match the hardware configuration and the desired system elements.

### MAX I

MAX I is a core resident operating system designed for use as a software development tool in minimum configuration MODCOMP II and III systems. It provides operator communications, input/output handlers, debug features, and load/dump capabilities. It allows direct operator control for assemblies, program debugging operations and program executions through the console teletypewriter or card reader. All processors which run under MAX I are loaded into memory through the I/O service routines which are resident with the basic elements of the executive.

#### Features

- Assemble programs using the MODCOMP assembler
- Load programs in absolute and relocatable formats
- Assign logical files to peripheral devices
- Dump memory locations in absolute core-image object code

- Dump memory locations and general register contents in hexadecimal form
- Alter contents of general registers or memory
- Transfer control to any memory location

MAX I is loaded into memory by the automatic hardware fill procedure from either paper tape, cards, or magnetic tape. Upon completion of loading and initiation of the program, operator inputs are requested through the console teletypewriter. Commands can then be typed in to load other programs, alter memory, transfer control, etc. When a program running under MAX I completes its execution, it transfers control to the executive which again requests input from the operator at the console teletypewriter. The card reader can be assigned to the control input logical file in place of the console teletypewriter so that control cards can be used instead of typed-in commands for batch job processing.

The minimum MAX I hardware configuration is the basic MODCOMP II or III with 4K words of memory and the ASR-33. The additional computer options supported by MAX I include:

- Memory to maximum configuration
- Multiply/Divide

In addition to the console teletypewriter, the following peripheral devices are supported by MAX I and are shown with their standard and optional assignments to logical files.

#### Peripheral Device Assignments

LOGICAL FILE	STANDARD DEVICE	OPTIONAL DEVICE
Symbolic Input	Card Reader	Paper Tape Teletype Magnetic Tape
Binary Input	Paper Tape	Card Reader Magnetic Tape
Control Input	Teletype	Card Reader
Binary Output	Paper Tape	Magnetic Tape
Listing Output	Line Printer	Teletype Magnetic Tape
Diagnostic Output	Teletype	Line Printer

## MAX II

MAX II is an operating system designed for the batch-oriented user requiring limited real-time capabilities. It is a multiprogramming system capable of executing multiple core-resident tasks concurrently with a batch job stream. Two versions are available: core and batch.

#### Core Version Features

- A taskmaster which multiplexes the central processor time among any number of core resident tasks.

- Up to 128 unique execution priority levels
- An operator communication package for task communication and control
- Task activation based on operator directive, directly connected interrupts or another task
- Re-entrant executive services for I/O operations, execution control, byte string syntax analysis, code conversions and other utility services
- A device independent I/O system which support all MODCOMP standard peripherals
- Interrupt driven I/O for full overlap with task execution
- Global areas and file assignments for multitasks communication
- Optional background task to support batch processing operations
- Optional loader service for non-resident overlay programs
- Re-entrant floating point simulation package
- Re-entrant FORTRAN IV run-time package

#### Batch Version Features

In addition to all features available in the core version, the batch version supports the usage of bulk storage devices such as magnetic tape and disc (moving or fixed head). Its additional features include:

- A standard loader service which allows core resident tasks to load and execute overlay programs and sub-routines in core areas already assigned to the calling task
- A resident background task which uses a non-resident JOB CONTROL overlay to control batch processing operations
- Non-resident operator communication directives which are cataloged as overlays on the disc. Its open-ended design allows the user the capability of adding his own operator directives.
- JOB CONTROL procedures may be cataloged on disc. This allows any sequence of JOB CONTROL statements to be executed with a single macro-type statement (\$DO)

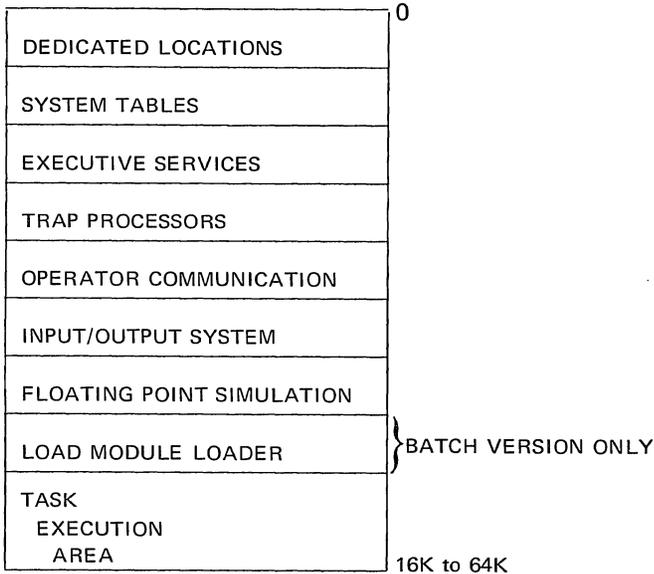
#### Hardware Requirements

Both MAX II versions require at least a MODCOMP II or III with 16K words of memory. Hardware multiply/divide and executive features are also required as mainframe options. The required peripherals include an ASR-33 and a binary input/output device combination which can include a paper tape reader/punch, a card reader, disc or magnetic tape.

In addition, the batch version requires a bulk storage device such as a magnetic tape or disc unit with at least 128K word capacity.

## Memory Utilization

Memory allocation among executing tasks is determined at SYSGEN time. All tasks are core resident but each task may have any number of overlays which can be loaded on request from the load module file on disc (batch version only). A memory map follows:



## MAX II Batch-Processing Operation

One of the core resident tasks defined to MAX II may be a background task which can request the execution of the JOB CONTROL overlay. This overlay allows the utilization of a rich set of JOB CONTROL LANGUAGE statements to initiate execution and control of any of the language processors or utility processors. In addition, user written programs may be compiled, assembled, link-edited, cataloged and executed through an appropriate stream of JOB CONTROL statements.

All executive services are available to the user to initiate I/O operations, control task execution and other utility functions such as code conversions and byte-string manipulation.

## MAX III

**General** — MAX III is a real-time multiprogramming system having foreground/middleground/background capabilities. It is a task oriented system that can handle up to 256 active tasks (128 foreground, 127 middleground and one background). MAX III is available in a variety of configurations because it consists of software modules that are linked at system generation time to form a real time executive tailored to the hardware configuration and operating environment.

Three versions are available: the core, batch and extended versions. Each is designed to provide the user with maximum capability within his configuration.

## Core Version

The core version of MAX III executes core resident foreground tasks which are contained entirely within fixed areas of core memory. Additional features include:

- A real-time clock for maintaining the time-of-day, timing task delays, and updating system "watchdog" timers.
- A CPU execution control executive, driven by the clock and by external event interrupts, which permits the efficient execution of system-connected tasks on up to 128 unique foreground priority levels.
- Optional execution of more than one task at each priority level.
- Tasks may be activated by hardware interrupt, by operator request, by a request from another active task, by elapsed time, or by time-of-day.
- Re-entrant executive services available to all system-connected tasks — for critical response requirements.
- Queued Input/Output services which may be performed concurrently with task execution or with the calling task suspended. Error recovery may be automatic or may be under complete control of the calling task.
- An Input/Output device may be assigned exclusively to a privileged task so that only that task can use the device.
- A modular operator-communications package which provides the system operator with complete control of all system resources; and can be expanded so that the user can develop his own inter-active control language for controlling his processes.
- Off-line system-generation program for configuring the resident elements and tasks of the system. This program allows system-generation of a large core-resident system in a small core configuration.
- Transient core allocation of any remaining core not used for the resident elements.
- Important (or frequently-used) library subroutines may be declared resident at system-generation time. If they are re-entrant, they may be made global (accessible to multiple tasks). Core tables and variables may also be made global in this manner and provide a convenient method for intertask communication.

The FORTRAN IV run time package is an example of a global re-entrant subroutine resulting in core savings of 2.7K words of core per additional FORTRAN written task.

## Batch Version

The batch version provides, in addition to the capabilities of the core version, a full-service loader which can load non-resident overlay programs cataloged on either sequential or random access devices. An optional background task may be added which uses a non-resident JOB CONTROL overlay to control batch processing operations.

The batch version is basically a foreground/background without middleground or background checkpointing capabilities.

### Extended Version

The extended version of MAX III has foreground/middleground/background capabilities with the following additional features:

- One or more independent core pools can be established for foreground and middleground execution. Core is then dynamically allocated to each executing task on a priority basis.
- Active tasks can request additional core blocks at run-time which will be deallocated automatically when the task exits.
- A background area to support batch processing operations can be defined. This area is checkpointable (saved to a disc file) by higher priority non-resident foreground programs which require its core area. Low priority foreground tasks may be defined as checkpointable to implement multi-level checkpointing operations. By defining a disc file large enough for a worst case condition of background/foreground checkpointing, the user may insure execution of a non-resident foreground task regardless of task activation sequence.
- Background and middleground core area sizes can be changed by the operator through the console typer.
- Spooling of all low speed printing devices is implemented. The system will automatically buffer all printed output to an intermediate disc file for later processing by a spooling task which is optionally included in the MAX III system at SYSGEN time.
- Multiple user BASIC may execute as a foreground/middleground task or background overlay.

### Hardware Requirements

All versions of MAX III require a MODCOMP II or III with 16K of core memory and the following mainframe options:

- Hardware multiply/divide
- Executive features
- System protect feature

The core only version requires a console typer (ASR-33 or equivalent) and binary input/output device combination which may include a paper tape reader/punch, card reader, magnetic tape or disc (fixed or moving head).

The batch version requires a magnetic tape or disc drive in addition to the above items. A disc drive with at least 256K word capacity is required for the extended version.

### Taskmaster

In the MAX III multiprogramming environment, many tasks can compete for computer time. Order is maintained by the Taskmaster, a resident system element which transfers CPU control to the highest priority task and threads new requests for CPU time into a queue according to priority. The Taskmaster is directly connected to the

lowest priority interrupt level. All tasks are assigned software priority levels below the lowest hardware level.

More than one task can be assigned to each software priority level. These software priority levels can be scheduled and controlled by operator request, external or internal hardware interrupt, elapsed time, time-of-day, or by another task.

### Operator Communications

The Operator Communication Dispatcher provides on-line control of MAX III operations. The operator can assign devices to logical files, create logical files, assign tasks to priority levels, control the execution of tasks, establish disc-resident tasks as core-resident, and even add his own control commands. The user's control commands can be implemented for entry on a dedicated terminal device or they can be entered through the basic Operator Communication file.

The MAX III executive is designed to operate with minimum operator intervention but the flexibility of the Operator Communication dispatcher makes it well suited to applications requiring extensive operator/system interaction. Such a system can be supported through the standard console teletype or through additional remote terminals where the specific set of operator control functions can even be made unique to that terminal.

### Task Execution

Tasks may execute under MAX III in either of two modes: privileged or unprivileged.

The privileged mode is the "supervisory mode" where the task has absolute control over memory and system resources. The task may write over any core area, branch to any core address and execute all instructions including I/O and interrupt handling instructions.

The unprivileged mode is the "user mode" where the task has absolute control within its own memory boundaries and must utilize executive services to perform I/O or other system resource manipulation. In addition, the task can write into the unprotected GLOBAL COMMON area.

Execution modes are assigned as follows:

- FOREGROUND — privileged or unprivileged, depending upon execution priority
- MIDDLEGROUND — always unprivileged
- BACKGROUND — always unprivileged

### Memory Protection and System Security

Memory protection is implemented under MAX III to allow secure system operation with minimum system overhead. Memory is dynamically protected and un-protected according to the execution mode of each task.

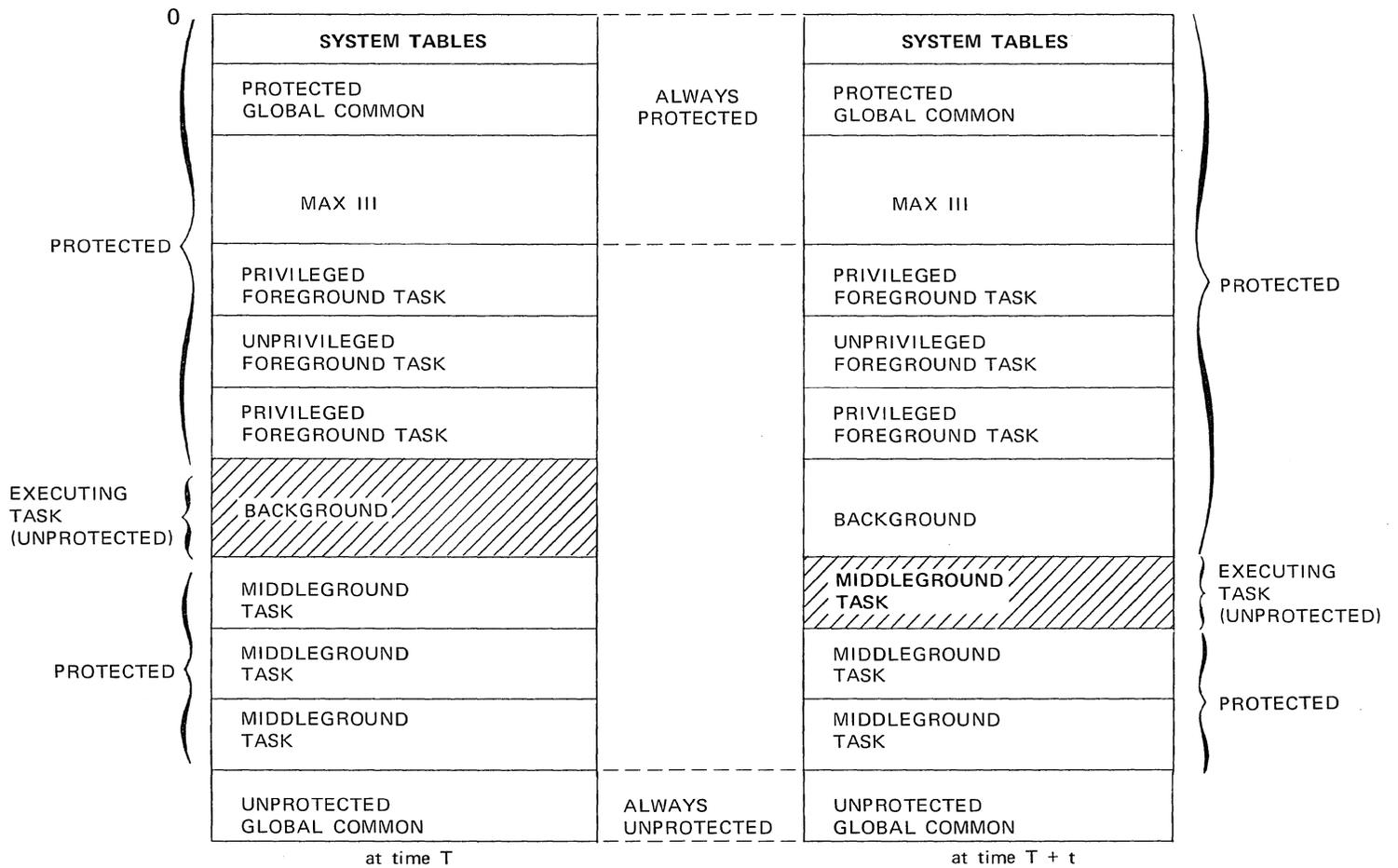
Three hardware boundaries are provided to implement this memory protection scheme in the MODCOMP II processor. One boundary is provided for the MODCOMP III.

## MODCOMP II Operation

Foreground tasks running in the privileged mode always have memory allocated in the protected state, allowing these tasks to access any memory area.

Unprivileged tasks (foreground, middleground or background) always run with memory allocated in the un-

protected state with the rest of core memory (except unprotected GLOBAL COMMON) set in the protected state. This operation insures that unprivileged tasks will not alter any other tasks in core in case of faulty internal task logic. The following picture illustrates this point:



MODCOMP II Memory Protect Operation

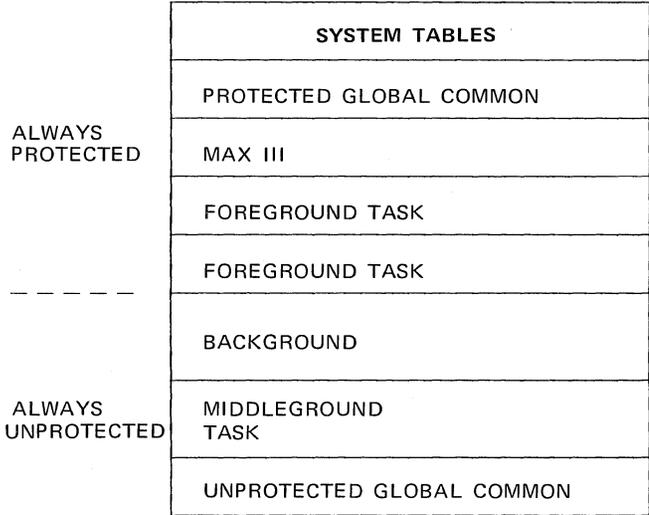
**MODCOMP III Operation**

Foreground tasks always run in protected core while middleground and background always run in unprotected core.

Protection is implemented on a core pool basis rather than on a task basis. The opposite picture illustrates this point:

**Batch Processing Capabilities**

Batch processing is provided under the batch or extended version of MAX III. The JOB CONTROL overlay allows execution of any of the language and utility processors, or user written batch programs. The Job Control Language is identical to that of MAX II, providing full compatibility between both systems in source and job control statements.



**MODCOMP III Memory Protect Operation**

## PERIPHERAL CONTROLLER INTERFACE & OPTIONS



### Features

- Models 4901 and 4902 – MODCOMP III
- Model 4903 – MODCOMP I and II

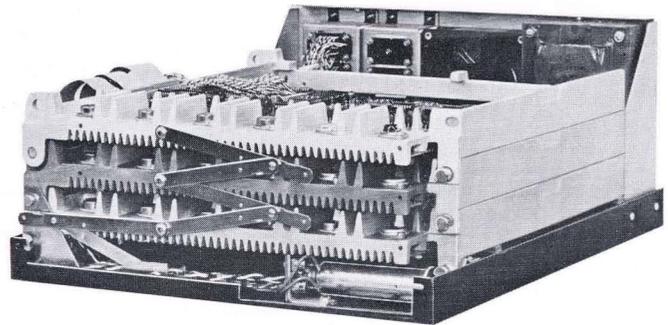
The Peripheral Controller Interface (PCI) consists of an enclosure, power supplies, a differential or single ended interface to the I/O bus and DMP, and up to four planes on which the peripheral controllers are mounted.

The Model 4901 and 4902 PCIs contain differential cable drivers and receivers which are connectable to a MODCOMP III. The Model 4903 PCI contains a TTL Single-Ended cable driver and receiver module which is connectable to a MODCOMP I or II computer.

Each driver/receiver module is capable of connecting from one to four peripheral controllers to the MODCOMP I/O bus. All controllers have identical interfaces, and therefore any controller can be connected in any PCI. The Model 4901 and 4903 PCIs contain one driver/receiver module, and the Model 4902 contains two driver/receiver modules.

From one to eight driver/receiver modules of the same type can be connected to one computer. These modules can be either in PCIs or in Input/Output Interface Subsystems. All driver/receiver modules are connected serially by I/O cables, which may have a combined length of 100 feet.

The planes in the PCI use the same type frames as those in the MODCOMP computers. Each driver/receiver module occupies one half plane position. Each peripheral controller occupies from one to three half plane positions. Most controllers occupy a single position. The disc and magnetic tape controllers occupy two positions, and the Universal Communications Multiplexer controller occupies three positions.



4903 PCI (Front Panel Removed)

### Physical Dimensions

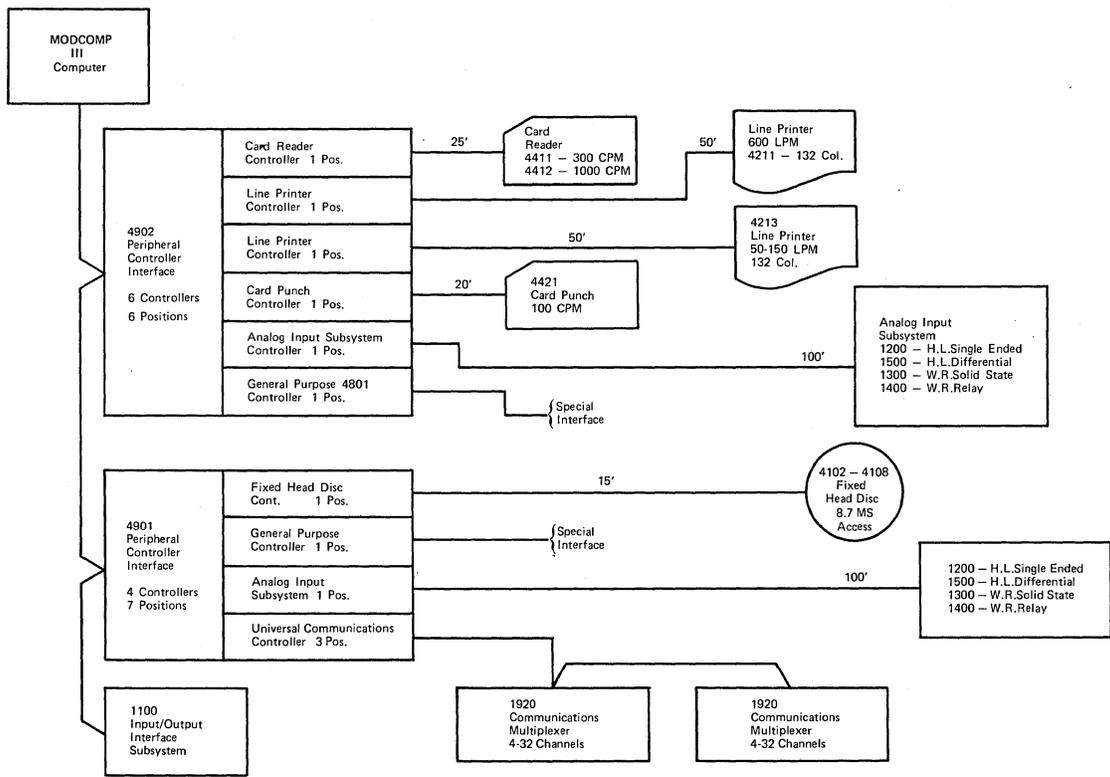
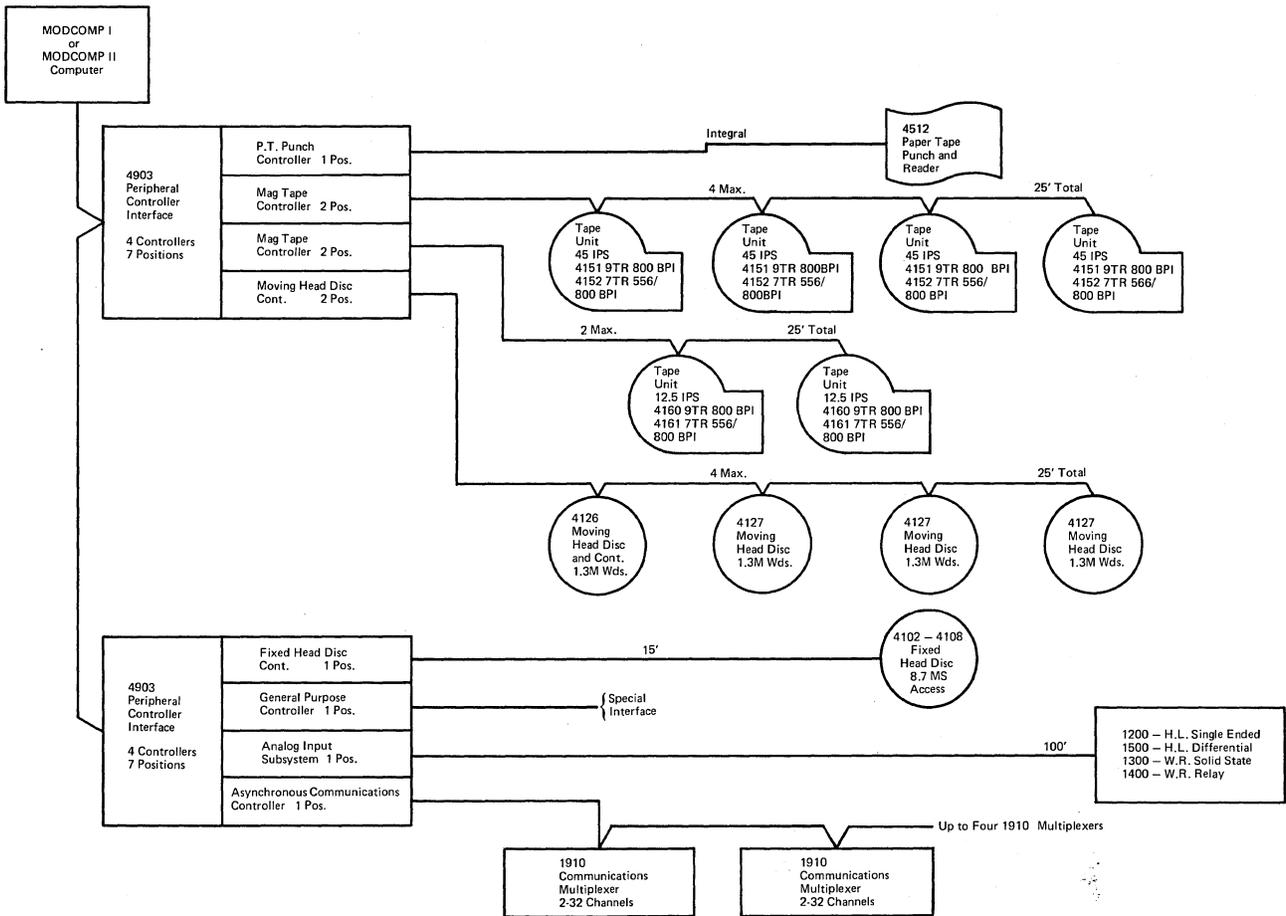
- Models 4901 and 4902 are rack mountable in a standard 19" rack and are 26-1/4 inches high including power supplies.
- Model 4903 is rack mountable in a standard 19" rack and is 8-3/4 inches high including power supplies.

### Peripheral Device Configurations

The Peripheral Device Configurator illustrates the use of the PCIs. Any controller shown in the Peripheral Device Configurator can be connected in any model 4901, 4902 or 4903 PCI. All controllers have the same interface to a PCI.

#### Direct Memory Processor (DMP)

Peripheral Device Controllers which have high transfer rates are connected to DMP channels to reduce the amount of program involvement in I/O transfers. A DMP interface is included in the controllers for discs, magnetic tape units, solid state analog input subsystems, and many communication and custom interface units. No special placement or cabling is required for controllers connected to the DMP.



Peripheral Device Configurator

# Communications Channels

The 481X series of communications channels provide the MODCOMP system user an economical means of interfacing a small number of communication lines. In installations requiring numerous communications lines either the Asynchronous or Universal Multiplexing subsystems become more cost effective. The 481X series offers both asynchronous and synchronous channels, providing an efficient means of communicating with a remote terminal or computer.

## Channel Features

The channels are configured for maximum flexibility and minimum processor overhead. Standard features of the channels are:

- Double Character Buffering
- Full or Half Duplex Operation
- RS232 or TTY Current Loop Interfaces
- 75-50 Kilo Baud
- Hardware Echo (Asynchronous)
- Programmable Hardware Wraparound
- Programmable Frame Size (5, 6, 7 or 8 Bits)
- Programmable Character Parity (ODD, EVEN, or NONE)
- Character Parity Checking/Generation
- Selectable Sync Character (Synchronous)
- Automatic Leading Sync Character Generation (Output)
- Automatic Leading Sync Character Deletion (Receive)
- Programmable Stop Bits (1 or 2 Bits, Asynchronous)
- Hardware CRC Generation/Accumulation (4817 Synchronous)
- Baud Rates — 1 of 5 Internal or External Clocking

## Channel Characteristics

The 481X Series of Communications channels contains 4 different channel configurations. These are:

- 4810 Dual Asynchronous Interface, two full/half duplex channels 75-9600 baud, 20 MA current loop
- 4811 Dual Asynchronous Interface, two full/half duplex channels 75-9600 baud, RS232-C compatible modem interface
- 4815 Dual Synchronous Interface, two full/half duplex channels 110-50K baud, RS232-C compatible modem interface
- 4817 Synchronous Interface, one full/half duplex channel with CRC hardware generation/accumulation, RS232-C compatible

With the above interface capabilities, almost any terminal or remote computer communication requirement can be met.

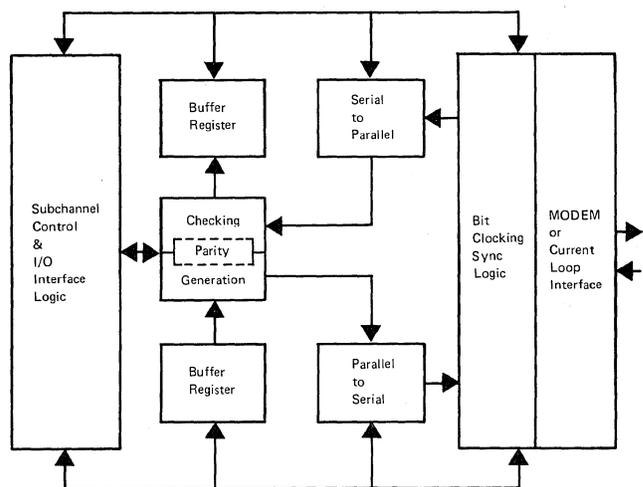
## Functional Description

Each of the channels is packaged on a single half plane and requires one controller position within a standard MODCOMP PCI.

The primary function of each half/full duplex subchannel is to perform serial to parallel conversion on the receive line and parallel to serial conversion of data to be transmitted. Each synchronous subchannel has a set of eight micro switches with which the sync character code is entered. The synchronous channels automatically, upon initiation of output, insert 6 leading sync characters. Upon initiation of input the subchannels automatically establish synchronization and strip all leading sync characters.

Each subchannel, in addition to the parallel to serial and serial to parallel registers, contains a character buffer register, providing double buffering of all data. This feature reduces considerably the chances of an overflow condition occurring.

During input, if character parity is specified, the subchannels check and strip the parity bit before transferring the character to the processor. During output the parity bit is generated and added to the character by the channel hardware before transmission occurs. A block diagram of a single full duplex subchannel is shown below.



Single Full Duplex Subchannel

# Interval Timer

The model 4701-X Interval Timer consists of a 16 bit counter that can be set and interrogated under program control. It provides an interrupt to the computer when countdown is complete.

The Interval Timer occupies one half-plane controller position in a PCI.

The Interval Timer features a choice of seven different frequencies plus an external clock for updating of the 16 bit counter.

- Model 4701-1      1 us interval
- Model 4701-2      2 us interval
- Model 4701-3      5 us interval
- Model 4701-4     10 us interval
- Model 4701-5     20 us interval
- Model 4701-6     50 us interval
- Model 4701-7     100 us interval
- Model 4701-10    External Clock

## General Description

Two modes of operation are available with the Interval Timer – recycle mode or single interval mode. The mode

of operation is selected by executing an output command instruction from the computer.

Once the mode of operation has been selected, an Output Data instruction may be executed to load the interval count desired in the output register of the interval timer module. Simultaneously the complement of the output register is loaded into the interval counter and the clock counting is started. The frequency of this clock depends on the model number selected. When the interval counter has counted up to all ones, signifying completion of the interval, the detector enables the End Interval line to the control logic. If single interval mode had been selected, the control enables the Interrupt Request Line and terminates operation. If recycle mode had been selected, the control logic will reload the interval counter from the output register after requesting the interrupt, and it will begin the counting of the next interval.

During any interval, an Output Data instruction will cause the timer to reinitialize to the interval applied to the data bus and resume the count without interrupting. This feature permits the timer to be used as a watchdog timer.

The current timer count can also be read into the computer at any time by the execution of an Input Data instruction.

# KEYBOARD/PRINTERS AND ALPHANUMERIC CRT DISPLAYS



## Features

A variety of keyboard/printer/display devices are offered with MODCOMP computers to perform the functions:

- Console control devices for use with the MAX, MIN and SAX operating systems
- Source input, object output, and listing output devices for use with assemblers and compilers
- Interactive BASIC terminals
- Remote logging, control and display terminal devices

### Choice of Devices

The standard devices available with all MODCOMP computers consist of the Model 33 and Model 35 Teletype keyboard/printers and a CRT unit. Three of these devices – the ASR-33, ASR-35 and KSR-35 are inventoried to be available for quick delivery.

All devices which have asynchronous RS232C interfaces or current loop interfaces and use ASCII character codes can be connected to MODCOMP computers and used for the functions listed above. A wide selection of alphanumeric CRT displays and communications terminals are available with RS232C and/or current loop interfaces.

### Choice of Controllers

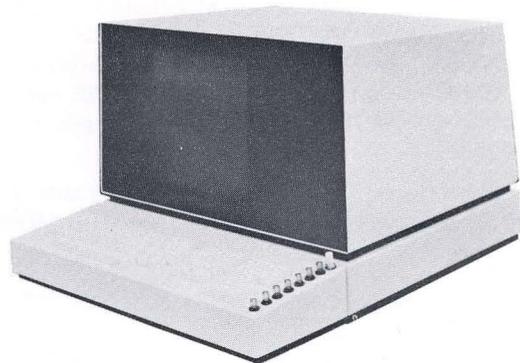
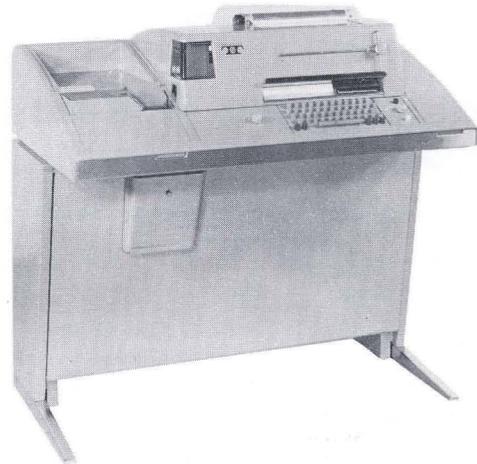
The console device controller in MODCOMP computers can handle a variety of devices as defined in the table below:

Computer	ASR-33	KSR-35	ASR-35	RS232C Terminals	625 CPS Paper Tape Reader
MODCOMP I	X	X	—	—	X
MODCOMP II	X	X	X	X	X
MODCOMP III	X	X	X	X	X

The other asynchronous device controllers available are:

Models	Contained In
4810, 4811	4901, 4903 Peripheral Controller Interfaces
1115, 1116	1100, 1199 Input/Output Interface Subsystems
1911, 1912	1910 Asynchronous Communications Multiplexer
1924, 1925	1920 Universal Communications Multiplexer

The controllers contained in the PCI and I/OIS units are assignable to logical devices in the MAX II and III systems. Therefore they can be used as operating system control, source input, object output, and listing output devices.



# Device Specifications

## Model 4223 and 4233 Keyboard/Printer

These models are ASR-33 Teletype units. They contain keyboard, printer, paper tape reader and paper tape punch. The two models differ in that the Model 4223 is a standard ASR-33 and the Model 4233 is modified to have program controlled paper tape start/stop capability for console operation. The Model 4223 can be connected to a MODCOMP computer through all of the asynchronous controllers listed except the console device controllers. The Model 4233 can be connected through all MODCOMP console device controllers.

A model 4250 Modification Kit is available which enables a standard ASR-33 to be modified to a Model 4233 Console keyboard/printer.

### Specifications

Speed – 10 characters per second  
 Code – Standard ASCII  
 Cable Length – 30 feet  
 Printer – 8-1/2 inch paper, 72 characters per line  
 Paper Tape – 8 level, 1 inch wide oiled paper  
 Keyboard – 4 row, similar to typewriter  
 Environmental Requirements  
     Operating Temperature – 40° to 110°F Ambient  
     Humidity – 95% maximum  
 Power – 115-V AC ±10%, 60 Hz ±0.45 Hz  
     Current – 8A Starting, 2A Continuous  
 Dimensions – 32-7/8 inches high, 22 inches wide,  
                   18-1/2 inches deep  
 Weight – 56 pounds

## Models 4224, 4225, 4234 and 4235 Keyboard/Printers

These keyboard/printers are Teletype Model 35 units:

MODCOMP Model	Teletype Model	Use
4224	KSR-35	Remote Operation
4225	ASR-35	Remote Operation
4234	KSR-35	Console Operation
4235	ASR-35	Console Operation

All units have keyboards and printers. Only the ASR units have paper tape reader and punch. The remote units can be connected to all MODCOMP asynchronous controllers except the console device controllers. The Model 4234 console unit can be connected to any MODCOMP computer, and the Model 4235 can be connected to any MODCOMP computer except the MODCOMP I.

The modification kits are available to enable standard Model 35 Teletype units to be converted to MODCOMP console devices:

Kit Model	Converts Teletype Model to	MODCOMP Model
4251	KSR-35	4234
4252	ASR-35	4235

### Specifications

Speed – 10 characters per second  
 Code – Standard ASCII  
 Cable Length – 30 feet  
 Printer – 8-1/2 inch paper, 72 characters per lint  
 Paper Tape – 8 level, 1 inch wide oiled paper  
 Keyboard – 4 row, similar to typewriter  
 Environmental Requirements  
     Operating Temperature – 40° to 110°F Ambient  
     Humidity – 95% maximum  
 ASR-35 Power – 115-V AC ±10%, 60 Hz ±0.45 Hz  
     Current – 9A Starting, 2A Continuous  
 Dimensions:  
     4224, 4234 – 38-1/2 inches high, 20 inches wide,  
                   24 inches deep  
     4225, 4235 – 38-1/2 inches high, 40 inches wide,  
                   24 inches deep  
 Weight – 4224, 4234 – 136 pounds  
           4225, 4235 – 225 pounds

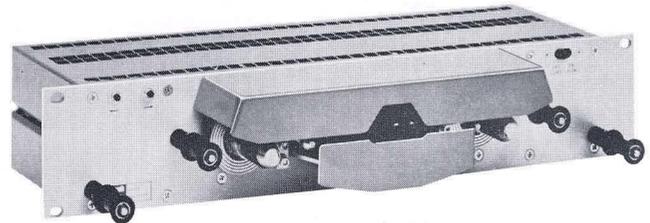
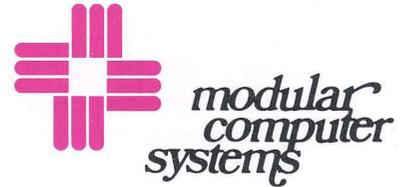
## Console Alphanumeric CRT

The Model 4620 Alphanumeric Crt display and keyboard can be connected to a MODCOMP computer via any of the available asynchronous RS232C interfaces. When connected in place of the console teletypewriter, this unit can be used as the control input for the MAX I, II and III Operating Systems.

### Specifications

Screen Size – 12 inch diagonal  
 Memory Type – 2048 x 8 magnetic core  
 Operating Modes – Full duplex, half duplex or batch (by switch)  
 Transmission Ratio – 110 - 9600 baud  
 Character Structure – 5 x 7 dot matrix, using standard 525 line TV raster  
 Character Repertoire – 64 alpha-numerics and symbols. 32 ASCII control codes.  
 Screen Character – 1998 characters. 74 characters per line. 27 lines per display.  
 Editing Features – Thirteen distinct editing operations from the keyboard, including character and line insert/delete. Eight distinct editing operations under computer control.  
 Split Screen – Two level video intensity is utilized to distinguish computer derived and protected data from unprotected data, which can be modified by the keyboard operator  
 Cursor Addressability – Program may direct the cursor to any character position on the screen simply by transmitting X-Y coordinates  
 Status Lights – Five status lights are provided to indicate the operational state of the system  
 Refresh Rate – 60 fields per second  
 Power – 350 watts  
 Dimensions – 22 inches deep, 18-1/2 inches wide, 12-1/2 inches high  
 Weight – 73 pounds

## PAPER TAPE READER AND PUNCH



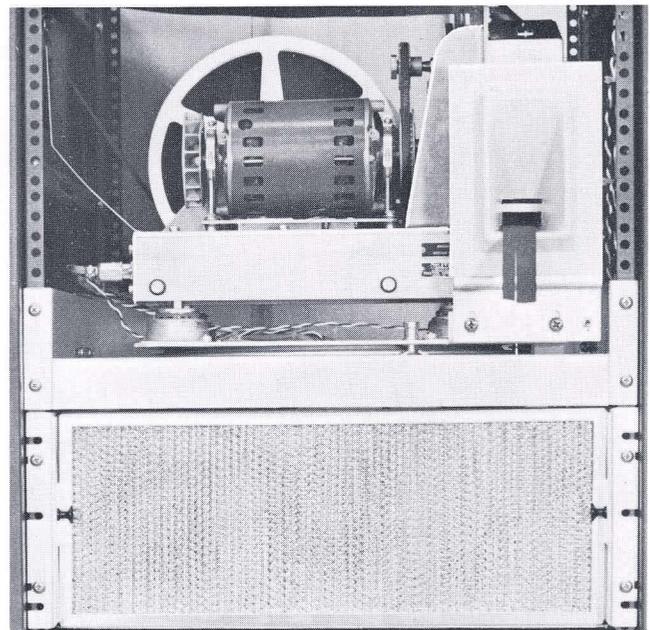
### Paper Tape Reader

The Models 4511 and 4513 paper tape readers offer an economical and high speed means for loading programs and data into MODCOMP computers. Both models operate at 625 characters per second. The Model 4511 operates with MODCOMP III computers and is mounted as an integral console unit. The Model 4513 operates with MODCOMP I and II computers. It is normally mounted directly below the computer control panel.

The paper tape reader is connected to the same controller as the console keyboard/printer. If the console device includes a paper tape reader, the controller will automatically connect to the console unit to read paper tape, provided that the Model 4511 or 4513 power is turned off. If the power is turned on in the Model 4511 or 4513 reader, the console device controller will automatically connect to this higher speed paper tape reader. Therefore the operator's use of the two units, if present, is program transparent.

### Specifications

- Reading Speed – Start/Stop – 0 to 150 CPS  
Continuous – 625 CPS
- Start Time – 25 milliseconds
- Stop Time – 200 microseconds
- Stopping Characteristics – On character to full  
rated speed
- Tape – 1 inch, EIA Standard, 8 level & sprocket,  
50% opacity, .0025 – .005 inch thick. No  
adjustments required for thickness or  
opacity.
- Dimensions – 3.5 inches high, 19 inches wide,  
5.7 inches deep
- Controller – Integral to MODCOMP central processor
- Environmental Requirements
  - Operating temperature – 0°C to 50°C ambient
  - Relative humidity – 10% to 90% noncondensing
- Power – 117 VAC ±10% at 60 Hz ±1 Hz single phase,  
1-1/2 amps



Above – Paper Tape Reader  
Below – Punch and Power Supply

### Paper Tape Reader and Punch

The Model 4512 paper tape reader and punch combination consists of the Model 4511 or 4513 paper tape reader and a 110 characters per second Teletype punch. The punch is a separate unit, normally mounted in the top of a MODCOMP system cabinet to provide convenient access for changing paper tape. The punch has a separate controller mounted in a Peripheral Controller Interface enclosure.

The Model 4512 operates with MODCOMP I, II and III computers.

All specifications and descriptions given for the Models 4511 and 4513 apply to the paper tape reader in the Models 4512. The additional specifications for the paper tape punch are given below.

## **PUNCH Specifications**

Punching Speed – 110 CPS  
Tape Reel Capacity – 835 feet of 4.5 mil tape  
Tape – 1 inch, oiled black paper tape  
Dimensions – 15-3/4 inches high, 19 inches wide,  
18 inches deep

## **Environmental Requirements**

Operating temperature – 0°C to 50°C ambient  
Relative humidity – 10% to 90% noncondensing  
Power – 117 VAC  $\pm$ 10%, 60 Hz  $\pm$ 1 Hz single phase,  
2 amps

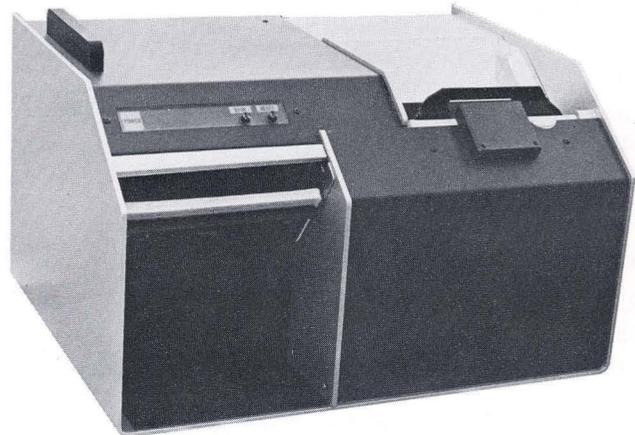
## CARD READERS AND PUNCHES



### Available Units

A choice of two card readers and two card punches, one with interpreting capability is available with MODCOMP systems:

Model		Speed cards/minute
4411	Card Reader	300
4412	Card Reader	1,000
4421	Card Punch	100 - 400
4425	Keypunch/On Line Card Punch	35 - 60
4426	Keypunch/On Line Card Punch/ Automatic Interpreter	35 - 60



300 CPM Card Reader

### Model 4411 Card Reader

The Model 4411 Card Reader is a compact, reliable unit which reads standard 80 column punched cards photoelectrically at speeds up to 300 cards per minute. Its vacuum picker mechanism handles cards gently and smoothly to reduce card wear and facilitates the reading of worn and well used cards.

The card reader can read either binary or Hollerith (IBM 029) card codes. The Hollerith code is translated to an eight-bit code in the controller before being transferred to the computer.

The card reader incorporates extensive self checking and error checking features for reliable, error free reading over a wide range of environmental conditions. It can be operated up to fifteen feet away from the controller which is located in the Peripheral Controller Interface.

#### Specifications

- Reading Rate — 300 cards per minute
- Card Type — 80 column cards (EIA Standard RS-292, January 1964)
- Coding — 12 bit or 8 bit translate code upon command
- Hopper Capacity — 600 cards
- Stacker Capacity — 600 cards
- Card Feeding Mechanism — Vacuum picker
- Cable Length — 15 feet
- Reader Dimensions — 12-1/2 inches high, 23 inches wide, 14 inches deep
- Weight — 68 pounds
- Environmental Conditions:
  - Operating Temperature — 32° to 125°F
  - Relative Humidity — 30% to 90%

- Power Requirements — 115 VAC ( $\pm 10$  VAC), 60 Hz  $\pm 3$  Hz Single Phase
- Starting Current — 9 amps
- Run Current — 3.5 amps

### Model 4412 Card Reader

The Model 4412 Card Reader is an extremely reliable unit which reads standard 80 column punched cards photoelectrically at speeds up to 1,000 cards per minute. It has been specifically designed for a high tolerance to mutilated, warped, and edge damaged cards. Its vacuum picker mechanism handles cards gently and smoothly to reduce card wear and facilitate the reading of worn and well used cards.

This unit has the same code handling, program control and error checking features as the Model 4411 Card Reader.

#### Specifications

- Reading Rate — 1,000 cards per minute
- Card Type — 80 column cards (EIA Standard RS-292, January 1964)
- Coding — 12 bit or 8 bit translate code upon command
- Hopper Capacity — 1,000 cards
- Stacker Capacity — 1,000 cards
- Card Feeding Mechanism — Vacuum picker
- Cable Length — 15 feet
- Reader Dimensions — 13-1/2 inches high, 23 inches wide, 18 inches deep
- Weight — 86 pounds

#### Environmental Conditions:

Operating Temperature — 32° to 125°F

Relative Humidity — 30% to 90%

Power Requirements: — 115 VAC ( $\pm 10$  VAC), 60 Hz  
 $\pm 3$  Hz Single Phase  
Starting Current — 10 amps  
Run Current — 4.5 amps

## Model 4421 Card Punch

The Model 4421 Card Punch can punch 80-column cards at the variable rate of 100 cards per minute for 80 columns and up to 400 cards per minute for 1-8 columns.

A dual punching head mechanism significantly reduces operating times by punching two columns simultaneously. A punch check detects any errors made during the current punching operation. Detection of an error sets an indicator which may be tested by the program. The error card is offset-stacked in the output stacker for quick identification as a rejected card.

### Specifications

Hopper Capacity: 1,200 cards  
Stacker Capacity: 1,300 cards  
Cards: Industry-standard 80-column cards  
Interface Cable: 50 feet (maximum)  
Physical Dimensions: 42 inches high, 44 inches wide, and 30 inches deep  
Weight: Approximately 735 pounds  
Input Power Requirements: Voltage: 120/208 VAC  $\pm 10\%$   
Frequency: 60 Hz  $\pm 1/2$  Hz  
(50 Hz Optional)  
Phase: Three Phase  
Current: 5.0, 7.5, and 8.0 amperes per phase  
Service Connections: Four-wire plus ground

Environmental Conditions: Temperature: 60° to 90°F  
(15.5 to 32°C)  
Relative Humidity: 20% to 80%

Controls/Indicators: Controls: POWER ON/OFF, START, STOP and RUNOUT  
Indicators: CYCLE, PUNCH, TRANSPORT, CARDS, INPUT, CHIPS, RE-CHECK, and AUXILIARY

## Models 4425 and 4426 Keypunch/On Line Card Punch

These flexible units enable standard 80-column cards to be punched either off line by an operator or on line connected to a MODCOMP computer. The two units are the same, except that the Model 4426 prints the punched characters at the top of each column.

All information is stored in a magnetic core memory prior to being punched. This feature permits verifying and error correcting to be accomplished in one card pass when the unit is used as a conventional off-line keypunch.

The unit is capable of punching binary or Hollerith coded cards. Characters to be punched in Hollerith can be sent to the controller in either ASCII or MODCOMP translate code for hardware translation to Hollerith. Program selection of the three translate/punch modes is provided.

### Specifications — Model 4425 (VP and Model 4426 (VIP)

#### Cards

Standard 80-column, round or corner cut

#### Card Processing Stations

Input hopper, auxiliary input, read station, advance station, punch station, print mechanism, select stack, output stacker

#### Punching Methods

Two columns at a time

#### Punching Speed (VP)

35 CPM maximum

#### Punching Speed (VIP)

60 CPM when column 22 (or less) is the last column punched

42 CPM when column 50 is the last column punched

35 CPM when column 80 is the last column punched

#### Reading Method

Fibre-optic read station

#### Verifying Speed\* (VIP)

60 CPM maximum

#### Verifying Speed\* (VIP)

Without printing: 60 CPM maximum

With printing: 60 CPM when column 35 (or less) is the last column verified

40 CPM when column 75 (or more) is the last column verified

#### Input Hopper Capacity

600 words

#### Auxiliary Input Capacity

1 card

#### Output Stacker Capacity

600 cards

#### Select Stacker Capacity

20 cards

\*When the VP or VIP is converted to a reader-punch, the read rate is the same as the verify rate.

### Physical Characteristics

Width: 38 inches

Height: 39-1/2 inches

Depth: 39 inches

Depth of Desk Top: 14-1/2 inches minimum,  
18-1/2 inches maximum

Height of Desk Top: 27 inches

Weight: VP: Approximately 275 pounds

VIP: Approximately 325 pounds

### Power Requirements

Nominal Voltage: 120 VAC

Nominal Frequency: 60 Hz \*

Phases and Lines: Single phase, 3 wire

Nominal Load: VP: 400W

VIP: 500W

Heat Dissipation: VP: 1400 BTU per hour

VIP: 1700 BTU per hour

\*50 Hz models available.

## HIGH SPEED PRINTERS

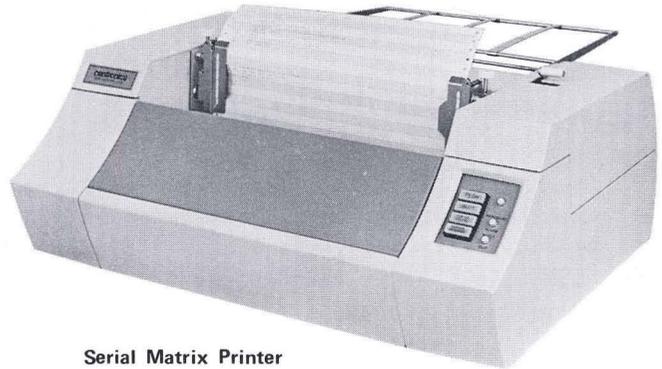


### Line Printers

Model 4211 – 600 LPM

Model 4214 – 300 LPM

The Model 4211 and 4214 Line Printers provide high speed printing capability to the MODCOMP computer family.



Serial Matrix Printer

### Hardware Features

- Vertical Format Control
- Variable Form Width
- Data Buffering
- Paper Storage and Printout Stacking
- Self-Test System for off-line adjustment

The tape controlled vertical format unit is standard on both units and provides maximum flexibility in form control and in data formatting.

These printers are buffered and are capable of accepting data at a maximum rate of 20 KHz. The line printer enclosure provides a number of convenience features like paper storage and printout stacking.

These printers contain standard self-test systems which provide the capability for off-line adjustment and maintenance without interfering with the rest of the computer system.

The line printer controller occupies a half plane in the Peripheral Controller Interface unit.



600 LPM Line Printer

### Performance Specifications

Line Speed – 600 lines per minute – Model 4211  
300 lines per minute – Model 4214

Line Spacing – 6 lines/inch

Character Spacing – 10 characters/inch

Number of Columns – 132 columns/line

Vertical format unit – 8 channel

Form width – Model 4211 – 3-1/2 to 19-1/2 inches  
Model 4214 – 19-1/2 inches

## Physical Characteristics

### Dimensions and Weights

Models 4211 and 4214 — 44 in. high, 36 in. wide,  
34 in. deep, 600 lbs.

### Environmental Requirements

Operating temperature — 32° to 120°F

Relative Humidity — 10% to 90%

Power — 117 VAC ±10%, 60 Hz ±1 Hz Single Phase,  
7 amps

## Serial Matrix Printer

The Model 4213 matrix printer provides the MODCOMP computer family with an economical, buffered, line printing capability. The printing rate is 60 lines per minute on full, 132 character lines, and up to 150 lines per minute on short lines.

## Hardware Features

- Pin Feed Form Handling
- Variable Form Width
- Single Line Buffering
- Vertical Format Control
- Audio Alarm

The single line buffer is capable of accepting data from the MODCOMP computers at a parallel data rate of up to 75,000 characters per second.

The vertical format control feature provides “top of form” movement under control of an instruction received from the control unit. Vertical line spacing is 6 lines per inch.

The audio alarm alerts the operator of an out of paper condition or paper handling malfunction.

The basic character set of the Model 4213 is USASCII compatible. This character set consists of 10 numeric digits (0 through 9), 26 upper case letters (A through Z) and 26 special characters including the FORTRAN character set.

## Controls and Indicators

Stop-Start Switch — Lighted in the ON position

Top of Form Switch — Manual slewing to top of form or proper location of the Vertical Format Control tape when installing forms

Select Switch — Selects printer after turning on power

Forms Override — Operator override on paper out switch. This allows the operator to complete the form which was being printed before changing paper.

## Performance Specifications

Speed — Variable, 60 LPM to 150 LPM

Line Spacing — 6 lines/inch

Character Spacing — 10 characters/inch

Number of Columns — 132 columns/line

Vertical Format — 2 channels

Paper Width — 4 inches to 14-1/2 inch form

Dimensions — 27-1/2 inches wide, 11-1/4 inches high,  
19-1/4 inches deep

Weight — 155 pounds

Environmental — Temperature 40°F to 100°F  
Humidity 0% to 95%

Electrical Requirements — 117 VAC ±10%, 60 Hz  
— 600 watts

## MAGNETIC TAPE UNITS



## Magnetic Tape Systems

Model 4148/4151 – 9 track

Model 4149/4152 – 7 track

The Models 4148 and 4149 provide economical, IBM compatible 7 and 9 track magnetic tape capability for data storage and program entry.

The model 4148 includes a controller for up to four tape drives and a 9 track tape drive.

The model 4149 includes a controller for up to four tape drives and a 7 track tape drive.

## Hardware Features

- Up to four magnetic tape units can share a single controller
- The four magnetic tape units can be any combination of 7 and 9 track units.
- Tape speed of 45 IPS with a density of 800 BPI.
- CRC character generation.
- Single capstan drive with a velocity servo system
- System cabinet included

## Program Selectable Operations

- Format (7 track) – Binary or interchange
- Parity (7 track) – Odd or even
- Density (7 track) – 556 or 800 BPI

- Read Forward
- Write Forward
- Write End of File
- Space Forward/Reverse, Record/File
- Rewind
- Select Transport

## Status Available

- Data Overflow
- Device Parity Error
- Device Inoperable
- Memory Parity Error
- File Protect
- Tape Detect
- Controller Busy
- Data Ready
- End of Tape
- End of File
- Beginning of Tape
- Device Offline or Rewinding
- Partial Word

## Performance Specifications

<u>Model</u>	<u>Tracks</u>	<u>Density</u>	<u>Transfer Rate (ch/sec)</u>
4151	9	800	36 KHz
4152	7	556,800	25.02 KHz, 36 KHz

Tape velocity – 45 IPS

Recording mode – NRZI IBM compatible

Tape – Computer grade, 0.5 inch wide, 1.5 mil thick

Rewind speed – 150 IPS

Reel size – 10-1/2 inches

Dimensions – 24" high, 19" wide, 11" deep

Weight – 100 pounds

Environmental Requirements – 40°F to 90°F  
Operating Temperature

Environmental Requirements:

Operating Temperature – 40°F to 90°F

Relative Humidity – 15% to 95% non-condensing

Power Requirements – 117 VAC  $\pm 10\%$ , 60 Hz  $\pm 2$  Hz  
500 watts

## Low Speed Magnetic Tapes

Model 4160 – 9 track

Model 4162 – 7 track

These magnetic tapes provide low speed, IBM compatible magnetic tape medium for use with MODCOMP computers. These tapes are program compatible with the 45 IPS in the Modular peripheral line.

## Performance Specifications

<u>Model</u>	<u>Tracks</u>	<u>Density</u>	<u>Transfer Rate (ch/sec)</u>
4160	9	800	10 KHz
4162	7	556,800	6.95 KHz, 10 KHz

Tape Velocity – 12.5 IPS

Recording mode – NRZI compatible

Tape – Computer grade 0.5 inch wide, 1.5 mil thick

Reel size – 10-1/2 inch

## FIXED HEAD DISC



## Fixed Head Disc

Fixed Head Disc subsystems with a storage capacity ranging from 131,072 words on the Model 4102 to 2,097,152 words on the Model 4107 are available with the MODCOMP computer family.

The Fixed Head Disc Controller included with each disc operates one disc unit with up to 16,384 addressable sectors. Each sector contains 128 sixteen bit words. The controller is connected to MODCOMP computers by means of a Direct Memory Processor channel which provides automatic block transfer capability between the computer memory and disc.

### Hardware Features

- A logical record may be a portion of a sector or may consist of any number of contiguous sectors up to the total unit capacity.
- Record size is controlled by the word count of the DMP channel or the End of Record indicator in the Read Command. Therefore data from either one sector or multiple sectors can be transferred by a single block transfer operation.
- Write Lock Out is provided to prevent writing to any contiguous number of tracks starting from track 0. A panel of eight manual switches may be used to select the number of the highest locked-out track. An additional 3-way switch allows overriding the setting of the eight switches and either permits or locks out all the tracks for Write Command.
- Automatic Head Switching is provided to automatically increment the head address when an origin mark is encountered during write or read operation.

### Performance Specifications

Number of tracks – 32 to 512  
Sectors per track – 32  
Words per sector – 128  
Transfer rate (nominal) – 235,520 words/sec  
Average latency time – 8.7 msec.

Model Number	Number of Tracks	Capacity in Words
4102	32	131,072
4103	64	262,144
4108	96	393,216
4104	128	524,288
4106	256	1,048,576
4107	512	2,097,152

### Physical Characteristics

Power Requirements: 115 VAC  $\pm$  10%, single phase  
– 50 or 60 Hz  $\pm$  3%  
Start Current – 2.5 amp  
Run Current – 0.6 amp

#### Environmental:

Temperature – 32°F - 110°F  
Relative Humidity – 5% to 95%

#### Weights:

Model 4102 thru 4106 – 100 pounds  
Model 4107 – 140 pounds

## MOVING HEAD DISCS



### Moving Head Disc - Extended Capacity

Model 4132/4133 — 12.5 million word capacity

Model 4134/4135 — 25 million word capacity

The Model 4132 and 4134 disc subsystems provide for high storage capacity at high transfer rates. The Model 4132 includes a controller for up to four disc drives. Up to three Model 4133 disc drives can be added to the Model 4132 for a total storage capacity of 50 million words. The Model 4134 includes a controller for up to four disc drives. Up to three Model 4135 disc drives can be added to the Model 4134 for a total storage capacity of 100 million words.

The moving head disc controller is connected to MOD-COMP computers by means of a Direct Memory Processor channel which provides automatic block transfer capability between the computer memory and disc.

### Hardware Features

- The Models 4132 and 4134 provide for overlapping seeks and automatic sector and head switching.
- A logical record may be a portion of a sector or may consist of any number of contiguous sectors up to the capacity limit of a cylinder.
- Record size is controlled by the word count of the DMP channel. Therefore data from either one sector or multiple sectors on the same track can be transferred by a single block transfer operation.
- Indicators for End of Record, End of Device and End of File are provided to aid in file organization.
- Eight words of buffering are provided by the controller to insure fast transfer rate.
- Write Lock Out is provided to insure cylinder protection. A panel of eight manual switches may be used to inhibit writing from cylinder zero to any cylinder up to 255.



Model 4133 Moving Head Disc



Model 4127 Cartridge Disc

## Performance Specifications

	Models 4132-4133	Models 4134-4135
Bit density	2200 BPI	2200 BPI
Tracks per disc pack	4060	8120
Tracks per cylinder	20	20
Cylinders per disc pack	203	406
Sectors per track	24	24
16 bit words per sector	128	128
Transfer rate — words/sec.	156,000	156,000
Words per disc pack	12,472,320	24,944,640
Medium	IBM 2316 type disc pack	IBM 2316 type disc pack
Average rotational latency	12.5 msec	12.5 msec
Maximum head positioning times:		
• Single cylinder	10 msec	10 msec
• Average	32 msec	32 msec
• 200 cylinders	60 msec	60 msec

## Physical Characteristics

### Power Requirements:

- Voltage — 208 VAC,  $\pm 10\%$ , 3 phase
- Frequency — 60 Hz  $\pm 10\%$
- Current — Starting 30 amps — Running 6 amps

### Environment:

- Temperature — 60° - 90°F
- Relative Humidity — 8 - 80%
- Cooling supplied — 68 CFM  $\pm 5\%$
- Heat dissipation — 2700 BTU/hour

## Moving Head Disc- Replaceable Cartridge

Model 4126/4127 — 1,299,200 words capacity

Model 4128/4129 — 2,598,400 words capacity

The Model 4126 and 4128 disc subsystems provide an economical storage capacity at high transfer rates.

The Model 4126 includes a controller for one to four disc drives and one disc drive. From one to three Model 4127 disc drives can be added to the Model 4126.

The Model 4128 includes a controller for two or four disc drives and two disc drives, one of which is removable by the operator. The Model 4129 also contains two disc drives, one of which is removable by the operator. One Model 4129 dual disc drive can be connected to the controller included in the Model 4128. The moving head disc controller is connected to MODCOMP computers by means

of a Direct Memory Processor channel to provide automatic block transfer capability between the computer memory and disc.

## Hardware Features

- Data from either a single sector or multiple sectors on the same track can be transferred by a single block transfer operation.
- A checksum is recorded and checked with each sector to provide a reliable means of error detection.
- Write Lock Out is provided to insure track protection. The switch panel provided with the disc may be used to inhibit writing on any track starting with Track 0 and up to Track 63.
- Indicators on the front panel of the disc to notify status conditions such as Power ON, Cartridge Loaded, Disc Ready and Error Indication.

## Performance Specifications

	Models 4126-4127	Models 4128-4129
Rotational speed	1,500 RPM $\pm 1\%$	1,500 RPM $\pm 1\%$
Average latency time	20 msec	20 msec
Head positioning times		
Maximum track to track	15 msec	15 msec
Average	70 msec	70 msec
Tracks	406	812
Sectors per track	32	32
Words per sector	100	100
Data addressability	Track and Sector	Track and Sector
Transfer rate — words/sec	97,800	97,800

## Physical Characteristics

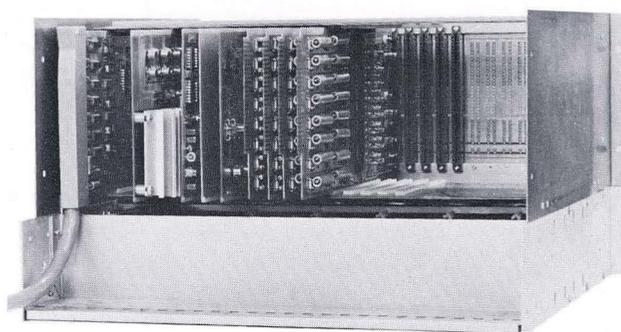
Dimensions:	Width	x	Depth	x	Height
Model 4126	19"		22-7/8"		10-1/2"
Model 4127	19"		22-7/8"		7"
Model 4128	19"		22-7/8"		17-1/2"
Model 4129	19"		22-7/8"		14"

Power Requirements — 117 VAC  $\pm 10\%$ , 60 Hz  $\pm 1$  Hz  
single phase, 5 amps

### Environment:

- Temperature — 60° - 90°F
- Relative Humidity — 8 - 80%

## HIGH LEVEL ANALOG INPUT SUBSYSTEM



High Level Analog Input Subsystem showing enclosure with the MOSFET multiplexer gate cards and input filters on the right and power supplies in the bottom.

## General Description

Model 1200 Single-Ended Inputs

Model 1500 Differential Inputs

The High Level Analog Input Subsystem (HLAIS) provides the capability for economical and highly flexible analog signal multiplexing when used with the MODCOMP computer family. The basic enclosure houses the entire subsystem. The subsystem provides the capability of selecting, either randomly or sequentially from 16 to 128 high level single-ended inputs or 8 to 128 differential inputs and digitizing the channel analog values to an 11 bit plus sign digital value at a rate up to 50,000 channel per second.

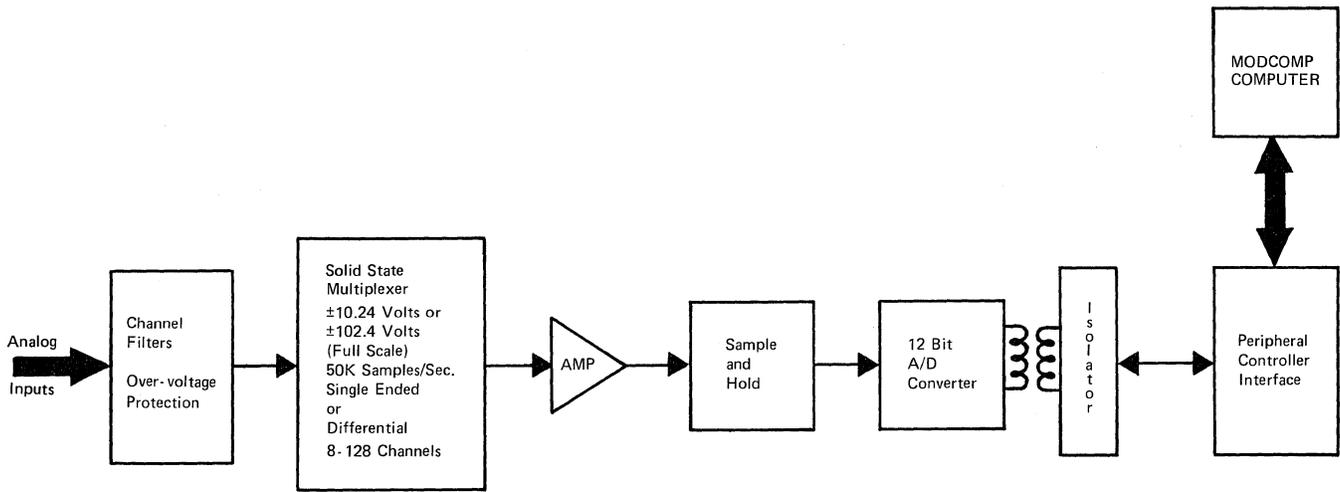
## Subsystem Features

- Multiplexer Filter Module — Plugs into filter module and provides for various input options
- Signal Bandwidth Control — Single pole R-C filters provide a wide variety of signal bandwidth limiting
- Single Ended or Differential Inputs — Provides optional single ended or differential multiplexing capability
- Signal Attenuation Capability — Precision attenuators extend signal range from  $\pm 10.24$  volts full scale to  $\pm 102.4$  volts full scale

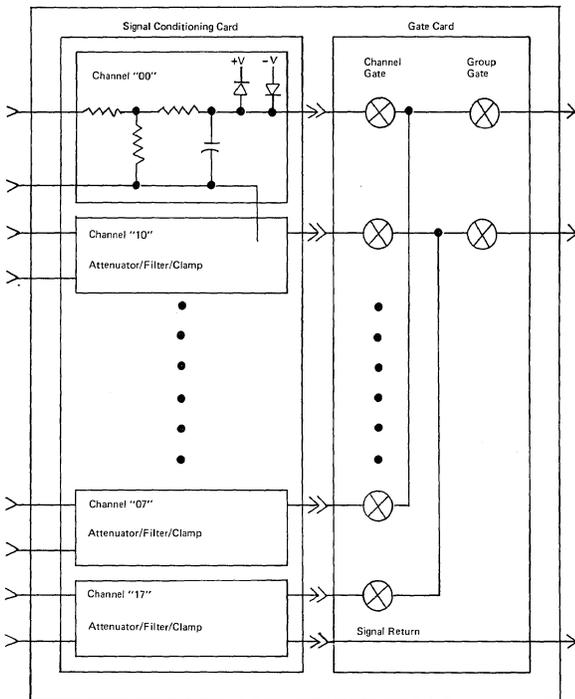
- Overvoltage Clamps — Inputs are clamped to  $\pm 12$  volts to provide for overvoltage protection up to  $\pm 24$  volts
- Fused Inputs — Unattenuated inputs are fused to prevent catastrophic failure in the event of excessive overvoltage ( $\pm 65V$  peak will blow the fuse)
- MOSFET Gate Switches — Provides excellent signal to control line isolation and automatic signal disconnect in the event of power failure
- Fully Wired Backplane — Multiplexer is field expandable up to 128 channels by adding multiplexer modules.
- Differential Sample and Hold — High input impedance and common mode rejection capability by providing a common analog signal return (single-ended). Allows the next channel to be selected while previous channel is being converted thereby increasing throughput rates. Aperture time less than 100 nanoseconds.
- Successive Approximation A/D Converter — High conversion accuracy at high conversion speed.
- Transformer Coupled Interface — Digital interface and analog measuring sections of subsystem are transformer isolated, providing complete isolation of the analog and digital systems.

## Functional Description

The HLAIS consists of five functional units. These are the random access high level analog multiplexer, the subsystem timing and control, the differential sample and hold amplifier, the successive approximation analog-to-digital converter and the isolation interface.



High Level Analog Input Subsystem



Multiplexer Module

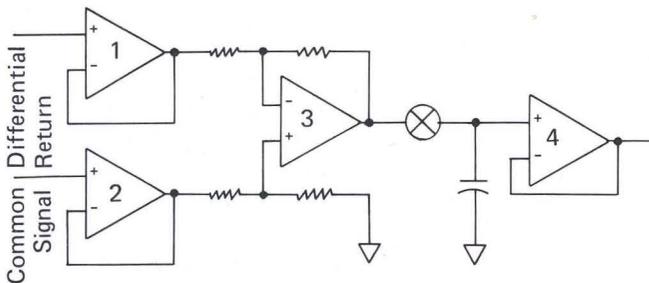
### Analog Multiplexer

Analog input signals from up to 128 transducers or other high level sources can be interfaced to the HLAIS. Signal connection to the multiplexer is made through printed circuit card, edge type connectors in the multiplexer. Analog inputs in the range of  $\pm 10.24$  volts or  $\pm 102.4$  volts full scale are accepted depending upon the multiplexer module used. The multiplexer module consists of a signal conditioner card and a gate card. The multiplexer module accepts 16 single ended input signals or 8 differential signals. The input signals are subdivided into 16 groups of 8 signals each. The signal conditioner card provides for input signal filtering and/or attenuation and over-voltage protection. Each input line is diode protected against a non-damaging overvoltage level of up to  $\pm 24$  volts in the case of the non-attenuated  $\pm 10.24$  input range and  $\pm 200$  volts for the attenuated  $\pm 102.4$  input range.

The gate card performs analog switching by using P-channel, enhancement mode MOSFET gates. Two levels of analog switching are used in order to minimize channel-to-channel crosstalk and also to minimize distributed capacitance tied to the analog bus. The first level switch selects one channel out of eight on every switch module. The second level switch selects one of two groups on the addressed multiplexer module (one of eight). This sequence of switch closures places the selected analog signal at the input to the high input impedance differential sample and hold amplifier.

**Differential Sample and Hold Amplifier** — This amplifier presents a high input impedance to the signal source and also provides an improved sampling aperture for the analog-to-digital conversion. It also allows time interlacing of successive multiplexer channels which improves total system throughput rate. The sample and hold function is accomplished by a configuration of four general purpose operational amplifiers. The two input amplifiers (AMPS 1 & 2, See Figure) are connected as unity gain non-inverting (potentiometric) amplifiers. This provides the signal source a differential input with very high input impedance. The low side of the signal sources are connected together at the input to AMP 2 in single-ended systems.

This feature of common differential signal return provides common mode rejection capability in situations where there is a potential difference between the signal source reference and the Analog Subsystem reference. Amplifier 3 converts the differential input to a single ended signal and references this signal to the AIS ground. Amplifier 4 buffers the sampling gate and the holding capacitor. Once the analog signal has been sampled and the AIS is in the hold state, the digitizing of the analog sample begins.



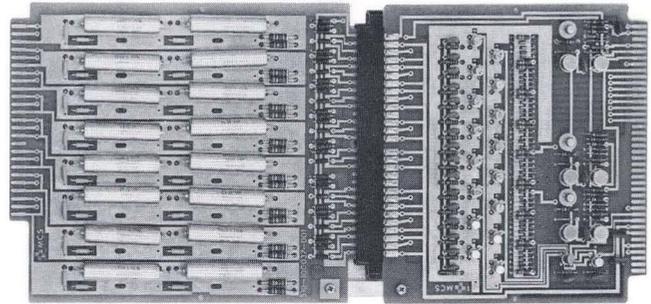
Differential sample and hold amplifier

**Analog-to-Digital Converter** — This unit is a moderate-speed successive approximation device that digitizes the sampled analog signal into an 11 bit plus sign binary value in 15 microseconds. The ADC serial data output, which is in 2's complement format, is transformer coupled to the Isolation Interface to await transfer which is a function of the controller located in a Peripheral Controller Interface enclosure.

**Isolation Interface** — This interface permits the HLAIS subsystem reference plane to be returned to the total system ground reference point independently from the digital system ground bus structure. The transformer-coupled serial transfer scheme allows the HLAIS to be located at distances up to 100 feet from the controller.

**Subsystem Timing and Control** — The control logic contains a channel address register which stores each channel address as it is received from the computer. Once the

address has been received, address decoding logic proceeds to close the MOSFET gate of the selected channel. Channel selection may be sequential or defined by the channel address supplied to the AIS from the MODCOMP computer.



High level MOSFET multiplexer gate card capable of handling 16 single-ended or 8 differential analog inputs.

## Programming

In any particular system configuration the AIS Subsystem is capable of being used with either the Register Input/Output Subsystems or with the Direct Memory Processor (DMP) capabilities of the MODCOMP computers. Two DMP channels, one for channel addresses and one for data values, are used to provide 50 KHz random sampling, conversion and computer input. Single word program controlled transfers can be used for operation at asynchronous or program controlled rates.

## Performance Specifications

Input Type — Single ended (Model 1200) or differential (Model 1500)

Channel Capacity — 128 channels expandable in 16 channel increments (Model 1200) or 8 channel increments (Model 1500)

Input Ranges —  $\pm 10.24$  volts full scale  
—  $\pm 102.4$  volts full scale with optional precision attenuators.

Input Filters — 8 ranges — 3db cut-off frequencies from 14.8 Hz to 14.8 KHz

Input Impedance —  $20 \text{ M}\Omega$  shunted by  $\frac{3 \times 10^3}{S} \text{ M}\Omega \text{ max}$

Where S = Sample rate

Source Impedance —  $1 \text{ K}\Omega \text{ Max}$

Sample Rate – 50,000 samples/sec.  
Overall Subsystem Accuracy –  $\pm 0.05\% \pm 1/2$  LSB  
Subsystem Noise – 0.01% F.S. peak (3 Sigma; D.C. to  
    subsystem bandwidth)  
Subsystem Zero Offset – 0.11% F.S.  
Subsystem Gain Accuracy – 0.014% F.S.  
Subsystem Linearity – 0.011% F.S.  
Resolution – 12 bits binary including sign  
Digital Interface – Interfaces with MODCOMP I/O Bus  
and DMP via a controller located in a Peripheral Controller  
Interface.

## Physical Characteristics

### Size and Packaging

The High Level Analog Input Subsystem is designed for mounting in equipment cabinets which have standard 19" rails. It occupies 10-1/2" of rack panel height and is 18" deep.

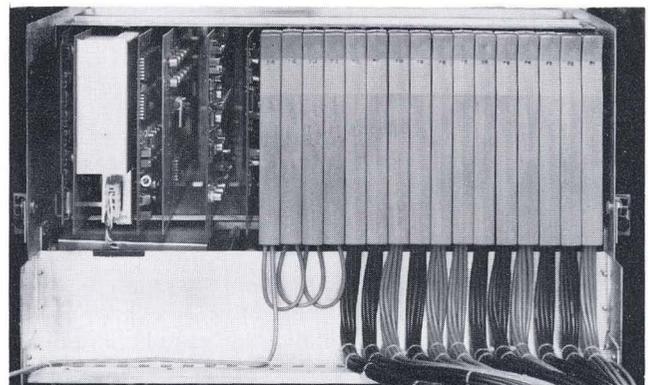
### Power and Environmental

The power requirements are: 120 VAC  $\pm 10\%$ , 2.5 AMP at 50-60 HZ  $\pm 2$  Hz

Ambient Temperature Range: 0-55°C

Ambient Relative Humidity Range: 10-90% non-condensing

# WIDE RANGE ANALOG INPUT SUBSYSTEM Model 1300 - Solid State Multiplexer



Wide Range Solid State Analog Input Subsystem showing eight-channel analog gate cards on the right. The card file is wired for a total of 128 channels.

## General Description

The Wide Range Analog Input Subsystem (AIS 1300) provides a capability for economical highly flexible bipolar analog signal multiplexing when used with the MODCOMP computer family.

The subsystem accepts up to 512 differential analog inputs in groups of eight channels.

Programmed or automatic gain ranging from a gain of 1 to a gain of 2048 in 12 binary increments give the AIS 1300 a full scale measurement capability from  $\pm 5\text{Mv}$  to  $\pm 10.24\text{V}$ . This wide dynamic range allows the AIS 1300 to satisfy application requirements in which either low level analog signals with a wide dynamic range must be sampled and digitized or a wide variety of transducer types must be accommodated.

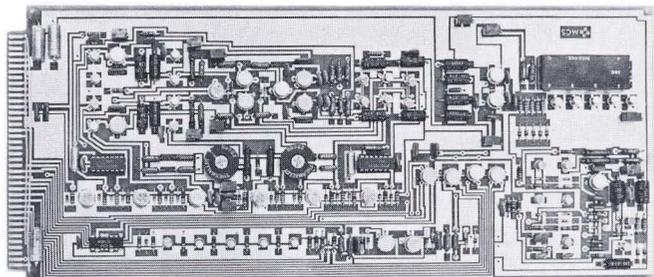
The dynamic signal range of the AIS can be further increased by the addition of a zero suppression capability. This function provides an eight to one offset to signal suppression ratio with suppression resolution of 15 bits including sign.

A choice of seven different R.C. single pole or seven different R.C. double pole filter configurations provide any necessary signal bandwidth limiting.

## Subsystem Features

- Signal Bandpass Control — R-C single pole and double pole filter input conditioners.
- Input Voltage Clamps — Inputs are clamped  $\pm 12$  volts to provide for overvoltage protection.

- Fused Input Capability — For additional protection in the event of an excessive overvoltage condition.
- Excellent Channel-to-Channel Crosstalk Rejection — Contributes to high over-all system accuracy.
- P Channel, Enhancement Mode MOSFET Gate Switches — Provides for excellent control line/signal isolation and signal source automatic disconnect in the event of power failure.
- Full Backplane Wiring — Multiplexer is field expandable up to 512 channels by adding expander units and multiplexer modules.
- High Common-Mode Rejection — 120 db DC to 60 Hz at gains of 128 or greater.
- Zero Suppression Capability — Provides an eight to one offset to signal suppression ratio.
- Programmable/Automatic Gain Ranging — Wide dynamic signal range measurement.

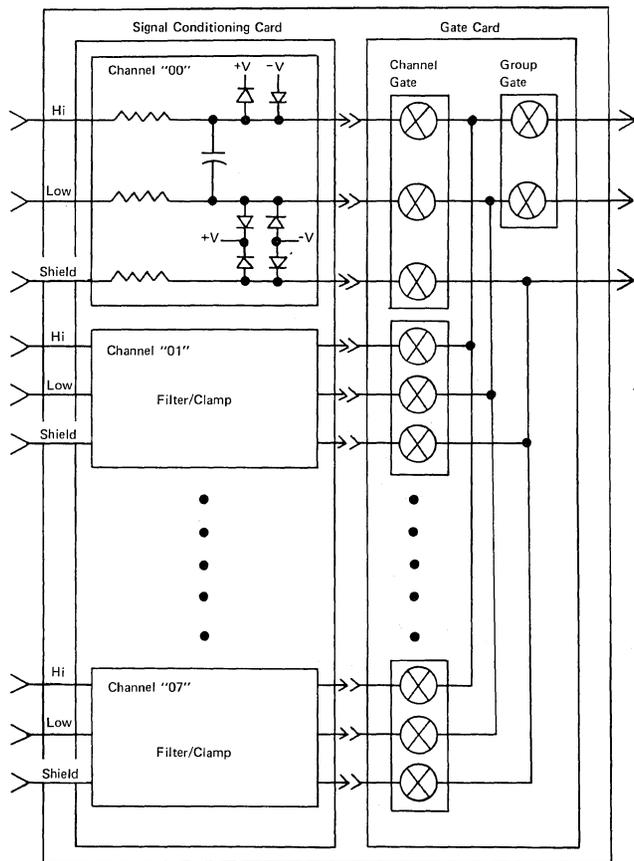


Wide Range Amplifier Card with auto-gain-ranging as well as program-selectable gain and zero suppression capabilities.

- Driven Guard — Increases common mode input impedance.
- Sample and Hold Amplifier — Allows next channel to be selected while previous channel is being converted thereby increasing throughput rates. Aperture time less than 100 nanoseconds.
- Successive Approximation Encoder — High conversion accuracy at high conversion speed.
- Double Buffered Output — Output data is available for readout 95% of the time.
- Transformer Coupled Interface — Complete d-c isolation of the analog and digital systems.

## Functional Description

The high performance wide range AIS 1300 (Block Diagram) includes the random access, wide range, guarded differential multiplexer, the subsystem timing and control, the wide range amplifier, the sample and hold amplifier, the successive approximation analog-to-digital converter and the isolation interface.



Multiplexer Module

**Multiplexer** — A wide range of bipolar analog input signals from up to 512 transducers or other signal sources can be interfaced to the AIS 1300. Signal connection to the multiplexer is made through printed circuit card edge type connectors in the multiplexer. Analog signal input ranges from  $\pm 5$  millivolts to  $\pm 10.24$  volts full scale are conditioned and switched into a switchable gain, wide range differential amplifier by the multiplexer modules. The multiplexer module consists of a signal conditioner card and a gate card. A multiplexer module accepts eight differential signal inputs. The signal conditioner card provides for input signal filtering and over-voltage protection. Each input signal is diode protected against a non-damaging over-voltage level of up to  $\pm 24$  volts.

The multiplexer module utilizes two levels of signal switching. The gate card performs this analog switching through use of P-Channel, enhancement mode MOSFET Gates. Two levels of analog signal switching are used in order to minimize channel-to-channel crosstalk and also to minimize differential distributed capacitance tied to the analog bus. The first level switch selects one channel out of eight on the multiplexer module. The second level switch selects the addressed multiplexer module (one of sixteen). This sequence of switch closures places the selected analog signal at the input to the differential wide range amplifier.

**Wide Range Amplifier** — The differential wide range amplifier output signal level is optimized to provide maximum resolution of the digitized data. One of twelve amplifier gains can be selected either under control of the program (Programmed Gain Ranging) or the AIS (Automatic Gain Ranging). When automatic gain ranging is selected the AIS automatically selects the highest gain level which does not produce overflow in the 12-bit converted value.

**Differential Sample and Hold Amplifier** — This amplifier receives the analog data from the wide range amplifier. It provides an improved sampling aperture for the analog-to-digital conversion. It also allows time interlacing of successive multiplexer channels which improves total system throughput rate. The sample and hold function is accomplished by a configuration of four general purpose operational amplifiers.

**Analog-to-Digital Converter** — The converter utilized in the AIS is a moderate speed successive approximation device that digitizes the sampled analog signal into an 11 bit plus sign binary value in 15 microseconds. The ADC is a self contained unit in that it houses all the required control logic, timing circuits and reference supplies required for functional operation. The ADC serial data output, which is in 2's complement format, is transformer coupled across the Isolation Interface to await transfer into the computer.

**Isolation Interface** — This subsystem function provides all the necessary requirements for the interconnection of the AIS and the MODCOMP computers. The distinctive feature of this system function is the complete trans-

former coupling of all control, address, and data lines. This permits the AIS 1300 subsystem reference plane to be returned to the total system ground reference point independently from the digital system ground bus structure.

**Subsystem Timing and Control** – A channel address-gain register stores each address-gain word as it is received from the computer. Once received, this information is decoded to close the MOSFET gate of the selected channel and to set the gain of the wide range amplifier. An internal timing chain controls the selection, sampling and digitizing cycle of the AIS. When operating in the automatic gain ranging mode, the subsystem timing and control function operates in conjunction with the comparator circuitry of the wide range amplifier to optimize the amplifier gain setting.

## Performance Specifications

Input Type – Guarded, differential (3 wire)  
 Channel Capacity – 512 channels, expandable in 8 channel increments.  
 Input ranges – 12 programmable –  $\pm 5\text{mv}$ ,  $\pm 10\text{ mv}$ ,  $\pm 20\text{mv}$ ,  $\pm 40\text{mv}$ ,  $\pm 80\text{mv}$ ,  $\pm 160\text{mv}$ ,  $\pm 320\text{mv}$ ,  $\pm 640\text{mv}$ ,  $\pm 1.28\text{V}$ ,  $\pm 2.56\text{V}$ ,  $\pm 5.12$  and  $\pm 10.24\text{V}$  full scale.

Maximum Inputs –  $\pm 10\text{V}$  peak common mode  
 $\pm 12\text{V}$  peak signal plus common mode  
 $\pm 24\text{V}$  peak overvoltage

Input Filters – 7 ranges – 3 db cut-off frequencies from 2.8 Hz to 740 Hz.

Differential Source Impedance – 1K ohm maximum

Common Mode Source Impedance – 1.0 megohm maximum

Common Mode Rejection – 120 db DC to 60 Hz

Overall System Accuracy –  $\pm 0.05\%$   $\pm 1/2$  LSB

Sample and Hold Aperture – 100 nanosec. maximum

Resolution – 12 bits binary including sign

System Throughput Rate:

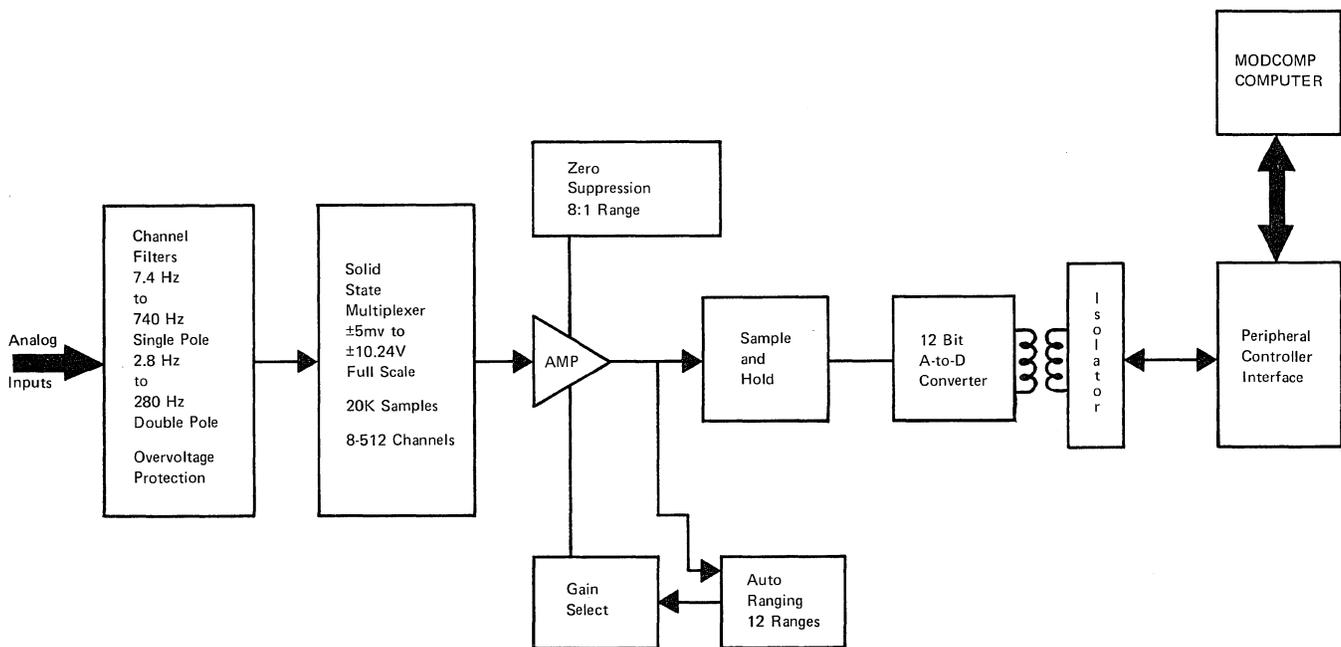
Standard – 20 KHz

Zero Suppression – 10 KHz

Auto Ranging – 6 KHz

Zero Suppression – 8 to 1 full scale suppression to full scale signal ratio capability with 14 bit plus sign digital to analog converter

Digital Interface – Interfaces directly with the MOD-COMP I/O bus via a controller located in a Peripheral Controller Interface enclosure



Block Diagram – Wide Range Solid State Analog Input Subsystem

## Physical Characteristics

### Size and Packaging

The Wide Range Solid State Subsystem is designed for mounting in equipment cabinets which have standard 19" rails. The rack mountable enclosure is 10-1/2" high and 17" deep.

Each unit has a capacity of 128 channels, therefore for a full complement of 512 channels, the subsystem will contain three expander units in addition to the basic

chassis. Expander units have the same physical size as the basic units.

### Power and Environmental

The power requirements are 120 VAC  $\pm 10\%$ , 2.5 A for the basic subsystem (128 channels) and 2 AMPS for each additional expander unit.

Frequency — 50 to 60 Hz  $\pm 2$  Hz

Ambient Temperature Range — 0 - 55°C

Ambient Humidity Range — 10 - 90% non-condensing

# WIDE RANGE RELAY ANALOG INPUT SUBSYSTEM Model 1400 - Relay Multiplexer



## General Description

The Wide Range Relay Analog Input Subsystem (AIS 1400) provides a capability for economical highly flexible bipolar analog signal multiplexing when used with the MODCOMP computer family.

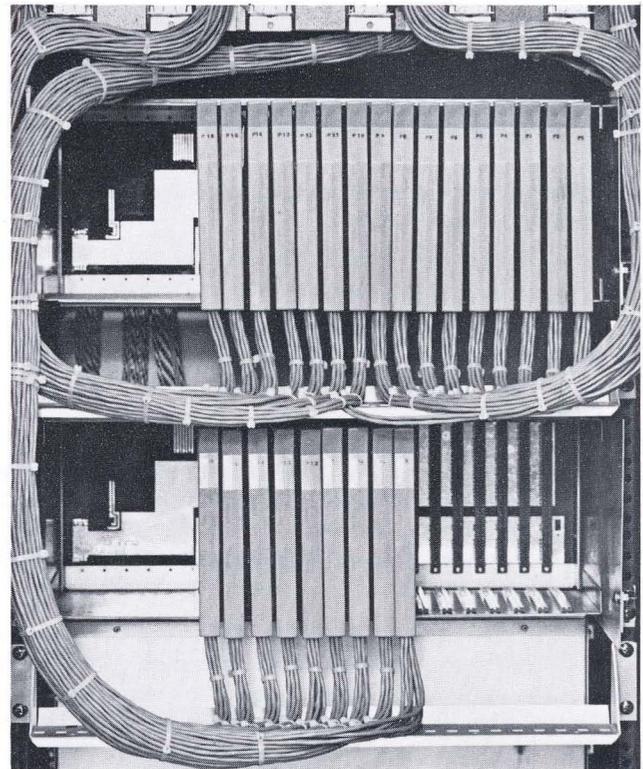
The subsystem accepts up to 512 differential analog inputs in groups of eight channels. Programmed or automatic gain ranging from a gain of 1 to a gain of 2048 in 12 binary increments gives the AIS 1400 a full scale measurement capability from  $\pm 5\text{Mv}$  to  $\pm 10.24\text{V}$ . This wide dynamic range allows the AIS 1400 to satisfy application requirements in which either low level analog signals with a wide dynamic range can be sampled and digitized or a wide variety of transducer types must be accommodated.

The resolution of the AIS can be further increased by the addition of a zero suppression capability. This function provides an eight to one offset to signal suppression ratio with suppression resolution of 15 bits including sign.

A choice of seven different R-C single pole filter configurations provide any necessary signal bandwidth limiting.

## Subsystem Features

- Mercury Wetted Contact Relays — High reliability, excellent switching characteristics maintained for greater than 10 billion operations.



Multiplexer gate cards. Up to 16 cards can be contained per chassis.

- Filter/Attenuator Options — Single pole R-C filters or 128 volt attenuators optional.
- Overvoltage Protection — Differential input is clamped to  $\pm 12$  volts to provide sustained overvoltage protection up to  $\pm 30$  volts. An automatic channel disconnect is provided above this level extending this protection up to  $\pm 200$  volts peak.
- Fully Wired Back Plane — Multiplexer is field expandable up to 512 channels by adding multiplexer modules and expander files for each group of 128 channels.
- High Common Mode Voltage Capability — Accepts input signals at common mode voltages up to  $\pm 200$  volts peak.
- Wide Dynamic Range — 12 programmable binary gain ranges from  $\pm 5\text{ Mv}$  to  $\pm 10.24\text{V}$ .
- Auto-Ranging — Program selectable auto-ranging mode on a per channel basis provides automatic gain selection for optimum measuring resolution.

- Zero Suppression Capability — Programmable eight to one offset to signal suppression ratio, with suppression resolutions of 15 bits including sign.
- Integrating Analog to Digital Converter — Provides increased common mode rejection by integrating resultant normal mode line frequency noise over one or more full cycles. Scan rate options 5, 12.5, 15, 25, 30 and 100 samples/sec.
- Saturation Detection — Wide Range Amplifier over-ranging is detected and transmitted back to the computer, indicating the resultant data value, after integration, is invalid.

## Functional Description

The Wide Range Relay Analog Input Subsystem consists of six functional elements:

- Differential Guarded Relay Multiplexer
- Differential Wide Range Amplifier
- Integrating Analog to Digital Converter
- Address Decode
- Isolation Interface
- A.I.S. Controller

**Differential Guarded Relay Multiplexer** — A wide range of bipolar analog input signals from up to 512 transducers can be interfaced to the AIS 1400. Signal connection to the multiplexer is made through printed circuit card edge type connectors.

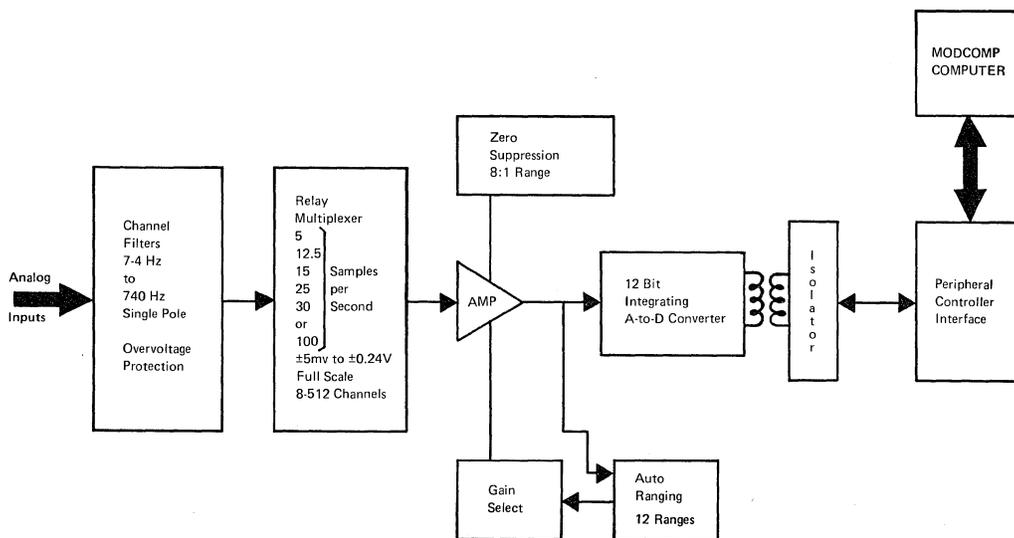
The multiplexer accepts inputs in the range of  $\pm 5\text{Mv}$  to  $\pm 10.24\text{V}$  full scale. Optional input attenuators (100 to 1) extend the differential input upper limit to  $\pm 128$  volts full scale. The input ranges then become  $\pm 500$  Mv to  $\pm 128$  V full scale. Seven single pole R-C input filter options are also available with cut-off frequencies which range from 7.4 Hz to 740 Hz. A differential overvoltage

of  $\pm 30$  volts can be sustained on all channels simultaneously without damage. To provide additional protection, for extreme overvoltage, an automatic channel disconnect feature is provided which enables those channels without input filters to sustain overvoltage up to  $\pm 200$  volts peak.

The multiplexer module utilizes three levels of signal switching. The gate card performs analog switching through use of mercury wetted relay switches. Three levels of analog signal switching are used to minimize channel-to-channel crosstalk and also to minimize differential distributed capacitance tied to the analog bus. The first level switch selects one channel out of eight on the multiplexer module. The second level switch selects the addressed multiplexer module (one of eight). The third level switching is performed by the Sub-Multiplexer Module which selects one of eight groups, each group consisting of 64 channels.

**Differential Wide Range Amplifier** — This unit accepts the output of the Sub-Multiplexer and provides 12 programmable binary gain ranges from unity to 2048. Gain selection and analog clamp control is provided via the Address Decode module. In the autorange mode, a voltage comparator on the output of the amplifier determines if the output signal level is less than  $\pm 3/8$  full scale. If less than this level, the gain counter in the Isolation Interface is allowed to step to the next highest gain. This process is repeated until the output is greater than  $+ 3/8$  full scale or maximum gain is reached.

The Zero Suppression option provides for an eight to one offset to full scale signal, suppression capability. This is accomplished by loading a 15 bit data word into a Digital To Analog converter, the output of the D/A is then applied to the input of the Post Amplifier section of the Wide Range Amplifier to null out the equivalent input offset voltage. This allows the gain of the amplifier ahead of the Post Amplifier to be increased by a factor



Block Diagram — Wide Range Relay Analog Input Subsystem

of 8 over that range on which the offset was measured. The overall resolution in measuring offset plus signal then becomes 15 bits including sign.

When the Resistance Check feature is employed, a one milliamp current source, balanced with respect to the guard bus, is applied to the selected channel. The resultant voltage drop is then measured in the same way as the signal input, with the binary resistance ranges becoming 5 ohms to 10240 ohms in 12 ranges.

**Integrating Analog To Digital Converter** — This unit accepts the output of the Wide Range Amplifier for conversion into digital data. The ADC also contains the timing and control for the multiplexer and provides six optional scan rates of 5, 12.5, 15, 25, 20 and 100 samples per second. At scan rates below 100 samples/sec. increased common mode rejection is realized by the integration of the resultant normal mode power frequency noise over one or more full cycles. A considerable reduction in amplifier noise is also achieved at all sample rates by this integration process providing "referred to input" noise levels of less than 5  $\mu$ V peak on the  $\pm 5$  mV range.

The amplified data is converted into an 11 bit plus sign binary value by means of a double integration technique which makes the digitized value virtually independent of integrating capacitor variations. The 12 bits of data, together with the 4 bits of gain information, is transmitted back to the AIS Controller via the Isolation Interface.

**Isolation Interface** — This unit accepts serial address, gain, mode and suppression data from the controller and sends back to the controller the magnitude and gain data received from the A/D converter. All data and control signals to or from the Isolation Interface are transformer coupled to provide common mode isolation, and also transmitted and received by differential driver and receivers so that the AIS Controller can be located up to 100 feet from the subsystem.

**AIS Controller** — This unit provides all the necessary requirements for interfacing the AIS 1400 to the MODCOMP I/O bus. This includes cable drivers and receivers and associated controller logic to provide Register I/O under test and transfer or interrupt control.

**Programming** — The Wide Range Relay AIS is a moderate speed device and therefore is program controlled on a single word basis. The program transfers to the AIS a single command word containing the desired channel address and gain value, unless the automatic gain ranging mode has been selected. After the designated analog channel value has been sampled and converted, a computer interrupt is generated. The digitized channel value (and gain if auto-ranging) can then be transferred into the computer. If interrupt operation is not desired, the program can test the AIS to determine when the digitized

channel value is available for input. When zero suppression is used, a second output command word is used to specify the offset value.

## Performance Specifications

- Input Type — Guarded, differential (3 wire)
- Channel Capacity — 128 channel basic, with 128 channels per expander chassis, expandable up to 512 channels in 8 channel increments.
- Input Ranges — 12 programmable —  $\pm 5$ mv,  $\pm 10$ mv,  $\pm 20$ mv,  $\pm 40$ mv,  $\pm 80$ mv,  $\pm 160$ mv,  $\pm 320$ mv,  $\pm 640$  mv,  $\pm 1.28$ V,  $\pm 2.56$ V,  $\pm 5.12$ V and  $\pm 10.24$ V Full Scale.
- Maximum Input Signal plus Common Mode Voltage —  $\pm 200$ V peak operating
- Channel to Channel Common Mode Voltage — 200V peak operating (500V on special order)
- Signal —  $\pm 12$ V peak operating ( $\pm 150$ V with input attenuator)
- Signal Overvoltage — 30V peak on all channels simultaneously without damage (200V peak on no filter options)
- Input Filters — Single pole R-C filters with cut-off frequencies from 7.4 to 740 Hz.
- Differential Source Impedance — 1K ohms maximum
- Common Mode Rejection — 110 db maximum
- Overall System Accuracy —  $\pm 0.05\%$   $\pm 1/2$  LSB or  $\pm 5$ uv
- Resolution — 12 bits binary including sign
- Scan Rates — 5, 12.5, 15, 25, 30 and 100 samples/second.
- Zero Suppression Option — 8-to-1 full scale suppression to full scale signal ratio capability. Resolution of 15 bits binary including sign.
- Digital Interface — The wide range relay AIS interfaces with the MODCOMP I/O bus via the AIS controller.

## Physical Characteristics

### Size and Packaging

The Wide Range Relay AIS is designed for mounting in a standard 19" rack. The basic chassis occupies 21" of rack panel height including power supplies and cables and is 18" deep.

Each expander chassis requires 10-1/2" of rack panel height.

### Power and Environmental

The power required is 120 VAC  $\pm 10\%$ , 2.5A 50-60 Hz  $\pm 2$  Hz  
Ambient Temperature Range — 0-55°C  
Ambient Relative Humidity Range — 10-90%  
non-condensing

# MODAC

## Modular Data Acquisition Subsystem



## Features

The MODAC subsystem provides a low cost data acquisition and control capability for system applications which require small to moderate quantities of:

- Analog Inputs
- Analog Outputs
- Digital Inputs
- Digital Outputs

The MODAC subsystem interfaces directly to the MODCOMP I and MODCOMP II computers.

## General Description

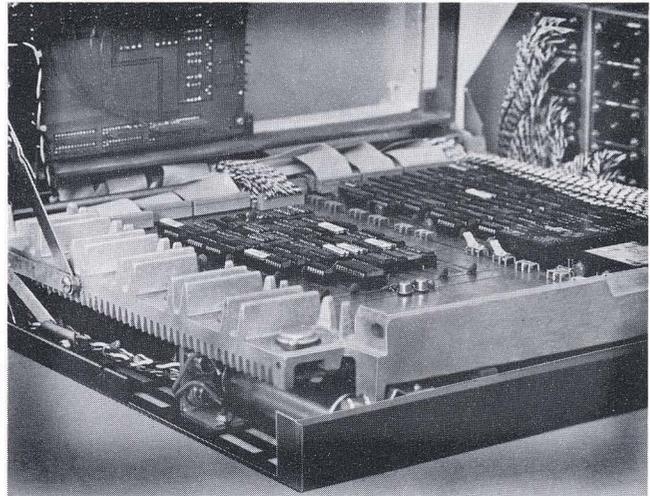
The MODAC subsystem consists of the Model 1601 MODAC subsystem controller and enclosure and six types of input/output interface modules:

- Model 1605 Analog Input Module
- Model 161X Analog Output Module
- Model 16XX Analog Output Module
- Model 162X Digital Dual Word Input Module
- Model 163X Digital Dual Word Output Module
- Model 166X I/O Interrupt Extender Module, where X is assigned specific numerical values to designate specific signal conditioning.

The MODAC package can contain up to four hinged planes. The controller and each interface module occupy one-half plane. Therefore up to seven interface modules can be connected to the controller on the four planes. Any combination of interface modules can be connected to the controller.

The basic MODAC subsystem includes unregulated power supplies, fans and one half-plane, on which the controller is mounted. The subsystem is expanded to a full complement of seven interface modules by adding plane castings with power regulator assemblies as required. A maximum of three planes can be added to the MODAC subsystem.

User connection to the MODAC subsystem is through 106 pin AMP connectors mounted on the rear panel. One connector per interface module is provided.



MODAC Subsystem. Each analog or digital interface module occupies one half plane. The subsystem can be expanded to a full complement of seven interface modules.

## Physical Characteristics

The packaging format employed is similar to that of the MODCOMP I computer. The subsystem is 8.75" in height and is completely self-contained with respect to power and cabling.

### Weight, Power and Environmental

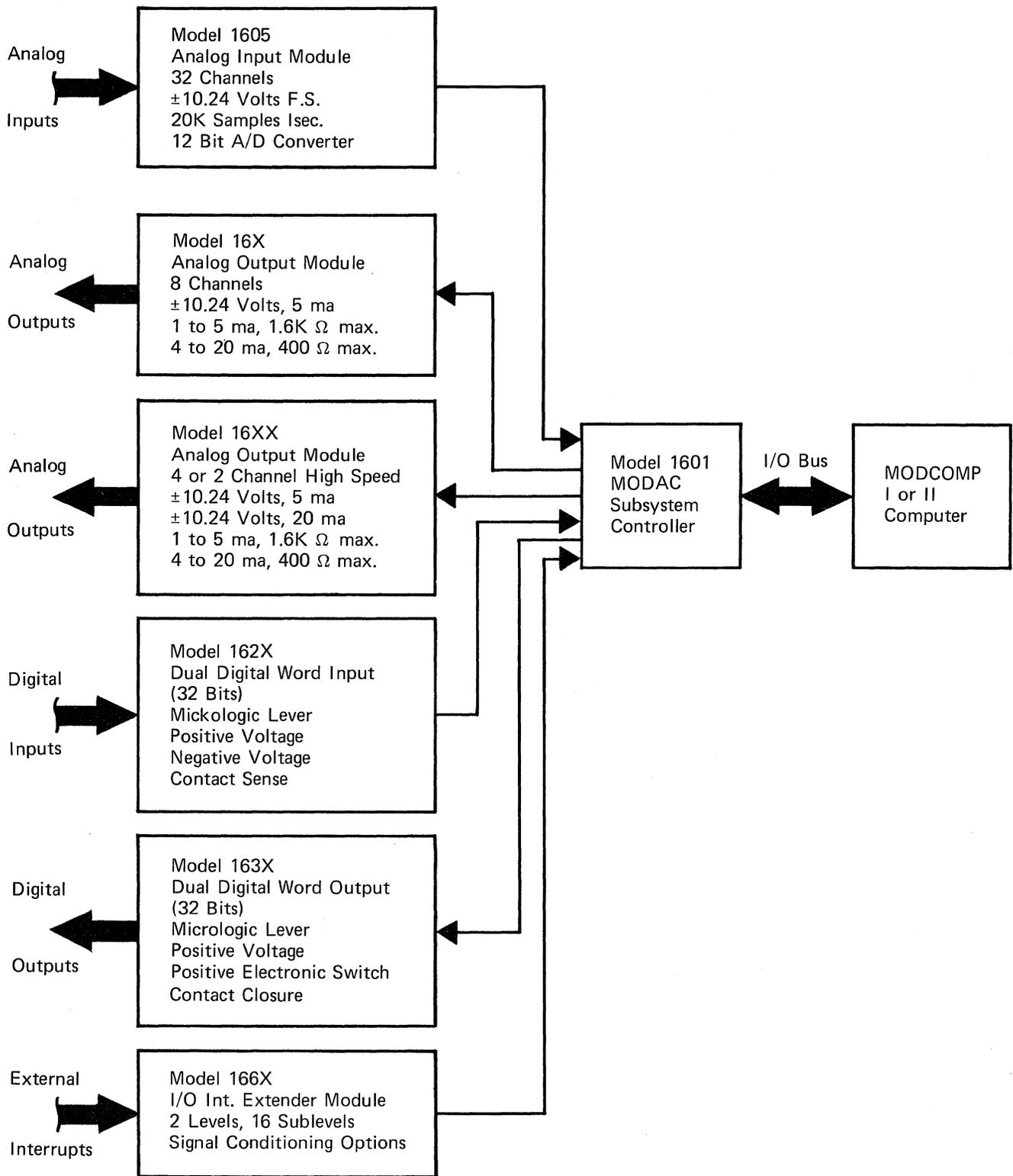
A full MODAC subsystem weighs 70 pounds. The power requirements are 120 VAC  $\pm 10\%$  at 58 to 62 Hz. The power dissipation of a full MODAC subsystem is 600 watts.

The MODAC subsystem is designed for the following ambient environments:

OPERATING TEMPERATURE — 0 to 55°C

RELATIVE HUMIDITY — 10 to 90%, non-condensing

Interface module descriptions for those modules available with the MODAC subsystem are included below.



MODAC Subsystem Block Diagram

# Model 1605 Analog Input Module

## Functional Description

The Analog Input Module (AIM) accepts up to 32 channels, with input signals of  $\pm 10.24$  volts full scale. These signals are multiplexed into a sample and hold, with an aperture of approximately 100 nanoseconds, and a 12 bit (including sign) successive approximation Analog to Digital Converter. The maximum throughput rate is 20 KHz. Sequential address selection capability is provided. Digitized channel values can be read into the computer under single-word program control or blocks of channel values can be transferred in on an automatic cycle stealing basis if the MODCOMP computer contains the optional

Direct Memory Processor. More than one AIM can share the same DMP channel, if only one of the modules is permitted to be active at a time.

## Multiplexer Specifications (@ 25°C unless otherwise specified)

Analog Inputs: Single ended  
Channel Capacity: 32 channels  
Input Signal Range:  $\pm 10.24$  volts full scale  
Input Voltage:  $\pm$  volts maximum  
Source Impedance: 1 K  $\Omega$  maximum  
Sample Rate: 20K samples/sec./maximum  
Input Filter: Single pole R-C;  
fco = 340 KHz ( $\pm 20\%$ )  
Input Impedance: 20M ohm shunted by  $\frac{5 \times 10^3}{S}$  M ohm  
where S = Sample Rate

Multiplexer: Channel to Channel Offset  
Offset  $\leq \pm 1$  mv

Drift =  $(1 + \frac{R_s}{1K}) \times 90$  uV/°C Maximum  
where  $R_s$  – Signal source resistance

Crosstalk (D.C. to 1 KHz); % of crosstalk signal  
 $(1 + \frac{R_s}{1K}) N [5 \times 10^{-5} + 3 \times 10^{-5} T + 1.5 \times 10^{-6} f_x]$  %

Where  $R_s$  == Source resistance of selected channel  
N == Number of channels with crosstalk signal

Where  $R_s$  = Source resistance of selected channel  
N = Number of channels with crosstalk signal  
T = Temperature differential above 25°C  
fx = Frequency of the crosstalk signal

## Analog to Digital Converter and Sample and Hold Specifications

Resolution: 12 Bits Including Sign  
Sample Time: 23.8 usec.  
Conversion Time: 26.2 usec.  
Aperture Time: 100 nsec.  
Offset:  $\pm 0.01\%$  full scale  
Offset Drift:  $\pm 40$  ppm/°C,  $\pm 0.01\%$ /Day  
Gain:  $\pm 0.025\%$  full scale  
Gain Drift:  $\pm 40$  ppm/°C,  $\pm 0.02\%$ /Month

Linearity:  $\pm 0.025\%$  full scale (straight line between  $\pm$  full scale)

Noise (3 Sigma; D.C. to 1 MHz): 0.02% full Scale Peak

Quantizing Error:  $\pm 1/2$  LSB

# Model 161X Analog Output Module

## General

The Model 161X Analog Output Module provides eight low speed channels for use with the MODAC subsystem. Three different output options are available to enable selection of either voltage or current output.

## Functional Description

The digital to analog converters used in this module employ a pulse averaging technique which provides an economical means of implementing analog outputs where high speed settling times are not required.

The common elements to the eight channels are an output data buffer, channel address decoder, a binary pulse width generator and reference supply.

The binary pulse width generator provides twelve signal lines, namely;  $2^0$  through  $2^{11}$ . Each of these signals consists of a pulse which has a duty cycle weighted in binary from 1/4096 (line  $2^0$ ) to 1/2 (line  $2^{11}$ ). All signals are mutually exclusive so that when logically combined (OR'ed) they produce a pulse with a duty cycle of 4095/4096, which is equivalent to full scale.

Output data is loaded into each of eight D/A registers. Each register bit which is set enables the corresponding pulse train to be applied to an OR gate, the output of which is applied to a FET driver, analog switch and pulse averaging amplifier. Voltage or current outputs are accommodated by selection of the appropriate feedback network. Available output options are:

Model 1610 –  $\pm 10.24$  volts at 5 ma maximum

Model 1611 – 1 to 5 ma into 1.6K ohms maximum

Model 1612 – 4 to 20 ma into 400 ohms maximum

Output settling to within  $\pm 0.02\%$  full scale is less than 80 milliseconds for all options.

## Performance Specifications (@ 25°C unless otherwise specified)

Resolution: 12 Bits Binary Including Sign

Accuracy (% Full Scale)

Zero Offset

Setability –  $\pm 0.01\%$

Drift –  $\pm 40$  ppm/°C,  $\pm 0.02\%$ /Day

Gain Accuracy

Setability @ full scale –  $\pm 0.02\%$

Drift –  $\pm 40$  ppm/°C,  $\pm 0.02\%$ /Month

Linearity:

(Straight line between zero and full scale)  
@ 25°C  $\pm 0.02\%$

Drift —  $\pm 10$  ppm/ $^{\circ}\text{C}$ ,  $\pm 50$  ppm/Month  
Noise (Peak 3 Sigma) — 0.02% full scale d.c.  
to 1 MHz.

**Settling Time:**

80 millisecond maximum to within  $\pm 0.02\%$   
full scale for full scale step input

## Model 16XX Analog Output Module

### General

The Model 16XX Analog Output Interface Module provides four or two high speed channels for use with the MODAC subsystem. Output options are available to enable selection of either voltage or current outputs.

### Functional Description

The Model 16XX Analog Output Interface Module consists of digital-to-analog converters which contain a 12-bit data register, switch drivers, current switches, 12-bit ladder network, output amplifier and reference supplies. Various type voltage and current outputs are available. Available as an option are control signals enabling the DAC's to be used for driving X and Y axis of Tektronix Type 611 and 603 Storage CRT's.

### Performance Specifications (@ 25 $^{\circ}\text{C}$ unless otherwise specified)

Resolution: 12 Bit Binary Including Sign

#### Output Options (4 DAC Modules)

- Model 1615 —  $\pm 10.24$  volts full scale @ 5 ma
- Model 1616 —  $\pm 10.24$  volts full scale @ 20 ma
- Model 1617 —  $\pm 10.24$  volts full scale @ 5 ms with Tektronix 611 storage scope controls
- Model 1618 —  $\pm 10.24$  volts full scale @ 5 ms with Tektronix 603 storage scope controls
- Model 1619 — 1 ma to 5 ma into 1.6K  $\Omega$  max.
- Model 1620 — 4 ma to 20 ma into 400  $\Omega$  max.

#### Output Options (2 DAC Modules)

- Model 1675 —  $\pm 10.24$  volts full scale @ 5 ma
- Model 1676 —  $\pm 10.24$  volts full scale @ 20 ma
- Model 1677 —  $\pm 10.24$  volts full scale with Teletronix 611 storage scope controls
- Model 1678 —  $\pm 10.24$  volts full scale with Teletronix 603 storage scope controls

#### Accuracy (% Full Scale)

##### Zero Offset

- Setability —  $\pm 0.01\%$
- Drift —  $\pm 25$  ppm/ $^{\circ}\text{C}$ ,  $\pm 0.01\%$ /Day

##### Gain Accuracy

- Setability @ full scale —  $\pm 0.02\%$
- Drift —  $\pm 30$  ppm/ $^{\circ}\text{C}$ ,  $\pm 0.02\%$ /Month

##### Linearity:

- (Straight line between  $\pm$  full scale): @ 25 $^{\circ}\text{C}$   
 $\pm 0.025\%$
- Drift =  $\pm 10$  ppm/ $^{\circ}\text{C}$ ,  $\pm 50$  ppm/Month

#### Settling Time:

(Full Load; CL = 0.01  $\mu\text{F}$ ): 15 usec. to settle  
to within  $\pm 0.02\%$  of final value for a full scale  
step

D/A Switching Transient: 3V for 2 usec.

#### Digital Outputs (CRT Controls):

##### Output Levels

- One =  $\pm 5\text{V}$  thru 1K resistive pull up
- Zero =  $-5\text{V}$  to  $-4.3\text{V}$  for Tektronix 611
- Zero = 0 to  $\pm 0.4\text{V}$  for Tektronix 603
- Low Level Sink : 20 ma maximum

For 603 and 611 storage scopes the Z axis output is normally at the zero level (blanked). Unblanking occurs 15 usec. after leading edge of channel Y strobe and has a pulse width of 10 usec.

## Model 162X Dual Digital Word Input Module

### General

The Dual Digital Word Input Module provides 32 bits of digital inputs which are transferred to the computer in two words of 16 bits each. Several signal conditioning options are available as an integral part of the input channels. Any option selected is provided for all 32 bits of the input channels.

Input signal conditioning options are shown in the table below.

### Functional Description

Each input (2 words — 16 bits each) drives a single-ended line receiver thru a current limiting resistor. The inputs are diode clamped for over-voltage protection.

As optional features, each dual input module can be provided with the synchronization option and/or the interrupt option.

The synchronizer option provides each of the input channels with a "transfer request" input which enables the computer program to input a channel value based on the receipt of an external request signal.

The interrupt option provides each of the input channels with I/O data and service interrupt control which enables the external device to interrupt the computer and request a transfer.

## Model 163X Dual Digital Word Output Module

### General

The Dual Digital Word Output Module provides 32 bits of digital outputs which are transferred to the computer in two words of 16 bits each. Several signal conditioning options are available as an integral part of the output channels and are specified at the time of subsystem configuration. Any option selected is provided for all 32 bits of the output channels.

Dual Word Input Options	Logic "1" (Vin 1)	Logic "0" (Vin 0)	Maximum Overvoltage
Model 1621 TTL/DTL Logic Level	+2.8 to +15V IL = -0.25 ma max.	0 to +0.7V at 2.8 ma max.	±60V Peak
Model 1622 Positive Voltage	+11.5 to +60V at 4 ma max.	-60 to +3.5V at -4 ma max.	±170V Peak
Model 1623 Contact Sense	Contact Closed 0 to +1V at -1 ma max.	Open Contact Vin (Min) = +7.5V	±170V Peak
Model 1624 Negative Voltage	-11.5 to -60V at -4 ma max.	+60 to -3.5V at 4 ma max.	±170V Peak

### Functional Descriptions

Each discrete output (2 words – 16 bits each) line is provided from a different driving element depending on the signal conditioning option selected.

As optional features, each dual output module can be provided with the synchronization option and/or the interrupt option.

The synchronizer option provides each of the output channels with a "transfer complete" output which signals

the external device that a new data word has been transferred from the computer to the digital word output module.

The interrupt option provides each of the output channels with I/O data and service interrupt control which enables the external device to interrupt the computer and request a transfer.

The output signal conditioning options are shown in the following table:

Dual Word Output Options	Logic "1"	Logic "0"	Output Type
Model 1631 TTL/DTL Logic Level	+2.4V to +5.2V IL = -500 $\mu$ a max.	0V to +0.4V Isink = 20 ma	TTL Totem Pole Output
Model 1632 Positive Voltage	"OFF" +30V max. IL = 100 $\mu$ a max.	"ON" 0V to 0.4V Isink = 300 ma max.	Open Coll. NPN Transistor
Model 1633 Contact Closure (Resistive Load Only)	Contact Closed 0.5A max.	Contact Open 100V max. 10VA Switching max.	1 Form A Relay Contact
Model 1634 Electronic Switch	"ON" 0V to 0.4V Isink = 300 ma max.	"OFF" +30V max. IL = 100 $\mu$ a max.	Open Coll. NPN Transistor

Dual Interrupt Input Options	Logic "1" (Vin 1)	Logic "0" (Vin 0)	Maximum Overvoltage
Model 1651 TTL/DTL Logic Level	+1.8 to +15V at .25 ma max.	0 to +0.8V at -2.8 ma max.	±60V Peak
Model 1652 Positive Voltage	+11.5 to +60V at 4 ma max.	-60 to +2.5V at -4 ma max.	±170V Peak
Model 1653 Contact Sense	Contact Closed 0 to +2V at -1 ma max.	Open Contact Vin (Min) = +7.5V	±170V Peak
Model 1654 Negative Voltage	-11.5 to -60V at -4 ma max.	+60 to -2.5V at 4 ma max.	±170V Peak

## Model 166X I/O Interrupt Extender Module

### General

The I/O Interrupt Extender Module provides the capability of extending the I/O Data and Service Interrupts into 8 additional levels each. Several signal conditioning options are available as an integral part of the input sublevels. These options are shown in the table below.

### Functional Description

All interrupts share the same source ID and priority level within the subsystem.

Each of the 16 interrupt sublevels can be enabled or disabled individually; also each of the 16 request lines can be reset individually under program control.

Any of the eight inputs in each group going true will cause a corresponding interrupt request. The interrupt routine when serviced will perform an Input Status to the device for subsequent software queueing.

I/O Interrupt Extender Input Options	Logic "1" (Vin 1)	Logic "0" (Vin 0)	Maximum Overvoltage
Model 1661 TTL/DTL Logic Level	+1.8 to +15V IL = .25 ma max.	0 to +0.8V at -2.8 ma max.	±60V Peak
Model 1662 Positive Voltage	+11.5 to +60V at 4 ma max.	-60 to +2.5V at -4 ma max.	±170V Peak
Model 1663 Contact Sense	Contact Closed 0 to +1V at -1 ma max.	Open Contact Vin (Min) = 7.5V	±170V Peak
Model 1664 Negative Voltage	-11.5 to -60V at -4 ma max.	+60 to -2.5V at 4 ma max.	±170V Peak

# INPUT/OUTPUT INTERFACE SUBSYSTEM



## Features

- Model 1100 – MODCOMP III
- Model 1199 – MODCOMP I and II

The Input/Output Interface Subsystem (IOIS) provides the MODCOMP computer family with a very flexible capability to input and output real time information. The IOIS offers a wide variety of interface options to provide compatibility with almost any type of measurement and control, or communications equipment such as:

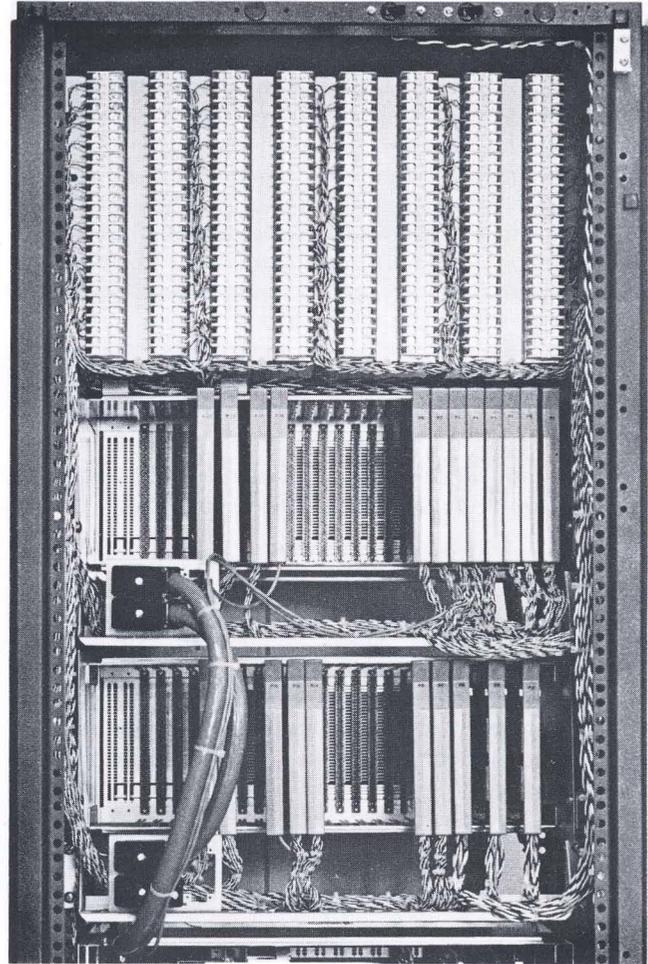
- Digital Outputs
- Digital Inputs
- Analog Outputs
- Communications Channels
- Interval Timers
- Synchronizer Channels
- External and I/O Interrupt Channels

The IOIS is designed to multiplex and scan up to 16,384 input or output lines in groups of 16 lines. It can be dedicated to all input or all output functions or any combination of inputs and outputs in groups of 16 lines per channel.

## Functional Description

In its maximum configuration, the IOIS consists of the basic Subsystem Controller and power supplies, the Channel Multiplexer, the Expander Unit, many types of Interface Channels, the Channel Synchronizer, I/O Interrupt Coupler, External Interrupt Coupler and the Interval Timer.

**Subsystem Controller** – The basic subsystem controller contains the computer I/O bus interface and all the address decode, timing and control logic required by the IOIS. In addition, the enclosure which contains the controller can accommodate up to 16 input or output channels, up to eight communication interfaces in place of up to eight of the I/O interface channels, two external synchronizer cards, two I/O interrupt couplers and one external interrupt coupler.



Input/Output Interface Subsystems (two) showing computer I/O cable in the left center daisy-chained to the two IOIS units. The twisted-pair signal cables are wired to connectors which mate with edge connectors on the front of the input and output channel cards.

**Channel Multiplexer** – This unit in conjunction with the Expander Unit provides for expansion of the basic subsystem. The Multiplexer interfaces the Expander to one of the 16 Channels in the basic subsystem. This channel now becomes a multiplexed channel to provide multiple inputs and/or outputs via one channel. A maximum of four Expander Units (16 Channels each) can be interfaced by one Multiplexer. Up to 16 Multiplexers can be accommodated in the Basic IOIS file. The multiplexer channels may be operated on a sequential scan basis or each of the channels may be accessed randomly.

**Expander** — This unit in conjunction with the channel Multiplexer provides a housing and power supply for expansion of an additional 16 channels to the basic Input/Output Interface Subsystem. Up to sixty-four expanders may be added to the basic subsystem.

**Interface Channels** — The basic types of interface channels which provide signal conditioning and buffering between the computer system and the external equipment are: digital input channel, digital output channel, analog output channel, and communications interface channel. In addition, several types of special channels such as common alarm input, interval timer, and counter input are also available.

The Digital Input Channel accepts a word (16 bits) of digital information for transfer into the computer. The Digital Output Channel provides a word (16 bits) of digital information from the computer to an external device. The Analog Output Channel provides either one or two computer controlled digital-to-analog converters. The Common Alarm Channel produces a computer interrupt signal when any of 16 inputs change state. The computer can then input the 16 bits to determine which bit changed state. The Counter accumulates input pulses. The contents can be read into the computer under program control. The Communications Channel provides one half-duplex communications line interface.

The detailed specifications for the interface channels available appear at the end of this discussion.

**I/O Interrupt Coupler** — The I/O Couplers provide the necessary interface capability required to allow external devices to utilize the two standard I/O party-line interrupts. One coupler allows up to eight external interrupts to use the standard service interrupt party-line. Interface signal conditioning options are the same as available on the digital input channels. A unique memory location is assigned to each party-line interrupt for sub-routine vectoring.

**External Interrupt Coupler** — The interrupt system of the MODCOMP III computer provides a capability of up to 32 interrupt levels, expandable in groups of four levels. The external interrupt coupler of the IOIS provides connection for 16 priority interrupt levels. The outputs of the coupler are directly connected to the priority interrupt inputs at the computer. Interface signal conditioning options are the same as available on the digital input channels.

**Interval Timer** — The Model 1109 Interval Timer Module provides an accurate, programmable time base for task/event scheduling or I/O scan rate control. The interval complete output signal from the timer may be connected to any of the optional interrupt couplers. The time interval is set by outputting a 16 bit word containing the count for the desired interval. Count interval options from 1  $\mu$  second to 50  $\mu$  secs, derived from the computer clock are available, or an external time base may be employed.

**Asynchronous Communication Interface** — These options are available to enable MODCOMP computers to commu-

nicate with asynchronous devices such as Teletypes, CRT terminals and serial printers. Two interface circuits are available, 20 ma current loop or RS-232-C compatible. Up to eight asynchronous interfaces can be supplied in an IOIS.

**Channel Synchronizer** — This functional element of the IOIS provides the necessary control and signal lines required for synchronizing an external device with the Input/Output Interface Subsystem. A "data ready" input is provided to enable data transfers to the computer to be controlled by the external device. A "data transfer" output is provided to inform the external device that a data transfer is occurring. One synchronizer provides signals for eight Interface Channels. Interface signal conditioning options are the same as available on the digital input and output channels. One type of signal conditioning option is permitted per synchronizer card. Two channel synchronizer cards can be accommodated in the IOIS.

**Common Alarm Module** — This module performs essentially the same function as the basic input channel but also provides an output which occurs when any of the 16 inputs change state. This output may be coupled to any of the optional IOIS Interrupt Couplers. The output can be specified to occur on leading edge, trailing edge or on both transitions.

## Physical Characteristics

### Size and Packaging

The basic subsystem and the subsystem channel expanders are packaged in a card file suitable for mounting in a standard 19 inch rack. Each card file occupies 17-1/2 inches of panel space (including power supplies) and is 18 inches deep.

A blower assembly is required in conjunction with the IOIS. This assembly occupies 7 inches of rack panel space.

### Power and Environment

The power required is 120 VAC  $\pm$ 10%, 5A, 50-60 Hz  $\pm$ 2 Hz

Ambient Temperature Range — 0 to 55°C

Ambient Relative Humidity Range — 10 to 90% non-condensing

### Specifications

The specifications of the individual channels and other units available with the IOIS are given below. Each signal condition option applies to all 16 signals (bits) in one channel.

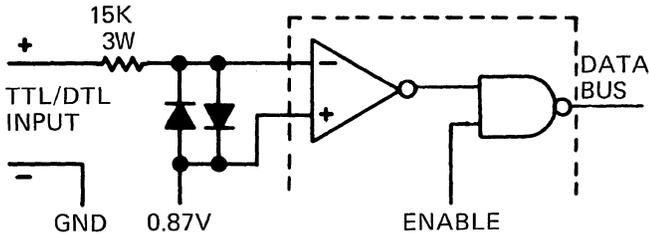
## Digital Input Channels

The specifications for Models 1121-1125 are given below. Modular also offers an unprotected version of these models. This version consists of Models 1126-1129. These models have the same input specifications as models 1121-1125.

## Model 1121 Logic Level Input Option

Each input signal is required to drive a differential line receiver thru a current limiting resistor. The inputs are diode clamped for over-voltage protection (170 volts D.C. or Peak A.C.). The 16 inputs have a common return which is fuse protected.

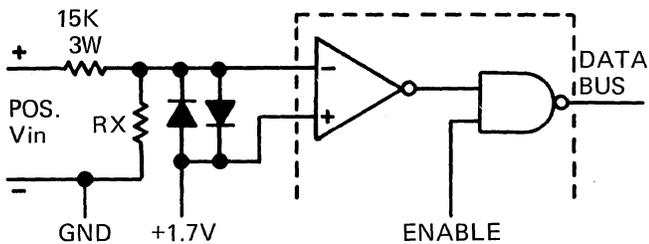
Input Signal Level: Logic ZERO: 0.0V to 0.8V  
(-100  $\mu$ a max.)  
Logic ONE: 2.0V to 5.0V  
(300  $\mu$ a max.)



## Model 1122 Positive Voltage Input Option

Each input signal is required to drive a differential line receiver thru a current limiting resistor. The inputs are diode clamped for over-voltage protection (170 volts D.C. or Peak A.C.). The 16 inputs have a common return which is fuse protected.

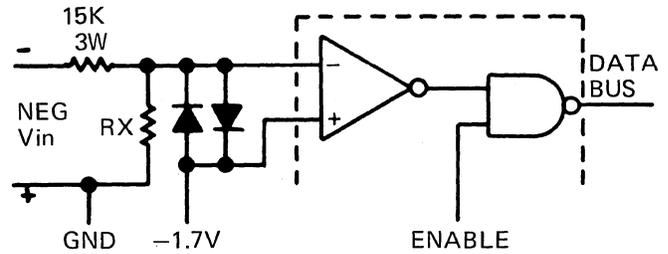
Input Signal Level: Logic ZERO:  $-30 \leq V_{in} \leq 1.5$  volts  
(-2 ma max.)  
Logic ONE:  $3.0 \leq V_{in} \leq 30$  volts  
(2 ma max.)



## Model 1123 Negative Voltage Input Option

Each input signal is required to drive a differential line receiver thru a current limiting resistor. The inputs are diode clamped for over-voltage protection (170 volts D.C. or Peak A.C.). The 16 inputs have a common return which is fuse protected.

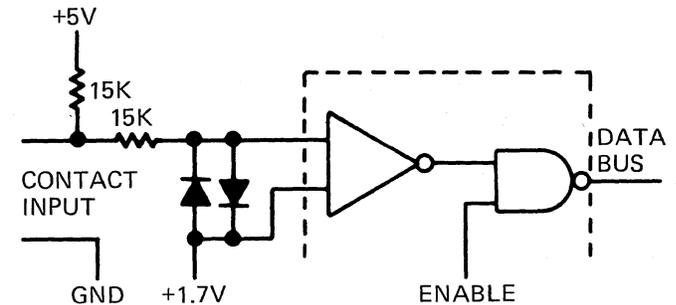
Input Signal Level: Logic ZERO:  $-1.5 \leq V_{in} \leq 30$  volts  
(2 ma max.)  
Logic ONE:  $-30 \leq V_{in} \leq -3.0$  volts  
(-2 ma max.)



## Model 1124 Contact Sense Input Option

An internal power supply produces drive current to a differential line receiver. Each input is required to sink approximately 0.5 ma. The inputs are diode clamped for over-voltage protection (170 VDC or Peak A.C.).

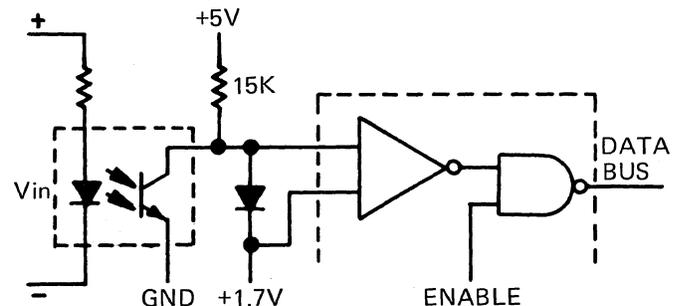
Input Signal: Logic ZERO: Contact Open  
Logic ONE: Contact Closed  
(-500  $\mu$ a max.)



## Model 1125 Isolated Current Input Option

Each input is required to provide current into a light emitting diode (LED). Isolation is achieved by LED - photo-transistor coupling.

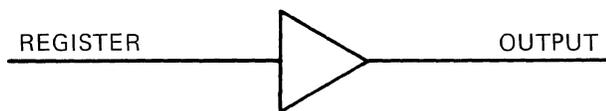
Input Signal Level: Logic ONE: 15 to 25 Volts  
(35 ma max.)  
Logic ZERO: -2 to +1.0 Volts  
(0.5 ma max.)



## Model 1131 Logic Level Output Option

Each discrete output line is provided for a standard TTL inverting element.

Output Signal Level: Logic ZERO:  $0.0 \leq V_{out} \leq 0.4$  volts (-16 ma max.)  
 Logic ONE:  $2.4 \leq V_{out} \leq 5$  volts (0.5 ma max.)

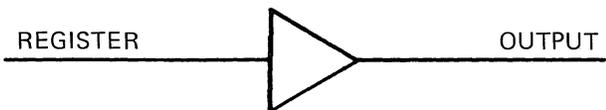


## Model 1132 Positive Voltage Output Option

Each discrete output line is provided from an open collector TTL high voltage driver element.

Output Signal Level: Logic ZERO:  $0.0 \leq V_{out} \leq 0.4$  volts (40 ma max.)  
 Logic ONE: Open Collector

NOTE: Maximum supply voltage = 30 volts

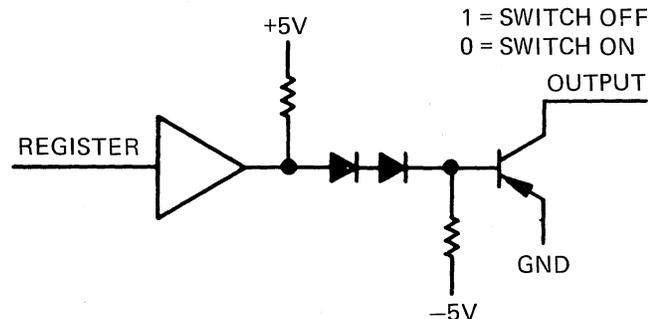


## Model 1133 Negative Voltage Output Option

Each discrete output is provided from a discrete PNP open collector transistor driver.

Output Signal Level: Logic ZERO:  $0.0 \leq V_{out} \leq 0.4$  volts (20 ma max.)  
 Logic ONE: Open Collector

NOTE: Maximum supply voltage = -30 volts

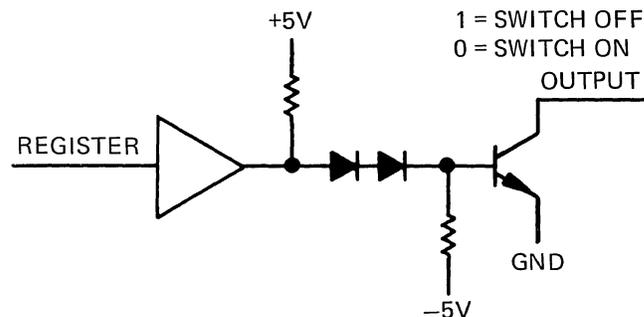


## Model 1134 Electronic Switch Output-Positive Option

Each discrete output is provided from a discrete NPN high current transistor driver.

Output Signal Level: Logic ZERO: Open Collector  
 Logic ONE:  $0.0 \leq V_{out} \leq 0.5$  (150 ma max.)

NOTE: Maximum supply voltage = 50 volts

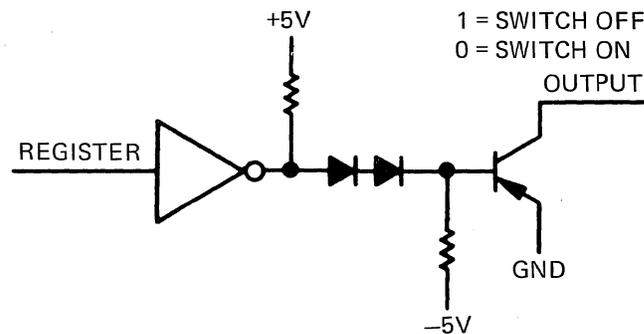


## Model 1135 Electronic Switch Output-Negative Option

Each discrete output is provided from a discrete PNP high current transistor driver.

Output Signal Level: Logic ZERO: Open Collector  
 Logic ONE:  $-0.4 \leq V_{out} \leq 0.0$  Volts (100 ma max.)

NOTE: Maximum supply voltage = -50 volts.

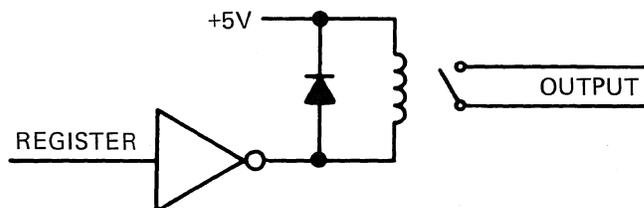


## Model 1136 Contact Closure Output Option

Each discrete output is provided by an isolated reed relay contact.

Output Signal Level: Logic ZERO: Contact Open  
 Logic ONE: Contact Closed

NOTE: Contact Rating  
 100 volts maximum  
 0.5 amps maximum  
 10 volt-amps maximum



## Model 1137 Triac Switch Output Option

The Triac Switch Output Module provides eight isolated AC switch outputs (bits 8 through 16 of digital output word). Each output will handle 3 amps RMS, 60 CPS at up to  $\pm 200$  volts peak.

A zero crossing detector senses the zero crossover of the AC line. The detector outputs are differentiated and applied to the input of a gated 25 KHz oscillator. The pulse bursts of the oscillator are transferred through an isolation transformer to the gate of a bidirectional output triac. This pulse burst technique permits near zero turn on for a wide variety of resistive loads.

## Model 1138 Contact Closure Output Option

Each discrete output is provided by an isolated relay contact.

Output Signal Level: Logic ZERO: Contact Open  
Logic ONE: Contact Closed

NOTE: Contact Rating — 2 amps maximum, 500 volts maximum, 100 VA max.

## Model 115X External Interrupt Coupler Option

This option enables 16 external signals to be connected to individual levels in the computer. An interrupt can be generated on either a positive or negative input signal transition. The model numbers for the External Interrupt coupler with the different input signal conditioning are:

Model	Input Type
1151	Micro Logic
1152	Positive Voltage
1153	Negative Voltage
1154	Contact Closure
1155	Isolated

## Model 116X I/O Interrupt Coupler Option

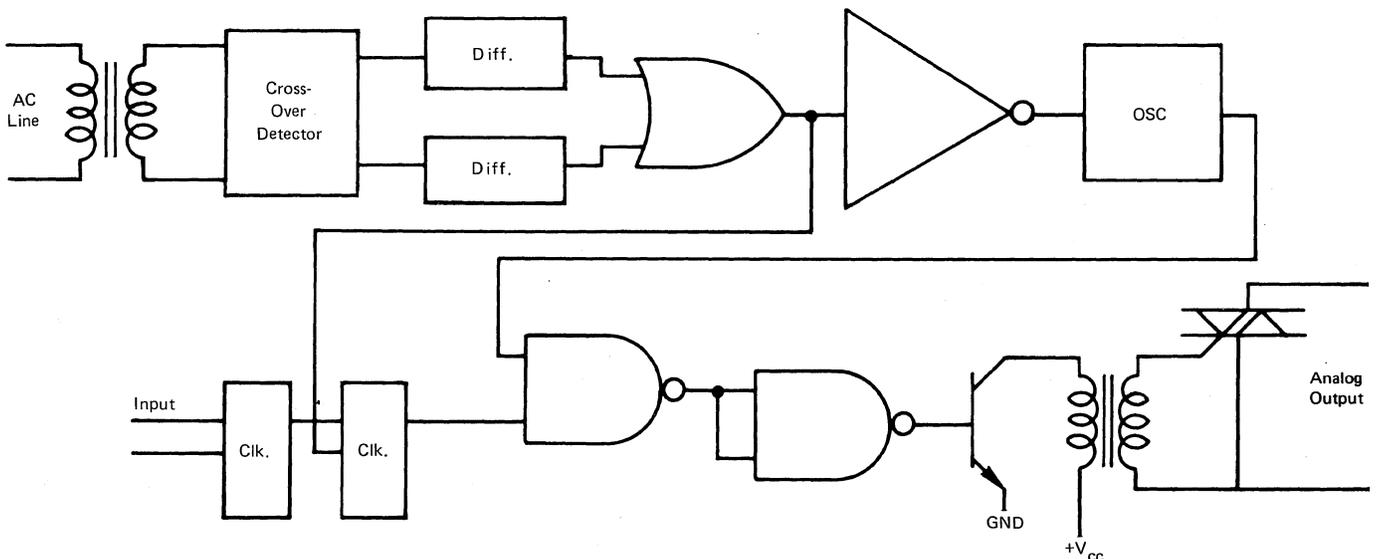
This option interfaces eight interrupt signals to either the I/O Data interrupt party line level (C<sub>16</sub>) or the I/O Service interrupt party line level (D<sub>16</sub>), which are standard in MODCOMP computers. A unique memory location is dedicated to each sub-level connected to each party line level.

The IOIS contains one position for eight Data sub-levels and a second position for eight Service sub-levels. Therefore, up to two I/O Interrupt Couplers can be included in an IOIS. The model numbers for the I/O Interrupt Couplers with the different signal conditioning circuits are:

Model	Input Type
1161	Micro Logic
1162	Positive Voltage
1163	Negative Voltage
1164	Contact Closure
1165	Isolated

## Model 114X and 117X Analog Output Modules

Either one or two digital-to-analog converters are available on a single channel card. Each module consists of a 12 bit data register, switch drivers, current switches, 12 bit ladder network, output amplifier and reference supplies. Various type voltage and current outputs are available.



## Performance Specifications

Resolution — 12 Bits Binary, including Sign  
Settling Time:

Voltage Outputs — 20 u secs. to 0.5% final value  
for full scale step input  
Current Outputs — 100 u secs. to 0.5% final value  
for full scale step input

Update Rate — 50 KHz max.

Output Model Numbers — Voltage:

Single and Dual

1141 and 1171  $\pm 10$  volts full scale at 100 ma max.  
1142 and 1172  $\pm 20$  volts full scale at 50 ma max.

Current:

1143 and 1173 1 to 5 ma. into 0 to 3.2K  
1144 and 1174 2 to 20 ma. into 0 to 800 ohms  
1145 and 1175 10 to 50 ma. into 0 to 320 ohms

Overall Accuracy:

Voltage Outputs —  $\pm 0.5\%$  full scale  
Current Outputs —  $\pm 0.1\%$  full scale

Digital Interface Inputs:

Address — 4 bits binary plus unitary unit select  
Data — 12 bits binary, including sign  
Strobe — Transfers data to addressed channel

## Model 118X Analog Output Modules

These modules are available for driving storage tube displays such as the Tektronix 611 storage scope. These dual DAC's contain the control logic for the display as well as X and Y axis 12-bit digital-to-analog converters. The different types of outputs available are as follows:

Model 1181 —  $\pm 10$  volts — Tektronix 611 storage scope  
Model 1182 —  $\pm 20$  volts — Tektronix 611 storage scope  
Model 1183 —  $\pm 10$  volts — Tektronix 603 storage scope  
Model 1184 —  $\pm 20$  volts — Tektronix 603 storage scope

## Model 111X Asynchronous Communications Interface

### General

This module provides a single, half-duplex, interface to a serial communications line up to 2000 feet in length. The module may be used to interface asynchronous devices such as Teletype-writers, CRT terminals and serial printers. Up to eight interfaces can be supplied in an IOIS.

The communication module accepts and transmits the 11 bit code structure at a choice of transmission speeds from 110 baud to 9600 baud.

The communication interface is connected to the data and service interrupts of the MODCOMP computer I/O Interrupt System. Character assembly/disassembly registers and character input buffer register are provided.

## Performance Specifications

Line Speed — Any of the following baud rates may be selected — 110, 150, 300, 600, 1200, 1800, 2400, 4800, or 9600 baud

Transmission Type — Asynchronous

Type Service — Half-Duplex

Code Format — 11 Bit (1 Start, 8 Data, 2 Stop)

The two electrical interface types available as part of the Asynchronous Communications Interface are:

Model 1115 — 20 ma current loop, Teletype compatible

Model 1116 — RS-232-C

## Model 119X Common Alarm Digital Input Option

This module provides the capability to share one interrupt level (external or I/O) among sixteen digital signals. The module provides an output suitable for setting an interrupt request when any one of the sixteen (16) input bits of the module change state. Three interrupt triggering options are selectable: interrupt on leading edge, interrupt on trailing edge or interrupt on both edges. The pulse outputs from each bit are OR'ed and may be used to set the request of an I/O interrupt on the optional I/O interrupt coupler module.

The signal conditioning circuits available for the inputs are the same as those available with the other types of input channels.

<u>Model</u>	<u>Inputs</u>
1191	Micro Logic
1192	Positive Voltage
1193	Negative Voltage
1194	Contact Sense
1195	Isolated

## Model 110X Synchronizer Module

This option provides a means for synchronizing the transfer of data over eight input or output channels. A total of two synchronizer units can be included in an IOIS. The synchronizing function is performed by a pair of signals per channel. A Transfer Request signal can be generated by an external unit. This signal can be tested by instruction execution. When a data transfer is made in response to an external request, a Transfer Data signal is sent to the unit to acknowledge the inputs, for input channels, or signify that valid data is present, for output channels. The synchronizer is offered with the following signal conditioning options:

<u>Model</u>	<u>Input</u>
1101	Micro Logic/Micro Logic
1102	Positive Voltage/Positive Voltage
1103	Negative Voltage/Negative Voltage
1104	Contact Sense Input/Micro Logic Output
1105	Isolated Input/Micro Logic Output

# UNIVERSAL COMMUNICATIONS SUBSYSTEM

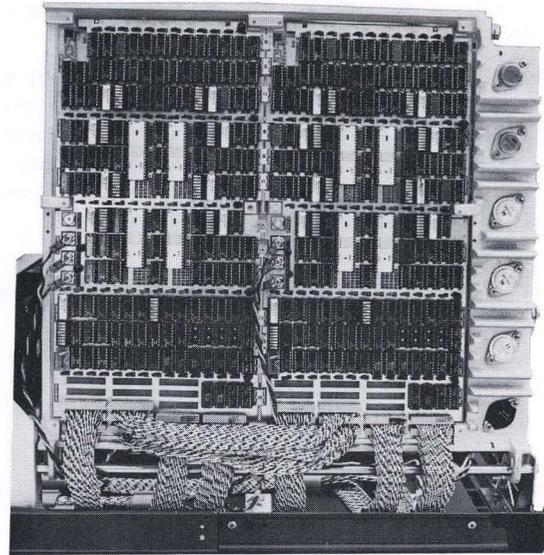


## Features

The Universal Communications Subsystem provides a flexible yet economical means of interfacing a large number of high and low speed lines using both synchronous and asynchronous modes of data transmission. The Universal Communications Subsystem is particularly applicable to front-end and stand-alone communications applications where flexibility as well as throughput are both crucial factors. A single system can interface up to 64 full duplex lines. Multiple subsystems can be utilized on a single MODCOMP III CP.

- Synchronous and Asynchronous Line Interfaces
- Full or Half-Duplex Operation
- Direct Block Transfer To and From Memory (DMP)
- Baud Rates To 10 Kilo Baud Standard.  
Options To 50 Kilo Baud
- Hardware Selectable Sync Character
- Leading Sync Character Insertion and Deletion
- Auto Answering Standard
- Internal or External Clocking
- Program Selectable Character Parity Checking and Generation
- Program Selectable Stop Bits (1 or 2 Bits)
- Special Character Detection During Block Transfers  
One Hardware Patchable Character  
Two Program Selectable Characters
- Program Selectable Hardware Echo on Asynchronous Lines
- Program Selectable Baud Rate
- 4 to 64 Full Duplex Channels
  - Expandable In Groups of 4
  - Mixed Mode In Groups of 4
  - Speed Variable Channel by Channel
- Concurrent I/O of Different Mode and Speed On All Channels
- RS-232-C and TTL Compatible Modem Interfaces or TTY 60/20 MA Current Loop Interfaces
- Wrap Around On Output Under Program Control

The flexibility in speed and mode of data transmission available through the Universal Communications Subsystem enables the MODCOMP III CP to communicate simultaneously with synchronous and asynchronous terminals as well as other remote computers.



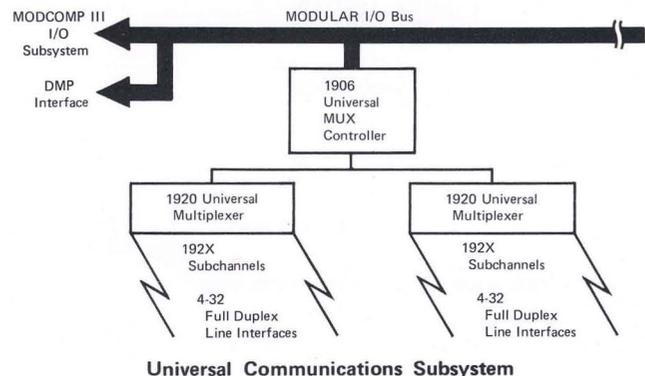
Universal Multiplexer plane containing eight line interfaces.

## Functional Description

The Universal Communications Subsystem consists of several basic components. These components and their functions are:

- Model 1906 — Universal Communications Multiplexer Controller
- Model 1920 — Universal Communications Multiplexer
- Models 1922/1923 — Synchronous Channels
- Models 1924/1925/1926 — Asynchronous Channels

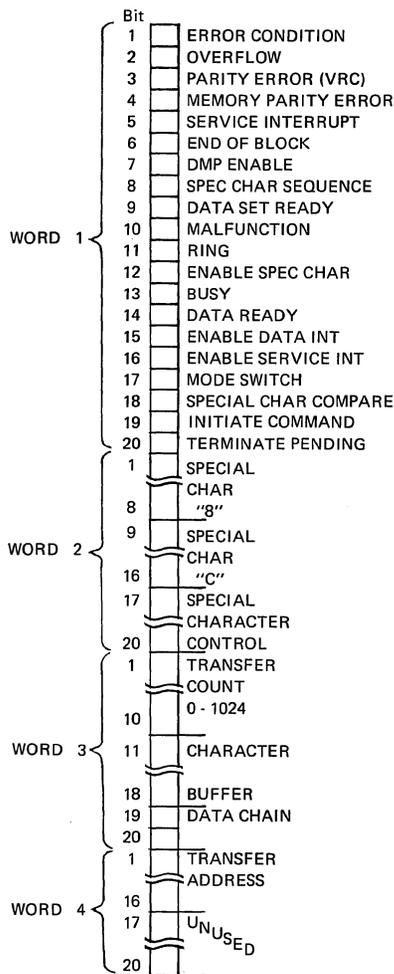
The figure below illustrates the functional components.



## Model 1906 - Universal Communications Multiplexer Controller (UCM)

The UCM controller is housed on a standard Peripheral Controller interface plane and requires two controller positions for the basic controller and one additional position if internal clocking is to be provided. The controller provides centralized control for up to 64 full duplex subchannels and performs instruction decoding, data transfers to and from the I/O bus, and block transfer control via the Direct Memory Processor.

The controller maintains status/control information and provides character buffering for each sub-channel via a solid state random access memory (RAM). The RAM is integral to the UCM controller and provides 80 bits of storage for each input and output subchannel. The format and contents of the RAM are depicted below.



Subchannel RAM Format

Since information concerning each subchannel is maintained independently of other subchannels, any or all subchannels may operate in the same or different modes concurrently.

## Model 1920 - Universal Communications Multiplexer

The Universal Communications Multiplexer provides a rack mountable enclosure, power supplies, controller interface and connectors for up to 32 full duplex channels. Up to 2 multiplexers may be interfaced to the controller, providing a 64 channel capacity.

## Model 192X Communication Line Interface Channels

The Communications Line Interface Channels provide the character assembly and disassembly required to receive or transmit data via the respective communication lines. The subchannels are packaged in groups of four full duplex interfaces per unit. Each subchannel within a group is of the same mode (synchronous or asynchronous). The baud rate, frame size, parity control, etc., can vary from channel to channel, however.

The primary function of the subchannels is to perform serial to parallel conversion of the input data and parallel to serial conversion of data to be transmitted. Each subchannel has a set of manually operated micro switches with which the special character to be detected is selected. The synchronous channels have a second set of switches with which the sync character code is entered. The synchronous channels automatically, upon initiation of output, insert six leading sync characters. Upon initiation of input the subchannels automatically establish synchronization and strip all leading sync characters.

Each subchannel, in addition to the parallel to serial and serial to parallel registers, contains a character buffer register which, combined with the buffer register in the controller, provide triple buffering of all data. This feature reduces considerably the chances of an overflow condition occurring.

The synchronous channels are available with either RS 232-C or TTL compatible modem interfaces.

Model 1922 — RS-232-C Compatible Synchronous Modems

Model 1923 — TTL Compatible Synchronous Modems

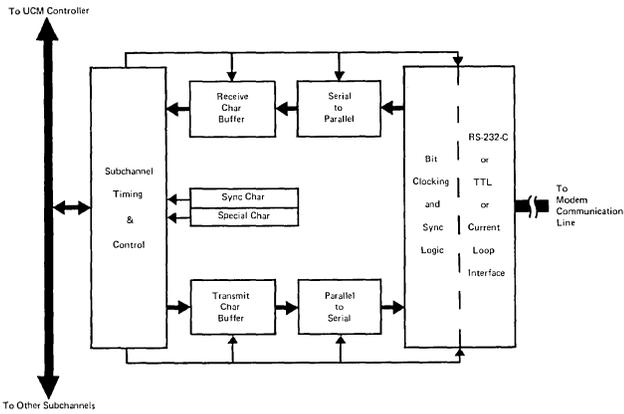
The asynchronous channels are available with current loop interfaces in addition to the modem interfaces.

Model 1924 — 60/20 MA Current Loop TTY Compatible

Model 1925 — RS-232-C Compatible Asynchronous Modems

Model 1926 — TTL Compatible Asynchronous Modems

The figure below depicts the functional logic of each full duplex subchannel.



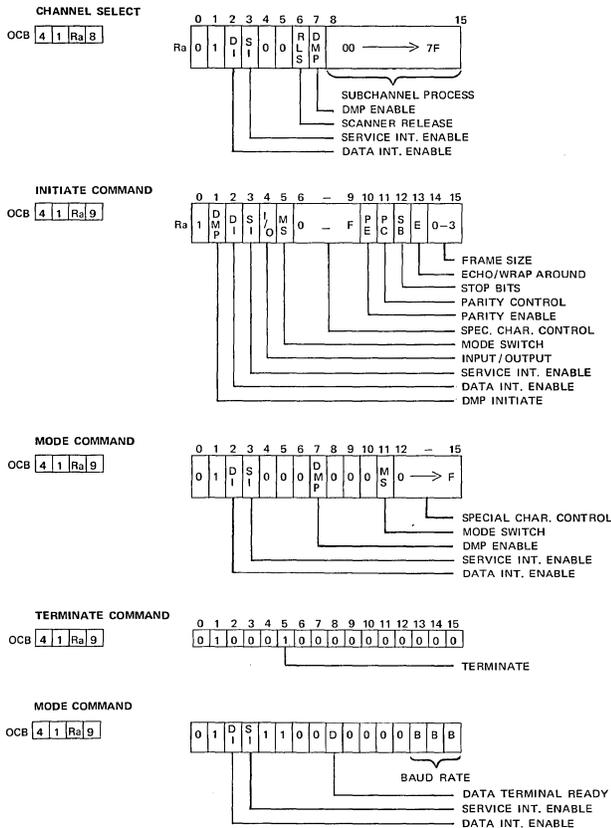
Full Duplex Subchannel

## Input/Output Instruction Formats

### Command Formats

The commands which may be issued to the Universal Communications Controller are defined in the table below.

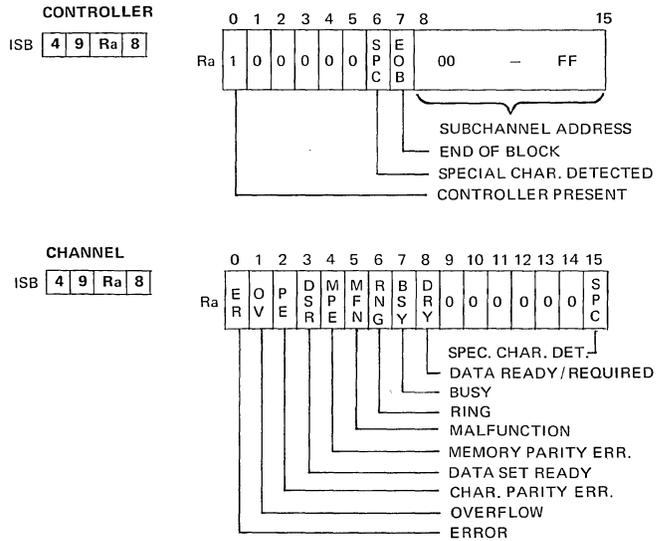
The channel select command (41Ra8) is issued to select a specific subchannel. The remaining instructions (41Ra9) command the selected channel and enable/disable DMP, Data and Service interrupt request, as well as initiate and terminate data transfers.



Control Command Formats

### Status Formats

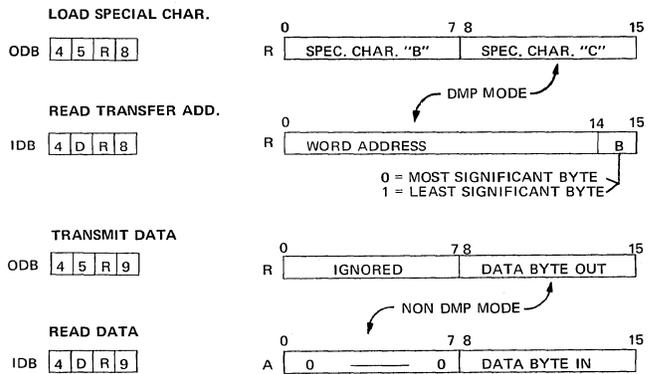
The status requests and the resulting status indicators available from the controller and the channel after performing a channel select are shown below.



Status Formats

### Data Formats

The commands and the data formats that are used to pass or receive data information to or from a selected channel are shown below. If data is being transferred via DMP, the transfers are transparent to the program and the channel only needs attention upon detection of a special character or end of block.



I/O Data Formats

## Special Character Detection

The special character detection feature provides the ability to interrupt the CPU upon detection of a specific character or sequence of characters. Three special characters are provided. One is patchable in the channel and two may be selectively set under program control. Upon detection of a special character or sequence, the channel will request a data interrupt. The program may then issue a terminate or a mode command to change the character sequence and continue data transfers.

The special character detect logic is initialized via either an initiate or mode command and provides the following character or sequence of character detection command.

- 0<sub>16</sub> = NO SPECIAL CHARACTER DETECT
- 1 = INTERRUPT ON 'A' COMPARE
- 2 = INTERRUPT ON 'B' COMPARE
- 3 = INTERRUPT ON 'C' COMPARE
- 4 = INTERRUPT ON 'A' OR 'B' OR 'C' COMPARE
- 5 = INTERRUPT ON 'A' OR 'B' COMPARE
- 6 = INTERRUPT ON 'A' OR 'C' COMPARE
- 7 = INTERRUPT ON 'B' OR 'C' COMPARE
- 8 = INTERRUPT ON 'A' FOLLOWED BY 'A' FOLLOWED BY ANY CHARACTER
- 9 = INTERRUPT ON 'A' FOLLOWED BY 'A' FOLLOWED BY 'B' OR 'C'
- A = INTERRUPT ON 'A' FOLLOWED BY 'A' FOLLOWED BY 'B'
- B = INTERRUPT ON 'A' FOLLOWED BY 'A' FOLLOWED BY 'C'
- C = INTERRUPT ON 'A' FOLLOWED BY ANY CHARACTER
- D = INTERRUPT ON 'A' FOLLOWED BY 'B' OR 'C'

- E = INTERRUPT ON 'A' FOLLOWED BY 'B'
- F = INTERRUPT ON 'A' FOLLOWED BY 'C'
- 'A' = HARDWARE PATCHABLE CHARACTER
- 'B' } = PROGRAM SELECTED CHARACTERS
- 'C' }

## PROGRAMMABLE SPECIAL CHARACTER DETECTION OPTIONS

## Summary

The Universal Communications Subsystem coupled with the MODCOMP III Communications Processor provides an unequalled hardware configuration in its price range. The system offers an economical solution to applications requiring a mix of high and low speed lines using both synchronous and asynchronous techniques.

The flexibility of the system makes it ideal for message switching and large preprocessing applications. The ability to use both register I/O and block memory transfers enables efficient operation in polled network environments. Since frame size and special characters are variable, any common code structure or communication protocol may be implemented.

Device independent software handlers are available under the powerful MODCOMP MAX III operating system, and new application software is being developed on a continual basis.

Extensive diagnostic software is available performing static tests and dynamic exercising via the hardware wrap-around feature, eliminating the need for special cabling.

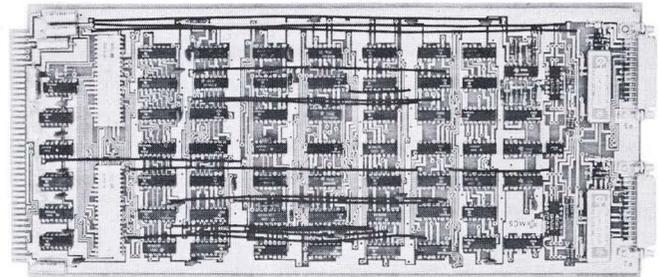
# ASYNCHRONOUS COMMUNICATIONS SUBSYSTEM



## Features

The Asynchronous Communication Subsystem (ACS) provides an economical means of interfacing a large number of asynchronous communication lines to any one of the MODCOMP family of processors. The features provided by the ACS enable efficient system operation in applications such as low speed concentrators, store and forward message switching, and interactive time-sharing.

- 2 to 128 Full Duplex Line Interfaces
- Field Expandable in Multiples of 2
- 75-9600 Baud, 5 Rates Per Multiplexer
- Programmable Stop Bit (1 or 2 Bits)
- Programmable Frame Size (5, 6, 7, or 8 Bits)
- Automatic Character Parity Checking/Generation
- Programmable Character Parity (Odd, Even or None)
- Auto Answering Standard
- RS-232-C Compatible Modem Interfaces
- TTL Compatible Modem Interfaces
- 60/20 MA Current Loop Interfaces (TTY Compatible)
- Programmable Hardware Echo During Input
- Programmable Hardware Wraparound During Output
- Interrupt Driven Character Transfers

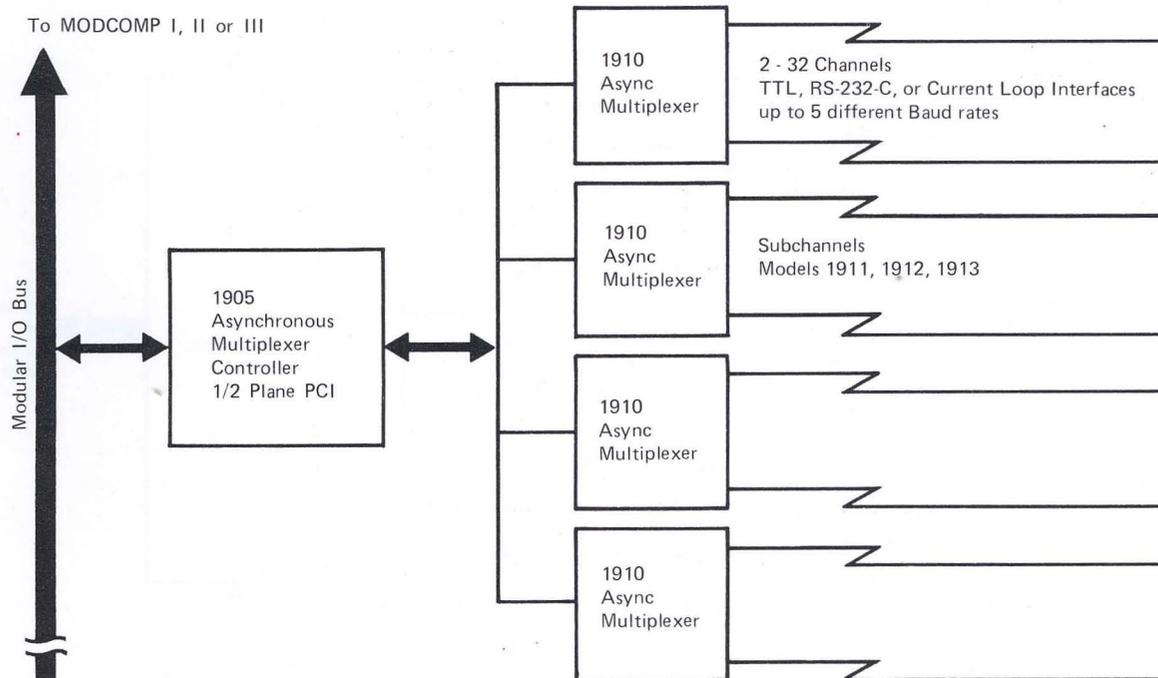


Asynchronous Multiplexer card containing two line interfaces.

- Double Character Buffering
- Concurrent Operation of Any Number of Channels at Different Baud Rates, Frame Size, and Parity Options

## Functional Description

The Asynchronous Communications Subsystem consists of a half plane controller, from one to four multiplexers, and two or more full duplex asynchronous line interfaces. A block diagram of the subsystem is shown below.



Asynchronous Multiplexing Subsystem

## Model 1905 Asynchronous Communications Multiplexer (ACM) Controller

The ACM controller is packaged in a standard MODCOMP Peripheral Controller Interface and requires one controller position (half plane). The controller provides the I/O Bus interface and control for up to four multiplexers. The controller is responsible for scanning each of the subchannels and detecting/generating Data and/or Service interrupts as required by the subchannels.

- 1911 – 60/20 MA Current Loop, TTY Compatible
- 1912 – RS-232-C Compatible Modem Interface
- 1913 – TTL Compatible Interface

The functional characteristics of each of these models are the same, the only difference being in the external signals and levels provided for interfacing to the communication line or modem.

## Model 1910 Asynchronous Communications Multiplexer

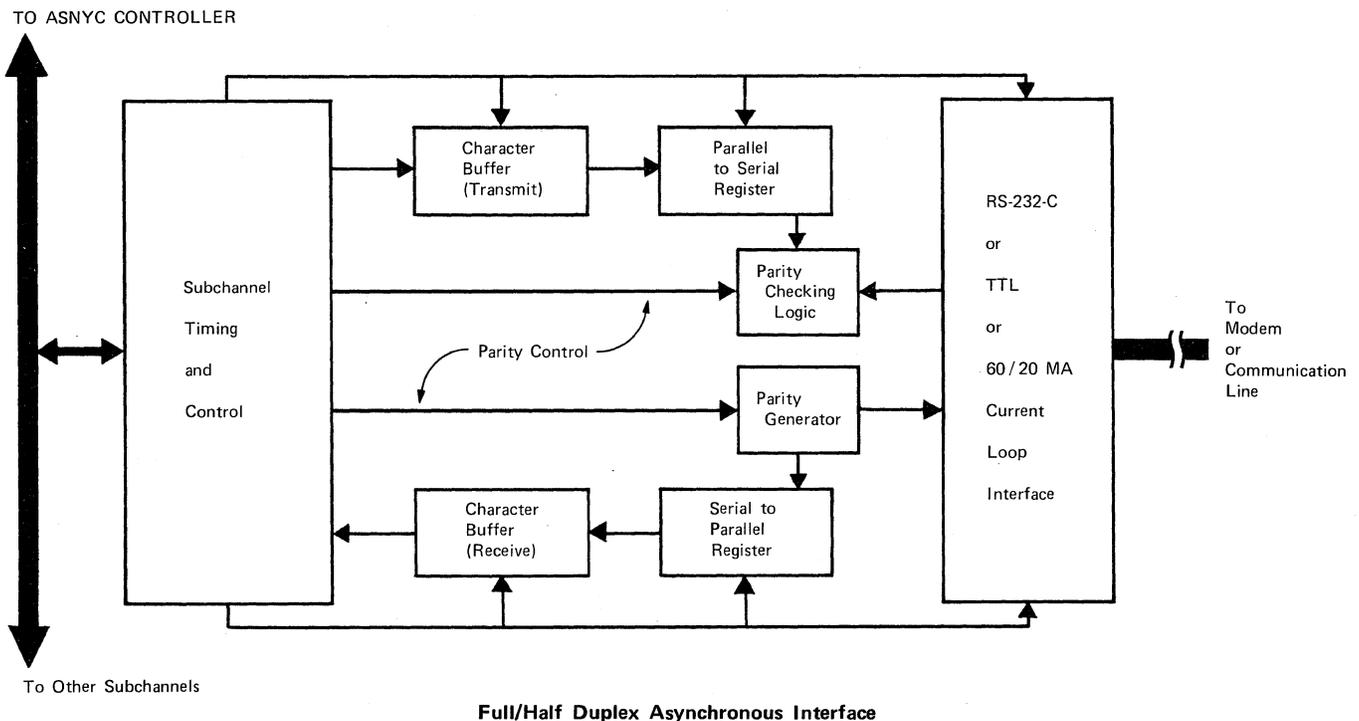
Each Asynchronous Communications Multiplexer provides the power source, controller interface, clock generator, and card cage for up to 32 full duplex channels. Standard clock rates available from the multiplexer are, 75, 110, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 baud. Within a single multiplexer any five baud rates may be selected. Provisions have been made in the multiplexer to provide special clock rates upon request.

The subchannels are packaged on a PC card. Each card contains two full duplex channels. Each full duplex channel contains a parallel-to-serial and a serial-to-parallel register for disassembling/assembling data to and from the communication line. During input all start and stop bits are deleted by the channel and the character parity checked before passing data to the I/O bus. During output the channels generate and insert character parity as selected, as well as generating the required start and stop bits. A character buffer is provided in each channel to provide a margin of safety in available latency time between servicing data requests. This is particularly important during input.

## 191X Dual Asynchronous Full Duplex Subchannels

The subchannels within the multiplexers are available in three standard models.

A block diagram depicting the functional elements of a single full duplex interface is shown below.



# I/O Instruction Formats

There are three groups of instructions which are used to effect data transfer through the Asynchronous Subsystem. These instruction groups are Command, Status, and Data transfer instructions.

## Command Instructions

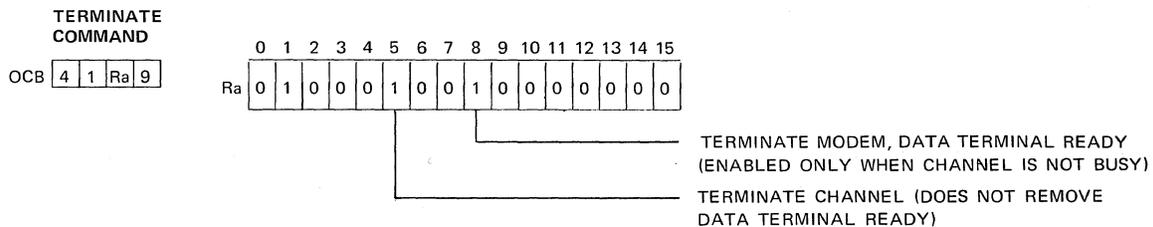
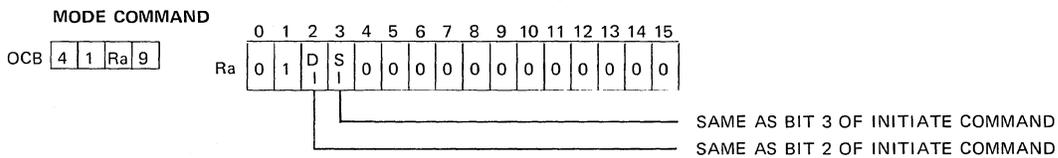
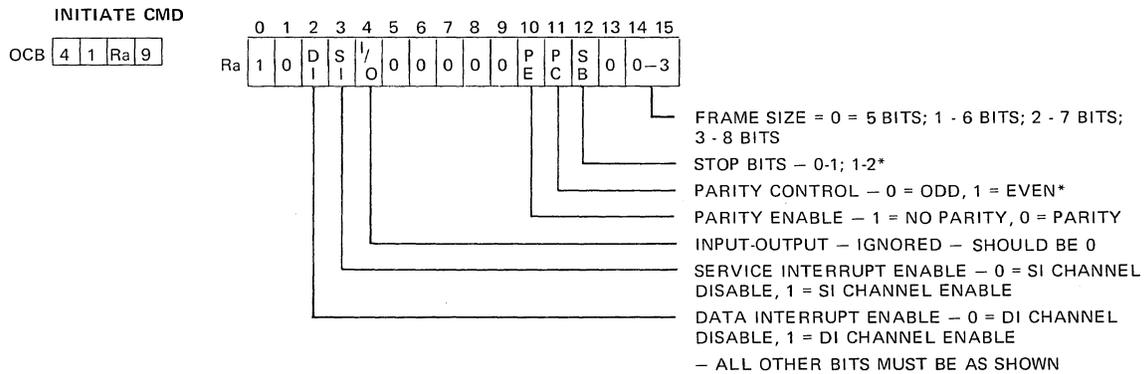
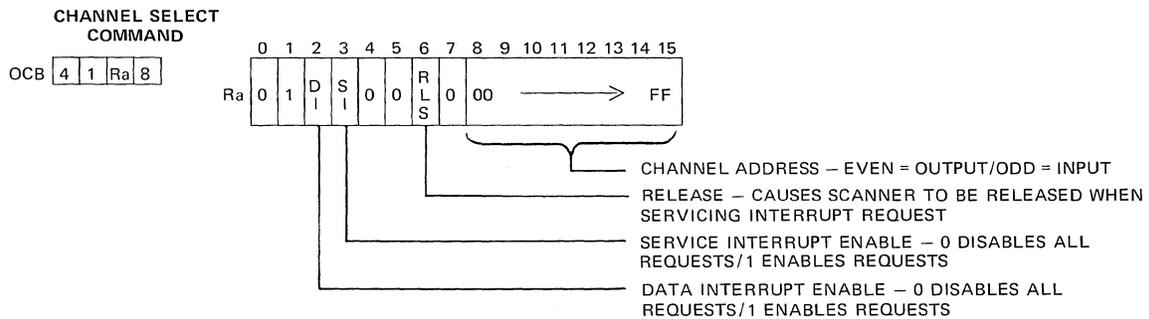
There are four command instructions, one of which is used to select the subchannel with which communication is desired. The remaining three instructions are used to condition the selected subchannel for data transfer and set up the associated parameters about that transfer. The parameters which are unique to each channel and are program selectable include character frame size, number of stop bits, parity, and interrupt service to be utilized.

The opcodes and formats for each of the command type instructions are shown below.

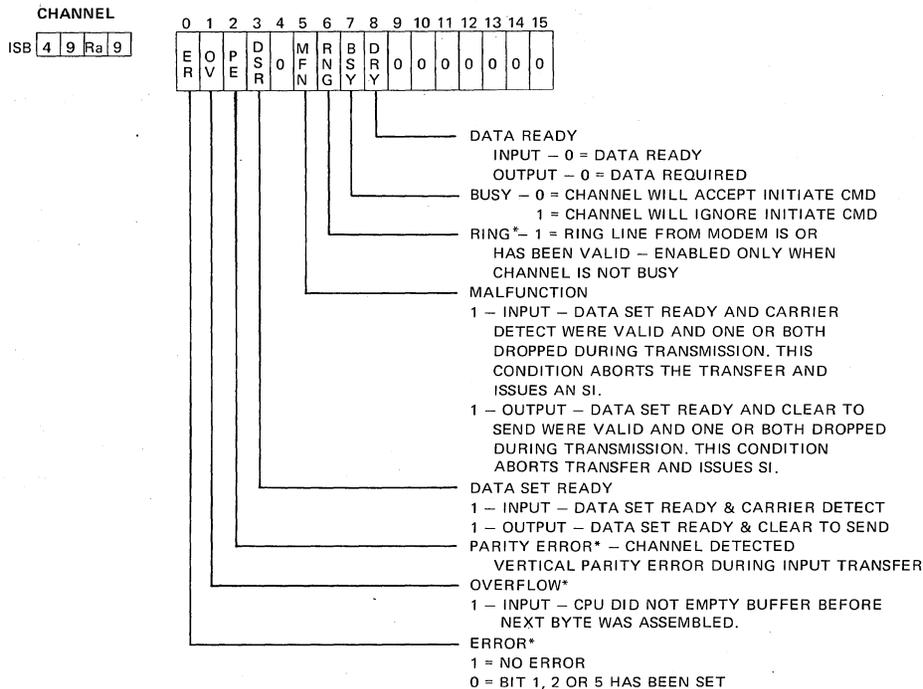
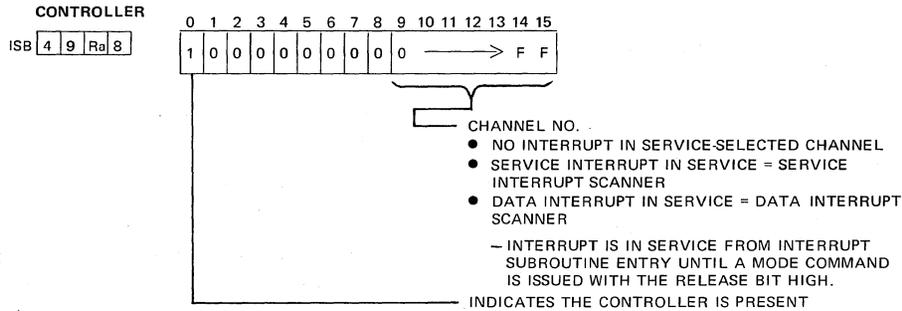
## Status Instructions

Two status instructions are used to obtain information from the controller and the subchannels. The first input status instruction is normally used in conjunction with the data and/or service interrupt level. The status response defines which subchannel is requesting attention. The input channel status instruction may then be used to further define the condition of the channel, such as a ring, parity error, malfunction, or data transfer needed condition.

The opcodes and formats for the status instructions are shown on page 4.



Command Formats

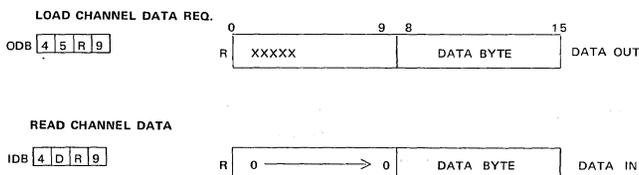


\*THESE CONDITIONS ARE CLEARED BY THE INITIATE COMMAND OR MASTER CLEAR.

### Status Formats

## Data Transfer Instructions

The Asynchronous subsystem effects data transfer on a character basis only. Two data transfer instructions are provided, one for transferring a character to the channel for subsequent transmission and one instruction for transferring a character from the channel into a specified register. Both instructions may be used in either the test and transfer mode or the interrupt and transfer mode. The opcodes and data formats for the status instructions are shown below.



### Data Formats

## Software

### Handlers

Handlers for the Asynchronous Subsystem are available with the MAX III operating system. The user's interface to the handlers is through the standard MAX III I/O system using REX services. The standard MAX III handler is designed for TTY compatible devices. Special terminal handlers for polled, multidropped terminals can be integrated into the system.

### Diagnostics

Diagnostic tests for the Asynchronous subsystem include full range tests including wraparound testing or testing through utilization of a Teletype for input and output of data.

# INTERFACING TO MODCOMP COMPUTERS



## Features

The basic ways to interface equipment to MODCOMP computers are:

- Through the Input/Output Interface Subsystem
- Directly to the Input/Output Cable Driver/Receiver Set
- Through the General Purpose Controller
- Through the MODCOMP I or II Modular Bus Control
- Through a Separate Memory Port

This application note contains a summary of the information required to connect equipment to the MODCOMP I, II or III computers through these interfaces. The details and drawings are contained in the MODCOMP computer and I/OIS technical manuals.

The only difference between the MODCOMP III I/O system and that of the MODCOMP I and II is the method of driving signals on the I/O cable. The timing relationship of signals for the MODCOMP I, II and III are identical. The cable drivers for the MODCOMP III are differential drivers capable of driving 100 feet of I/O cable. The cable drivers for the MODCOMP I and II are single-ended drivers capable of driving 100 feet of I/O cable. A mixture of single-ended and differential drivers is not operable in a single system.

## Interfacing to the Input/Output Interface Subsystems

The Input/Output Interface Subsystem (IOIS) is designed to provide a very simple computer interface. The basic IOIS contains any combination of up to 16 digital input channels, digital output channels, analog output channels and a variety of other input or output types. A channel multiplexer for up to 64 multiplexed channels is also available.

Each digital channel is capable of transferring up to sixteen bits of data in parallel by instruction execution. Each digital output channel contains a 16-bit buffer

which stores the last word transferred from the computer. The digital input channel lines are sampled directly when an input instruction is executed. The analog output channels receive and store a 12-bit binary value from the computer, which is then converted to an analog signal.

A variety of signal conditioning options are available with the IOIS channels. The proper option can be selected to make the channels directly connectable to most types of user equipment. Connection is made by means of a cable that has a connector which mates with the front edge of the channel card.

The programming of word transfers via the IOIS is straightforward. Each channel in an IOIS has a unique peripheral device address in Group C (first IOIS) or Group D (second IOIS). A word is transferred to or from a channel by execution of an Input Data to Group C instruction:

IDC,R,C  
ODC,R,C

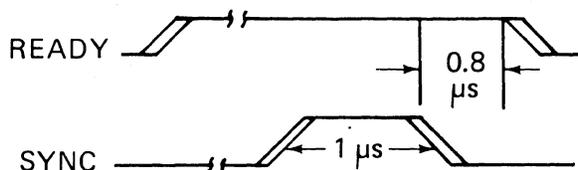
, where R specifies any of the 15-general registers in the computer and C (on the right) specifies any of the 16 channels in the IOIS. The entire execution is completed in less than 2 usec, depending on the instruction and computer.

No synchronization or control is required from the user equipment in this type of transfer. Therefore, only the data lines are connected to the user equipment. Twisted pair is normally used for each data line.

Synchronization and control of data transfers can be performed by the external device in either of two ways. The device can send an interrupt signal to the computer through either the External Interrupt Coupler or the I/O Interrupt Coupler option in the IOIS. If the interrupt is sent when a data word is ready for input or can be accepted for output, then the computer can process the interrupt and execute an Input Data or Output Data instruction as described above.

When positive interlocking is required by the external unit, the Synchronizer option can be included in the IOIS. The two control lines (for each of eight channels) can be connected to the unit along with the data lines.

The timing for the two signals — Ready, generated by the unit, and I/O sync, generated by the computer are shown below.



The computer can test the Ready line by means of the Input Status instruction and then execute an input or output transfer after the ready status (high level) is detected. The timing of the transfer is indicated by the Sync signal. The unit should reset the Ready signal within 0.8 μs after the trailing edge of the Sync signal to insure that another transfer is not made.

## Interfacing Directly to the Input/Output Cable Driver/Receiver Set

The MODCOMP I/O bus is connected serially (“daisy-chained”) to each Peripheral Controller Interface enclosure and to the Input/Output Interface Subsystem. Each connection is made by means of a cable driver/receiver set which converts all signals on the I/O cable to TTL logic levels for use by the peripheral device controllers.

The I/O cable connection rules are:

- (1) The maximum combined cable length between the computer and all controllers is 100 feet.
- (2) All connections must be made via a cable driver/receiver set.
- (3) A maximum of eight cable driver/receiver sets can be connected to the cable, in addition to the set in the computer.
- (4) Up to four device controllers can be connected to each driver/receiver set.

The block diagram of the computer I/O subsystem shows the types of signals in the cable (which is cut by the dashed line in the figure). The signals are described below.

### Address (6 Pairs)

Designate which device controller is to respond to the control lines. The six-bit binary value is obtained from the I/O instruction word (bits 6-7, 12-15). An address of zero will be acknowledged by the controller currently in DMP service.

### Control (5 Pairs)

The four I/O instruction functions are coded on two lines: Command (false)/Data (true) and Input (true)/Output (false).

The I/O Sync signal indicates that an I/O transfer is occurring. When this signal is true, the Command/Data, Input/Output and Address signals are valid.

The other two control signals are Master Clear, which is generated at the computer control panel, and Clock, which is a 5 MHz square wave generated in the computer. The Master Clear signal normalizes all units and the Clock signal provides a timing signal to all controllers, eliminating the need for an internal time base.

### Data (16 Pairs)

All commands, status, data and controller priority are transmitted over this bi-directional bus.

### DMP Control (2 Pairs)

The DMP Request signal is sent to the computer by controllers operating under DMP Control. It signifies a request for a word transfer.

The DMP responds with a DMP Update Queue signal. In response to this signal, each (if more than one) controller having a current DMP request places a true signal on one of the 16 data bus lines, indicating one of 16 DMP channel priorities.

The Source ID of the unit, which is a six-bit pointer to the dedicated memory locations for the channel, is also placed on the Source ID lines. Each requesting unit examines the data bus lines to determine if a higher priority unit is also requesting a transfer. If so, the lower priority unit removes its priority and Source ID signals. However, it keeps the Request signal true, so that the DMP will issue a new DMP Queue Update as soon as the current word transfer is complete.

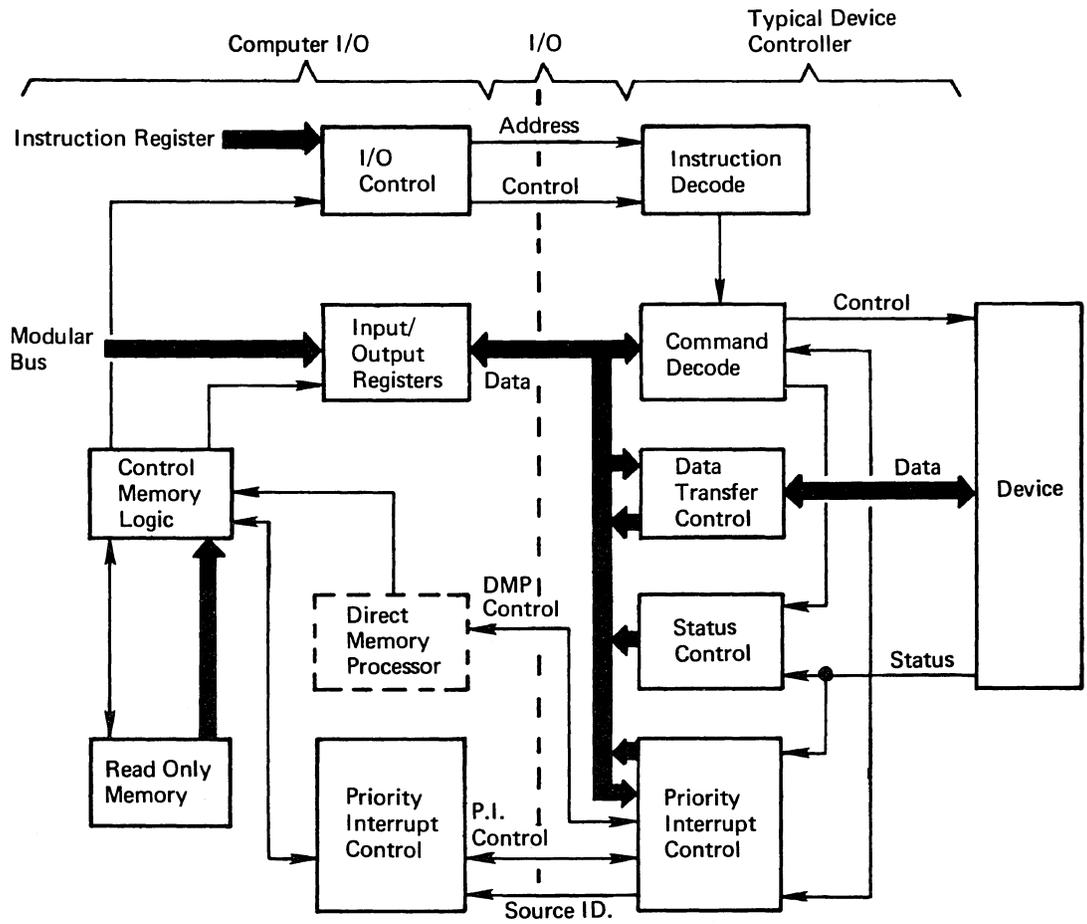
### Priority Interrupt Control (4 Pairs)

These signals consist of a Request signal and an Update Queue signal for both of the two party line interrupts. Therefore the four signals are Data Request, Data Queue Update, Service Request, and Service Queue Update. These two pairs of signals are handled just like the DMP Request and DMP Queue Update except they are serviced at priority interrupt levels C<sub>16</sub> and D<sub>16</sub>. The DMP transfers are serviced in the DMP independently of the interrupt priority structure. Each requesting controller places its priority bit on one of the 16 data bus lines and its Source ID on the Source ID lines. All but the highest priority requesting controller remove their signals before the interrupt request signal is transferred to the computer.

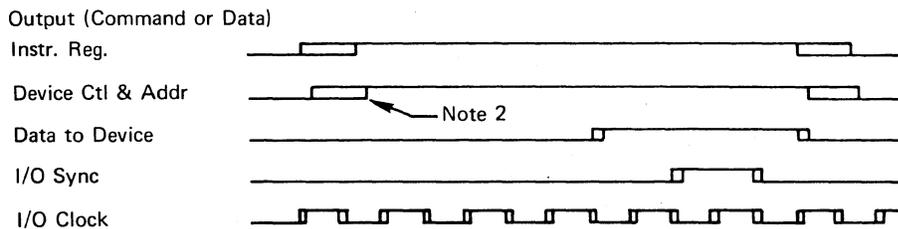
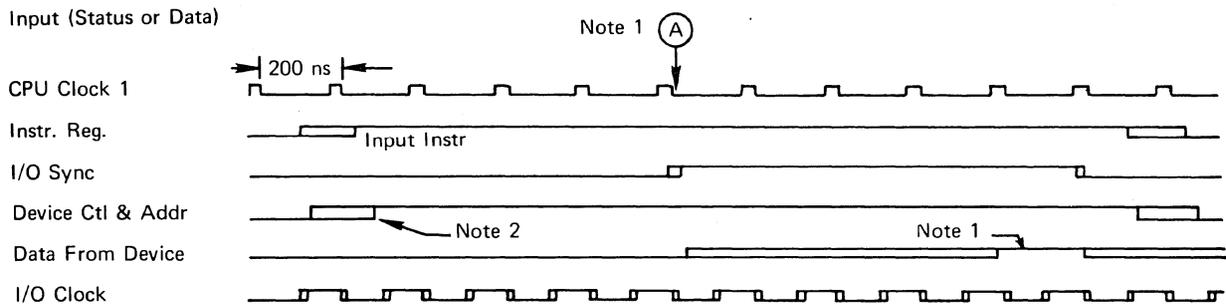
### Source ID (6 Pairs)

Each device has a unique Source ID code which is sent to the computer in response to an update queue command. This code is used to identify the dedicated memory location assigned to the interrupt sublevel or the DMP channel.

The timing for the I/O signals is illustrated in the following diagrams. The waveforms show how a controller at the computer (the console teletypewriter) and a second controller 100 cable feet away can both operate within the allowed time margins.



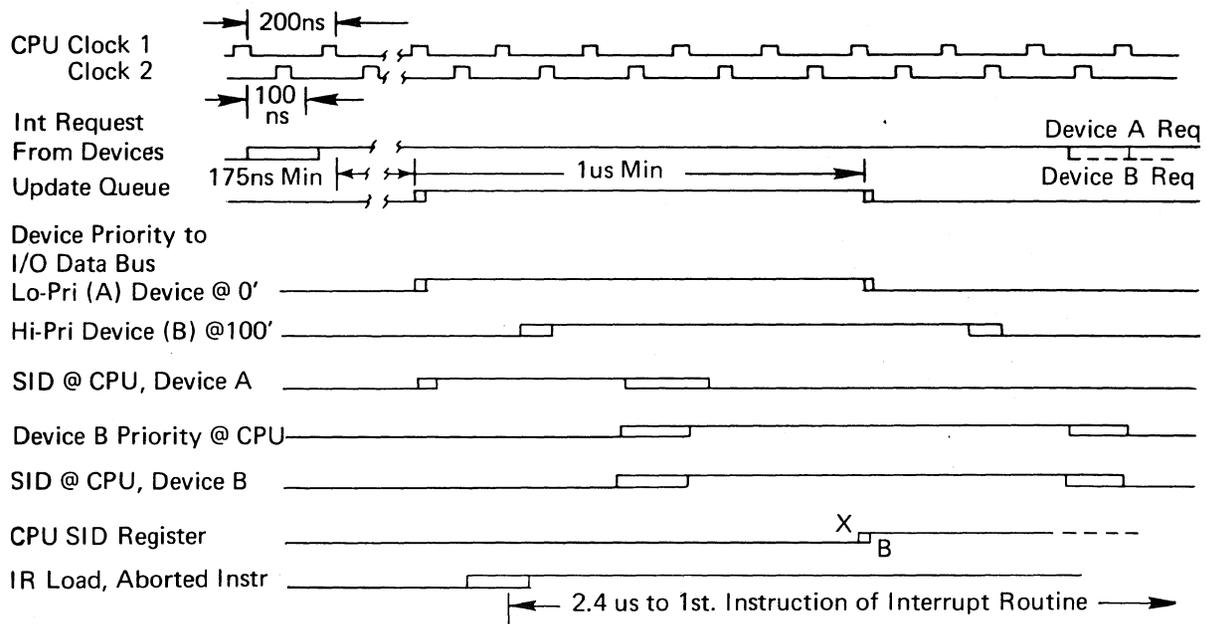
MODCOMP I/O Diagram



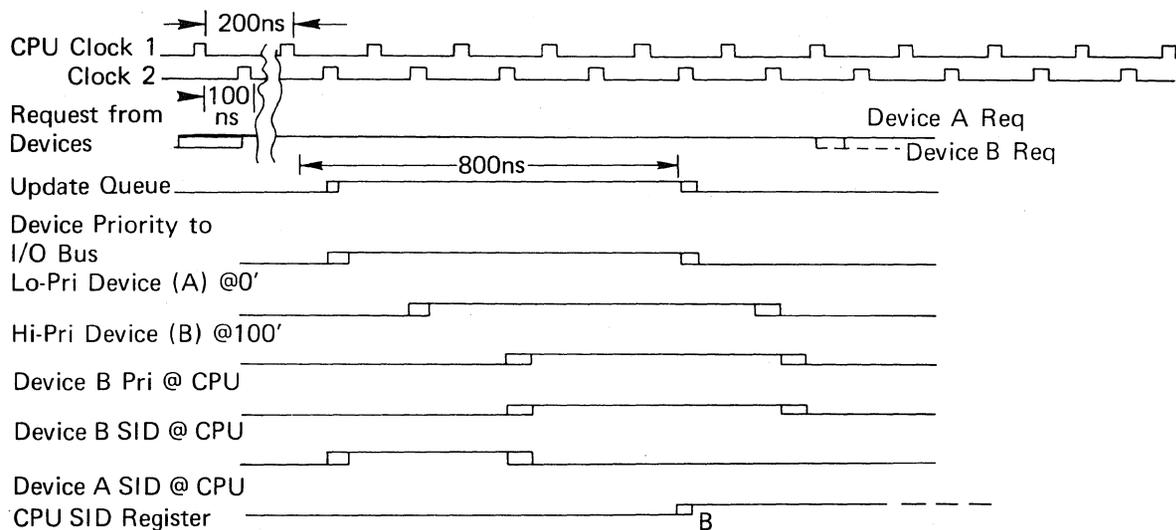
Note 1: Data must be valid at CPU not later than 810 ns after Clock A trailing edge

Note 2: Device Control and Address lines valid 200 ns nom prior to L. E. DMP operations

MODCOMP I/O Timing



MODCOMP Update Queue Timing for Service or Data Interrupt



MODCOMP DMP Queue Update Timing

## Signal Levels

The signal levels at the cable driver/receiver interface to the controller logic are:

Logic 0: 2.4 to 5.5 Volts

Logic 1: 0 to 0.4 Volts

Except IOICB which is inverted.

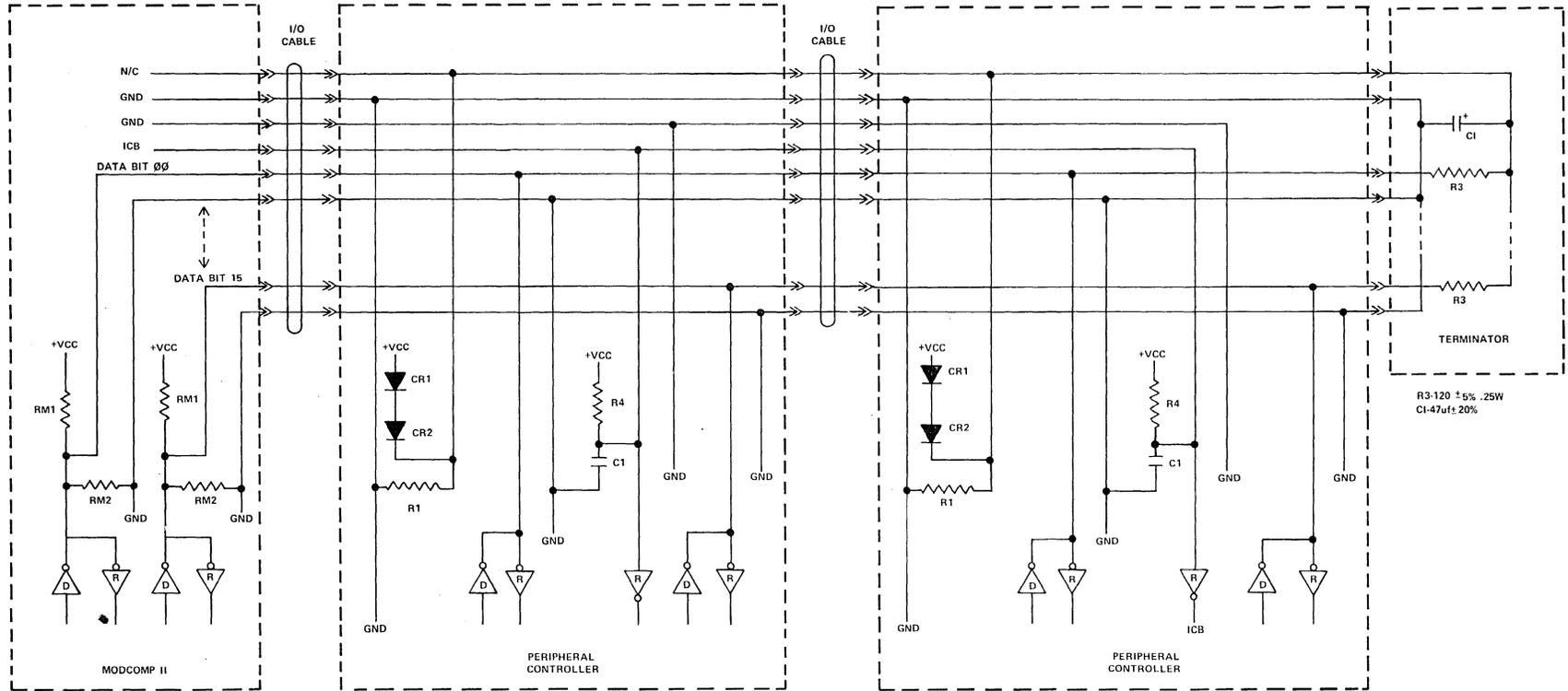
The cable diagram illustrates a MODCOMP II I/O Bus system with the driver/receiver sets and the associated termination network.

The I/O Clock (IOCLKN), a 5 MHz square wave, is dis-

tributed on the I/O bus for general purpose use in the controllers.

When the IOICB (Initial Condition Bus) comes true, each controller will normalize (not busy, no interrupt or DMP Requests, no interrupt enabled, device normalized, etc.). This signal is present if the CPU power is going down and is present to normalize the system when power is returned to the CPU and when the master clear switch on the CPU console is depressed.

All signals are ground true except IOICB. This allows each controller to recognize the absence of a current sink in the CPU and normalize when CPU power is absent.



RM1-220  $\pm 3\%$ , 140MW  
 RM2-330  $\pm 3\%$ , 140MW  
 D-SINKS 70 MA MIN. FOR LOGICAL 1 (.4V MAX.)  
 -100 $\mu$ A MAX. LEAKAGE FOR A LOGICAL 0 (.15V MAX.)  
 R- $\emptyset$  OUT FOR INPUT  $\approx 2.0V$   
 -1 OUT FOR INPUT  $\approx .8V$   
 MAX SOURCE CURRENT .2MA

R1-220  $\pm 5\%$ , .25W  
 C1-.01 $\mu$ F, CERAMIC (-20%, +80%)  
 CR1, CR2-IN4001 or EQUIV.  
 R4-1.2K $\pm 5\%$ , .25W

R1-220  $\pm 5\%$ , .25W  
 C1-.01 $\mu$ F, CERAMIC (-20%+80%)  
 CR1, CR2-IN4001 OR EQUIV.  
 R4-1.2K $\pm 5\%$ , .25W

R3-120  $\pm 5\%$ , .25W  
 C1-47 $\mu$ F $\pm 20\%$

Input/Output Cable Diagram

# Interfacing to the General Purpose Controller

The general-purpose controller provides the means for customer implementation of a standard interface between the cable driver/receiver set and special device controllers.

The general purpose controller includes all the general interfacing logic required to connect an I/O device to the I/O cable. It contains an available work area where data buffer registers, setup registers, input status logic and special control logic can be implemented. It also provides the logic for two I/O interrupts and a DMP channel interface. The controller generates the timing pulses for transferring data, commands and status into and out of the work area.

Internal jumpers must be connected to satisfy variable I/O functions such as device addresses and device priority. If the DMP interface is used, some jumpers must be connected to select the DMP channel number. If custom I/O macros are to be used, the ROM entry address of the firmware program must be jumpered to the source ID lines. Thirty two entry addresses within a 128 word ROM are available. Detailed descriptions of the internal jumpers required are described in the Peripheral Controller Manual.

Data transfers are controlled by two signals from the general purpose controller. One signal (Output Data Command) is a strobe pulse used to output a data word to a buffer register in the work area. A second signal (Input Data Command) is a gating pulse used to gate data from a buffer register in the work area. These are the only two signals required for data transfers.

When inputting a status word, a gating signal (Enable Input Status) is provided. This signal is used just like the Input Data Command signal.

An additional feature of the general purpose controller is the interlocking logic for device dependent functions. A busy signal from the work area is required to enable and disable the interlocking function. The interlocking function is used to prevent a device from receiving motion commands, caused by program errors, during a period in which the device is performing a previous motion command.

For setup operations, the command instruction causes a gating signal that will load the command register in the work area. This pulse only occurs if the busy signal is false. For more complex operations, several sub-functions of the commands are available and are discussed in detail in the I/O Design Manual.

The interrupt logic and its enabling and disabling logic are contained in the general purpose controller. The two interrupts can be used for any function, but the Data Interrupt is normally used for data transfers and the Service Interrupt is normally used to indicate when a controller is not busy. The two interrupts are requested by signals from the work area. The cause of the Service Interrupt request signal is normally reset when the inter-

rupt has been accepted by a Reset Service Interrupt Request pulse from the controller. The cause of the Data Interrupt is normally reset by an Output Data Command, Input Data Command or a Terminate Command.

The interfacing logic required by the DMP is also contained in the general purpose controller. The Data Request signal must be generated in the work area. Each time the Data Request signal is true, a transfer sequence will be started.

A 5.0 MHz square wave and a Master Clear pulse are also available to the work area for use as a time base and reset signal respectively.

Logic diagrams and physical layout drawings are provided in the Peripheral Controller Manual as a guide to implementing all of the logic functions common to most bi-directional devices. 54 integrated circuit connectors with wirewrap pins are provided for the implementation of this logic together with the integrated circuits required. In addition, a total of 89 unassigned dual-in-line integrated circuit connectors are provided on the same printed circuit card. These may be used for the custom logic required for each controller, in addition to that portion of the general purpose logic implemented.

The general-purpose controller is packaged on a 7" x 14½" printed circuit card. It contains dual in-line integrated circuit connectors for all logic circuits. Power and ground are distributed by printed wiring. The number of connectors available for custom wiring is:

PINS	CONNECTORS	POWER AND GROUND CONNECTED
14	64	Yes
16	18	Yes
16	7	No
26	8	No

The power connections are +5V, pin 14 and ground, pin 7. The 26-pin connectors are at the front edge of the card and are available for connecting twisted pair cables between the controller and eight 106-pin I/O cable connectors mounted in the back of the enclosure. These eight connectors and standard I/O cables are used for connecting peripheral devices to the controller. The 16-pin connectors which are not tied to the power or to ground are used for cable terminating resistors.

## Interfacing Through the Modular Bus Control

### Features

The MODCOMP I and II computers provide a unique input/output control capability that allows control of the system resources from a ROM or hardwired control logic. An external interface is provided not only for data lines,

but also for the micro-control functions in the processor. Control lines are available to perform the following functions:

- Enable any available source to the "A" input of the Arithmetic Logic Unit (ALU)
- Enable any available source to the "B" input of the ALU
- Control the function performed in the ALU
- Control the output gating
- Control the destination strobe
- Initiate input or output transfer
- Initiate memory read or write cycle

All of the control lines which move data on and off the Modular Bus are available externally. Therefore, data can be moved in any desired manner between input/output, register file and main memory. This capability not only includes that of transferring data in and out of memory on a cycle-stealing basis, but it also provides far more flexibility than a conventional Direct Memory Access. The external controller can generate instructions to cause the processor to operate arithmetically or logically on an input or output bit, byte, or word as part of the transfer process. In addition, since input/output instructions can be generated externally, data can be transferred from one external device to another device, with or without CPU processing, all under external control.

## General Description

The external logic can take control of the system resources by raising the external request line. The next instruction which is accessed will be loaded into the instruction register and the CPU will suspend operation. An acknowledge signal is returned from the CPU to indicate the MBC logic has control. During this period of suspended CPU operation the MBC logic can manipulate the system resources according to the following rules.

### Source "A" Control

Four lines are provided for source A control, two enable and two select. The enable lines must be held high except when the MBC logic is in control. The source A control lines must be held valid and stable a minimum of 160 ns prior to the leading edge of destination strobe and should not be removed prior to the trailing edge of the destination strobe.

### Source "B" Control

Three lines are provided for source B control, one enable and two select. These lines must be held high except when the MBC logic is in control. The source B control lines must be held valid and stable a minimum of 140 ns prior to the destination strobe and should not be removed prior to the trailing edge of the destination strobe.

### Adder Control

Four lines are provided for ALU control. These lines must be held high except when the MBC logic is in control. The ALU control lines must be held valid and stable a minimum of 100 ns prior to the trailing edge of the destination strobe.

A Zero Detect line is provided. This line will be valid a maximum of 140 ns from stable source A, source B and adder control signals may be used for comparing operands, etc.

### Output Control

Three lines are provided for output control. These lines must be held high except when the MBC logic is in control. These lines manipulate the position of each byte when they are presented to the output bus. The output control lines must be held valid and stable a minimum of 50 ns prior to the destination strobe and should not be removed prior to the trailing edge of the destination strobe.

### Destination Control

Three select lines and one strobe line are provided for destination control. When the MBC control logic is active, these lines select the destination to general purpose registers, memory address, memory data, adder register or data out.

The destination select lines must be valid and stable a minimum of 25 ns prior to the leading edge of strobe and must remain valid until after the trailing edge of strobe.

## MBC-Memory Control

Four lines are provided for Memory Control, Memory Request, Memory Data Strobe and Write Request.

To initiate a read memory cycle the following steps are required.

1. Load the memory address register utilizing the MBC source and destination logic.
2. Generate a memory request strobe any time after the memory address register is loaded.
3. Data from memory will be valid and stable no later than 468 ns from the leading edge of the memory request strobe and remain valid until the next memory request.

To write into memory the following steps are required:

1. Load the memory address register using the MBC source and destination logic.
2. Generate a memory request strobe any time after the memory address register is loaded.
3. Load the memory data register using the MBC source and destination logic.
4. Generate a write request strobe.

If memory parity is present, parity will be automatically generated and checked.

## MBC Input/Output

Two I/O request lines are provided, one for input and one for output. The I/O system is asynchronous and initiates and times out the transfers.

### Output

To output a command or data to any controller, the following steps are required:

1. Enable output data, device address, output line and Command/Data line in sync with I/O clock and I/O sync line.
2. Set Output Request with trailing edge of the next I/O clock.

3. Reset I/O Request on the following I/O clock.

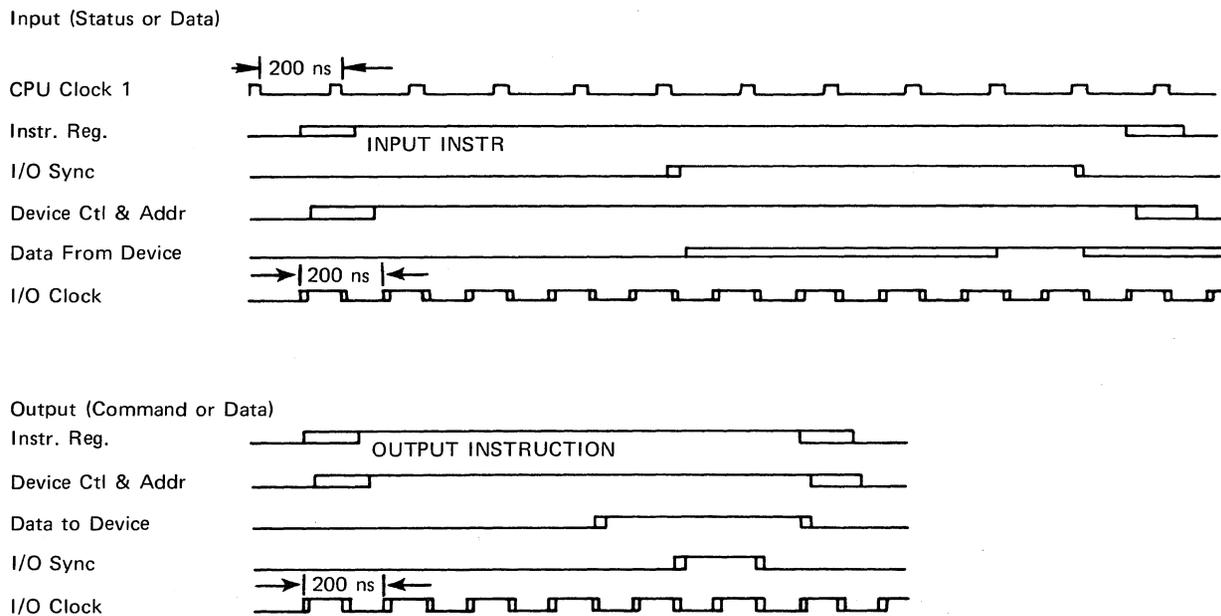
4. Remove or update data and device address on next I/O clock.

### Input

To input data or status from any controller, the following steps are required:

1. Enable device address, input line and command/data line in sync with I/O clock and I/O sync line.
2. Set Input Request with the trailing edge of the same clock.
3. Reset the Input Request with the trailing edge of the next I/O clock.
4. Wait for input acknowledge.

The MODCOMP I/O timing is shown in the following chart:



MODCOMP I/O Timing

## Interfacing Through a Second Memory Port

Very high speed devices such as MODCOMP II central processors, External Direct Memory Processors and user equipment with similar transfer capabilities can be connected directly to a separate memory port. The advantage of a separate path to memory is that a device can be accessing a memory module every cycle time while another device can be accessing a separate module at the same maximum rate through a separate port. Therefore the

operation of one device does not degrade the operation of the other by "stealing cycles," providing that the two devices do not attempt to access the same module. When simultaneous access is attempted, access is granted first to the higher priority device.

The standard MODCOMP devices connectable to memory ports are MODCOMP II CPU's and External DMP's. Other devices can be connected, using the same interface as these devices. This interface consists of a 16-bit parallel data bus, 16-bit parallel address bus, read request, write request, and data ready lines. Devices connected to a separate memory port must be located in the same or adjacent cabinet.

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