MSC 8101
Floppy-Disk Interface/Controller

14 Inverness Drive East
Englewood, Colorado, 80112
(303) 770-7400

MSC 8101

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INTRODUCTION

SECTION 1
INTRODUCTION

1.1 SCOPE

This manual provides information that the user needs to understand the operation of the MSC 8101 Floppy-Disk Interface/Controller.

1.2 UNIT DESCRIPTION

The MSC 8101 is a single-board flexible-disk-drive Interface/ Controller for MULTIBUS* compatible computer systems. It provides all interface and control functions for single-density, hard-sector disk operation -- both single- and dual-head drives. The MSC 8101 is a MULTIBUS interface for regular (8-inch) or mini (4-inch) disk drives such as the Shugart SA800 and SA400.

The MSC 8101 consists of a 6.75- by 12-inch printed-circuit board and cable for two disk drives. A First-In/First-Out (FIFO), full-sector buffer (192-byte capacity) provides timing independence for completely asynchronous computer communication. The FIFO concept allows the computer to read the first byte of data that falls through the buffer. This reduces the latency introduced by other buffering algorithms that require an entire sector to be read before the computer receives data. A higher-priority processor or DMA interface has bus precedence over the MSC 8101 at any instant for any length of time without data loss.

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1.2.1 Supporting Software

A complete disk-monitor system is available for the MSC 8001 single-board computer -- MSC 8303 Software Package MSOS. The MSOS disk-monitor software is designed for throughput and reliability. For write operations, MSOS reads to verify positioning and then checks each block of data after it is written. This redundancy enhances system reliability without hindering system operation significantly. Although data confirmation is recommended, the MSC 8101 can be programmed to write data at the full speed of the disk without data verification.

Because new commands and I/O devices are easily interfaced into the system, MSOS can be used as the basis for a disk-based OEM system. The MSC 8101 design permits MSOS to be run as a time-independent task under Real Time Executive. The source code of the MSOS is provided so that an OEM can incorporate it into a system application.

1.3 COMPATIBLE DISK DRIVES

Either Shugart's SA800 (single head) or the SA400 (single head) mini Floppy-Disk drives are compatible with the MSC 8101. For the storage capacity of these drives, see the following table.

MODEL NUMBER		
MSC 8101	SHUGART	STORAGE CAPACITY
303-0191-001	SA800	315K bytes/drive including 128 bytes/sector, 32 sectors/track, 77 tracks
303-0191-002	SA400	80K bytes/drive including 144 bytes/sector, 16 sectors/track, 35 tracks

Tables 1-1 and 1-2 list the jumper requirements to make the Shugart disk drives compatible with the MSC 8101.

SIGNALS	PRIMARY DRIVE*	SECONDARY DRIVE*
T3,T4,T5,T6,T1	Plugged (Shorted)	Open
DS1	Plugged (Shorted)	Open
DS2	Open	Plugged (Shorted)
DS3,DS4	Open	Open
T2	Plugged	Plugged
X	Open	Open
C	Plugged	Plugged
HL	Open	Open
DS	Plugged	Plugged
A	Plugged	Plugged
B	Plugged	Plugged
Z	Open	Open
R	Plugged	Plugged
S	Cut Run	Cut Run
800	Plugged	Plugged
801	Open	Open
D	Open	Open
DC	Open	Open
L	See Note 1	See Note 1

NOTE: 1. When using the MSC 8206 power supply, nothing has to be done concerning jumper L.

2. The primary drive should be placed at the end of the cable connecting the drives to the interface, because the terminators are on this drive.

Table 1-1

SA 800/801 DRIVE JUMPER CONFIGURATION

SIGNAL	PRIMARY DRIVE*	SECONDARY DRIVE
HS (HL) 1-14)	Open	Open
DS11 (2-13)	Jumpered	Open
DS22 (3-12)	Open	Jumpered
DS3 (4-11)	Open	Open
MX (5-10)	Open	Open
(6-9)	Not Used	Not Used
HM (MH) (7-8)	Jumpered	Jumpered
RESISTOR PACK	Installed	Removed

NOTE: 1. The primary drive should be placed at the end of the cable connecting the drives to the interface, because the terminators are on this drive.

Table 1-2
SA400 DRIVE JUMPER CONFIGURATION

1.4 SPECIFICATIONS

FORMAT: Supports single-density, double frequency recording format for hard-sector disks -- regular (32 sector) and mini (16 sector).

BUFFER: Full sector FIFO buffer for real-time applications (192 bytes maximum).

FUNCTIONS: On-board sector/index separator.
On-board read data/clock separator.
Automatic-head unload time out.
Motor ON/OFF control for DC drives.

SUPPORTING SOFTWARE: MSC 8303 (MSOS, a ROM resident, disk monitor system.

CABLE: Mini Floppy-34 conductor cable with connectors for two drives. Regular Floppy-50 conductor cable with connectors for two drives.

CONNECTORS: MULTIBUS - 86-pin edge connector.
Disk Drive - 50-pin connector.

DC POWER REQUIREMENTS: DC voltages obtained from MULTIBUS.
+5 VDC 850 mA (typ.); 1.7A (max.)
-12 VDC 72 mA (max.)

PHYSICAL DIMENSIONS: 12-in. (width) X 6.75-in. (height) X 0.5-in. (thickness)

MULTIBUS

SECTION 2
MULTIBUS

2.1 SCOPE

This section gives a brief description of the MULTIBUS convention and how it controls the functions of the MSC 8101.

2.2 MULTIBUS CONVENTION

The MULTIBUS is a set of standard signal lines that interconnect a family of system modules such as processors, memories, and I/O devices. Twenty address lines, sixteen bidirectional data lines, eight parallel interrupt lines, bus-control signals, data-transfer signals, and power distribution lines make up the MULTIBUS. The physical structure of the system bus normally takes the form of a backplane that system modules plug into. Interconnections between modules are usually printed-circuit lines or wire-wrapped connections on a backplane.

A system bus convention may be considered as three buses -- the Data bus, the Address bus, and the Control bus. The Data bus provides the path over which data is transmitted between sources and destinations. Data travels on the Data bus between the CPU and memory, between CPU and I/O devices, between memory and I/O devices, or even between peripheral devices.

The Address bus specifies the sources and destinations of I/O devices or memories located externally to the CPU. When transferring data between a CPU register and an external I/O device or memory, the CPU places the addresses, and then the data transfer takes place.

The Control bus establishes direction and timing of the data to or from the selected I/O device or memory location. Separate control signals are provided for I/O read (IORC/) and I/O write (IOWC/) operations, then slave will respond with XACK to indicate the completion of the requested operation.

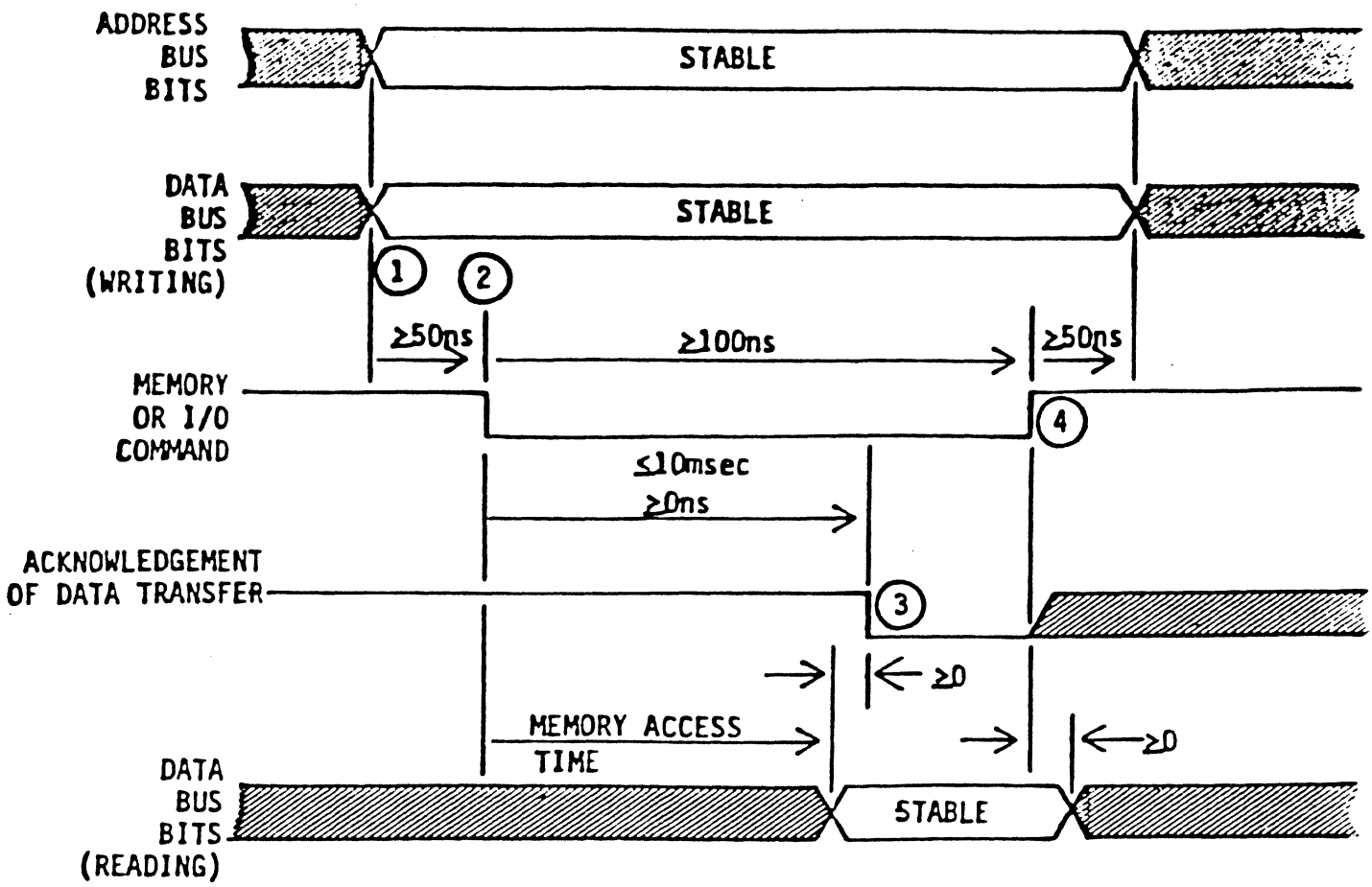
2.3 DATA TRANSFER OPERATIONS

All modules connected to the MULTIBUS behave in a master/slave relationship. At any given time, only one device has control of the MULTIBUS, and this device is referred to as the bus master. The bus master drives the address bus and the control lines. Also, it can initiate data transfers with other devices on the bus called slaves. Either the master or slave can drive the data bus depending on the direction of the data transfer. A slave never drives the address bus. It merely responds to addresses that are asserted onto the bus by a bus master. The MSC 8101 is an example of a slave module.

2.3.1 Data Transfer Timing

The MULTIBUS data transfer operates on a handshaking principle so that no one module depends on another's internal timing. When the bus master issues a command to either read from or write into a specified location, the bus master waits in a state of suspension until the MSC 8101 acknowledges (XACK/) that the transfer is complete.

The sequence of a data transfer operation to the MULTIBUS is as follows (Refer to Figure 2-1):



Circled numbers correspond to sequence steps outlined in paragraph 2.3.1.

Figure 2-1
MULTIBUS DATA TRANSFER TIMING

1) The address bus must be stable and if data is to be written, the data bus must also stabilize.

2) Either IOWC/ (write) or IORC/ (read) is asserted 50 nanoseconds later (minimum).

3) The command remains asserted until the MSC 8101 responds with an acknowledge (XACK/). Acknowledge signal XACK/ is asserted as soon as the MSC 8101 recognizes either a read or write command (IORC/ or IOWC/).

4) The address, data, and acknowledge lines must remain stable until the command is complete. The address and data lines must remain stable for at least 50 nanoseconds after the termination of a write operation. For read operations, the data may be removed immediately upon command termination. The acknowledge terminates within 100 nanoseconds of command termination.

2.4 SPECIFICATIONS

A single, 86-pin connector (P1) interconnects all signals listed in paragraph 2.4.4.

2.4.1 Electrical Characteristics

A "low" (nominal 0V) on the active-low bus indicates a logic "1". A slash (/) following the signal mnemonic indicates that the bus signal is active low. Timing and electrical specifications for all signals are listed in Table 2-1.

SIGNAL	DESCRIPTION	MIN.	MAX.	REMARKS
IORC/	Pulse Width	100 ns	-	-
IOWC/	Pulse Width	100 ns	-	-
XACK/	Acknowledge Hold	-	100 ns	Relative to command removal.
ADR0/-ADR7/	Address Line Set Up	50 ns	-	Relative to command assertion.
ADR0/-ADR7/	Address Line Hold	50 ns	-	Relative to command removal.
DAT0/-DAT7/	Write Data Set Up	50 ns	-	Relative to command assertion.
DAT0/-DAT7/	Write Data Hold	50 ns	-	Relative to command removal.
DAT0/-DAT7/	Read Data Set Up	0 ns	-	Relative to XACK/.
DAT0/-DAT7/	Read Data Hold	0 ns	-	Relative to command removal.
DAT0/-DAT7/	Read Data Access	0 ns	-	Maximum is DC.

Table 2-1
MULTIBUS AC REQUIREMENTS

2.4.2 Mechanical Characteristics

The bus connector is an 86-pin edge connector (two rows of 43) with 0.156-inch spacing between pins. Board thickness of the MSC 8101 is nominally 0.062-inches, and spacing between installed boards should be 0.6-inches. Odd-numbered pins are located on the component side or top side of the board, and even-numbered pins on the circuit side or bottom. When viewing the board with the bus connector P1 down, pin 1 is located on the component side to the left.

2.4.3 Signal Specifications

The following specifications are bus standard, and the MSC 8101 meets or exceeds these requirements.

INPUT

High Level Voltage:	2.0V to 5.0V
Low Level Voltage:	0.0V to 0.8V
Leakage Current:	0.04 mA

OUTPUT

High Level Voltage:	2.4V to 5.25V
Low Level Voltage:	0.0V to 0.45V
Leakage Current:	0.1 mA

CAPACITANCE

Maximum bus capacitance is 300 pF on any one line.

2.4.4 Signal Description

Bus connector P1 provides the signal path between the MSC 8101 and the MULTIBUS for the following signals:

PIN	MNEMONIC	DESCRIPTION
1-2	GND	Signal Ground
3-6	+5	+5 VDC
11-12	GND	Signal Ground
14	INIT/	System Initialization signal conditions the MSC 8101 to a known state.
21	IORC/	Read command signal causes the address of data to be transferred from the addressed location into the MULTIBUS data lines.
22	IOWC/	Write command transfers data from the MULTIBUS into the addressed location.
23	XACK/	Transfer acknowledge signal tells the processor that the command is complete.
51-58	ADR0/-ADR7/	The MSC 8101 uses only the eight lower address lines. Bit 0 (ADR0/) is least-significant.
67-74	DATA0/DAT7/	Eight bidirectional data lines that the MSC 8101 uses to transmit or receive data. Bit 0 (DAT0/) is least-significant.
75-76	GND	Signal Ground
79-80	-12	-12 VDC
81-84	+5	+5 VDC
85-86	GND	Signal Ground

PROGRAMMING

SECTION 3
PROGRAMMING

3.1 SCOPE

This section describes the command structure and procedures needed to program a floppy-disk system using the MSC 8101 Interface/Controller.

3.2 COMMAND STRUCTURE

The MSC 8101 accepts from the MULTIBUS an eight-bit command word (DAT0/ thru DAT7/) that either specifies the mode of operation (See Figure 3-1), or contains the data to be exchanged with the MULTIBUS, depending on the mode of operation.

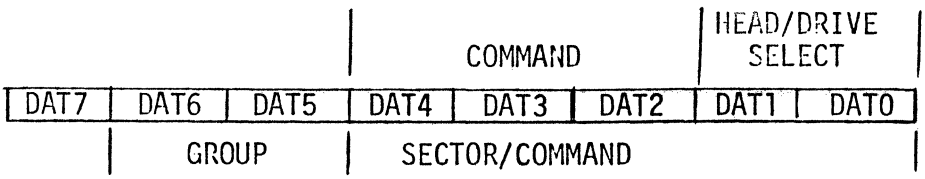


Figure 3-1
COMMAND WORD FORMAT

3.2.1 Group

Bits DAT5 and 6 define four modes of operation -- Reset, Sector Write, Sector Read, and Command operations (Refer to paragraph 3.2.2). The following table lists these modes in terms of the MULTIBUS inputs DAT5/ and DAT6/ (logic "1" represents active "low").

DAT6	DAT5	MODE
0	0	Reset
0	1	Sector Write
1	0	Sector Read
1	1	Command

3.2.2 Command

Bits DAT0 and DAT1 designate the disk drive as follows:

DAT1	DAT0	DRIVE	HEAD
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

Bits DAT2/ thru DAT4/ define eight operations as outlined in the following table. These signals apply only when DAT6 and DAT5 are logic "1" (Command Mode).

DAT4/	DAT3/	DAT2/	
0	0	0	Set up the interface to receive data from the disk-drive system.
0	0	1	Transfer data from the disk system thru the buffer to the processor.
0	1	0	Control the head current.*
0	1	1	Control the head current.*
1	0	0	Turn the drive motor off.*
1	0	1	Turn the drive motor on.* Also used to strobe drive and head select.
1	1	0	Step the head out toward Track 00.
1	1	1	Step the head in toward the inner track (SA800/, Track 76; SA400/, Track 34).

*These commands are not applicable to the SA800 and SA400.

Based on the command word format (Figure 3-1), the complete commands as used in a program to control a disk are:

HEX NOTATION	COMMAND WORD	DESCRIPTION
00	00000000	System Reset
10 + Sector No.	0010ssss	Write Sector "ssss"
40 + Sector No.	0100ssss	Read Sector "ssss"
60 + Command	0110cccc	Perform one of the following Commands, defined by "cccc"
60	01100000	Set Up to Read
64	01100100	Set Up to Write
74 + Unit No.	01110luu	Select Unit "uu"
78	01111000	Step Out Toward Track 00
7C	01111100	Step In Toward Inner Track

3.2.3 Special Considerations

The following points should be considered when programming a floppy disk via the MSC 8101.

1) If a "Motor On" command (Hex 74) is issued, a delay is imposed to guarantee that the sector counter is synchronized with the disk drive.

2) The internal data buffer is automatically reset upon the assertion of either a "Read Sector" or "Setup Write" command. This means that data from the previous transaction is cleared.

3) During the "Step Out" operation, a busy condition (DAT3 is "high") is indicated during the step time until the selected unit reaches Track 00. At that time, the busy condition will be removed. Checking the condition of DAT3 provides a convenient software flag for finding Track 00.

3.3 STATUS REGISTER

An internal, 8-bit register asserts information onto the MULTIBUS to denote functional conditions of the disk drive and the MSC 8101. Designation for each of these bits are as follows:

DAT0 and DAT1 (least-significant bits) are identical to the settings of DAT0 and DAT1 during a "Motor On" command. DAT0 selects the drive and DAT1 the head (Refer to paragraph 3.2.2).

DAT2 indicates the direction of data flow. A "high" signfies Sector Read and a "low" for Sector Write.

DAT3 identifies Track 00 with a "low" placed on the MULTIBUS. For all other tracks, this is "high". If the user does not know the position of the head, it is recommended to "step out" to Track 00 and then "step in" to the desired track.

DAT4 tells the user that the door of the selected unit is open with a "high". This signal is not available on all types of drive.

DAT5 is "high" when the disk media is write protected, inhibiting a write command. This bit must be "low" to perform a write operation.

DAT6 signifies a busy FIFO buffer when "low". A "high" indicates that the buffer is ready for data transfer.

DAT7 (most-significant bit) denotes a busy drive system when "low". A "high" means that the drive will accept a command from the processor.

3.4 PROGRAMMING SECTOR READ

The following procedure is recommended to program a disk drive for Sector Read using the MSC 8101.

1) Verify that the unit is ready to accept a command and transfer data.
2) Confirm that DAT2 of the Status register is "high", signifying that data will flow from the disk drive to the processor.
3) Position the head to the desired track using one of three techniques.
   - Method 1: Step to Track 00, then count into the proper track.
   - Method 2: Store the track number being operated on into the computer. Then use this number to compute through software the number of steps and direction needed for the next track change.
   - Method 3: Record within each sector, a block of information containing the track number. This number will be read out and used to compute the number of steps and direction of movement for the next track change For increase reliability, Method 2 and 3 combined minimizes any errors that could occur due to erroneous stepping.

4) Issue a READ SECTOR command (Hex 40) from the processor with the proper Sector address or number (Refer to paragraph 3.2 and Table 3-1).

DRIVE	HEX ADDRESS	READ	WRITE
4-in. (mini)	D0	Read Data	Write Data
4-in. (mini)	D1	Status	Command
4-in. (mini)	D2	Same as D0	Same as D0
4-in. (mini)	D3	Same as D1	Same as D1
8-in. (regular)	E0	Read Data	Write Data
8-in. (regular)	E1	Status	Command
8-in. (regular)	E2	Same as E0	Same as E0
8-in. (regular)	E3	Same as E1	Same as E1

Table 3-1
I/O ADDRESSES

5) Start testing DAT6 of the status register. When data is ready, DAT6 goes "high", indicating to the processor that data can now be read from the bus.
6) Continue with the read operation until all data within a sector has been read into the computer (132 to 144 usable bytes/sector, depending on the type of floppy disk drive).
7) If there is a further attempt to read more data than contained within a sector, DAT6 of the Status register will be "high" indicating a busy I/O. However, the last byte of data will be read repetitively.

3.5 PROGRAMMING SECTOR WRITE

A Sector Write is accomplished in the following manner:

1) Perform Steps (1) thru (6) of paragraph 3.4 (Sector Read).
2) Establish the write current if the disk drive is so equipped.
3) Send a "Preamble" to synchronize the read electronics. For a standard disk system, the Preamble consists of eight, "0" bytes proceeded by one byte of Hex 80 (decimal 128).
4) Insert data into the buffer. It is recommended that the first byte to be recorded contains the track number for software check (Refer to Method 3 under Step 3 of paragraph 3.4).
5) Send a "Postamble" byte of Hex 00. This will be repeated automatically by the FIFO buffer until the end of the sector.
6) Issue a WRITE SECTOR command (Hex 20) to write the data onto the disk. Even though the program step is complete, it is recommended that the user wait until DAT7 of the Status register goes "high", indicating the interface is not busy and the write operation has actually terminated. Then read the data back for verification. This requires time, but increases reliability. If many blocks of information are being written, it is quicker to write all the information and then check all the data.

THEORY OF OPERATION

SECTION 4
THEORY OF OPERATION

4.1 SCOPE

This section details the theory of operation necessary to understand and use the MSC 8101.

4.2 INTERFACE

The MSC 8101 interfaces with the MULTIBUS through the 86-pin connector, P1 (Refer to Table 2-1), and with the disk drives via J1 (See Figure 4-1 and 4-2). Table 4-1 gives signal and pin indenification of J-1.

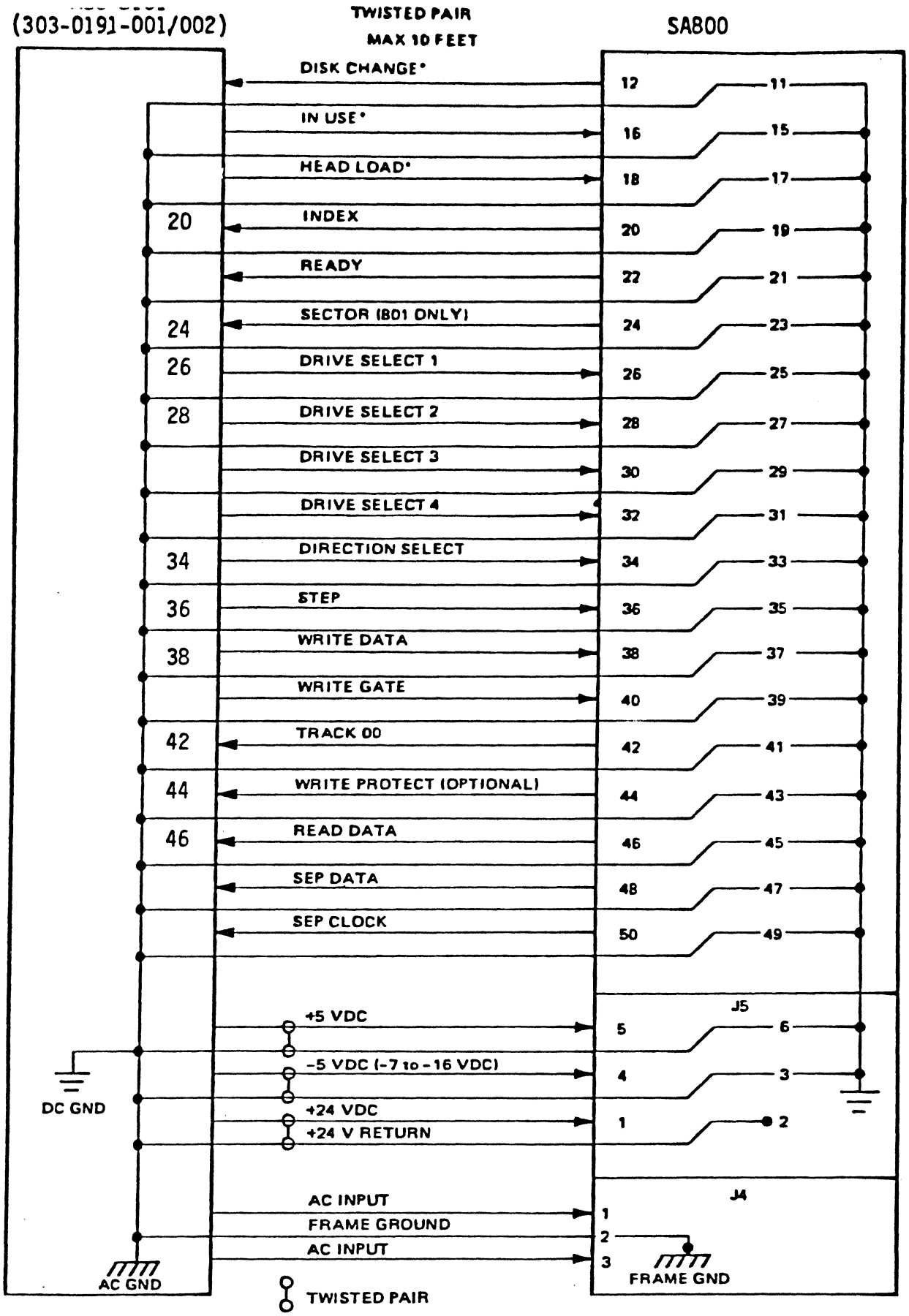
4.3 SYSTEM DESCRIPTION

The MSC 8101 performs either a read or write operation using the following MULTIBUS signals.

1) ADR0/ thru ADR7/ address MSC 8101.
2) DAT0/ thru DAT7/ form the 8-bit data and command word.
3) INIT/ conditions the system to a known state.
4) IORC/ transfers data from the interface to the processor via eight,bi-directional data lines.
5) IOWC/ sends data to the interface via the eight, bi-directional data lines.
6) XACK/ tells the processor to terminate the command.

PIN	SIGNAL	DESCRIPTION
14	HEAD1/	Head select signal
18	HOLD	Hold the head down
20	INDEX/	Index/sector holes
22	DOOR/	Status of the disk-drive door
26	DRIVESEL0/	Select Drive 0
28	DRIVESEL1/	Select Drive 1
32	DMOTON/	Motor On/Off Control
34	DIRECTION	Motional direction of the head
36	STEP/	Step pulse
38	WRITE DATA	Record data onto the disk
42	TK00	Track 00 identification signal
44	WTPROTECT/	Write protect signal
46	READ DATA	Read data recorded on the disk

Table 4-1
DISK-DRIVE INTERFACE SIGNALS



NOTE: Not shown are 6 of the 9 Alternate I/O connections. The connections for these lines are on pins 2, 4, 6, 8, 10, and 14. Signal return for these lines are on pins 1, 3, 5, 7, 9 and 13 respectively. Reference section 7 for uses of these lines.

*These lines are alternate input/output lines and they are enabled by plugs. Reference section 7 for uses of these lines.

Figure 4-1
FLOPPY DISK INTERCONNECTION
(Shugart's SA800)

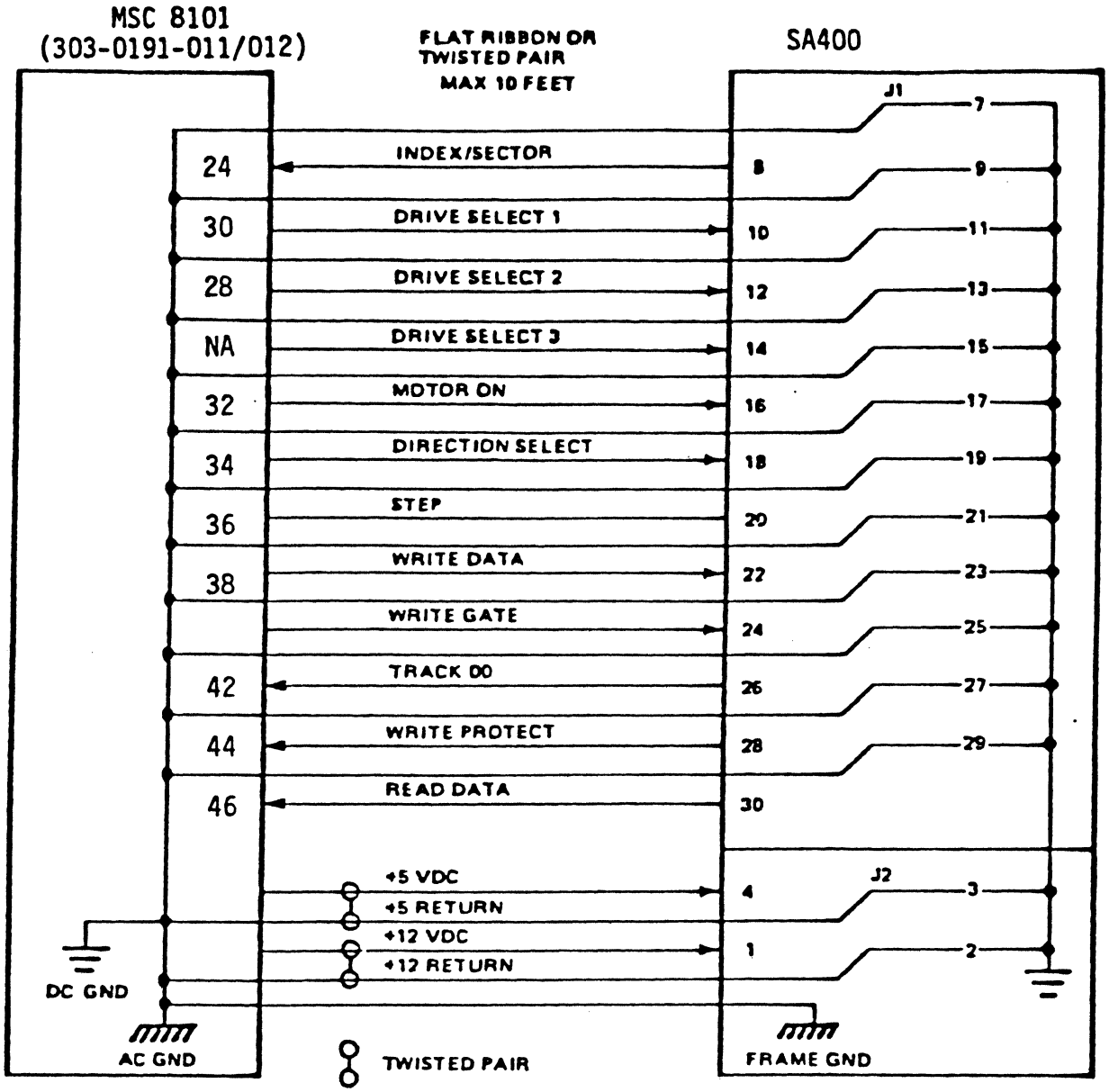


Figure 4-2
MINI FLOPPY INTERCONNECTION
(Shugart's SA400)

4.3.1 Addressing

MULTIBUS outputs ADR2/ thru ADR7/ address the desired MSC 8101 via Comparator U60. These input levels are compared with the board address that is set up on the hardwire-matrix.

4.3.1.1 Sector Address

MULTIBUS signals DAT0/ thru DAT4/ make up the sector address. When the MSC 8101 accepts a command, the address is retained in COMMAND LATCH U53. In turn, SECTOR COMPARATOR accepts these inputs and compares them with the outputs of the SECTOR COUNTER U50. This counter is incremented with a SECTOR INDEX pulse from the disk drive via U40 and U32. Upon reaching the desired sector, pin 9 of U58 (SECTOR) asserts a "high" on pin 2 of the INITIATE gate U13.

4.3.2 Command Decoding

The MULTIBUS asserts command word DAT0/ thru DAT7/ on the inputs of U62 and 63. In turn, these bits are applied to U22 and 23, if the MULTIBUS CONTROL DECODER U64 asserts a "low" on the COMMAND WT/line. This "low" also forces PULSE/ "low" via U46.

4.3.2.1 Group

Circuit U23 establishes one of four operations (Refer to paragraph 3.2.1) through the decoding of B5 and B6. A "low" on both lines of the selected unit (BO's "low") forces pin 12 of U4 "low", setting all circuits to a known state.

4.3.2.2 Command

A "high" on both B5 and B6 denotes that one of eight operations will be used to control the disk (Refer to paragraph 3.2.2). This condition asserts a "low" on the COMMAND ENABLE line, enabling the COMMAND DECODER U22 to decode inputs B2, B3 and B4. With a "high" representing a logic "1" and a "low", a logic "0", these inputs are decided as follows:

B4	B3	B2	OUTPUT SIGNAL (low)	RESULTS
0	0	o	BUSIN/	Set bus for write
0	0	1	BUSOUT/	Set bus for Read
0	1	0	CURROFF/*	
0	1	1	CURRON/*	
1	0	0	MOTOFF/*	
1	0	1	MOTON/*	Turn on drive motor, select head and drive strobe
1	1	0	SOUT/	Step head to Track 00
1	1	1	SIN/	Step head to inner Track

* Not applicable to Shugart's SA800/SA400 drives

4.3.2.3 Data Flow Control

A "low" on BUSIN/ sets BUS DIRECTION flip-flop U21, forcing RDS "high". Signal RDS defines BIT 2 condition of the Status register U44 and 45. This condition implies a read operation and RD/ (complement of RDS) establishes a data flow from the disk through the FIFO DATA BUS onto the MULTIBUS.

A "low" on BUSOUT/ resets U21 to force RDS "low", signifying a write operation. This condition reverses the data flow. Now information goes from the MULTIBUS through the FIFO DATA BUS to the disk drive.

4.3.2.4 Head Current

Some floppy-disk systems, other than Shugart, require the head current to change, depending on the track being written -- the purpose of this command. A "low" on CURROFF/ resets CURRENT SWITCH flip-flop U21. In turn, output signal CURSW/ to the disk drive is asserted "high". When CURRON/ goes "low", U21 is set, forcing CURSW/ "low"/

4.3.2.5 Motor Control

Systems having separate motor control use control level DMOTON/ (J1, pin 32). A "low" on MOTOFF/ resets MOTOR flip-flop, causing DMOTON/ to go "high". When MOTON/ goes "low", U21 is set, forcing DMOTON "low". However, INITIATE signal that initiates either a read or write operation is delayed approximately 5 seconds via MOTOR START TIME U29 so that the disk drive is full speed before the operation begins.

4.3.2.6 Stepping Control

Repeated pulsing on STEP/ (J1, pin 36) moves the head of the disk drive in the direction defined by DIRECTION (J1, pin 34). If the head is to be stepped toward Track 00, the COMMAND DECODER U22 asserts a "low" on SOUT/. This level generates a positive pulse (U29, pin 5) if TK00 is "high" -- signifying that the head is not positioned over Track 00. The rising edge of the pulse triggers U39, asserting a "low" on STEP/ for 12 microseconds.

A "low" on SIN/ moves the head toward the inner-most track. This signal generates the pulse from U29. In turn, a "low" is now asserted on STEP/. Both conditions assert "low" on STEPPING/ and STEP/ -- signals used in the INITIATE gate U13.

4.3.3 Sector Read

The processor starts a sector-read operation, by sending a READ SECTOR command (bit 6 "high", bit 5 "low") with the desired sector number merged in bits 0 thru 4. This causes the head to be loaded if it is not already and starts a search for the addressed sector.

4.3.3.1 Sector Search

After locating the desired track (Refer to paragraph 4.3.2.6) with the selected head, the electronics are ready to be synchronized with the disk-drive circuits and locate the desired sector of information (See paragraph 4.3.1.1). When the addressed sector has been located, INITIATE (U13, pin 6) goes "high" and sets U49 forcing SECTOR FOUND "high" to set FIND FIRST ONE flip-flop(RSYNC goes "high"), initiating the read of the Preamble.

4.3.3.2 FIFO Bus Operation

Data from the disk (READ DATA) is asserted into U32 and the rising edge triggers RCLK. This pulse generates signal SI which allows one byte of data to be placed into the FIFO and on the DATA READ BUS (RD0 thru RD7). If there is no information in the FIFO DATA BUS, RCLK goes "low", forcing IOBSY "low".

Bit 6 of the Status Register indicates this condition (See Paragraph 3.3).

Once the data is in the FIFO, the program can retrieve it through successive reads from the data address. Asserting IORC/ places the data onto the MULTIBUS. After the processor receives the data, it is shifted out of the FIFO so that the next byte can fall through.

4.3.4 Sector Write

When the processor issues a write command to the data address, a "low" as asserted onto the IOWC/ input. The MULTIBUS CONTROL DECODER U64 generates the signal WSTROBE. In turn, WSTROBE generates the signal SO (U36) to permit the MULTIBUS data DO thru D7 to be entered into the FIFO DATA BUS.

When the data for a complete sector is in the FIFO, a WRITE SECTOR command is then asserted to transfer this data from the FIFO to the disk. The processor sends this command (bit 6 "low" and bit 5 "high") with bits 0 thru 4 defining the desired sector. As soon as the sector is located, pin 9 (SECTOR) of the SECTOR COMPARATOR (U58) goes "high", generating the INITIATE signal via U13. The data is then strobed out of the FIFO, one byte at a time into an 8-bit shift register (U47 and 48). In turn, the data is shifted from the shift register one-bit at a time to the disk through data encoder U51 at a bit rate of either 125 or 250 KHz, depending on the type of drive. A crystal oscillator (U7); a divider network, and a jumper interconnect establishes the bit rate.

4.3.5 Status Register

Circuits U44 and 45 asserts 8-bits of data (DO thru D7) onto the MULTIBUS that inform the processor of the operating status of the floppy-disk system. The definition of these bits are shown in Figure 4-3 and discussed in paragraph 3.3.

D7	D6	D5	D4	D3	D2	D1	D0
DRIVE BUSY	I/O BUSY	WRITE PROT.	DOOR	TRACK 00	DATA DIR.	HEAD *	DRIVE

Figure 4-3
STATUS REGISTER FORMAT

When the MULTIBUS CONTROL DECODER U64 asserts a "low" on STAT RD/, the condition of the Status Register is sent to the processor. The UNIT SELECT flip-flop U5 defines bit DO -- a direct relationship to the BO output of the COMMAND LATCH U53. There is a similar affiliation with bit D1 except that D1 is associated with head selection, the output of the HEAD SELECT flip-flop U5.

Bit D2 identifies the direction of data flow as established by the BUS DIRECTON flip-flop. A "high" on D2 signifies a read operation and that data is to be asserted onto the MULTIBUS. A "low" denotes a write and data will be accepted from the MULTIBUS and written onto the disk.

Bit D3 signifies that the head is on Track 00 with a "high". A "low" asserted on J1, pin 22 (DOOR/) controls Bit D4 via gate U2 and 14. Bit D5 is the result of input-level WTPROTECT/ applied to pin 44 of J1. This level forces DRIVE BUSY/ "low" via gates U11 and 13, causing Bit D7 to indicate a busy drive system (Refer to paragraph 3.3). Other signals that effect D7 are output of READ flip-flop; WRITE/, and MOTOR START TIMEOUT flip-flop. These signals control the output of U13. For IOBSY indication, D6 is "low" denoting that the FIFO buffer is busy. This bit goes "high" when the buffer is ready for data transfer.

WARRANTY

SECTION 5
WARRANTY

5.1 SCOPE

Monolithic Systems Corporation (MSC) warrants for a period of twelve (12) months from the data of shipment that each item of equipment (except those materials supplied by Buyer) shall be free from defects in materials and workmanship under normal use and service. Any equipment which is not as warranted may be returned to MSC at MSC's risk and expense for repair or replacement.

If the Buyer establishes that any one of the items of equipment is not as warranted above in order to benefit from the warranty, the Buyer shall advise MSC in writing during the warranty period describing in detail the defect claimed. MSC shall thereafter be afforded the opportunity, for a reasonable period of time after the defective equipment is returned to MSC's place of manufacture, to modify, adjust or repair such item of equipment in order to render it in conformity with the above warranty. If at the end of such period, the Buyer establishes that such item of equipment is still not in conformity with the above warranty, then MSC shall replace the defective item at its expense or may refund the purchase price of such item of equipment to the Buyer. The Buyer recognizes that the remedy of refund of the purchase price in the case of the breach by MSC of the above warranty constitutes the sole and exclusive remedy to the Buyer for such breach. Equipment may consist in whole or in part, of refurbished components which are warranted equivalent to new when used for the purposes intended.

This warranty shall immediately terminate if the equipment is subjected to misuse, neglect, accident, damage in transit, transported in other than MSC authorized containers, or is altered, repaired or overhauled by any person other than MSC.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, PROMISES, AFFIRMATIONS OR REPRESENTATIONS, WHATSOEVER, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR IMPLIED WARRANTY OF FITNESS OF EQUIPMENT FOR A PARTICULAR PURPOSE, AND OF ANY OTHER OBLIGATIONS ON THE PART OF THE SELLER.

DRAWINGS

REVISIONS				
REV	ECO	DESCRIPTION	DATE	APP.
B	1948	UPDATE TO NEW FORMAT DC 12/28/79	1-11-80	MOH
C	2197	REVISED PER ECO	6-24-80	WP

5. SERIAL NUMBER IS TO BE MARKED IN A CLEAR AREA WITH NO DUPLICATIONS.

4. STAMP APPROPRIATE DASH NO. AND DRAWING REVISION LEVEL, ON THE COMPONENT SIDE OF THE P.C. BOARD ASSEMBLY NEAR THE "303" NUMBER SHOWN IN ETCH OR SILKSCREEN, AS SHOWN UNDERLINED IN THE EXAMPLE. (EXAMPLE: 303-0000-XXX REV. A).

3. CROSS REF. VALUES PER DASH NO. ARE SHOWN ON 305-0191-000, SHT. 8.

2. DASH NUMBERS: -002 Shugart SA400 COMPATIBLE.
-001 Shugart SA800 COMPATIBLE.

1. SEE JUMPER TABLE FOR APPROPRIATE JUMPER INSTALLATIONS, SHT. 5.

NOTES: UNLESS OTHERWISE SPECIFIED:

REV STATUS OF SHEETS																										
REV																										
SHEET																										
REV	C	B	B	C	B	C																				
SHEET	1	2	3	4	5	6																				

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:

MATERIAL

		DATE
DRAWN	SFR	7/6/78
CHECKED	Dale C.	8/14/78
APPROVED		1-11-80
APPROVED		

MONOLITHIC SYSTEMS CORP.

P.C. BOARD ASSEMBLY
MSC 8101
FLOPPY DISC

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0191-000

SCALE | REV C | SHEET 1 of 6

MSF-1015 REV A

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
004	003	002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
		1	1	304-0191-001	P.C. BOARD			1
								2
								3
		3	3	210-0504-005	74LS123	U1,U29,U43		4
		1	1	210-0501-005	74LS14	U2		5
		3	3	210-0300-001	7406	U3,U4,U34		6
		8	8	210-0604-005	74LS74	U5,U15,U25,U32,U42,U46, U49,U54		7
		2	2	210-0718-005	74LS197	U6,U18		8
		6	6	210-1040-001	3341	U9,U10,U19,U20,U37,U38		9
		3	3	210-0100-005	74LS00	U11,U51,U52		10
		2	2	210-0200-005	74LS08	U12,U30		11
		3	3	210-0204-005	74LS21	U13,U16,U31		12
		3	3	210-0103-005	74LS04	U14,U33,U61		13
		1	1	210-0642-005	74LS279	U21		14
		2	2	210-0900-005	74LS42	U22,U23		15
		2	2	210-0506-005	74LS221	U24 ,U39		16
		1	1	210-0202-005	74LS11	U28		17
		3	3	210-0916-005	74LS157	U36,U65,U66		18
		1	1	210-0804-005	74LS32	U40		19
		1	1	210-0308-001	7438	U41		20
								21
								22

SIZE A

CODE IDENT NO 51513

DWG NO. 303-0191-000

REV B

SHEET 2

MSF-1015 REV A

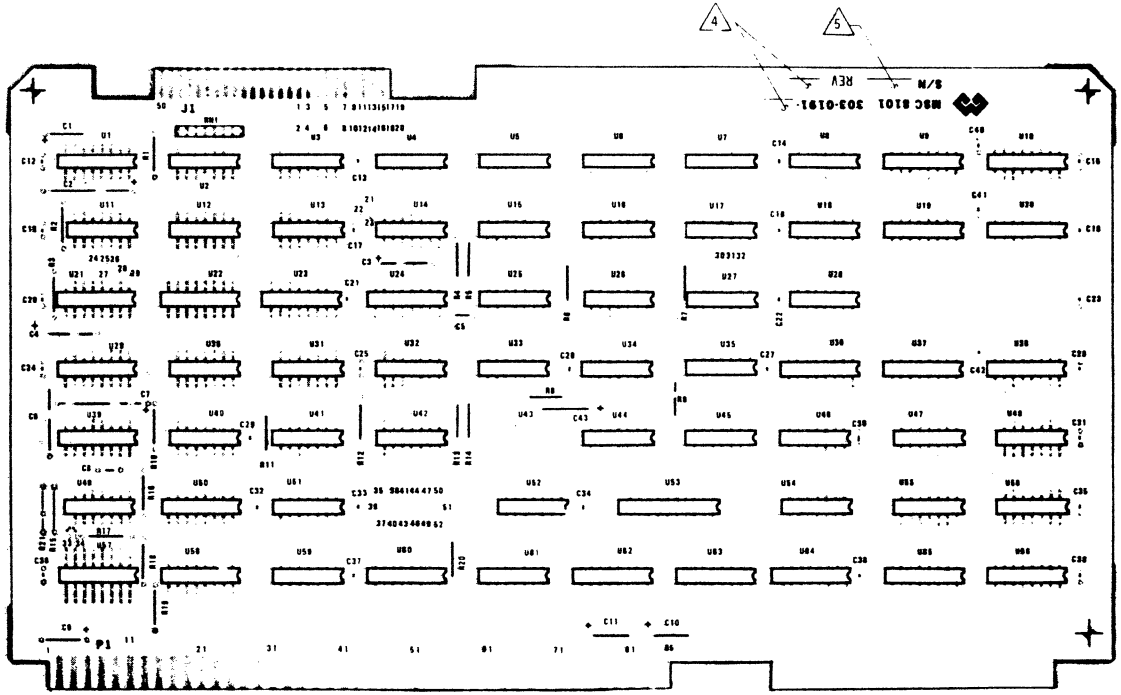
QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
004	003	002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
		2	2	210-0611-005	74LS95	U47,U48		23
		1	1	210-0707-005	74LS163	U50		24
		4	4	210-0400-005	74LS125	U44,U45,U55,U56		25
		1	1	210-0722-005	74LS393	U17		26
		1	1	210-0908-005	74LS138	U64		27
		1	1	210-0651-005	74LS374	U53		28
		1	1	222-0008-002	CRYSTAL OSCILLATOR	U7	K1115A ,16MHZ	29
		2	2	210-0950-001	8160	U58,U60		30
		2	2	210-0414-001	8835	U62,U63		31
		6	6	214-0002-065	RESISTOR, 470Ω, ¼W.,5%	R6,R7,R9,R18,R20 ,R11		32
		1	1	214-0027-250	RESISTOR NETWORK	RN1	220/330	33
		3	3	SAT	RESISTOR, UNSPECIFIED	R4,R13,R21		34
		1	1	214-0002-125	RESISTOR, 150K, ¼W. 5%	R1	3	35
		3	3	214-0002-081	RESISTOR, 2.2K, ¼W. 5%	R12,R17,R19		36
		-	1	214-0002-106	RESISTOR, 24K, ¼W. 5%	R3	3	37
		-	1	214-0002-121	RESISTOR, 100K, ¼W. 5%	R2	3	38
		-	1	214-0002-130	RESISTOR, 240K, ¼W. 5%	R10	3	39
		-	2	214-0002-113	RESISTOR, 47K, ¼W. 5%	R8,R14	3	40
		-	1	214-0002-109	RESISTOR, 33K ¼W. 5%	R15	3	41
		-	1	214-0002-092	RESISTOR, 6.2K, 1/4W, 5%	R5	3	42
								43
								44

SIZE A | CODE IDENT NO 51513 | DWG NO. 303-0191-000 | REV B | SHEET 3

MSF-1015 REV A

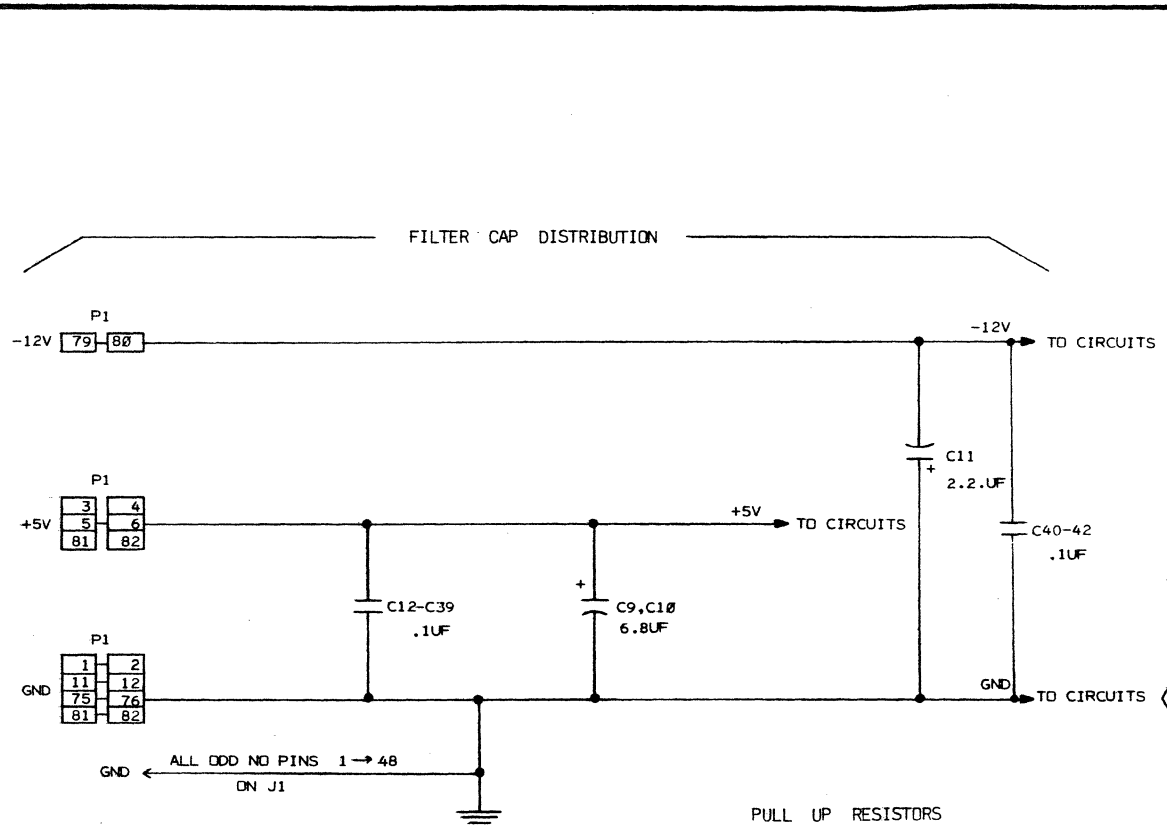
QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
004	003	002	001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
		1	-	214-0002-130	RESISTOR, 240K, ¼W, 5%	R2	3	45
		4	-	214-0002-121	RESISTOR, 100K, ¼W, 5%	R3,R8,R10,R14	3	46
		1	-	214-0002-117	RESISTOR, 68K, ¼W, 5%	R15	3	47
		1	1	214-0002-113	RESISTOR, 47K, ¼W, 5%	R16	3	48
		1	-	214-0002-101	RESISTOR, 15K , ¼W, 5%	R5	3	49
								50
		4	4	201-0007-065	CAPACITOR, 1uf, ±5%	C1,C3,C4,C43	3	51
		2	2	201-0006-045	CAPACITOR, 100pf, ±5%	C5,C8	3	52
		1	1	201-0002-033	CAPACITOR, .01uf, ±5%	C6	3	53
		2	2	201-0018-001	CAPACITOR, 6.8uf,	C9,C10		54
		1	1	201-0018-002	CAPACITOR, 2.2uf,	C11		55
		31	31	701-0001-003	CAPACITOR, .1uf	C12-C42		56
		2	2	201-0001-014	CAPACITOR, 33uf, +20%	C2,C7	3	57
		6	6	204-0059-003	SOCKET, 16 PIN	(U9,10,19,20,37,38)		58
		52	52	208-0085-006	WIRE WRAP POSTS	E1-E52		59
		2	2	208-0063-003	EJECTOR & PIN			60
		-	1	301-0115-001	CABLE, ASSY-50 COND.			61
		1	-	301-0116-001	CABLE, ASSY-34 COND.			62
								63
		REF	REF	305-0191-000	SCHEMATIC			64

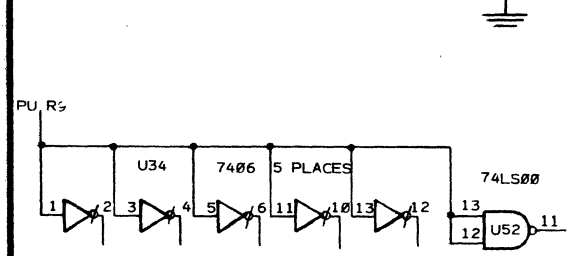
SIZE A
CODE IDENT NO 51513
DWG NO. 303-0191-000
REV C
SHEET 4

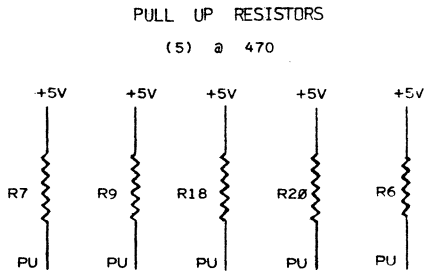


MONOLITHIC SYSTEMS CORP.			
SIZE	CODE IDENT NO.	DWG NO.	REV
C	51513	303-0191-000	C
SCALE 1/1		SHEET 6	

REVISIONS				
LTR	ECO	DESCRIPTION	DATE	APPRV'D
B	1948	ENG RELEASE	1-11-80	
C	2197	REVISED PER ECO.	6-24-80	







(7) CROSS REF. VALUES PER DASH NO. ARE SHOWN ON SHT. 8.

-002, SHUGART SA400 COMPATIBLE.

6. -001, SHUGART SA800 COMPATIBLE.

(5) REFER TO SHEET 8 OF THIS DWG. FOR TIMING COMPONENT VALUES NOT SPECIFIED.

4. THE SYMBOL [XX] REPRESENTS P1.
   THE SYMBOL (XX) REPRESENTS J1.

3. LAST REF. DESIG. USED: U66, C43, RN1 — REF. DESIG. NOT USED: U8, U26, U27, U35, U57, U59

2. PULL UP RESISTORS ARE DESIGNATED AS "PU R( )"; PULL UP CONFIGURATIONS ARE SHOWN ON SHEET 1.

1. ALL RESISTORS ARE 1/4W, 5% UNLESS OTHERWISE SPECIFIED.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	C	B	B	B	B	B	B	C
SHEET	1	2	3	4	5	6	7	8

REVISION STATUS OF SHEETS

DRAWN		
CHECKED		
APPROVED		1-11-80
APPROVED		

MONOLITHIC SYSTEMS CORP.
Englewood, Colorado 80110

TITLE: P.C. BOARD SCHEMATIC
MSC 8101
FLOPPY DISC

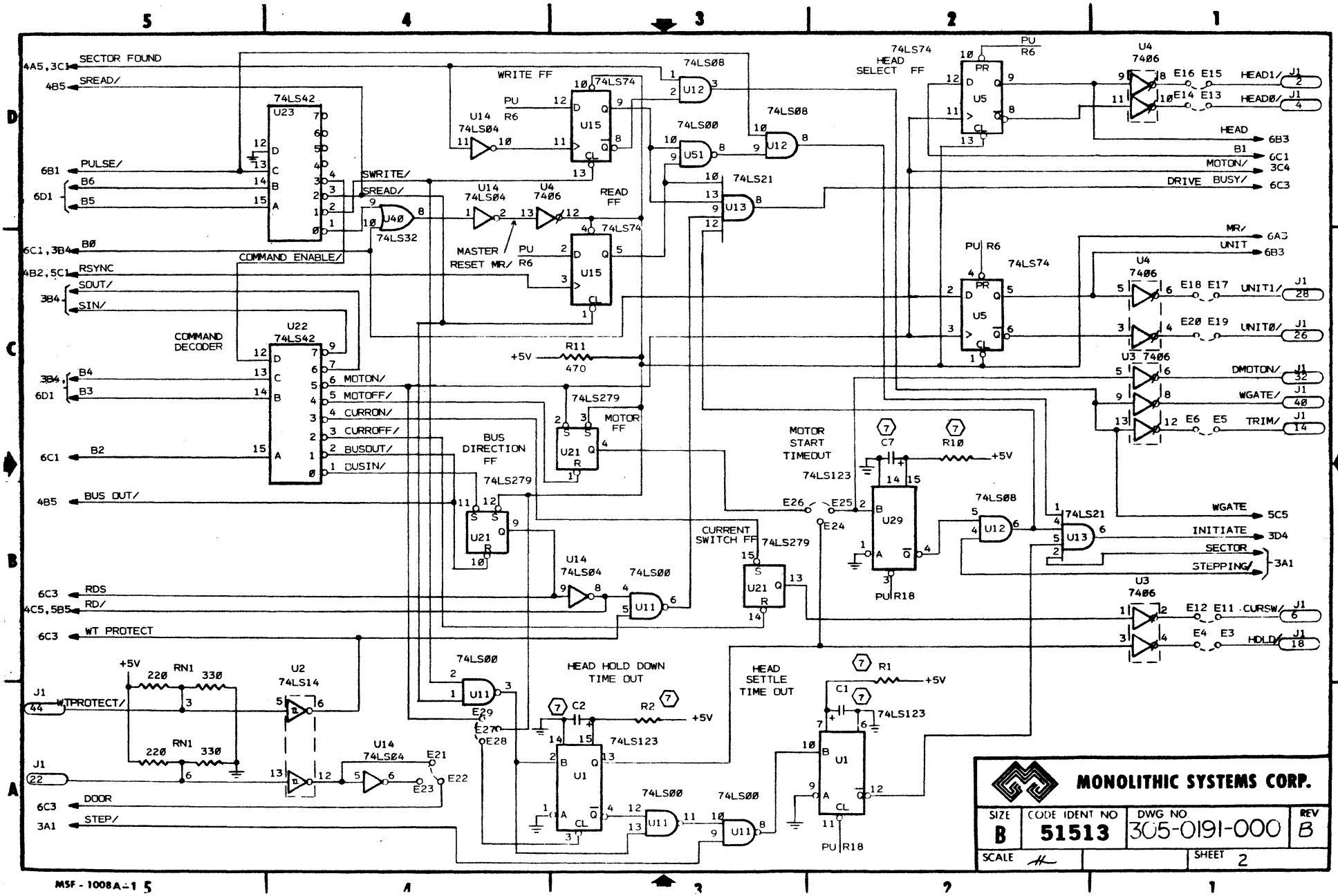
SIZE	CODE IDENT NO.	DWG NO.	REV
B	51513	305-0191-000	C

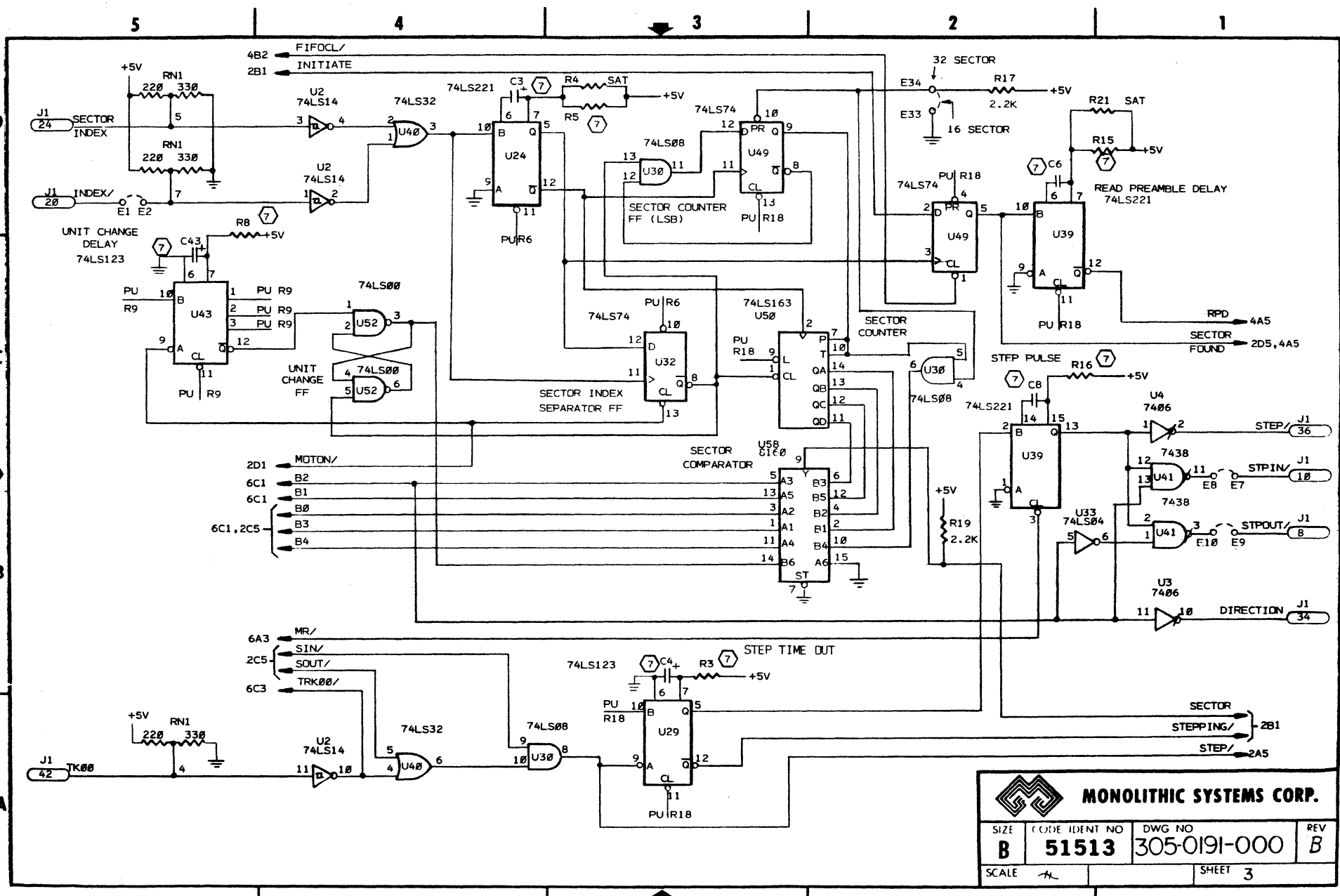
SCALE: — SHEET 1 of 8

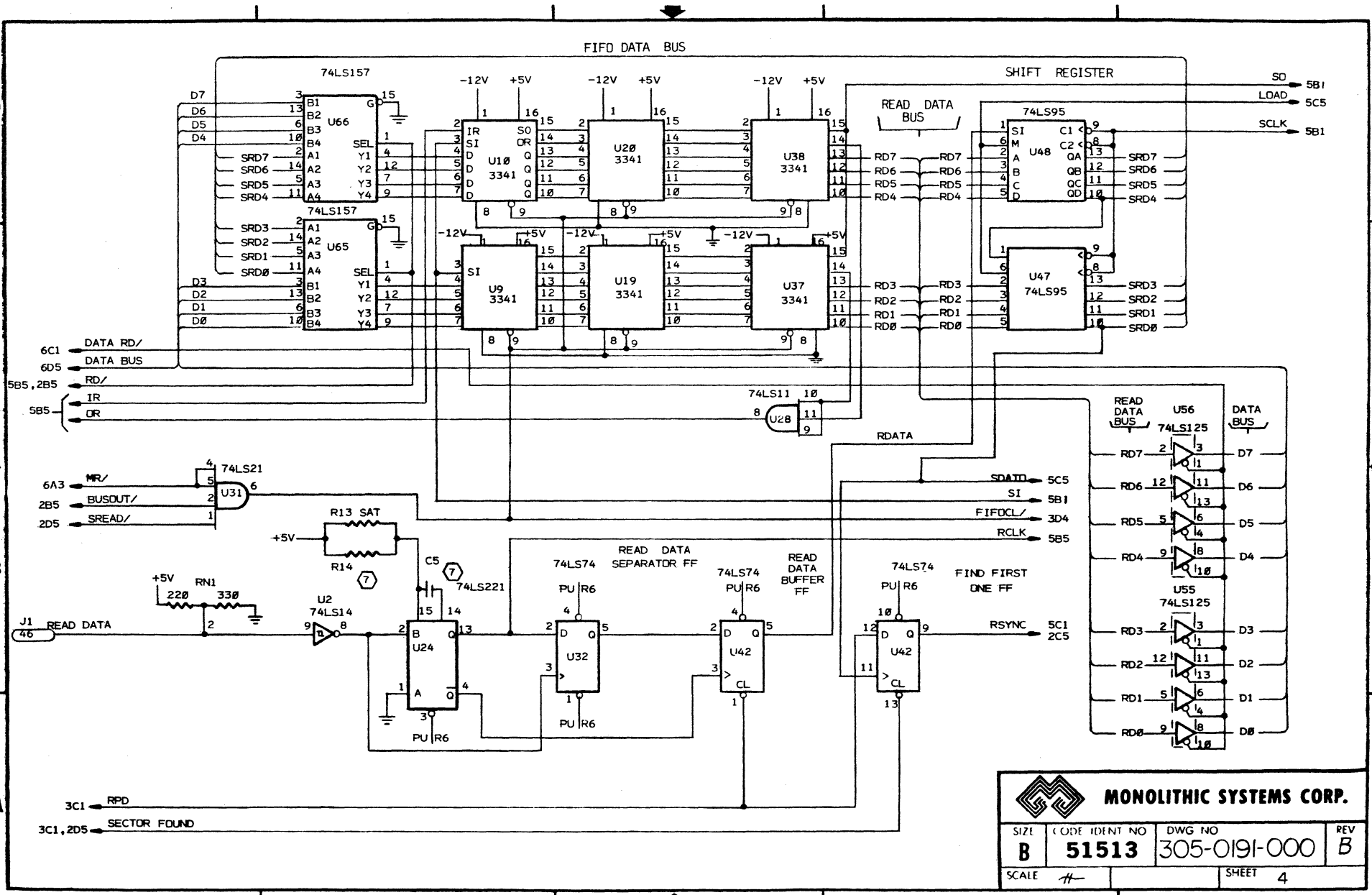
LAST USED									
NOT USED									
LAST USED									
NOT USED									

REFERENCE DESIGNATIONS LAST USED/NOT USED

MSF 1052

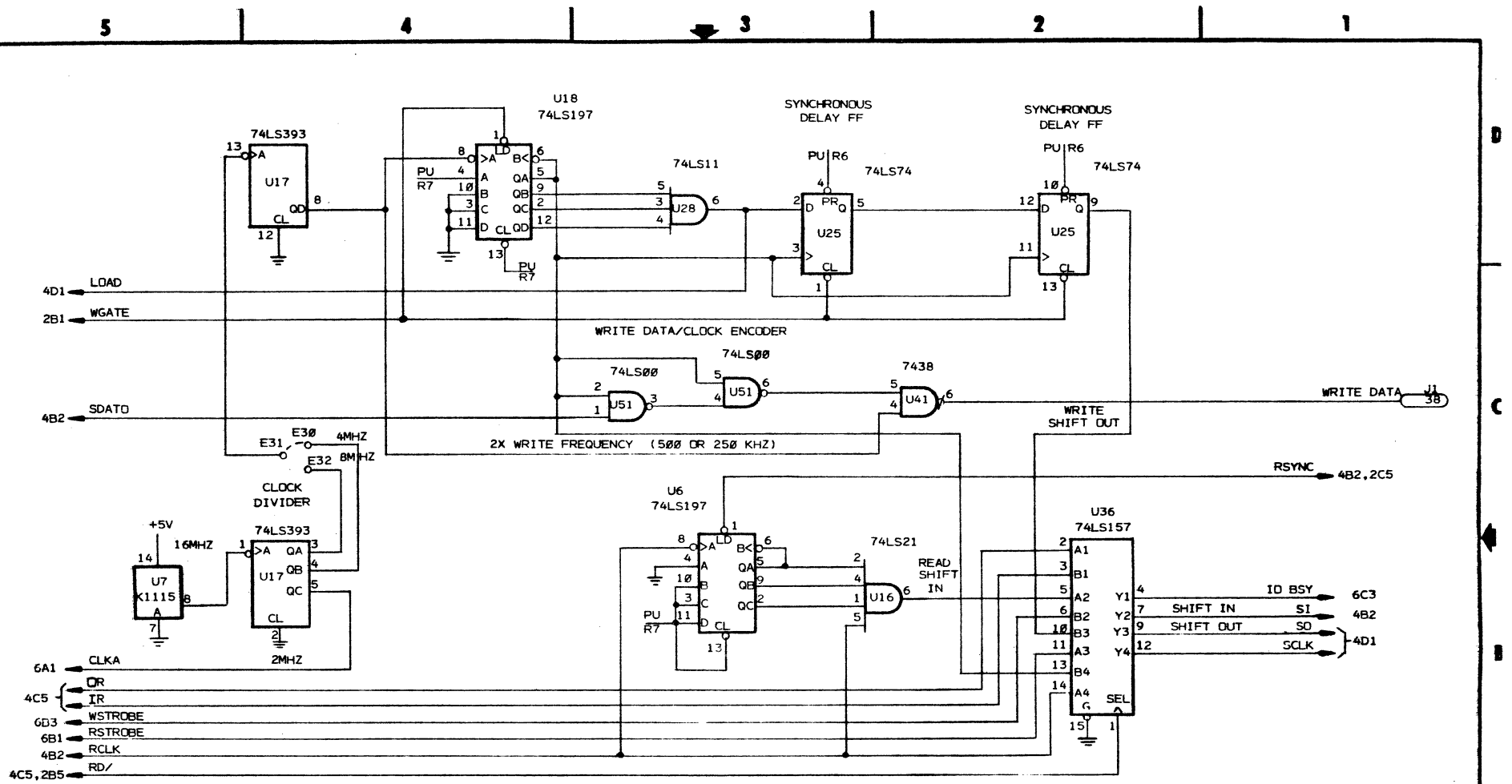

SECTOR FOUND
SREAD/
PULSE/
B6
B5
B0
COMMAND ENABLE/
RSYNC
SOUT/
SIN/
COMMAND DECODER
B4
B3
B2
BUS OUT/
RDS
RD/
WT PROTECT
WTPROTECT/
DOOR
STEP/
MOTON/
MOTOFF/
CURRON/
CURROFF/
BUSOUT/
BUSIN/
SWRITE/
WRITE FF
READ FF
MASTER RESET MR/
MOTOR FF
BUS DIRECTION FF
CURRENT SWITCH FF
MOTOR START TIMEOUT
HEAD HOLD DOWN TIME OUT
HEAD SETTLE TIME OUT
HEAD SELECT FF
HEAD1/
HEAD0/
HEAD
B1
MOTON/
DRIVE BUSY/
MR/
UNIT
UNIT1/
UNIT0/
DMOTON/
WGATE/
TRIM/
WGATE
INITIATE
SECTOR
STEPPING/
CURSW/
HDLD/
MONOLITHIC SYSTEMS CORP.
SIZE B
CODE IDENT NO 51513
DWG NO 305-0191-000
REV B
SCALE
SHEET 2
MSF - 1008A-1


FIFOCL/
INITIATE
32 SECTOR
16 SECTOR
SECTOR INDEX
INDEX/
UNIT CHANGE DELAY 74LS123
SECTOR COUNTER FF (LSB)
SECTOR INDEX SEPARATOR FF
UNIT CHANGE FF
SECTOR COUNTER
READ PREAMBLE DELAY 74LS221
STEP PULSE
SECTOR COMPARATOR
MOTON/
STEP TIME OUT
RPD
SECTOR FOUND
STEP/
STPIN/
STPOUT/
DIRECTION
MR/
SIN/
SOUT/
TRK00/
TK00
SECTOR
STEPPING/
MONOLITHIC SYSTEMS CORP.
SIZE B
CODE IDENT NO 51513
DWG NO 305-0191-000
REV B
SCALE
SHEET 3
MSF - 1008A-1

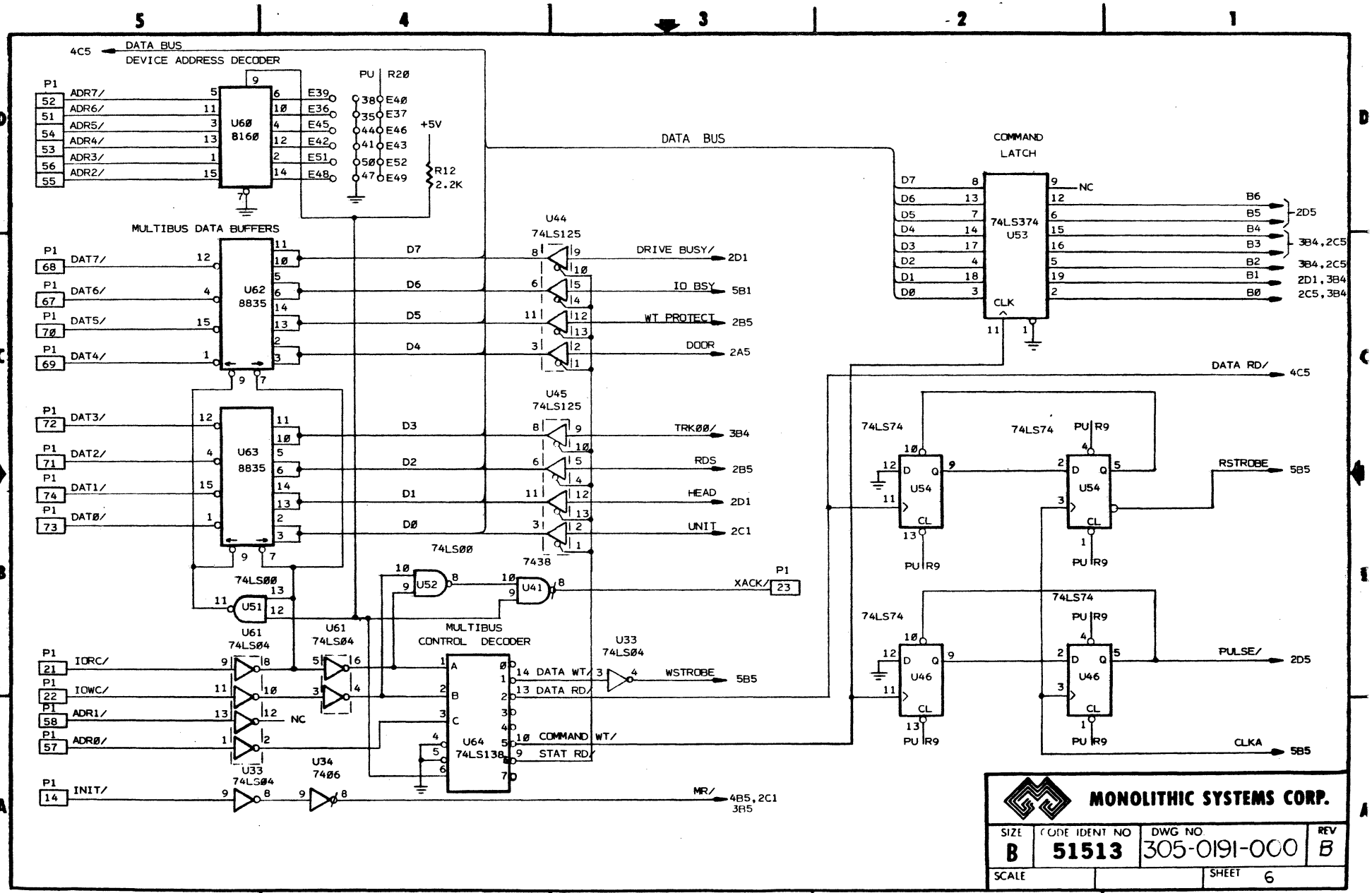


MONOLITHIC SYSTEMS CORP.			
SIZE B	CODE IDENT NO 51513	DWG NO 305-0191-000	REV B
SCALE #—		SHEET 4	

MSF-1008A-1



MONOLITHIC SYSTEMS CORP.			
SIZE B	CODE IDENT NO 51513	DWG NO 305-0191-000	REV B
SCALE		SHEET 5	


4C5 DATA BUS
DEVICE ADDRESS DECODER
P1
ADR7/
ADR6/
ADR5/
ADR4/
ADR3/
ADR2/
U60 8160
PU R20
+5V
R12 2.2K
MULTIBUS DATA BUFFERS
DAT7/
DAT6/
DAT5/
DAT4/
DAT3/
DAT2/
DAT1/
DAT0/
U62 8835
U63 8835
U44 74LS125
U45 74LS125
DRIVE BUSY/ 2D1
IO BSY 5B1
WT PROTECT 2B5
DOOR 2A5
TRK00/ 3B4
RDS 2B5
HEAD 2D1
UNIT 2C1
74LS00
74LS00
U51
U52
U41
7438
XACK/ 23
U61 74LS04
U61 74LS04
MULTIBUS CONTROL DECODER
U33 74LS04
IORC/
IOWC/
ADR1/
ADR0/
NC
U64 74LS138
14 DATA WT/
13 DATA RD/
10 COMMAND WT/
9 STAT RD/
WSTROBE 5B5
U33 74LS04
U34 7406
INIT/
MR/ 4B5, 2C1 3B5
DATA BUS
COMMAND LATCH
74LS374 U53
D7
D6
D5
D4
D3
D2
D1
D0
CLK
NC
B6
B5
B4
B3
B2
B1
B0
2D5
3B4, 2C5
3B4, 2C5
2D1, 3B4
2C5, 3B4
DATA RD/ 4C5
74LS74
U54
PU R9
RSTROBE 5B5
74LS74
U46
PULSE/ 2D5
CLKA 5B5
MONOLITHIC SYSTEMS CORP.
SIZE B
CODE IDENT NO 51513
DWG NO 305-0191-000
REV B
SCALE
SHEET 6
MSF - 1008A-1

DEVICE TYPE NO.	REFERENCE DESIGNATION	NOTE	POWER & GROUND								REMARKS/SPARES	LINE NO.
			GND	+5V	-12V							
74LS00	U11,U51,U52		7	14							U52- 1 SPARE	1
74LS04	U14,U33,U61		7	14							U14- 2 SPARES U33- 3 SPARES	2
7406	U3,U4,U34		7	14								3
74LS08	U12,U30		7	14							U12- 1 SPARE U30- 1 SPARE	4
74LS11	U28		7	14							U28- 1 SPARE	5
74LS14	U2		7	14							U2 - 1 SPARE	6
74LS21	U13,U16,U31		7	14							U16- 1 SPARE U31- 1 SPARE	7
74LS32	U40		7	14							U40 - 1 SPARE	8
7438	U41		7	14								9
74LS42	U22,U23		8	16								10
74LS74	U5,U15,U25,U32,U42,U46, U49,U54		7	14								11
74LS95	U47,U48		7	14								12
74LS123	U1,U29, U43		8	16							U43 - 1 SPARE	13
74LS125	U44,U45,U55,U56		7	14								14
74LS138	U64		8	16								15
74LS157	U36,U65,U66		8	16								16
74LS163	U50		8	16								17
74LS197	U6,U18		7	14								18
74LS221	U24,U39		8	16								19
74LS279	U21		8	16							U21 - 1 SPARE	20
74LS374	U53		10	20								21
74LS393	U17		7	14								22
8160	U58,U60		8	16								23
3341	U9,U10,U19,U20,U37,U38		8	16	1							24
8835	U62,U63		8	16								25
K1115A	U7		7	14								26
220/330	RN1		8	1								27

DEVICE TYPE NO.	REFERENCE DESIGNATION	NOTE	POWER & GROUND							REMARKS/SPARES	LINE NO.
			GND	+5V							

MONOLITHIC SYSTEMS CORP.

SIZE	CODE IDENT NO	DWG NO.	REV
B	51513	305-0191-000	B
SCALE		SHEET 7	

SHEET LOCATION	SIGNAL	⑤	⑦ SA800 001	⑦ SA400 002	⑦ SA850 003	⑦ SA450 004
2C2	MOTOR START TIMEOUT		2.4SEC	1.0SEC		
2A3	HEAD HOLD DOWN TIMEOUT		800MS	2.2SEC		
2A2	HEAD SETTLE TIMEOUT		50MS	50MS		
3C5	UNIT CHANGE DELAY		15MS	30MS		
3D4	SECTOR-INDEX SEPARATOR		3.7MS	8.9MS		
3D2	READ PREAMBLE DELAY		200US	400US		
3C2	STEP PULSE		2US	2US		
3B3	STEP TIMEOUT		8MS	40MS		
4B4	READ DATA SEPARATOR		2.84US	5.68US		
2C2	MOTOR START TIMEOUT	C7	33UF	33UF		
		R10	240K	100K		
		T	2.4SEC	1.0SEC		
2A3	HEAD HOLD DOWN TIMEOUT	C2	33UF	33UF		
		R2	100K	240K		
		T	800MS	2.2SEC		
2A2	HEAD SETTLE TIMEOUT	C1	1UF	1UF		
		R1	150K	150K		
		T	50MS	50MS		
3C5	UNIT CHANGE DELAY	C43	1UF	1UF		
		R8	47K	100K		
		T	15MS	30MS		

SHEET LOCATION	SIGNAL	⑤	⑦ SA800 001	⑦ SA400 002	⑦ SA850 003	⑦ SA450 004
3D4 3D3	SECTOR INDEX SEPARATOR	C3	1UF	1UF		
		R5	6.2K	15K		
		T	3.7MS	8.9MS		
3D2	READ PREAMBLE DELAY	C6	.01UF	.01UF		
		R15	33K	68K		
		T	200US	400US		
3C2	STEP PULSE	C8	100PF	100PF		
		R16	47K	47K		
		T	2US	2US		
3B3	STEP TIME OUT	C4	1UF	1UF		
		R3	24K	100K		
		T	8MS	40MS		
4B4	READ DATA SEPARATOR	C5	100PF	100PF		
		R14	47K	100K		
		T	2.84US	5.68US		

MONOLITHIC SYSTEMS CORP.

SIZE	CODE IDENT NO	DWG NO	REV
B	51513	305-0191-000	C

SCALE — SHEET 8