MSC 8204

Universal Card

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MSC 8204

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SECTION 1
INTRODUCTION

1.1 SCOPE

This manual provides the design engineer with information on how to use the MSC 8204 Universal Card for custom prototyping of MULTIBUS* compatible systems.

1.2 UNIT DESCRIPTION

The MSC 8204 will hold a matrix of wirewrap sockets that accommodate any length components on width of 0.3, 0.4 and 0.6 inches. The mechanical dimensions and pin callouts are the same as the MSC 8001 for the MULTIBUS interconnection -- one, 26-pin I/O connector and two, 50-pin I/O connectors. The MSC 8204 accepts either a standard edge connector or the holes at the bottom of each conductive surface permit the mounting of a right-angle header connector. Power and ground planes terminate on uniformly-spaced pads for ease of access.

1.3 CONTROL LOGIC

The MSC 8204 contains its own programmable, bus-master control system. Full address decoding permits the use of either memory mapped or normally isolated I/O addressing. Also, the MSC 8204 contains Transfer-Acknowledge logic and the option of including inhibits.

*Registered Trade Mark of Intel Corporation

1.4 POWER DISTRIBUTION

Marked printed-circuit pads provide easy access to +5V and ground. Also, -5V and ±12V can be easily connected to a component using the wirewrap pins. Filter capacitors may be installed for additional voltages if required. These capacitors and associated voltages are:

+12 VDC	C2
-5 VDC	C3
-10 VDC	C4
-12 VDC	C5

SECTION 2
MULTIBUS *

2.1 SCOPE

This section gives a brief description of the MULTIBUS convention and how it interfaces with the MSC 8204.

2.2 MULTIBUS CONVENTION

The MULTIBUS* is a standard set of signal lines consisting of twenty, address lines, sixteen, bi-directional data lines, eight, parallel interrupt lines, bus-control signals, data-transfer signals and power distribution. These lines interconnect a family of system modules such as computers, memory boards, I/O boards and a combination of these. A low level (nominal 0V) on these lines represent a logic "1" or bus signals are active low (indicated with a slash "/"). Table 2-1 lists only the signals and pin assignments for P1 (bus connector) that tie the MSC 8204 to the MULTIBUS.

2.3 DATA TRANSFER OPERATIONS

The MULTIBUS data transfer operations work on a hand-shake principal so that no one module depends on another for internal timing. After the computer issues a command to read from or write into the location specified on the address lines, the computer then waits until there is acknowledgement that the transfer has taken place.

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PIN	MNEMONIC	DESCRIPTION
1-2	GND	Signal Ground
3-6	+5	+5 VDC
7-8	+12	+12 VDC
9-10	-5	-5 VDC
11-12	GND	Signal Ground
13	BCLK/	Bus Clock
14	INIT/	Initialize Signal
15	BPRN/	Bus Priority In
16	BPRO/	Bus Priority Out
17	BUSY/	Bus Busy
18	BREQ/	Bus Request
19	MRDC/	Memory Read Command
20	MWTC/	Memory Write Command
21	IORC/	I/O Read Command
22	IOWC/	I/O Write Command
23	XACK/	Transfer Acknowledge Signal
24	INH1/	RAM Inhibit Signal
25	AACK/	Special Acknowledge Signal
26	INH2/	PROM Inhibit Signal
43-58	ADR0/-ADRF/	Address Bus
67-74	DAT0/-DAT7/	Bi-directional Data Lines
75-76	GND	Signal Ground
77-78	-10	-10 VDC
79-80	-12	-12 VDC
81-84	+5	+5 VDC
85-86	GND	Signal Ground

Table 2-1
MULTIBUS SIGNALS (P1)

2.3.1 MULTIBUS Timing

The sequence of a data transfer to and from the MULTIBUS is as follows (Refer to Figure 2-1):

1) The address bus must be stable and if data is to be written, the data bus must also stabilize.
2) Either IOWC/ (write) or IORC/ (read) is asserted 50 nanoseconds later (Minimum).
3) The command remains asserted until there is an acknowledge (XACK/) response. Acknowledge signal XACK/ is asserted as soon as either a read or write command (IORC/ or IOWC/) is recognized.
4) The address, data and acknowledge lines must remain stable until the command is complete. The address and data lines must remain stable for at least 50 nanoseconds after the termination of a write operation. For read operations, the data may be removed immediately upon command termination. The acknowledge terminates within 100 nanoseconds of command termination.

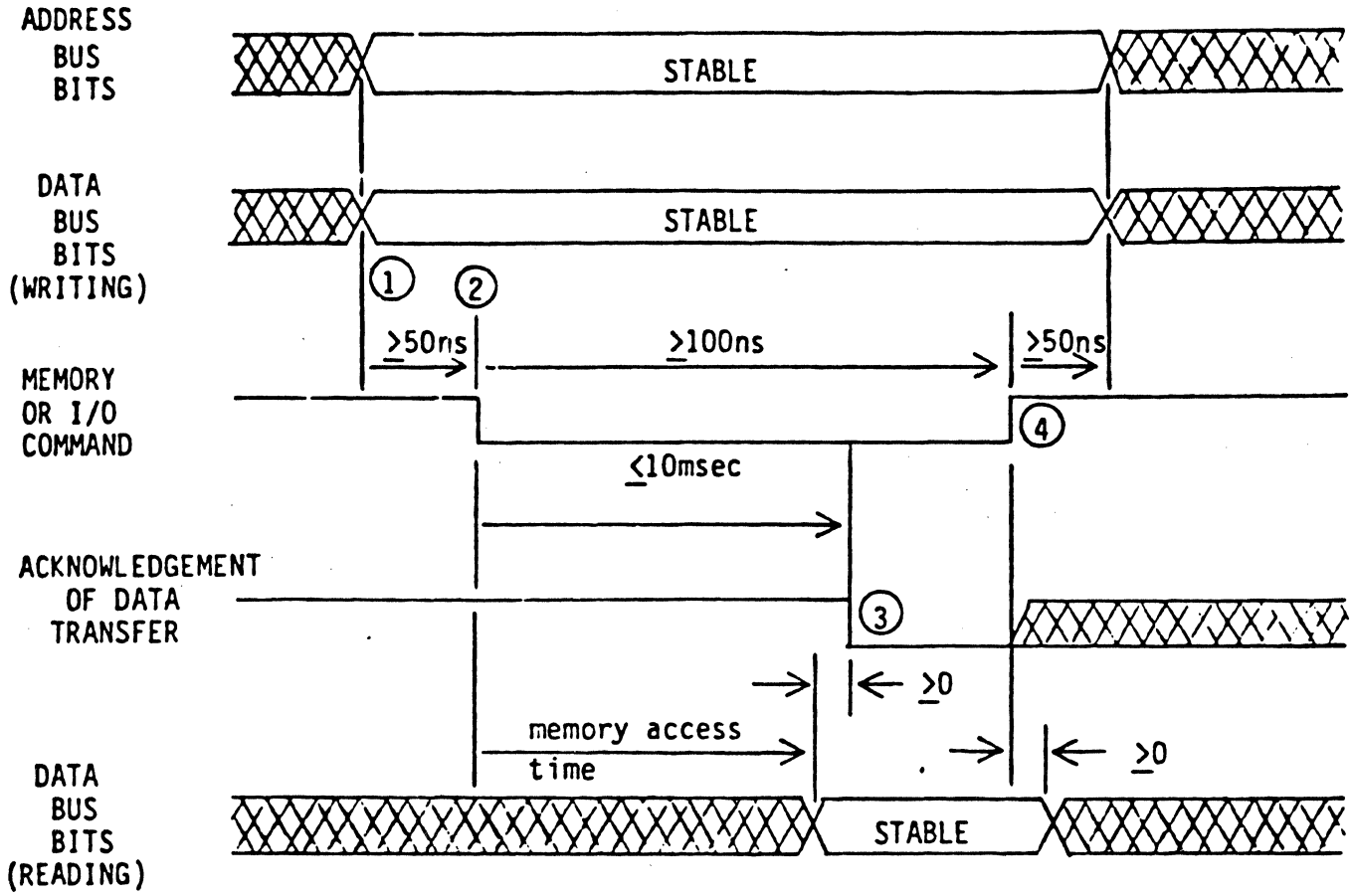
Refer to Table 2-2 for the AC requirements of the MULTIBUS.

2.3.2 Interface Specifications

The following specifications are for the bus standard. The MSC 8204 meets or exceeds these requirements.

Input Voltage: High 2.0V to 5.0V
Low 0.0V to 0.8V

Output Voltage: High 2.4V to 5.25V
Low 0.0V to .45V



Circled numbers correspond to sequence steps outlined in paragraph 2.3.1.

Figure 2-1
MULTIBUS DATA TRANSFER TIMING

Leakage Current of an Input 0.04 mA.

Leakage Current of an Output 0.1 mA.

Maximum Bus Capacitnace: 300 pF on any one line.

National DS 8833 and 8835 Quad Bi-directional transceivers fully comply with these specifications.

SIGNAL	DESCRIPTION	MIN.	MAX	REMARKS
BLCK/	Bus Clock	100 ns	DC	35 to 65% duty cycle
MRDC/	Pulse Width	100 ns	-	-
MWTC/	Pulse Width	100 ns	-	-
IORC/	Pulse Width	100 ns	-	-
IOWC/	Pulse Width	100 ns	-	-
XACK/	Acknowledge Hold	-	100 ns	Relative to command removal
INH1/	Inhibit Delay	100 ns	-	Relative to address assertion
AACK/	Acknowledge Hold	-	100 ns	Relative to command removal
INH2/	Inhibit Delay	100 ns	-	Relative to address assertion
ADR0/-ADR7/	Address Line Set Up	50 ns	-	Relative to command assertion
ADR0/-ADR7/	Address Line Hold	50 ns	-	Relative to command removal
DAT0/-DAT7/	Write Data Set Up	50 ns	-	Relative to command assertion
DAT0/-DAT7/	Write Data Hold	50 ns	-	Relative to command removal
DAT0/-DAT7/	Read Data Set Up	0 ns	-	Relative to XACK/.
DAT0/-DAT7/	Read Data Hold	0 ns	-	Relative to command removal
DAT0/-DAT7/	Read Data Access	0 ns	-	Maximum is DC

Table 2-2
MULTIBUS AC REQUIREMENTS

SECTION 3
PROGRAMMING

3.1 SCOPE

This section gives some examples such as a Slave I/O Interface and Bus Master using the MSC 8204.

3.2 SLAVE CONFIGURATION

The MSC 8204 has all bus-interface logic that is needed to make up a Slave I/O Interface. One approach is outlined in the following paragraphs and Table 3-1.

3.2.1 Address Bus

For memory-mapped I/O only, use chip U6, which is programmed to select the proper page. Pins E51 thru 58 provide a means to select groups of 32 addresses (Hex 20). If one of these pins is connected to E50, groups of four addresses are selected by E67 thru 74. These addressing output pins can be used to generate board select (E13) or the user can supply additional logic to fabricate this.

3.2.2 Data Bus

The data bus is divided into two sections to provide independent output terminals (DO0 thru DO7) and input terminals (DI0 thru DI7). If a bi-directional bus is required, these buses may be tied together.

E PIN	MNEMONIC	SLAVE I/O (Example 2-1)	BUS MASTER (Example 2-2)
1	MRQ/	NA	X
2	IORQ/	NA	X
3	BAACK/	NC	X
4	BXACK/	NC	X
5	BLCK	X	X
6	RD/	NA	NA
7	-	NA	NA
8	WT/	NA	X
9	BMWTC/	X	NC
10	BIOWC/	X	NC
11	BMRDC/	X	NC
12	BIORC/	X	NC
13	BRDSEL/	X	NA
14	CMND/	X	NC
15	INH1/	NC	NC
16	INH2/	NC	NC
17	WRITE/	X	NA
18	READ/	X	NA
19	T1	X	NC
20	T2	X	NC
21	T3	X	NC
22	T4	X	NC
23	UAACK	X	NC
24	MADRE	NA	X
25	ADRE	X	NC
26	UXACK	X	NA
27	MADRF	NA	X
28	ADRF	X	NC
29	GRANT/	NC	X
30	T5	X	NC
31	T6	X	NC
32	T7	X	NC

X - Use For This Application
NA - Input Not Used For This Application. Tie To Pullup If No Other Connection
NC - Output Not Used For This Application

Table 3-1
E-TERMINAL INTERCONNECTIONS

E PIN	MNEMONIC	SLAVE I/O (Example 2-1)	Bus MASTER (Example 2-2)
33	T8	X	NC
34	MADRA	NA	X
35	ADRA	X	NC
36	MADRC	NA	X
37	ADRC	X	NC
38	MADRB	NA	X
39	ADRB	X	NC
40	MADRD	NA	X
41	ADRD	X	NC
42	MADR6	NA	X
43	ADR6	X	NC
44	MADR8	NA	X
45	ADR8	X	NC
46	MADR7	NA	X
47	ADR7	X	NC
48	MADR9	NA	X
49	ADR9	X	NC
50	DAXEN/	X	NA
51	DAOX/	X	NC
52	DA2X/	X	NC
53	DA4X/	X	NC
54	DA6X/	X	NC
55	DA8X/	X	NC
56	DAAX/	X	NC
57	DAEX/	X	NC
58	DACX/	X	NC
59	MADR2	NA	X
60	ADR2	X	NC
61	MADR4	NA	X
62	ADR4	X	NC
63	MADR3	NA	X
64	ADR3	X	NC

X - Use For This Application
NA - Input Not Used For This Application. Tie To Pullup If no Other Connection
NC - Output Not Used For This Application.

Table 3-1 (cont)
E-TERMINAL INTERCONNECTIONS

E PIN	MENMONIC	SLAVE I/O (Example 2-1)	BUS MASTER (Example 2-2)
65	MADR5	NA	X
66	ADR5	X	NC
67	DAX00/	X	NC
68	DAX04/	X	NC
69	DAX08/	X	NC
70	DAX0C/	X	NC
71	DAX10/	X	NC
72	DAX14/	X	NC
73	DAX1C/	X	NC
74	DAX18/	X	NC
75	DO6	X	X
76	DI6	X	X
77	MADR0	NA	X
78	ADR0	X	NC
79	DO7	X	X
80	DI7	X	X
81	MADR1	NA	X
82	ADR1	X	NC
83	DO4	X	X
84	DI4	X	X
85	DO5	X	X
86	DI5	X	X
87	RDEN/	X	X
88	WTEN/	X	X
89	DO2	X	X
90	DI2	X	X
91	DO0	X	X
92	DI0	X	X
93	DO3	X	X
94	DI3	X	X
95	DO1	X	X
96	DI1	X	X

X - Use For This Application
NA - Input Not Used For This Application. Tie To Pullup If No Other Connection.
NC - Output Not Used For This Application.

Table 3-1 (cont)
E-TERMINAL INTERCONNECTIONS

Then signals RDEN (E87) and WTEN (E88) provide directional control of data flow to and from the MULTIBUS. However, these signals require an external source that is appropriate for the specific application. One simple approach that allows a bi-direction data bus is shown in Figure 3-1, using two sections of a 74LS32. However, more intricate the application, the more complex the circuit.

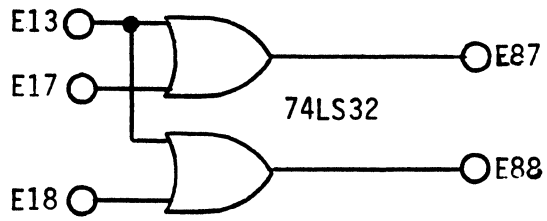


Figure 3-1
RDEB/ AND WREN/ CONTROL

3.2.3 Command

Board selection requires a "low" on BRDSEL/ (E13). In turn, CMND/ (E14) indicates that a command is in progress. To control a read or write operation using MULTIBUS commands, tie READ/ (E18) and WRITE/ (E17) to either BMRDC/ (E11) or BIORC/ (E12) and BMWTC/ (E9) or BIORC/ (E12) respectively.

Based on the frequency of the bus clock, outputs E19 thru 22 and E30 thru 33 provide the timing for MULTIBUS acknowledge signals AACK/ and XACK/. Pin E19 yields the minimum delay and E10 provides an 800- to 1000-nanosecond delay. Tying two of these outputs to E23 and 26 generate UAACK and UXACK -- signals for AACK/ and XACK/ respectively.

3.3 BUS MASTER CONFIGURATION

The MSC 8204 contains the logic circuits required to handle the bus-arbitration algorithm defined for the MULTIBUS. The following paragraphs discuss one procedure for configuring the MSC 8204 as a Bus Master (Refer to Table 3-1).

3.3.1 Address Bus

The address to which the DMA should take place is connected to inputs MADRO (E77) thru MADRF (E27). These inputs must be stable before the desired operation can proceed.

3.3.2 Sequence of Operation

After the address has stabilized, a "low" may be asserted onto MRO/ (E1) and either RD/ (E6) or WT/ (E8), depending whether the operation is to be a read or write. A transaction takes place until BAACK/ (E3) or BXACK/ (E4) occurs. At that time, the command should be removed after an appropriate delay. If there is no memory, an acknowledgement will not be generated. This must be detected and the command aborted.

When a "low" is asserted on GRANT/ (E29), RDEN/ (E87) or WTEN/ (E88) can be enabled as required. They will remain enabled until either GRANT/ is unasserted or at least 50 nanoseconds after the command has terminated. Figure 3-2 provides this required function, but has no provision for slave operation. The actual ciruit is more complex.

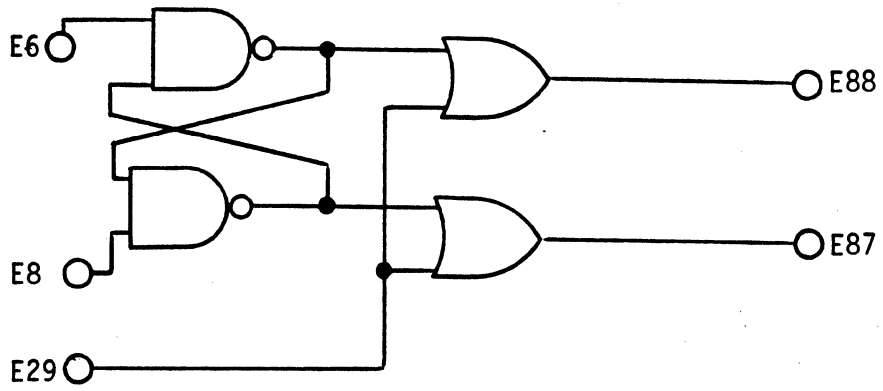


Figure 3-2
READ/WRITE CONTROL

It is also possible to communicate with I/O devices in a bus-master mode. In performing this, the high and low bytes of the address must be the same.

3.3.3 Special Considerations

If there's a special requirement to retain control of the bus between transactions, leave MRQ/ asserted and only release either RD/ or WT/. This is useful for high-speed DMA transfer rates since there is no bus-arbitration delay. In fact, the realizable bus transfer rate is easily doubled at the expense of inhibiting further executions of other processes.

SECTION 4
THEORY OF OPERATION

4.1 SCOPE

This section details the interface buffers and control-logic circuits that are contained on the Universal Card.

4.2 INTERFACE

All address and data buffers are bi-directional and MULTIBUS compatible. Table 2-1 identifies the MULTIBUS signals with pin numbers. For internal-signal identification, refer to Table 3-1.

4.3 SYSTEM DESCRIPTION

The MSC 8204 has its own programmable, bus-master control system. The address decoding permits the use of either memory-mapped I/O addressing or regular, isolated I/O addressing. Also, the card contains transfer-acknowledge circuits in addition to inhibit options. Easy-to-use, wirewrap terminals (E-terminals) make these signals available to speed prototyping of MULTIBUS compatible systems.

4.3.1 Address Bus

Line drivers and receivers U13 to 16 either accept or transmit the address bits ADR0 thru ADRF. Signals MADR0 thru MADRF are connected to a set of E-terminals (wirewrap) and asserted onto the MULTIBUS via the line drivers of U13 to 16.

In turn, the line receivers of U13 to 16 accept the MULTIBUS address signals and either make them available on the E-terminals for prototyping applications or apply them to address-decoding circuits U6 to 8. Chip U6 is programmed to select the proper page for memory-mapped I/O only. The other decoders (U7 and 8) provide outputs on the E-terminals for isolated I/O addressing (Refer to paragraph 3.2.1).

4.3.2 Data Bus

Circuits U17 and 18 are the interface buffers needed for the bi-directional data lines DAT0 thru DAT7. The basic configuration provides independent output and input terminals. For bi-directional requirements, these terminals can be tied together with terminals E87 and E88 available for directional control of the data flow.

4.3.3 Control Signals

Line driver and receiver U11 accepts the read/write commands used during either a memory or I/O operation. This line buffer conveys the read/write control signals to and from the MULTIBUS.

Circuits U1 and 9 make up an internal, bus-master control that is under direction of various MULTIBUS commands. Acknowledgement signals such as AACK and XACK are required for either a read or write operation and generated through the logic gates of U10 and 12. A set of eight, timing outputs are available on terminals E19 to E22 and E30 to E33 for MULTIBUS acknowledgement timing. An eight-bit, shift register (U5) provides these levels using the bus clock BLCK as the basic timing element.

SECTION 5
WARRANTY

5.1 SCOPE

Monolithic Systems Corporation (MSC) warrants for a period of one (1) year from the date of shipment that each item of equipment (except those materials supplied by Buyer) shall be free from defects in material and workmanship under normal use and service. Any equipment which is not as warranted may be returned to MSC at MSC's risk and expense for repair or replacement.

This warranty shall immediately terminate if the equipment is subjected to misuse, neglect, accident, damage in transit, transported in other than MSC authorized containers, or is altered, repaired or overhauled by any person other than MSC.

The foregoing warranty is in lieu of all other warranties, promises affirmations or representations, whatsover, express or implied, including, but not limited to, any implied warranty of merchantability or implied warranty of fitness of equipment for a particular purpose, and of any other obligations on the part of the seller.

REVISIONS				
REV	ECO	DESCRIPTION	DATE	APP.
C	1281	ENGINEERING RELEASE	10-9-78	BwS

△2 U6 IS OPTIONAL, CUSTOMER REQUEST ONLY.

△1 CAPACITORS USED ONLY WHEN ADDITONAL VOLTAGES ARE NEEDED: (TO BE INSTALLED BY USER) C2/+12V, C3/-5V,C4/-10V,C5/-12V.

NOTES: Unless Otherwise Specified:

REV STATUS OF SHEETS																											
	REV																										
	SHEET																										
	REV	C	C	C																							
	SHEET	1	2	3																							

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE:

MATERIAL

		DATE
DRAWN	Ed Sexton	4/4/78
CHECKED	Dale C.	6/9/78
APPROVED	J. Schumacher	9 OCT 78
APPROVED		

MONOLITHIC SYSTEMS CORP.

ASSEMBLY, UNIVERSAL CARD

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0221-000

SCALE – REV C SHEET 1 of 3

MSF-1015 REV A

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
			001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
			1	304-0221-001	P.C. BOARD	REV. C		1
			1	210-0100-005	I.C. 74LS00	U4		2
			1	210-0103-005	I.C. 74LS04	U2		3
			1	210-0300-001	I.C. 7406	U12		4
			2	210-0804-005	I.C. 74LS32	U3,10		5
			2	210-0908-003	I.C. 74S138	U7,8		6
			1	210-0629-005	I.C. 74LS164	U5		7
			1	210-0634-005	I.C. 74LS175	U9		8
			1	323-0018-001	PROGRAMMED PROM	U1		9
			1	210-0409-001	I.C. 8833	U11		10
			6	210-0414-001	I.C. 8835	U13,14,15,16,17,18		11
								12
			A/R	———	CAPACITOR	C2-5 (1)		13
			2	201-0018-001	CAPACITOR, 6.8uf, 10V	C1,6		14
			9	701-0001-003	CAPACITOR, 0.1uf, 50V	C7-15		15
			5	214-0002-073	RES. 1K, 1/4W, 5%	R1-5		16
			97	208-0085-003	WIRE WRAP POSTS	E1-97		17
			6	208-0023-004	14 PIN HEADER	U2-5,10,12		18
			12	208-0023-001	16 PIN HEADER	U1,6-9,11,13-18		19
			2	208-0063-003	SET EJECTOR HANDLE & PIN			20
			REF	323-0019-xxx	PROGRAMMED PROM	U6 (2)		21
								22

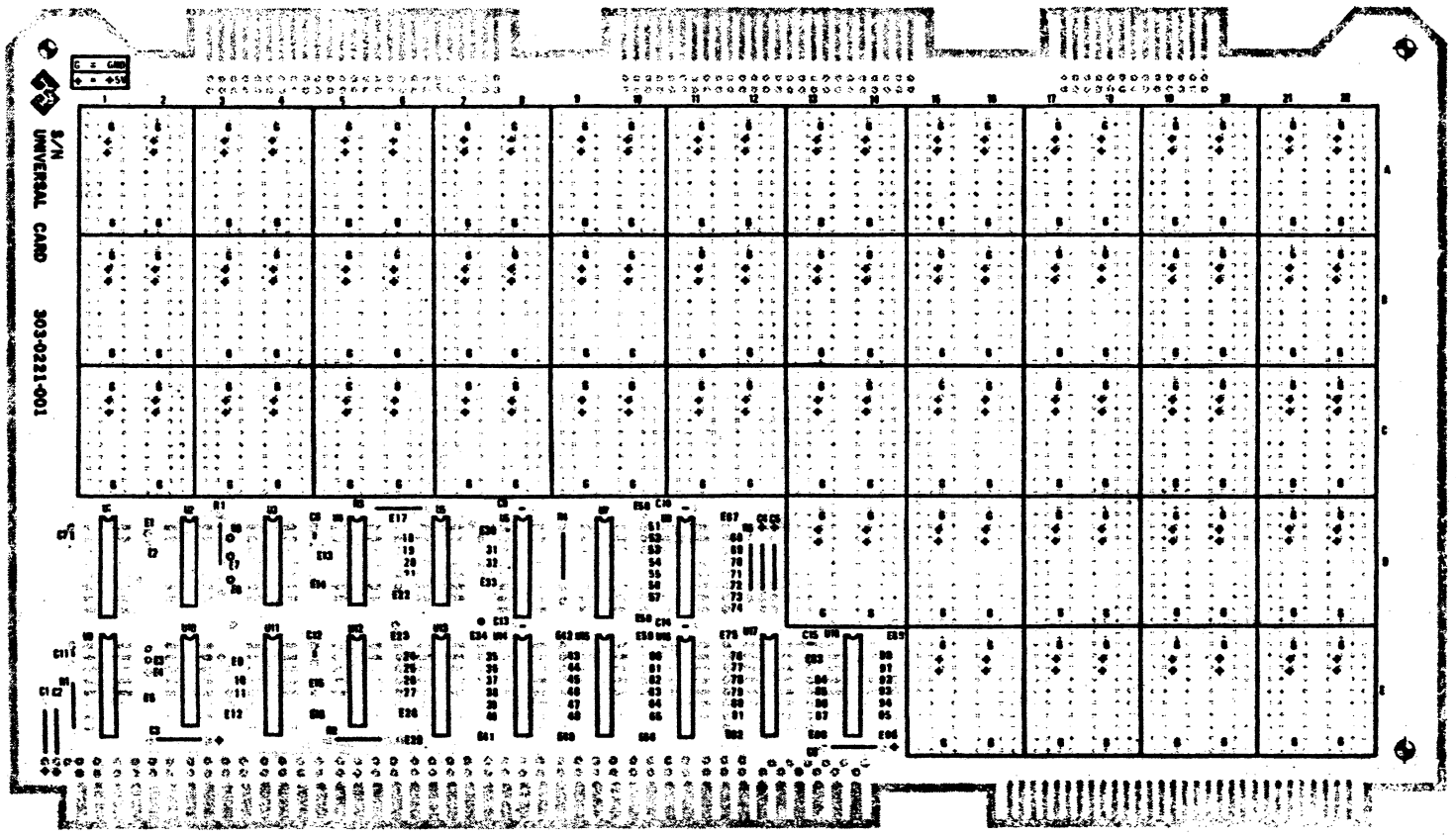
SIZE A

CODE IDENT NO 51513

DWG NO. 303-0221-000

REV C

SHEET 2 - 2



NOTE: COMPATIBLE WITH REV. C ARTWORK.

-001

MONOLITHIC SYSTEMS CORP.

SIZE	CODE IDENT NO.	DWG NO.	REV
B	51513	303-0221-000	C
SCALE 1-1		SHEET 3	

MSP - 1008A

INTEGRATED CIRCUIT DATA TABLE

DEVICE TYPE NO.	REFERENCE DESIGNATION	NOTE	POWER & GROUND GND	POWER & GROUND +5V	REMARKS/SPARES	LINE NO.
I.C. 74LS00	U4		7	14		1
I.C. 74LS04	U2		7	14		2
I.C. 7406	U12		7	14		3
I.C. 74LS32	U3,10		7	14		4
I.C. 74S138	U7,8		8	16		5
I.C. 74LS164	U5		7	14		6
I.C. 74LS175	U9		8	16		7
I.C. 74S287	U1,6		8	16	U6 IS OPTIONAL	8
I.C. 8833	U11		8	16		9
I.C. 8835	U13,14,15,16,17,18		8	16		10

REVISIONS				
ECO	LTR	DESCRIPTION	DATE	APPROVED
1281	C	ENGINEERING RELEASE	10-9-78	RWC

3. "E" INDICATES WIRE WRAP POST.

2. THE FOLLOWING CAPACITORS ARE USED ONLY WHEN ADDITIONAL VOLTAGES ARE USED:
C2/+12V; C3/-5V; C4/-10V; C5/-12V.

1. ALL RESISTANCE VALUES IN OHMS, 1/4W, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

U18	
R5	
E93	
C15	C2,3,4,5 (2)
LAST USED	NOT USED
REF DESIGNATIONS	

	C	C	C																REV
	1	2	3																SHEET

MONOLITHIC SYSTEMS CORP.

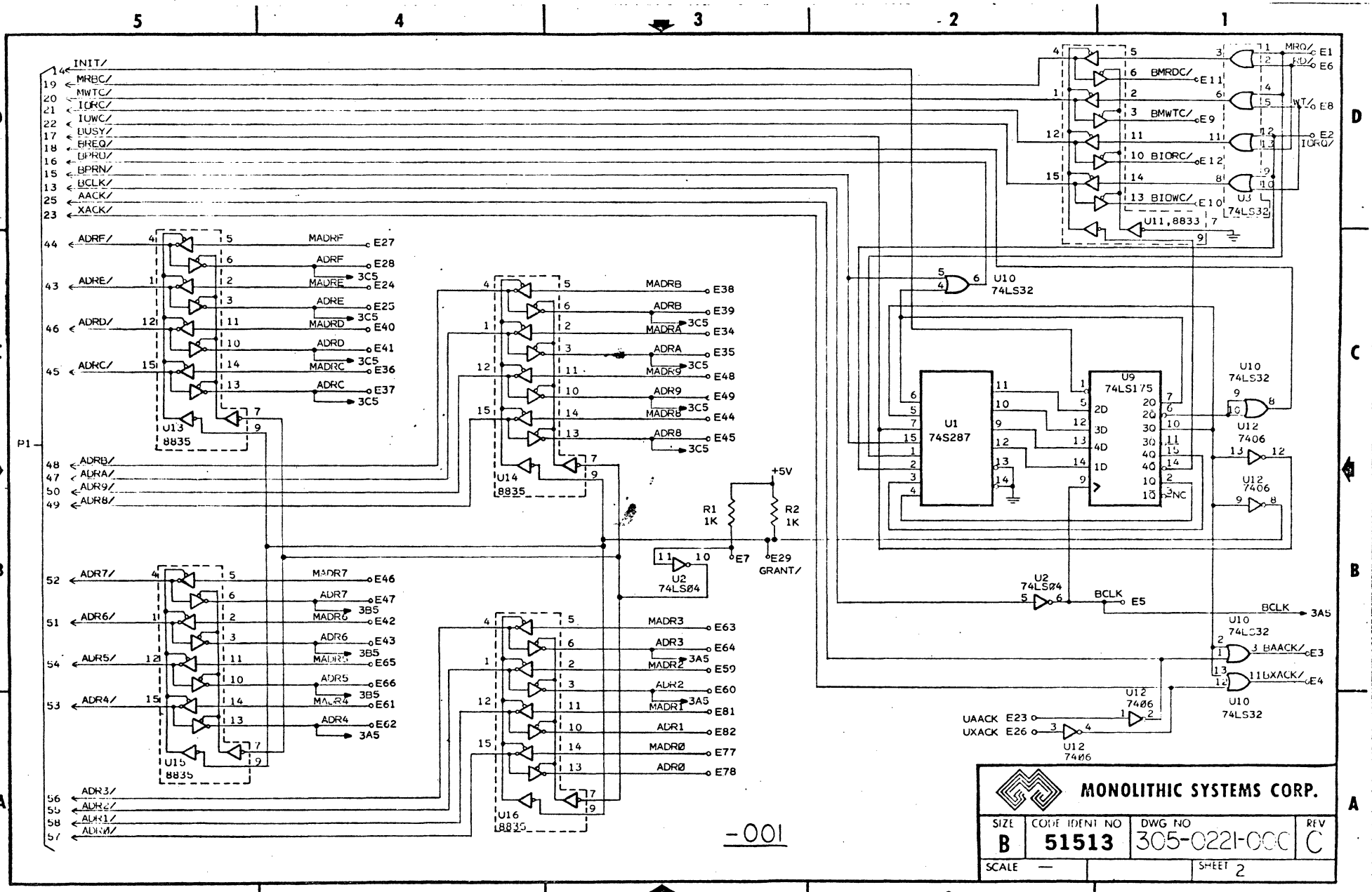
SCHEMATIC DIAGRAM, UNIVERSAL CARD

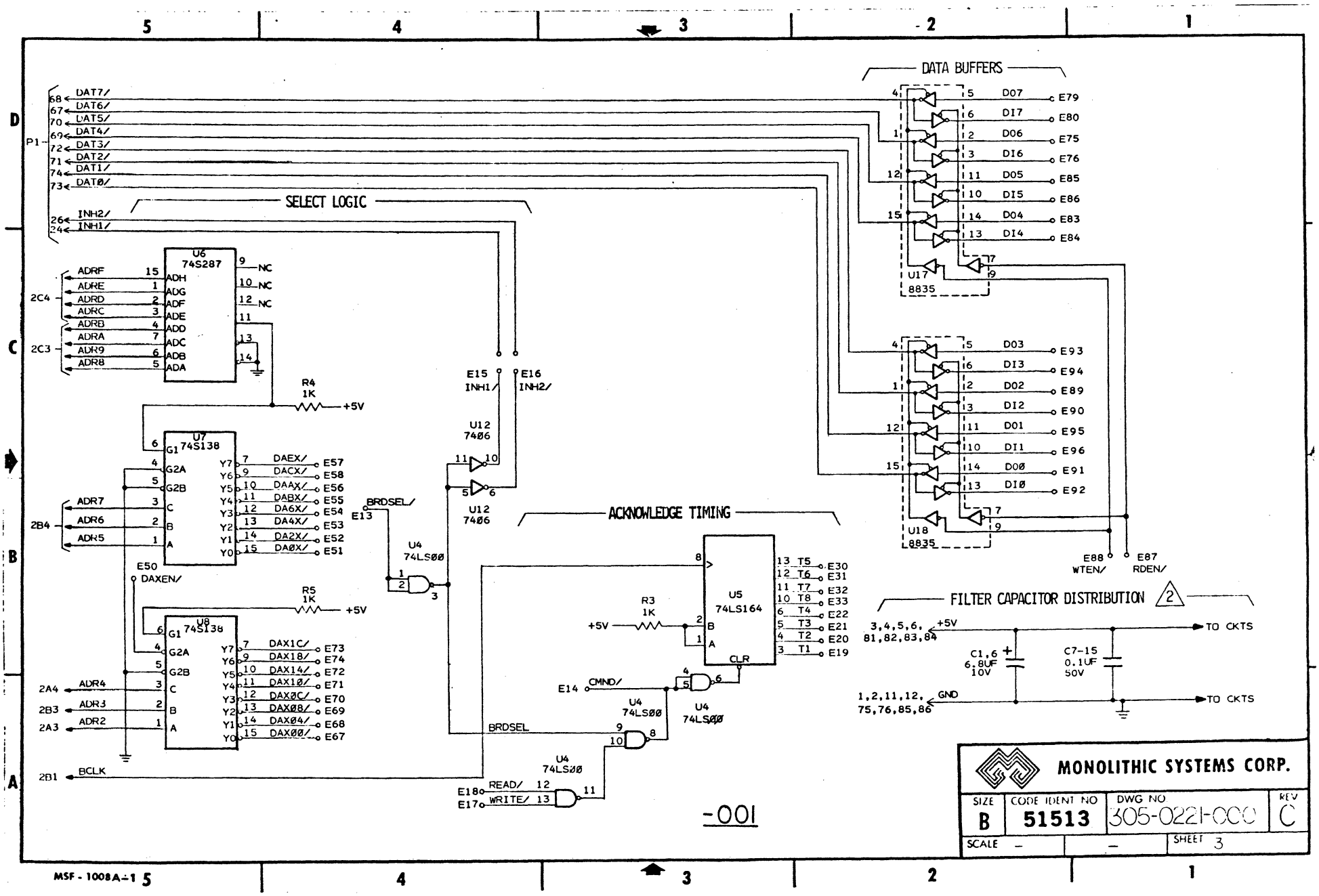
	DATE
DRAWN	G. Spence 4-4-78
CHECKED	Dale E 10/9/78
APPROVED	
APPROVED	

SIZE	CODE IDENT NO.	DWG NO.	REV
B	51513	305-0221-000	C

SCALE NONE SHEET 1 of 3

MSF - 1008


INIT/
MRBC/
MWTC/
IORC/
IOWC/
BUSY/
BREQ/
BPRO/
BPRN/
BCLK/
AACK/
XACK/
ADRF/
ADRE/
ADRD/
ADRC/
ADRB/
ADRA/
ADR9/
ADR8/
ADR7/
ADR6/
ADR5/
ADR4/
ADR3/
ADR2/
ADR1/
ADR0/
P1
U13 8835
U14 8835
U15 8835
U16 8835
MADRF E27
ADRF E28
MADRE E24
ADRE E25
MADRD E40
ADRD E41
MADRC E36
ADRC E37
MADRB E38
ADRB E39
MADRA E34
ADRA E35
MADR9 E48
ADR9 E49
MADR8 E44
ADR8 E45
MADR7 E46
ADR7 E47
MADR6 E42
ADR6 E43
MADR5 E65
ADR5 E66
MADR4 E61
ADR4 E62
MADR3 E63
ADR3 E64
MADR2 E59
ADR2 E60
MADR1 E81
ADR1 E82
MADR0 E77
ADR0 E78
3C5
3B5
3A5
+5V
R1 1K
R2 1K
E7
E29
GRANT/
U2 74LS04
U1 74S287
U9 74LS175
U10 74LS32
U11,8833
U3 74LS32
BMRDC/ E11
BMWTC/ E9
BIORC/ E12
BIOWC/ E10
MRQ/ E1
RD/ E6
WT/ E8
IORQ/ E2
U12 7406
BCLK E5
BCLK 3A5
BAACK/ E3
BXACK/ E4
UAACK E23
UXACK E26
NC
-001
MONOLITHIC SYSTEMS CORP.
SIZE B
CODE IDENT NO 51513
DWG NO 305-0221-000
REV C
SCALE —
SHEET 2
MSF - 1008A-1


DATA BUFFERS
SELECT LOGIC
ACKNOWLEDGE TIMING
FILTER CAPACITOR DISTRIBUTION
DAT7/
DAT6/
DAT5/
DAT4/
DAT3/
DAT2/
DAT1/
DAT0/
INH2/
INH1/
U6 74S287
U7 74S138
U8 74S138
U5 74LS164
U4 74LS00
U12 7406
U17 8835
U18 8835
R4 1K
R5 1K
R3 1K
+5V
E15 INH1/
E16 INH2/
BRDSEL/
DAXEN/
BCLK
CMND/
READ/
WRITE/
WTEN/
RDEN/
GND
TO CKTS
C1,6 6.8UF 10V
C7-15 0.1UF 50V
MONOLITHIC SYSTEMS CORP.
SIZE B
CODE IDENT NO 51513
DWG NO 305-0221-000
REV C
SCALE –
SHEET 3
-001
MSF-1008A-1