MSC 8901

MEMORY MANAGER

USER'S MANUAL

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7-8-82

MSC 8901

TABLE OF CONTENTS

SECTION 1
INTRODUCTION

SECTION 2
INSTALLATION

SECTION 3
OPERATION

SECTION 4
WARRANTY

FIGURES

TABLES

SECTION 1

INTRODUCTION

1.1 DESCRIPTION

The MSC 8901 Memory Manager is a Multibus*-compatible board which can control from one to eight microprocessors. Each processor can address up to one megabyte of memory.

The MSC 8901 Memory Manager is designed for use in a system containing a combination of processor boards and additional memory boards, such as MSC's 8000 series microprocessors and 4000 series memory expansion boards.

The MSC 8901 Memory Manager has three major functional areas:

Real-Time Clock
Memory Extender/Page Mapper
Parallel Bus Master Arbitrator

When combined, these three areas make this unit a powerful addition to any Multibus computer system.

1.1.1 Real Time Clock

The MSC 8901 provides a continuously running, battery-backed time-of-day clock, which is useful for dating files and which can also be used as an "alarm clock" to generate interrupts. This clock provides counters for thousandths, hundredths, tenths of seconds and seconds; minutes, hours, days, weeks and months. It can generate real-time interrupts as often as every millisecond, or at any specific time up to once per month.

1.1.2 Memory Extender/Page Mapper

The board provides a Memory Extender/Page Mapper. The processor can page between various memory boards by writing data into the page register in the Memory Extender/Page Mapper.

*Multibus is a registered trademark of Intel Corporation.

1.1.3 Parallel Bus Master Arbitrator

The MSC 8901's Parallel Bus Master Arbitrator can control systems which contain from four to eight potential bus masters. Display LEDs mounted on the 8901 indicate which board is currently selected as bus master.

1.2 SPECIFICATIONS

General

Bus:	Multibus, 16, 20, 24 address bits Signals TTL Compatible
Power Supply Required:	+5V only 1.4A typical

Operating Environment

Temperature:	0° - 65°C
Humidity:	0% - 95% without condensation

Physical Dimensions

Length:	12"
Width:	6.75"
Depth:	0.5"

SECTION 2

INSTALLATION

2.1 GENERAL

To properly install the MSC 8901 Memory Manager, the 8901 and other system boards must be assigned to specific slots in the backplane, the Multibus chassis must be wired to establish the priority of the boards, and several jumpers must be installed on the 8901 board corresponding to the capabilities of the system processors.

2.2 BACKPLANE SLOTS

In order to use the MSC 8901's Memory Mapper, both the MSC 8901 and the processor board (or boards) must be assigned specific slots on the Multibus backplane. Once these slots are assigned, the boards assigned to them must remain in these slots as long as the MSC 8901 is in use.

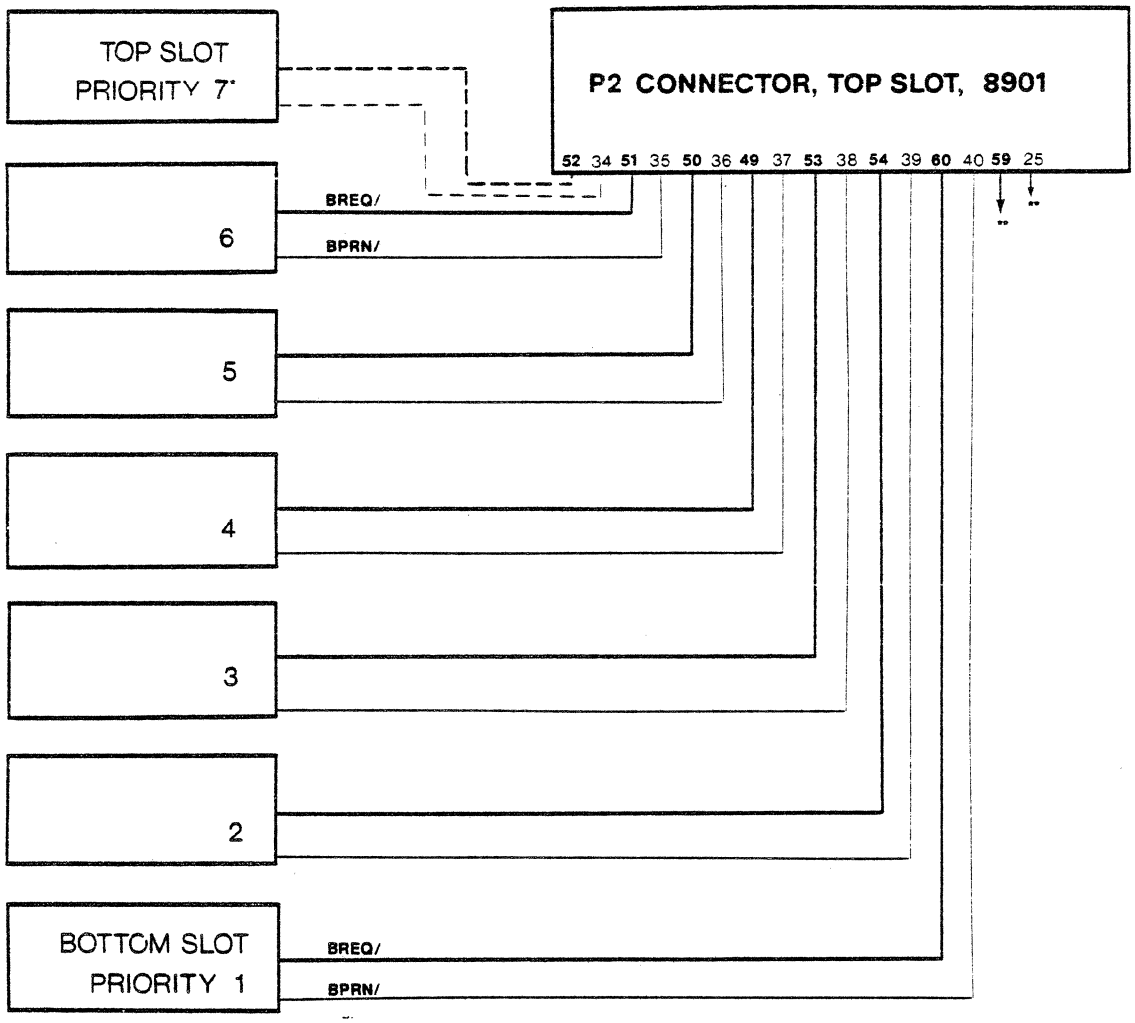
If the system to which the MSC 8901 is added contains more than one processor board, then the boards must be assigned slots depending upon their individual priorities for use on the bus.

Normally, the MSC 8901 is assigned the highest priority slot on the backplane. This will make wiring of the backplane, as described below, much more straightforward.

2.3 WIRING THE BACKPLANE

The backplane that the MSC 8901 board will be mounted in must have a card-edge connector for the auxiliary P2 connector on the board. Wires must be installed from this connector to the Bus Request (BREQ/) and Bus Priority In (BPRN/) pins of each processor's slot in the backplane. The actual wiring of the backplane will determine the priority of each card slot.

Figure 1 indicates the proper method of wiring the backplane to implement parallel priority resolution.



These connections may be implemented by installing jumbers 1-2 and 3-4 at location E10.
**Since there are only seven (7) slots in an MSC Multibus backplane, these lines are not used unless an expansion chassis is used, in which case these lines run to that chassis. These are priority 0 lines.

Figure 1 Wiring for Parallel Priority Resolution

Multibus boards that are capable of being bus masters are normally equipped with circuitry for serial bus priority resolution. The MSC 8901 Memory Manager requires that this serial priority scheme not be used, so that the board can determine which bus master is actually in control of the bus. For this purpose, a parallel priority arbitrator has been included in the MSC 8901.

The serial priority scheme can be disabled in one of several ways:

1. If the processor card has a jumper for Bus Priority Out (BPRO), this jumper can be removed.

2. On the newer revisions of the MSC Multibus backplane, there are several jumpers which must be removed.

3. On most other types of backplanes, the run between BPRO/ of each of the processor boards and BPRN/ of the next lower processor boards may be cut. (Alternately, the run to BPRO/ on the processor may be cut.

2.4 JUMPERS AND JUMPER CONNECTION

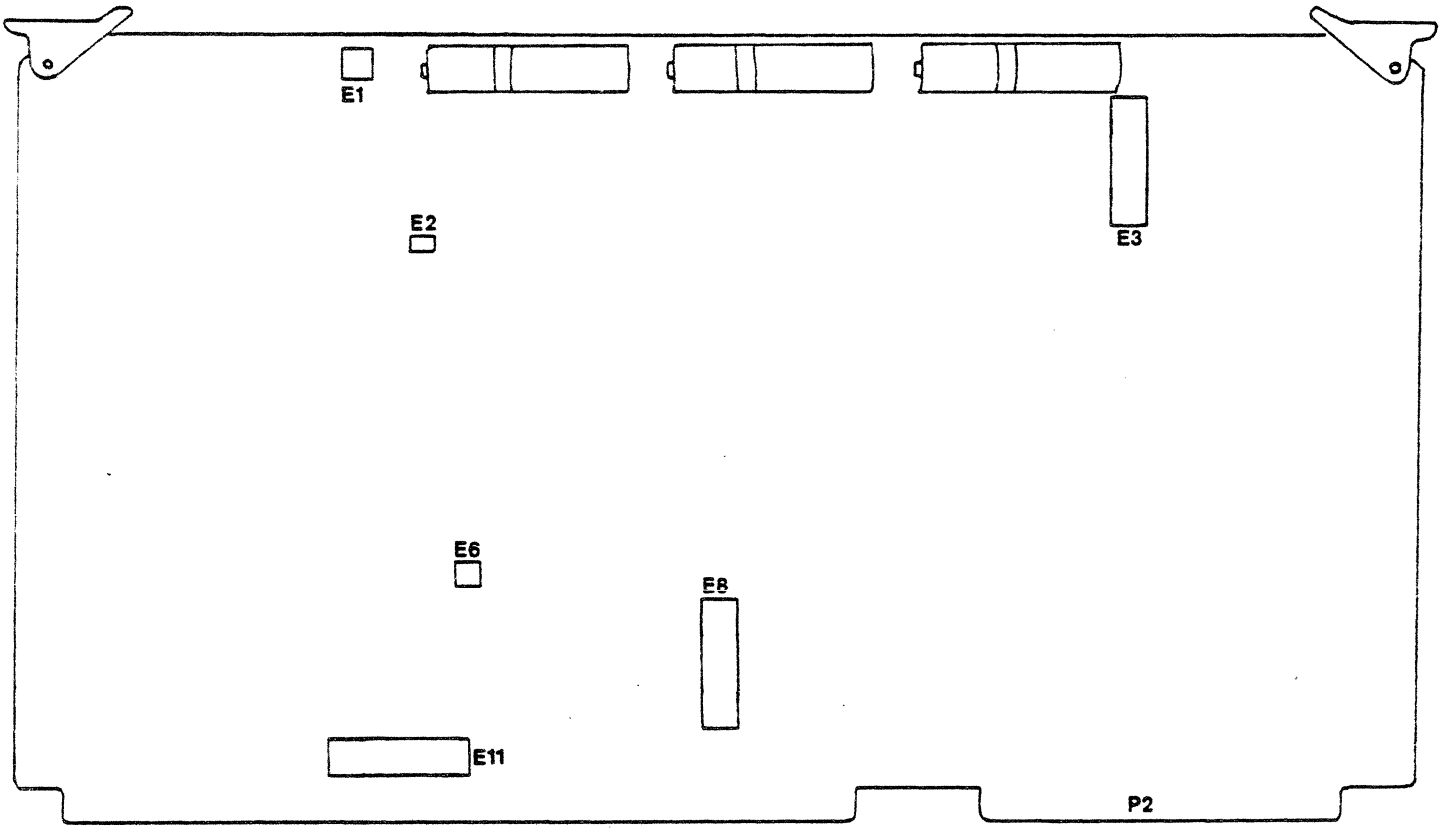


Figure 2 Locations of Jumpers on the MSC 8901

2.4.1 Address Line Control

Once the backplane has been wired to accommodate the processors, the MSC 8901 must be informed how many address bits each processor will generate. This is accomplished through a series of jumpers at location E3 (See Figure 2).

The pins at that location are configured in eight rows of three pins each. The eight rows correspond to the eight priority levels (0-7) that the MSC 8901 will recognize for bus master arbitration. Table 1 shows how jumpers should be installed, depending on what size data address (16, 20, or 24 bits) each processor will generate.

Priority of Board	16 Bit	20 Bit	24 Bit
Highest Priority 7 (Normally 8901 Board)	23-24	22-23	*
6	20-21	19-20	No Jumper Installed if Master Will Generate 24 Address Bits.
5	17-18	16-17	
4	14-15	13-14	
3	11-12	10-11	
2	8- 9	7- 8	
1	5- 6	4- 5	
Lowest Priority 0	2- 3	1- 2	

* 8901 Generates 24 Bits of Address.

Table 1 Jumpers for Address Size of Each Bus Master

The MSC 8901 generates 8 address bits for assertion on the Multibus. As supplied, the MSC 8901 asserts data from the appropriate mapper RAM location onto address lines AD10 to AD13 when a 16-bit bus master is controlling the bus and address lines AD14 to AD17 are asserted at logic 0.

When a bus master capable of generating 20-bit addresses controls the bus, the MSC 8901 asserts data from the appropriate mapper RAM location onto address lines AD14 to AD17, and does not assert address lines AD10 to AD13. In the case of a bus master that will generate 24 bits of address, the MSC 8901 will not assert any address lines.

If all 24 address lines need to be controlled by a master which generates only 16 bits of address, an additional four-bit mapper RAM IC can be installed in the socket at location U10 on the MSC 8901 board. The IC is a 29705 16x4 Dual Port RAM (MSC part number 210-1035-001). When this IC is installed, and a bus master which generates 16 bits of address is using the bus, the MSC 8901 will assert eight bits of address on address lines AD10 to AD17, from the appropriate location in the mapper RAM.

2.4.2 Clock Starting Address

Before the MSC 8901 can be inserted into an existing system, jumpers must be installed on-board to insure that the I/O locations used by the clock will not conflict with those already reserved by system software. The board is provided with jumpers and hardware in sufficient quantity to make this possible.

The area on the board which contains the addressing pins is labeled E8 (See Figure 2). When holding the board so that the batteries are on the top, E8 is found in the very center of the bottom row of ICs. Take careful note of the way in which these jumpers are numbered, because not every one is so labeled.

When the board arrives, the jumpers will be positioned so that the starting I/O address for the clock is 40H. This starting address is compatible with most software: if it is inconvenient for some reason, it may be changed so that the addressing for the clock alternatively begins at 0H, 20H, 60H, 80H, A0H, C0H, or E0H.

Table 2 shows which pins must be connected in order to achieve a given starting address.

E8 Jumper Pins	Clock Starting Address
1 - 2	0H
5 - 4	20H
7 - 8	40H
10 - 11	60H
13 - 14	80H
16 - 17	A0H
19 - 20	C0H
23 - 22	E0H

Table 2 Setting Clock Starting Address

2.4.3 Clock Interrupts

The clock can generate an interrupt on one of eight Multibus lines (INT0-INT7). The desired line is selected by connecting jumpers at location E12 as shown in Table 3.

Multibus Interrupt Line	E12 Jumper Pins
INT0	20 - 21
INT1	23 - 24
INT2	14 - 15
INT3	17 - 18
INT4	8 - 9
INT5	11 - 12
INT6	2 - 3
INT7	5 - 6

Table 3 Multibus Line Selection for Clock Interrupts

2.4.4 Battery Connection

Three rechargeable nickel-cadmium batteries are located on the top of the board; however, when the board arrives from the factory, they will not as yet be supplying power to the clock.

Connecting and disconnecting the batteries is accomplished by connecting or disconnecting, respectively, the jumper pins at location E1. When the board is held so that the batteries are at the top, location E1 is immediately to the left of the line of batteries.

The board is now ready to be installed in the Multibus. When the clock alone is going to be tested or used, the MSC 8901 can be installed in any unoccupied slot. At any other time, specific slots in the Multibus must be used as described previously.

The batteries are automatically recharged when power is applied to the MSC 8901 board. The clock will run on battery power for at least 1000 hours (approximately 40 days) without needing to be recharged.

2.4.5 Option for 16-Bit I/O Addresses

If the system to which the MSC 8901 is being added has a processor that generates 16-bit addresses for I/O devices, an option decoder may be installed in location U51. This decoder is a 74LS682 8-bit comparator (MSC part #210-0823-005). Jumpers at location E7 must be reconnected to match the 16-bit I/O address required (See Table 4) and the jumper installed at location E6 must then be removed.

Address Bit	E7 Jumper
Add 8	1 - 2
9	3 - 4
A	5 - 6
B	7 - 8
C	15 - 16
D	13 - 14
E	11 - 12
F	9 - 10

For a true compare with address bit low, remove jumper. (L.C. to locate the 8901 in I/O page 00, remove all E7 jumpers. To locate the 8901 in I/O page 2/H install jumpers E7 1-2 and 13-14.

Table 4 Jumpers for 16-Bit I/O Address Option

SECTION 3

OPERATION

3.1 THE REAL TIME CLOCK

The clock used by the MSC 8901 is a National MM58167 Real Time Clock, a CMOS circuit that is microprocessor compatible. This section describes how the clock is set, read and configured to provide easy and effecient use.

3.1.1 Setting the Clock

Time on this clock is set by writing data into several counters within the clock itself. There are also RAM locations into which any data may be written.

The easiest method of setting the time is to start at the highest counter (months, in this case), and set for progressively smaller periods of time. It is a good idea to set the minutes counter to `minutes desired +1`; in this way, when the `go` command is given, the clock can then start counting from an exact time.

Table 5 shows the I/O addresses to which data must be written in order to set the clock. A machine language program, or a program written in a high-level language (such as a BASIC with IN and OUT commands) can be employed to this end. Keep in mind that address values must be added to the base value, that is, the value at which the starting address pins were jumpered, as shown in Table 2.

Starting I/O Address Plus	Counter Set:
00H	Ten-thousandths seconds
01H	Hundredths, 10ths seconds
02H	Seconds
03H	Minutes
04H	Hours
05H	Day of Week
06H	Day of Month
07H	Month
15H	"GO" command

Table 5 I/O Addresses for Setting Time-of-Day Clock

All of the data to be written to these counters is in the form of two BCD digits. Thus, October is written in as 10H, not as 10 decimal or as 0AH. Similarly the 22nd day of a month is written as 22H, not as 22 decimal or as 16H.

Table 6 shows the BCD data to be entered for each of the counters in order to set them to a particular time and date.

Counter	BCD Data
Ten-thousandths of seconds	Set initially to 0
Hundredths & 10ths	Set initially to 0
Seconds	Set initially to 0
Minutes	1H-60H BCD (AH, BH, etc. skipped) Set to Minutes +1 and give "GO" command on exact time
Hours	24 hour clock 10 AM = 10H, (not AH) 10 PM = 22H
Day of Week	Sunday = 1H Saturday = 7H
Month	January = 1H October = 10H (not AH)
"GO" command	Any data will reset clock to start at an exact minute.

Table 6 BCD Data for Setting Counters

3.1.2 The GO Command

A write of data to clock address base + 15H will reset the milliseconds, hundredths, tenths, units and tens of seconds counters. This is called the "GO" command, and although its implementation is not necessary to set the clock, it provides a convenient method of starting the clock at an exact minute.

Data on the data bus is ignored during this write. If the seconds counter is greater than 40 when the GO command is issued, the minutes counter will increment; otherwise, the minutes counter is uneffected.

3.1.3 Alarm Clock Functions

Fifty-six bits of RAM contained in the clock are used as comparator registers for the alarm clock operation.

Data stored here is compared with data contained in the time counters. By writing data to the interrupt control register, an interrupt can be generated at a specific time. The format of the Real Time Counter is shown in Table 7.

Counter Addressed	Base Address +	Units D0	D1	D2	D3	Max BCD Code	Tens D4	D5	D6	D7	Max BCD Code	RAM Addressed	Units D0	D1	D2	D3	Tens D4	D5	D6	D7	
1/10,000 of Seconds	(00H)	0	0	0	0	0	X	X	X	X	9	(08H)	0	0	0	0	X	X	X	X	
Hundredths and Tenths Sec	(01H)	X	X	X	X	9	X	X	X	X	9	(09H)	X	X	X	X	X	X	X	X	
Seconds	(02H)	X	X	X	X	9	X	X	X	0	5	(0AH)	X	X	X	X	X	X	X	X	
Minutes	(03H)	X	X	X	X	9	X	X	X	0	5	(0BH)	X	X	X	X	X	X	X	X	
Hours	(04H)	X	X	X	X	9	X	X	0	0	2	(0CH)	X	X	X	X	X	X	X	X	
Days of the Week	(05H)	X	X	X	0	7	0	0	0	0	0	(0DH)	X	X	X	X	0	0	0	0	*
Days of the Month	(06H)	X	X	X	X	9	X	X	0	0	3	(0EH)	X	X	X	X	X	X	X	X	
Month	(07H)	X	X	X	X	9	X	0	0	0	1	(0FH)	X	X	X	X	X	X	X	X	

X—Indicates D or 1
0—Indicates unused bits
TRI STATE® is a registered trademark of National Semiconductor Corp.

* These bits are not RAM locations—they are always 0.
All other bits may be read or written.

Table 7 Real Time Counter and RAM Format

3.1.4 Periodic Interrupts

Periodic interrupts may be generated at 10Hz (100 milliseconds), once per second, once per minute, once per hour, once per day, once per week or once per month. To enable this, a "1" is written into the interrupt control register, at a bit location corresponding to the desired output frequency, as shown in Table 8.

Interrupt Register Format								
	D0	D1	D2	D3	D4	D5	D6	D7
READ Base + 10H	RAM Compare	1/10 Sec.	1 Sec.	1 Min.	1 Hour	1 Day	1 Week	1 Month
WRITE Base + 11H	RAM Compare	1/10 Sec.	1 Sec.	1 Min.	1 Hour	1 Day	1 Week	1 Month

Table 8 Interrupt Register Format

Once one or more bits have been set, the corresponding counters roll over to 0 count and then the counters will cause the interrupt status output to go high. To reset and identify the frequency which caused the interrupt, the status register is read. Reading then places the contents of the status register on the data bus. The frequency will be identified by a "1" in the respective bit position. The completion of a read will reset the interrupt.

The clock chip on the MSC 8901 board contains a second interrupt output-standby. This output is connected to a jumper post at location E2. This output is not supported by the MSC 8901 board, however, it is provided for user applications.

Base Address +	Function
00H	Counter—Ten Thousandths of Seconds
01H	Counter—Hundredths and Tenths of Seconds
02H	Counter—Seconds
03H	Counter—Minutes
04H	Counter—Hours
05H	Counter—Day of Week
06H	Counter-Day of Month
07H	Counter—Month
08H	RAM—Ten Thousandths of Seconds
09H	RAM—Hundredths and Tenths of Seconds
0AH	RAM—Seconds
0BH	RAM—Minutes
0CH	RAM—Hours
0DH	RAM—Day of Week
0EH	RAM—Day of Month
0FH	RAM—Months
10H	Interrupt Status Register
11H	Interrupt Control Register
12H	Counter Reset
13H	RAM Reset
14H	Status Bit
15H	GO Command
16H	Standby Interrupt
17H	Not Used

Table 9 Address Codes and Functions

3.1.5 Reading the Clock

Reading the clock is accomplished simply by writing a program which will read data from these same I/O locations. This process is essentially, the reverse of that used for setting the clock.

The purpose of the status in the status register is to inform the user that the clock is in the process of rolling over when a counter is read. The system clock into the thousandths of seconds counter has a pulse width of 61 microseconds. If a read of the real-time counter is done during this 61

microsecond period, the status bit will be set, indicating that the clock is rippling through the real-time counter. Because the clock is rippling, invalid data may be read from the counter at this time, so if the status bit is set following a counter read, the counter should be reread.

The status bit appears on DO when address base + 14H is read. All the other data lines will be zero. The status bit is set when a logical one appears, and should be read every time a counter read or series of counter reads is performed. The trailing edge of the read at address base + 14H will reset the status bit.

3.1.6 Resetting Counters

Individual counters and RAM locations may be reset by writing data with the appropriate bit or bits set to address base + 12 for counters, or address base +13 for RAM. Refer to Table 10 for exact bit patterns.

D0	D1	D2	D3	D4	D5	D6	D7	Counter or RAM Reset
1	0	0	0	0	0	0	0	Ten Thousands of Seconds
0	1	0	0	0	0	0	0	Hundredths and Tenths of Seconds
0	0	1	0	0	0	0	0	Seconds
0	0	0	1	0	0	0	0	Minutes
0	0	0	0	1	0	0	0	Hours
0	0	0	0	0	1	0	0	Days of the Week
0	0	0	0	0	0	1	0	Days of the Month
0	0	0	0	0	0	0	1	Months

For counters reset address = 12H

For RAM, reset address = 13H

Table 10 Counter and RAM Reset Format

3.1.7 Adjusting the Clock

The crystal oscillator that drives the clock and is responsible for its accuracy has been set at the factory. A variable capacitor, C3, is used to adjust the actual frequency of oscillation by a small amount. If the clock does not keep time accurately over a period of a week, a small adjustment of C3 may correct the problem.

Note that the area around C3, Y1, and C4 are high impedance circuits and touching the board in this area while the clock is running can cause great changes in the oscillator frequency and affect the timekeeping accuracy.

3.2 THE MEMORY EXTENDER/PAGE MAPPER

The Memory Extender/Page Mapper circuit can be viewed as consisting of two functional blocks (as illustrated in Figure 3): the Priority Arbitrator and the Page Mapper RAM.

3.2.1 Parallel Priority Arbitrator

The Parallel Priority Arbitrator serves a dual function.

1. It provides parallel bus master arbitration among multiple bus masters.

2. It supplies the Page Mapper RAM with the identity of the current bus master.

Information on bus masters is used to select one of the eight locations in Page Mapper RAM. The data at the selected location is asserted on address lines AD10 to AD17, depending on how the jumpers were set. This data is appended to the 16 or 20 bits of address generated by the bus master; in this way, a 24-bit address is obtained.

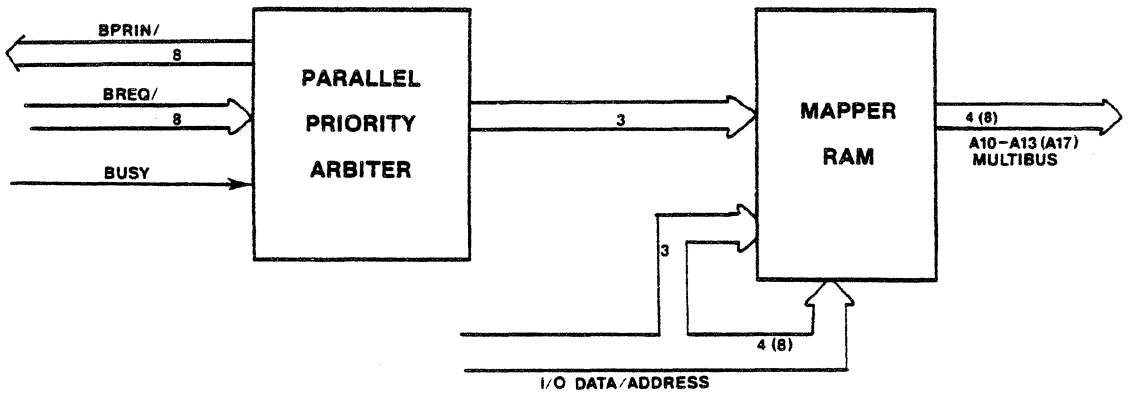


Figure 3 Block Diagrams of the Memory Extender/Page Mapper

3.2.2 Page Mapper RAM

The data contained in the Page Mapper Ram can be read or written at eight consecutive I/O locations. That data which is appended to the present Multibus address then corresponds to the data whose address is the priority level of the bus master currently controlling the bus.

For example: Consider a system containing two processor boards, where processor "A" is assigned a priority of 6 and processor "B" is assigned a priority of 5.

When processor "A" is using memory on the Multibus, the data in RAM location 6 (corresponding to "A's" priority of 6) will be appended to the processor's own 16 bits of address. This provides a 20-bit address on the Multibus. Likewise, when processor "B" is using memory on the Multibus, the data in mapper RAM location 5 will be appended to processor "B's" 16 bits of address. However, if processor "B" can generate 20 address bits, then nothing will be asserted on address lines AD10 to AD13 when processor "B" is in control of the bus directly.

The memory mapper does not modify the 16 address bits generated by the bus master. It simply asserts 4 (or 8) additional address lines on the Multibus, effectively expanding the processor's addressing range to 1 megabyte (or 16 megabytes).

The information from the priority arbitrator also goes to a decoder. The outputs of this decoder go to a number of jumpers which have been set up to tell the MSC 8901 how many address bits each bus master can generate. This information is used by the decoder to enable or disable the address drivers for the address lines which the MSC 8901 can control.

In order for a processor to access memory on the Multibus, the processor must write the four high order address bits to its particular I/O location on the MSC 8901 board. The eight locations of the Mapper RAM are at addresses base + 18H through base + 1FH. Table 11 shows the hexidecimal value which must be added to the base address (the same as the starting address for the real time clock) to obtain the proper four high order address bits.

For Example: If a processor in slot 4 wants to access memory at address 50000H, it would have to first write 05H to I/O location base + 1CH. After this is done, anytime the processor in slot 4 accesses the Multibus for memory operations, it will access the 5th 64K block of memory. The MSC 8901 will supply the four highest addresses and the processor will supply the other 16 addresses. In this way each processor can access a different 64K page whenever it accesses the Multibus for memory.

I/O Address of Mapper RAM	Backplane Slot Priority
Base + 1FH	HIGHEST 7
1EH	6
1DH	5
1CH	4
1BH	3
1AH	2
19H	1
18H	LOWEST 0

Data Format							
D7	D6	D5	D4	D3	D2	D1	D0
Add 17	Add 16	Add 15	Add 14	Add 13	Add 12	Add 11	Add 10

Note 1: Data is read/written in true form.

Note 2: D4-D6 may only be read/written if customer-supplied, optional RAM is installed in U10.

Table 11 I/O Addresses to Access Memory

3.3 INDICATOR LEDs

Indicator LEDs are located on the top right corner of the MSC 8901 board (to the immediate right of the batteries). They are used to indicate which of the bus masters is currently in control of the bus, and the LEDs are lit only for the duration of a bus transaction. Since a bus transaction may be approximately a microsecond in duration, a single bus transaction will not be visable. Many bus transactions will cause the LEDs to glow.

SECTION 4

WARRANTY

4.1 General

Monolithic Systems Corporation (MSC) warrants for a period of one (1) year from the date of shipment that each item of equipment manufactured by MSC shall be free from defects in material and workmanship under normal use and service.

In the event of a failure of a product covered by this warranty within 1 (one) year of the original purchase, MSC will repair such product without charge provided the warrantor's examination concludes to its satisfaction that the product was defective. The warrantor may at its option, replace the product in lieu of repair. If the failure has been caused by misuse, neglect, accident, user modification, or abnormal conditions of operations, the warranty shall become void and product subject to normal repair charges. In such cases, an estimate will be submitted before repair is performed.

All replaced products and/or components shall become MSC property.

The foregoing warranty is in lieu of all other warranties, promises, affirmations, or representations, whatsoever, expressed or implied, including, but not limited to, any implied warranty of merchantability or implied warranty of fitness of equipment for a particular purpose, and of any other obligations on the part of the seller.

4.2 Warranty Registration

To implement the warranty, please complete the WARRANTY REGISTRATION card located at the front of this manual and return it to Monolithic Systems Corporation.

4.3 Warranty Service

To obtain warranty service, the buyer must:

1. Contact MSC and provide Customer Service with part number, serial number, and nature of defect. Customer Service will issue a Warranty Return Authorization number.

2. Pack product in original container, if available, or in a rigid container of adequate size. Product should be wrapped to protect it from static discharge and packed in a shock absorbing material. Include Warranty Return Authorization number on outside of shipping container.

3. Ship product prepaid to MSC Customer Service, 84 Inverness Circle East, Englewood, Colorado 80112.

4. MSC will return the product prepaid via U.P.S. Request for any other transportation will be subject to customer expense.

REVISIONS				
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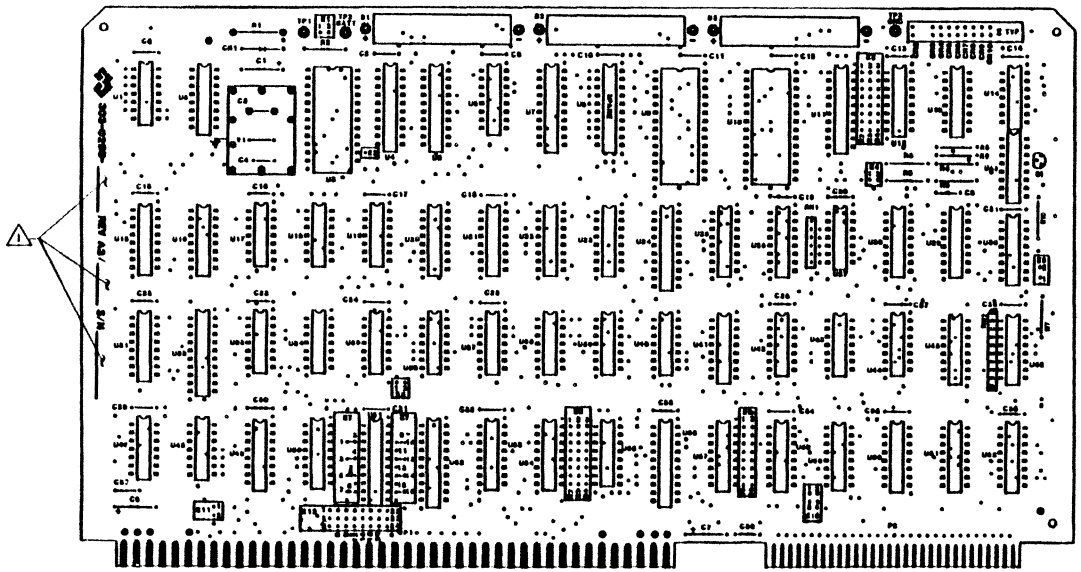
3341	C	ARTWORK & DOCUMENTATION UPDATE		



-001

2. SEE PRIME SYSTEM FOR PARTS LIST.

⚠1 FOR STAMPING INFORMATION, REFER TO 313-0003-006 & -007.

NOTES UNLESS OTHERWISE SPECIFIED

MSP - 1009

	MSC 8901
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN Dale Greaves	8/3/82
CHECKED Dale	7/15/82
APPROVED	
APPROVED	
PHASE	

REV	C
SHEET	1

REVISION STATUS OF SHEETS

MONOLITHIC SYSTEMS CORP.
ENGLEWOOD, COLORADO 80112

TITLE:
PCA BOARD
MSC 8901
MEMORY MANAGEMENT

SIZE	CODE IDENT NO.	DRAWING NO.	REV
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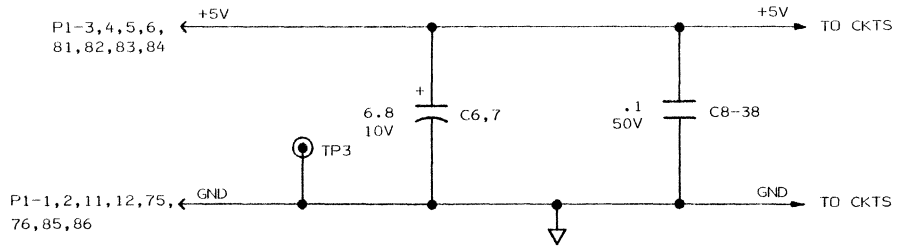
SCALE 1/1 SHEET 1 OF 1



REVISIONS				
LTR	ECO	DESCRIPTION	DATE	APPRV'D
C	3341	ENG RLSE PER ECO	↓	↓
D	3281	REV. PER ECO Dale C 7/23/82	7-30-82	[illegible]

3.) IC POWER & GROUND CONNECTIONS NOT SHOWN ON SCHEMATIC:

REFERENCE DESIG.	+5 PIN	GND PIN
U1,14,17,18,19,27,28, 30,33,34,35,36,37,38, 39,40,42,43,44,47,48	14	7
U2,6,12,13,15,16,20,21, 22,23,25,26,29,31,41, 45,46,49,50,53,54,55, 57,58,59,60,61,62	16	8
U4,5,7,11,24,32,51,52, 56	20	10
U3	24	12
U9,U10	28	14

2.) ALL CAPACITANCES IN MICRO-FARADS, ±20% TOL.

1.) ALL RESISTANCES IN OHMS, 1/4 WATT, 5%.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	D	D	C	C	C	C	C	C	C												
SHEET	1	2	3	4	5	6	7	8	9												

REVISION STATUS OF SHEETS

LAST USED									
NOT USED									

REFERENCE DESIGNATIONS LAST USED/NOT USED

DRAWN	
CHECKED Dale C	12/15/81
APPROVED [illegible]	1/12/82
APPROVED	

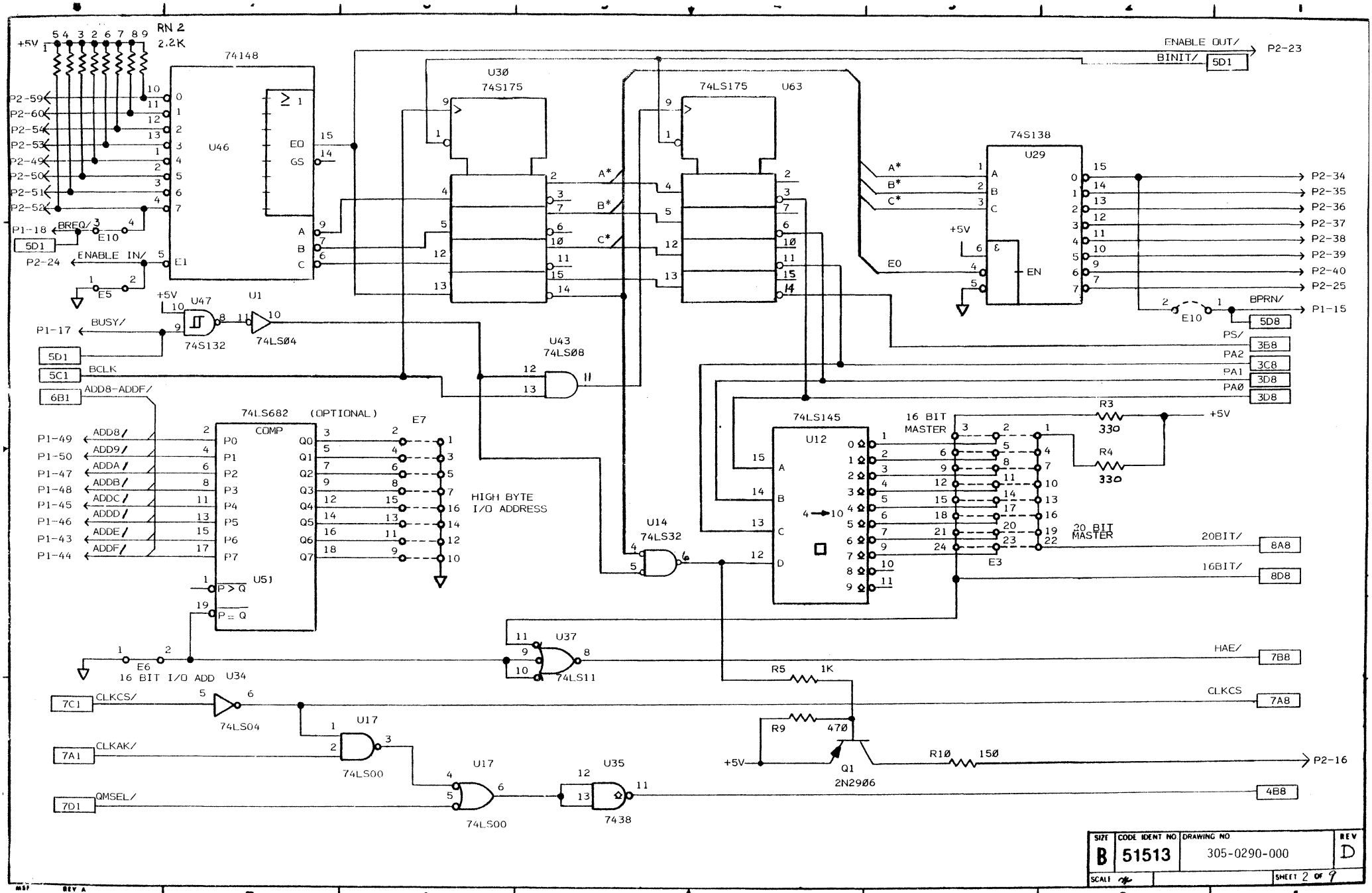
MONOLITHIC SYSTEMS CORP.
Englewood, Colorado 80112

TITLE: SCHEMATIC, MSC 8901 MEMORY MANAGEMENT

SIZE	CODE IDENT NO.	DWG NO.
B	51513	305-0290-000

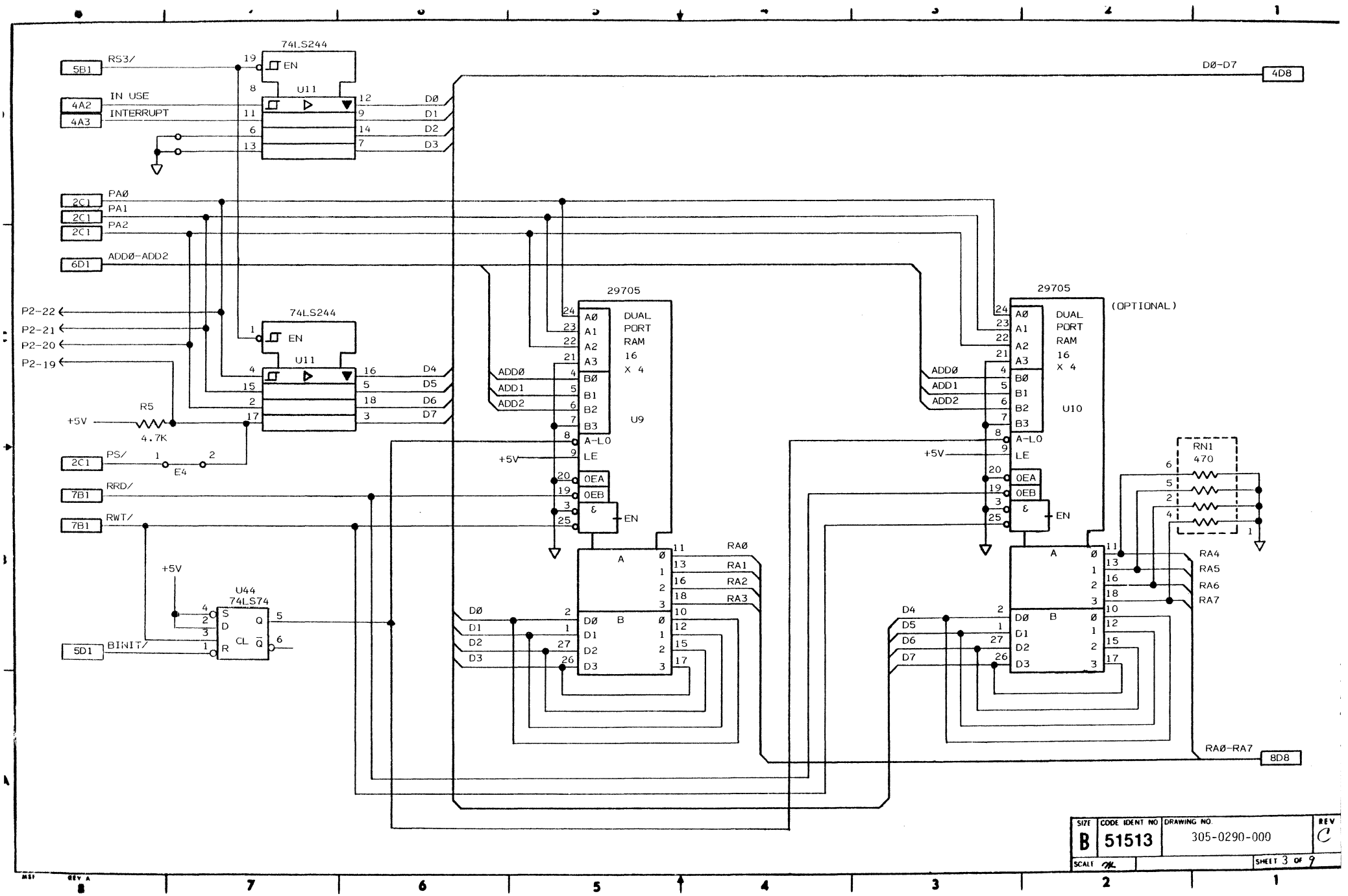
SCALE NONE | SHEET 1 of 9

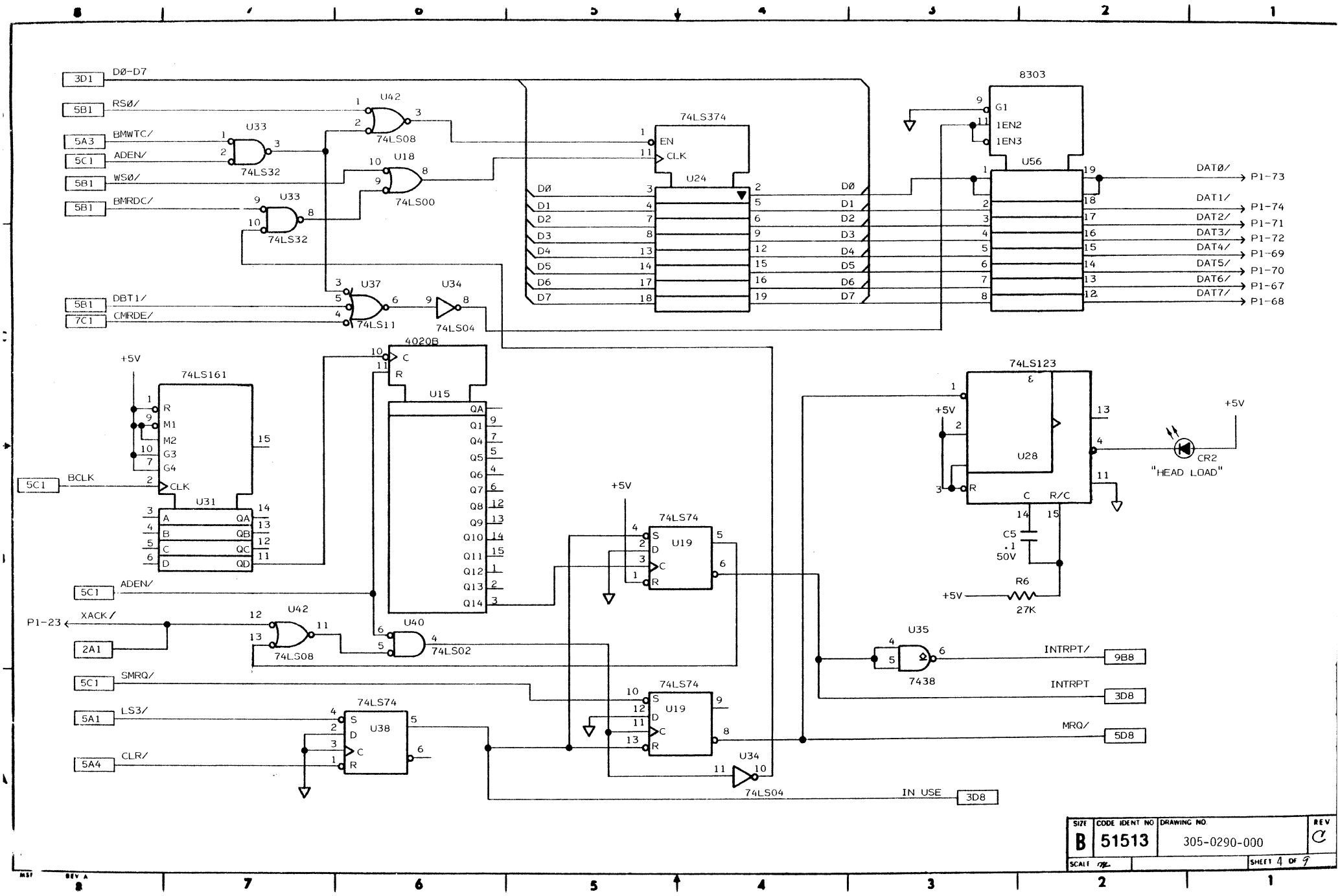
MSF 1052



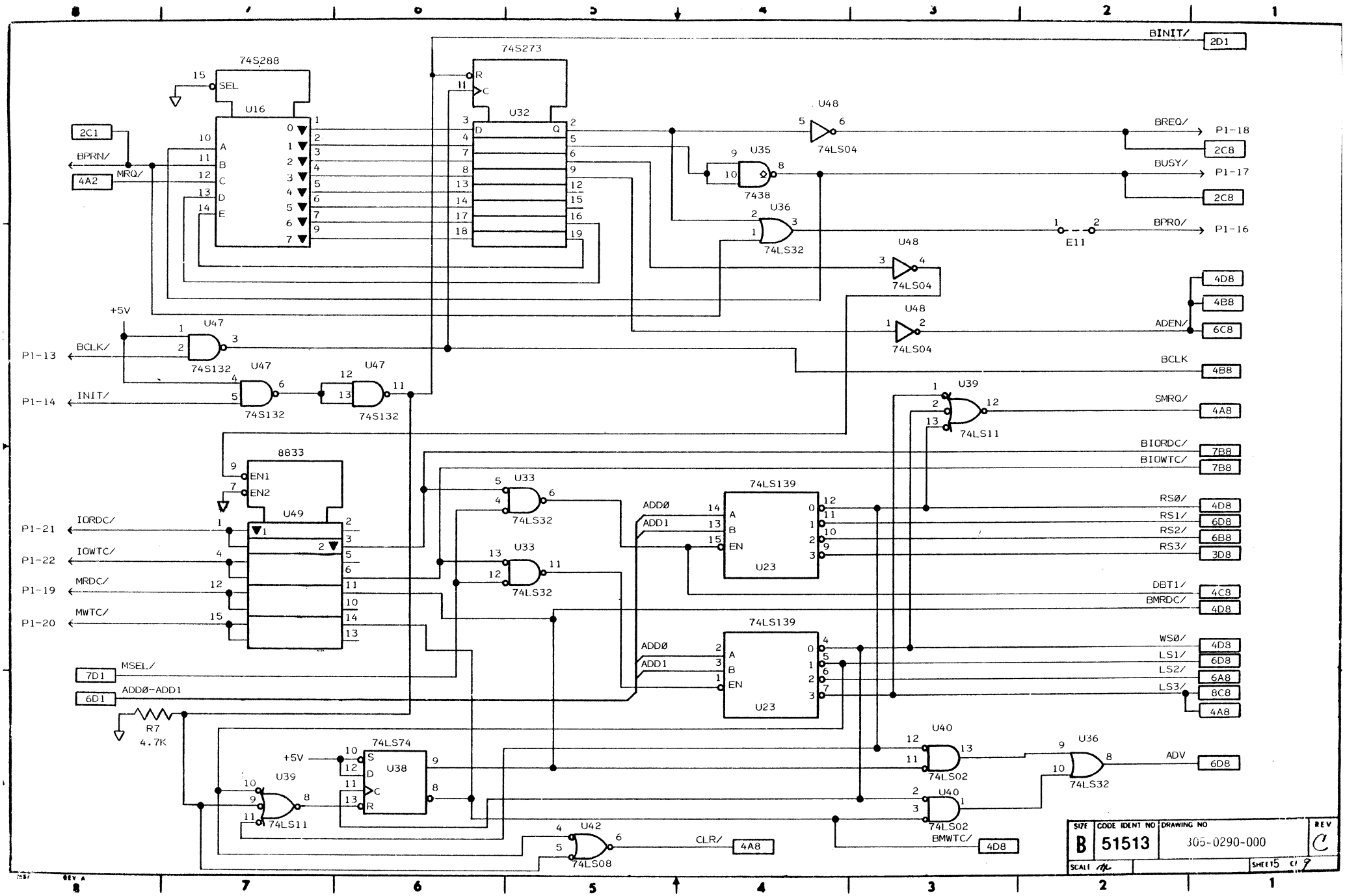
SIZE	CODE IDENT NO	DRAWING NO	REV
B	51513	305-0290-000	D
SCALE		SHEET 2 OF 9	

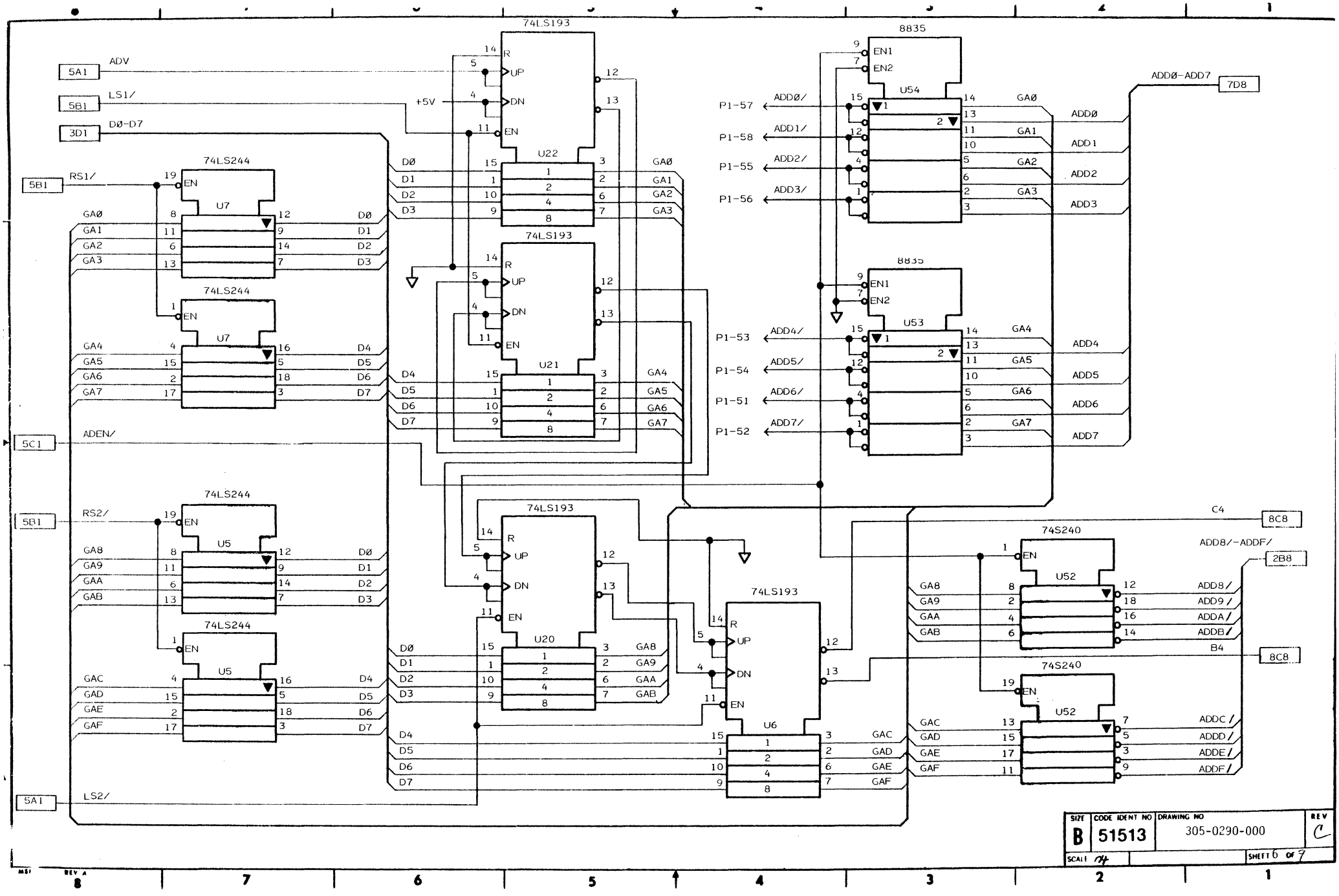
MSF REV A


74LS244
U11
RS3/
5B1
IN USE
4A2
INTERRUPT
4A3
EN
D0
D1
D2
D3
D0-D7
4D8
PA0
PA1
PA2
2C1
ADD0-ADD2
6D1
P2-22
P2-21
P2-20
P2-19
R5
+5V
4.7K
PS/
E4
RRD/
7B1
RWT/
29705
DUAL
PORT
RAM
16
X 4
U9
U10
(OPTIONAL)
A0
A1
A2
A3
B0
B1
B2
B3
A-L0
LE
0EA
0EB
ADD0
ADD1
ADD2
RA0
RA1
RA2
RA3
RA4
RA5
RA6
RA7
RN1
470
U44
74LS74
BINIT/
5D1
RA0-RA7
8D8
SIZE
B
CODE IDENT NO
51513
DRAWING NO.
305-0290-000
REV
C
SCALE
SHEET 3 OF 9

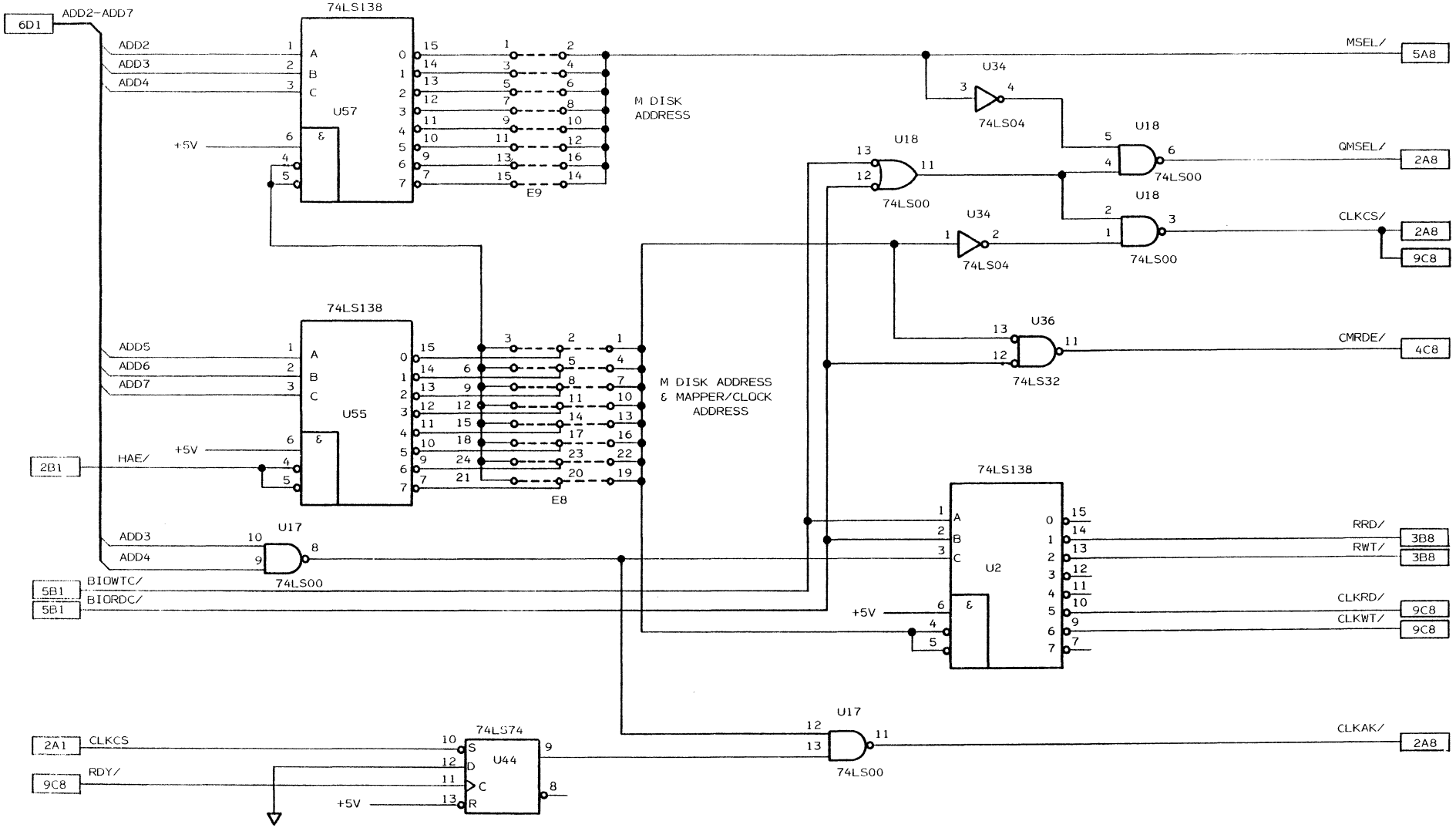


SIZE	CODE IDENT NO	DRAWING NO.	REV
B	51513	305-0290-000	C
SCALE			SHEET 4 OF 9

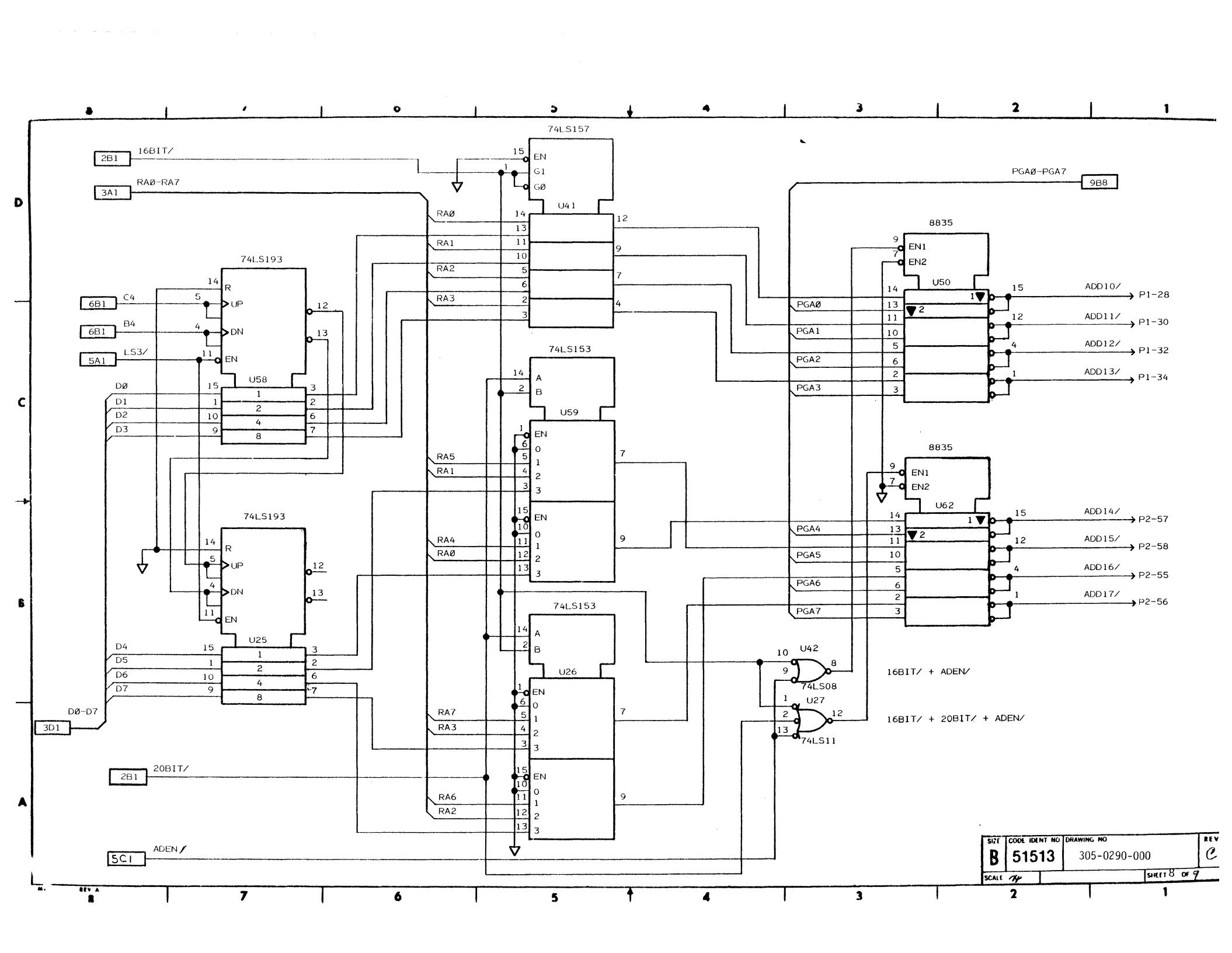

BINIT/
2D1
74S288
U16
SEL
2C1
BPRN/
4A2
MRQ/
74S273
U32
U48
74LS04
U35
7438
U36
74LS32
BREQ/
P1-18
2C8
BUSY/
P1-17
2C8
BPRO/
P1-16
E11
4D8
4B8
ADEN/
6C8
BCLK
4B8
+5V
U47
74S132
P1-13
BCLK/
P1-14
INIT/
SMRQ/
4A8
U39
74LS11
BIORDC/
BIOWTC/
7B8
7B8
8833
U49
EN1
EN2
P1-21
IORDC/
P1-22
IOWTC/
P1-19
MRDC/
P1-20
MWTC/
U33
74LS32
74LS139
U23
ADDØ
ADD1
RSØ/
RS1/
RS2/
RS3/
4D8
6D8
6B8
3D8
DBT1/
BMRDC/
4C8
4D8
WSØ/
LS1/
LS2/
LS3/
4D8
6D8
6A8
8C8
4A8
7D1
MSEL/
6D1
ADDØ-ADD1
R7
4.7K
74LS74
U38
U40
74LS02
ADV
6D8
CLR/
4A8
74LS08
U42
BMWTC/
4D8
SIZE
B
CODE IDENT NO
51513
DRAWING NO
305-0290-000
REV
C
SCALE
SHEET 5 OF 9



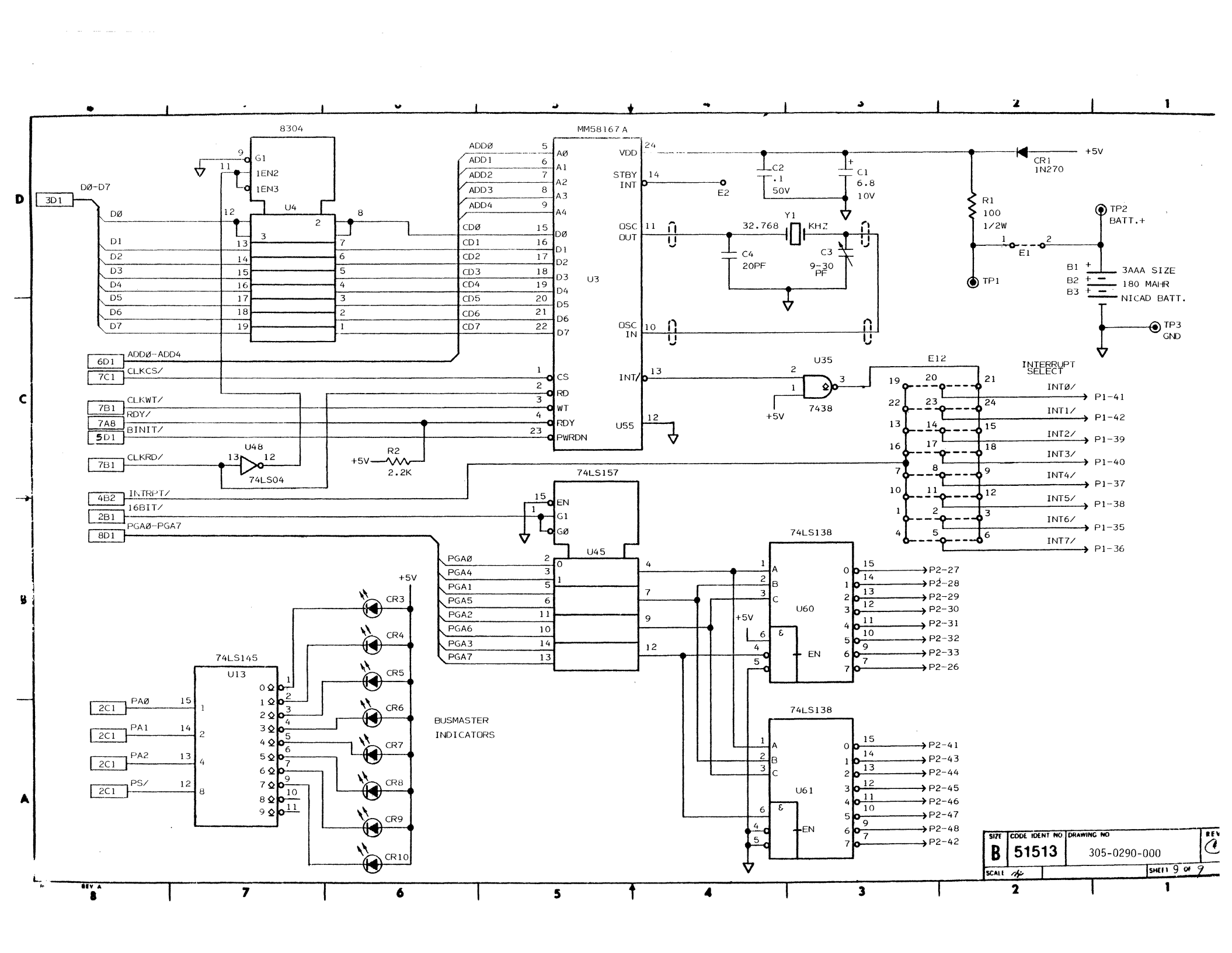
SIZE	CODE IDENT NO	DRAWING NO	REV
B	51513	305-0290-000	C
SCALE 1/4		SHEET 6 OF 7	



SIZE	CODE IDENT NO	DRAWING NO.	REV
B	51513	305-0290-000	C
SCALE NONE		SHEET 7 OF 9	



SIZE	CODE IDENT NO	DRAWING NO	REV
B	51513	305-0290-000	C
SCALE 1/4		SHEET 8 OF 9	


8304
MM58167A
U4
U3
U35
U48
U45
U60
U61
U13
74LS04
74LS157
74LS138
74LS138
74LS145
7438
D0-D7
3D1
ADD0-ADD4
6D1
CLKCS/
7C1
CLKWT/
7B1
RDY/
7A8
BINIT/
5D1
CLKRD/
7B1
INTRPT/
4B2
16BIT/
2B1
PGA0-PGA7
8D1
R2
2.2K
+5V
C1
6.8
10V
C2
.1
50V
C3
9-30
PF
C4
20PF
Y1
32.768
KHZ
CR1
1N270
R1
100
1/2W
E1
E2
E12
TP1
TP2
BATT.+
TP3
GND
B1
B2
B3
3AAA SIZE
180 MAHR
NICAD BATT.
INTERRUPT
SELECT
INT0/
INT1/
INT2/
INT3/
INT4/
INT5/
INT6/
INT7/
P1-41
P1-42
P1-39
P1-40
P1-37
P1-38
P1-35
P1-36
P2-27
P2-28
P2-29
P2-30
P2-31
P2-32
P2-33
P2-26
P2-41
P2-43
P2-44
P2-45
P2-46
P2-47
P2-48
P2-42
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
BUSMASTER
INDICATORS
PA0
PA1
PA2
PS/
2C1
ADD0
ADD1
ADD2
ADD3
ADD4
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
PGA0
PGA4
PGA1
PGA5
PGA2
PGA6
PGA3
PGA7
CS
RD
WT
RDY
PWRDN
INT/
STBY
INT
OSC
OUT
OSC
IN
VDD
SIZE
B
CODE IDENT NO
51513
DRAWING NO
305-0290-000
SCALE
SHEET 9 OF 9
REV A