

MAINTENANCE MANUAL

MONOSTORE V/PLANAR

PDP-8 ADD-IN

SEMICONDUCTOR MEMORY SYSTEM

MSC 3102

		REVISIONS		
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Α		ENG RELEASE	1/21/75	TSP
В		REVISED	9/12/75	J.W.
С		ADDED PARA. 4.4	7/28/76	J.W.

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# MONOSTORE V/PLANAR PDP-8 Add-In

# SEMICONDUCTOR MEMORY SYSTEM

# CONTENTS

SECTION	I GENERAL DESCRIPTION	PAGE
1.2 1.3	INTRODUCTION GENERAL DESCRIPTION MODES OF OPERATION SYSTEM SPECIFICATIONS	3 4 4 4
SECTION	II INSTALLATION & OPERATION	
2.2 2.3	INTRODUCTION UNPACKING AND INSPECTION INSTALLING MEMORY SYSTEM I/O SIGNALS	6 6 6 7
SECTION	III THEORY OF OPERATION	
3.2 3.3 3.4	INTRODUCTION  MEMORY LOCATION PROGRAMMING  ADDRESS CHANNEL  DATA CHANNEL  TIMING CIRCUITRY	8 8 9 9
SECTION	IV MAINTENANCE AND TROUBLESHOOTING	
4.2	INTRODUCTION PREVENTIVE MAINTENANCE TROUBLESHOOTING	12 12 12
SECTION	V DRAWINGS	14
5.2	PARTS LIST ASSEMBLY SCHEMATIC	



SIZE | CODE IDENT NO. DWG NO.

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SCALE

REV A

SHEET

### SECTION I

### GENERAL DESCRIPTION

### 1.1 INTRODUCTION

This manual provides information for installing, operating, and maintaining the MONOSTORE V/Planar PDP-8 add-in memory systems. The material is arranged in five sections as follows:

Section I General Description

This section provides the scope, contents, and arrangement of the manual. A general description and a list of system specifications are also given.

Section II Installation and Operation

Instructions are provided for unpacking, inspecting and installing the memory system.

Section III Theory of Operation

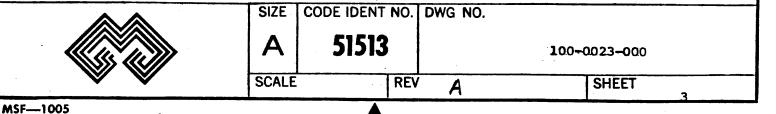
An overall description of the memory system is provided along with a timing diagram to aid in understanding the system and to support troubleshooting.

Section IV Maintenance and Troubleshooting

This section gives recommended general maintenance procedures and troubleshooting information for diagnosing and locating a malfunction.

Section V Drawings

This section contains schematics, assembly, and parts list for the memory system.



### 1.2 GENERAL DESCRIPTION

The MONOSTORE V/Planar PDP-8 Add-In Memory System, P/N 303-0112-000, consists of a single planar 8Kx12 memory assembly. All electronics and semiconductor static N-channel memory storage elements are contained on a single printed circuit board.

All signal interface is made through the DEC OMNIBUSTM Assembly. Data interfacing is provided by 12 bidirectional data bits. Addressing any one of the 8192 words is provided by 13 binary address bits, together with command and control information to define the memory mode required.

The memory system uses the +5V power available on the OMNIBUS assembly.

The maximum capacity of the board is 8192 words by 12 bits. The system can also be configured in 1024 word increments from 1024 up to and including 8192 words.

#### MODES OF OPERATION 1.3

Read Cycle - 1.2 M sec Transfers data from memory to the OMNIBUS.

Read/Write Cycle - 1.4 Asec Transfers data from memory to the OMNIBUS during MD DIR L = 1 and then writes data into memory from the OMNIBUS during MD DIR L = 0.

MD DIR L

1

#### 1.4 SYSTEM SPECIFICATIONS

Characteristic

Storage Capacity

Specification

1024 words x 12 bits

8192 words x 12 bits

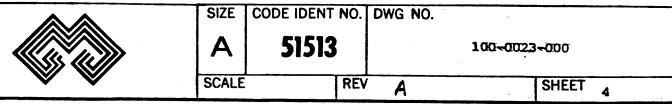
(1024 word increments)

Cycle Time Read Read/Write

1.2 A sec

1.4 Msec

NOTE: DEC and OMNIBUS are trademarks of Digital Equipment Corporation.



1.4 System Specifications continued ...

Characteristic

Read Access Time

Input Power

Operating Environment Temperature Relative Humidity

Physical Dimensions Height Depth Width Specification

600 nsec

+5V . 33.0 amps

0°C to +50°C 90% maximum without condensation.

8.44 inches 0.5 inches 10.44 inches

SIZE | CODE IDENT NO. | DWG NO.

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### SECTION II

### INSTALLATION & OPERATION

# 2.1 INTRODUCTION

This section contains information for installation and operation of the memory system.

# 2.2 UNPACKING AND INSPECTION

Carefully remove the memory system from the shipping container. Remove any packing material from the assembly. Inspect the system for any damage or loose connections.

# 2.3 INSTALLING MEMORY SYSTEM

Remove the external top cover from the PDP-8 computer. Insert the memory system into the OMNIBUS Assembly. Reassemble the top cover. The memory system is now ready for use.

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# I/O SIGNALS

				<del> </del>				
PIN	Dl	D2	Cl	C2	B1	<b>B</b> 2	A1	A2
<u> </u>	TP	+15V	TP	+5V	TP	+5V	TP	+5V
_B	TP	-15V	<b>T</b> P	<b>-1</b> 5v	TP	<b>-15</b> V	TP	<b>-1</b> 5V
_c	GND	GND	<b>GN</b> D	<b>G</b> ND	GND	<b>GN</b> D	SP GND*	GND
Ð	MASL	IROL	I/O PAUSE L	трін	MA4L	INT STROBE L	MAOL	EMAOL
E	MA9L	IRLL	COL	TP2H	MA5L	BRK IN PROG L	MAIL	<b>E</b> MAlL
F	<b>GN</b> D	GND	GND	<b>GN</b> D	GND	<b>GN</b> D	GND	<b>GN</b> D
Ħ	MAlOL	IR2L	ClL	<b>Т</b> РЗН	MA6L	MA, MS LOAD CONT L	MA2L	EMA2L
J	MA11L	FL	C2L	ТР4н	MA7L	OVERFLOW L	MA3L :	MEM START L
K	MDSL	DL	BUS STROBE L	TS1L	MD4L	BREAK DATA CONT L	MDOL	MD DIR L
L	MD9L	. EL	INTERNAL I/O L	TS2L	MD5L	BREAK CYCLE L	MD1L	SOURCE H
M	MD10L	DSER MODE H	NOT LAST XFER L	TS3L	MD6L	LA ENABLE L	MD2L	STROBE H
n	<b>GN</b> D	<b>G</b> ŃD	<b>GN</b> D	<b>GN</b> D	GND	<b>GN</b> D	<b>GN</b> D	<b>GN</b> ID
P	MD11L	F SET L	INT ROST L	TS4L	MD7L	INT IN PROG H	MD3L	INHIBIT H
R	DATA 8L	PULSE LA H	INITIALIZE H	LINK DATA L	DATA 4L	RES 1 H	DATA OL	RETURN H
s	DATA 9L	STOP L	SKIP L	LINK LOAD L	DATA 5L	RES 2H	DATA 1L	WRITE H
T	<b>GN</b> D	GND	<b>GN</b> D	<b>GN</b> D	<b>GM</b> D	<b>CEN</b> ID	<b>CEN</b> ID	<b>GN</b> D
ט	DATA 10L	KEY CONTROL L	CPMA DISABLE L	IND 1L	DATA 6L	RUN L	DATA 2L	ROM ADDRESS L
٧	DATA 11L	SW	MS, IR DISABLE L	IND 2L	DATA 71	POWER OK H	DATA 3L	LINK L



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### SECTION III

## THEORY OF OPERATION

# 3.1 INTRODUCTION

This section describes the overall organization and operation of the MONOSTORE V/Planar PDP-8 Add-in Semiconductor Memory System. The system has a maximum capacity of 8192 words of 12 bits.

This section is organized into the following major parts:

Description	Paragraph
Memory Location Programming	3.2
Address Channel	3.3
Data Channel	3.4
Timing Circuitry	3.5

# 3.2 MEMORY LOCATION PROGRAMMING

The memory location is programmed via wire jumpers on the board. The user can program the memory to any location according to the following table:

STARTING	~	(TT T =	1777	1			<del>.</del>		
		HI LE EMA		1	x8K GRAM	BOARD	MOD EN PROGRAM		
ADDRESS	0	1	2	С	D	CAPACITY	A	В	
OK	0	0	0	E	F	4K 8K	1	A 2	
<b>4</b> K	0	0	1	F	E	4K 8K	2 2	A 3	
<b>8</b> K	0	1	0	Е	F	4K 8K	3	A 4	
12K	0	1	1	F	E	4K > 8K	4	A 5	
16K	1	0	0	Ė	F	4K 8K	5 5	<b>A</b> 6	
<b>2</b> 0K	1	0	1	F	E	4K 8K	6 6	A 7	
24K	1	1	0	E	F	4K 8K	7	<b>A</b> 8	
<b>28</b> K	1	1	1	P	E	4K	8	A	

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# 3.2 Memory Location Programming continued ...

The computer generated addresses EMAO, EMAI, and EMA2 are decoded in blocks of 4K with a maximum of two 4K blocks of memory on a single board. If the generated addresses are within the programmed range a memory cycle will be initiated by MEM START L. This circuitry is shown on Sheet 1 of the schematic.

# 3.3 ADDRESS CHANNEL

When a memory cycle is initiated the information on the address lines MAOL -> MAILL is used as follows:

MA2L - MAllL - These address bits are buffered in order to drive the complete memory array.

MAOL, MAIL - These address bits are decoded in conjunction with EMA2 to generate the 1K, 2K...8K cenable pulses required by the memory elements. The cenable pulse then enables only one row of memory elements at any one time thereby preventing interaction of data bits.

The address channel and cenable circuits are shown on Sheet 1 of the schematic.

## 3.4 DATA CHANNEL

When a memory cycle, READ, is initiated, the information previously stored in the memory elements is accessed and transmitted onto the MDOL  $\rightarrow$  MDILL lines for use by the computer for as long as MD DIR L = 1.

When a memory cycle, READ/WRITE, is initiated the READ cycle is repeated until MD DIR L = 0. At that time the WRITE phase of the memory cycle is performed and the information on the MDOL  $\rightarrow$  MDILL lines is buffered and stored in the memory elements at the same address as the first phase READ portion of the cycle.

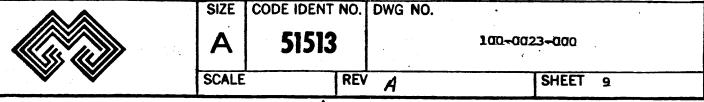
The data channel circuit is shown on Sheet 2 of the schematic.

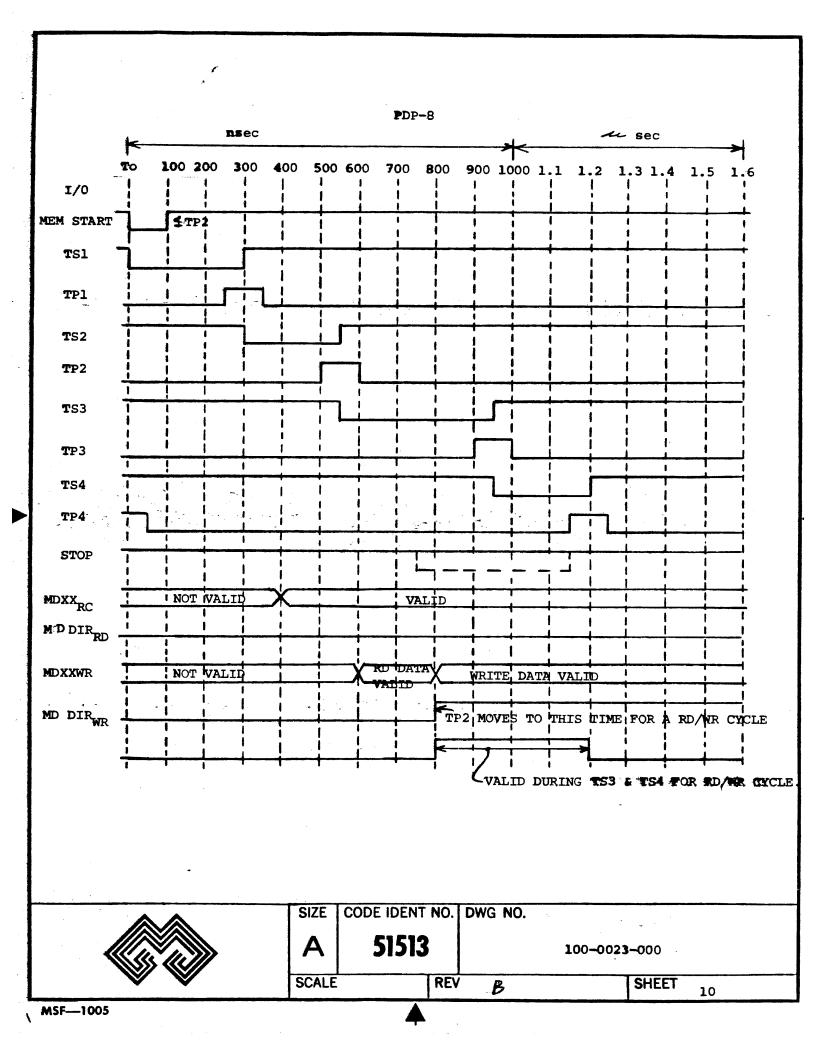
## 3.5 TIMING CIRCUITRY

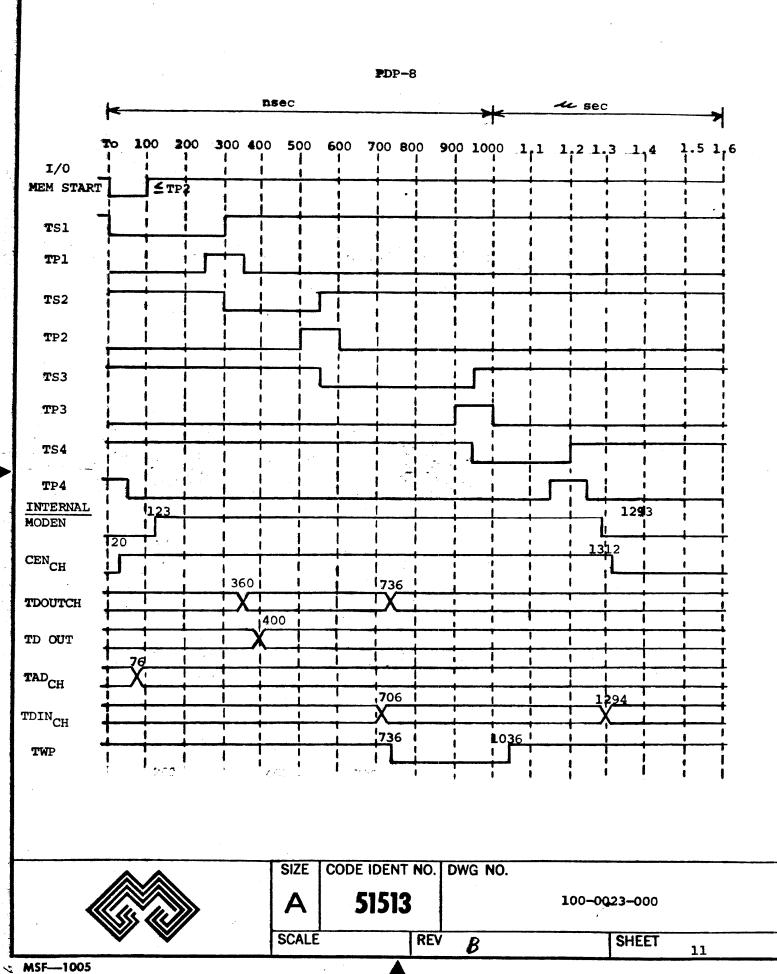
All internal and I/O pulses or signals, except the storage element "write" pulse, are generated from timing pulses TSLL -> TS4L, TPLH->TP3H, received at the OMNIBUS interface.

The MEM START L signal is received by the memory system and generates a READ or READ/WRITE cycle depending upon whether MD DIR L is a "1" or "1/0" respectively.

The timing pulses and signals at the CMNIBUS interface are generated according to the following timing diagram. The miscellaneous timing and control circuitry is shown on Sheets 1 and 2 of the schematic.







### SECTION IV

### MAINTENANCE AND TROUBLESHOOTING

### INTRODUCTION

This section presents troubleshooting instructions for ease of trouble location. Further localization of the trouble is to be found by means of the maintenance drawings in Section V. The theory of operation in Section III should be read and understood, along with a detailed review of the schematics in Section V in order to make effective use of this section.

### PREVENTIVE MAINTENANCE

#### 4.2.1 Visual Inspection

This inspection includes checking for loose programming wires, components, and discoloration of parts. The inspection should be performed with a minimum of prying or moving of parts.

#### 4.2.2 Cleaning

Cleaning should be limited to removal of excess dust or particles. Never use any abrasive on any part of the gold fingers on the edge connectors. Low pressure compressed air can be used for removing dust or dirt and an aerosol cleaner can be used, with light brushing, to do the gold contacts.

#### 4.2.3 DC Voltages

The +5V DC voltage should be maintained at:

+5V + 5%

#### 4.3 TROUBLESHOOTING

To facilitate troubleshooting the following information, cause and effect, can be used to isolate the proglem to a particular area. From there on the schematics should be used to determine the exact component that is at fault.

## Effect

Cause

Single bit failure, all addresses.

Data receiver/driver/read register

Complete word failure, all addresses.

DC voltage/WR pulse/strobe pulse.



CODE IDENT NO. DWG NO. SIZE

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51513

SCALE

REV

SHEET

12

# 4.3 Troubleshooting continued ...

Effect

Single bit failure, single address.

Four bit failure, all addresses

Complete word failure, a 1K section.

Complete or major part of word failure, all addresses

Non-retention of data.

Cause

Memory element

Read register/read data I/O driver.

CENABLE driver/CEN programming jumpers/address circuit for MAOL and MAIL.

Address receiver/address buffer.

DC voltage.

SIZE CODE IDENT NO. DWG NO.

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SCALE

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REV

SHEET

13

# 4.4 TEST PROGRAMS

To provide reliable memory operation and to locate failed bits or locations, it is necessary to exercise the memory system with memory system tests.

The DEC memory tests which are available as standard test software are recommended for testing the MSC Monostore V/PDP-8 memory system.

Three tests are used for field maintenance and should be run periodically for preventative maintenance purposes and also used to locate memory failures. These tests are as follows:

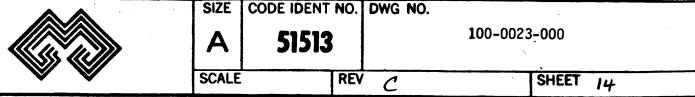
- PDP-8E EXTENDER MEMORY ADDRESS TEST, MAIN DEC-8E-DIFB-D.
- 2. PDP-8E EXTENDED MEMORY DATA AND CHECKERBOARD TEST, MAIN DEC-08-DHKMA-AD.
- 3. MEMORY ADDRESS TEST, MAIN DEC-8E-DIEC-D.

Normal trouble-shooting procedures are applied in using the memory tests.

First, the problem is isolated to a particular memory section. This is determined by the fact that the memory has been assigned a certain field (stack) identification on the memory bus. If the board is a 4K board, the unit represents one field. If the board is an 8K board, it represents two fields. There are 8 total fields numbered "O" thru "7".

Each field represents 4K with the "0" field representing the first 4K.

By looking at the table under 3.2 and checking the programming wires on



the board, the memory can be identified as to the field to which it is assigned.

In many cases, the maintenance program will call for removal of the defective memory and replacement by another.

The next level of maintenance would be to isolate a defective component. Element failures are the most probable because of the number of elements on the board. Element failures are single bit oriented failures because each element represents 1024 locations of one particular bit.

A failed element is located by examining the test program print out and then locating the element physically on the memory board. A typical print out is shown to illustrate the method.

PDP-8E EXT MEM DATA & CHKBD

SETUP SR & CONT 4 FIELDS IN THIS SYSTEM FIELDS SEL'D ARE 7 6 5 PROG WILL RELOCATE PR LOC FAIL ADR GOOD BAD **PATTERN** 01662 74000 0000 2000 ALL O - NC 01662 74000 **0000** 2000 ALL 0 - 2C 01662 74001 0000 2000 ALL O - NC 01662 74001 **0**000 **2000** ALL 0 - 2C OX

The print out shows the failed addresses (FAIL ADR), the good bit pattern and the bad bit pattern. The print out is octal. The address identifies the field by the left most digit of the address and can be read directly as field 7. This corresponds to the 5K thru 8K marked on the Monostore V/PDP-8 board. Now we know the field and must locate the particular 1K row and then the bit. This will then identify the element at fault. The



SIZE CODE IDENT NO. DWG NO.

A 51513

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SCALE

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SHEET 15

particular row is identified by the two upper bits of the next octal
digit just to be right of the left most digit. The following code applies:

OCTAL	BINA	RY	K ROW LOWER	K ROW UPPER
0	00	0	1K	5K
ì	<b>0</b> 0	1	1K	<b>5</b> K
2	01	0	<b>2</b> K	<b>6</b> K
3	01	1	2K	<b>6</b> K
4	10	0	<b>3</b> K	<b>7</b> K
5	10	1	<b>3</b> K	<b>7</b> K
6	11	0	4K	<b>8</b> K
7	11	1	<b>4</b> K	<b>8</b> K

The row is the 7K because of the 4 print out and the upper field as previously identified.

The remainder of the address tells us that the first two locations are bad. Now we must find the bit to complete the identification. The test pattern is all zeros and we see that we have an octal 2 which gives an 010. Bits are identified as 0 thru 11 from right to left. Bit 10 is bad. The complete location is the board assigned to field 7, the 3K or 7K row depending upon the field assignment and bit 10. This narrows it to one element to be replaced.

Other failures would be approached in a similar manner.



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## SECTION V

**DRAWINGS** 

PARTS LIST

303-0112-000

ASSEMBLY

303-0112-000

SCHEMATIC

305-0112-000



SIZE | CODE IDENT NO. | DWG NO.

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В	ADDED NEW MSC I.C. PARTS NOS.	3-4-76	TSP
c	REVISED ITEM 14.	9-26-76	
D	ITEMS 23 &24 REVISED PER ECO 0580	2-4-77	Bret-
E	REVISED PER ECO 0608	2/24/77	BUS
F	REVISED PER ECO 0640	5-5-77	Bref.
G	REPLACED SHEET 4 PER ECO 0681	6-16-77	BUS.
н	CHANGED PER ECO 0816	11-18-77	البري

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OF SHEETS																										
UNLESS OTHERW SPECIFIED DIMEN ARE IN INCHES ANCES FRACTION DECIMALS ANGLE		DATE										M	ON	101	.ITI	HIC	: S	YS'	TE	MS	CC	RF	•			
MATERIAL	·	DRAWN LMG 1/6/75 CHECKED							1	7OM	7 1			102 8 <b>a</b>		MBL	Y									
				APPROVED Vallenger						SIZ	1		51!	IDE1	1 TV	NO.	DV	VG 3		011:	2-0	00				
ASF - 1004									_		SCA	LE N	מש	E		REV		H		:	SHEE	1	of	4	****	

MSE-1015			QT	Y/DAS	H NC	o.	FIG. O. MATERIAL										
		002 001		001	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	NO.								
"					17	1	304-0112-001	P.C. BOARD			1						
(											2						
4					3_	3	210-0605-001	I.C. SN7475	U1,4,6		3						
`					3_	3_	210-0200-001	I.C. SN7408	U2,3,5		4						
					6	6	210-0103-0 02	I.C. SN74H04	U7,9,10,12,13,18	(	5						
					10	10	210-1104-002	I.C. 8640	U8,15,22, <b>2</b> 4,25,26,27,	28,30,35	6						
	A	SIZE			2	2	210-0100-002	I.C. SN74H00	U11,31,**		7						
					3	3	210-0105-002	I.C. SN74H10	U14,19,21		8						
	51	CODE IDENT NO.			2	2	210-0200-002	I.C. SN74H08	U16,20		9						
	51513	DENT			3_	3	210-030 <b>8</b> -001	I.C. SN7438	U17,33,34		10						
		Ö		·	1	1	210-0914-001	I.C. SN74155	U23.		11						
REV . H	7	DWG			1	1	210-0504-001	I.C. SN74123	U29		12						
		NO.									13						
	3	-			-	96	210-1003-016	MEMORY ELEMENT 2102 LHPC	U100-U195	FAIRCHILD	14						
	303-0112-000				48	-	210-1003-016	MEMORY ELEMENT 2102 LHPC	U100-U147	FAIRCHILD	14						
	12-00				96	96	208-0023-001	I.C. HEADER 16 PIN			16						
SHEET	8				1	1	317-0058-001	MODIFICATION INSTRL	· · · · · · · · · · · · · · · · · · ·		17						
ET					25	25	201-0018-001	CAP. 6.84F,10V	C3-C27		18						
2 of					31	31	701-0001-003	CAP 14F,50V	C28-58		19						
f 4							· · · · · · · · · · · · · · · · · · ·				20						
					1	1	201-0006-046	CAP 100pf	C2		21						
											22						

