2-$\overline{AD\ 15}$ LS266 7C SIP-6 V_{CC}
SW1-1 7A SIP-4 V_{CC}

2-$\overline{AD\ 14}$ LS266 7B SIP-4 V_{CC}
SW1-2 7A

2-$\overline{AD\ 13}$ LS266 7B SIP-4 V_{CC}
SW1-3 7A

2-$\overline{AD\ 12}$ LS266 7C SIP-4 V_{CC}
SW1-4 7A SELECT BLOCK A

2-$\overline{AD\ 15}$ LS266 7C SIP-4 V_{CC}
SW1-5 7A SIP-4 V_{CC}

2-$\overline{AD\ 14}$ LS266 7B SIP-4 V_{CC}
SW1-6 7A

2-$\overline{AD\ 13}$ LS266 7B SIP-4 V_{CC}
SW1-7 7A

2-$\overline{AD\ 12}$ LS266 7C SIP-4 V_{CC}
SW1-8 7A SELECT BLOCK B

2-$\overline{AD\ 15}$ LS266 8C SIP-6 V_{CC}
SW3-1 8A SIP-5 V_{CC}

2-$\overline{AD\ 14}$ LS266 8B SIP-5 V_{CC}
SW3-2 8A

2-$\overline{AD\ 13}$ LS266 8B SIP-5 V_{CC}
SW3-3 8A

2-$\overline{AD\ 12}$ LS266 8C SIP-5 V_{CC}
SW3-4 8A SELECT BLOCK C

2-$\overline{AD\ 15}$ LS266 8C SIP-4 V_{CC}
SW3-5 8A SIP-5 V_{CC}

2-$\overline{AD\ 14}$ LS266 8B SIP-5 V_{CC}
SW3-6 8A

2-$\overline{AD\ 13}$ LS266 8B SIP-5 V_{CC}
SW3-7 8A

2-$\overline{AD\ 12}$ LS266 8C SIP-5 V_{CC}
SW3-8 8A SELECT BOLCK D

A11 [87] A 23
A10 [37] B 22

SELECT BLOCK D A_0 O_1 C
SELECT BLOCK C A_1 O_2 D
SELECT BLOCK B A_2 8E O_3 $\overline{G}_2$
SELECT BLOCK A A_3 6331
A_4 CS

74LS154 3F

$\overline{MEM\ OP}$ LS32 9E
$\overline{MEM\ ENBL}$ $\overline{G}_1$ 18

SIP-6
V_{CC}
PHANTOM [67] SW4-6 8D LS00 9D $\overline{MEM\ ENBL}$
2-SELECT

2-$\overline{STATUS\ WRITE}$ LS02 9C
2-STATUS OUTPUT LS02 9C $\overline{MEM\ OP}$
SMEMR [47]

Q_{15} 7E SIP-2 V_{CC} SW5-8 SEL A-3 LS30 6E
Q_{14} SW5-7 SEL A-1
Q_{13} SW5-6 SEL A-2
Q_{12} SW5-5 SEL A-0
Q_{11} SW5-4 SEL B-3
Q_{10} SW5-3 SEL B-1
Q_9 SW5-2 SEL B-2
Q_8 SW5-1 SEL B-0
Q_7 SW6-8 SEL C-3
Q_6 SW6-7 SEL C-1 LS30 6F
Q_5 SW6-6 SEL C-2
Q_4 SW6-5 SEL C-0
Q_3 SW6-4 SEL D-3
Q_2 SW6-3 SEL D-1
Q_1 SW6-2 SEL D-2
Q_0 SW6-1 SIP-1 SEL D-0 7F

LS02 9C $\overline{BOARD\ SELECT}$

SUPERRAM 16K MEMORY MASTER
BOARD SELECT LOGIC & BANK SELECT LOGIC   COPYRIGHT 1979 G. MORROW

SUPERRAM 16K MEMORY MASTER

I/O SELECTION, DATA & ADDRESS BUFFERS

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	LOW DATA	HIGH DATA	LOW DATA	HIGH DATA	
	1	2	3	4	
A	SECTION A BLOCK 0	SECTION A BLOCK 0	SECTION B BLOCK 0	SECTION B BLOCK 0	A
B	SECTION A BLOCK 2	SECTION A BLOCK 2	SECTION B BLOCK 2	SECTION B BLOCK 2	B
C	SECTION A BLOCK 1	SECTION A BLOCK 1	SECTION B BLOCK 1	SECTION B BLOCK 1	C
D	SECTION A BLOCK 3	SECTION A BLOCK 3	SECTION B BLOCK 3	SECTION B BLOCK 3	D
E	SECTION C BLOCK 0	SECTION C BLOCK 0	SECTION D BLOCK 0	SECTION D BLOCK 0	E
F	SECTION C BLOCK 2	SECTION C BLOCK 2	SECTION D BLOCK 2	SECTION D BLOCK 2	F
G	SECTION C BLOCK 1	SECTION C BLOCK 1	SECTION D BLOCK 1	SECTION D BLOCK 1	G
H	SECTION C BLOCK 3	SECTION C BLOCK 3	SECTION D BLOCK 3	SECTION D BLOCK 3	H

Left IC (2114):

Pin	Signal	Pin	IC pin
2-$\overline{AD}$ 9	15	A_9	
2-$\overline{AD}$ 8	16	A_8	
2-$\overline{AD}$ 7	17	A_7	
2-$\overline{AD}$ 6	1	A_6	
2-$\overline{AD}$ 5	2	A_5	
2-$\overline{AD}$ 4	3	A_4	
2-$\overline{AD}$ 3	4	A_3	I/O_4 11 — DATA 7
2-$\overline{AD}$ 2	7	A_2	I/O_3 12 — DATA 6
2-$\overline{AD}$ 1	6	A_1	I/O_2 13 — DATA 5
2-$\overline{AD}$ 0	5	A_0	I/O_1 14 — DATA 4
2-$\overline{WRITE}$ X	10	$\overline{WE}$	
1-$\overline{SEL}$ Y-Z	8	$\overline{CS}$	

Right IC (2114):

Pin	Signal	Pin	IC pin
2-$\overline{AD}$ 9	15	A_9	
2-$\overline{AD}$ 8	16	A_8	
2-$\overline{AD}$ 7	17	A_7	
2-$\overline{AD}$ 6	1	A_6	
2-$\overline{AD}$ 5	2	A_5	
2-$\overline{AD}$ 4	3	A_4	
2-$\overline{AD}$ 3	4	A_3	I/O_4 11 — DATA 3
2-$\overline{AD}$ 2	7	A_2	I/O_3 12 — DATA 2
2-$\overline{AD}$ 1	6	A_1	I/O_2 13 — DATA 1
2-$\overline{AD}$ 0	5	A_0	I/O_1 14 — DATA 0
2-$\overline{WRITE}$ X	10	$\overline{WE}$	
1-$\overline{SEL}$ Y-Z	8	$\overline{CS}$	

SEL A-0, SEL A-1, SEL A-2, SEL A-3 GO WITH WRITE A
SEL B-0, SEL B-1, SEL B-2, SEL B-3 GO WITH WRITE B
SEL C-0, SEL C-1, SEL C-2, SEL B-3 GO WITH WRITE C
SEL D-0, SEL D-1, SEL D-2, SEL D-3 GO WITH WRITE D