



computer systems

ND812 INSTALLATION
MANUAL

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1. INTRODUCTION

A. GENERAL INFORMATION

The ND812 Installation Manual is a preliminary text intended to serve the user until a full and complete hardware instruction manual is provided. At that time, the contents of this manual will be incorporated as an integral part of the final edition.

B. SPECIFIC INFORMATION

The scope of this installation manual is of necessity limited to providing information which will aid the user initially upon receipt of the ND812 Central Processor. It will cover the installation and interconnections with any of the peripherals ordered with the ND812. It further offers a complete explanation of the usage and functions of the front panel controls and indicators. Also, it provides operational procedures in loading program tapes. The operating instructions for the programs themselves are furnished by their associated software instruction manuals.

2. INSTALLATION

A. UNPACKING AND INSPECTION

Carefully unpack the ND812 Central Processor and ASR33 Teletype, saving the shipping cartons for possible re-shipment. Thoroughly inspect the units for possible damage. Check parts list against associated mounting hardware, instruction manuals and program tapes. If damage is apparent or parts missing, notify your nearest Nuclear Data sales office or the Nuclear Data home office and the discrepancy will be promptly adjusted.

B. VENTILATION

Normal heat generated by the ND812 will not hamper its operation. However, it should not be located over radiators or systems using vacuum tubes since the high ambient heat may affect the operation. Do not place anything over the ventilation fan filters which are located on both sides of the ND812.

C. POWER SOURCE

The ND812 power supply requires a 115/230 Vac, 50/60 Hz source free of excessive noise or fluctuations. A voltage stabilizing transformer can be inserted between the source and the power supply where available power is subject to large fluctuations. Noise produced by various types of electrical equipment can be eliminated or greatly reduced by connecting a suitable filter between the source and the interfering equipment.

D. INTERCONNECTION

The following procedure includes optional equipment interconnection. Disregard devices which are not applicable. Refer to Figure 2-1 for board and connector locations.

- 1) Connect the gray ribbon cable and IC connector originating from the ASR33 Teletype to the IC socket labeled "TTY" on the teletype interface board.

NOTE

The IC connector can be easily reversed in the IC socket. Caution must be taken to assure proper pin correlation.

- 2) Connect the gray ribbon cable and IC connector originating from the high speed reader to the IC socket labeled "READER" on the high speed punch/reader interface board.
- 3) Connect the gray ribbon cable and IC connector originating from the high speed punch to the IC socket labeled "PUNCH" on the high speed punch/reader interface board.
- 4) Connect the multicolored ribbon cable and card edge connector labeled "I/O" to the peripheral (Magnetic Tape, ADC, Disc) that is to be interfaced to the ND812.
- 5) Ascertain that the front panel POWER ON/POWER OFF/CONTROL OFF switch is in the POWER OFF position.
- 6) Connect the line cord to the 115 Vac source.

NOTE

Only the ASR33 Teletype or the Tape Cassette System should be powered through the 115 Vac outlet provided on the rear panel of the ND812.

TURN ON/TURN OFF PROCEDURE

Either the peripherals or the central processor can be turned on first. However, no peripheral should ever be turned on or off while the processor is in the run state.

3. CONTROLS AND INDICATORS

POWER/CONTROL Key Switch

In the POWER OFF position, all primary power is removed from the processor. In the POWER ON position, power is applied to all circuits and manual program control is possible. In the CONTROL OFF position, power is maintained but all front panel switches are disabled, with the exception of the SWITCH REGISTER.

START Switch

When this switch is depressed, the interrupt is disabled, the Overflow bit is set to "0", the flag bit is set to "0", and the processor enters the run state. The contents of the Program Counter is transferred to the Address Register are then used as the address of the first instruction of the program.

LOAD AR Switch

Depressing this switch loads the contents of the Switch Register into the Program Counter and the Address Register and updates the Memory Register to reflect the contents of core at the address contained in the Address Register.

LOAD MR Switch

Depressing this switch loads the contents of the Program Counter into the Address Register, the Switch Register into the Memory Register and initiates a memory cycle which transfers the Memory Register into core at the address in the Address Register. The Program Counter is then incremented by one. In this way it is possible to load consecutive

LOAD MR Switch
(Cont'd)

core locations without continually resetting the address register from the Switch Register.

STOP Switch

Depressing this switch causes the processor to stop at the end of the current instruction.

SINGLE STEP Switch

When this switch is set up, the run mode is terminated and the timing circuits are disabled at the completion of one cycle (step) of the current instruction. Depressing CONTINUE causes the program to advance one additional cycle of the current instruction.

SINGLE INSTRUCTION Switch

When this switch is set up, execution is stopped at the end of a complete instruction. Depressing CONTINUE executes the next instruction in the logical sequence.

NEXT WORD Switch

Depressing this switch sets the contents of the address specified by the Program Counter into the Address Register and the Program Counter is incremented by one. Reloading the Address Register generates a memory cycle which updates the Memory Register to reflect the contents of memory at the address now contained in the Address Register. In this way it is possible to display the contents of consecutive memory locations without continually reloading the Address Register from the Switch Register.

CONTINUE Switch

Depressing this switch begins execution of the program at the address specified by the Program Counter.

SWITCH REGISTER Switches

These switches permit manual loading of a 12-bit word into the registers. Switches in the up position correspond to binary "1's", down to "0's". The contents of the Switch Register is loaded into the Program Counter and Address Register by the LOAD AR Switch, into the memory by the LOAD MR Switch, or into the J Register during program execution with a LJSW instruction.

MEMORY FIELD Switches

These switches determine the Memory Field to be loaded and can be considered as an extension of the Address Register. These switches affect only the "LOAD AR" operation. Each Memory Field is a 4K core memory and are numbered from 0 through 3.

<u>Memory Field</u>	<u>Switch 0</u>	<u>Switch 1</u>
0	0	0
1	0	1
2	1	0
3	1	1

MEMORY FIELD Indicator Lamps

These lamps indicate the Memory Field in which the program is currently being executed.

<u>Memory Field</u>	<u>Lamp 0</u>	<u>Lamp 1</u>
0	off	off
1	off	on
2	on	off
3	on	on

MEMORY REGISTER Indicator Lamps

These lamps indicate the contents of the Memory Register. A lamp "on" indicates a "1" and "off" indicates a "0".

RUN Indicator Lamp

If this lamp is "on", it indicates that a program is being executed.

INTERRUPT Indicator Lamp

If this lamp is "on", it indicates that one of the interrupt levels is enabled.

OVERFLOW INDICATOR Lamp

This lamp is "on" when the overflow bit is set to "1".

SELECTED REGISTER Indicator Lamps

These lamps indicate the contents of the register selected by the SELECT REGISTER Switch.

SELECT REGISTER Switch

This switch selects the register to be displayed on the SELECTED REGISTER Indicator Lamps. Positions S, R, K, and J select the respective registers. Position PC selects the Program Counter, ADDRESS selects the Address

SELECT REGISTER Switch
(Cont'd)

Register, and STATUS selects the circuitry and signals listed below.

<u>Indicator Lamp Number</u>	<u>Logic Circuit Signal Name</u>	<u>Status</u>
∅	FLAG	If this lamp is "on", it indicates that the flag is set.
1	OV	If this lamp is "on", it indicates that the overflow is set.
2	JPSMF∅	These lamps indicate the Memory Field in which the last JPS instruction is located that caused the program to branch to another Memory Field.
3	JPSMF1	

<u>Memory Field</u>	<u>Lamp 2</u>	<u>Lamp 3</u>
∅	off	off
1	off	on
2	on	off
3	on	on

<u>Indicator Lamp Number</u>	<u>Logic Circuit Signal Name</u>	<u>Status</u>
4	INTMF∅	These lamps indicate the Memory Field in which execution was taking place at the time the last interrupt occurred.
5	INTMF1	

<u>Memory Field</u>	<u>Lamp 4</u>	<u>Lamp 5</u>
∅	off	off
1	off	on
2	on	off
3	on	on

<u>Indicator Lamp Number</u>	<u>Logic Circuit Signal Name</u>	<u>Status</u>
6	IONL	If this lamp is "on", it indicates that the lowest level priority interrupt circuitry is enabled.

<u>Indicator Lamp Number</u>	<u>Logic Circuit Signal Name</u>	<u>Status</u>
7	IONB	If this lamp is "on", it indicates that the B level and highest level priority interrupt circuitry is enabled.
8	IONA	If this lamp is "on", it indicates that the A level and highest level priority interrupt circuitry is enabled.
9	IONH	If this lamp is "on", it indicates that the highest level priority interrupt circuitry is enabled.
10	MF0	These lamps indicate the Memory Field in which the program is currently being executed.
11	MF1	

4. BINARY LOADER

A. INTRODUCTION

A Binary Loader is a short program designed to load programs or data in binary format into the processor. The basic loader for this system is the program-controlled or Software Binary Loader. An optional hardware-controlled Binary Loader is also available.

The Software Binary Loader loads binary formatted paper tape or cassette stored program records into any Memory Field of the memory. Each Memory Field consists of 4096 core locations and are defined as: Memory Field 0, core locations 00000_8 through 07777_8 ; Memory Field 1, core locations 10000_8 through 17777_8 ; Memory Field 2, core locations 20000_8 through 27777_8 ; and Memory Field 3, core locations 30000_8 through 37777_8 . (Memory Fields 2 and 3 are optional 12 and 16K memories.) The Software Binary Loader may reside in any Memory Field.

Since the Binary Loader is itself a program, some means must be provided to load it into memory. This is accomplished with a Bootstrap. The Bootstrap is a very short program which is loaded from the Switch Register. When executed, the Bootstrap loads enough of the Binary Loader to allow the Binary Loader to complete loading itself. The Bootstrap is destroyed in the process so that if it is necessary to reload the Binary Loader, the Bootstrap must first be reloaded from the Switch Register.

B. MANUAL LOADING

In loading a program from one of the paper tape readers, the Binary Loader begins by reading leader. Actual loading of the processor begins when the Binary Loader detects the first character different from 0200_8 (eight level punch only). For this reason, it is essential that a program tape be placed in the reader with the leader at the read station. Should the program tape be placed in the reader with blank tape at the read station, the Binary Loader will begin loading zeros into memory beginning with location 0000_8 . Blank tape is not a 200 level and the loader assumes that it must begin loading another program. The actual leader of the program record will be interpreted as trailer.

The loading process consists of assembling consecutive pairs of frames using levels one through six as high and low order halves of 12-bit words. The assembled 12-bit words are stored in the processor in consecutive memory locations, as determined by the presence and interpretation of the origins on the paper tape. Field change characters cause the storage to take place in memory fields specified by the field change characters. When a program record is created, the last two characters are written in such a way as to make the sum of all the 12-bit words (including the last) on the tape equal to zero. The loader keeps a running sum or checksum of the 12-bit words in the record. When the loader detects the trailer, it tests the checksum to determine whether or not the loading process has been correct. If the checksum is zero, the loading process is assumed to be correct and the loader will stop with the J register equal to zero. If the checksum is non-zero, the loading process may be assumed to be in error. In any case, the checksum is left in the J register at the completion of the loading process.

C. AUTO-START

There are three alternative methods of using the Binary Loader. In all cases, the format of the record being loaded remains the same. The differences lie in the manner of entering the Binary Loader and exiting once the loading process has been completed. In all three of the cases to be described, location 7751_g contains the exit address. That is, instead of stopping when the loading process is complete, the Binary Loader performs a jump to the address contained in location 7751_g, provided the contents of location 7751_g is not zero. This feature will be described as the Auto-start feature of the Binary Loader.

Manual load with Auto-start is the simplest use of the Auto-start feature of the Binary Loader. The program record being loaded includes the necessary coding to cause location 7751_g to be set equal to some non-zero address. When the Binary Loader completes the loading process, it will jump to this address with the checksum, (normally zero), in the J register and the exit address in the K register. The exit address should be the starting address of the program being loaded. The program making use of the Auto-start feature should check the J register to determine if the loading process was correct and take appropriate action should the J register be non-zero.

Second use of the Auto-start involves performing a JPS to the Binary Loader from a program outside the Binary Loader. The JPS is performed to location 7751_g. When the loading process is completed the Binary Loader will return to the calling location plus one with the checksum in the J register, as though the Binary Loader were a subroutine. The program being loaded must not alter location 7751_g. When entering the Binary Loader in this fashion, it is necessary that the status word, which is normally loaded from the switch register, be loaded in the J register by the calling program before the JPS to the Binary Loader is executed.

The third method of using the Auto-start feature is very similar to the second method but rather than a JPS, the calling program performs a JMP to location 7752_g. Again, the status word must have been loaded into the J register by the calling program. It is necessary that the calling program either set location 7751_g to zero, thereby causing the

Binary Loader to stop at the end of the loading process (provided the program being loaded does not alter the location 7751g) or the calling program should set an appropriate exit address into location 7751g.

D. OPERATOR OR USER CONTROL

The status word is the only control the user has over the loader. The bits of the status word are interpreted by the loader as follows: BITS 0 and 1 determine the input device; BITS 2, 3 and 4 determine the input cassette drive if a cassette is to be selected; and BITS 5 through 11 indicate the tagword when loading from magnetic tape cassette. Each one of these three functions is described in detail below.

Input Device Selection	BITS 0 and 1 determine the device from which the record is to be read. If BIT 1 is "0", input is from cassette and BIT 0 is ignored. If BIT 1 is "1", input is from one of the paper tape readers as controlled by BIT "0". When BIT 0 is "0", the input is from the high speed reader and if BIT 0 is "1", the input is from the low speed or teletype reader.
Cassette Drive Selection	BITS 2, 3 and 4 permit the user to select one of the three cassette drives for input. No two of these bits should be on together as the loader will try to read from two or more drives simultaneously. BIT 2 set to "1" selects drive three, BIT 3 selects drive two, and BIT 4 selects drive one.
Tagword Selection	Any tagword from 0000g to 0177g may be selected by BITS 5 through 11. Capacity to select a tagword allows the user to select at random one of many records on a particular cassette without the need to hunt manually for the record in question. Starting with the beginning of the cassette, the Binary Loader will search for the correct tagword by reading the first character of each program record on the tape.

NOTE

Entering the Binary Loader under software control demands that the J register be set to the desired status word by the software performing the call to the Binary Loader (as described above).

E. OPERATIONAL PROCEDURE

1. Bootstrap

The following is the procedure by which the Bootstrap is loaded in the ND812.

- 1) Place the POWER ON/POWER OFF/CONTROL OFF switch in the POWER ON position.
- 2) Set the Switch Register to 7762_g and depress LOAD AR.
- 3) It is now necessary to load fourteen instructions from the Switch Register, each of which is followed by depressing the LOAD MR key.

ADDRESS	INSTRUCTION	ADDRESS	INSTRUCTION
7762	7404	7771	7404
7763	6101	7772	6101
7764	7403	7773	7403
7765	1146	7774	1122
7766	1501	7775	5700
7767	6105	7776	6114
7770	1101	7777	7745

- 4) To check if the instructions were stored in the proper locations, set the Switch Register to 7762_g and depress LOAD AR. Place the SELECT REGISTER switch in the ADDRESS position. Depressing the NEXT WORD key causes the SELECTED REGISTER indicator lamps to display the contents of the address. Continue to depress the NEXT WORD key until all instructions have been checked.
- 5) Set the Switch Register to 7773_g and depress LOAD AR.
- 6) Place the paper tape of the ND41-0005 Binary Loader on the low speed reader, turn teletype to LINE and reader ON.
- 7) Depress START.

The paper tape is read and will stop on reaching trailer. If the J register is zero after reading the paper tape, no errors occurred. Repeat the above from Step 2 if J register is non-zero.

The Binary Loader is now in memory and is used to load program records from either paper tape or cassette.

2. Low Speed Paper Tape

- 1) Set the Switch Register to 7700_g and depress LOAD AR.
- 2) Place the binary formatted program tape to be read into the ASR33 Reader with the leader at the read station.

- 3) Place the START/STOP switch on the ASR33 Reader to START.
- 4) Set Switch Register BITS 1 and 2 to "1".
- 5) Depress START.
- 6) The Binary Loader will read the program tape and stop at trailer. If the content of the J register is zero at completion of the loading process, the program tape was loaded correctly. If the J register is non-zero, re-start this operational procedure from Step 2.

3. High Speed Paper Tape

- 1) Set the Switch Register to $77\emptyset\emptyset_8$ and depress LOAD AR.
- 2) Place the binary formatted program tape to be read on the high speed reader with the leader at the read station.
- 3) Set Switch Register BIT \emptyset to " \emptyset " and BIT 1 to "1".
- 4) Depress START.
- 5) The Binary Loader will read the program tape and stop at trailer. If the content of the J register is zero at completion of the loading process, the program tape was loaded correctly. If the J register is non-zero, re-start this operational procedure from Step 2.

4. Magnetic Tape Cassette

- 1) Set the Switch Register to $77\emptyset\emptyset_8$ and depress LOAD AR.
- 2) Set Switch Register BITS \emptyset and 1 to " \emptyset ", set BITS 2, 3 and 4 for the desired cassette drive, set BITS 5 through 11 to desired tagword.
- 3) Depress START.
- 4) The Binary Loader will read from the cassette and conduct a tagowrd search. When the tagged record is reached, the Binary Loader will read the record and stop at completion. If the content of the J register is zero, the loading process was correct. If the content of the J register is non-zero, restart from Step 2 of this procedure.

NOTE

If the Binary Loader proceeds to the end of tape without stopping, the user has specified a tagword which does not exist on the cassette. To recover from this condition, depress STOP, rewind the cassette, and re-start from Step 1 after ascertaining that the tagword specified exists on the cassette.

F. ERROR DIAGNOSTICS

The checksum is stored in the J register at the completion of either a manual or software controlled program loading procedure. A non-zero J register indicates an erroneous load. Refer to the appropriate section of the OPERATIONAL PROCEDURE and re-load the program. If an error is encountered under software control, check the calling program and the exit address of the Binary Loader.

If a non-existent input device is specified, the Binary Loader will enter an endless loop. The processor must be stopped with the front panel STOP switch and the loader re-started.

Failure to load a tape with leader over the read station will cause the loader to stop on reaching the program's leader. The J register will be zero, but since the program was not read, it will not be loaded. The user is particularly warned against placing blank tape at the read station when loading overlays, as part of the background program is likely to be lost when the loader tries to load the blank tape.

G. STATUS WORD SUMMARY

INPUT DEVICE	BIT 0	BIT 1	
Cassette	0	0	
High Speed Paper Tape Reader	0	1	
Low Speed Paper Tape Reader (ASR33)	1	1	
CASSETTE DRIVE	BIT 2	BIT 3	BIT 4
DRIVE 1	0	0	1
DRIVE 2	0	1	0
DRIVE 3	1	0	0

BITS 5 through 11 are used to specify the tagword.

H. HARDWARE LOADER

The Hardware Loader is a hard wired binary loader that allows the loading of binary formatted paper tapes with a minimum of manual control selections. The following is the Hardware Loader procedure:

- 1) Place paper tape in reader and turn reader on.
- 2) Simultaneously depress both the LOAD ADDRESS and NEXT WORD switches.

The paper tape is read-in and will halt on trailer.

NOTE

The Hardware Loader can be used to load binary formatted paper tapes in a single Memory Field. If a more sophisticated loader is needed, the hardware loader may be used to load a binary formatted paper tape of one of the software loaders.

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