Pin	Designation	Description	Pin	Designation	Description
2	GND	System Power and Logic Ground	1	+5	Positive 5 volts Power Supply
4	GND	System Power and Logic Ground	3	+5	Positive 5 volts Power Supply
6	GND	System Power and Logic Ground	5	+5	Positive 5 volts Power Supply
8	GND	System i ower and Logic Ground	7	MA0	1 Ositive 3 voits I owel Supply
				CAS	
10			9		
12	GWAIT		11	MA6 MA5	
14 16		Foot Curitob	13		
16	FAST	Fast Switch	15 17	MA4	
18	SB_RFSH	Shared Bus Dynamic RAM Refresh	17	MA3	
20	0000		19	MA2	
22	OSCS		21	MA1	O
24	RAMK1L	Observat Bura Mashina Ossarda Ossala	23	CLK	Current Clock 1.789 mHz or 2.4576 mHz
26	SB_M1	Shared Bus Machine Opcode Cycle	25	IRESET	IceBox Reset
28	GRESET	Game Reset	27	SB_A3	Shared Bus Address Bit 3
30	DBEN	Game Microcycle Data Bus Disable (BUZOFF)	29	SB_A4	Shared Bus Address Bit 4
32	???	This is connected to pin 6 of U1 on Backplane	31	SB_A2	Shared Bus Address Bit 2
34	ZWAIT		33	SB_A1	Shared Bus Address Bit 1
36	NMI		35	SB_A0	Shared Bus Address Bit 0
38	GRESETL	Game Reset Switch	37	IRESETL	IceBox Reset Switch and Power On Reset
40	WP		39	ADDSHT	Address Shift to \$Fxxx for Boot Rom
42	SEL0	Select Floppy Drive 0	41	SB_A11	Shared Bus Address Bit 11
44	SEL1	Select Floppy Drive 1	43	SB_A10	Shared Bus Address Bit 10
46	IREN	Floppy Drive Read Enable	45	ĪWEN	Floppy Drive Write Enable
48	BUSREQ		47	WS	
50	BUSACK		49	SB_IORQ	Shared Bus Input / Output Request
52	ICLK	IceBox Clock 2.4576 mHz	51	BRK	Break
54	OSEN		53		
56	GCLK	Game (Device) Clock 1.789 mHz	55		
58	7M		57		
60	EXT	External Clock Switch	59		
62	SB_HALT		61	SB_A15	Shared Bus Address Bit 15
64	ĪNT		63		
66	BUZOFF		65	SB_A14	Shared Bus Address Bit 14
68	SB_D3	Shared Bus Data Bit 3	67		
70	SB_D1	Shared Bus Data Bit 1	69	SB_WR	Shared Bus Write
72	SB_D6	Shared Bus Data Bit 6	71		
74	SB_D4	Shared Bus Data Bit 4	73		
76	RFSHCARD		75	BUZOFF	
78	SB_A12	Shared Bus Address Bit 12	77	SB_D7	Shared Bus Data Bit 7
80	SB_A13	Shared Bus Address Bit 13	79	SB_D5	Shared Bus Data Bit 5
82	SB_RD	Shared Bus Read	81	SB_D0	Shared Bus Data Bit 0
84	SB_MREQ	Shared Bus Memory Request	83	SB_D2	Shared Bus Data Bit 2
86			85	SB_A9	Shared Bus Address Bit 9
88	SB_A5	Shared Bus Address Bit 5	87	SB_A8	Shared Bus Address Bit 8
90	SB_A7	Shared Bus Address Bit 7	89	SB_A6	Shared Bus Address Bit 6
92	RxDSP	Receive Data Serial Printer	91	TxDCRT	Transmit Data CRT Terminal
94	TxDSP	Transmit Data Serial Printer	93	CARD3	RAM Bank 3 Select
96	CTSSP	Clear To Send Serial Printer	95	CARD2	RAM Bank 2 Select
98	RTSSP	Request To Send Serial Printer	97	CARD1	RAM Bank 1 Select
100	DSRSP	Data Set Ready Serial Printer	99	CARD0	RAM Bank 0 Select
102	RAMDIS		101	RxDCRT	Receive Data CRT Terminal
104	DTRSP	Data Terminal Ready Serial Printer	103	IDRQ	
106	TxCSP	Transmit Clock Serial Printer	105	INTR	
108	+15V	Positive 15 volt Power Supply	107		
110	+15V	Positive 15 volt Power Supply	109		
112	+15V	Positive 15 volt Power Supply	111		
114		•	113	-5V	Negative 5 volt Power Supply
116	KEY		115	KEY	• • •
118	GND	System Power and Logic Ground	117	+5V	Positive 5 volt Power Supply
120	GND	System Power and Logic Ground	119	+5V	Positive 5 volt Power Supply
122	GND	System Power and Logic Ground	121	+5V	Positive 5 volt Power Supply
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