DIGITAL COMPUTER NEWSLETTER

The purpose of this newsletter is to provide a medium for the interchange among interested persons of information concerning recent developments in various digital computer projects. Distribution is limited to government agencies, contractors, and contributors.

OFFICE OF NAVAL RESEARCH • MATHEMATICAL SCIENCES DIVISION

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Jean S. Campbell, Asst. Editor

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NAVEXOS P-645

COMPUTERS AND DATA PROCESSORS, NORTH AMERICA

MERLIN COMPUTER - BROOKHAVEN NATIONAL LABORATORY - UPTON, L. I., NEW YORK

Merlin is a high-speed digital computer being constructed at Brookhaven National Laboratory. It is similar in concept to the Maniac II now in operation at Los Alamos and is intended to provide, on a limited budget, speeds and capacities competitive with presently available computers.

Initially the electrostatic memory of Merlin will hold 12,288 random access, self-checking 48 bit words, with an access time of 8 microseconds; however, provision is being made for addressing over 64,000 words. (Construction of Merlin began in late 1956 at which time the cost of magnetic cores offset their obvious advantages in terms of speed and reliability. Recent developments in the design and manufacture of electrostatic storage tubes indicates their use at a density of 6,000 bits per tube within acceptable tolerances.) It will operate in fixed or floating points with the number representation $N = 2^{8y}x$ with 41 bits for x, including sign, and 5 bits for y, including sign. The remaining two bits of a number may be used as tags or markers which may be detected either programwise or automatically by the computer.

In addition to three shifting registers which are essential for arithmetic operations, the arithmetic unit of Merlin will contain four non-shifting registers which will be used as fast access temporary storage. The basic add time will be 3 microseconds, with a shift time of 1 microsecond per stage or 1 microsecond per simultaneous 8 stage shift. The computer operates asynchronously and an average floating add time of 7 microseconds and an average multiply time of 90 microseconds are expected.

A Merlin word will hold one instruction which may contain one or two memory addresses, and up to three addresses if the fast access registers are involved. The fetching of an instruction is performed during the execution of the previous instruction in order to minimize the access time involved. Automatic address modification by means of six index registers has been provided and, following the design of MANIAC II, a separate register has been provided to hold the contents of the control counter upon transfer.

It was felt that Merlin, as a research tool, should have flexible provisions for manual interventions, and easy manual access to the various parts of the machine is provided.

Input to Merlin is achieved via paper tape, magnetic tape, and a typewriter. Output is via paper tape, magnetic tape, the typewriter, and a 600 lines per minute on-line printer. Provisions have been made for incorporating up to sixteen magnetic tape units.

Viewed from an engineering standpoint, Merlin is unique. As a transitional machine, bridging the gap between the Thermionic and Solid State Eras, it utilizes vacuum tubes, crystal diodes, and transistors. The Arithmetic and Control Sections are largely tube operated; the memory presents an interesting amalgam of tubes and transistors.

The approximately 8,000 tubes and transistors, along with their associated circuitry, are contained in 31 free standing racks distributed over a floor space of 150 square feet. Throughout the design, emphasis is placed on accessibility and ease of maintenance. The input-output equipment, power supplies, and cooling system occupy an additional 600 square feet.

HONEYWELL 800 - DATAMATIC DIV. - NEWTON HIGHLANDS, MASSACHUSETTS

The Honeywell 800 is a transistorized medium-scale data processing system which is medium-scale in size and price only. Its magnetic tape speeds and internal operating speeds are faster than those of any other medium-scale system. For business applications, it has the ability to perform decimal arithmetic. For scientific applications it can perform binary arithmetic, either fixed-point or floating-point. An exclusive feature called Automatic Parallel Processing gives the ability to perform several independent programs simultaneously. Thus, in addition to being equally adaptable to scientific and business applications, it can do both types of jobs simultaneously. As many as eight programs may be processed in parallel. No special programming is necessary and individual programs may be started and stopped independently.

The 800 incorporates complete checking from input through output and includes Orthotronic Control, exclusive Honeywell technique for instantaneous correction of lost or garbled information.

A powerful three-address order structure conserves time and memory capacity and facilitates programming. A full complement of automatic programming and library routines will be available to every user.

Parallel Processing is a breakthrough that exacts maximum efficiency from all units of the system. It is a combination of two engineering achievements called Traffic Control and Multi-program Control.

Traffic Control is a device which monitors all peripheral activities of the system, including magnetic tapes and the console, and provides the proper channel connections at the proper time between these devices and the central processor. As many as eight input and eight output channels may be active simultaneously.

Multi-program Control coordinates the demands of up to eight completely independent programs running in parallel.

The internal operating speed is 30,000 three-address operations per second. This is equivalent to 40,000 two-address or 60,000 single-address operations per second. A series of numbers can be accumulated at a rate of 125,000 per second.

Core storage is available in modules of 4,096 words and one, two, three, or four modules may be employed. Each word of core storage is individually addressable. Parallel transmission is employed in sending words to and from core storage. An entire word can be sent to or from the memory in six microseconds. The memory is the basic storage unit for both data and instructions. High-speed random-access drum storage is available as optional equipment.

The word consists of 54 bits, of which six are used for checking. The 48 information bits may represent an 11-decimal-digit number with its sign, several smaller decimal numbers, with signs for each, eight alphabetic characters, or a combination of these. A word may also be interpreted as a 44-bit binary number with its sign, or as an instruction. Using the floating-point option, a word may represent a sign bit, a seven-bit exponent, and a 40-bit mantissa in binary form.

In the instruction word, the information bits are divided logically into four sections which are interpreted as an operation code followed by three addresses.

Each address in an instruction may be designated as absolute or indexed. A total of eight index registers are available to each program.

The ability to mask words allows most internal processing instructions to work with fields of variable length. Each program may designate a group of 32 memory locations as masking registers. Such a designation may be changed by the programmer at any point in his program. Thus, an essentially unlimited number of masking registers is at his disposal.

THE NBS MULTI-COMPUTER SYSTEM - NATIONAL BUREAU OF STANDARDS - WASHINGTON, D. C.

At the National Bureau of Standards a new digital data processor has been designed as a flexible pilot facility for exploring complex processing, information retrieval, and control problems of importance to the Government. Because the system is intended for research on such a wide range of applications — ranging from automatic searching and interpreting of information records to real-time scheduling and control of commercial aircraft traffic — it is characterized by a variety of features not ordinarily associated with a single installation. It has not only a high computation rate and a wide repertoire of internal processing operations but also very flexible and powerful control capabilities for communicating with human operators and with devices external to the system.

The over-all system, devised by A. L. Leiner, W. A. Notz, J. L. Smith, and A. Weinberger of the Data Processing Systems Division, is an integrated network of three independently programmed computers, each of which is specially adapted for performing certain particular classes of mathematical or logical operations. All three computers operate concurrently and intercommunicate with each other in a way that permits them to work together collaboratively on the solution of problems being tackled by the system. The primary computer, a high-speed general-purpose computer, carries out most of the high-precision arithmetic calculations and logical processing operations. The smaller secondary computer acts as its partner, keeping track of various parts of the program and carrying out short-word operations, usually manipulations on address numbers or other "red-tape" information, which it supplies automatically as needed to the primary computer. Each of these computers utilizes only 16 basic instructions, thus providing a simple code structure. However, because many variations of the formats are provided, a wide variety of operations can be performed with these few instructions. Both computers, acting cooperatively, can carry out special complex sorting or search operations.

The third computer has charge of information flowing into or out of the system. This computer may be supplied with information about the anticipated needs of the primary computer for external data and can then search the external storage or input-output devices, convert the data in these devices to the proper form for internal use, and feed it into the primary computer at the right instant. All three computers as well as all the external units share access privileges to the common high-speed internal memory, which is linked to the input-output and external storage units via independent trunks for effecting data-transfers. The system can accommodate up to 16 such input-output trunks along which data can flow concurrently, though only two trunks are planned for the initial installation of the system. Using two such trunks, it is possible to maintain two continuous streams of data, flowing simultaneously between any two external units and the internal memory, without interrupting the data processing program.

The system can operate with a wide variety of input-output devices, both digital and analog, either proximate or remotely located. The external control capabilities of the system enable it to supervise this wide family of external devices and, on an unscheduled basis, to interrupt or redirect its over-all program automatically in order to assist or manage them. Such impromptu interchanges of information between the system and the devices or people external to it can occur at the instigation of either the external world or the internal system, or both acting jointly. Automatic controls regulate all the interplay among the different parts of the system and guard against the possibility of internal traffic jams.

The system will run more than 100 times faster than SEAC on most types of programs, and more than 1,000 times as fast on some programs.

AIRBORNE COMPUTERS - NORTRONICS - HAWTHORNE, CALIFORNIA

Nortronics, Division of Northrop Corporation, presently has in production a fully transistorized airborne digital computer (APAC) which has been fully flight tested and environmentally qualified. It has been operational in both manned and unmanned aircraft since November 1957 and has accumulated some 200 hours of successful airborne operation. This device is a medium speed D.D.A. consisting of 375 germanium transistors and 1200 germanium diodes. Input is from punched paper tape. D. C. power supplies are an integral part of the computer module, deriving the required D. C. voltages from 115 volt, 400 cycle primary power source. All circuitry is constructed on removable etched circuit boards of which a total of 20 are utilized. The memory device used is a non-contact drum consisting of 5 channels. The complete computer weighs 100 pounds; its volume is 2 cubic feet and requires 132 watts of 115 volt, 400 cycle single phase power.

Nortronics also has under development an airborne digital computing system which is designed to perform the computation function for the Lightweight Inertial Navigation System (LINS). This computing system combines the advantages of integral and incremental computer techniques in an integrated digital system. Computations for sensor quantizing, navigation, gyro control, inertial instrument erection, and pilot's display of present position, range to target and heading to target are performed within the digital system.

The complete computing system, including input-output equipment, weighs 50.7 pounds and occupies a volume of 1.3 cubic feet. Designed for a severe airborne environment the system is presently in the assembly stage and is scheduled for completion during the summer of 1959.

The division has also recently completed programming of the IBM 704 computer for a multi-stage decision process. The operation, which formerly was carried out manually and with a small general purpose computer taking 2-1/2 hours, now requires less than 20 seconds.

Nortronics is also presently developing a computer for an advanced guidance system application.

TRANSAC S-2000 - PHILCO CORP. - PHILADELPHIA, PENNSYLVANIA

Installation of the first TRANSAC S-2000 Electronic Data Processing System was made in November 1958 at the Western Development Laboratory, Palo Alto, California — a Philco subsidiary. Application of the TRANSAC (Transistorized Automatic Computer) at WDL is primarily for data reduction. The second system will be installed in Philco's Corporate Division, Philadelphia, Pennsylvania. This system will be applied to Philco's commercial data processing.

Although Philco has not made its TRANSAC commitments public, the Naval Supply Center, Oakland, California has announced its intention to install the system.

Highlights of the TRANSAC S-2000 (see Digital Computer Newsletter April 1957):

Mode	Parallel.
Core Memory	4096 - 32,768 words (48 bits).
Magnetic Tape Speed	90,000 alphanumeric characters or 168,000 decimal digits per second.
Punched Cards	2,000 cards per minute read.
High Speed Printing	900 lines per minute.
Paper Tape	1,000 characters per second read.
Simultaneous Operations	Provision is made for the simultaneous operation of up to nine input/output devices, including four magnetic tape units. Of the total, up to five may be communicating with the central computer concurrent with processing.

A unique feature, the Universal Buffer Controller, provides common buffer storage and control for off-line data conversions, and on-line punched card and printer operations. In so doing, the Universal Buffer Controller reduces the number of magnetic tape, punched card, high speed printer and buffer storage units necessary in a system. The Universal Buffer Controller also allows for the simultaneous operations described above. There may be four Universal Buffer Controllers on-line and each can accommodate two tape units and up to five punched card and high speed printer units. The character transfer rate between the central computer and a buffer controller is 90,000 alphanumeric characters per second.

COMPUTING CENTERS

COMPUTING CENTER - FRANKLIN INSTITUTE - PHILADELPHIA, PENNSYLVANIA

In January 1959 The Franklin Institute Computing Center started its third year of operation. The basic equipment—a Univac I System acquired from the Sperry Rand Corporation through a lease purchase arrangement—is maintained by their own engineering staff. The Mathematics Analysis Section, formerly a division of the Laboratories for Research and Development but now an integrated part of the Computing Center, provides analysis and programming services as required.

In all respects, the second year of operation was highly successful. Machine performance and production scheduling exceeded expectation, and in the field of technical and systems research, progress was most satisfactory. Much of the data processing scheduled on the machine during 1958 was handled on a sub-contract basis. The Institute itself is a non-profit organization primarily noted for research and development in the "mechanical arts and sciences." Consequently, the majority of service bureau jobs directly contracted for by the Center were of a mathematical or engineering nature. Many involved Institute personnel additionally qualified as experts in fields other than computing.

During 1959 the Institute will continue to provide machine time and personnel for back-up facilities, research, one-shot, and repetitive data processing jobs of whatever nature required by our users. They also hope to serve as a means of introduction to computers for those industries or organizations which while interested in electronic data processing have for one reason or another delayed their entry into the field. The Institute is more than a little disturbed by the increasingly critical content of many articles dealing with the concept of large or medium scale computing systems currently evident in a number of national periodicals, management, and consulting publications. While such publicity is embarrassing to the industry as a whole, its effect is particularly evident among the less experienced or potential users of the type normally contacted by a service organization such as The Franklin Institute. Through judicious application of the large and comprehensive library of "canned" routines and the proven record of reliability established by Univac I, it is hoped to convincingly demonstrate that industry of modest size and endowment can economically convert chosen segments of its operation to electronic means. It is the Institute's belief that demonstration of the feasibility of this approach, devoid of high initial installation, rental, and personnel costs, is one of the simplest and most effective rebuttals to the skepticism being generated by the currently "fashionable" practice of singling out one or two poorly managed or unsuccessful installations and concluding through broad, sometimes irresponsible generalizations that computers in their present stage of development are little more than expensive playthings for government agencies and a handful of giant corporations.

One such "canned" routine, successfully utilized during 1958 and to be emphasized throughout 1959, is an economic time series analysis (Seasonal Adjustments by Electronic Computer Methods). A preliminary seminar for area businessmen revealed much interest and a real need for the type of information available through use of this routine. Surprisingly enough, several of the firms contracting for this service had computing facilities of their own but had never considered this particular area of application. Others, new to the use of computers, were favorably impressed by the economy and ready availability of the routine.

Another routine (Big Ben - 25) for solving systems of linear algebraic equations up to and including order 25, has been in constant use since its development by the staff. In many cases solutions are delivered on the same day the input data are received at the Center. With respect to this and many similar routines, it may be safely said that the facilities of the Center are no further away from the area engineer or mathematician than the phone at his elbow.

RICH ELECTRONIC COMPUTER CENTER - GEORGIA INSTITUTE OF TECHNOLOGY - ATLANTA, GEORGIA

The Computer Center has added a Burroughs 220 digital computer to its existing facility of a Univac Scientific (ERA 1101) and an IBM 650. The system includes 5000 (10 decimal digit) words of core storage, a high speed 1000 character per second photo-electric paper tape reader, paper tape punch, a Cardatron system of one card collator (089) input and one output unit controlling either a line printer (407) or a card punch (523). This complement of equipment is undergoing tests and will be further tested with four additional magnetic tape reel units to be delivered shortly. The 220 will enable the Center to expand its research and educational activities. This computer has built-in floating point operations as well as effective data processing abilities.

The addition of a 4,096 core storage unit to the Univac Scientific is nearing completion. This will supplement the 16,384 word (24 bits) drum memory and provides a computing speed of within 20 percent of the 1103A. All design modifications were planned and done by the Center's staff.

The compiler Fortran is being adapted to the 1101 by the Center and is expected to be available for the 220 as well. It is now used on the IBM 650 through Fortransit. This will make three different computers available through a common language to a user within certain limitations.

COMPUTATION LABORATORY - NATIONAL BUREAU OF STANDARDS - WASHINGTON, D. C.

During January the IBM 704 was equipped with half-word logic. This makes the machine identical to that operated by the Weather Bureau. The Bureau of Standards machine is to be used as a stand-in for the Weather Bureau machine, both for overflow work and to avoid delays in regular weather prediction services in case of temporary machine breakdown.

Early in May a 32,000-word magnetic core memory will be installed, while the 8000-word auxiliary magnetic drum memory will be retained. The machine will continue to be available to agencies and contractors of the Federal Government. After installation of the larger memory it is expected that the hourly cost of machine time will be $215.

AEC COMPUTING AND APPLIED MATHEMATICS CENTER - NEW YORK UNIVERSITY - NEW YORK, N. Y.

Through the offices of the U. S. Atomic Energy Commission a committee has been selected to evaluate requests for the use of computing machines at the AEC Computing and Applied Mathematics Center of N. Y. U. Only proposals coming from non-profit institutions can be considered. The Physical Sciences and Mathematics are the areas for which computing may be approved subject to the availability of time on the Univac and the IBM 704. At present the Univac is much more readily available than is the 704. Interested parties should write for further information to: Eugene Isaacson, AEC Computing and Applied Mathematics Center, New York University, 4 Washington Place, New York 3, New York.

RESEARCH COMPUTATION CENTER - THE UNIVERSITY OF NORTH CAROLINA - CHAPEL HILL, N. C.

In May 1959, the Consolidated University of North Carolina will install a new Univac Scientific ERA-1105 Digital Computer in the new Physics and Mathematics Building now being built at Chapel Hill. Purchase of this machine was made possible through the support and cooperation of the Sperry-Rand Corporation, The Bureau of Census, and the National Science Foundation.

Although the computer itself is located on the campus in Chapel Hill, it will be used by students and faculty of the North Carolina State College in Raleigh and the Woman's College of the University of North Carolina as well. Plans are underway to make time available on a cooperative basis to other nearby institutions, both in North Carolina and the Southeastern United States.

In addition to serving as a teaching and research aid in present university areas, it is planned to use the computer as a research tool in such frontier areas as language translation, automatic programming, automatic numerical analysis, business, statistical and other data processing, linguistics analysis, numerical solution of partial differential equations, mathematical logic and decision processes, and many other regions of investigation that have become important only since the advent of the high-speed digital computer.

New courses in high-speed computation, both credit and non-credit, for graduates and undergraduates, are to be given or are under consideration. Special opportunities will be available for graduate students to work as programmer-analysts in the new Computation Center, either as research assistants or supported by graduate fellowships. Undergraduates will have opportunities to serve in part-time jobs as computer operators or as data preparation specialists.

In February of this year Dr. John W. Carr, III, formerly Associate Professor of Mathematics at the University of Michigan and formerly President of the Association for Computing Machinery, assumed the post of Director of the Computation Center and Associate Professor of Mathematics at the University.

A particular effort is being made to make research assistantships available to programmers now working in computer installations who are interested in returning to a University as candidates for the Ph.D. degree in computer-oriented areas. Assistantships also are planned that will allow a student to work as a liaison programmer between his particular University department and the Computation Center.

The first of a series of Conferences on Frontier Research in Digital Computers is being planned for August 17-28 of this year, with lecturers from the United States and overseas scheduled to participate.

The Univac ERA-1105 computer, which is on order, has floating-point operations, over 12,000 words of magnetic core storage, over 32,000 words of directly operable magnetic drum storage, 17 Uniservo magnetic tape units, punched card and paper tape input-output, and a high-speed printer. Complete buffering allows independent operation of the main computer unit and the magnetic tapes. Similar machines will be in use at the Bureau of Census, various Air Material Command installations, and Armour Research Foundation.

MATHEMATICS DEPARTMENT - U. S. NAVAL ORDNANCE LABORATORY, WHITE OAK - SILVER SPRING, MARYLAND

On 2 February 1959 an IBM 704 was installed at the Naval Ordnance Laboratory. The computer is equipped with a 32,768 word memory, eight tape units, a card reader, a card punch, a printer, and a cathode ray tube display and recorder. Off line equipment includes a printer and a card-to-tape converter. Present plans call for the 704 to be operated on a single shift basis. At the present time it is being used for scientific computations and data reduction problems.

NAVAL ORDNANCE COMPUTATION CENTER - U. S. NAVAL PROVING GROUND - DAHLGREN, VIRGINIA

The UDT (Universal Data Transcriber), designed and built at the Naval Proving Ground to enable interchange of NORC input and output with a variety of digital media, is now undergoing systems checkout.

The high speed Charactron microfilm printer built by Stromberg Carlson for attachment to NORC passed its reliability acceptance test in February during which 11,000 frames were recorded with only one error, that error being detected by printer check circuits. The printer had been undergoing debugging and intermittent use since delivery in April 1958.

During 1958, the NORC was staffed 6520 hours, of which 5194 hours were scheduled for computing and 4868 hours of good computing time were realized. Losses during the scheduled time were caused by:

Arithmetic and Control	2.1% of scheduled time
Tape system	1.9
CRT memory	1.2
Printers (mechanical)	.7
Power supplies	.4
	6.3%

COMPUTERS AND CENTERS, OVERSEAS

NATIONAL-ELLIOTT 802 - ELLIOTT BROTHERS LTD. - LONDON, ENGLAND

The order code for the National-Elliott 802 (see Digital Computer Newsletter, January 1959) was evolved as a result both of long experience with various types of computers, and of close collaboration between engineers and programmers. It is extremely simple, yet contains a large variety of orders. Careful logical design has ensured that there are no exceptions to the rules. The functions are numbered in a logical way that is learned very rapidly with no conscious effort on the part of the programmer. Each order refers implicitly to the single accumulator, and to one store address. The comprehensive order code provides a set of 64 different instructions.

Orders are of the single address type, with two orders per word. There is an extra digit in each word which is used for automatic modification of orders (B-modification). By means of this digit any location in the store may be used as a B-line. A B-lined order takes no longer to obey than the same order without a B-line. The ability to modify their own orders is one of the features that make automatic computers so powerful. In previous computers, facilities for doing this automatically have been limited to a few registers, often less than eight. The 1024 B-registers in the 802 give the user tremendous advantages by simplifying the programming of extremely complex problems.

Reliability is achieved by careful electronic design and by the use of solid state devices. The store consists of a matrix of magnetic cores. Cores are also used, in conjunction with transistors, to form the basic logical elements in the machine. By these means long periods of trouble-free operations are ensured. The basic logical elements, which are completely standard, consist only of a magnetic core, a resistor and a transistor, with printed-circuit connections. These units are themselves mounted on printed-circuit plug-in boards. The printed-circuit techniques further increase reliability and the system of plug-in units, pioneered by Elliott Brothers, makes maintenance very simple.

Only three keys are used to control the operation of the machine. This extreme simplicity virtually eliminates the possibility of error due to incorrect manual operation of the controls. A loudspeaker indicates the machine is calculating and produces a sequence of tones according to the instructions being obeyed.

A comprehensive library of subroutines is provided with the machine. This minimizes the programming required for the solution of any special problem.

The dimensions of the basic computer are little greater than those of a desk and it can be used in a normal room. Weight is low, no special ventilation or temperature control is necessary. The 802 can be installed in the most convenient location for ease of access by office, laboratory, or control room staff.

The computer is a stored program machine which operates from a single level very fast access store. This means that all the instructions and data are available immediately, wherever they are situated in the store. Thus minimum access coding is not required, and the computer is always operating at its full speed. No time is wasted in transferring information from a backing store to the working store since the computer has such a large rapid access memory.

Construction	The computer consists of an assembly of individually-ventilated steel cabinets, with an attractive grey hammer finish and of convenient desk-height. These cabinets contain the logical units on plug-in boards, the core store, stabilized power supplies and the built-in control console.
Input	By 5-hole punched paper tape at speeds up to 170 characters per second.
Output	By 5-hole punched paper tape, punched at approximately 25 characters per second and subsequently interpreted at 10 characters per second.
Optional Input and Output	Punched card reader, manual keyboard input, analogue and digital recording mechanisms, additional tape readers and punch. Special devices designed to customers' requirements can be provided.
Storage	Magnetic core store, capacity 1020 words of 33 binary digits each, plus 4 words of fixed orders. Access time (negligible) included in operating speeds.
Arithmetic Unit	Digit rate: 166,500 per second. Notation & arithmetic mode: Binary, Serial. Word Length: 33 binary digits.
Order Code	Single address, two orders per word.
B Modification	Any location in the store may be used as a B-modifier. When the B digit is present the contents of Address 1 are added to the Order 2 before it is obeyed. This operation takes no extra time.
Operating Speeds	Addition, Subtraction, and 46 other orders: 612 microseconds. Multiplication and Division: 21.4 milliseconds.
Negative Number Representation	Complement with respect to 2.
Accumulator	33 binary digits. There is an Auxiliary Register of 32 binary digits used with the Accumulator for double length working.
Power Requirements	2KVA.
Dimensions	The 802 is "L" shaped. One arm contains the store and arithmetic unit and the other arm comprises the control console and the input and output circuitry. The power supplies are housed in a separate free-standing cabinet.

Store and arithmetic unit	7' 4" x 2' 6" (223 x 76.2 cm)
Console and input/output	5' 2" x 2' 9" (158.5 x 83.8 cm)
Power unit	2' 9" x 2' 6" (83.8 x 76.2 cm)

All units are 2' 8" (81.3 cm) high

An 802 computer was delivered to Panellit Inc., Skokie, Illinois, during January 1959 and will become the central processing center for the Panellit 609 data logging system.

EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH (CERN) - GENEVA, SWITZERLAND

Computer. A standard Ferranti Mercury Computer has been installed in the Scientific and Technical Services Division of CERN. The computer completed its acceptance tests on 13 October 1958.

There is core storage for 1024 40-bit words and 16,384 words on magnetic drums. One word represents either a floating point binary number (10-bit exponent, 30-bit fractional part) or two single-address instructions. There are seven 10-bit B-registers and a comprehensive set of instructions for manipulating 10-bit quarter-words. Times for floating-point arithmetical instructions are:

Transfers	120 microseconds
Add or subtract	180 "
Multiply	300 "

Division is by sub-programme and takes 3.8 milliseconds. All other instructions, including those for 10-bit arithmetic, take 60 microseconds. Input and output is by 5-level punched tape, 200 characters-per-second reading, 30 characters-per-second punching. A 60 character-per-second Teletype punch is being installed.

Auxiliary equipment. A Dataplotter 1133 B system (Electronic Associates) has been delivered. This plots directly from punched tape.

Programming. The computer is available to all of the scientific staff at CERN, and most programmes have been written by the physicists or engineers using the "Autocode" scheme developed at the University of Manchester, England. Larger problems are programmed in machine code by specialized staff attached to the computer. Basic sub-programmes are permanently available on the magnetic drum, and a library of programmes on tape is being built up in collaboration with other Mercury users.

Staff. The computer is at present working one shift a day only, with occasional evening shifts. The present staff of 11 is made up as follows: 6 Mathematicians and programmers, 2 Operators, and 3 Maintenance engineers. Enlargement of staff to about 20-25 is in progress.

PROCESS CONTROL COMPUTER - FERRANTI, LTD. - LONDON, ENGLAND

The first transistor electronic digital computer designed to provide fully automatic control of many industrial processes is being developed by Ferranti Ltd. It is about the size of two small office filing cabinets and the first production models are expected to be available in 1960. At present in the prototype stage it is technically known as the PCTC (Process Control Transistor Computer). The transistor logical circuits in the computer have been thoroughly tested, and an experimental model has controlled a machine which simulates a plant process for more than 2,000 hours operation without component failure. Additional vibration and temperature tests have also been carried out to simulate the most rigorous conditions the computer is likely to meet in industrial use. The price of the new computer will probably be in the range of £20,000 - £50,000, depending on the size of the installation.

Input for the computer can be in the form of shaft rotations, voltages, pressures, temperatures and so on, which will be converted to digital form for processing by the computer. However if a very large number of input channels are required it may be necessary to add a further cabinet to house additional selection and conversion equipment. It is not possible to state precisely how many input channels can be handled on account of the variety of possible types of input. As a guide, however, it is quite feasible to think in terms of several hundred inputs of 4 or 5 different types. Both electronic and mechanical switching between input channels will be used and the corresponding selection times will vary between microseconds and milliseconds. It should be noted that each input channel can be directly addressed, and as a consequence there is no delay as would occur in a sequential scanning process.

Output will consist of different types of signals and analogue currents which can be used directly for control purposes.

In addition to the input and output of information in analogue form, numbers can be inserted manually by means of a small keyboard for direct input to the computer, and output to an electric typewriter for data logging and other purposes is available. A further use of the keyboard is for specifying the starting point of the programmes.

It may be desirable, in certain circumstances, to have punched paper tape available as a form of input and output. Should this be so, there would be no difficulty in providing the facility.

Special attention has been given to providing a comprehensive order code which is easy to use, and the result is in many ways similar to the Pegasus order code. Instructions are pegged up in the same form as they are written. Each order location on the pegboard consists of a row of six groups of eight holes. (There are 32 rows on a tray and 16 trays in the basic computer, making 512 order locations in all.) The two left hand groups refer to the function, the next to the accumulator and modifier while the last three groups specify the address.

There are four accumulators, designated A, B, C, D. Accumulator A can be used for either single or double length arithmetic, including multiplication, while B, C, and D are single length accumulators. They are mostly used for modifying and counting or for arithmetic and red tape operations, the main accumulator at the same time performing a multiplication or division.

The word length is 10 bits, but the computer can work with either 10 or 20 bit numbers depending on the accuracy required. The 10 bits, including sign, give an accuracy of 1 part in 500 and for most control applications this is sufficient; in those cases where greater accuracy is required, double length working (20 bits including sign) can be used. The order code has been designed so that both single- and double-length arithmetic can be used with equal ease.

The computer is simple to programme and the comprehensive order code which, for example, includes eleven types of jump instructions, results in compact and efficient programmes. The speed of the computer, up to 40,000 operations per second is adequate for all foreseeable control applications.

It is of course possible to store several programmes in tray form in the computer, and the operator can select any of the programmes stored in this way as and when required. If a completely different programme is required, ready pegged trays can be easily slid into position. For some applications it may be possible and consequently more economic, to have extra trays pre-pegged in this way than to increase the programme capacity of the computer.

A Library of Programmes can be stored on special perforated cards which slide into the programme trays. Thus the problem of pegging up any given programme becomes a very simple matter. Routines which are in constant use, such as those required for input and output purposes, can be held on permanently wired trays. It is likely that this latter facility will only exist for machines with extended programme space.

In some forms of programme storage, particularly magnetic devices, it is possible by the gain or loss of digits, for an instruction to become altered and so wrongly interpreted by the computer. If this should happen while a control system is operating, the consequences might be serious. For this reason pegboard programming has been used with this computer, particular attention being paid to ensuring that pegs are not dislodged by vibration.

During the running of a plant under computer control it may be necessary to examine a certain quantity at some stage in the programme. Rather than stopping the computer each time such a quantity is required, a facility has been provided to examine the contents of certain parts of the computer at a specified instruction in the programme, while the computer is still running. This is done by setting the number, or address of the instruction on the handswitches, and when that instruction is obeyed the contents of all the accumulators, the multiply/divide register and the instruction itself are displayed on indicators on the indicator panel. These indicators will remain set until the next time that the specified instruction is obeyed. This monitoring facility has been found to be indispensable when the computer is used for real time process control.

In this design Ferranti Ltd. have envisaged the computer exercising complete control over the process concerned. This should not be confused with the simpler problem of a computer used merely for data reduction providing results from which a human operator is left to decide which course of action to take. The computer will not only exercise control during the steady state of the process, but also over the complicated start up and shut down procedures.

HIPAC-I - HITACHI, LTD. - TOKYO, JAPAN

At the Central Research Laboratory, Hitachi, Ltd., a general-purpose medium-size automatic computer was started in the fall of 1956 and completed on December 23 last year. Since then various computing jobs, both at the Laboratory itself and at the various plants of Hitachi, Ltd., have been done on the machine.

The machine differs quite a bit from other automatic computers in that it uses parametrons, invented in Japan, as its primary logical element. HIPAC-I is an abbreviation of "Hitachi Parametron Automatic Computer Mark I."

Parametron Principles. The parametron is a logical element of computers invented by Eiichi Goto, of Professor Takahashi's laboratory at Tokyo University. The fundamental circuit of the parametron is a resonant circuit of frequency f including a non-linear reactance coil, which is excited at frequency 2f.

To produce non-linear reactance, various methods are conceivable, such as using a ferro-magnetic or ferro-electric material. For this application, ferro-magnetic material was used. The inductance coil has a ferrite core with a typical B-H curve. The curvatures at the right and left of the performance point determined by I_{dc} are different. That is, when the part of the curve where μ markedly changes is utilized, L can be changed by applying a high-frequency exciting current.

One example of a fundamental circuit of the parametron is as follows: Two inductances of L_1 and L_2 are connected in reverse direction so that the exciting current of frequency 2f will not act on the resonant circuit, nor the resonant current on other logical circuits via the excitation line. The input signal enters the resonant circuit by means of a coupling transformer, but if a current of frequency 2f should be flowing in the excitation line, the resonant current is amplified by the action of the parametron and a current sufficient to control the next stage is produced in the output circuit. This is because, if the exciting current is greater than the direct current I_{dc}, when the instantaneous current of inductance increases, the inductance decreases and helps the current to increase and, when the instantaneous current decreases, the exciting current grows less than I_{dc} and the inductance increases to promote the decrease of the instantaneous current.

The parametron action can be explained by a mechanical analogy. Suppose an object of mass m is suspended with a spring of stiffness s and pulled toward the right by means of a pulley with force F. First m is pushed to the left. If, when the object has swung fully to the left, F is eased a little, the object goes further to the left. And if F is pulled when the body returns to the center by means of a spring, the speed at which the object passes the center will increase and it will swing to the right. Let F be eased again to make m swing further to the right. It is then pulled as it returns to the center. By a series of this process, the amplitude of the swing will be gradually increased. If we put the natural swing frequency as f, determined by m and s, F can be eased or tensed with frequency 2f.

In brief, the easing or tensing of F is equivalent to changing the stiffness s. The oscillation equation thus is exactly the same in form for electrical and mechanical systems, where m corresponds to inductance L and s to the reciprocal of capacity C. Since, in this way, the device is oscillated by changing the parameter of the oscillation equation, it has been named "parametron."

A parametron once set oscillating continues to oscillate even if the input stops. As this makes logical process impossible, excitation must be suspended so as to halt oscillation pending the next input. Thus in the parametron circuit I_{2f} must constantly be interrupted.

In the mechanical analogy of the parametron action, two modes of oscillation are possible, one in which m is pushed to the left at the start and that in which it is pushed to the right at the start.

A parametron, starting from a small oscillation induced by an input signal alone, gradually amplifying it with the help of excitation, finally acquires a sufficiently large resonant current.

The two states are called the 0 phase and π phase, or - and + phase, respectively. If to the - phase is set the 0 of the binary system and to the + phase 1, 1-beat counting can be done.

In order to combine parametrons to form various logical circuits, the parametrons must be set oscillating by turns. They are excited intermittently as mentioned in the foregoing. The signals, however, should not travel backwards. Accordingly, the method called the three-beat excitation has been adopted. All the parametrons used are divided into three groups and each group is excited by turns. Moreover, since the oscillating output of some parametrons must become the input of others, the excitations of adjacent groups must overlap more or less. If this method of excitation is used, the output of the I-beat excited parametrons will become the input of the II-beat excited parametrons and the output of the II-beat excited parametrons the input of the III-beat excited parametrons. Repeating the series I, II, III.......I, II, III.......in this way signals of the - or + phase will be transferred.

HIPAC-I. The HIPAC-I is a stored-program type of automatic computer for scientific use. The input is by means of perforated tape. After initial input all operations proceed automatically and the results come out on a printer. For memory a 1024 word magnetic drum is used.

The HIPAC-I uses about 4,000 parametrons as the logical element. Parametrons operate somewhat slower than vacuum tubes but are far more reliable. In the HIPAC-I the slower speed of parametrons is remedied by the use of a parallel system. The net computation time of the computer proper is 4 milliseconds for addition and subtraction, 8 for multiplication, and 160 for division. For the actual computing time, however, the access time to the memory has to be taken into account in addition to those values.

The numerical values treated by the HIPAC-I are confined to those between -1 and +1 and the machine can handle 37 binary digits (that is, about 11 decimal digits) plus a sign digit at the head, which expresses whether a number is positive or negative. It works on the fixed decimal point system in which the decimal point is placed next to the sign digit.

Since it is a general-purpose computer, it can perform quite a wide range of computations depending on the program. There are 38 types of direct arithmetic and control orders in the instruction code including addition, subtraction, multiplication, and division operations. Also it is possible to modify the address in the memory designated by the program with a number set beforehand in a register, called the cycle counter, or with a number varying from moment to moment, so as to transfer to another kind of operation. This is quite convenient from the point of view of programming and is a proof of its great usefulness.

Another feature of the machine is its control circuit and its control code. By means of a group of control codes various parts of the computer can be controlled directly. Thus there is no need to make an initial order as regards to the read-in of information and the memory can be read into by direct control. The control codes can be used to perform a computation by means of tape control.

The information, on the paper tape, is first put onto the magnetic drum through the input register and accumulator in the arithmetic and control units.

The computation starts from the address designated by the start control order and proceeds in turn. The instruction code read out of the memory enters the decoder and control circuits and controls the various registers and gates. The numerical values read out of the drum enter these registers and the accumulator and the machine performs the ordered operation. The result first appears in the accumulator and is then transferred into the magnetic drum again or printed out on the printer, depending on the next order.

There are two cycle counters, which can revise the content in the address register. The designated address can also be revised by the content in the address counter.

The magnetic drum has 40 heads, and rotates at 3,600 rpm. The two heads at the left end determine the number of addresses. The position of each address is identified by counting the number of "1"'s equidistantly written in along the circumference. The remaining 38 heads work in parallel to write in and read out 38 bits. One-half of that number, 19 bits, is taken as a short word. For an instruction code, a short word is always used. The address is given to each memory location, starting from 0 and ending with 2,047. When the number of counts of the clock pulse counter and the content in the address register coincide, the gates of the flip-flop group open and the memory content at the desired address is taken out.

The HIPAC-I has the 1-1/2 address system. That is, to one operation order, one address is designated in the memory but this can also be revised. If there is no revision, the operation is performed in the order of the addresses unless otherwise specified.

Each instruction word is composed of the following three parts: 11 bits are assigned to the address of an instruction and 3 bits are used for its modification. The remaining 5 bits are assigned to the order code which specifies an operation such as addition, subtraction, multiplication, and division, etc.

Some computations performed during the last six months were:

Calculate the tension and sag of power transmission lines. For a series of long transmission wires supported by steel towers, the tension and sag of the suspended wires were computed from data such as the distances between the towers and the differences in height of the bearing points. It would have taken a human 400 days to do what the HIPAC-I completed in 15 hours.

Another task was the design of a linear accelerator. An equation, for the motion of electrons involved in this problem was solved for various initial conditions in a little over 10 hours.

In the design of nuclear reactors, the machine has been used to advantage. Computations have been made, first for a reactor of a simple shape, and then for a spherical reactor, and next for a cylindrical reactor. The calculations center on even values of partial differential equations. The machine is being used for the manipulation of experimental data for the study of the method of solving such equations.

The computer has also been used for various calculations on the numerical control of machine tools, mass spectrographic data, and even payrolls.

Among the established routines for the treatment of general problems for the machine are: the routine for simultaneous equations of the first order with five to 15 variables; routines for various methods of solving ordinary differential equations, and function subroutines for square root calculations, and for elementary functions such as trigonometric, logarithmic functions, etc.

LEO I AND II - LEO COMPUTERS, LTD. - LONDON, ENGLAND

LEO Computers Ltd. was formed to exploit the computer designed and built by the staff of J. Lyons and Co., Ltd., well known food manufacturers and caterers. Active interest in computers dates from 1947. The original computer group was formed in 1949 and forms the nucleus of the present management. LEO I is claimed to be the first computer in the world to have gone into regular daily operational use on business clerical jobs. Since January 1954 it has worked without a break on a 6-day, 2-shift schedule. The prototype LEO II went into service in 1957 and last year production models were installed for three British companies; all were fully working within 3 weeks of the equipment being dismantled in the factory. An additional 3 or 4 production models are scheduled for 1959 including one for the British Ministry of Pensions and National Insurance.

Besides manufacturing computers for sale or rent, the company undertakes a large volume of clerical computing work for other companies on contract, including production and stock control, invoicing, payroll and statistical, and group pension fund calculations. Users of this service include many large industrial concerns, insurance offices, borough councils etc. Most of the work is undertaken to a close time-table with data arriving in unprepared form one day and results being dispatched the next.

One of the 1959 production models will be installed in a service bureau in Central London in April/May 1959. This computer will be equipped with magnetic tape.

An experienced programming and consultant staff is engaged with customers applications, jobs being charted and programmed on their behalf in all cases. Charges for computing are based on the volume of results produced and not on hours worked so there is every reason for the computers to be operated to maximum efficiency.

LEO II is a binary machine using long life thermionic valves and diode logic. The word length is 19 bits, with provision for double words of 39 bits; pulse repetition rate is 525 kc., except in the mercury delay line store where it is 2.1 mc.; automatic facilities are built in for conversion to and from sterling or decimal notation by single programme instruction. There are thirteen immediate access registers including three index registers. It may be fitted with up to 4 independent input and up to 4 independent output channels, each with its own buffer. Input channels read direct from cards and both paper and magnetic tape, and output devices include on-line printers, card punches and tape recorders. Hollerith, Bull and Samastronic printers are fitted to current machines. Development of link-up for the Anelex printer is in hand. All input and output channels handle blocks of 32 words and operate concurrently with normal computing. The machine is thus exceptionally efficient on business problems where heavy loads of data and results are normal. In addition, up to four magnetic drum auxiliary stores of 16,384 words each can be fitted. The reading and writing circuits of the drum are seaprately buffered so that up to 70 transfers of a block of 32 words to or from the drums can be made per second with negligible loss of computing speed.

A similar buffering system is applied to the magnetic tape system, which uses British Decca tape decks. Half inch tape of 100 inches per second is employed and there is full automatic checking of the information written at the time of writing. Out of contact recording is used thus eliminating risk of drop-outs due to dust. Up to 8 tape decks (in 4 cabinets) can be coupled to one tape channel. Concurrent reading, writing, and computing is provided for, and two separate tape channels can be fitted.

A fully transistorized core storage system with a unit capacity of 8192 words will be available in 1960 in place of delay lines. Several units of this size can be coupled if desired.

MATHEMATICAL INSTITUTE - THE UNIVERSITY OF LIVERPOOL - LIVERPOOL, ENGLAND

The Mathematical Laboratory of the Department of Applied Mathematics in Liverpool University has been expanded by the addition of a Computer Laboratory. An English Electric DEUCE computer is being installed. The machine is a standard Deuce with 64 column punched card input and output and will have in addition punched tape input and output facilities. The machine is expected to be operational in June 1959. Mr. Andrew Young has been appointed Director of the Laboratory.

INSTITUTE FOR APPLIED MATHEMATICS - UNIVERSITY OF MAINZ - MAINZ, GERMANY

The digital computer Z 22 was put in full operation during January 1959. The computer has been operated from the beginning with a formula translating system using a restricted version of ALGOL (algorithmic language proposed by the joint ACM-GAMM committee).

ACE - NATIONAL PHYSICAL LABORATORY - TEDDINGTON, ENGLAND

The ACE or Automatic Computing Engine is the latest digital computing machine to be built at the National Physical Laboratory for the use of its Mathematics Division. This new machine, with its increased operating speed, its larger storage capacity and its many additional functional facilities, is a considerable advance as a computing tool on its predecessors, the experimental Pilot Model ACE and its engineered counterpart DEUCE.

Speed. It is not easy to assess the speed of a machine from the times taken by the elementary arithmetic and logical operations. This is particularly true of any machine with high speed stores of less than about 8,000 words on which many problems will demand the use of the backing-up store. The times taken for a few basic computations probably give as accurate a picture of the overall speed as can be obtained without a detailed study.

The zeros of a 16th degree polynomial may be obtained in an average time of 15 secs. Because of the long word length, (48 digits) accurate roots even of very ill-conditioned polynomials of this degree will be obtained. Polynomials of degrees up to about 250 may be found without using the drum store, though no sharp discontinuity in speed results from using the drum on this problem.

A set of simultaneous equations of order 30 can be solved in about 5 seconds. Sets containing no zero coefficients of orders up to 170 may be solved, the time taken varying approximately as the cube of the order but diminishing as "n" becomes large.

The solution of Poisson's equation, $\nabla^2 V = 4\pi\rho$ on a square with 400 mesh points, may be obtained in about 75 seconds. This time is for the direct solution of the finite difference equations and will give values correct to at least 10 decimals. After solving one such problem, solutions corresponding to different distributions of ρ may be obtained in about 15-20 seconds each.

Machine description. ACE is a serial computer in which numbers and instructions have 48 binary digits. The digit rate is 1.5 million per second and therefore its word time or minor cycle is 32 microseconds.

The main working store consists of 24 mercury delay lines each containing 32 words, circulating in a major cycle of 1024 microseconds. Rapid access storage is obtained by using mercury delay lines of one, two, and four words capacity. The backing store is four magnetic drums containing a total of 32,768 words.

The ACE instruction specifies a three address operation of the form 'A function B to D' where A and B are the store addresses of the operands and D is the store address to which the result of the operation is to be sent. Instructions also specify a further store address N from which the next instruction is to be extracted. The time needed to execute this operation (for single length numbers) is 32 microseconds and since each operation may be followed immediately by another, a maximum rate of operation of 30,000 per second is possible.

The instruction word uses 47 of the 48 digits divided into groups as follows:

Group	W	A	B	F	D	St	N	J	T	Ch
No. of digits	5	6	6	6	6	1	5	5	5	2

Wait Number (W) The minor cycle with which the operation will start.

Source A	Address of operand A
Source B	Address of operand B
Function (F)	Specifies one of 64 functions, selected from the following main function groups

0 Logical

1 Shift

2 Add, Subtract

3 Clear and Add, Subtract

4 Instruction Modify

5 Multiply, Divide, Standardize, Input and Output Operations

6 Multiply by small integers

7 Add, Subtract and Discriminate on Result

Destination (D)	The address to which result is sent. In addition to store addresses there are special destinations such as those for discrimination on the result (i.e., conditional transfer of control).
Stop (ST)	Allows computer to be stopped on selected instructions (Used mainly during program testing).
Next Instruction Source (N)	Store address from which next instruction will come, which may be any of the 24 long or some of the shorter delay lines.
Auxiliary Timing (J)	Used for counting prior to a transfer of control.
Timing Number (T)	The minor cycle from which the next instruction is extracted.
Characteristic (Ch)	Determines the length of the operation which may be:-
a. Single.	Transfer occurs during minor cycle W only.
b. Double.	Transfer occupies minor cycles W and W + 1.
c. Quadruple.	Transfer occupies minor cycles W, W + 1, W + 2 and W + 3.
d. Long.	Transfer starts at W and continues until T inclusive.

b., c., and d. are useful for operations concerned with multiple length numbers.

The Drum Store, the Multiplier, and the Divider are independent units. These are put into operation by the appropriate instructions and then work independently until they have completed their operation. This feature provides a parallelism of operation, since a multiplication, division, drum transfer, and a series of ordinary operations could be in progress at the same time.

The three address operation of the machine allows the multiplier and multiplicand to be selected and the multiplication process to be initiated by a single instruction. The product is formed in 14 minor cycles, i.e., 430 microseconds. The division process is similarly specified and the quotient (rounded or unrounded) is formed in approximately 1.5 milliseconds. The divider also contains an automatic standardizing process for use in floating point arithmetic operations.

The Magnetic Drum Store has a total capacity of 1024 long delay lines, i.e., about 1.5 million digits. There are four drums each having 256 tracks, each track storing the contents of one delay line. Each drum has 16 read heads and 16 write heads, the 256 tracks being obtained by moving the heads as one unit into one of 16 discrete positions. Each drum is 6.75 inches long by 5 inches diameter, allowing a linear digit packing of 100 per inch. The drum is driven by a hysteresis motor running synchronously at 12,000 rpm, and is phase corrected so as to rotate exactly once in five major cycles of the machine.

Punched card and magnetic tape equipment will be provided for input and output. The installation will initially consist of two machines. A broadside card reader, running at 450 cards per minute, and a broadside card punch running at 100 cards per minute.

In order to read or punch 80 columns of a card the computer has an 80 digit input dynamiciser and an 80 digit output staticiser.

The ACE has been designed and constructed to allow easy maintenance. Extensive marginal checking facilities are provided and the chassis units are designed to give complete accessibility to all components, valve connections etc.

The machine is housed in 10 cabinets, each having a cooled air circulation system. Each cabinet is fitted with a rising door which permits immediate access to all the 24 chassis units contained therein. The number of valve envelopes is about 6000.

X 1 - N.V. ELECTROLOGICA - AMSTERDAM, HOLLAND

The electronic computer X 1 (see Digital Computer Newsletter, July 1957) is a product of the N.V. Electrologica, Amsterdam. It has been designed and developed in close collaboration with the Mathematical Centre in Amsterdam, which has much experience in building electronic computers. It incorporates the most modern developments as, for example, transistors and magnetic cores. Both of these have the merit of giving very long service.

The X 1 can be used for arithmetical and logical operations for business or for scientific purposes; it works at the very high speed of 15,000 additions or subtractions, or 2,000 multiplications or divisions per second.

By the application of transistors instead of thermionic valves power consumption has been reduced to a few hundred watts and special cooling apparatus is no longer needed in view of the small amount of heat produced. The dimensions of the basic machine are no greater than those of an ordinary writing-desk.

The storage, consisting of magnetic cores, comprises an "active" and "dead" part, both with the same access time, so that the elaborate procedure of optimum programming is no longer needed. The active storage is used for variable data and current programmes. The dead storage is especially suitable for the storing of fixed programmes such as often occur in business administration; its component parts can readily be changed and as their cost is low, a large stock of fixed programmes ready for immediate use can be maintained at moderate cost. In consequence, the size of the more expensive active storage can be kept smaller than would otherwise be possible.

The capacity of the standard equipment, 512 words active and 512 words dead storage, can be expanded if necessary by adding supplementary units to a maximum of 32,768 words in all.

For the input of data, either punched cards or punched paper tape may be employed. Output is by means of punched cards, punched tape, or typewriter. The input capacity when tape is used is 150 characters per second, the output being 25 characters per second, except that the output capacity of the typewriter is 10 characters per second. Punched paper tape for use with the X 1 can, of course, be obtained as a by-product of suitable office machinery, e.g., typewriters, adding-and-listing, or bookkeeping machines.

For input in the form of punched cards either one or two reproducers may be coupled with the X 1 with a capacity of 7,000 cards per hour for each reproducer. A fast reading unit with an input capacity of 42,000 cards per hour may also be used in addition to the reproducers if so desired. If all three are used the input capacity is 56,000 cards per hour against an output capacity of about 14,000 cards per hour. The fast reader mentioned could also act as a sorter controlled by the X 1 computer. In linking an X 1 to a reader or reproducer, buffer storage is employed and the computer can continue calculations during card reading and card punching cycles.

Extensive facilities for operating and controlling the machine as well as for testing programmes are provided with the X 1. Notwithstanding the high degree of reliability of the X 1, both sections of the storage are provided with built-in parity controls. The reading and punching apparatus is automatically checked, and control can also be applied to typewriter output.

The price of the X 1 brings the use of an electronic computer within the reach of medium-sized enterprises. The capacity of the standard equipment can be increased by enlarging the storage capacity, and by supplementary input and output devices. It is possible, for example, to begin with the use of a small basic equipment and to expand it gradually as automation proceeds or as the volume of business grows. The machine is available either for outright purchase or on hire.

Instructions. Single address code.

Number System. Whatever the input and output medium used (punched cards, punched tape or typewriter) data are fed in or extracted in decimal form, the machine automatically transferring to and from its internal number system. The internal use of a binary system makes maximum use of the storage capacity available. The machine works with a fixed decimal point.

Word length. 27 binary digits (bits); or 26 binary digits and one sign digit. This gives a storage capacity for numbers to about 67 million. Larger numbers up to about 4.5×10^{15} can be stored by making use of two addresses. The programming of computations with such large numbers is simple.

Registers. Inter alia two registers (A and S), each of 27 bits, and an address modification register (b) of 16 bits. All these registers are available for adding and subtracting. For multiplication and division purposes the A and S registers are used as a double-length register.

Speed. Addition/subtraction, 64 microseconds; multiplication/division, 500 microseconds.

SIEMENS 2002 - SIEMENS & HALSKE AG - MUNICH, GERMANY

The Siemens 2002 is a medium-scale transistorized computer. It is a general purpose decimal machine with a word length of 12 decimals plus sign and an average speed of 2000 operations per second. Special features of the 2002 include three index registers, the use of the instruction location counter for address modifications, the automatic address substitution, and fixed and floating point operations. The 2002 has a magnetic core memory of variable size (units of 1000, 2500, 5000, and 10,000 words, up to ten memory units can be connected with the central processing unit) and a magnetic drum memory with a capacity of 10,000 words. Input and output data are handled by punched paper tape, punched cards, and magnetic tape. Magnetic core buffers for the input and output units allow the execution of input and output operations simultaneously with the operations in the central processing unit. A cathode ray tube unit permits the analogue display of output data.

Word structure. The 2002 is a decimal machine, where a decimal digit is represented by a four-digit binary number (excess-three-code). A word can be interpreted by the machine in four different ways, namely:

1. As an instruction.

±	M	R	0	0	0	S	A	A	A	A	A	I
S	1	2	3	4	5	6	7	8	9	10	11	12

Decimal 1 can be used together with the sign to mark an instruction. Decimal 2 serves several purposes. It indicates for instance, whether the result of an arithmetical or shift operation is to be rounded or not. The operation to be executed is identified by the three decimals 3 to 5. Both decimal 6 (address substitution) and 12 (index tag) are used for address modifications. The address part of the instructions is given by decimals 7 to 11.

2. As a fixed-point number, with the decimal point being assumed on the left of the most significant digit, the numbers being represented by sign and magnitude.

3. As a floating-point number, where the mantissa occupies ten (decimals 1 to 10) and the characteristic two places (decimals 11 to 12).

4. As an alpha-numerical expression with two decimal digits characterizing one alpha-numerical character.

Address modification. The usefulness of an instruction code depends greatly on the possibility of performing automatically address modifications. The 2002 allows for modifying the address part of an instruction in two different ways, namely by "address substitution" and by "index register modification," this being dependent on the contents of position 6 (substitution) and position 12 (index register modification) of the instruction word. These two types of modification can be combined and are carried out as follows:

The control unit of the 2002 include three index registers, numbered 1, 2, and 3. When executing "indexable" instructions the number in position 12 of the instruction (in the instruction register) determines the index register, the contents of which is to be added to the address part x (position 7 to 11) of the instruction. Number "4" in the index tag indicates that the contents of the instruction location counter is to be added to the address part of the instruction.

After this modification of the address part by the contents of one of the index registers or by the contents of the instruction location counter, resulting in a modified address x_1, position 6 of the instruction word is checked.

In the case the number in position 6 is "0," the instruction will be executed in the normal way with the modified address x_1. If the number in position 6 is "1," then the contents of location x_1 is read out of the memory, and positions 6 to 12 of the contents of location x_1 replace positions 6 to 12 of the instruction in the instruction register (address substitution). Then the cycle starts again with a modification of the new address part by the contents of one of the index registers or by the contents of the instruction location counter, dependent on the number in position 12 of the instruction word and so forth. The process ends, when after an index register modification resulting in a modified address x_n, position 6 of the instruction word contains "0." Following this the instruction (with address part x_n) is executed in accordance with the instruction list.

If the instruction to be executed is "not indexable," the modifications by the contents of one of the index registers are suppressed. In the case the number in position 6 is "0," the instruction will be executed in the normal way. If position 6 of the instruction word contains "1," only positions 6 to 11 of the contents of location x replace positions 6 to 11 of the instruction word in the instruction register. Then again position 6 of the instruction word is checked and so on.

Instructions and speed. The 2002 contains 80 instructions:

1. 28 instructions for arithmetic operations for fixed-point and floating-point numbers, shift operations, and other specific operations. In order to increase the calculating speed, devices are provided which produce multiples of multiplicands and divisors. Special attention

has been paid to the built-in unnormalized floating-point arithmetic, so that, roughly speaking, the precision of the results is about the same as the minimal precision of the two operands.

2. 12 jump and other control instructions, one of which, the so called subroutine jump UNT (unterprogramm) is executed as follows: supposed the instruction "UNT β" is stored in memory location α, then $\alpha + 1$ is stored automatically by this instruction in memory location β (precisely; in positions 7 to 11, all other positions being reset to 0), the next instruction to be performed will be taken from memory location $\beta + 1$. The last instruction of a subroutine is a fine example of address substitution. The (unconditional) jump instruction SPR (springe) for switching the control to memory location $\alpha + 1$ of the main program has the form "SPR 1β" where position 6 (address substitution) is equal to 1.

3. 9 instructions for index register operations, including jump instructions dependent on the contents of an index register.

4. 4 instructions for a transfer of data between drum and core memory in blocks of variable length.

5. 9 instructions for punched paper tape input and output.

6. 9 instructions for punched card input and output.

7. 7 additional instructions for magnetic tape equipment.

8. 2 instructions for a cathode ray tube output unit.

The sign of an instruction is used for program testing. Normally the sign of an instruction is not considered by the control unit. After pressing a button on the control desk, instructions with a positive sign are executed as usual, instructions with a negative sign initiate the following procedure:

1. The contents of the instruction location counter is stored in memory location 0.

2. The next instruction in sequence will be taken from memory location 1.

In memory location 1 for example there may be the start of a program printing the contents of the instruction location counter, of the accumulator a.s.f. (tracing). After the execution of this program the control can be switched back to the main program by a jump instruction "SPR 1 0," using address substitution.

All operation cycles of the 2002 are integral multiples of the "basic machine cycle," which requires 90 microseconds. One basic machine cycle is equal to the time interval necessary for adding the contents of a memory location to a number in the accumulator, including the reading out of the addend. Reading out of an instruction from the core memory, its interpretation by the control unit, and the address modification by index registers are performed in one basic machine cycle. Each address substitution requires another 90 microseconds.

The execution of an instruction is not normally controlled by the central control unit but by separate circuits of the arithmetic, input and output unit a.s.f. That means that normally reading, interpreting, and address modifications of the next instruction are performed by the central control unit simultaneously to the carrying out of the preceding instruction, provided the execution of the preceding instruction requires more than one basic machine cycle. For this reason the numbers listed under Operational Speed do not include the 90 microseconds for reading, interpreting, and address modification (by index registers) of the instruction. The next instructions are even carried out during the execution of a preceding one, if this is possible, i.e., if the control circuits for carrying out the next instruction are not used by preceding instructions. Under certain assumptions concerning the distribution of instructions of a program (25% additions, 25% multiplications, and 50% instructions for organization a.s.o.) the average speed of the 2002 amounts to 2200 operations per second for fixed point and 1850 for floating point calculations.

Operations Speeds (including reading out of the operand)

Add	fixed point	90	microseconds
Multiply	" "	1260	"
Divide	" "	3510	"
Add	floating point, normal	450	"
Multiply	" " "	1350	"
Divide	" " "	3240	"
Shift accumulator, n places		180	"

Memory. The basic memory unit is coincident current ferrite cores, and is available in units of 1000, 2500, 5000, and 10,000 words of 13 decimal digits each. Up to ten memory units can be connected with the 2002.

A drum memory (capacity 10,000 words) is attached to the ferrite core memory. Data are transferred between these two types of memory in blocks of variable length by a sequence of three instructions, giving the drum address of the first word of the block, the length of the block, and the address of the first word in the core memory. The direction of transfer is also indicated by the last instruction. The average access time per word to the drum memory is greatly reduced when transferring blocks of reasonable length. The drum revolution time is 23 milliseconds, the drum clock frequency 200 kc. The average access time to the first word of a block is about 19 milliseconds. With a word transfer of 90 microseconds, the transfer time of a block of n words is $(19 + n \cdot 0{,}09)$ milliseconds. The average transfer time of 1000 words from the drum memory to the core memory is therefore 109 milliseconds.

Input-Output. Input and output data are handled by means of punched paper tape, punched card, and magnetic tape equipment. In the case of punched paper tape, data can be read into the machine, one character per instruction, with a speed up to 200 characters per second. Results are punched on paper tape at a speed of 50 characters per second. A special built-in input routine allows the input of data without using a stored program.

The punched card control unit contains a core buffer storage for each punched card input resp. output. The buffer storage has a capacity of 80 x 12 = 960 bits, the columns (rows) of the buffer being the equivalent of the columns (rows) of the punched card. The next card is read into the input buffer storage (the contents of the output buffer storage is punched into the next card) by separate control circuits while calculating. A special column, numbered 0, is provided in the input buffer storage. Any of the 960 points of a card can be wired into any position of column 0.

Data is read out of the input buffer columnwise, beginning with column 0, continuing with column 1, 2, 3, ... Up to 12 consecutive columns can be read by one instruction, the number of columns as well as the buffer unit are indicated by the address part of the read instruction. The execution time for reading 12 columns is 540 microseconds. Data is read into the accumulator. There are two groups of instructions for reading numerical and alphanumerical characters, alphanumerical characters being represented by two decimal digits. The output buffer is filled columnwise in a similar way. If a printer is to be connected with an output buffer, the number of columns can be increased.

The magnetic tape equipment is attached to the 2002 in a similar way. The tape control unit contains one or two buffers with a capacity of 1260 x 6 bits (one character per column).

The net record on tape is read into the buffer storage (the contents of the buffer storage is written on the tape) by read (write) instructions by separate control circuits while calculating. If two buffers are installed, two records can be transferred simultaneously to or from two tape units. Up to 10 tape units can be connected with the tape control unit.

The instructions for reading data out of the tape buffer into the accumulator and for filling the tape buffer from the accumulator are the same as for the punched card buffers. The execution time for reading 12 columns is 270 microseconds. Because of the length of the tape buffer, four block transfer instructions are provided, which transfer the next n columns of tape buffer k into the core memory, beginning with memory location x resp. In like manner the data stored in the core memory beginning with memory location x, transfers into the next n columns of tape buffer k. Two instructions serve the transfer of alphanumerical and two instructions the transfer of numerical data.

Special instructions permit the sensing of the conditions of each input and output unit. Thus, for example, each input and output buffer is equipped with a flip-flop, which can be sensed and is "1" during the reading in of the next record (punched card) or during writing the contents of the buffer on tape or punched card. This makes it possible to continue the program up to the very moment the required input or output buffer gets free. The simultaneous carrying out of several input and output operations is possible because of independent control circuits for each input and output buffer.

Certain applications necessitate a digital-analogue conversion of results. A cathode ray tube unit permits the analogue display of output data, 3 decimal digits representing the x coordinate and 3 decimal digits the y coordinate. Generation of axes and diagonals is possible by one instruction. The cathode ray tube unit can be furnished with a camera unit, the transportation of the film is effected by the central processing unit.

SOCIETE D'ELECTRONIQUE ET D'AUTOMATISME - COURBEVOIE, FRANCE

The SOCIETE D'ELECTRONIQUE ET D'AUTOMATISME has just completed the installation of 2 large electronic sets for data processing (statistics and management). The first is at the INSTITUT NATIONAL de la STATISTIQUE et des ETUDES ECONOMIQUES in the establishment of general type statistics and various theoretical work. The second is for accountant work, statistics, and operational research at the COMPTOIR FRANCAIS des PRODUITS SIDERURGIQUES. Their order was placed in October 1956, and the machine was delivered October 24, 1958, and was put at the client's disposal on November 20.

These two installations consist mainly of a general purpose digital computer CAB 3030 with a recorded internal program and three or four magnetic tape equipments.

<u>CAB 3030</u>. The 3030 works with a fixed point, or floating point by program. The machine word is 32 binary digits, including one for sign, and one for parity. Negative numbers are represented by their 2's complement in order to obtain immediate notification of overflow. Instructions are single address—except for those involving accumulators, which are addressable by a second address.

The machine is serial, with 4 accumulators, and a parallel binary multiplier. The execution of one order, and the finding of the next, are carried out simultaneously.

Storage consists of magnetic drum with 128 tracks of 128 words each (16,384 words), a quick access ferrite core store with a capacity of 1,024 words. Transfers between the drum and the core store are performed automatically. A parity digit is used for control in the transfer of numbers and instructions between the different elements.

Inputs are: Ferranti photo-electric punch tape reader (200 or 400 characters per second); Flexowriter electric typewriter; and magnetic tape equipment (30 groups of 32 words or 160 characters per second).

Outputs are: Flexowriter electric typewriter; S.E.A. high speed punch at 45 characters per second; S.E.A. electronic printer "Numerograph" on microfilm (2,000 characters per second); and magnetic tape equipment.

The 3030 has 3600 valves and 35,000 diodes. Power required is 30 kilowatts.

<u>Numerograph</u>. The first Numerograph has recently been set up at the Societe MONSAVON L'OREAL. It is a fast electronic printer which enables the immediate printing on standard microfilm of the output from an electronic computer at a rate which can reach 2,000 characters per second.

A 6-bit code at the input controls two types of orders, Writing and Auxiliary.

Auxiliary orders: Capitals - Lower case - Advance - Return - Tabulation - Spacing - Colour change. The "Capital" and "Lower Case" orders enable the selection to be made from the group corresponding to a given cathode ray tube where the characters originate. The character writing orders, as well as "Advance," "Tabulation," and "Spacing" determine the position on the line. A special electronic counter performs the same part as the carriage on a typewriter. The position of each character is set on a special cathode ray tube based on the information received from the counter, and a camera placed in front of this tube registers the results. The "Spacing" order moves the film forward. The "Change colour" order changes standard type to italics, through a simple electronic anamorphosis.

Writing orders: The coded information positions the "Character" cathode ray tube spot, and in this way selects the corresponding character drawn on a transparent sighting screen. At the same time the "photographed" tube spot is placed on the line which is written at the place indicated by an internal counting and tabulation system in the "Numerograph." The 2 spots synchronously sweep the rectangle surrounding the character to be reproduced. A photoelectric cell, placed in front of the "character" cathode ray tube, transmits to the "photographed" cathode ray tube, in front of which a camera photographs the characters as they are inscribed.

At present, groups of 42 "Capital" and "Lower Case" characters are available. This can be increased to 50 for each group. The number of groups could subsequently be increased to 10 (each approximately 40 characters).

At the present both straight and italic characters are available. The introduction of auxiliary orders "Index" and "Exponent" could subsequently be envisaged, with changes in size involving whole groups of characters which would give, with the previous combinations, 3 sizes of characters.

Printing rate is 840 microseconds per character. Line spacing requires 10 milliseconds. These times could be subsequently reduced to 560 microseconds and 5 milliseconds (with a forward film speed limit of approximately 150 lines per second).

Most errors are automatically detected with the exception of character alignment faults (framing of characters on the line) which can be corrected by a simple and rapid adjustment.

TAPE MERGING EQUIPMENT - ULTRA ELECTRIC LIMITED - LONDON, ENGLAND

Ultra Electric's first entry into the Data Processing field is the fully-transistorized Tape Merging Equipment, which was shown at the London Computer Exhibition.

This equipment is primarily intended to combine the information recorded on two punched paper tapes, automatically producing a new tape which contains the result of the merging operation.

In a computer installation fitted with paper tape equipment, the Tape Merging Equipment makes it possible to exploit some of the powerful data-processing techniques which have been evolved for magnetic tapes, so that the time of using a computer can be much reduced and it becomes practical to do small and medium data-processing tasks.

Further, use of this equipment in conjunction with small computers opens up new uses for them in data-processing, and it has applications in the building-up of programmes.

A typical application is in up-dating an inventory file. The two input tapes are the brought-forward file and a tape containing amended items, the latter having been prepared on the computer. The amended items tape also contains programme instructions, which cause the equipment to copy items from either of the two input tapes or to ignore an unwanted item on the brought-forward file tape. In this way an up-dated carry-forward file is prepared as an off-line operation.

The equipment can also function as a high-speed tape copier or as a comparator, or can carry out these two functions simultaneously.

ELECTRONIC COMPUTER SECTION - THE WEIZMANN INSTITUTE OF SCIENCE - REHOVOTH, ISRAEL

WEIZAC. The memory capacity of WEIZAC (see Digital Computer Newsletter, January 1958) has been boosted by the installation of two magnetic tape handlers, using Potter 905 tape transports. The design of the tape circuits is conservative, character repetition rate being 5000 per second. These tape units were used heavily during 1958, doing mostly high-order matrix work. Present plans call for the installation of two additional tape units during 1959, doubling the character rate.

An off-line device has been built for the print-out of data from magnetic tape onto paper tape, via a magnetic drum. This unit is now undergoing final tests.

Month	Code Checking		Production		Total Computation Time		Idle Time		Scheduled Engineering and Development		Unscheduled Breakdowns	
	Hrs.	Mins.	Hrs.	Mins.	Hrs.	Mins.	Hrs.	Mins.	Hrs.	Mins.	Hrs.	Mins.
Oct. 57	78	48	252	02	330	50	5	23	64	40	20	05
Nov	67	43	309	09	376	52	5	48	70	46	8	03
Dec	106	37	332	27	439	04	5	46	58	49	14	14
Jan. 58	52	46	408	47	461	33	5	45	79	14	30	52
Feb	53	22	378	33	431	55	-	58	76	26	44	28
March	54	57	491	04	546	01	2	42	77	55	44	42
April	51	19	566	46	618	05	1	51	53	32	31	47
May	66	49	574	21	641	10	1	49	65	16	20	25
June	57	18	532	12	589	30	-	05	52	50	52	24
July	42	25	554	31	596	56	3	28	55	27	46	42
Aug	41	45	561	36	603	21	-	23	60	01	57	30
Sep	66	57	416	23	483	20	2	25	40	07	32	56
Oct	45	51	617	30	663	21	2	28	40	45	24	18
Nov	60	47	547	41	608	28	4	56	62	20	42	56
Dec	88	47	527	13	616	-	1	50	66	27	48	48
	936	11	7070	15	8006	26	45	37	924	35	520	10

Recent problems. They have solved for the first eigenvalue of a determinant of order 1078. The problem arose in connection with the determination of the energy level of the ground state of Helium. They have also been engaged in the development of methods of carrying out algebraic operations on WEIZAC. The need for this approach arose in an investigation on the propagation of a seismic pulse in a layered elastic half-space.

A recent trend in their work has been to operate with invisible equations: the equations become so long that it is impossible to write them down, so that WEIZAC increasingly operates with equations which it generates itself.

COMPONENTS

HIGH SPEED PRINTER - A. B. DICK CO. - CHICAGO, ILLINOIS

Time, Inc. has awarded a contract to A. B. Dick Company of Chicago, Illinois for 2 address-label printing systems, each capable of printing in excess of 130,000 1" x 2-3/4" labels per hour per system from digitally coded magnetic tape. Each system will include an A. B. Dick Model 910-1 label printer and a Model 940A tape reader and buffer unit.

The printer unit employs A. B. Dick Company's recently announced VIDEOGRAPH high-speed printing process (see Digital Computer Newsletter, July 1958). Principle element of the process is a special CRT having a dense matrix of fine wires permanently bonded through the face-plate instead of the conventional phosphor screen. Deflecting and modulating the electron beam across the inner side of the matrix while simultaneously transporting dielectrically coated paper past the face of the tube deposits latent charges on the paper, which are then developed by "dusting" with a powder. The visible images are then fixed on the surface.

In employing this process with digital input systems, a specially developed character generator is utilized which converts pulses into the alphanumeric video waveforms required to drive the electrostatic printing tube at writing rates that may be in excess of 20,000 characters per second.

In the Time, Inc. equipment, the tape reader and buffer unit (TRBU) will fully edit the information provided on the magnetic tape input and provide a continuous flow of data to the printer. The unit will employ a 2184 character core buffer to receive the edited information, from which the city and postal zone codes are read into a 144 character magnetic storage unit for recirculation into the output for the successive series of labels directed to the same city and zone.

Delivery of the two printing systems to the magazine's Subscription Service Division in Chicago is scheduled for June 1960. Major subcontractors include Stanford Research Institute, Cook Electric Company, and Telemeter Magnetics, Inc.

HIGH SPEED DIGITAL PLOTTER - LOCKHEED MISSILES AND SPACE DIV. - SUNNYVALE, CALIFORNIA

The High Speed Digital Plotter developed by the Computer Research Department of the Lockheed Missiles and Space Division accepts magnetic tape from IBM or Remington Rand Univac Computers and records the output on electrolytic facsimile paper. The maximum plotting rate is in excess of 4,000 data points per second, in addition to coordinate lines which are automatically generated.

Data points are recorded on facsimile paper by the passage of current from selected styli, which are arranged in a line perpendicular to the direction of paper travel. Spacing between styli is 0.01 inch. The paper feed rate and electronic timing allow marking of adjacent points 0.01 inch apart perpendicular to the stylus array. Thus, accuracy is 0.01 inch for both X and Y coordinates. Many curves, including a complete coordinate system, can be written simultaneously with this plotter.

The use of the high speed plotter has already proven of great value in speeding data reduction. It is now possible to produce completely annotated digital plots within a few hours following a test flight. With the great speed and flexibility of the plotter, it should prove to be an increasingly valuable tool for reducing data.

SYSTEMS COMPONENTS - PACKARD BELL COMPUTER CORP. - LOS ANGELES, CALIFORNIA

The Impact Prediction Systems for Vandenberg Air Force Base has been delivered. This system is based on the conversion of shaft position information into digital form, computing certain functions, and converting the output to voltages for display on analog plotters. A paper describing this system is available for anyone who wishes to write for it.

Certain systems are being made in which a Bendix G-15 general purpose computer is being tied to an analog computer. In one typical system, there are the channels of analog-to-digital information being multiplexed into the G-15, and three channels of digital-to-analog information being transferred back to the analog computer. The cost of the coupling unit is approximately $25,000. This same technique may be used on other computers, and on more elaborate systems.

SERIES RB STORAGE UNITS - TELEMETER MAGNETICS, INC. - LOS ANGELES, CALIFORNIA

The Series RB random access data storage units have been announced by Telemeter Magnetics, Inc. These memory-buffer units offer addressable random access, sequential access, or a combination of both as desired, and have a combination of features not previously realized.

High Speed	200 kc operating rate.
Long Term Reliability	Solid state active elements; conservative derating of components; advanced design and manufacturing techniques.
Wide Range of Capacities	From 256 to 1024 words of from 4 to 20 bits per word.
Random or Sequential Access	Addressable storage registers for regenerative read/write or buffer operation in a sequential non-regenerative mode.
Binary or Decimal	Either binary or binary coded decimal addressing.
Variable Input/Output	Will accept pulses or levels of either polarity and input may be changed during operation. Output is equally versatile. Accepts and emits single-ended or double-ended information.
Speed	Load or unload a word (all bits in parallel) in 5 microseconds. Random access with regenerative storage — complete cycle in 10 microseconds.
Operating Mode	Sequential loading and unloading. Random access addressing for loading and unloading or regenerative read/write. Operations can be intermixed in any manner desired without loss of speed.
Control Levels and Signals	Input and output levels may be single ended or double ended and a ONE may be represented by -5 or +5 volts as desired. Input pulses must rise to between 2 and 10 volts from a quiescent level of -5 volts. Rise time between 0.2 and 1.0 microsecond. Output pulses rise to 5 volts from a quiescent level of -5 volts. At the top of the pulse 25 milliamperes are available. Reference levels of ±5 volts are available at the output of the unit.

Clearing	Electronic clearing is provided and address register may be cleared to the all ONE or all ZERO state.
Power Required	Nominal 115 volts, 60 cps, less than 250 watts. Satisfactory operation is obtained from supply voltages between 100 and 130 volts.
Dimensions	Size depends on capacity. Largest Series RB unit approximately 30 inches high by 14 inches deep. All units are supplied for relay rack mounting.
Environment	Reliable operation between 0° and 55°C. Unaffected by humidity.
Low Cost	Series RB random access storage units are priced below most memory units designed to do only a portion of the job these memories will handle.

MISCELLANEOUS

CONTRIBUTIONS FOR DIGITAL COMPUTER NEWSLETTER

The Office of Naval Research welcomes contributions to the NEWSLETTER. Your contributions will assist in improving the contents of this newsletter, and in making it an even better medium of exchange of information, between government laboratories, academic institutions, and industry. It is hoped that the readers will participate to an even greater extent than in the past in transmitting technical material and suggestions to this Office for future issues. Because of limited time and personnel, it is often impossible for the editor to acknowledge individually all material which has been sent to this Office for publication.

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