ANHANG E-2

ASM 80-INSTRUCTION SET NUMERICAL ORDER

The following tables list the instructions that comprise the ASM 80 instruction set. As shown, each instruction requires a number of CPU cycles and Memory cycles. For an ASM 80 system employing a 0.5μsec CPU clock and a 1 μsec memory, the time required to execute an instruction is calculated as follows:

Time (inμsec) = (0.5) (CPU cycles) + (1.0) (Memory cycles)

Several conditional branch instructions can have one of two timing values. This is indicated, in the tables, by two values, for the number of CPU cycles and for the number of Memory cycles. The lower value of each should be used for the non-branch condition; the higher value for the branch condition.

CODE	MNEMONIC	CPU CYCLES	MEMORY CYCLES	NAME
00	NOP	3	1	No Operation
01	I.BC	7	3	Load Immediate Into BC
02	A.@BC	5	2	Store Accumulator Into (BC)
03	INBC	4	1	Increment BC
04	INB	4	1	Increment B
05	DCB	4	1	Decrement B
06	I.B	5	2	Load Immediate Into B
07	RLC	3	1	Rotate A Left
08				
09	ADBC	7	3	Add BC to HL
0A	@BC.A	5	2	Load (BC) Into A
0B	DCBC	4	1	Decrement BC
0C	INC	4	1	Increment C
0D	DCC	4	1	Decrement C
0E	I.C	5	2	Load Immediate Into C
0F	RRC	3	1	Rotate A Right
10				
11	I.DE	7	3	Load Immediate Into DE
12	A.@DE	5	2	Store A Into (DE)
13	INDE	4	1	Increment DE
14	IND	4	1	Increment D
15	DCD	4	1	Decrement D
16	I.D	5	2	Load Immediate Into D
17	RAL	4	1	Rotate A Left Thru Carry
18				
19	ADDE	7	3	Add DE to HL
1A	@DE.A	5	2	Load (DE) Into A
1B	DCDE	4	1	Decrement DE
1C	INE	4	1	Increment E
1D	DCE	4	1	Decrement E
1E	I.E	5	2	Load Immediate Into E
1F	RAR	4	1	Rotate A Right Thru Carry
20				
21	I.HL	7	3	Load Immediate Into HL
22	HL.@I	11	5	Store HL Direct
23	INHL	4	1	Increment HL
24	INH	4	1	Increment H
25	DCH	4	1	Decrement H
26	I.H	5	2	Load Immediate Into H
27	DAA	3	1	Decimal Adjust Accumulator
28				
29	ADHL	7	3	Add HL to HL
2A	@I.HL	11	5	Load HL Direct
2B	DCHL	4	1	Decrement HL
2C	INL	4	1	Decrement L
2D	DCL	4	1	Decrement L
2E	I.L	5	2	Load Immediate Into L
2F	CMA	3	1	Complement Accumulator
30				
31	I.SP	5	2	Load Immediate Into SP
32	A.@I	9	4	Store Accumulator Direct

CODE	MNEMONIC	CPU CYCLES	CYCLES	NAME
33	INSP	4	1	Increment SP
34	INM	7	3	Increment MEMORY
35	DCM	7	3	Decrement MEMORY
36	I.M	7	3	Load Immediate Into MEMORY
37	STC	3	1	Set Carry
38				
39	ADSP	7	3	Add SP to HL
3A	@I.A	9	4	Load Accumulator Direct
3B	DCSP	4	1	Decrement SP
3C	INA	4	1	Increment Accumulator
3D	DCA	4	1	Decrement Accumulator
3E	I.A	5	2	Load Immediate To Accumulator
3F	CMC	3	1	Complement Carry
40				
41	C.B	4	1	Load C Into B
42	D.B	4	1	Load D Into B
43	E.B	4	1	Load E Into B
44	H.B	4	1	Load H Into B
45	L.B	4	1	Load L Into B
46	M.B	5	2	Load M Into B
47	A.B	4	1	Load A Into B
48	B.C	4	1	Load B Into C
49				
4A	D.C	4	1	Load D Into C
4B	E.C	4	1	Load E Into C
4C	H.C	4	1	Load H Into C
4D	L.C	4	1	Load L Into C
4E	M.C	5	2	Load M Into C
4F	A.C	4	1	Load A Into C
50	B.D	4	1	Load B Into D
51	C.D	4	1	Load C Into D
52				
53	E.D	4	1	Load E Into D
54	H.D	4	1	Load H Into D
55	L.D	4	1	Load L Into D
56	M.D	5	2	Load M Into D
57	A.D	4	1	Load A Into D
58	B.E	4	1	Load B Into E
59	C.E	4	1	Load C Into E
5A	D.E	4	1	Load D Into E
5B				
5C	H.E	4	1	Load H Into E
5D	L.E	4	1	Load L Into E
5E	M.E	5	2	Load M Into E
5F	A.E	4	1	Load A Into E
60	B.H	4	1	Load B Into H
61	C.H	4	1	Load C Into H
62	D.H	4	1	Load D Into H
63	E.H	4	1	Load E Into H
64				
65	L.H	4	1	Load L Into H
66	M.H	5	2	Load M Into H
67	A.H	4	1	Load A Into H

CODE	MNEMONIC	CPU CYCLES	MEMORY CYCLES	NAME
68	B.L	4	1	Load B Into L
69	C.L	4	1	Load C Into L
6A	D.L	4	1	Load D Into L
6B	E.L	4	1	Load E Into L
6C	H.L	4	1	Load H Into L
6D				
6E	M.L	5	2	Load M Into L
6F	A.L	4	1	Load A Into L
70	B.M	5	2	Load B Into M
71	C.M	5	2	Load C Into M
72	D.M	5	2	Load D Into M
73	E.M	5	2	Load E Into M
74	H.M	5	2	Load H Into M
75	L.M	5	2	Load L Into M
76	HLT	6	1	Halt
77	A.M	5	2	Load A Into M
78	B.A	4	1	Load B Into A
79	C.A	4	1	Load C Into A
7A	D.A	4	1	Load D Into A
7B	E.A	4	1	Load E Into A
7C	H.A	4	1	Load H Into A
7D	L.A	4	1	Load L Into A
7E	M.A	5	2	Load M Into A
7F				
80	ADB	3	1	Add B to Accumulator
81	ADC	3	1	Add C to Accumulator
82	ADD	3	1	Add D to Accumulator
83	ADE	3	1	Add E to Accumulator
84	ADH	3	1	Add H to Accumulator
85	ADL	3	1	Add L to Accumulator
86	ADM	5	2	Add Memory to Accumulator
87	ADA	3	1	Add Accumulator to Accumulator
88	ACB	3	1	Add B to Accumulator with Carry
89	ACC	3	1	Add C to Accumulator with Car.
8A	ACD	3	1	Add D to Accumulator with Carry
8B	ACE	3	1	Add E to Accumulator with Carry
8C	ACH	3	1	Add H to Accumulator with Carry
8D	ACL	3	1	Add L to Accumulator with Carry
8E	ACM	5	2	Add Memory to Accumulator with Car
8F	ACA	3	1	Add Accumulator to Accumulator with Carry
90	SUB	3	1	Subtract B from Accumulator
91	SUC	3	1	Subtract C from Accumulator
92	SUD	3	1	Subtract D from Accumulator
93	SUE	3	1	Subtract E from Accumulator
94	SUH	3	1	Subtract H from Accumulator
95	SUL	3	1	Subtract L from Accumulator
96	SUM	5	2	Subtract Memory from Accumulator
97				
98	SBB			Subtract B from Accumulator with Borrow

CODE	MNEMONIC	CPU CYCLES	MEMORY CYCLES	NAME
99	SBC	3	1	Subtract C from Accumulator with Borrow
9A	SBD	3	1	Subtract D from Accumulator with Borrow
9B	SBE	3	1	Subtract E from Accumulator with Borrow
9C	SBH	3	1	Subtract H from Accumulator with Borrow
9D	SBL	3	1	Subtract L from Accumulator with Borrow
9E	SBM	5	2	Subtract M from Accumulator with Borrow
9F	SBA	3	1	Subtract Accumulator from Accumulator with Borrow
A0	NDB	3	1	And B with Accumulator
A1	NDC	3	1	And C with Accumulator
A2	NDD	3	1	And D with Accumulator
A3	NDE	3	1	And E with Accumulator
A4	NDH	3	1	And H with Accumulator
A5	NDL	3	1	And L with Accumulator
A6	NDM	5	2	And Memory with Accumulator
A7				
A8	XRB	3	1	Exclusive Or B with Accumulator
A9	XRC	3	1	Exclusive Or C with Accumulator
AA	XRD	3	1	Exclusive Or D with Accumulator
AB	XRE	3	1	Exclusive Or E with Accumulator
AC	XRH	3	1	Exclusive Or H with Accumulator
AD	XRL	3	1	Exclusive Or L with Accumulator
AE	XRM	5	2	Exclusive Or Memory with Accumulator
AF	XRA	3	1	Exclusive Or Accumulator with Accumulator
B0	ORB	3	1	Or B with Accumulator
B1	ORC	3	1	Or C with Accumulator
B2	ORD	3	1	Or D with Accumulator
B3	ORE	3	1	Or E with Accumulator
B4	ORH	3	1	Or H with Accumulator
B5	ORL	3	1	Or L with Accumulator
B6	ORM	5	2	Or Memory with Accumulator
B7	TST	3	1	Test Accumulator
B8	CPB	3	1	Compare B with Accumulator
B9	CPC	3	1	Compare C with Accumulator
BA	CPD	3	1	Compare D with Accumulator
BB	CPE	3	1	Compare E with Accumulator
BC	CPH	3	1	Compare H with Accumulator
BD	CPL	3	1	Compare L with Accumulator
BE	CPM	5	2	Compare Memory with Accumulator
BF	CPA	3	1	Compare Accumulator with Accumulator
C0	RFZ	4/8	1/3	Return if False Zero
C1	ST.BC	7	3	Pop Stack Into BC
C2	JFZ	7	3	Jump if False Zero
C3	JMP	7	3	Jump

CODE	MNEMONIC	CPU CYCLES	CYCLES	NAME
C4	CFZ	8/12	3/5	Call if False Zero
C5	BC.ST	8	3	Push BC Into Stack
C6	ADI	5	2	Add Immediate to Accumulator
C7	RSTØ	8	3	Restart Ø
C8	RTZ	4/8	1/3	Return if True Zero
C9	RET	7	3	Return
CA	JTZ	7	3	Jump if True Zero
CB				
CC	CTZ	8/12	3/5	Call if True Zero
CD	CAL	12	5	Call
CE	ACI	5	2	Add Immediate to Accumulator with Carry
CF	RST1	8	3	Restart 1
D0	RFC	4/8	1/3	Return if False Carry
D1	ST.DE	7	3	Pop Stack Into DE
D2	JFC	7	3	Jump if False Carry
D3	OPT	7	3	Output Instruction
D4	CFC	8/12	3/5	Call if False Carry
D5	DE.ST	8	3	Push DE Into Stack
D6	SUI	5	2	Subtract Immediate from Acc
D7	RST2	8	3	Restart 2
D8	RTC	4/8	1/3	Return if True Carry
D9				
DA	JTC	7	3	Jump if True Carry
DB	IPT	7	3	Input Instruction
DC	CTC	8/12	3/5	Call if True Carry
DD				
DE	SBI	5	2	Subtract Immediate from Accu with Borrow
DF	RST3	8	3	Restart 3
E0	RFP	4/8	1/3	Return if False Parity
E1	ST.HL	7	3	Pop Stack Into HL
E2	JFP	7	3	Jump if False Parity
E3	HL ST	13	5	Exchange HL with Stack
E4	CFP	8/12	3/5	Call if False Parity
E5	HL.ST	8	3	Push HL Into Stack
E6	NDI	5	2	And Immediate with Accumulato
E7	RST4	8	3	Restart 4
E8	RTP	4/8	1/3	Return if True Parity
E9	J@HL	4	1	Jump Indirect
EA	JTP	7	3	Jump if True Parity
EB	HL DE	3	1	Exchange HL with DE
EC	CTP	8/12	3/5	Call if True Parity
ED				
EE	XRI	5	2	Exclusive Or Immediate with Accumulator
EF	RST5	8	3	Restart 5
F0	RFS	4/8	1/3	Return if False Sign
F1	ST.A	7	3	Pop Accumulator and Flags
F2	JFS	7	3	Jump if False Sign

CODE	MNEMONIC	CPU CYCLES	MEMORY CYCLES	NAME
F3	DIN	3	1	Disable Interrupts
F4	CFS	8/12	3/5	Call if False Sign
F5	A.ST	8	3	Push Accumulator and Flags
F6	ORI	5	2	Or Immediate with Accumulator
F7	RST6	8	3	Restart 6
F8	RTS	4/8	1/3	Return if True Sign
F9	HL.SP	4	1	Load HL Into SP
FA	JTS	7	3	Jump if True Sign
FB	EIN	3	1	Enable Interrupts
FC	CTS	8/12	3/5	Call if True Sign
FD				
FE	CPI	5	2	Compare Immediate with Accumulator
FF	RST7	8	3	Restart 7

ASM 80-INSTRUCTION SET – FUNCTIONAL ORDER

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLES	NAME
		ARITHMETIC/LOGIC UNIT INSTRUCTIONS		
ACA	8F	3	1	Add Accumulator to Accumulator with Carry
ACB	88	3	1	Add B to Accumulator with Carry
ACC	89	3	1	Add C to Accumulator with Carry
ACD	8A	3	1	Add D to Accumulator with Carry
ACE	8B	3	1	Add E to Accumulator with Carry
ACH	8C	3	1	Add H to Accumulator with Carry
ACI	CE	5	2	Add Immediate to Accumulator with Carry
ACL	8D	3	1	Add L to Accumulator with Carry
ACM	8E	5	2	Add Memory to Accumulator with Carry
ADA	87	3	1	Add Accumulator to Accumulator
ADB	80	3	1	Add B to Accumulator
ADC	81	3	1	Add C to Accumulator
ADD	82	3	1	Add D to Accumulator
ADE	83	3	1	Add E to Accumulator
ADH	84	3	1	Add H to Accumulator
ADI	C6	5	2	Add Immediate to Accumulator
ADL	85	3	1	Add L to Accumulator
ADM	86	5	2	Add Memory to Accumulator
ADBC	09	7	3	Add BC to HL
ADDE	19	7	3	Add DE to HL
ADHL	29	7	3	Add HL to HL
ADSP	39	7	3	Add SP to HL
CMA	2F	3	1	Complement Accumulator
CMC	3F	3	1	Complement Carry
CPA	BF	3	1	Compare Accumulator with Accumulator
CPB	B8	3	1	Compare B with Accumulator
CPC	B9	3	1	Compare C with Accumulator
CPD	BA	3	1	Compare D with Accumulator
CPE	BB	3	1	Compare E with Accumulator
CPH	BC	3	1	Compare H with Accumulator

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLES	NAME
		ARITHMETIC/LOGIC UNIT INSTRUCTIONS		
CPI	FE	5	2	Compare Immediate with Accumulator
CPL	BD	3	1	Compare L with Accumulator
CPM	BE	5	2	Compare Memory with Accumulator
DAA	27	3	1	Decimal Adjust Accumulator
NDB	A0	3	1	And B with Accumulator
NDC	A1	3	1	And C with Accumulator
NDD	A2	3	1	And D with Accumulator
NDE	A3	3	1	And E with Accumulator
NDH	A4	3	1	And H with Accumulator
NDI	E6	5	2	And Immediate with Accumulator
NDL	A5	3	1	And L with Accumulator
NDM	A6	5	2	And Memory with Accumulator
NOP	00	3	1	No Operation
ORB	B0	3	1	Or B with Accumulator
ORC	B1	3	1	Or C with Accumulator
ORD	B2	3	1	Or D with Accumulator
ORE	B3	3	1	Or E with Accumulator
ORH	B4	3	1	Or H with Accumulator
ORI	F6	5	2	Or Immediate with Accumulator
ORL	B5	3	1	Or L with Accumulator
ORM	B6	5	2	Or Memory with Accumulator
SBA	9F	3	1	Subtract Accumulator from Accumulator with Borrow
SBB	98	3	1	Subtract B from Accumulator with Borrow
SBC	99	3	1	Subtract C from Accumulator with Borrow
SBD	9A	3	1	Subtract D from Accumulator with Borrow

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLES	NAME
		ARITHMETIC/LOGIC UNIT INSTRUCTIONS		
SBE	9B	3	1	Subtract E from Accumulator with Borrow
SBH	9C	3	1	Subtract H from Accumulator with Borrow
SBI	DE	5	2	Subtract Immediate from Accumulator with Borrow
SBL	9D	3	1	Subtract L from Accumulator with Borrow
SBM	9E	5	2	Subtract Memory from Accumulator with Borrow
STC	37	3	1	Set Carry
SUB	90	3	1	Subtract B from Accumulator
SUC	91	3	1	Subtract C from Accumulator
SUD	92	3	1	Subtract D from Accumulator
SUE	93	3	1	Subtract E from Accumulator
SUH	94	3	1	Subtract H from Accumulator
SUI	D6	5	2	Subtract Immediate from Accumulator
SUL	95	3	1	Subtract L from Accumulator
SUM	96	5	2	Subtract Memory from Accumulator
TST	B7	3	1	Test Accumulator
XRA	AF	3	1	Exclusive Or Accumulator with Accumulator
XRB	A8	3	1	Exclusive Or B with Accumulator
XRC	A9	3	1	Exclusive Or C with Accumulator
XRD	AA	3	1	Exclusive Or D with Accumulator
XRE	AB	3	1	Exclusive Or E with Accumulator
XRH	AC	3	1	Exclusive Or H with Accumulator
XRI	EE	5	2	Exclusive Or Immediate with Accumulator
XRL	AD	3	1	Exclusive Or L with Accumulator
XRM	AE	5	2	Exclusive Or Memory with Accumulator

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLES	NAME
		LOAD/STORE INSTRUCTIONS		
A.B	47	4	1	Load A into B
A.C	4F	4	1	Load A into C
A.D	57	4	1	Load A into D
A.E	5F	4	1	Load A into E
A.H	67	4	1	Load A into H
A.L	6F	4	1	Load A into L
A.M	77	5	2	Load A into M
A.@BC	02	5	2	Store Accumulato into (BC)
A.@DE	12	5	2	Store Accumulato into (DE)
A.@I	32	9	4	Store Accumulato Direct
B.A	78	4	1	Load B into A
B.C	48	4	1	Load B into C
B.D	50	4	1	Load B into D
B.E	58	4	1	Load B into E
B.H	60	4	1	Load B into H
B.L	68	4	1	Load B into L
B.M	70	5	2	Load B into M
C.A	79	4	1	Load C into A
C.B	41	4	1	Load C into B
C.D	51	4	1	Load C into D
C.E	59	4	1	Load C into E
C.H	61	4	1	Load C into H
C.L	69	4	1	Load C into L
C.M	71	5	2	Load C into M
D.A	7A	4	1	Load D into A
D.B	42	4	1	Load D into B
D.C	4A	4	1	Load D into C
D.E	5A	4	1	Load D into E
D.H	62	4	1	Load D into H
D.L	6A	4	1	Load D into L
D.M	72	5	2	Load D into M

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLES	NAME
		LOAD/STORE INSTRUCTIONS		
E.A	7B	4	1	Load E into A
E.B	43	4	1	Load E into B
E.C	4B	4	1	Load E into C
E.D	53	4	1	Load E into D
E.H	63	4	1	Load E into H
E.L	6B	4	1	Load E into L
E.M	73	5	2	Load E into M
H.A	7C	4	1	Load H into A
H.B	44	4	1	Load H into B
H.C	4C	4	1	Load H into C
H.D	54	4	1	Load H into D
H.E	5C	4	1	Load H into E
H.L	6C	4	1	Load H into L
H.M	74	5	2	Load H into M
I.A	3E	5	2	Load Immediate to Accumulator
I.B	06	5	2	Load Immediate into B
I.C	0E	5	2	Load Immediate into C
I.D	16	5	2	Load Immediate into D
I.E	1E	5	2	Load Immediate into E
I.H	26	5	2	Load Immediate into H
I.L	2E	5	2	Load Immediate into L
I.M	36	7	3	Load Immediate into Memory
I.BC	01	7	3	Load Immediate into BC
I.DE	11	7	3	Load Immediate into DE
I.HL	21	7	3	Load Immediate into HL
I.SP	31	5	2	Load Immediate into SP
L.A	7D	4	1	Load L into A
L.B	45	4	1	Load L into B
L.C	4D	4	1	Load L into C
L.D	55	4	1	Load L into D
L.E	5D	4	1	Load L into E
L.H	65	4	1	Load L into H
L.M	75	5	2	Load L into M

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLE	NAME
		JUMP INSTRUCTIONS		
JFC	D2	7	3	Jump if False Carry
JFP	E2	7	3	Jump if False Parity
JFS	F2	7	3	Jump if False Sign
JFZ	C2	7	3	Jump if False Zero
JMP	C3	7	3	Jump
JTC	DA	7	3	Jump if True Carry
JTP	EA	7	3	Jump if True Parity
JTS	FA	7	3	Jump if True Sign
JTZ	CA	7	3	Jump if Tru Zero
J@HL	E9	4	1	Jump Indirect
		CALL INSTRUCTIONS		
CAL	CD	12	5	Call
CFC	D4	8/12	3/5	Call if False Carry
CFP	E4	8/12	3/5	Call if False Parity
CFS	F4	8/12	3/5	Call if False Sign
CFZ	C4	8/12	3/5	Call if False Zero
CTC	DC	8/12	3/5	Call if True Carry
CTP	EC	8/12	3/5	Call if True Parity
CTS	FC	8/12	3/5	Call if True Sign
CTZ	CC	8/12	3/5	Call if True Zero

MNEMONIC	CODE	CPU CYCLES	MEMORY CYCLES	NAME
		RETURN INSTRUCTIONS		
RET	C9	7	3	Return
RFC	D0	4/8	1/3	Return if False Carry
RFP	E0	4/8	1/3	Return if False Parity
RFS	F0	4/8	1/3	Return if False Sign
RFZ	C0	4/8	1/3	Return if False Zero
RTC	D8	4/8	1/3	Return if True Carry
RTP	E8	4/8	1/3	Return if True Parity
RTS	F8	4/8	1/3	Return if True Sign
RTZ	C8	4/8	1/3	Return if True Zero
		RESTART INSTRUCTIONS		
RST0	C7	8	3	Restart 0
RST1	CF	8	3	Restart 1
RST2	D7	8	3	Restart 2
RST3	DF	8	3	Restart 3
RST4	E7	8	3	Restart 4
RST5	EF	8	3	Restart 5
RST6	F7	8	3	Restart 6
RST7	FF	8	3	Restart 7
		SYSTEM PROGRAMMING INPUT/OUTPUT INSTRUCTIONS		
DIN	F3	3	1	Disable Interrupts
EIN	FB	3	1	Enable Interrupts
HLT	76	6	1	Halt
IPT	DB	7	3	Input Instruction
OPT	D3	7	3	Output Instruction

ASM 80-INSTRUCTION MAP

HI→ / LOW ↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	–	–	–	–	B.D	B.H	B.M	ADB	SUB	NDB	ORB	RFZ	RFC	RFP	RFS
1	I.BC	I.DE	I.HL	I.SP	C.B	C.D	C.H	C.M	ADC	SUC	NDC	ORC	ST.BC	ST.DE	ST.HL	ST.A
2	A.@BC	A.@DE	HL.@I	A.@I	D.B	–	D.H	D.M	ADD	SUD	NDD	ORD	JFZ	JFC	JFP	JFS
3	INBC	INDE	INHL	INSP	E.B	E.D	E.H	E.M	ADE	SUE	NDE	ORE	JMP	OPT	HL\ST	DIN
4	INB	IND	INH	INM	H.B	H.D	–	H.M	ADH	SUH	NDH	ORH	CFZ	CFC	CFP	CFS
5	DCB	DCD	DCH	DCM	L.B	L.D	L.H	L.M	ADL	SUL	NDL	ORL	BC.ST	DE.ST	HL.ST	A.ST
6	I.B	I.D	I.H	I.M	M.B	M.D	M.H	HLT	ADM	SUM	NDM	ORM	ADI	SUI	NDI	ORI
7	RLC	RAL	DAA	STC	A.B	A.D	A.H	A.M	ADA	–	–	TST	RST0	RST2	RST4	RST6
8	–	–	–	–	B.C	B.E	B.L	B.A	ACB	SBB	XRB	CPB	RTZ	RTC	RTP	RTS
9	ADBC	ADDE	ADHL	ADSP	–	C.E	C.L	C.A	ACC	SBC	XRC	CPC	RET	–	J@HL	HL.SP
A	@BC.A	@DE.A	@I.HL	@I.A	D.C	D.E	D.L	D.A	ACD	SBD	XRD	CPD	JTZ	JTC	JTP	JTS
B	DCBC	DCDE	DCHL	DCSP	E.C	–	E.L	E.A	ACE	SBE	XRE	CPE	–	IPT	HL\DE	EIN
C	INC	INE	INL	INA	H.C	H.E	H.L	H.A	ACH	SBH	XRH	CPH	CTZ	CTC	CTP	CTS
D	DCC	DCE	DCL	DCA	L.C	L.E	–	L.A	ACL	SBL	XRL	CPL	CAL	–	–	–
E	I.C	I.E	I.L	I.A	M.C	M.E	M.L	M.A	ACM	SBM	XRM	CPM	ACI	SBI	XRI	CPI
F	RRC	RAR	CMA	CMC	A.C	A.E	A.L	–	ACA	SBA	XRA	CPA	RST1	RST3	RST5	RST7

I/O CODES

IPT

IFL	00
INP	01
IIN	02
FIX1	03
FIX2	04

OPT

INIT	00
SEL	01
OUT	02
DVCL	03
OFL	04
COM1	05
COM2	06
COM3	07
SBT	08
EBT	09
–	0A
ATCL	0B
SMSK	0C
BEEP	0D
CLICK	0E

CONDITION FLAGS

SZ ØAc ØPIC

ANHANG F-1

INSTALLATIONSDATEN

Abmessungen (mm)	T × B × H 630 580 425
Stellfläche	0,368 m^2
Gewicht	ca. 31 kg
Stromversorgung	220 V ± 10%, 50 Hz ± 1 Hz, 240 VA
Absicherung	5 A MT (220 V)
Wärmeabgabe	~ 200 kcal/h
Lüfterleistung	65 m^3/h
Klimabereich	+ 15 . . . + 38°C Raumtemperatur 20 — 85% rel. Feuchte
Geräuschpegel	50 dB
Schutzklasse	I
VDE-Vorschrift	0804
FTZ-Zulassungsnummer	A52-10 DEE 763