

# PDS 1020/1068 MACHINE REFERENCE HANDBOOK

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## FOREWORD

The PDS 1020 and the PDS 1068 are in essence the same machine implemented in two different configurations.

This handbook discusses the hardware characteristics of the basic machine, which is identical for both the 1020 and the 1068 configurations. Differences, where they exist, have been pointed to in the text.

It should be noted that this is basically a hardware handbook; it is designed to be used in conjunction with the Programmer's Handbook, to gain full understanding of the working of the machine. References to programming and specific instructions have been made in this handbook only where the omission would considerably obscure the meaning and usefulness of certain hardware features. This is, basically, a guide to the internal workings of the machine and a reference document for communicating with the computer on a hardware level, with particular stress on input and output interface.

#### GENERAL DESCRIPTION

The Pacific Data Systems' computer is a general purpose, digital, decimal, serial unit which is manufactured in two configurations. The PDS 1020 configuration is designed for engineering and scientific use, the 1068 configuration is designed as a modular logic unit for systems application. Disregarding various additional options, there are three principal differences between the two machines:

- 1. The PDS 1020 is a desk-mounted machine whereas the PDS 1068 is designed for rack-mounting.
- 2. The PDS 1020 has 2048 words of memory as standard equipment, where the PDS 1068 has 1024 words of memory as standard equipment.
- 3. The PDS 1020 is equipped with a paper tape reader, paper tape punch, typewriter and a numeric keyboard as input/output devices; the PDS 1068 has four input channels and three output channels designed to accommodate these devices, but does not include any of the above equipment in its standard configuration.

In all other respects, both electrical and mechanical, the two units are identical. The programming language, the input/output characteristics, the internal logic of the machine, the type of memory used, etc., all of these are common to both machines. To avoid confusion, all references to the computer, the main frame, the registers, the memory, etc., can be understood to apply equally to both machines except where either the 1020 or the 1068 is specifically mentioned by name.

The main frame of the PDS computer consists of a delay line memory, circuit boards containing the registers and other logic devices of the machine, input and output channels for communicating with external equipment, a control keyboard and panel, and associated wiring and circuitry used to interconnect the various elements.

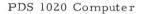
Sixteen basic logic boards are used in the machine, and these contain all the flip-flops, signal amplifiers, gates, the short delay line which houses some of the machine registers, the oscillator clock, and all the clock-associated circuitry, and other logical elements. An additional board is used optionally if the typewriter input channel is activated. In total, the machine contains a minimum of 62 flip-flops plus 4 flip-flops for every 1000 words of memory. All back-panel connections, used for connecting the various machine elements and the input/output channels, are wire-wrapped for greater reliability.

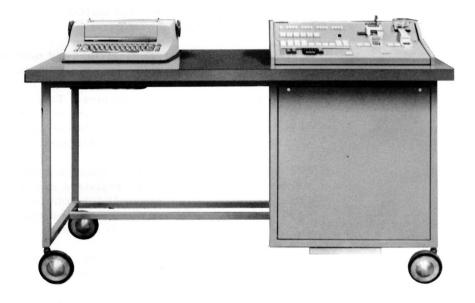
All circuits are worst-case designed to conservative end-of-life tolerances for the greatest reliability possible. Only actual component failure will cause any machine malfunction.

The machine language is both versatile and powerful, including 45 commands, not counting options, for binary and decimal arithmetic, address arithmetic, binary and decimal shifts, logic tests, etc. A built-in hardware index register provides maximum efficiency in utilizing instruction storage and in execution times. A field length register provides automatic control of variable word length arithmetic to simplify such operations.

Data is entered directly into the accumulator. Instructions may be entered into the accumulator, and then stored in memory (data mode) or entered directly into the instruction register and executed (instruction mode). The computer may, therefore, operate under control of a stored program, or receive and execute instructions from an external device such as a keyboard or paper tape. The computer can receive and execute instructions from any combination of these devices, and internal memory storage.

All basic machine arithmetic is decimal (8, 4, 2, 1 BDC) to provide the greatest simplicity of operation and assure maximum speed of processing incoming information without requiring conversion from binary to decimal and vice versa.





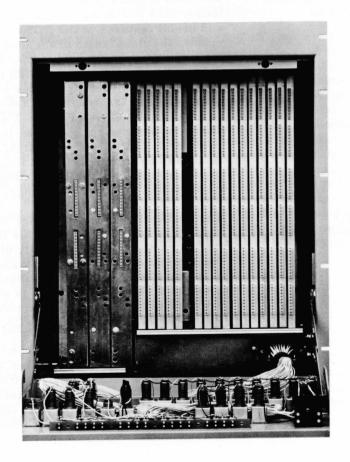
#### COMPUTER MEMORY

The PDS computer memory is a magnet-strictive delay line, operating at a 2.02 megabit/sec. rate. This type of memory was chosen because it does not carry the prohibitive cost penalty of core type storage, and is reliable, being an electrical device, and free of the mechanical problems of magnetic discs or drum storage units. The principle of delay line storage consists of introducing a time delay into electrical pulse transmissions, which, when synchronized with a pulse generating clock, can be used for dynamic storage of binary information.

The memory is worst-case designed to operate in the temperature range of  $+10^{\circ}$ C to  $+50^{\circ}$ C. Each memory module is sealed in its own atmosphere and is able to maintain this seal in altitudes up to 40,000 feet. All memory, its associated circuitry and cabling, is shielded and the entire memory is parity checked.

Basic memory capacity is 1024 words for the PDS 1068 Computer, and 2048 words for the PDS 1020 Computer. Additional memory modules of 1024 words each may be added to either machine configuration. Memory locations are addressed hexadecimally; the hexadecimal representations in the PDS computer for the decimal values 10, 11, 12, 13, 14, 15 are L, C, A, S, M, D respectively. Memory addressing is modulo the size of the particular memory unit. For example, an attempt to store data in the 1025th location of the 1024 word machine would result in the information being stored in word zero. An attempt to store information in the 2049th word of the 2K memory machine would bear the same results.

PDS with Front Panel Open. Memory Modules are at Left.



#### REGISTERS

There are seven machine registers which are of interest to the user and programmer since they affect directly the operation of the computer. These registers are numbered from 0 to 6 and are referred to in this handbook as G 0 through G 6. All seven registers can be displayed in the register display lights on the control panel, by setting the register display switch to the number of the register to be examined.

G 0 - NEXT INSTRUCTION ADDRESS The G 0 register holds the address of the next command to be executed. It is automatically incremented whenever memory instruction access is affected, and after an instruction has been executed the computer looks at this register to determine where it is to go for its next instruction. Register length is four decimal digits, plus sign, but only three of these are used in the addressing of memory since all memory addresses can be expressed in three hexadecimal digits (i.e. 4095 decimal = DDD Hexadecimal). The register is not directly addressable by programming, but may be accessed indirectly by interchanging it with the G 4 register and exchanging the G 4 register with the accumulator. The contents of this register can be read on the display lights by setting the register display switch to 0.

G 1 - INSTRUCTION REGISTER

The G l register holds the instruction currently being executed. This register is not accessible to the programmer for readout purposes. The contents of G l register can be displayed by setting the display switch to l. Register length is 4 decimal digits, plus sign.

G 2 - FIELD LENGTH REGISTER

The field length register, when loaded by the program, controls the word length used in arithmetic operations. This is one of the most important and useful features of the PDS computer. It allows the programmer to specify the field length of the data and to control this field length automatically. All memory access operations to retrieve data, store data, index data and so forth, are controlled by this register and will be performed in the exact length specified by the program. Thus if double length arithmetic is to be performed, using 8 decimal digits, the programmer has only to load the G 2 register with a 2 and proceed to write his program as though he were working with a single data word of 8 decimal digits. The register is four digits, plus sign, long, but only the least significant digit is used to determine the field length desired. The most significant three digits are ignored by all operations except when the register is first loaded or during a register exchange.

G 3 - INDEX REGISTER

The availability of the hardware index register is another important feature of the PDS computer. This feature allows maximum utilization of the instruction storage capacity of the machine, and speeds up operations for applications requiring indexing. The register is accessible to the program, and is loaded with an initial value to initiate its operation. The contents of the index register is subtracted from the operand address of every indexed instruction to arrive at a new effective address. The register consists of 4 digits and sign, but the sign is not used.

Only one command is needed to control the operations of the index register once it is loaded. The command TXH (Transfer Index High) compares the contents of the index register with the least significant digit of the field length register (G 2); if the contents of the index register is greater than or equal to this digit a transfer takes place. Simultaneously with the comparison, the same digit is also subtracted from the index register, and the

result becomes the new contents of the index register. When the least significant digit of G 4 becomes smaller than the contents of the field length register, the transfer is not executed and the computer resumes sequential operations.

The TXH instruction thus serves a triple purpose:

- 1. It decrements the index register.
- 2. It controls the number of times the indexed instructions will be executed.
- 3. It transfers control to repeat the sequence until the indexed operation has reached the specified limits.

G 4 - LINK ADDRESS

The link address register is used to store a return address when the program exits to a subroutine. When a JUMP-LINK command is executed, the register is loaded with the address of the JUMP-LINK instruction, +1. When a RETURN instruction is issued at the end of the subroutine, control is returned to this address.

G 5 - SIGN REGISTER

The G 5 register holds the sign of the accumulator. This register is also used internally by the machine for the purpose of counting iterations during multiply, divide and shift operations. The register is inaccessible by programming means but may be displayed by setting the register display switch to 5. When the register is displayed the sign of the accumulator is displayed as the tenth light from right. There is one instance where the sign of another operating register, which we will call the "B" accumulator is displayed in the ninth light from the right.

G 6 - ACCUMULATOR

G 6 is the accumulator of the PDS computer. This register is 25 decimal digits long, and is used in all arithmetic operations to hold one of the operands and the results of the computations. The register also serves as an input register for data entered into the machine or for instructions entered in the data mode. The contents of the register may be displayed by setting the display selector switch to 6. Since the register is 25 digits long, and only four decimal digits can be displayed in the display lights, the four least significant digits of the accumulator are displayed. During single word length operations, these are the digits used by the accumulator to hold the data. During multiple word length operations, the display lights show only the four least significant digits of the data in the accumulator. The 25th digit of the accumulator is an overflow and output digit. A left shift of a one bit into this digit will turn on the overflow indicator. Overflow resulting from 6 word operation will also be held in this digit. Additionally, some of the output commands utilize this digit for output to the punch and to the typewriter.

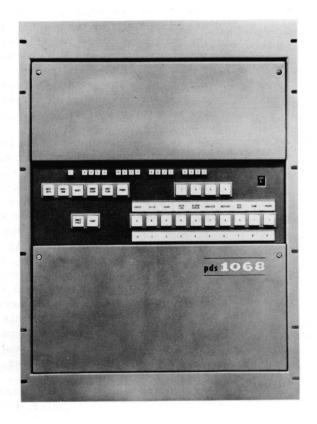
Associated with the accumulator is a second register not accessible or displayable. This register, known as the "B" accumulator, is also 25 digits long and is used by the computer to hold one of the data values during an arithmetic operation. Any of the arithmetic instructions cause this register to be loaded from the memory cell referred to in the instruction. This value is held in the "B" accumulator during execution of the arithmetic operation. The "B" accumulator also serves as the input register for instructions (except for instructions entered in the data mode). Instructions are transferred directly from the "B" accumulator to the instruction register where they are executed.

#### COMPUTER CONTROL PANEL

The PDS computer control panel contains four basic groups of switches and indicators (see photo).

- 1. Operating Controls. A group of switches and indicators used to start the machine, control operations, and display various conditions and states within the machine.
- 2. Register Display. A group of 17 lights and an associated switch used to display numerically the contents of the seven machine registers discussed previously.
- 3. Sense Switches. A group of four switches which may be tested by program to determine their setting at a given time.
- 4. Special Function Switches. A group of ten switches which may be given specific functional meaning by programming.





The PDS 1020 control panel additionally includes a numeric keyboard for entering data and instructions, and a group of switches for controlling the operations of the paper tape reader and the paper tape punch.

With the exception of the Register Display Switch, the PDS switches are of the push button type. Some of these switches have a momentary action, which terminates the moment they are released, others are of the pushpush variety, meaning that they are actuated by the first push and disengaged by the second push. Some of these switches also serve as indicators and light up when the switch is turned on or when a specified condition is detected internally by the computer.

POWER

This switch is of the push-push variety, and turns machine power on and off. The switch contains an indicator which lights up when machine power is on

OVERFLOW

This is an indicator only which illuminates when an overflow condition exists in the machine. Such a condition can be the result of an arithmetic error, such as addition, subtraction, or division yielding numbers beyond the scope of the machine, or it may be the result of planned and programmed operations. Testing of a sense switch or line by the program results in overflow if the switch is on or the line true. The overflow indicator can be tested by a Transfer on Overflow instruction, which transfers control when the indicator is on. The overflow indicator can be turned off by programming means only; it is automatically turned off by the Transfer on Overflow instruction.

ERROR CLEAR

This is an indicator which is turned on when a parity error in memory is detected. When the button is pushed, the error light will turn off, but corrective action must be taken to remedy the parity error.

RESET

Reset is a momentary switch which forces the computer into a halt or idle condition. It clears and resets all the control flip-flops and should not be used during normal machine operations. Its primary use is for maintenance and checkout purposes, but it may also be used when program control is lost due to a condition which prevents the computer from executing a command. For example, if the computer is executing an output command to an output device which is not connected or turned on, the computer will be unable to proceed; pushing Reset will release the computer from this condition and return control to the programmer.

OVERRIDE

The Override button is provided to allow the operator to interrupt the program operations manually, and to introduce changes or new commands through the keyboard. When this button is pushed, an "Input Instruction from Keyboard" command is executed after the computer completes the current instruction. The override light will come on when the computer is waiting for the keyboard instruction. After the instruction entered from the keyboard is executed, the computer returns for further instructions from the keyboard. This condition will persist until the Override button is pushed again, restoring control to the stored program. This manual interrupt capability is important in program checkout as well as during normal operations, and can be particularly useful in applications where operator judgment is used in conjunction with the computer to monitor and control an operating process. Optionally, the Override button can be actuated externally by a monitoring device, thus providing an automatic external interrupt capability.

INPUT DATA

Input data is an indicator which is turned on by the computer whenever it is ready to accept information through the keyboard channel and place it in the accumulator, that is to say whenever the keyboard channel is enabled in the data mode.

START

Start is a momentary switch and indicator used to start execution of a program when the computer is in an idle state. Start is also used to cycle the computer during a single-cycle mode. The indicator is turned on when the machine is in an idle condition.

SINGLE CYCLE

Single Cycle is the most convenient way to halt computer operations during

the normal execution of a program. When this button is actuated, the computer halts after it has executed its current instruction. As long as the Single Cycle light is on, the computer executes one instruction each time the Start button is pushed. This is a handy program checkout tool, allowing the programmer to evaluate the effects of each separate instruction. The Single Cycle mode is terminated by pushing the Single Cycle button a second time.

#### SENSE SWITCHES

Four Sense Switches are provided on the computer control panel. The switches can be set by the operator, on or off, and the setting can be tested by the program. If a tested Sense Switch is on, the computer turns on the Overflow indicator. By following the sense switch test with a Transfer on Overflow instruction, the computer will execute one sequence of instructions if the tested switch is on, another sequence if it is off.

The parallel input and output channels contain four additional Sense lines, which may be connected to external devices, or switches, and tested in the same way.

Thus eight separate switches and lines may be tested. It is also possible to test any desired combination of switches and lines, so that a total of 256 different conditions can be tested for by the computer.

The Sense Switches contain indicators, and illuminate when turned on.

#### REGISTER DISPLAY

The Register Display consists of sixteen lights plus a sign light showing the contents of the various registers. The display selector switch can be set to display any register 0 through 6, by setting the switch at the desired number of the register. When the accumulator (the number 6 register) is displayed, the least significant four digits of the contents of the accumulator and the sign of the accumulator, are displayed in the lights.

## SPECIAL FUNCTION SWITCHES

Ten special function switches are provided in the PDS computer. These switches can be used to allow the operator to execute complicated programs by the push of a button. Essentially each switch generates a transfer instruction with a different address. Thus it is possible to provide ten different sub-programs which can be used by the operator by pushing the appropriate button. This feature makes the use of the computer extremely simple in the interpretive mode, but may also be used in on-line process control or other applications to provide the operator with complete control over a process, a test procedure, or any other functional operation.

## NUMERIC KEYBOARD

The PDS 1020 Computer includes a numeric keyboard used for manual input of instructions and/or data. The keyboard contains 18 keys including the numerals from 0 - 9, the hexadecimal characters L, C, A, S, M, D, a plus key and a minus key. The keyboard may be used to input decimal data, or to input hexadecimal instructions to the computer.

## PAPER TAPE EQUIPMENT

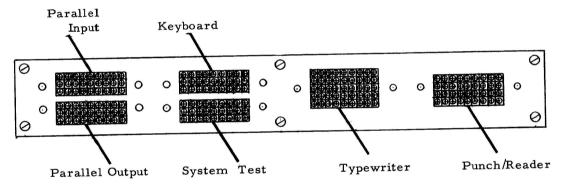
The PDS 1020 control panel contains four switches for use with paper tape equipment. An on/off switch indicator is provided for each of the paper tape units, the reader and the punch. Additionally the paper tape punch has a FEED switch used for punching leader tape, and the paper tape reader has an EJECT switch used to feed through leader tape after character reading is over.

## INPUT AND OUTPUT CHANNELS

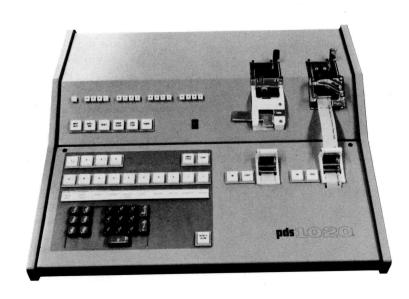
The PDS Computer is equipped with four input and three output channels. In the PDS 1020 configuration the input channels are occupied as follows: one input channel accommodates a numeric keyboard, (PDS Model No. 10-3), one input channel is occupied by a 50 ch./sec. paper tape reader (PDS Model 10-1), and one channel is left open to be used for input from the Selectric typewriter. In addition, a fourth input channel is open and may be used for parallel input of seventeen bits (4 decimal digits plus sign).

The PDS 1020 output channels are similarly occupied: one channel accommodates a 50 ch./sec. paper tape punch (PDS Model 10-2), a second channel is taken up by the Selectric 15 ch./sec. output typewriter, and a third channel is open and may be used to output seventeen bits in parallel (4 decimal digits plus sign).

In the PDS 1068 all these channels are open to be used at the discretion of the systems designer. For convenience sake, however, they will be referred to and identified by the devices which occupy these channels in the 1020 computer. That is to say, the paper tape channel for input/output, typewriter channel for input/output, parallel channel for input/output and the keyboard channel for input only.



PDS 1068 INPUT/OUTPUT CONNECTORS



PDS 1020 Control Panel, showing Keyboard, Paper Tape Reader and Paper Tape Punch.

## KEYBOARD INPUT CHANNEL

The keyboard input channel is designed to accept special purpose hexadecimal input from a numeric keyboard, PDS Model 10-3. The keyboard channel is operated by either of two computer instructions, and the input information is placed either in the accumulator (data mode), or in the instruction register (instruction mode).

#### INSTRUCTION MODE

## Input Instruction from Keyboard (0002+)

- 1. The instruction register is cleared.
- 2. Hexadecimal characters entered through the keyboard channel are placed in the instruction register.
- 3. As each character is entered it is placed in the least significant digit of the instruction register, and previously entered characters are left-shifted one digit.
- 4. A sign character when entered terminates the input.
- 5. The contents of the instruction register is then executed as an instruction.
  - a) If less than four characters were entered through the keyboard before the sign character, the computer will add leading zeros to the input.
  - b) If more than four characters are entered before the sign character is entered, the last four characters entered prior to the sign will be interpreted as the instruction.

## DATA MODE

## Input Data from Keyboard (0003+)

- The previous contents of the accumulator is left-shifted one digit.
- Hexadecimal characters are entered and placed in the accumulator.
- 3. Each hexadecimal character entered is placed in the least significant digit of the accumulator and the previous contents of the accumulator is left-shifted one digit.
- 4. A sign character, when entered through the keyboard, is placed in the sign position of the accumulator in register G 5 and terminates the input.
- 5. Input length may be variable and is terminated when a sign character is entered. The last character entered prior to the sign is located in the least significant digit of the accumulator, and preceding characters are located in digits 2 25 of the accumulator depending on the length of input; the first character entered occupies the most significant position.
  - a) If more than 25 characters are input before a sign character is entered, the first character or characters entered will be left-shifted out of the accumulator and

lost; the last 25 characters entered prior to the sign are held in the accumulator.

b) Overflow is not turned on when input characters are shifted into the 25th digit of the accumulator.

## CHARACTER FORMAT

The hexadecimal characters 0 through D (binary 0000 - 1111) and the sign characters + and - may be entered through the keyboard. The keyboard input is therefore transmitted over five data lines rather than four to accommodate the sign characters, with the fifth bit serving as a zone bit. This bit is 0 for all legitimate hexadecimal characters and is one when the character entered is a sign. Format of entries is shown below.

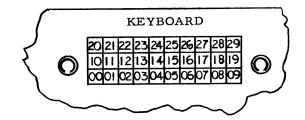
Table of Character Formats:

Hexadecimal Character	Bit Position				
	5 4 3 2 1				
0	0 0 0 0 0				
1	0 0 0 0 1				
2	00010				
3	00011				
4	0 0 1 0 0				
5	00101				
6	0 0 1 1 0				
7	0 0 1 1 1				
8	0 1 0 0 0				
. 9	0 1 0 0 1				
L	0 1 0 1 0				
С	0 1 0 1 1				
Α	0 1 1 0 0				
S	0 1 1 0 1				
M	0 1 1 1 0				
D	0 1 1 1 1				
+	10000				
-	10001				

## SPECIAL FUNCTION SWITCHES

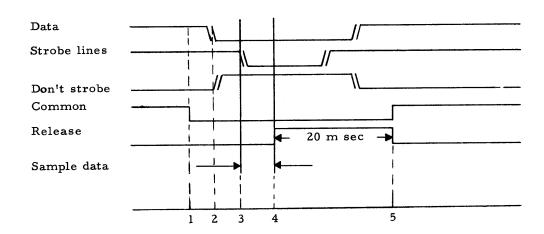
Execution by the computer of either keyboard input command will also enable the ten special function switches located on the computer control panel. When the computer executes a keyboard input instruction the operator therefore has the option of entering instructions or data through the keyboard, or actuating one of the ten special function switches. Actuation of the special function switch forces a JUMP-LINK instruction to a specified location into the instruction register of the computer. The input is then terminated and the computer will seek the next instruction at the specified location. The transfer locations are pre-determined as follows:

Switch Actuated	Transfer to Location 0 0 6
В	0 0 7
С	0 0 8
D	009
E	0 0 L
$\mathbf{F}$	0 0 C
G	0 0 A
н	0 0 S
I	0 0 M
J	0 0 D



Connector Pin		- INPUT SIGNALS -
00 01 02 03 04 18	Data Level 1 Data Level 2 Data Level 3 Data Level 4 Data Level 5 Strobe Lines	10ma. at -6V is logical "1" Ground or an open line is a logical "0"  10ma. at -6V will cause computer to sample the 7 data lines. Data lines must be settled before this signal is to be received.
20	Don't strobe	10ma. at -6V will cause computer to prepare for next character input.
		- OUTPUT SIGNALS -
07	Common	Supplies 100ma. at -6V when input instruction is executed. May be used as power supply for above input signals when switch contacts are used.
15	Release	Will pull 250ma. relay. This signal will ground a relay coil return for 20 msec after data lines have been sampled.
16 14	-24VK Ground	-l amp.
1.4	Ground	

The sequence of events for input through the keyboard channel begins with the computer executing an input instruction. This instruction enables a common line which permits a signal to be received from the keyboard. When a key is depressed by the operator, the keyboard automatically activates a relay switch which sets a "don't strobe" line false and a "strobe" line true. When the strobe line goes true, the data is sampled from the input lines and placed in the accumulator or the instruction register as called for by the instruction. The computer, when it has strobed the data lines sends a release signal, releasing the input device. Internally, a delay of 20 milliseconds occurs before the computer is ready to receive another character.



- 1. Common energized.
- 1 2. Computer waits for keyboard.
- 2 3. "Don't strobe" opening, "strobe" closing
- 3 4. Sample time.
- 4. Release signal initiated.
- 4 5. "Strobe" lines must open, "Don't Strobe" must close.

## PAPER TAPE INPUT CHANNEL

PDS paper tape input channel interface is designed to communicate with a 50 ch./sec. paper tape reader, PDS Model 10-1. Three computer commands operate the paper tape input channel, in one of three modes: 8-level input is converted by hardware to 4-bit hexadecimal characters and placed in the instruction register; 8-level input is converted by hardware to 4-bit hexadecimal characters and placed in the accumulator; 8-level input is placed directly in the accumulator without conversion.

#### INSTRUCTION INPUT

## Input Instruction from Tape (0000+)

- 1. The previous contents of the instruction register is cleared.
- 2. An 8-level character is read from tape, converted to a 4-bit hexadecimal character, and placed in the least significant digit of the instruction register.
- 3. If the preceding character was not a sign the computer reads another 8-level character from tape, converts it to a hexadecimal character, left-shifts the previous contents of the instruction register one digit, and places the new character into the least significant digit position of the instruction register.
- When a sign character is read by the computer, the input is terminated.
- 5. Upon termination of the input the contents of the instruction register is examined, interpreted as an instruction and executed immediately.
  - a) If less than four characters were read by the computer prior to its reading a sign, leading zeros will be added by the computer. If more than four characters were entered before the sign character was entered, the last four characters entered prior to the sign will be held in the instruction register as an instruction, and characters preceding these will have been shifted out of the instruction register and lost.
- 6. 8-level tape is converted to hexadecimal characters 0 through D (binary 0000 through 1111), + or -, as shown in Table A in the Appendix.

#### DATA INPUT

## Input Data from Tape (0001+)

- 1. The previous contents of the accumulator is left-shifted one digit.
- 2. The computer reads an 8-level character, converts it to a 4-bit hexadecimal digit and places it in the least significant digit of the accumulator.
- 3. If the preceding character was not a sign the accumulator is left-shifted one digit, an 8-level character is read from tape and converted to a 4-bit hexadecimal character, and the new character is placed in the least significant digit of the accumulator.

- When a sign character is read by the computer it is placed in 4. the sign position of the accumulator in register G 5 and input is terminated.
- Input length may be variable and continues until a sign charac-5. ter is read.
  - The last character entered before the sign character oca) cupies the least significant digit of the accumulator; preceding characters occupy digits 2 through 25 depending on the length of the input, with the first character entered in the most significant position.
  - If more than 25 characters were entered before the sign b) character, the last 25 characters entered will be held in the accumulator and the first character or characters will have been shifted out of the accumulator and lost.
- 8-level input is converted by hardware to 4-bit hexadecimal 6. characters 0 through D (binary 0000 through 1111) + or -, as shown in Table A in the Appendix.

## BINARY DATA INPUT

Feed Hole

Tape Direction

## Input Data Binary (0007+)

- The contents of the accumulator is left-shifted one field (4 1. decimal digits.)
- An 8-level character is read from tape and placed in the two 2. least significant digits of the accumulator. Tape level 1 occupies the least significant bit position of the accumulator and tape level 8 occupies the most significant bit position of the second digit of the accumulator. See Figure 1.
- No conversion takes place. Characters are entered as they 3. appear on tape.

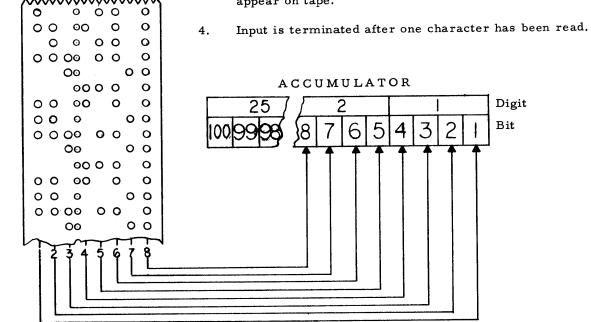
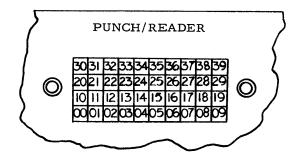
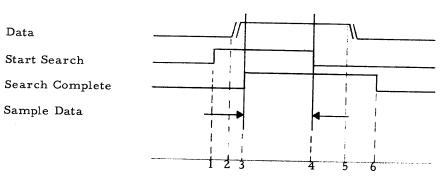


FIGURE 1.

${\tt Connector}$		
$\mathbf{Pin}$		- INPUT SIGNALS -
03 04 05 06 07 08 09	Data Level 1 Data Level 2 Data Level 3 Data Level 4 Data Level 5 Data Level 6 Data Level 7 Data Level 8	10ma. at Ground (from negative ref.) is logical "1"
01	Search Complete	10ma. at Ground (from neg. ref.) causes computer to sample data lines. Data lines must be settled before this signal is received.
		- OUTPUT SIGNALS -
00	Start Search	Ground (from -6V) when input instruction is executed. (25ma. max.)
17	Ground	(201141.)
14	-18V	
15	-18VD	Delayed 2 sec after power on.
16	-24V	*
13	+12V	



When an input from reader instruction is executed, the computer sends a "Start Search" signal to the input device. After the data lines have settled the reader sends a "Search Complete" signal to the computer. The computer then samples the data lines and turns off the "Start Search" signal. The reader turns off the "Search Complete" signal.



Maximum sample rate of non-sign characters is approximately 250/sec.

- 1. "Start Search" from computer.
- 2 3. Data placed on lines and allowed to settle.
- 3. "Search Complete" from reader.
- 3 4. Data sampled.
- 4. "Start Search" false.
- 5. "Search Complete" false.

## PAPER TAPE OUTPUT CHANNEL

The PDS computer paper tape output channel interface is designed to communicate with a 50 ch./sec. paper tape punch PDS Model 10-2. Three computer commands are used to output information to the punch in three different modes: the 8 least significant bits of the instruction register are output to the punch; the 8 least significant bits of the accumulator are output to the punch; digit 25 of the accumulator (overflow digit) is converted by hardware to 8-level code and output to the punch.

## OUTPUT FROM IN-STRUCTION REGISTER

## Output (10XX+)

- 1. The eight least significant bits of the instruction register are output to the punch; the least significant bit is output as level 1 of the tape and the most significant of the 8 bits is output as level 8.
- 2. The instruction is terminated after one character has been output.

## OUTPUT FROM ACCUMULATOR

## Output Binary (1L00+)

- 1. The 8 least significant bits of the accumulator (the two least significant digits) are output to the punch; the least significant bit of the accumulator is output as tape level 1, the most significant of the 8 bits is output as level 8. (See Figure 2.) The information is output exactly as it appears in the accumulator without conversion of any sort.
- Feed Hole The instruction is terminated after one character has been out-2. ^^^^^ 0 0 0  $\circ$ 00 00 0 0 0 00 O 000000 0 00 Oo Tape Direction ACCUMULATOR 0 O O 0 00 ΘO 0 Digit 00 00 0 5 Bit 000000 0 00 O٥ 0000 0 00 ΘO O 00 000 00 0 001

FIGURE 2.

## HEXADECIMAL OUTPUT

## Output to Punch (1200+)

Connector

29

30

17

13 14

15

16

Data Level 7

Data Level 8

Ground +12V

-18V

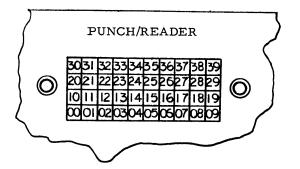
-24V

- 1. Digit 25 of the accumulator, 4-bits, is converted by hardware means to 8-level output and transmitted to the punch.
- 2. Only the hexadecimal characters 0 through D (binary 0000 through 1111) can be output by this instruction. The conversion is in accordance with the format shown in Table A in the Appendix.
- 3. The instruction is terminated after one character has been output to the punch.

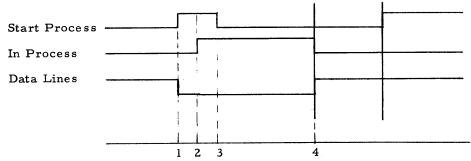
## SIGNAL LINES

#### Pin - INPUT SIGNALS -21 In Process Ground causes computer output lines to be energized. -6V causes output lines to be de-energized and releases computer from instruction. - OUTPUT SIGNALS -20 Start Process Ground (from -6 ref.) when output instruction is executed. 23 Data Level 1 24 Data Level 2 25 Data Level 3 26 Data Level 4 Supplied 10ma. at -6V for logical "1" 27 Data Level 5 28 Data Level 6 Ground or open for logical "0"

-18VD Delayed 2 sec. after power on.



The sequence of events to output a character to the punch begins with the computer executing an output instruction. The computer then sends a "Start process" signal to the punch and simultaneously places data on the output lines. The punch sends an "End process" signal to the computer, samples the lines, and releases the computer by returning the in-process line to its original state (-6 volts).



Maximum supply rate of 200/sec.

- 1. "Start process" signal from computer, and data on lines.
- 2. "In process" from punch.
- 2 4. Data sample time.
- 3. "Start process" returns to -6V.
- 4. "In process" from punch back to -6V, releases computer.

## TYPEWRITER INPUT CHANNEL

Interface to activate the typewriter input channel for input of alphanumeric information may be added to the PDS computer, at the user's option, by installing an additional logic board. The typewriter input channel will then accept alphanumeric information from a Selectric typewriter, PDS Model 10-4. One computer instruction is used to operate the typewriter input channel, and the input is to the accumulator.

#### TYPEWRITER INPUT

## Input from Typewriter (0006+)

- 1. The previous contents of the accumulator is left-shifted one field (4 decimal digits).
- 2. 17 data lines from the typewriter input channel are sampled; input from lines 1 through 16 is placed in the 16 least significant bits of the accumulator (four decimal digits). Input from line 17 is placed in the sign position of the accumulator in the register G 5 and serves as a parity check.
- 3. Input is terminated after the information has been placed in the accumulator.

#### INPUT FORMAT

Alphanumeric characters and machine functions may be input through the typewriter input channel. Alphanumeric information is transmitted over the first six data lines and placed in bits 1 through 6 of the accumulator. Machine functions are transmitted separately, 1 to a line, and placed in appropriate bit position of the accumulator as shown in the table below. In addition to alphanumeric characters and machine functions, special information regarding the input is also transmitted through the typewriter input channel and placed in bit positions 7, 8, 16 and the sign position of the accumulator in register G 5.

## Bit Position

```
1
       2
       3
               alphanumeric character
       4
               see Table B
       5
       6
       7
               parity bit
       8
               shift mode (l if u.c.)
       9
               space
      10
               CR
      11
               Tab
      12
               B. space
      13
               Index
      14
               U.C.
      15
               L.C.
      16
               EOL
sign of
accumulator
               Bit check
```

## PARITY CHECKING

Parity is checked for input of alphanumeric characters only. Bit 7 serves as a parity bit and is set to show odd parity over the first 7 bits of the accumulator. When parity is correct a 1-bit is placed in the sign position of the accumulator in register G 5. This bit is transmitted if parity is

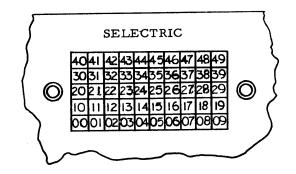
correct and is present only during input of alphanumeric characters; it is therefore possible by using a Transfer on Minus instruction to test each character input, and determine whether it is an alphanumeric character or a machine function.

SPECIAL INFORMATION

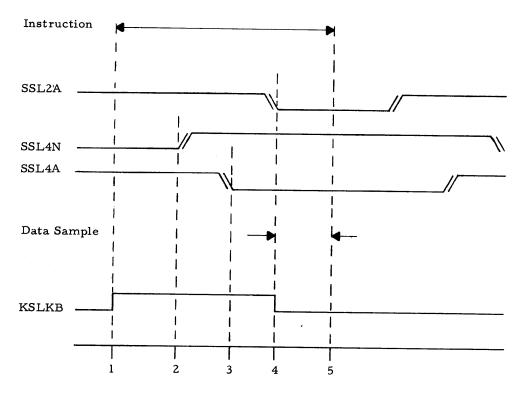
Bits 8 and 16 will be transmitted along with every input character. A 1 in the 8th bit position of the accumulator will indicate that the character input is upper case. A 1 in the 16th bit position of the accumulator indicates that the typewriter has reached the end of a line.

SIGNAL LINES

Connector	
Pin	- INPUT SIGNALS -
21	L. C. mode
23	SSL2A
26	EOL NC
27	EOL NO
28	U. C. mode
30	Keyboard unlocked
31	Keyboard locked -6 is logical "l"
33	Bit check open or ground is
34	Data 6 logical "0"
35	Data 7 (parity)
36	Data 5
37	Data 4
38	Data 3
39	Data 2
40	Data 1
42	Function 14 (tab)
43	Function 12 (space)
44	Function 13 (b. space)
45	Function 9 (C. R.)
46	Function 8 (index)
47	Function 10 (U. C.)
48	Function 11 (L. C.)
	- OUTPUT SIGNALS -
• •	W loom downlook and amoid will gupply
08	Keyboard unlock solenoid will supply
	250 ma to energize 24 volt solenoid.
19	-6V 100 ma from computer.
41	-ov 100 ma from computer.



The computer executes an input from typewriter instruction, and energizes the keyboard release solenoid. It then waits for the "Keyboard unlocked" to come true (-6V) and the "Keyboard locked" to open (ground). When the operator hits a key, the computer waits for the SSL2A signal to come true (-6V) and then samples the data lines. When the data has been read, the computer returns all signals to their initial condition.



- 1. Keyboard unlock set positive.
- 2. Keyboard locked opens.
- 3. Keyboard unlocked closes.
- 4. SSL2A closes.
- 4 5. Data sample.
- Instruction terminated.

MULTIPLE DEVICE OPERATION

The logic board which activates the typewriter input channel also provides an additional capability for input and output. When more than one device is connected to the parallel input or parallel output channel, some means are necessary to identify the device with which the computer is to communicate. This can be done by an external device, which decodes some special purpose bits in the input or the output instruction. The circuitry necessary to do this is included in the circuit board which activates the typewriter input channel.

It should be noted, however, that the board provides only the signals used for this operation. The actual decoding of the information must be accomplished by hardware external to the computer itself.

## TYPEWRITER OUTPUT CHANNEL

The typewriter output channel interface is designed to communicate with a Selectric typewriter, PDS Model 10-4. The typewriter output channel is operated by one of two computer instructions, and information is output either from the instruction register or from digit 25 of the accumulator.

## OUTPUT FROM INSTRUCTION REGISTER

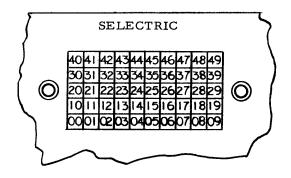
## Output (14XX+)

- 1. The least significant six bits of the instruction register (represented by XX in the instruction) are output to the typewriter.
- 2. A full set of alphanumeric characters and seven special machine functions may be output from the instruction register; the hexadecimal codes for typing letters and executing machine functions are shown in the Alphanumeric Conversion Table (Table B) in the Appendix.
- 3. The output to the typewriter is seven-level with the 7th level serving as an odd parity bit.
- 4. After the character is transmitted to the typewriter, the instruction is terminated.

## ACCUMULATOR OUTPUT

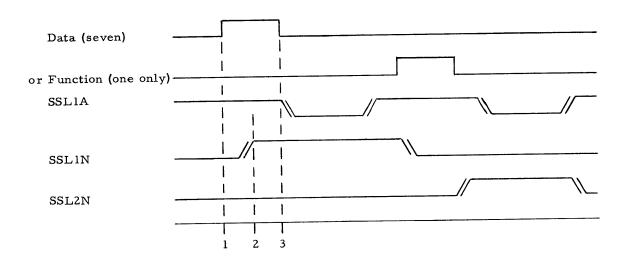
## Output to Typewriter (1630+)

- 1. Digit 25 of the accumulator (the overflow digit) is converted by hardware means into the proper code for typing the numerals 0 through 9 and the characters L, C, A, S, M, and D; the converted character is output to the typewriter.
- 2. Only the hexadecimal characters 0 through D (binary 0000 1111) may be output from digit 25 of the accumulator; plus and minus signs as well as other alphanumeric characters or machine functions must be output from the instruction register.
- 3. When the character is transmitted to the typewriter the output is terminated.
- 4. An odd parity bit is transmitted with each character.



Connector	
Pin	- OUTPUT SIGNALS -
06	Data Level 1
05	Data Level 2
04	Data Level 3
03	Data Level 4
02	Data Level 5 Each will pull a 250ma. solenoid.
00	Data Level 6 Solenoid common is tied to -24V
01	Data Level 7 J normally.
13	Function 8 (index)
12	Function 9 (C.R.)
14	Function 10 (U.C.)
15	Function 11 (L.C.)
10	Function 12 (SPACE)
11	Function 13 (B. Space)
09	Function 14 (tab)
07	-24V
19	Common will supply 100ma. at -6V if output instruction is executed. May be used as supply if
	switches are used on input lines.
	- INPUT SIGNALS -
32	SSL1A -6V (from gnd or open) releases
18	SSLIN computer from output instruction6V (from gnd or open) signals computer that data or function lines may
20	be energized. SSL2N

When the computer executes a typewriter output command, it verifies that the SSL1N signal is true and places the data on the lines. When SSL1N opens, SSL1A closes, informing the computer that the data has been sampled. The computer is then released and can proceed with its work. The SSL1N signal must come true before an additional character is output. The length of time for this depends on the letter or typewriter function executed.



- 1. Data placed on lines (7 lines).
- 2. SSL1N opens.
- 3. SSL1A closes, releasing computer.

## PARALLEL INPUT CHANNEL

The parallel input channel is left open both in the PDS 1020 and in the PDS 1068 Computers. It may be used by selected devices to input 17 bits (4 decimal digits and a sign) in parallel to the computer. The channel operates in one of three modes as dictated by the computer command being executed. Input may be placed in the instruction register and executed as an instruction (instruction mode); input may be placed in the least significant field of the accumulator (data mode); four external sense lines may be tested.

#### INSTRUCTION MODE

## Input Instruction Parallel (0004+)

- 1. The previous contents of the instruction register is cleared.
- 2. 17 data lines are sampled in parallel and their contents is placed in the instruction register.
- When the information has been placed in the instruction register input is terminated.
- 4. The computer then examines the contents of the instruction register; interprets the information as an instruction and executes it.

#### DATA MODE

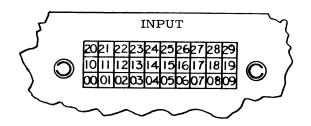
## Input Data Parallel (0005+)

- 1. The previous contents of the accumulator is left-shifted one field (4 decimal digits).
- 2. 17 data lines are sampled in parallel; the information contained in 16 of those lines is placed into the least significant field of the accumulator, 4 decimal digits, 16 bits. Information transmitted over the 17th data line is placed into the sign position of the accumulator in register G 5.
- When the information has been placed in the accumulator the instruction is terminated.

#### SENSE LINES

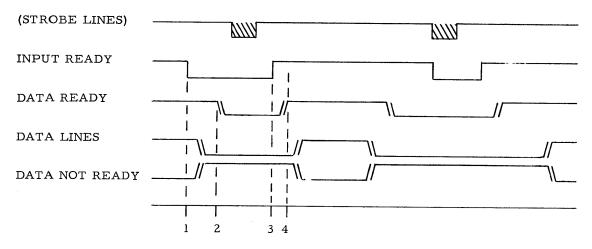
## Test Sense Switch (0X00-1)

- 1. The parallel input channel contains four external sense lines which may be set true by an external switch or device and tested under program control.
- 2. The sense lines are inter-connected to the four sense lines of the parallel output channel; a maximum of four sense lines may be tested by the computer regardless of whether the input or output sense lines are used.
- 3. The overflow indicator is turned OFF.
- 4. One or more of the sense lines is tested in accordance with information contained in digit X of the instruction; if any of the sense lines tested are true, the overflow indicator is turned ON.



Connector		·
Pin	Data Level	- INPUT SIGNALS -
Pin  00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 19 20 21 22 23 24 25	0 (1sb) 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 (msb) 16 (sign) Data Ready Data Not Ready Sense Line 5 Sense Line 6 Sense Line 6 Sense Line 8 Ground	10ma. at -6V is logical "1"  Ground is logical "0"  Unused data levels should be grounded  10ma. at -6V is logical "1"  Ground or open is logical "0"
17 18	Input Ready Input Not Ready	- OUTPUT SIGNALS - true is -6V false is ground 25 ma. max.
26 27 28	IMRIT IQCIT DSBMR	

When an input instruction is executed, the computer will send an "input ready" signal through one of the control lines of the input channel. The transmitting device, receiving this signal, will place the data on the input lines and then transmit to the computer the "Data ready" signal. The computer then samples the data lines and places the data in the accumulator or the instruction register as the case may be. As soon as the computer has accepted the data it will release the "Input ready" line, and the device must then release the "Data ready" line to terminate the input command. The input device does not need to wait for the "Input ready" signal before placing data on the lines. The data may already be on the lines, and in such a case it will be accepted by the computer as soon as the input instruction is executed. It is important however that once the data has been accepted by the computer, the device release the "Data ready" line to terminate the input instruction.



- Computer will strobe lines if DATA READY and INP instruction is created.
- 2) Device must release DATA READY after INPUT READY is released.
- 3) Maximum sample rate is approximately 200/sec.
  - 1. "Input ready" from computer.
  - 2. "Data ready" from device.
  - 3. "Input ready" released.
  - 4. "Data ready" released.

## PARALLEL OUTPUT CHANNEL

The parallel output channel of the PDS 1020 and the PDS 1068 Computers is left open, and its interface is designed to transmit 17 bits (4 decimal digits and sign) in parallel to a receiving device. Two modes of operation are possible over this channel, as dictated by the machine language command used: the least significant field of the accumulator and the sign of the accumulator may be output in parallel; four external sense lines may be tested.

## ACCUMULATOR OUTPUT

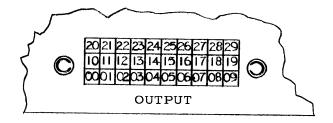
## Output Data Parallel (1800+)

- 1. The contents of the least significant field of the accumulator, bits 1 through 16 (4 decimal digits) and the sign of the accumulator from register G 5 are transmitted in parallel to a receiving device.
- 2. After the information has been transmitted the output is terminated.

#### SENSE LINES

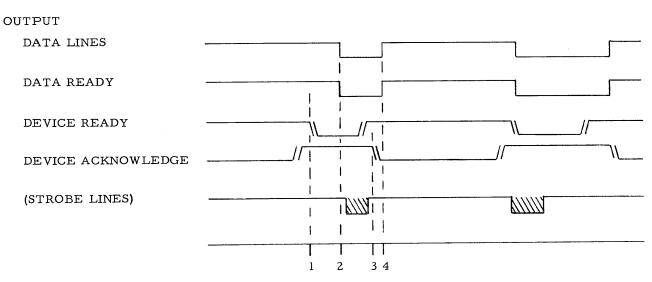
## Test Sense Switch (0X00-)

- 1. The parallel output channel contains four external sense lines which may be set true by an external switch or device and tested under program control.
- 2. The sense lines are inter-connected to the four sense lines of the parallel input channel; a maximum of four sense lines may be tested by the computer regardless of whether the input or output sense lines are used.
- 3. The overflow indicator is turned OFF.
- 4. One or more of the sense lines is tested in accordance with information contained in digit X of the instruction; if any of the sense lines tested are true, the overflow indicator is turned ON.



Connector	Data	
Pin	Level	- OUTPUT SIGNALS -
00 01 02 03 04 05 06 07 08 09 10 11	0 (1sb) 1 2 3 4 5 6 7 8 9 10 11 12 13	-6V is logical "1". ground is logical "0" 25 ma. max.
14 15	14 15 (msb)	
16	16 (sign)	J
17	Output Data Ready	7 -6V is true
18	Output Data Not Ready	
		- INPUT SIGNALS -
19	Device Ready	10ma. at -6V is true
20	Device Acknowledge	roma. at "ov is tide
21	Sense line 5	>
22	Sense line 6	Ground or open is false
23	Sense line 7	•
24	Sense line 8	1
25	Ground	

When the computer executes the output command it waits for a "Device ready" signal from the device. When signal is received, the computer places data on the lines and sends a "Data ready" signal to the device. When the device has sampled the data it sends an acknowledge signal and releases the computer.



Maximum supply rate is approximately 200/sec.

- 1. "Device ready" from device
- 2. Data and "Data ready" from computer.
- 3. Acknowledge from device.
- 4. Data lines released.

## APPENDIX TABLE A

8-LEVEL - HEXADECIMAL CONVERSION TABLE

Hes	ζ.	Tape Level		Input to Accumulator										
		8	7	6	5	4	3	2	l					
0		1	0	1	1	0	0	0	0	0	0	0	0	
1		1	0	1	1	0	0	0	1	0	0	0	1	
2		1	0	l	1	0	0	1	0	0	0	1	0	
3		1	0	1	1	0	0	1	1	0	0	1	1	
4		1	0	1	1	0	1	0	0	0	1	0	0	
5		1	0	1	1	0	1	0	l	0	1	0	1	
6		1	0	1	1	0	1	1	0	0	1	1	0	
7		1	0	1	1	0	1	1	1	0	1	1	1	
8		1	0	l	1	1	0	0	0	1	0	0	0	
9		1	0	1	1	1	0	0	1	1	0	0	1	
L		1	1	0	0	1	1	0	0	1	0	0	0	
С		1	1	0	0	0	0	1	1	l	0	1	1	
A		1	l	0	0	0	0	0	1	1	1	0	0	
S		1	1	0	1	0	0	1	1	1	1	0	1	
M		1	1	0	0	1	1	0	1	1	1	1	0	
D		1	1	0	0	0	1	0	0	1	1	1	1	
Input *	+	1	0	l	0	1	0	1	1		(+)	to ac	cumulator	Input *
Only	-	1	0	1	0	1	1	0	1		(-)		position	Only

<sup>\* +</sup> and - cannot be output from accumulator as Hexadecimal characters.

TABLE B

HEX CODE	u:c.	L.C.	HEX CODE	U.C.	L.C.
19	Α	Α	3M	Z	Z
20	В	В	3D	±	1
29	Ċ	С	3L	@	2
25	D	D	3C	#	3
2 A	E	E	35	\$	4
oc	F	F	3 A	8	5
OD	G	G	38	¢	6
24	н	Н	35	\$	7
18	I	I	39	×	8
0M	đ	J	30	(	9
28	Κ	κ	34	)	0
25	L	L	00	_	-
1D	М	М	0 L	+	=
2 L	N	N	1M	ø	!
15	0	0	0 5	?	1
0 A	Р	Р	1L	•	•
08	Q	Q	09	,	,
15	R	R	13	SPACE	
14	S	S	02	INDEX	
2 M	Т	Т	03	CAR RT	'N
2 C	U	U	06	U.C.	
10	V	٧	07	L.C.	
10	W	W	23	TAB	
2 D	×	X	17	BACK S	P.
04	Y	Y	05	:	;

## ALPHANUMERIC CODES

## SPECIFICATIONS PDS 1020/1068

## COMPUTER ORGANIZATION:

Type:

General purpose, serial, decimal, stored program.

Word Length:

4 decimal digits and sign, or multiplies up to 24

decimal digits and sign.

Memory:

Magnetostrictive delay line operating at 2.02

megabits/sec.

Capacity:

PDS 1020 - 2048 words) Expandable in modules

PDS 1068 - 1024 words) of 1024 words.

Commands:

32 basic commands not including special options.

Special Registers: Index register, word length register, jump-link

register, 24 decimal digits and sign accumulator,

Numeric display of 7 registers.

## **EXECUTION TIMES:**

LOAD/COPY

9.2 msec. avg.

ADD/SUBTRACT

9.2 msec. avg.

MULTIPLY/DIVIDE

46.0 msec. avg.

## PHYSICAL:

PDS 1020 Desk-Mounted.

PDS 1068 Rack-Mountable.

Desk Dimension: 57" long;

Dimensions: 19" wide; 26.21"

27" Wide; 30.2" high

high; 21.70" deep

Weight: 350 lbs. approx.

Weight: 200 lbs. approx.

## POWER REQUIREMENTS

PDS 1020

PDS 1068

Source: 115 VAC, 60 Cycle, Single

Phase

115 VAC, 60 Cycle, Single Phase

Consumption: 475 Watts

275 Watts

Convenience Outlet: Up to 10 Amps. Max. -----

## INPUT-OUTPUT:

## PDS 1020

Input:

Soroban Keyboard

Royal McBee Series 500, 50 ch./sec. Paper Tape

IBM Selectric Typewriter (optional)

17 bit Parallel Input (open)

## INPUT-OUTPUT: - Continued

## PDS 1020

Output:

Royal McBee Series 500, 50 ch./sec. Paper Tape

Reader

IBM Selectric, 15 ch./sec. Typewriter Printer

17 bit Parallel Output (open)

#### PDS 1068

Input:

3 Serial Channels

Max. Input Rate

250 ch./sec.

Max. Putaway Rate

(enter and store)

20 words/sec. (4 decimal

digits and sign per word)

1 Parallel Input Channel (17 bits)

Max. Putaway Rate

50 words/sec. (4 decimal

digits and sign per word)

Output:

Punch Channel:

12 words/sec. (4 decimal

digits and sign per word)

Parallel Channel:

50 words/sec. (4 decimal

digits and sign per word)

Typewriter Channel: Limited by device speed.

Solid State Printed
Board Circuits - Worst
Case Designed.

